TAS5404-Q1：具有负载突降保护和 I²C 诊断功能的 26W 模拟单端输入 4 通道 D 类放大器

1 特性

- TAS5404-Q1 - 单端输入
- 四通道 D 类功率放大器
- 4 个模拟输入，4 个桥接式负载 (BTL) 功率输出
- 在 10% 总谐波失真 (THD) + N 上典型输出功率
  - 14.4V 时，每通道 26W (4Ω)
  - 14.4V 时，每通道 45W (2Ω)
- 针对高电流应用，通道可被并联 (PBTL)
- THD + N < 0.02%，1kHz，为 4Ω 负载提供 1W
- 采用获专利的喀哒声和噼啪声降噪技术
  - 具有增益斜波控制的软静音
  - 共模斜波修整
- 已获专利的 AM 干扰避免
- 已获专利的逐周期电流限制
- 75dB 高电源抑制比 (PSRR)
- 针对器件配置和控制的 4 地址 I²C 串行接口
- 通道增益：12dB，20dB，26dB，32dB
- 负载诊断功能：
  - 输出打开和短接负载
  - 输出到电源和输出到接地短接
  - 已获专利的高频扬声器侦测
- 保护和监控功能：
  - 短路保护
  - 负载突降保护达 50V
  - 可承受偶然的接地开路和电源开路
  - 已获专利的在音乐播放的同时进行输出直流电平侦测
  - 过热保护
  - 过压和欠压条件
  - 削波检测
- 64 引脚四方扁平无引线 (QFP) (PHD) 功率封装（散热片朝上）
- 设计用于汽车电磁兼容性 (EMC) 要求
- 符合 AEC-Q100 标准
- 通过 ISO9000:2002 TS16949 认证
- -40°C 至 105°C 环境温度范围

2 应用

功能丰富且系统配置高，要求音频功率放大器具有高效性的原始设备制造商 (OEM) 或零售音响主机

3 说明

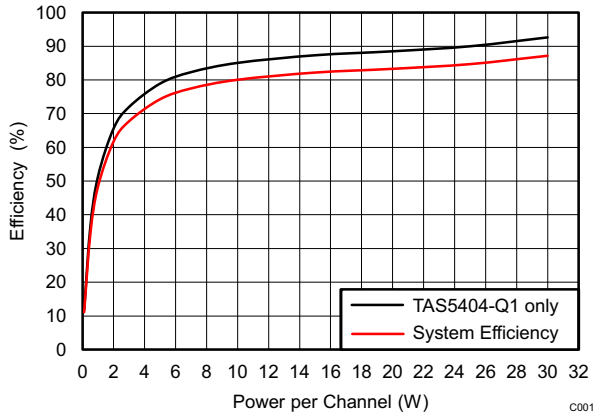
TAS5404-Q1 器件是一款四通道 D 类音频放大器，设计用于汽车类音响主机。 TAS5404-Q1 器件用于应用电路时，可在 14.4VDC 电源供电下以低于 1% 的 THD+N 为 4Ω 负载提供四通道 20W 的输出功率。 其输入配置为模拟单端接口。 此器件采用获专利的脉宽调制 (PWM) 拓扑，相比传统的线性放大器解决方案，效率和音频性能得到了显著提升。 在正常音乐播放条件下，效率和音频性能的提升使得放大器功耗降低了 10%。 该器件整合了 OEM 应用所需的全部功能。 内置负载诊断功能可用于检测和诊断断开连接的扬声器，帮助缩短制造过程中所需的测试时间。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TAS5404-Q1	HTQFP (64)	14.00mm x 14.00mm

(1) 如需了解所有可用封装，请参见数据表末尾的可订购产品附录。

效率
4Ω 负载条件下的四通道



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4 修订历史记录

Changes from Original (August 2015) to Revision A **Page**

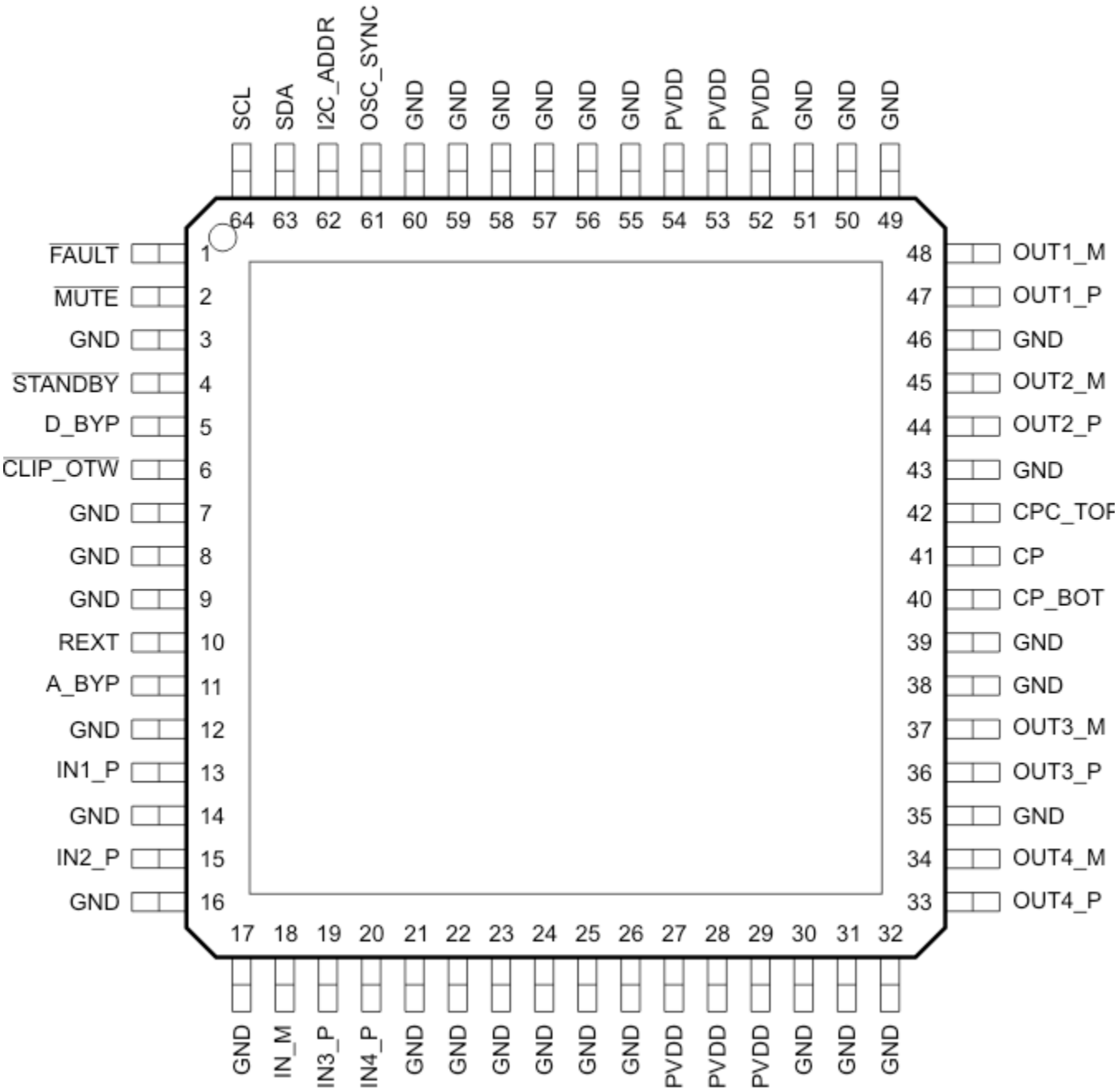
- 已更改 数据表状态，从产品预览改为量产数据。 ... 1

5 Device Comparison Table

PART NUMBER	MINIMUM POWER SUPPLY VOLTAGE	MAXIMUM POWER SUPPLY VOLTAGE
TAS5404-Q1	5.6 VDC	18 VDC
TAS5414C-Q1	6 VDC	24 VDC

6 Pin Configuration and Functions

Package
64-Pin QFP
(Top View)



Pin Functions

NAME	PIN	TYPE(1)	DESCRIPTION
A_BYP	11	PBY	Bypass pin for the AVDD analog regulator
$\overline{\text{CLIP\_OTW}}$	6	DO	Reports CLIP, OTW, or both. Also reports tweeter detection during tweeter mode. Open-drain
CP	41	CP	Top of main storage capacitor for charge pump (bottom goes to PVDD)
CPC_BOT	40	CP	Bottom of flying capacitor for charge pump
CPC_TOP	42	CP	Top of flying capacitor for charge pump
D_BYP	5	PBY	Bypass pin for DVDD regulator output
$\overline{\text{FAULT}}$	1	DO	Global fault output (open drain): UV, OV, OTSD, OCSD, DC
GND	3, 7, 8, 9, 12, 14, 16, 17, 21, 22, 23, 24, 25, 26, 30, 31, 32, 35, 38, 39, 43, 46, 49, 50, 51, 55, 56, 57, 58, 59, 60	GND	Ground
I2C_ADDR	62	AI	I^2C address bit
IN1_P	13	AI	Non-inverting analog input for channel 1
IN2_P	15	AI	Non-inverting analog input for channel 2
IN3_P	19	AI	Non-inverting analog input for channel 3
IN4_P	20	AI	Non-inverting analog input for channel 4
IN_M	18	ARTN	Signal return for the four analog channel inputs
$\overline{\text{MUTE}}$	2	AI	Gain ramp control: mute (low), play (high)
OSC_SYNC	61	DI/DO	Oscillator input from master or output to slave amplifiers
OUT1_M	48	PO	– polarity output for bridge 1
OUT1_P	47	PO	+ polarity output for bridge 1
OUT2_M	45	PO	– polarity output for bridge 2
OUT2_P	44	PO	+ polarity output for bridge 2
OUT3_M	37	PO	– polarity output for bridge 3
OUT3_P	36	PO	+ polarity output for bridge 3
OUT4_M	34	PO	– polarity output for bridge 4
OUT4_P	33	PO	+ polarity output for bridge 4
PVDD	27, 28, 29, 52, 53, 54	PWR	PVDD supply
REXT	10	AI	Precision resistor pin to set analog reference
SCL	64	DI	I^2C clock input from system I^2C master
SDA	63	DI/DO	I^2C data I/O for communication with system I^2C master
$\overline{\text{STANDBY}}$	4	DI	Active-low STANDBY pin. Standby (low), power up (high)

(1) DI = digital input, DO = digital output, AI = analog input, ARTN = analog signal return, PWR = power supply, PBY = power bypass, PO = power output, GND = ground, CP = charge pump.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
PVDD	DC supply voltage range	Relative to GND	–0.3	18	V
$PVDD_{MAX}$	DC supply voltage range	t ≤ 60 s exposure	–0.3	30	V
$PVDD_{PULSED}$	Pulsed supply voltage range	t ≤ 100 ms exposure	–1	50	V
$PVDD_{RAMP}$	Supply voltage ramp rate			15	V/ms
I_{PVDD}	Externally imposed dc supply current per PVDD or GND pin			±12	A
I_{PVDD_MAX}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms		17	A
I_O	Maximum allowed DC current per output pin			±13.5	A
I_{O_MAX}(2)	Pulsed output current per output pin (single pulse)	t < 100 ms		±17	A
I_{IN_MAX}	Maximum current, all digital and analog input pins(3)	DC or pulsed		±1	mA
I_{MUTE_MAX}	Maximum current on $\overline{MUTE}$ pin	DC or pulsed		±20	mA
I_{IN_ODMAX}	Maximum sink current for open-drain pins			7	mA
V_{LOGIC}	Input voltage range for pin relative to GND (SCL, SDA, I2C_ADDR pins)	Supply voltage range: 6 V < PVDD < 18 V	–0.3	6	V
V_{MUTE}	Voltage range for $\overline{MUTE}$ pin relative to GND	Supply voltage range: 6 V < PVDD < 18 V	–0.3	7.5	V
$V_{STANDBY}$	Input voltage range for $\overline{STANDBY}$ pin	Supply voltage range: 6 V < PVDD < 18 V	–0.3	5.5	V
V_{OSC_SYNC}	Input voltage range for OSC_SYNC pin relative to GND	Supply voltage range: 6 V < PVDD < 18 V	–0.3	3.6	V
V_{GND}	Maximum voltage between GND pins			±0.3	V
$V_{AIN\_AC\_MAX}$	Maximum ac-coupled input voltage(3), analog input pins	Supply voltage range: 6 V < PVDD < 18 V		1.9	Vrms
T_J	Maximum operating junction temperature range		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum- rated conditions for extended periods may affect device reliability.
(2) Pulsed current ratings are maximum survivable currents externally applied to the TAS5404-Q1 device. The TAS5404-Q1 device can encounter high currents during reverse-battery, fortuitous open-ground, and fortuitous open-supply fault conditions.
(3) See the *Application Information* section for information on analog input voltage and ac coupling.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2500	V
		Charged device model (CDM), per AEC Q100-011 PHD Package	Corner pins excluding SCL	±750	V
			All pins (including SCL) except CP and CP_Top	±600	
			CP and CP_Top pins	±400	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
$PVDD_{OP}$	DC supply voltage range relative to GND		6	14.4	18	V
V_{AIN}(2)	Analog audio input signal level (TAS5414C-Q1)	AC-coupled input voltage	0		0.25–1(3)	Vrms
T_A	Ambient temperature		–40		105	°C

(1) The *Recommended Operating Conditions* table specifies only that the TAS5404-Q1 device is functional in the given range. See the *Electrical Characteristics* table for specified performance limits.
(2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB
(3) Maximum recommended input voltage is determined by the gain setting.

Recommended Operating Conditions(1) (continued)

			MIN	NOM	MAX	UNIT
T_J	Junction temperature	An adequate heat sink is required to keep T_J within specified range.	–40		115	°C
R_L	Nominal speaker load impedance		2	4		Ω
V_{PU}	Pullup voltage supply (for open-drain logic outputs)		3	3.3 or 5	5.5	V
R_{PU_EXT}	External pullup resistor on open-drain logic outputs	Resistor connected between open-drain logic output and V_{PU} supply	10		50	kΩ
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
R_{I2C_ADD}	Total resistance of voltage divider for I^2C address slave 1 or slave 2, connected between D_BYP and GND pins		10		50	kΩ
R_{REXT}	External resistance on REXT pin	1% tolerance required	19.8	20	20.2	kΩ
C_{D_BYP} , C_{A_BYP}	External capacitance on D_BYP and A_BYP pins		10		120	nF
C_{OUT}	External capacitance to GND on OUT_X pins			150	680	nF
C_{IN}	External capacitance to analog input pin in series with input signal			0.47		µF
C_{FLY}	Flying capacitor on charge pump		0.47	1	1.5	µF
C_P	Charge pump capacitor	50 V required for load dump	0.47	1	1.5	µF
C_{MUTE}	$\overline{\text{MUTE}}$ pin capacitor		100	220	1000	nF
$C_{OSCSYNC\_MAX}$	Allowed loading capacitance on OSC_SYNC pin			75		pF

7.4 Thermal Information

THERMAL METRIC(1)		TAS5404-Q1	UNIT
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance	1.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	This TAS5404-Q1 device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. Refer to the *Thermal Consideration* section.	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see Figure 20)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All four channels in MUTE mode		170	220	mA
I_{PVDD_Hi-Z}		All four channels in Hi-Z mode		93		
I_{PVDD_STBY}	PVDD standby current	STANDBY mode, $T_J \le 85°C$		2	10	µA
OUTPUT POWER						
P_{OUT}	Output power per channel	4 Ω, THD+N ≤ 1%, 1 kHz, T_c = 75°C		20		W
		4 Ω, THD+N = 10%, 1 kHz, T_c = 75°C	25	26		
		4 Ω, square wave, 1 kHz, T_c = 75°C		43		
		2 Ω, THD+N = 1%, 1 kHz, T_c = 75°C		38		
		2 Ω, THD+N = 10%, 1 kHz, T_c = 75°C	40	45		
		2 Ω, square wave, 1 kHz, T_c = 75°C		70		
EFF_P	Power efficiency	4 channels operating, 20-W output power/ch, L = 10 µH, $T_J \le 85°C$		90%		
AUDIO PERFORMANCE						
V_{NOISE}	Noise voltage at output	Zero input, and A-weighting		60	100	µV
	Channel crosstalk	P = 1 W, f = 1 kHz, enhanced crosstalk enabled through I^2C (reg. 0x10)	70	85		dB
$CMRR_{5424}$	Common-mode rejection ratio (TAS5424C-Q1)	f = 1 kHz, 1 Vrms referenced to GND, G = 26 dB	60	75		dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz	60	75		dB
THD+N	Total harmonic distortion + noise	P = 1 W, f = 1 kHz		0.02%	0.1%	
f_S	Switching frequency	Switching frequency selectable for AM interference avoidance	336	357	378	kHz
			392	417	442	
			470	500	530	
R_{AIN}	Analog input resistance	Internal shunt resistance on each input pin	63	85	106	kΩ
V_{IN_CM}	Common-mode input voltage	AC-coupled common-mode input voltage (zero differential input)		1.3		Vrms
V_{CM_INT}	Internal common-mode input bias voltage	Internal bias applied to IN_M pin		3.3		V
G	Voltage gain (V_O/V_{IN})	Source impedance = 0 Ω, gain measurement taken at 1 W of power per channel	11	12	13	dB
			19	20	21	
			25	26	27	
			31	32	33	
G_{CH}	Channel-to-channel variation	Any gain commanded	–1	0	1	dB
PWM OUTPUT STAGE						
$R_{DS(on)}$	FET drain-to-source resistance	Not including bond wire resistance, T_J = 25°C		65	90	mΩ
V_{O_OFFSET}	Output offset voltage	Zero input signal, G = 26 dB		±10	±50	mV
PVDD OVERVOLTAGE (OV) PROTECTION						
V_{OV_SET}	PVDD overvoltage shutdown set		24.6	26.4	28.2	V
V_{OV_CLEAR}	PVDD overvoltage shutdown clear		24.4	25.9	27.4	V
PVDD UNDERVOLTAGE (UV) PROTECTION						
V_{UV_SET}	PVDD undervoltage shutdown set		4.9	5.3	5.5	V
V_{UV_CLEAR}	PVDD undervoltage shutdown clear		6.2	6.6	6.9	V
AVDD						
V_{A_BYP}	A_BYP pin voltage			6.5		V
$V_{A\_BYP\_UV\_SET}$	A_BYP UV voltage			4.8		V
$V_{A\_BYP\_UV\_CLEAR}$	Recovery voltage A_BYP UV			5.3		V
DVDD						
V_{D_BYP}	D_BYP pin voltage			3.3		V
POWER-ON RESET (POR)						
V_{POR}	PVDD voltage for POR	I^2C active above this voltage			4	V
V_{POR_HY}	PVDD recovery hysteresis voltage for POR			0.1		V

Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see Figure 20)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REXT						
V_{REXT}	Rext pin voltage			1.27		V
CHARGE PUMP (CP)						
V_{CPUV_SET}	CP undervoltage			4.8		V
V_{CPUV_CLEAR}	Recovery voltage for CP UV			4.9		V
OVERTEMPERATURE (OT) PROTECTION						
T_{OTW1_CLEAR}	Junction temperature for overtemperature warning		96	112	128	°C
T_{OTW1_SET} / T_{OTW2_CLEAR}			106	122	138	°C
T_{OTW2_SET} / T_{OTW3_CLEAR}			116	132	148	°C
T_{OTW3_SET} / T_{OTSD_CLEAR}			126	142	158	°C
T_{OTSD}	Junction temperature for overtemperature shutdown		136	152	168	°C
T_{FB}	Junction temperature for overtemperature foldback	Per channel	130	150	170	°C
CURRENT LIMITING PROTECTION						
I_{LIM}	Current limit (load current)		8.5			A
OVERCURRENT (OC) SHUTDOWN PROTECTION						
I_{MAX}	Maximum current (peak output current)	Any short to supply, ground, or other channels	9.8			A
TWEETER DETECT						
I_{TH_TW}	Load-current threshold for tweeter detect		330	445	560	mA
I_{LIM_TW}	Load-current limit for tweeter detect			2.1		A
STANDBY MODE						
V_{IH}	$\overline{\text{STANDBY}}$ input voltage for logic-level high		2			V
V_{IL}	$\overline{\text{STANDBY}}$ input voltage for logic-level low				0.7	V
I_{STBY}	$\overline{\text{STANDBY}}$ pin current			0.1	0.2	μA
MUTE MODE						
G_{MUTE}	Output attenuation	$\overline{\text{MUTE}}$ pin ≤ 0.5 V for 200 ms or I^2C Mute Enabled		100		dB
DC OFFSET DETECT						
$V_{TH\_DC\_TOL}$	DC offset detect threshold tolerance			25%		
t_{DCD}	DC offset detect step-response time for four channels				5.3	s
CLIP_OTW REPORT						
$V_{OH\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V to 5.5 V	2.4			V
$V_{OL\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level low (open-drain logic output)				0.5	V
$t_{DELAY\_CLIPDET}$	$\overline{\text{CLIP\_OTW}}$ signal delay when output clipping detected				20	μs
FAULT REPORT						
V_{OH_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V to 5.5 V	2.4			V
V_{OL_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level low (open-drain logic output)				0.5	

Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see Figure 20)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN, SHORT DIAGNOSTICS						
R_{S2P}, R_{S2G}	Maximum resistance to detect a short from OUT pin(s) to PVDD or ground				200	Ω
R_{OPEN_LOAD}	Minimum load resistance to detect open circuit	Including speaker wires	300	740	1300	Ω
$R_{SHORTED\_LOAD}$	Maximum load resistance to detect short circuit	Including speaker wires	0.5	1	1.5	Ω
I^2C ADDRESS DECODER						
$t_{LATCH\_I2CADDR}$	Time delay to latch I^2C address after POR			300		µs
V_{I2C_ADDR}	Voltage on I2C_ADDR pin for address 0	Connect to GND	0%	0%	15%	V_{D_BYP}
	Voltage on I2C_ADDR pin for address 1	External resistors in series between D_BYP and GND as a voltage divider	25%	35%	45%	
	Voltage on I2C_ADDR pin for address 2		55%	65%	75%	
	Voltage on I2C_ADDR pin for address 3	Connect to D_BYP	85%	100%	100%	
I^2C						
t_{HOLD_I2C}	Power-on hold time before I^2C communication	$\overline{\text{STANDBY}}$ high		1		ms
f_{SCL}	SCL clock frequency				400	kHz
V_{IH}	SCL pin input voltage for logic-level high	R_{PU_I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL}	SCL pin input voltage for logic-level low		–0.5		1.1	V
V_{OH}	SDA pin output voltage for logic-level high	I^2C read, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.4			V
V_O	SDA pin output voltage for logic-level low	I^2C read, 3-mA sink current			0.4	V
V_{IH}	SDA pin input voltage for logic-level high	I^2C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL}	SDA pin input voltage for logic-level low	I^2C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	–0.5		1.1	V
C_I	Capacitance for SCL and SDA pins				10	pF
OSCILLATOR						
V_{OH}	OSC_SYNC pin output voltage for logic-level high	I2C_ADDR pin set to MASTER mode	2.4			V
V_{OL}	OSC_SYNC pin output voltage for logic-level low				0.5	V
V_{IH}	OSC_SYNC pin input voltage for logic-level high	I2C_ADDR pin set to SLAVE mode	2			V
V_{IL}	OSC_SYNC pin input voltage for logic-level low				0.8	V
f_{OSC_SYNC}	OSC_SYNC pin clock frequency	I2C_ADDR pin set to MASTER mode, f_S = 500 kHz	3.76	4	4.24	MHz
		I2C_ADDR pin set to MASTER mode, f_S = 417 kHz	3.13	3.33	3.63	
		I2C_ADDR pin set to MASTER mode, f_S = 357 kHz	2.68	2.85	3	

7.6 Timing Requirements for I²C Interface Signals

over recommended operating conditions (unless otherwise noted)

		MIN	NOM	MAX	UNIT
t_r	Rise time for both SDA and SCL signals			300	ns
t_f	Fall time for both SDA and SCL signals			300	ns
$t_{w(H)}$	SCL pulse duration, high	0.6			µs
$t_{w(L)}$	SCL pulse duration, low	1.3			µs.
$t_{su(2)}$	Setup time for START condition	0.6			µs
$t_{h(2)}$	START condition hold time until generation of first clock pulse	0.6			µs
$t_{su(1)}$	Data setup time	100			ns
$t_{h(1)}$	Data hold time	0 (1)			ns
$t_{su(3)}$	Setup time for STOP condition	0.6			µs
C_B	Load capacitance for each bus line			400	pF

(1) The TAS5404-Q1 device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

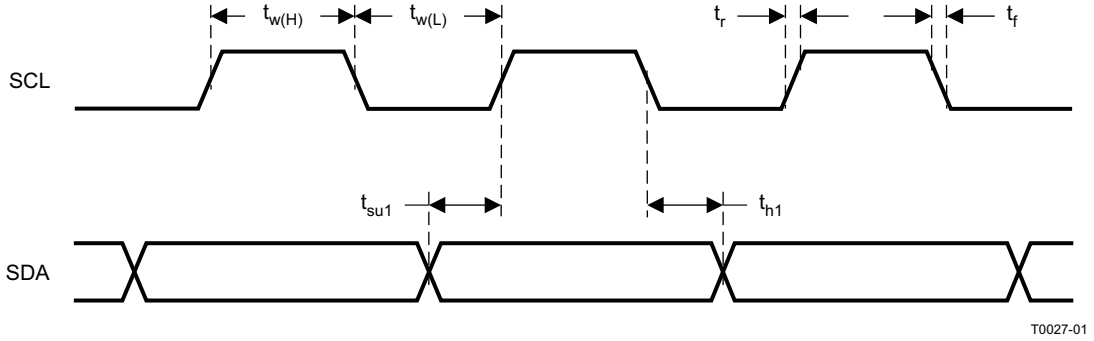


Figure 1. SCL and SDA Timing

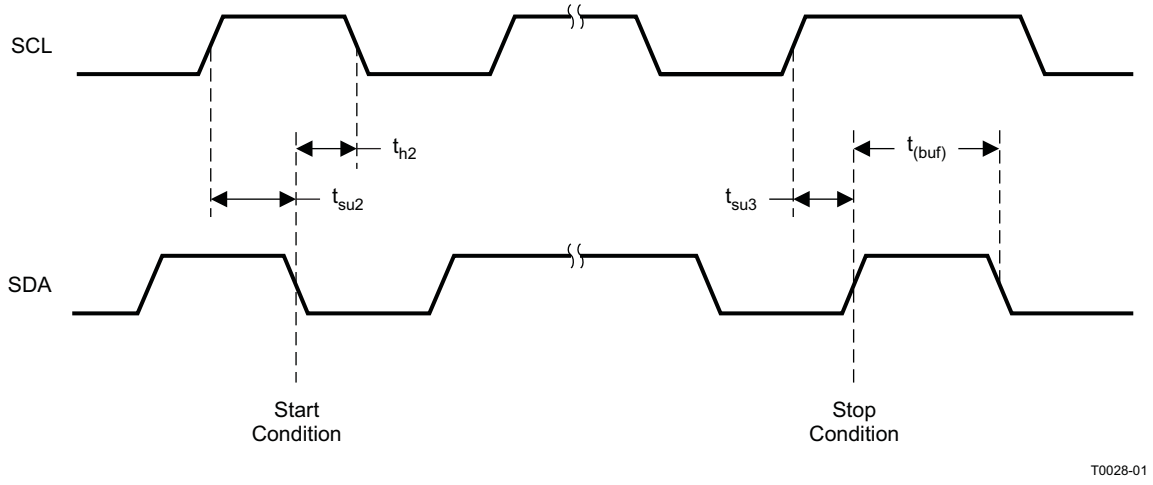


Figure 2. Timing for Start and Stop Conditions

7.7 Typical Characteristics

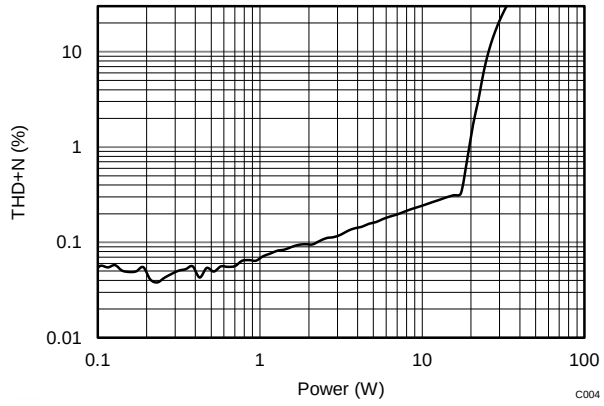


Figure 3. THD+N vs BTL Output Power at 1 kHz into 4 Ω

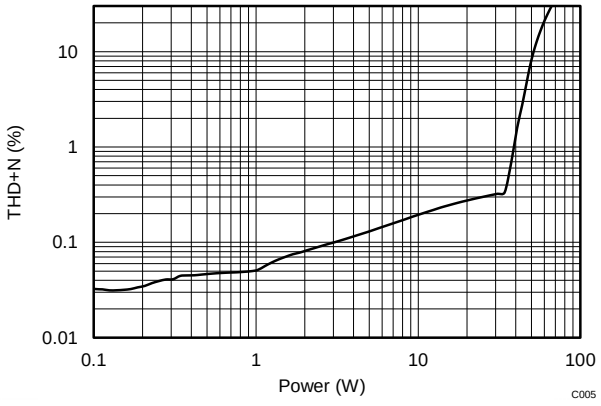


Figure 4. THD+N vs PBTL Output Power at 1 kHz into 2 Ω

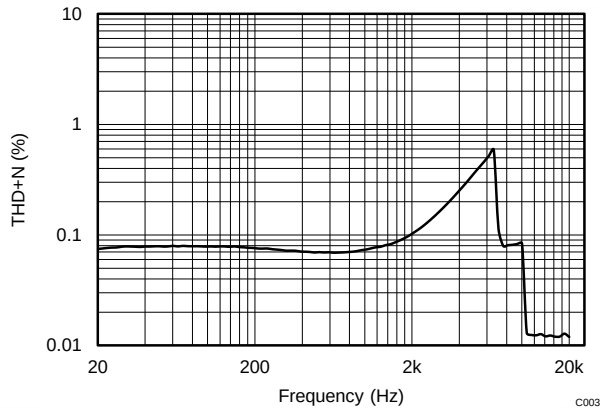


Figure 5. THD+N vs Frequency at 1 W into 4 Ω

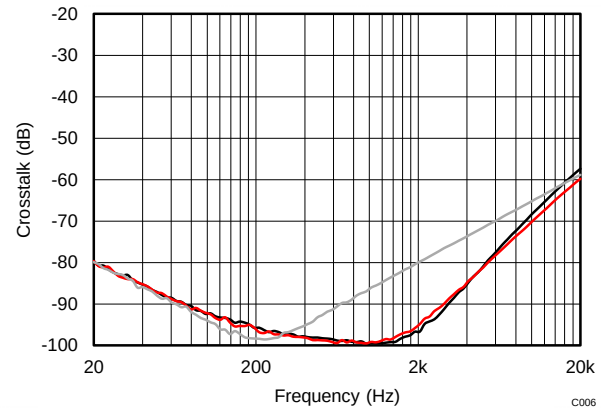


Figure 6. Crosstalk vs Frequency

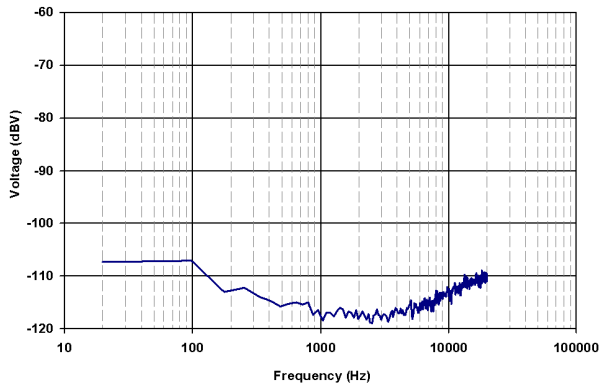


Figure 7. Noise FFT

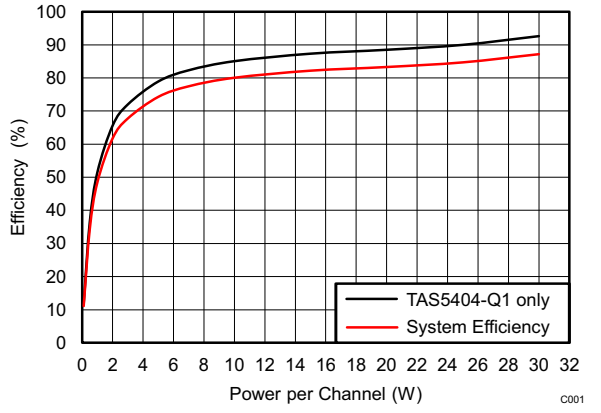


Figure 8. Efficiency
Four Channels at 4 Ω Each

Typical Characteristics (continued)

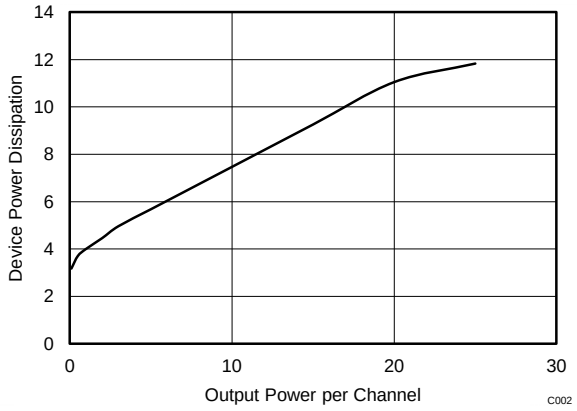


Figure 9. Device Power Dissipation
Four Channels at 4 Ω Each

8 Parameter Measurement Information

The parameters for the TAS5404-Q1 device were measured using the circuit in Figure 20.

9 Detailed Description

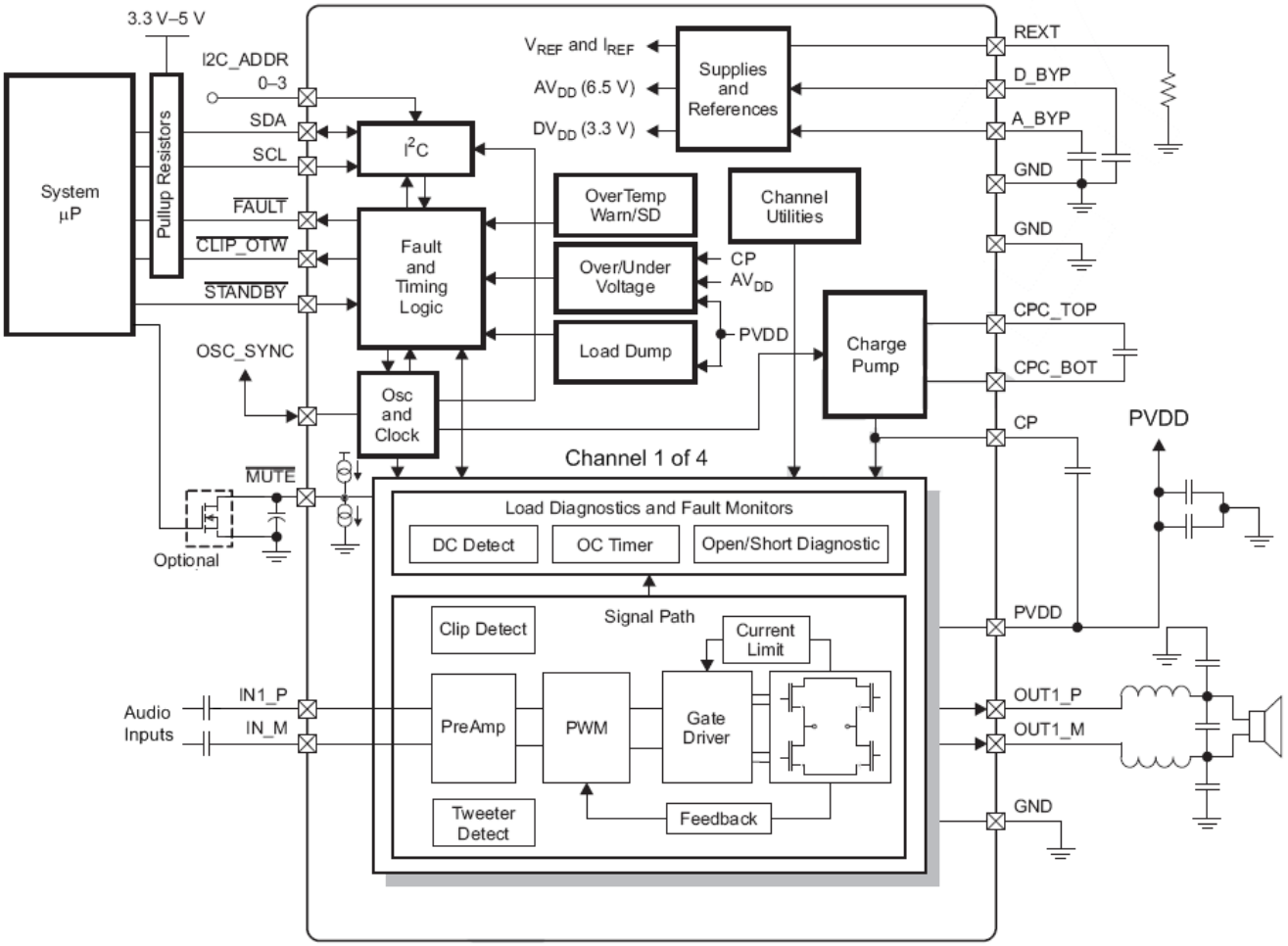
9.1 Overview

The TAS5404-Q1 device is a monolithic, four channel, audio amplifier with special features that are necessary for OEM automotive audio systems. The design of the TAS5404-Q1 device utilizes efficient, proprietary class-D technology developed by Texas Instruments. The technology of the TAS5404-Q1 device allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The TAS5404-Q1 device realizes an audio sound system design with smaller size and lower weight than class-AB solutions.

The TAS5404-Q1 device has eight core design blocks:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

9.2 Functional Block Diagram



9.3 Feature Descption

9.3.1 Preamplifier

The preamplifier is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance allows the use of low-cost input capacitors while still achieving extended low-frequency response. A dedicated, internally regulated supply powers the preamplifier, giving it excellent noise immunity and channel separation. The preamplifier in the TAS5404-Q1 device also includes:

1. **Fast Start Up** — The preamplifier will fast charge the input coupling capacitors at start up, which will allow for a fast turn-on without any pop or click.
2. **Mute Pop-and-Click Control** — The TAS5404-Q1 device ramps the gain gradually when receiving a mute or play command. The starting or stopping of switching in a class-D amplifier can cause another form of click and pop. The TAS5404-Q1 device incorporates a patented method to reduce the pop energy during the switching startup and shutdown sequence. Fault conditions require a rapid protection response, which do not have time to ramp the gain down in a pop-free manner. The TAS5404-Q1 device transitions into Hi-Z mode when encountering an OV, UV, OC, OT, or DC Offset fault. Advanced circuitry will allow for a fast, pop-free shutdown when the /STANBY pin is pulled low.
3. **Gain Control** — The gain is set for the four channels in the preamplifier through I^2C control registers. The gain control is outside of the global feedback network of the TAS5404-Q1 device, thus allowing for stability of the system at all gain settings with properly loaded conditions. A line output gain of 12 dB is provided for driving external amplifiers.

9.3.2 Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. The PWM is the critical stage that defines the class-D architecture. The modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0 to 100% modulation capability. The patented PWM uses soft clipping to for improved audio performance at clipping.

9.3.3 Gate Drive

The gate driver accepts the low-voltage PWM signal and level-shifts it to drive a high-current, full-bridge, power FET stage. The TAS5404-Q1 device uses proprietary techniques to optimize EMI and audio performance. The high-side FET power supply is generated by the charge pump circuitry.

9.3.4 Power FETs

The BTL output for each channel comprises four rugged N-channel 30-V 65-mΩ FETs for high efficiency and maximum power transfer to the load. These FETs are designed to withstand large voltage transients during load dump.

9.3.5 Load Diagnostics

The TAS5404-Q1 device incorporates load diagnostic circuitry designed to help pinpoint the nature of output misconnections during installation. These are functions for detecting and determining the status of output connections. The following diagnostics are supported:

- Short to GND (S2G)
- Short to PVDD (S2P)
- Short across load (SL)
- Open load (OL)
- Tweeter detection

Reporting to the system of the presence of any of the short or open conditions occurs through I^2C register read. Determine the tweeter-detect status from the $\overline{\text{CLIP\_OTW}}$ pin when properly configured.

1. **Output Short and Open Diagnostics** — The TAS5404-Q1 device contains circuitry designed to detect shorts and open conditions on the outputs. Invocation of the load diagnostic function will automatically place the channel into Hi-Z mode. All pop-free transitions will occur before the load diagostics will start. The test has four phases and two levels of test during load diagnostics. In the full level, all channels must be in the Hi-Z state. Testing covers all four phases on each channel on all four channels at the same time. When fewer than four channels are in Hi-Z, the reduced level of test is the only available option. In the reduced level, the

Feature Descption (continued)

only tests available are short to PVDD and short to GND. Load diagnostics can occur at anytime during operation of the TAS5404-Q1 device, by setting the proper bits in the control registers. Performance of the diagnostics is as shown in Figure 10. Figure 11 shows the impedance ranges for the open-load and shorted-load diagnostics. The results of the diagnostics are from the diagnostic register through I^2C for each channel. With the default settings and $\overline{\text{MUTE}}$ capacitor, the S2G and S2P phases take approximately 20 ms each, the OL phase takes approximately 100 ms, and the SL takes approximately 230 ms. In I^2C register 0x10, bit D4 can extend the test time for S2P and S2G to 80 ms each. To prevent false S2G and S2P faults, the time extension is necessary if the output pins have a capacitance higher than 680 nF to ground.

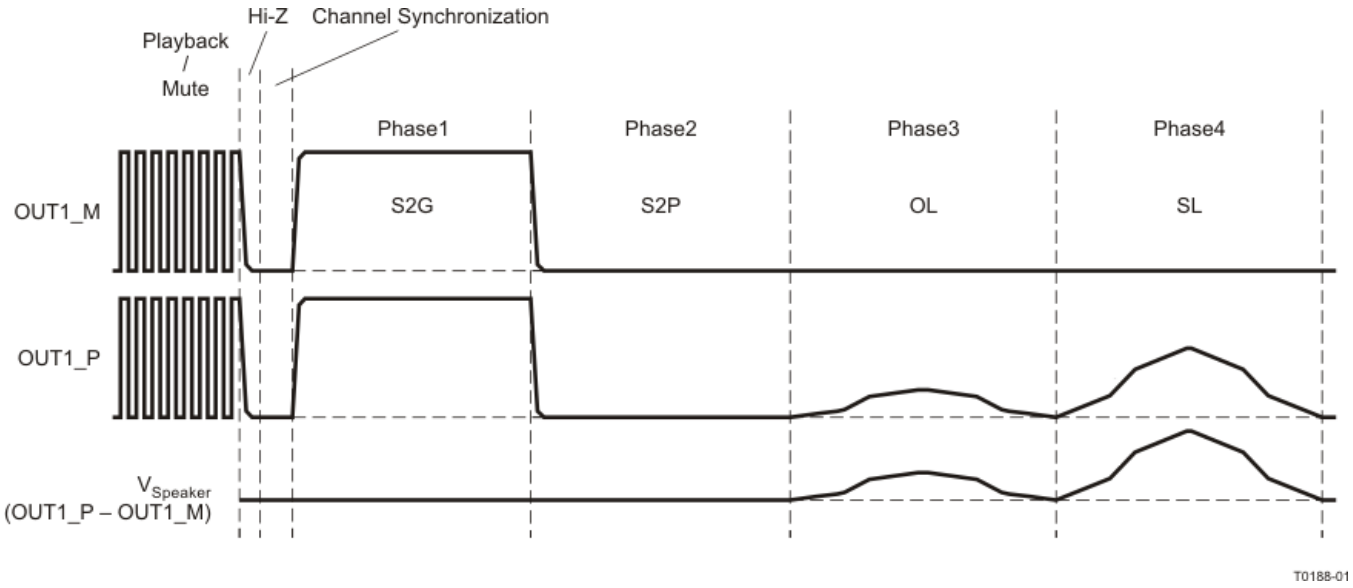


Figure 10. Load Diagnostics Sequence of Events

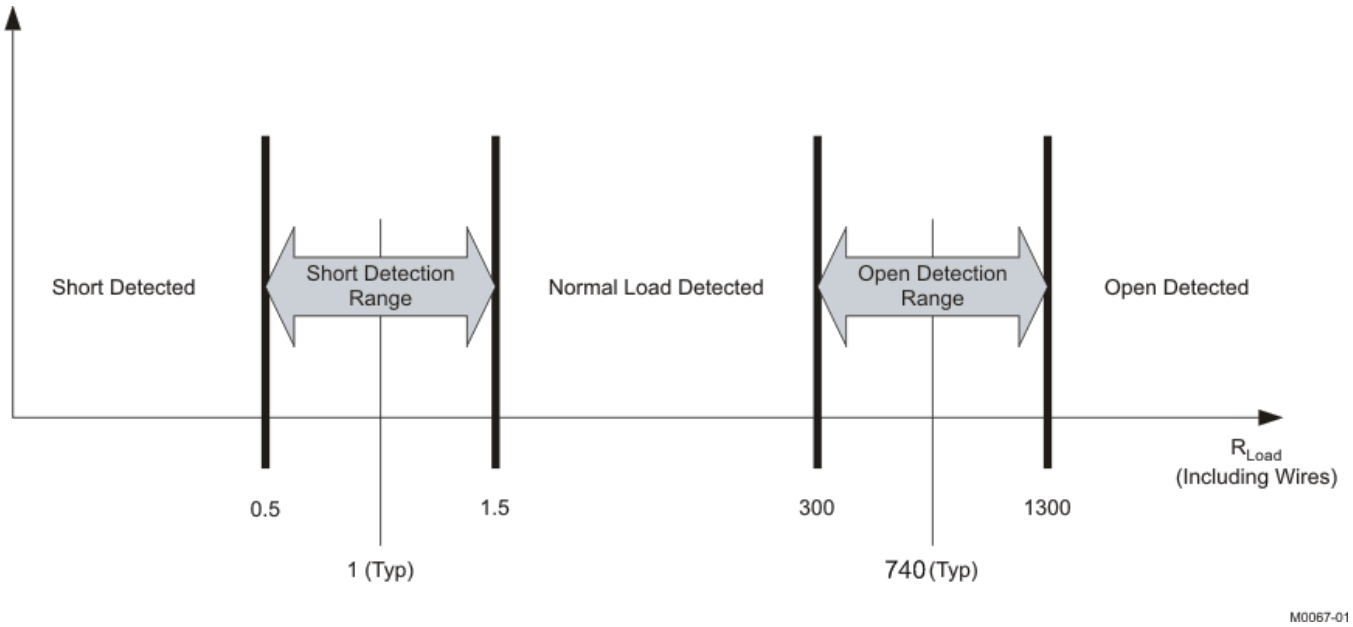


Figure 11. Open- and Shorted-Load Detection

Feature Descption (continued)

2. **Tweeter Detection** — Tweeter detection is an operating mode used to determine the proper connection of a frequency-dependent load (such as a speaker with a crossover). Tweeter detection is started through I^2C, and individual testing of all four channels is recommended. Tweeter detection uses the average cycle-by-cycle current limit circuit (see *CBC* section) to measure the current delivered to the load. The proper implementation of the diagnostic function depends on the amplitude of a user-supplied test signal and on the impedance-versus-frequency curve of the acoustic load. The external system must generate a signal to which the load responds. The frequency and amplitude of the signal must be calibrated by the user to result in a current draw that is greater than the tweeter detection threshold when the load under test is present, and less than the detection threshold if the load is unconnected. The current level for the tweeter detection threshold, as well as the maximum current that can safely be delivered to a load when in tweeter-detection mode, is in the Electrical Characteristics section of the data sheet. Reporting of the tweeter-detection results is on the $\overline{\text{CLIP\_OTW}}$ pin during the application of the test signal. With tweeter detection activated (indicating that the tested load is present), pulses on the $\overline{\text{CLIP\_OTW}}$ pin begin to toggle. The pulses on the $\overline{\text{CLIP\_OTW}}$ pins report low whenever the current exceeds the detection threshold, and the pin remains low until the current no longer exceeds the threshold. The minimum low-pulse period is equal to one period of the switching frequency. Having an input signal that increases the duration of detector activation (for example, increasing the amplitude of the input signal) increases the amount of time for which the pin reports low.

NOTE

Because tweeter detection is an alternate *operating mode*, place the channels to be tested in Play mode (through register 0x0C) after tweeter detection has been activated to commence the detection process. Additionally, set up the $\overline{\text{CLIP\_OTW}}$ pin through register 0x0A to report the results of tweeter detection.

9.3.6 Protection and Monitoring

1. **Cycle-By-Cycle Current Limit (CBC)** — The CBC current-limiting circuit terminates each PWM pulse to limit the output current flow to the average current limit (I_{LIM}) threshold. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, temporarily limiting power at the peaks of the musical signal and normal operation continues without disruption on removal of the overload. Premature shutdown does not occur in this condition. All four channels continue in play mode and pass signal.
2. **Overcurrent Shutdown (OCSD)** — Under severe short-circuit events, such as a short to PVDD or ground, the TAS5404-Q1 device uses a peak-current detector, and the affected channel shuts down in 200 µs to 390 µs if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels shut down in such a scenario. The user can restart the affected channel through I^2C. An OCSD event activates the fault pin, and the I^2C fault register saves a record of the affected channels. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.
3. **DC Offset Detect**—the circuit detects a dc offset at the output of the amplifier continuously during normal operation. If the DC offset reaches the level defined in the I^2C registers for the specified time period, the circuit triggers. By default, a DC offset detection event places the output in Hi-Z mode. Disabling and enabling the shutdown function is through I^2C. If enabled, the triggered channel shuts down, but the others remain playing, but with the $\overline{\text{FAULT}}$ pin asserted. The DC offset level is defined in the I^2C registers.
4. **Clip Detect**—The clip detect circuit indicates the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, a signal passed to the $\overline{\text{CLIP\_OTW}}$ pin asserts it until the 100% duty-cycle PWM signal is no longer present. All four channels connect to the same $\overline{\text{CLIP\_OTW}}$ pin. Through I^2C, change the $\overline{\text{CLIP\_OTW}}$ signal clip-only, OTW-only, or both. A fourth mode, used only during diagnostics, is the option to report tweeter detection events on the $\overline{\text{CLIP\_OTW}}$ pin (see the *Tweeter Detection* section). The microcontroller in the system can monitor the signal at the $\overline{\text{CLIP\_OTW}}$ pin, and can have a configuration that reduces the volume to all four channels in an active clipping-prevention circuit.
5. **Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD) and Thermal Foldback** — By default, the $\overline{\text{CLIP\_OTW}}$ pin setting indicates an OTW. The user can make changes through I^2C commands. If selected to indicate a temperature warning, $\overline{\text{CLIP\_OTW}}$ pin assertion occurs when the die temperature reaches warning level 1 as shown in the electrical specifications. The OTW has three temperature thresholds

Feature Descption (continued)

with a 10°C hysteresis. I²C register 0x04 indicates each threshold in bits 5, 6, and 7. The TAS5404-Q1 device still functions until the temperature reaches the OTSD threshold, at which time the outputs go into Hi-Z mode and the TAS5404-Q1 device asserts the FAULT pin. I²C is still active in the event of an OTSD, and the user can read the registers for faults, but all audio ceases abruptly. After the OTSD resets, turn the TAS5404-Q1 device back on through I²C. The OTW indication remains until the temperature drops below warning level 1. The thermal foldback decreases the channel gain.

6. **Undervoltage (UV) and Power-on-Reset (POR)** — The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the TAS5404-Q1 device asserts the FAULT pin and updates the I²C registerd, depending on which voltage caused the event. Power-on reset (POR) occurs when PVDD drops low enough. A POR event causes the I²C to go into a high-impedance state. After the TAS5404-Q1 device recovers from the POR event, the device re-initialization occurs through I²C.
7. **Overvoltage (OV) and Load Dump** — The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the TAS5404-Q1 device asserts the FAULT pin iand updates the I²C register. The TAS5404-Q1 device can withstand 50-V load-dump voltage spikes.

9.3.7 I²C Serial Communication Bus

The TAS5404-Q1 device communicates with the system processor through the I²C serial communication bus as an I²C slave-only device. The processor can poll the device through I²C to determine the operating status. All reports of fault conditions and detections are through I²C. The TAS5404-Q1 device also has numerous features and operating conditions that can be set through I²C.

The I²C bus allows control of the following configurations:

- Independent gain control of each channel. The gain can be set to 12 dB, 20 dB, 26 dB, and 32 dB.
- Select the AM non-interference switching frequency
- Select the functionality of the OTW_CLIP pin
- Enable or disable the dc-detect function with selectable threshold
- Place a channel in Hi-Z (switching stopped) mode (mute)
- Select tweeter detect, set the detection threshold, and initiate the function
- Initiate the open-load and shorted-load diagnostic
- Reset faults and return to normal switching operation from Hi-Z mode (unmute)

In addition to the standard SDA and SCL pins for the I²C bus, the TAS5404-Q1 device includes a single pin that allows up to four devices to work together in a system with no additional hardware required for communication or synchronization. The I2C_ADDR pin sets the device in master or slave mode and selects the I²C address for that device. Tie the I2C_ADDR pin to DGND for master, to 1.2 Vdc for slave 1, to 2.4 Vdc for slave 2, and to D_BYP for slave 3. The OSC_SYNC pin is for synchronizing the internal clock oscillators to avoid beat frequencies. An external oscillator can be applied to the OSC_SYNC pin for external control of the switching frequency.

Table 1. Table 7. I2C_ADDR Pin Connection

I2C_ADDR VALUE	I2C_ADDR PIN CONNECTION	I²C ADDRESSES
0 (OSC MASTER)	To SGND pin	0xD8/D9
1 (OSC SLAVE1)	35% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDA/DB
2 (OSC SLAVE2)	65% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDC/DD
3 (OSC SLAVE3)	To D_BYP pin	0xDE/DF

(1) TI recommends R_{I2C_ADDR} resistors with 5% or better tolerance.

9.3.8 I²C Bus Protocol

The TAS5404-Q1 device has a bidirectional serial control interface that is compatible with the Inter IC (I^2C) bus protocol and supports 400-kbps data transfer rates for random and sequential write and read operations. The TAS5404-Q1 device is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface programs the registers of the device and reads device status.

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data transfer on the bus is serial, one bit at a time. The transfer of address and data is in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, the receiving device acknowledges each byte transferred on the bus with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 12 shows these conditions. The master generates the 7-bit slave address and the read/write bit to open communication with another device and then wait for an acknowledge condition. The TAS5404-Q1 holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When the acknowledgment occurs, the master device transmits the next byte of the sequence. Each slave device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection. The SDA and SCL signals must have an external pullup resistor to set the HIGH level for the bus. Any number of bytes can be transmitted between start and stop conditions. When the last word transfers, the master device generates a stop condition to release the bus.

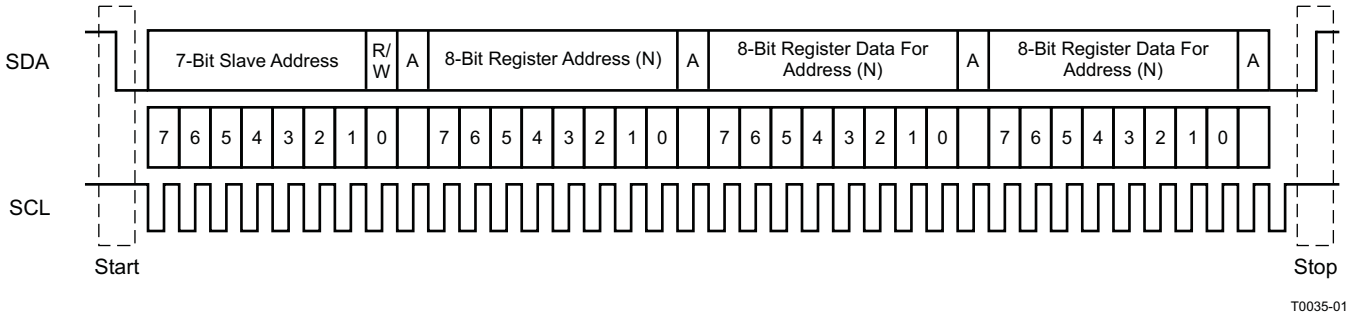


Figure 12. Typical I^2C Sequence

Use the I2C_ADDR pin (pin 2) to program the TAS5404-Q1 device for one of four addresses. These four addresses are licensed I^2C addresses and do not conflict with other licensed I^2C audio devices. The I^2C master device uses addresses shown in Figure 12 to communicate. Transmission of read and write data can be through single-byte or multiple-byte data transfers.

9.3.9 Hardware Control Pins

The TAS5404-Q1 device has four discrete hardware pins for real-time control and indication of device status:

1. $\overline{\text{FAULT}}$ pin: This active-low open-drain output pin indicates the presence of a fault condition that requires the TAS5404-Q1 device to go into the Hi-Z mode. On assertion of the $\overline{\text{FAULT}}$ pin, the TAS5404-Q1 device has protected itself and the system from potential damage. Read the details of the fault through I^2C with the exception of PVDD undervoltage faults below POR, in which case the I^2C bus is no longer operational. However, the fault is still indicated due to $\overline{\text{FAULT}}$ pin assertion.
2. $\overline{\text{CLIP\_OTW}}$ pin: Configured through I^2C, this active-low open-drain pin indicates one of the following conditions: overtemperature warning, the detection of clipping, or the logical OR of both of these conditions. During tweeter detect diagnostics, assertion of the CLIP_OTW pin also occurs when a tweeter is present. The CLIP_OTW pin can also indicate thermal foldback is active.
3. $\overline{\text{MUTE}}$ pin: This active-low pin is used for hardware control of the mute-unmute function for all four channels. Capacitor C_{MUTE} controls the time constant for the gain ramp required to produce a pop-and-click-free mute function. For pop-and-click-free operation, implementation of the mute function should be through I^2C commands. The use of a hard mute with an external transistor does not ensure pop-and-click-free operation, and TI does not recommend it except as an *emergency hard mute* function in case of a loss of I^2C control. The C_{MUTE} capacitor cannot be shared between multiple devices.
4. $\overline{\text{STANDBY}}$ pin: On assertion of this active-low pin, the TAS5404-Q1 device goes into a complete shutdown, and the typical current-draw limit is 2 μA, typical. $\overline{\text{STANDBY}}$ can be used to shut down the device rapidly. If all channels are in Hi-Z, the device enters standby in approximately 1 ms. If the channels are in play mode, the device enters standby in approximately 4.5 ms with a pop-and-click-free operation. All I^2C register content is lost and the I^2C bus goes into the high-impedance state on assertion of the $\overline{\text{STANDBY}}$ pin.

9.3.10 AM Radio Avoidance

To reduce interference in the AM radio band, the TAS5404-Q1 device has the ability to change the switching frequency through I^2C commands. Table 2 lists the recommended frequencies. The fundamental frequency and the second harmonic straddle the AM radio band listed, which eliminates the tones that can be present due to demodulation of the switching frequency by the AM radio.

Table 2. Recommended Switching Frequencies for AM Mode Operation

US		EUROPEAN	
AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)
540–670	417	522–675	417
680–980	500	676–945	500
990–1180	417	946–1188	417
1190–1420	500	1189–1422	500
1430–1580	417	1423–1584	417
1590–1700	500	1585–1701	500

9.4 Device Functional Modes

Table 3 and Table 5 depict the operating modes and faults.

Table 3. Operating Modes

STATE NAME	OUTPUT FETS	CHARGE PUMP	OSCILLATOR	I^2C	AVDD and DVDD
STANDBY	Hi-Z, floating	Stopped	Stopped	Stopped	OFF
Hi-Z	Hi-Z, weak pulldown	Active	Active	Active	ON
Mute	Switching at 50%	Active	Active	Active	ON
Normal operation	Switching with audio	Active	Active	Active	ON

Table 4. Global Faults and Actions

FAULT OR EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED OR SELF-CLEARING
POR	Voltage fault	All	$\overline{FAULT}$ pin	Hard mute (no ramp)	Standby	Self-clearing
UV		Hi-Z, mute, normal	I^2C + $\overline{FAULT}$ pin		Hi-Z	Latched
CP UV						
OV						
Load dump		All	$\overline{FAULT}$ pin		Standby	Self-clearing
OTW	Thermal warning	Hi-Z, mute, normal	I^2C + $\overline{CLIP\_OTW}$ pin	None	None	Self-clearing
OTSD	Thermal fault	Hi-Z, mute, normal	I^2C + $\overline{FAULT}$ pin	Hard mute (no ramp)	Standby	Latched

Table 5. Channel Faults and Actions

FAULT/ EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED OR SELF-CLEARING
Open-short diagnostic	Diagnostic	Hi-Z (I^2C activated)	I^2C	None	None	Latched
Clipping	Warning	Mute / Play	$\overline{CLIP\_OTW}$ pin	None	None	Self-clearing
CBC load current limit	Online protection			Current Limit	Start OC timer	Self-clearing
OC fault	Output channel fault		I^2C + $\overline{FAULT}$ pin	Hard mute	Hi-Z	Latched
DC offset detect				Hard mute	Hi-Z	Latched
OT Foldback	Warning		I^2C + $\overline{CLIP\_OTW}$ pin	Reduce Gain	None	Self-clearing

9.4.1 Audio Shutdown and Restart Sequence

The gain ramp of the filtered output signal and the updating of the I^2C registers correspond to the MUTE pin voltage during the ramping process. The value of the external capacitor on the MUTE pin dictates the length of time that the MUTE pin takes to complete the ramp. With the default 220-nF capacitor, the turn on common-mode ramp takes approximately 26 ms and the gain ramp takes approximately 76 ms.

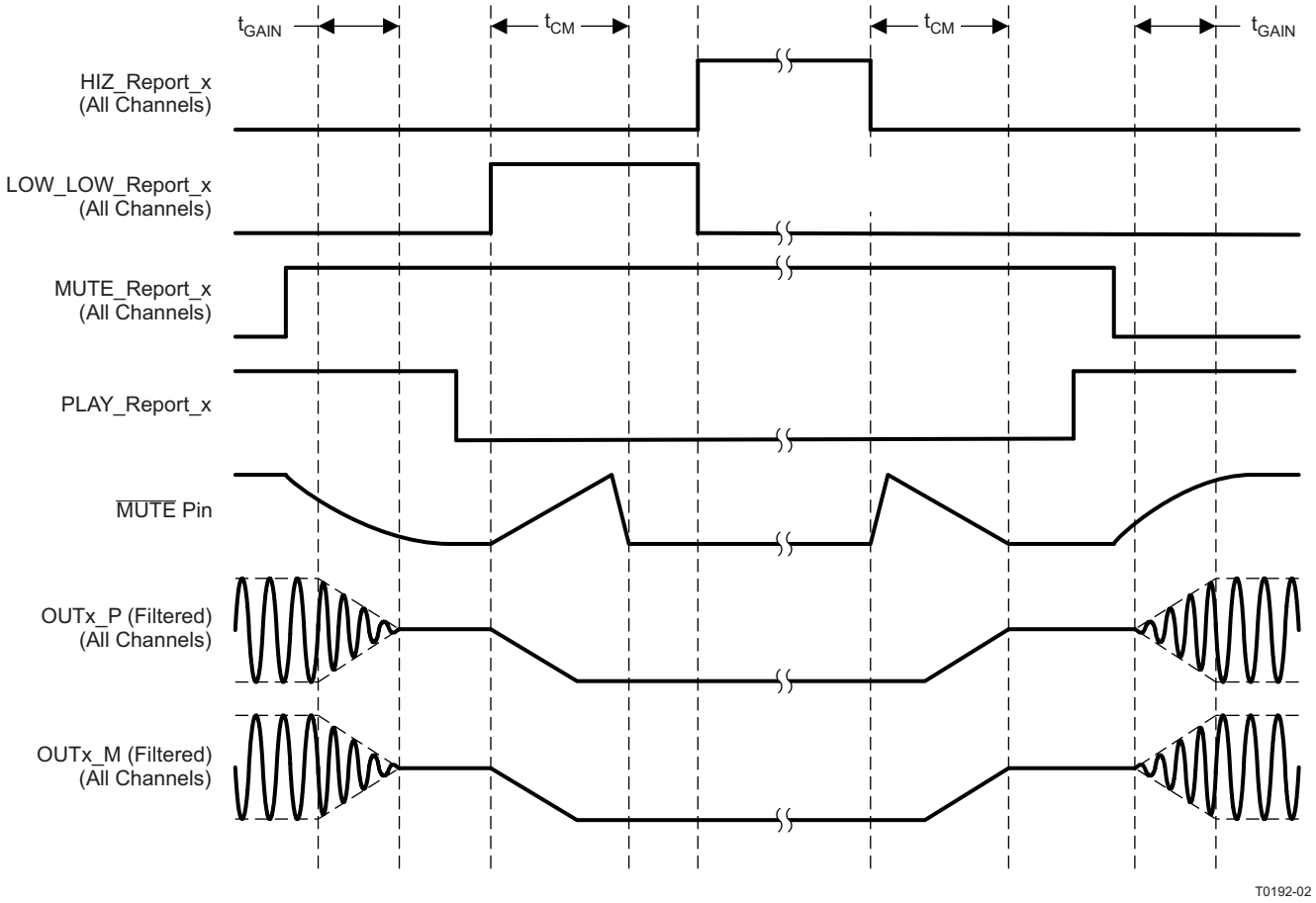


Figure 13. Timing Diagram for Click- and Pop-Free Shutdown and Restart Sequence

9.4.2 Latched-Fault Shutdown and Restart Sequence Control

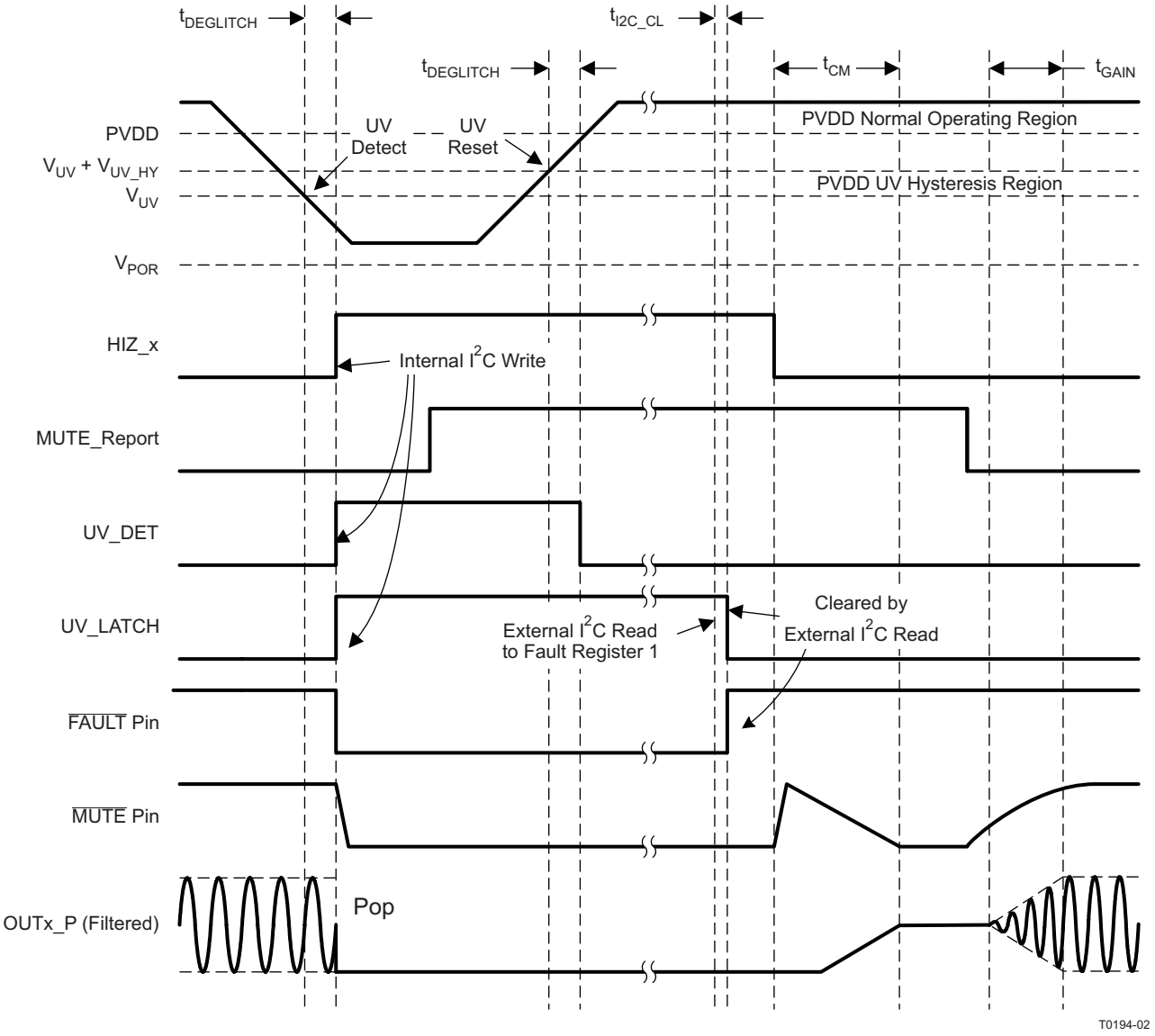


Figure 14. Timing Diagram for Latched-Global-Fault Shutdown and Restart (UV Shutdown and Recovery)

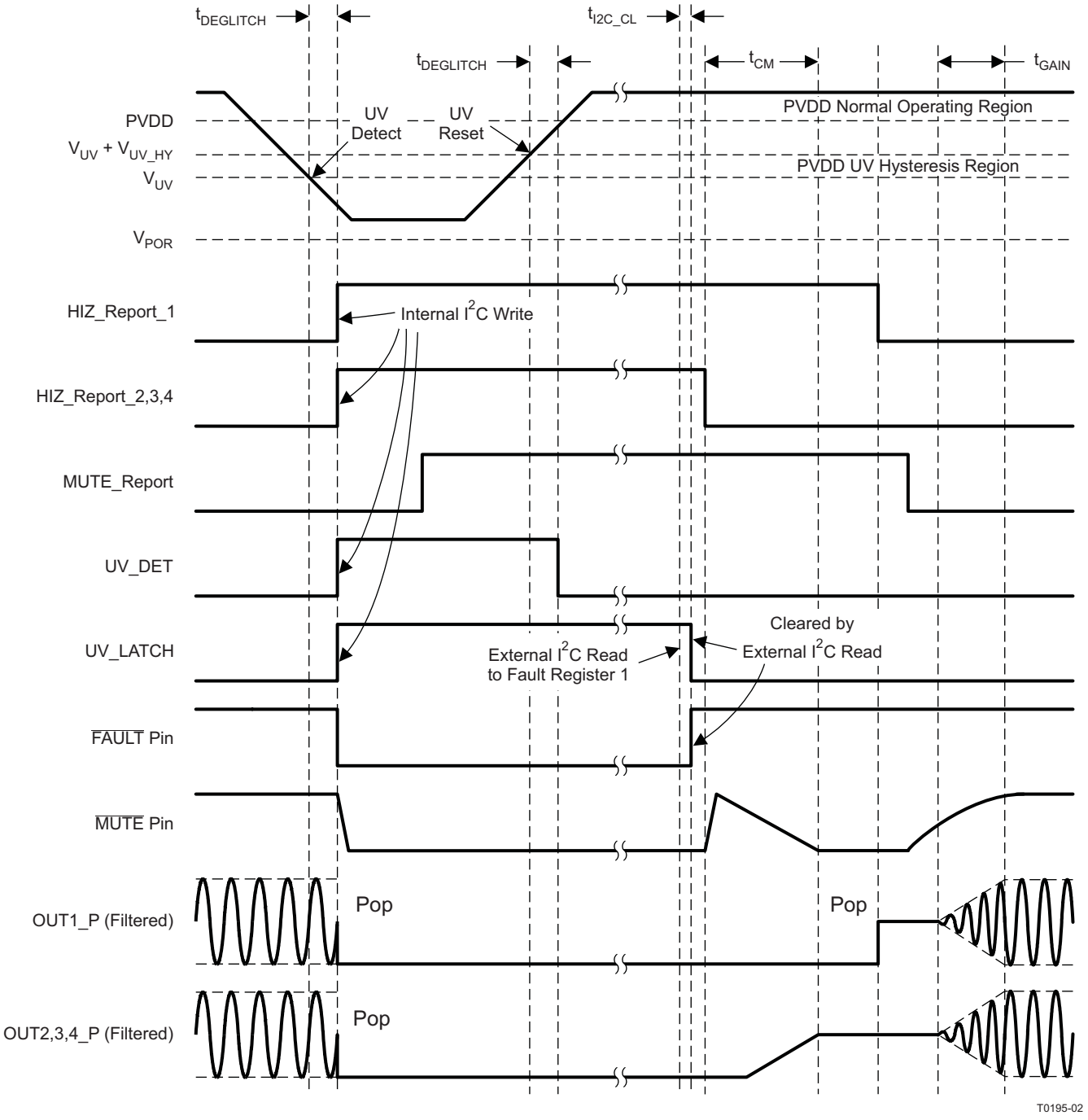


Figure 15. Timing Diagram for Latched-Global-Fault Shutdown and Individual-Channel Restart (UV Shutdown and Recovery)

9.5 Programming

9.5.1 Random Write

As shown in Figure 16, a random write or single-byte write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a single-byte write data transfer, the read/write bit is a 0. After receiving the correct I^2C device address and the read/write bit, the slave device responds with an acknowledge bit. Next, the master device transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the slave device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5404Q1 device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte write transfer.

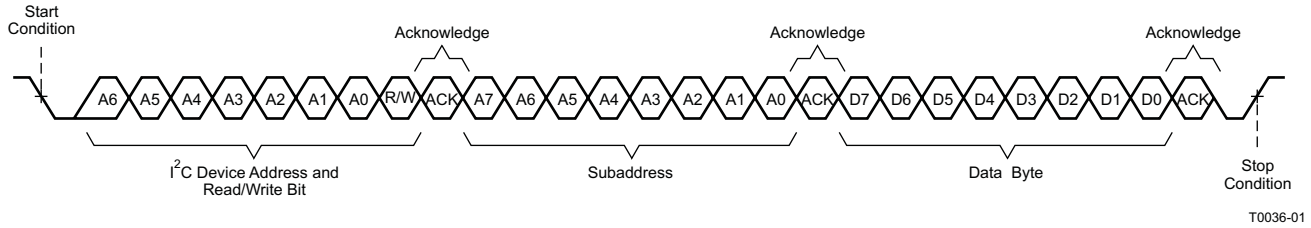


Figure 16. Random-Write Transfer

9.5.2 Sequential Write

A sequential write transfer is identical to a single-byte data-write transfer except for the transmisson of multiple data bytes by the master device as shown in Figure 17. After receiving each data byte, the slave device responds with an acknowledge bit and automatically increments the I^2C subaddress by one.

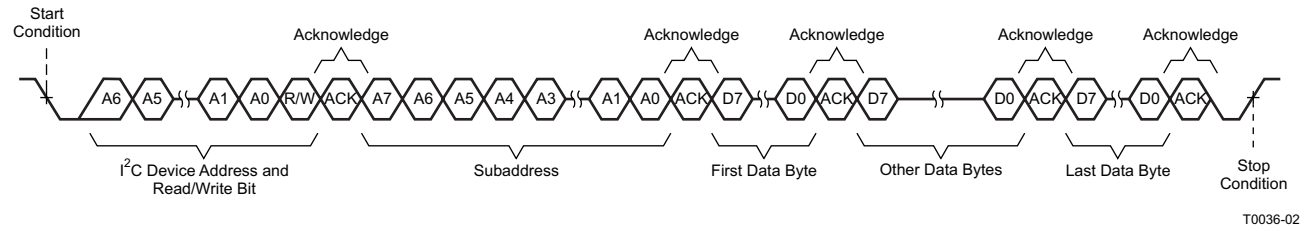


Figure 17. Sequential Write Transfer

Programming (continued)

9.5.3 Random Read

As shown in Figure 18, a random read or single-byte read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the single-byte read transfer, the master device transmits both a write followed by a read. Initially, a write transfers the address byte or bytes of the internal memory address to be read. Therefore, the read/write bit is a 0. After receiving the address and the read/write bit, the slave device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the device address and the read/write bit again. At that point the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the slave device again responds with an acknowledge bit. Next, the TAS5404-Q1 device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte read transfer.

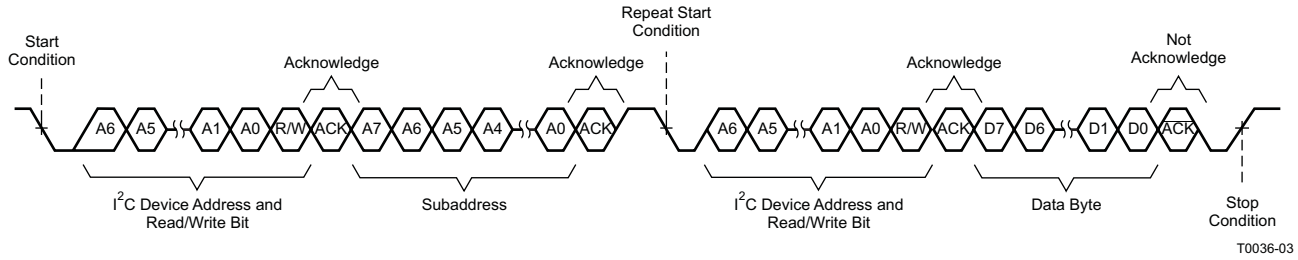


Figure 18. Random Read Transfer

9.5.4 Sequential Read

A sequential read transfer is identical to a single-byte read transfer except for the transmission of multiple data bytes by the TAS5404-Q1 device to the master device as shown in Figure 19. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

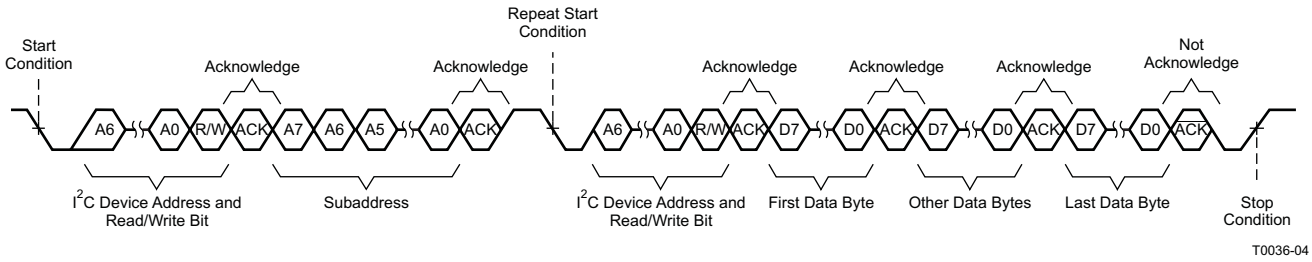


Figure 19. Sequential Read Transfer

9.6 Register Maps

Table 6. TAS5404-Q1 I²C Addresses

I2C_ADDR VALUE		FIXED ADDRESS					SELECTABLE WITH ADDRESS PIN		READ/WRITE BIT	I²C ADDRESS
		MSB	6	5	4	3	2	1	LSB	
0 (OSC MASTER)	I²C WRITE	1	1	0	1	1	0	0	0	0xD8
	I²C READ	1	1	0	1	1	0	0	1	0xD9
1 (OSC SLAVE1)	I²C WRITE	1	1	0	1	1	0	1	0	0xDA
	I²C READ	1	1	0	1	1	0	1	1	0xDB
2 (OSC SLAVE2)	I²C WRITE	1	1	0	1	1	1	0	0	0xDC
	I²C READ	1	1	0	1	1	1	0	1	0xDD
3 (OSC SLAVE3)	I²C WRITE	1	1	0	1	1	1	1	0	0xDE
	I²C READ	1	1	0	1	1	1	1	1	0xDF

Table 7. I²C Address Register Definitions

ADDRESS	TYPE	REGISTER DESCRIPTION
0x00	Read	Latched fault register 1, global and channel fault
0x01	Read	Latched fault register 2, dc offset and overcurrent detect
0x02	Read	Latched diagnostic register 1, load diagnostics
0x03	Read	Latched diagnostic register 2, load diagnostics
0x04	Read	External status register 1, temperature and voltage detect
0x05	Read	External status register 2, Hi-Z and low-low state
0x06	Read	External status register 3, mute and play modes
0x07	Read	External status register 4, load diagnostics
0x08	Read, Write	External control register 1, channel gain select
0x09	Read, Write	External control register 2, overcurrent control
0x0A	Read, Write	External control register 3, switching frequency and clip pin select
0x0B	Read, Write	External control register 4, load diagnostic, master mode select
0x0C	Read, Write	External control register 5, output state control
0x0D	Read, Write	External control register 6, output state control
0x0E, 0x0F	–	Not used
0x10	Read, Write	External control register 7, dc offset detect threshold selection
0x13	Read	External status register 5, overtemperature shutdown and thermal foldback

Table 8. Fault Register 1 (0x00) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Overtemperature warning has occurred.
–	–	–	–	–	–	1	–	DC offset has occurred in any channel.
–	–	–	–	–	1	–	–	Overcurrent shutdown has occurred in any channel.
–	–	–	–	1	–	–	–	Overtemperature shutdown has occurred.
–	–	–	1	–	–	–	–	Charge-pump undervoltage has occurred.
–	–	1	–	–	–	–	–	AVDD, analog voltage, undervoltage has occurred.
–	1	–	–	–	–	–	–	PVDD undervoltage has occurred.
1	–	–	–	–	–	–	–	PVDD overvoltage has occurred.

Table 9. Fault Register 2 (0x01) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Overcurrent shutdown channel 1 has occurred.
–	–	–	–	–	–	1	–	Overcurrent shutdown channel 2 has occurred.
–	–	–	–	–	1	–	–	Overcurrent shutdown channel 3 has occurred.
–	–	–	–	1	–	–	–	Overcurrent shutdown channel 4 has occurred.
–	–	–	1	–	–	–	–	DC offset channel 1 has occurred.
–	–	1	–	–	–	–	–	DC offset channel 2 has occurred.
–	1	–	–	–	–	–	–	DC offset channel 3 has occurred.
1	–	–	–	–	–	–	–	DC offset channel 4 has occurred.

Table 10. Diagnostic Register 1 (0x02) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to ground channel 1 has occurred.
–	–	–	–	–	–	1	–	Output short to PVDD channel 1 has occurred.
–	–	–	–	–	1	–	–	Shorted load channel 1 has occurred.
–	–	–	–	1	–	–	–	Open load channel 1 has occurred.
–	–	–	1	–	–	–	–	Output short to ground channel 2 has occurred.
–	–	1	–	–	–	–	–	Output short to PVDD channel 2 has occurred.
–	1	–	–	–	–	–	–	Shorted load channel 2 has occurred.
1	–	–	–	–	–	–	–	Open load channel 2 has occurred.

Table 11. Diagnostic Register 2 (0x03) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to ground channel 3 has occurred.
–	–	–	–	–	–	1	–	Output short to PVDD channel 3 has occurred.
–	–	–	–	–	1	–	–	Shorted load channel 3 has occurred.
–	–	–	–	1	–	–	–	Open load channel 3 has occurred.
–	–	–	1	–	–	–	–	Output short to ground channel 4 has occurred.
–	–	1	–	–	–	–	–	Output short to PVDD channel 4 has occurred.
–	1	–	–	–	–	–	–	Shorted load channel 4 has occurred.
1	–	–	–	–	–	–	–	Open load channel 4 has occurred.

Table 12. External Status Register 1 (0x04) Fault Detection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults are present, default value.
–	–	–	–	–	–	–	1	PVDD overvoltage fault is present.
–	–	–	–	–	–	1	–	PVDD undervoltage fault is present.
–	–	–	–	–	1	–	–	AVDD, analog voltage fault is present.
–	–	–	–	1	–	–	–	Charge-pump voltage fault is present.
–	–	–	1	–	–	–	–	Overtemperature shutdown is present.
0	0	1	–	–	–	–	–	Overtemperature warning
0	1	1	–	–	–	–	–	Overtemperature warning level 1
1	0	1	–	–	–	–	–	Overtemperature warning level 2
1	1	1	–	–	–	–	–	Overtemperature warning level 3

Table 13. External Status Register 2 (0x05) Output State of Individual Channels

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	1	1	1	1	Output is in Hi-Z mode, not in low-low mode(1), default value.
–	–	–	–	–	–	–	0	Channel 1 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	–	–	0	–	Channel 2 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	–	0	–	–	Channel 3 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	0	–	–	–	Channel 4 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	1	–	–	–	–	Channel 1 low-low mode (0 = not low-low, 1 = low-low)(1)
–	–	1	–	–	–	–	–	Channel 2 low-low mode (0 = not low-low, 1 = low-low)(1)
–	1	–	–	–	–	–	–	Channel 3 low-low mode (0 = not low-low, 1 = low-low)(1)
1	–	–	–	–	–	–	–	Channel 4 low-low mode (0 = not low-low, 1 = low-low)(1)

(1) *Low-low* is defined as both outputs actively pulled to ground.

Table 14. External Status Register 3 (0x06) Play and Mute Modes

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Mute mode is disabled, play mode disabled, default value, (Hi-Z mode).
–	–	–	–	–	–	–	1	Channel 1 play mode is enabled.
–	–	–	–	–	–	1	–	Channel 2 play mode is enabled.
–	–	–	–	–	1	–	–	Channel 3 play mode is enabled.
–	–	–	–	1	–	–	–	Channel 4 play mode is enabled.
–	–	–	1	–	–	–	–	Channel 1 mute mode is enabled.
–	–	1	–	–	–	–	–	Channel 2 mute mode is enabled.
–	1	–	–	–	–	–	–	Channel 3 mute mode is enabled.
1	–	–	–	–	–	–	–	Channel 4 mute mode is enabled.

Table 15. External Status Register 4 (0x07) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No channels are set in load diagnostics mode, default value.
–	–	–	–	–	–	–	1	Channel 1 is in load diagnostics mode.
–	–	–	–	–	–	1	–	Channel 2 is in load diagnostics mode.
–	–	–	–	–	1	–	–	Channel 3 is in load diagnostics mode.
–	–	–	–	1	–	–	–	Channel 4 is in load diagnostics mode.
–	–	–	1	–	–	–	–	Channel 1 is in overtemperature foldback.
–	–	1	–	–	–	–	–	Channel 2 is in overtemperature foldback.
–	1	–	–	–	–	–	–	Channel 3 is in overtemperature foldback.
1	–	–	–	–	–	–	–	Channel 4 is in overtemperature foldback.

Table 16. External Control Register 1 (0x08) Gain Select

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	0	1	0	1	0	1	0	Set gain for all channels to 26 dB, default value.
–	–	–	–	–	–	0	0	Set channel 1 gain to 12 dB.
–	–	–	–	–	–	0	1	Set channel 1 gain to 20 dB.
–	–	–	–	–	–	1	1	Set channel 1 gain to 32 dB.
–	–	–	–	0	0	–	–	Set channel 2 gain to 12 dB.
–	–	–	–	0	1	–	–	Set channel 2 gain to 20 dB.
–	–	–	–	1	1	–	–	Set channel 2 gain to 32 dB.
–	–	0	0	–	–	–	–	Set channel 3 gain to 12 dB.
–	–	0	1	–	–	–	–	Set channel 3 gain to 20 dB.
–	–	1	1	–	–	–	–	Set channel 3 gain to 32 dB.

Table 16. External Control Register 1 (0x08) Gain Select (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	–	–	–	–	–	–	Set channel 4 gain to 12 dB.
0	1	–	–	–	–	–	–	Set channel 4 gain to 20 dB.
1	1	–	–	–	–	–	–	Set channel 4 gain to 32 dB.

Table 17. External Control Register 2 (0x09) Overcurrent Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	1	1	1	0	0	0	0	Current limit level 2 for all channels, thermal foldback is active.
–	–	–	–	–	–	–	1	Disable thermal foldback
–	–	–	0	–	–	–	–	Set channel 1 overcurrent limit (0 - level 1, 1 - level 2)
–	–	0	–	–	–	–	–	Set channel 2 overcurrent limit (0 - level 1, 1 - level 2)
–	0	–	–	–	–	–	–	Set channel 3 overcurrent limit (0 - level 1, 1 - level 2)
0	–	–	–	–	–	–	–	Set channel 4 overcurrent limit (0 - level 1, 1 - level 2)
–	–	–	–	1	1	1	–	Reserved

Table 18. External Control Register 3 (0x0A) Switching Frequency Select and Clip_OTW Configuration

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	1	1	0	1	Set f_S = 417 kHz, report clip and OTW, 45° phase, disable hard stop, $\overline{\text{CLIP\_OTW}}$ pin does not report thermal foldback.
–	–	–	–	–	–	0	0	Set f_S = 500 kHz
–	–	–	–	–	–	1	0	Set f_S = 357 kHz
–	–	–	–	–	–	1	1	Invalid frequency selection (do not set)
–	–	–	–	0	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report tweeter detect only.
–	–	–	–	0	1	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report clip detect only.
–	–	–	–	1	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report overtemperature warning only.
–	–	–	1	–	–	–	–	Enable hard-stop mode.
–	–	1	–	–	–	–	–	Set f_S to a 180° phase difference between adjacent channels.
–	1	–	–	–	–	–	–	Send sync pulse from OSC_SYNC pin (device must be in master mode).
1	–	–	–	1	–	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report thermal foldback

Table 19. External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	1	0	1	0	0	0	0	Clock output disabled, master clock mode, dc offset detection enabled, load diagnostics disabled
–	–	–	–	–	–	–	1	Run channel 1 load diagnostics
–	–	–	–	–	–	1	–	Run channel 2 load diagnostics
–	–	–	–	–	1	–	–	Run channel 3 load diagnostics
–	–	–	–	1	–	–	–	Run channel 4 load diagnostics
–	–	–	0	–	–	–	–	Disable dc offset detection on all channels
–	–	1	–	–	–	–	–	Enable tweeter-detect mode
–	0	–	–	–	–	–	–	Enable slave mode (external oscillator is necessary)
1	–	–	–	–	–	–	–	Enable clock output on OSC_SYNC pin (valid only in master mode)

Table 20. External Control Register 5 (0x0C) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	1	1	1	1	1	All channels, Hi-Z, mute, reset disabled, dc offset detect is enabled
–	–	–	–	–	–	–	0	Set channel 1 to mute mode, non-Hi-Z
–	–	–	–	–	–	0	–	Set channel 2 to mute mode, non-Hi-Z
–	–	–	–	–	0	–	–	Set channel 3 to mute mode, non-Hi-Z
–	–	–	–	0	–	–	–	Set channel 4 to mute mode, non-Hi-Z
–	–	–	0	–	–	–	–	Set non-Hi-Z channels to play mode, (unmute)
–	–	1	–	–	–	–	–	DC offsett detect shutdown disabled, but still reports a fault
–	1	–	–	–	–	–	–	Reserved
1	–	–	–	–	–	–	–	Reset device

Table 21. External Control Register 6 (0x0D) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Low-low state disabled, all channels
–	–	–	–	–	–	–	1	Set channel 1 to low-low state
–	–	–	–	–	–	1	–	Set channel 2 to low-low state
–	–	–	–	–	1	–	–	Set channel 3 to low-low state
–	–	–	–	1	–	–	–	Set channel 4 to low-low state
–	–	–	1	–	–	–	–	Connect channel 1 and channel 2 for parallel BTL mode
–	–	1	–	–	–	–	–	Connect channel 3 and channel 4 for parallel BTL mode
1	1	–	–	–	–	–	–	Reserved

Table 22. External Control Register 7 (0x10) Miscellaneous Selection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	1	Normal speed CM ramp, normal S2P & S2G timing, no delay between LDG phases, Crosstalk Enhancement Disabled, Default DC offset detect value (1.6V)
–	–	–	–	–	–	0	0	Minimum DC offset detect value (0.8 V)
–	–	–	–	–	–	1	0	Maximum DC offset detect value (2.4 V)
–	–	–	–	–	1	–	–	Enable crosstalk enhancement
–	–	–	–	1	–	–	–	Adds a 20-ms delay between load diagnostic phases
–	–	–	1	–	–	–	–	Short-to-power (S2P) and short-to-ground (S2G) load-diagnostic phases take 4x longer
–	–	1	–	–	–	–	–	Slow common-mode ramp, increase the default time by 3x
–	1	–	–	–	–	–	–	Reserved
1	–	–	–	–	–	–	–	Slower common-mode (CM) ramp-down from mute mode

Table 23. External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Default overtemperature foldback status, no channel is in foldback
–	–	–	–	–	–	–	1	Channel 1 in thermal foldback
–	–	–	–	–	–	1	–	Channel 2 in thermal foldback
–	–	–	–	–	1	–	–	Channel 3 in thermal foldback
–	–	–	–	1	–	–	–	Channel 4 in thermal foldback
–	–	–	1	–	–	–	–	Channel 1 in overtemperature shutdown
–	–	1	–	–	–	–	–	Channel 2 in overtemperature shutdown
–	1	–	–	–	–	–	–	Channel 3 in overtemperature shutdown
1	–	–	–	–	–	–	–	Channel 4 in overtemperature shutdown

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TAS5404-Q1 device is a four-channel class-D audio amplifier designed for use in automotive head units and external amplifier modules. The TAS5404-Q1 device incorporates all the functionality required to perform in the demanding OEM applications area.

10.2 Typical Application

Figure 20 shows a typical application circuit for the TAS5404-Q1 device.

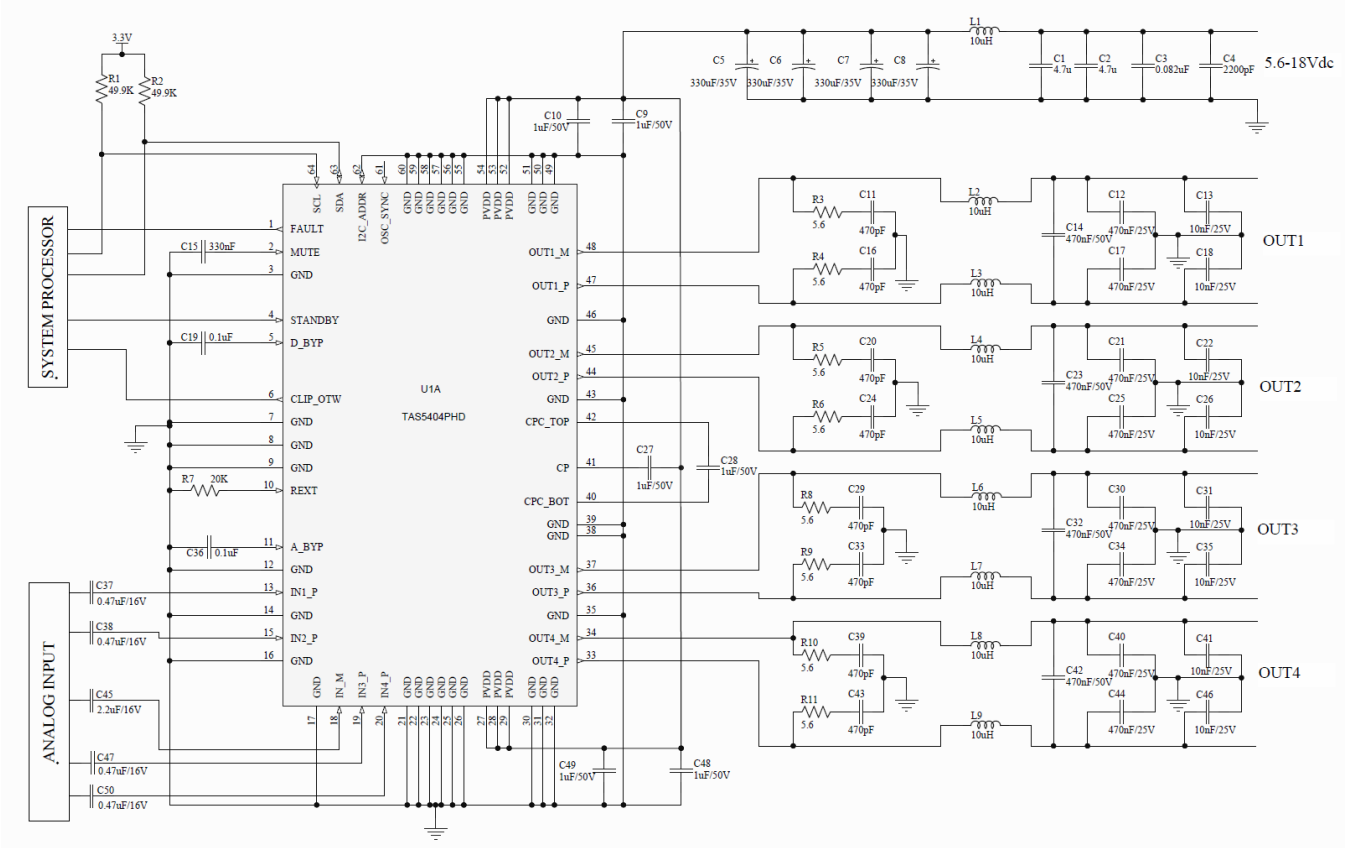


Figure 20. TAS5404-Q1 Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

- Power Supplies

  The TAS5404-Q1 device requires only a single power supply compliant with the recommended operation range. The TAS5404-Q1 device is designed to work with either a vehicle battery or regulated boost power supply.
- Communication

  The TAS5404-Q1 device communicates with the system controller with both discrete hardware control pins and with I^2C. The TAS5404-Q1 device is an I^2C slave and thus requires a master. If a master I^2C-compliant device is not present in the system, the TAS5404-Q1 device can only be used with the default settings. Diagnostic information is limited to the discrete reporting FAULT pin.
- External Components

  Table 24 lists the components required for the TAS5404-Q1 device.

Table 24. Supporting Components

EVM Designator	Quanity	Value	Size	Description	Use in Application
C37, C38, C47, C50	4	0.47μF ± 10%	1206	Film, 16-V	Analog audio input filter, bypass
C5, C6, C7, C8	4	330 μF ± 20%	10 mm	Low-ESR aluminum capacitor, 35-V	Power supply
C9, C10, C48, C49, C27, C28	6	1 μF ± 10%	0805	X7R ceramic capacitor, 50-V	Power supply
C45	1	2.2uF ± 10%	0805	Film, 16-V	Analog audio input filter, bypass
C14, C23, C32, C42	4	470nF ± 10%	0805	X7R ceramic capacitor, 50-V	Amplifier output filtering
C11, C15, C20, C24, C29, C33, C39, C43	8	470 pF ± 10%	0603	X7R ceramic capacitor, 50-V	Amplifier output snubbers
C19, C36	2	0.1 μF ± 10%	0603	X7R ceramic capacitor, 25-V	Power supply
C4	1	2200 pF ± 10%	0603	X7R ceramic capacitor, 50-V	Power supply
C3	1	0.082 μF ± 10%	0603	X7R ceramic capacitor, 25-V	Power supply
C1, C2	2	4.7 μF ± 10%	1206	X7R ceramic capacitor, 25-V	Power supply
C12, C17, C21, C25, C30, C34, C40, C44	8	0.47 μF ± 10%	0603	X7R ceramic capacitor, 25-V	Output EMI filtering
C15	1	220nF ± 10%	0603	X7R ceramic capacitor, 25-V	Mute timing
L1	1	10 μH ± 20%	13.5 mm ×13.5 mm	Shielded ferrite inductor	Power supply
L2, L3, L4, L5, L6, L7, L8, L9	8	10 μH ± 20%	12 mm × 14 mm	Dual inductor	Amplifier output filtering
R1, R2	2	49.9 kΩ ± 1%	0805	Resistors, 0.125-W	Analog audio input filter
R3, R4, R5, R6, R8, R9, R10, R11	8	5.6 Ω ± 5%	0805	Resistors, 0.125-W	Output snubbers
R7	1	20.0 kΩ ± 1%	0805	Resistors, 0.125-W	Power supply

10.2.2 Detailed Design Procedure

10.2.2.1 Hardware and Software Design

1. Hardware Schematic Design: Using Figure 20 as a guide, integrate the hardware into the system schematic.
2. Following the recommended layout guidelines, integrate the TAS5404-Q1 device and the supporting components into the system PCB file.
3. Thermal Design: The TAS5404-Q1 device has an exposed thermal pad which requires proper soldering. For more information, see the application reports *Semiconductor and IC Package Thermal Metrics* (SPRA953), and the *PowerPAD Thermally Enhanced Package* (SLMA002G).
4. Develop software: The EVM User's Guide has detailed instructions for how to set up the TAS5404-Q1 device, interpret diagnostic information, and so forth. For information about control registers, see the *Table 7* section.

For questions and support go to the E2E forums.

10.2.2.2 Parallel Operation (PBTL)

The TAS5404-Q1 device can drive more current by paralleling BTL channels on the load side of the LC output filter. Parallel operation requires identical I^2C settings for any two paralleled channels to have reliable system performance and even power dissipation on multiple channels. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, and so on) should be sent to the paralleled channels at the same time. The TAS5404-Q1 device also supports load diagnostics for parallel connection. Paralleling on the TAS5404-Q1 device side of the LC output filter is not supported, because it can result in device failure. When paralleling channels, use the parallel BTL I^2C control bits in register 0x0D. Parallel channels 1 and 2, and/or channels 3 and 4. Setting these bits allows the thermal foldback to react on both channels equally. Provide the audio input to channel 2 if paralleing channels 1 and 2, and channel 3 if paralleling channels 3 and 4.

10.2.2.3 Input Filter Design

The IN_M pin should have an impedance to GND that is equivalent to the parallel combination of the input impedances of all IN_P channels combined, including any source impedance from the previous stage in the system design. For example, if each of the four IN_P channels have a 1-µF dc blocking capacitor, 1 kΩ of series resistance due to an input RC filter, and 1 kΩ of source resistance from the DAC supplying the audio signal, then the IN_M channel should have a 4-µF capacitor in series with a 500-Ω resistor to GND (4 × 1 µF in parallel = 4 µF; 4 × 2 kΩ in parallel = 500 Ω).

10.2.2.4 Amplifier Output Filtering

The output FETs drive the amplifier outputs in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. The amplifier outputs require a low-pass filter to filter out the PWM modulation carrier frequency. People frequently call the filter the L-C filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole low-pass filter. The L-C filter attenuates the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which the load draws from the power supply. See the *Class-D LC Filter Design* application report (SLOA119) for a detailed description on proper component selection and design of an L-C filter based upon the desired load and response.

10.2.2.5 Line Driver Applications

In many automotive audio applications, the end user would like to use the same head unit to drive either a speaker (with several ohms of impedance) or an external amplifier (with several kilohms of impedance). The design is capable of supporting both applications; however, the one must design the output filter and system to handle the expected output load conditions.

10.2.3 Application Curves

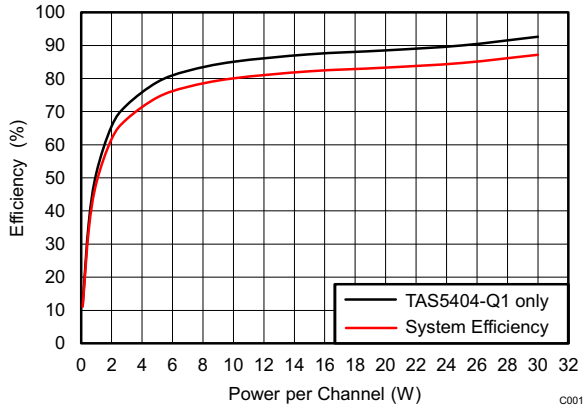


Figure 21. Efficiency
Four Channels AT 4 Ω Each

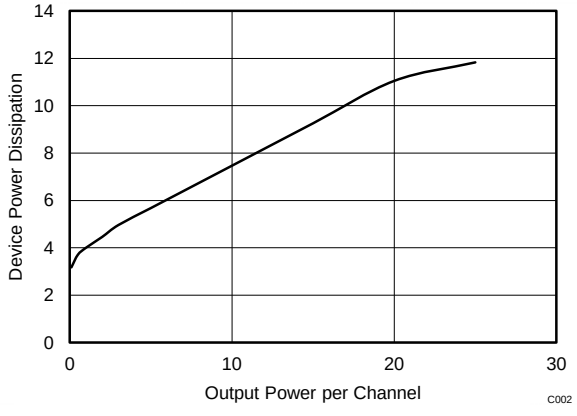


Figure 22. TAS5404-Q1 Device Power Dissipation
Four Channels at 4 Ω Each

11 Power Supply Recommendations

A car battery that can have a large voltage range most commonly provides the power for the TAS5404-Q1 device. PVDD is a filtered battery voltage, and it is the supply for the output FETS and the low-side FET gate driver. The supply for the high-side FET gate driver comes from a charge pump (CP). The charge pump supplies the gate-drive voltage for all four channels. An internal linear regulator provides AVDD which powers the analog circuitry. The supply requires a 0.1-µF, 10-V external bypass capacitor at the A_BYP pin. TI does not recommend connecting any external components except the bypass capacitor to the A_BYP pin. DVDD, which comes from an internal linear regulator, powers the digital circuitry. The D_BYP pin requires a 0.1-µF, 10-V external bypass capacitor. TI does not recommend connecting any external components except the bypass capacitor to the A_BYP pin.

The TAS5404-Q1 device can withstand fortuitous open-ground and open-power conditions. Fortuitous open ground usually occurs when a speaker wire shorts to ground, which allows for a second ground path through the body diode in the output FETs. The diagnostic capability allows debugging of the speakers and speaker wires, which eliminates the necessity to remove the amplifier to diagnose the problem.

12 Layout

12.1 Layout Guidelines

- The EVM layout optimizes for low noise and EMC performance.
- The TAS5404-Q1 device has a thermal pad up, so a the layout must take into account an external heatsink.
- Layout also affects EMC performance.
- The EVM PCB illustrations form the basis for the layout discussions.

12.2 Layout Example

The areas in Figure 23 and Figure 24 indicated by the label "A", are critical to proper operation and EMC layout. The PVDD and ground-decoupling capacitors should be close to the TAS5404-Q1 device. These ground-decoupling capacitors must be on both groups of PVDD pins to ground. The ground connections of the snubber circuits must also be close to the grounds of the TAS5404-Q1 device.

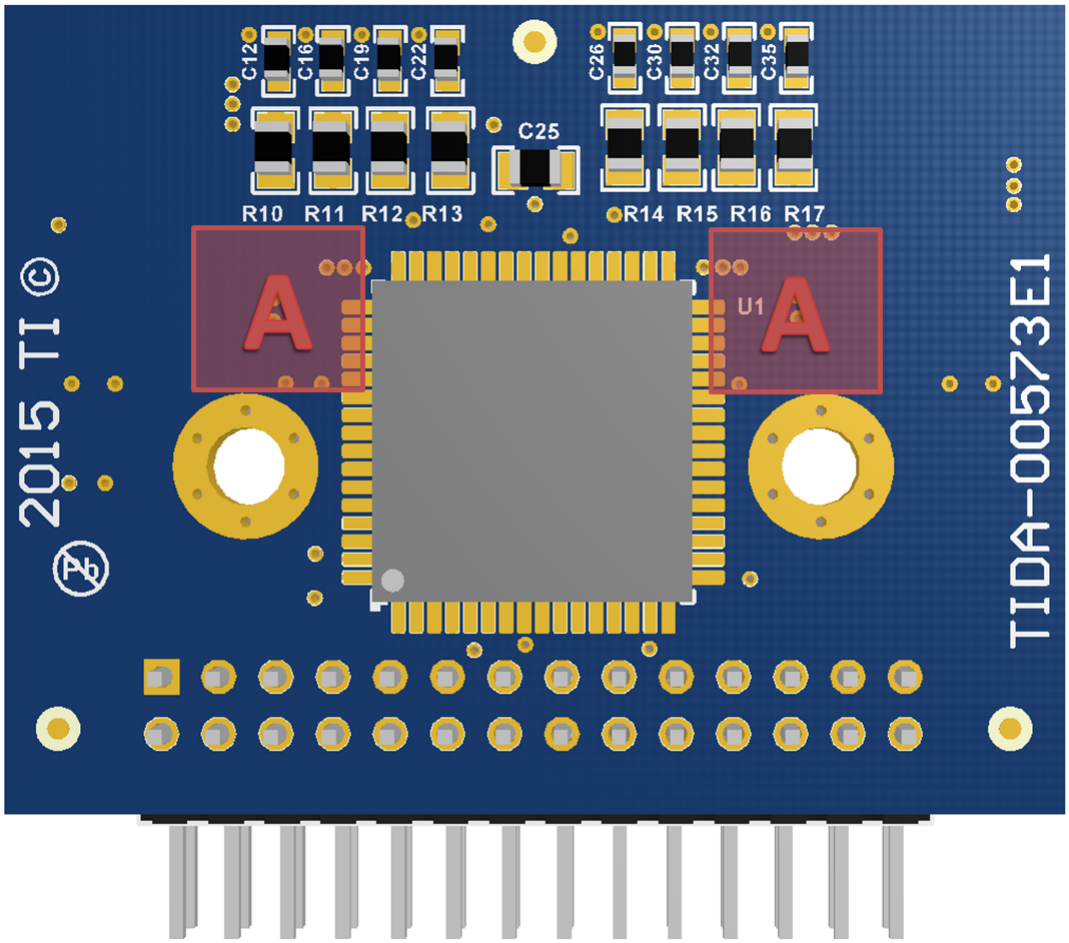


Figure 23. TAS5404 Board Layout - Top View

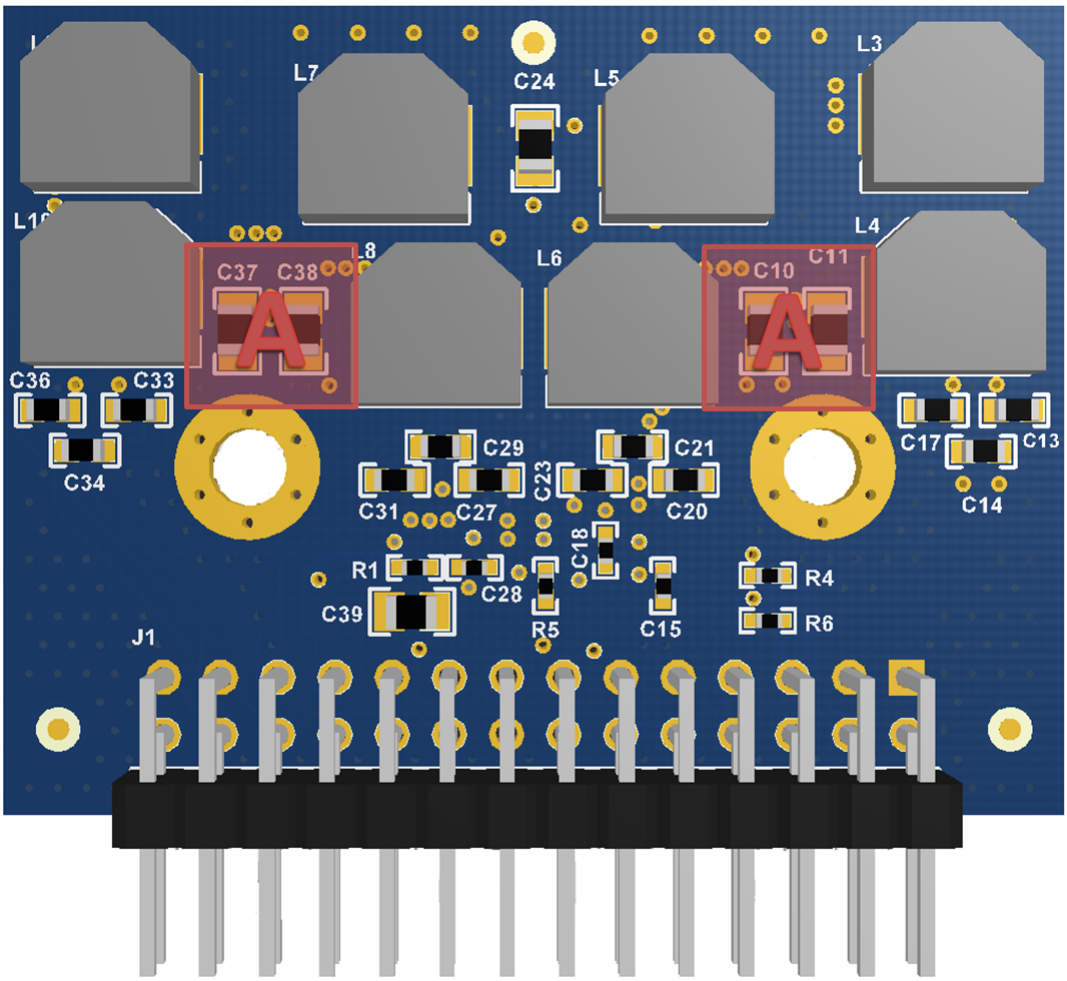


Figure 24. TAS5404 Board Layout - Bottom View

Each layer in the EVM contains a ground plane. All the ground planes should be connected together through many vias to reduce the impedance between the ground layers, which provides for low inductance paths for reduced EMI.

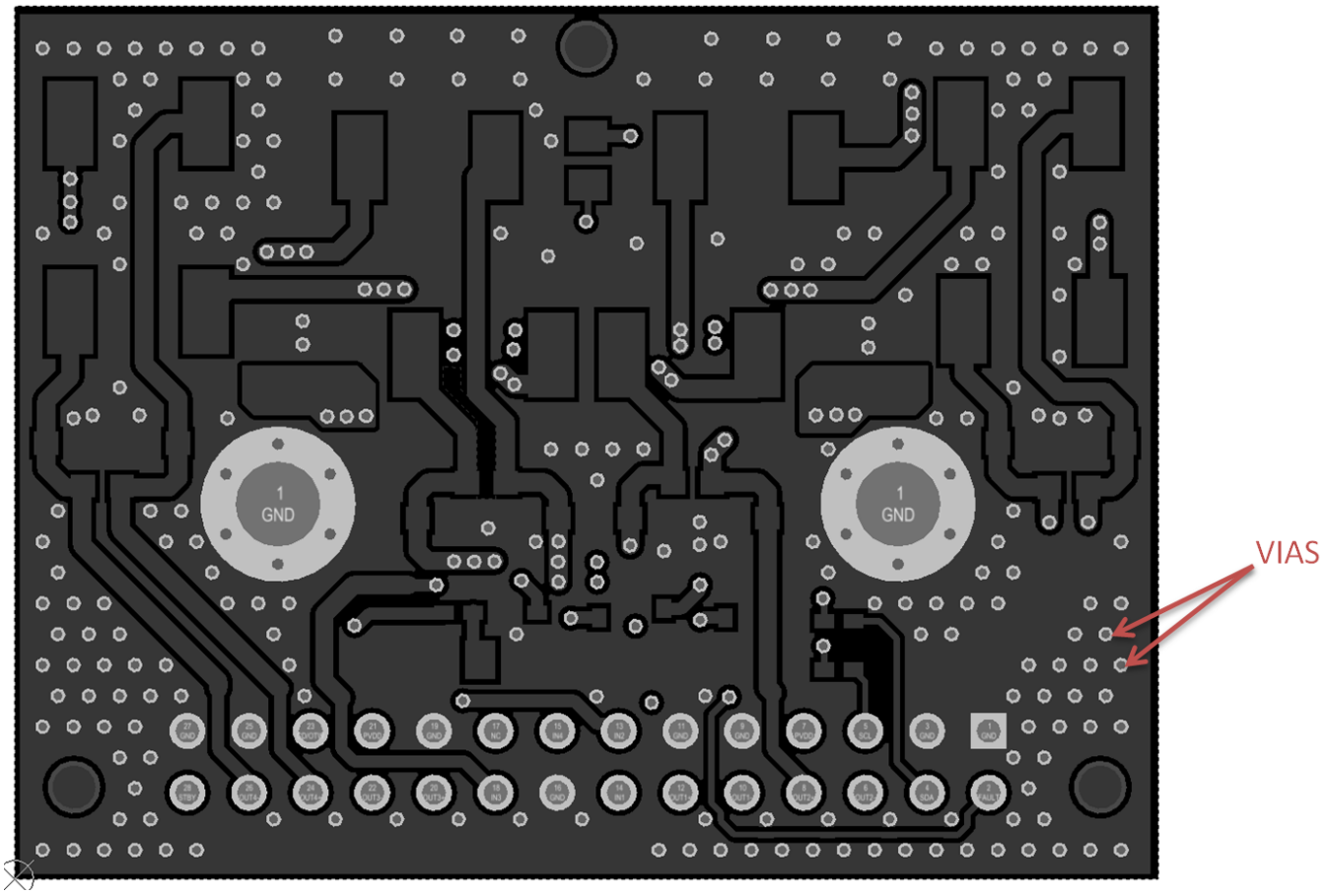


Figure 25. TAS5404 Board Layout - Bottom Layer

12.3 Thermal Consideration

The design of the thermally augmented package is to interface directly to heat sinks using a thermal interface compound (for example, Arctic Silver®, Ceramique thermal compound). The heat sink then absorbs heat from the ICs and couples it to the local air. With proper thermal management the process can reach equilibrium at a lower temperature, and heat can be continually removed from the ICs. Because of the efficiency of the TAS5404-Q1 device, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal resistance of the thermal grease
- Thermal resistance of the heat sink

One can calculate the thermal resistance of the thermal grease from the exposed heat slug area and the manufacturer's value for the area thermal resistance of the thermal grease (expressed in °C-in^2/W or °C-mm^2/W). The area thermal resistance of the example thermal grease with a 0.001-inch (0.0254-mm) thick layer is about 0.007°C-in^2/W (4.52°C-mm^2/W). The approximate exposed heat slug size for a 64-pin QFP is 0.099 in^2 (64 mm^2)

Dividing the example area thermal resistance of the thermal grease by the area of the heat slug gives the actual resistance through the thermal grease for both parts, which is 0.07°C/W.

The thermal resistance of thermal pads is generally considerably higher than a thin thermal-grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. The heat-sink vendor generally predicts heat sink thermal resistance, either modeled using a continuous-flow dynamics (CFD) model, or measured.

Therefore, for a single monaural channel in the IC, the system $R_{\theta JA}$ = $R_{\theta JC}$ + thermal-grease resistance + heat-sink resistance.

Table 25 indicates modeled parameters for one TAS5404-Q1 device on a heat sink. The exposed pad dimensions are 8 mm × 8 mm. The junction temperature setting is at 115°C while delivering 20 watts per channel into 4-Ω loads with no clipping. The assumed thickness of the thermal grease is about 0.001 inches (0.0254 mm).

Table 25. QFP Package Modeled Parameters

DEVICE	64-PIN QFP	UNIT
Ambient temperature	25	°C
Power to load	20	W × 4
Power dissipation	1.9	W × 4
ΔT inside package	7.6	°C
ΔT through thermal grease	0.46	°C
Required heatsink thermal resistance	10.78	°C/W
Junction temperature	115	°C
System $R_{\theta JA}$	11.85	°C/W
$R_{\theta JA}$ × power dissipation	90	°C

12.4 Electrical Connection of Heat Slug and Heat Sink

Electrically connect the heat sink attached to the heat slug of the TAS5404-Q1 device to GND, or leave it floating. Do not connect the heat slug to any other electrical node.

12.5 EMI Considerations

Automotive-level EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

EMI Considerations (接下页)

The design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The phase between channels is I^2C selectable to either 45° or 180°, to reduce EMI caused by high-current switching. The design also incorporates circuitry that optimizes output transitions that cause EMI.

13 器件和文档支持

13.1 器件支持

13.1.1 Third-Party Products Disclaimer

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13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5404TPHDRQ1	ACTIVE	HTQFP	PHD	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TAS5404TQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

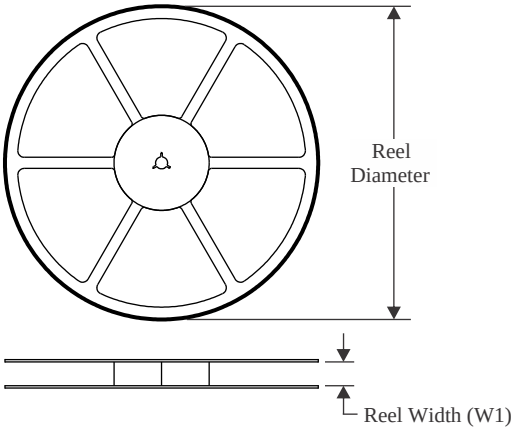
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

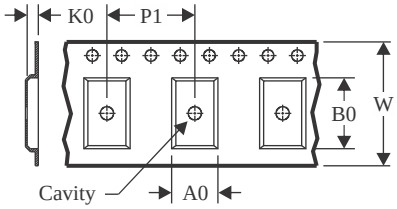
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

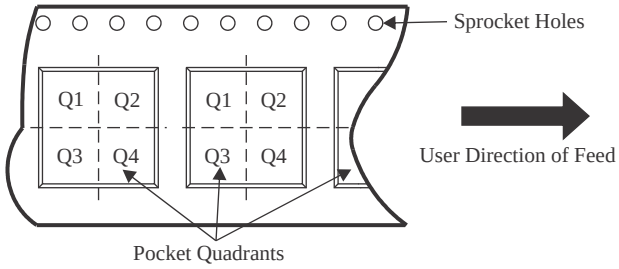


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

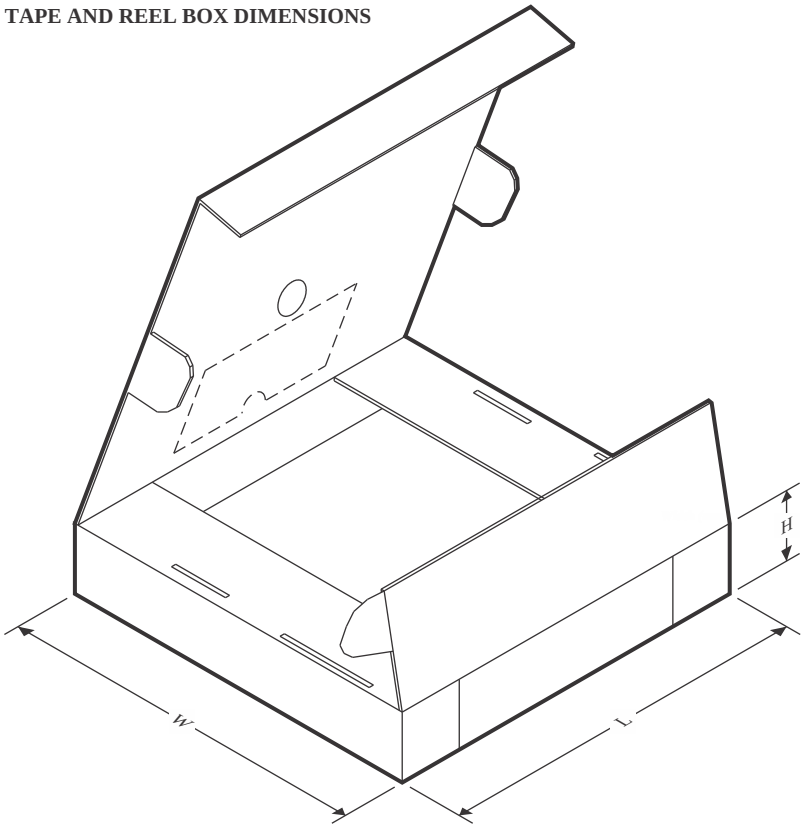
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5404TPHDRQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5404TPHDRQ1	HTQFP	PHD	64	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

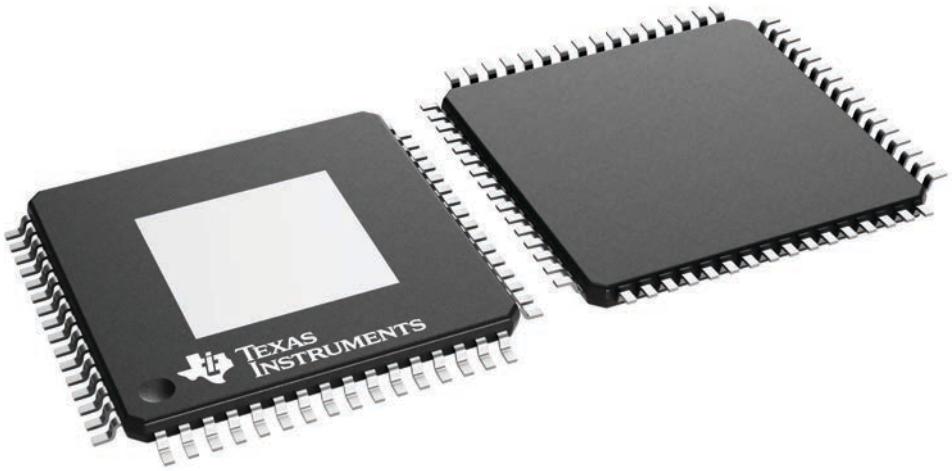
PHD 64

HTQFP - 1.2 mm max height

14 x 14, 0.8 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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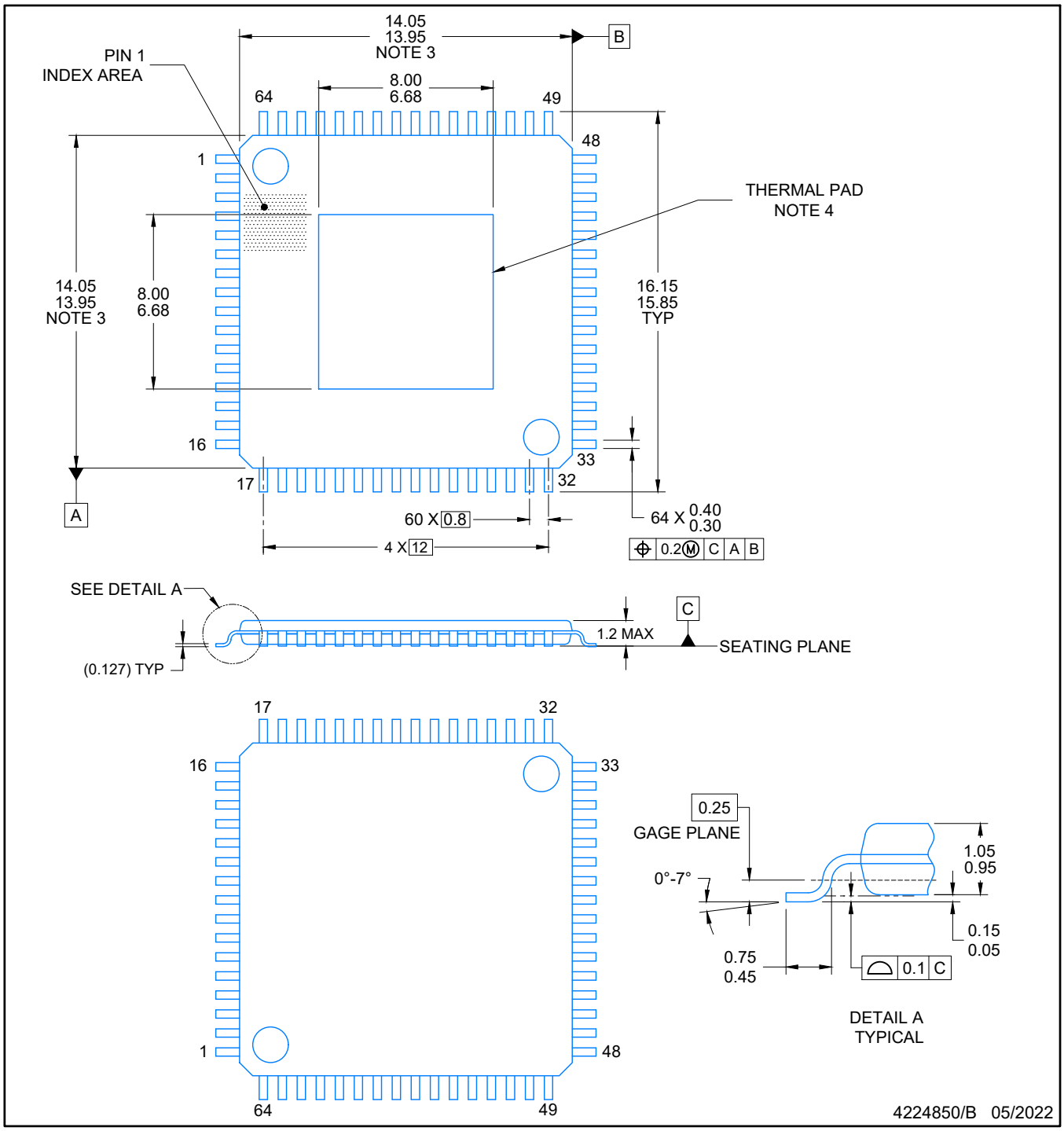
PACKAGE OUTLINE

PHD0064B

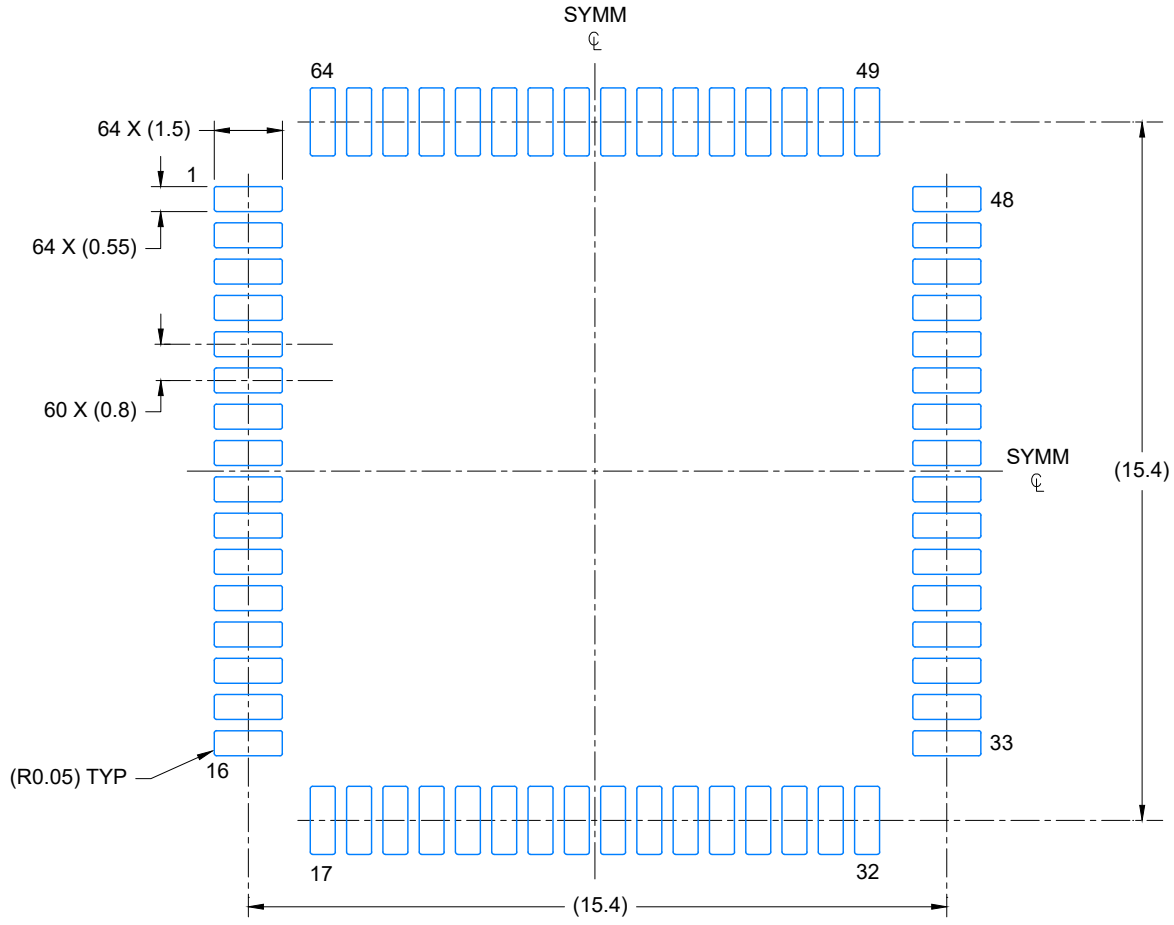
HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

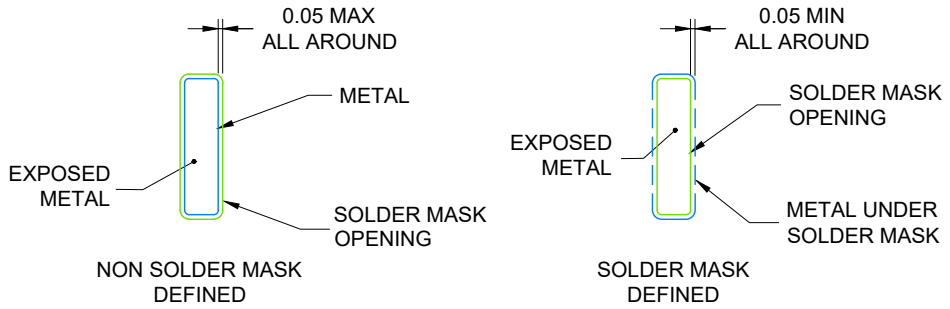


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



SOLDER MASK DETAILS

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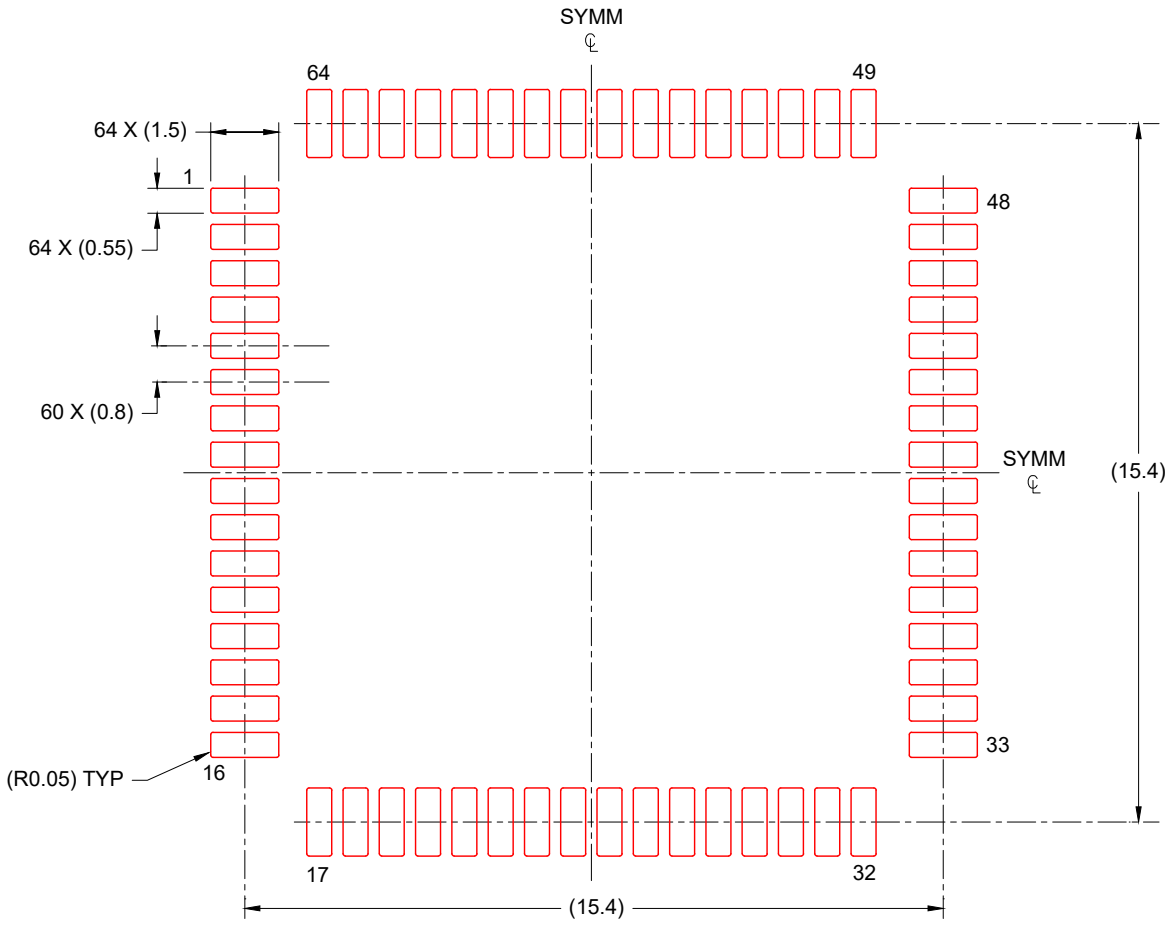
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
SCALE: 6X

4224850/B 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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