具有待机模式和 1.8V IO 支持的 TCAN1044V 故障保护 CAN FD 收发器

1 特性

- 符合 ISO 11898-2:2016 和 ISO 11898-5:2007 物理层标准的要求
- 支持传统 CAN 和经优化的 CAN FD 性能（数据速率为 2、5 和 8Mbps）
  - 具有较短的对称传播延迟时间和快速循环次数，可增加时序裕量
  - 在有负载 CAN 网络中实现更快的数据速率
- IO 电压范围支持 1.7V 至 5.5V
  - 支持 1.8V、2.5V、3.3V 和 5V 应用
- 总环路延迟 ≤ 210ns
- 小尺寸 SOT-23 封装 (2.9mm x 1.60mm)
- 接收器共模输入电压：±12V
- 保护 功能：
  - 总线故障保护：±58V
  - 欠压保护
  - 总线引脚限流
  - TXD 显性超时 (DTO)
    - 数据速率低至 9.2kbps
  - 热关断保护 (TSD)
- 工作模式：
  - 正常模式
  - 支持远程唤醒请求功能的低功耗待机模式
- 优化了未上电时的性能
  - 总线和逻辑引脚为高阻抗（运行总线或应用上无负载）
  - 支持热插拔：在总线和 RXD 输出上可实现上电/断电无干扰运行
- 结温范围：-40°C 至 150°C

2 应用

- 电网基础设施
- 工业运输（非汽车和非轻型卡车）
- 工厂自动化与控制
- 电器

3 说明

TCAN1044V 是一款符合 ISO 11898-2:2016 高速 CAN 规范物理层要求的高速控制器局域网 (CAN) 收发器。

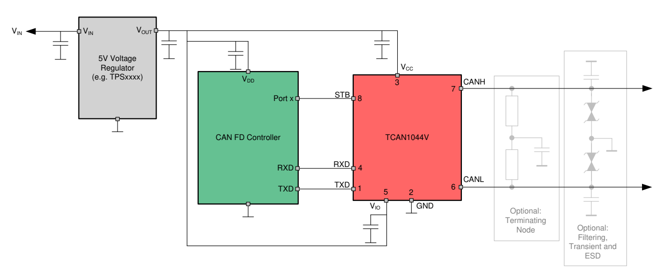
TCAN1044V 收发器支持传统 CAN 和 CAN FD 网络（数据速率高达 8 兆位/秒 (Mbps)）。TCAN1044V 包括通过 V_{IO} 端子实现的内部逻辑电平转换功能，允许将收发器 IO 直接连接到 1.8V、2.5V、3.3V 或 5V 逻辑 IO。该收发器具有低功耗待机模式，可通过 ISO 11898-2:2016 定义的唤醒模式 (WUP) 实现远程唤醒。TCAN1044V 收发器还包括许多保护和诊断 功能 ，其中包括热关断 (TSD)、TXD 显性超时 (DTO)、电源欠压检测和高达 ±58V 的总线故障保护。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TCAN1044V	SOT (8)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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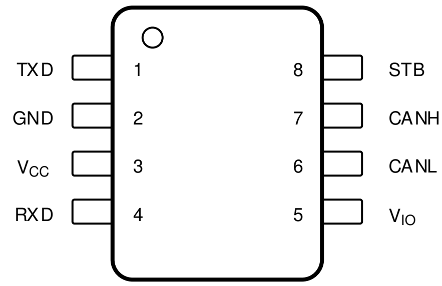
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 12 月	*	高级信息

5 Pin Configuration and Functions

DDF Package
8-Pin SOT
Top View



Not to scale

Pin Functions

Pins		Type	Description
Name	No.		
TXD	1	Digital Input	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	Supply	5-V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-state when powered off
V_{IO}	5	Supply	IO supply voltage
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby input for mode control, integrated pull-up

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage IO level shifter	–0.3	6	V
V_{BUS}	CAN Bus IO voltage CANH and CANL	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL	–45	45	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Operating virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential IO bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±3000	V
			HBM classififation level 3B for global pins CANH & CANL	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings

				VALUE	UNIT
V_{ESD}	System Level Electro-Static Discharge (ESD)(1)	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10650 Powered Contact Discharge	±8000	V
			SAE J2962-2 per ISO 10650 Powered Air Discharge	±15000	V
V_{Tran}	ISO 7637 ISO Pulse Transients(2)	CAN bus terminals (CANH, CANL)	Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	ISO 7637 Slow transients pulse(3)	CAN bus terminals (CANH, CANL) to GND	DCC slow transient pulse	±85	V

(1) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(2) Tested according to IEC 62228-3:2019 CAN Transcievers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(3) Tested according to ISO 7637-3 (2017); Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for IO level shifter	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current	–2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA
T_A	Operating ambient temperature	–40		125	℃

6.5 Thermal Characteristics

THERMAL METRIC		TCAN1044V DDF (SOT)	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	128.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	68.3	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	71.6	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	19.7	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	70.8	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

6.6 Supply Characteristics

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant	See 图 5,TXD = 0 V, STB = 0 V, R_L = 60 Ω, C_L = open		45	70	mA
			See 图 5, TXD = 0 V, STB = 0 V, R_L = 50 Ω, C_L = open		49	80	mA
		Recessive	See 图 5, TXD = V_{CC}, STB = 0 V, R_L = 50 Ω, C_L = open, RCM = open		4.5	7.5	mA
		Dominant with bus fault	See 图 5, TXD = 0 V, STB = 0 V, CANH = CANL = ±25 V, R_L = open, C_L = open			130	mA
I_{CC}	Supply current standby mode		TXD = STB = V_{IO} R_L = 50 Ω, C_L = open See 图 5		0.2	1	µA
I_{IO}	IO supply current normal mode	Dominant	TXD = 0 V, STB= 0 V RXD floating		125	300	µA
I_{IO}	IO supply current normal mode	Recessive	TXD = 0 V, STB = 0 V RXD floating		25	48	µA
I_{IO}	IO supply current standby mode		TXD = 0 V, STB = V_{IO} RXD floating		8.5	13.5	µA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.4	V
UV_{VCC}	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.25	V
UV_{VIO}	Rising under voltage detection on V_{IO}				1.56	1.65	V
UV_{VIO}	Falling under voltage detection on V_{IO}			1.4	1.51	1.59	V

6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		110		mW
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		110		mW
		V_{CC} = 5 V, V_{IO} = 5 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		110		mW
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_A= 125°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_A= 125°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle squarewave, C_{L_RXD} = 15 pF		120		mW
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

6.8 Electrical Characteristics

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics					

Electrical Characteristics (continued)

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(DOM)}$	Dominant output voltage normal mode	CANH	See 图 6 and 图 13, TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage normal mode	CANH and CANL	See 图 6 and 图 13, TXD = V_{IO}, STB = 0 V, R_L = open (no load), R_{CM} = open	2	0.5 V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		See 图 6 and 图 17, STB = 0 V, R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open, R_{CM} = open, TXD = 250 kHz, 1 MHz, 2.5 MHz	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		See 图 6 and 图 13, STB = 0 V, R_L = 60 Ω, C_L = open	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage normal mode Dominant	CANH - CANL	See 图 6 and 图 13, TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open	1.5		3	V
			See 图 6 and 图 13, TXD = 0 V, STB = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open	1.4		3.3	V
			See 图 6 and 图 13, TXD = 0 V, STB = 0 V, R_L = 2240 Ω, C_L = open	1.5		5	V
$V_{OD(REC)}$	Differential output voltage normal mode Recessive	CANH - CANL	See 图 6 and 图 13, TXD = V_{IO}, STB = 0 V, R_L = 60 Ω, C_L = open	–120		12	mV
			See 图 6 and 图 13, TXD = V_{IO}, STB = 0 V, R_L = open, C_L = open	–50		50	mV
$V_{O(STB)}$	Bus output voltage standby mode	CANH	See 图 6 and 图 13, STB = V_{IO}, R_L = open (no load), R_{CM} = open	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant, normal mode		See 图 11 and 图 13, STB = 0 V, $V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD = 0 V	–115			mA
			See 图 11 and 图 13, STB = 0 V, $V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open, TXD = 0 V			115	mA
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive, normal mode		See 图 11 and 图 13, STB = 0 V, –27 V ≤ V_{BUS} ≤ 32 V, Where V_{BUS} = CANH = CANL, TXD = V_{IO}	–6		6	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage normal mode		See 图 7, 表 1, and 表 6 STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V	500		900	mV
$V_{IT(STB)}$	Input threshold standby mode		See 图 7, 表 1, and 表 6 STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V	400		1150	mV
V_{DOM}	Normal mode dominant state differential input voltage range		See 图 7, 表 1, and 表 6 STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V	0.9		9	V
V_{REC}	Normal mode recessive state differential input voltage range		See 图 7, 表 1, and 表 6 STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V	-4		0.5	V
$V_{DOM(STB)}$	Standby mode dominant state differential input voltage range		See 图 7, 表 1, and 表 6 STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V	1.15		9	V
$V_{REC(STB)}$	Standby mode recessive state differential input voltage range		See 图 7, 表 1, and 表 6 STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold normal mode		See 图 7, 表 1, and 表 6 STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V		100		mV
V_{CM}	Common mode range normal and standby modes		See 图 7 and 表 6	–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current		CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	μA
C_I	Input capacitance to ground (CANH or CANL)		TXD = V_{IO}			20	pF
C_{ID}	Differential input capacitance					10	pF
R_{ID}	Differential input resistance		TXD = V_{IO} STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)			20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %		$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V	–1		1	%
TXD Terminal (CAN Transmit Data Input)							
V_{IH}	High-level input voltage			0.7 V_{IO}			V
V_{IL}	Low-level input voltage					0.3 V_{IO}	V

Electrical Characteristics (continued)

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{CC}= V_{IO} = 5.5 V	–200	-100	–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC}= V_{IO} = 0 V	–1	0	1	µA
C_I	Input Capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level input voltage	See 图 7, I_O = –2 mA	0.8 V_{IO}			V
V_{OL}	Low-level input voltage	See 图 7, I_O = 2 mA			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{CC}= V_{IO} = 0 V	–1	0	1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage		0.7 V_{IO}			V
V_{IL}	Low-level input voltage				0.3 V_{IO}	V
I_{IH}	High-level input leakage current STB	V_{CC} = V_{IO} = STB = 5.5 V	–2		2	µA
I_{IL}	Low-level input leakage current STB	V_{CC} = V_{IO} = 5.5 V, STB = 0 V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC}= V_{IO} = 0 V	–1	0	1	µA

6.9 Switching Characteristics

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See 图 8, normal mode, V_{IO} = 2.8 V to 5.5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		125	210	ns
		See 图 8, normal mode, V_{IO} = 1.7 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	See 图 8, normal mode, V_{IO} = 2.8 V to 5.5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		150	210	ns
		See 图 8, normal mode, V_{IO} = 1.7 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		180	255	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See 图 9			20	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See 图 15	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value	See 图 15	0.8		6	ms
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	See 图 6, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			20		ns
t_R	Differential output signal rise time			30		ns
t_F	Differential output signal fall time			50		ns
t_{TXD_DTO}	Dominant timeout	See 图 10, R_L = 60 Ω, C_L = 100 pF, STB = 0 V	1.2		4.0	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	See 图 7 STB = 0 V, $C_{L(RXD)}$ = 15 pF		90		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			65		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						

Switching Characteristics (continued)

Over recomended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	See 图 8, STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF STB = 0 V	450		530	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		400		550	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		120		220	ns
t_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-50		20	ns
t_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-45		15	ns

6.10 Typical Characteristics

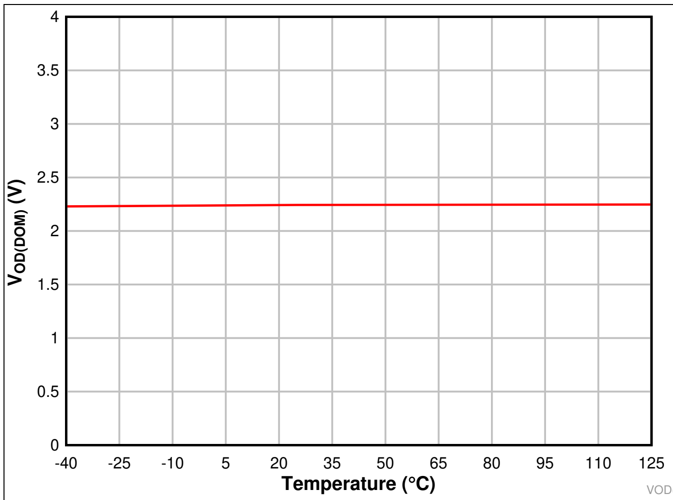


图 1. $V_{OD(DOM)}$ vs Temperature

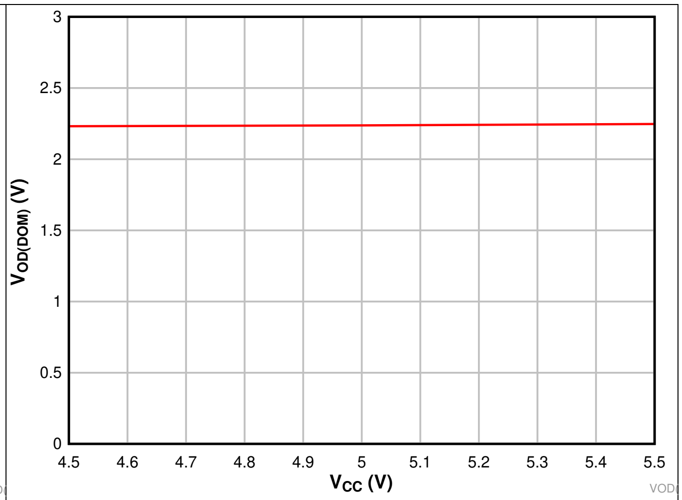


图 2. $V_{OD(DOM)}$ vs V_{CC}

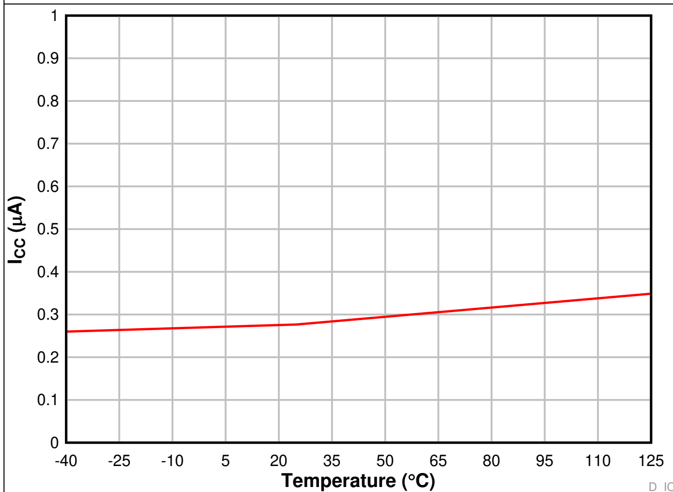


图 3. I_{CC} Standby vs Temperature

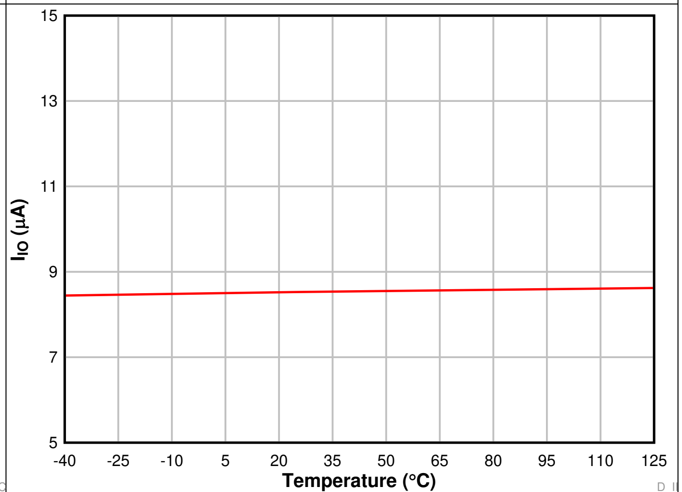


图 4. I_{IO} Standby vs Temperature

7 Parameter Measurement Information

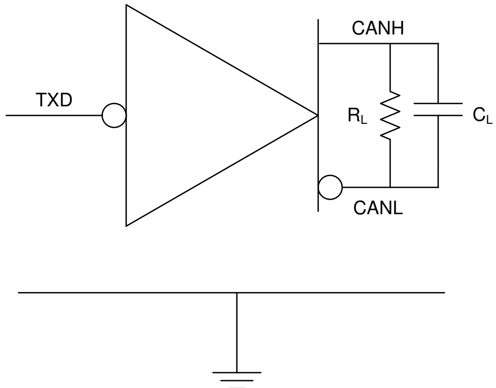


图 5. I_{CC} Test Circuit

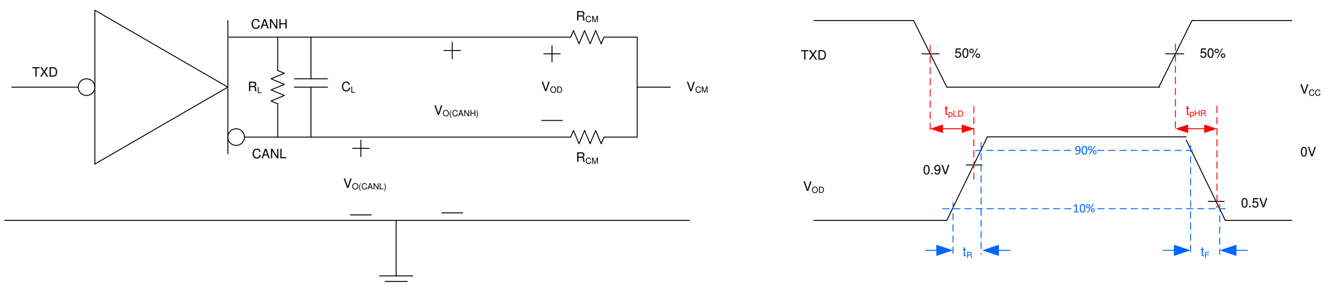


图 6. Driver Test Circuit and Measurement

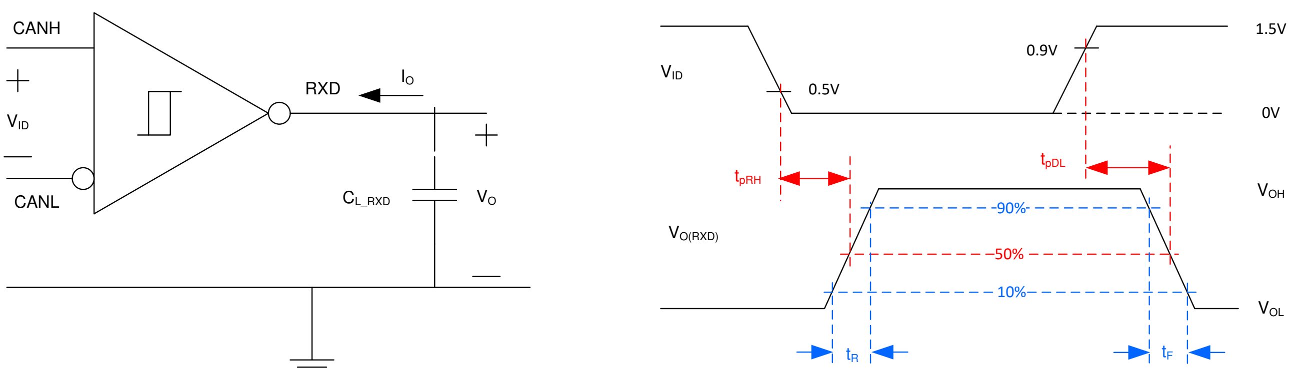


图 7. Receiver Test Circuit and Measurement

Parameter Measurement Information (接下页)

表 1. Receiver Differential Input Voltage Threshold Test (See 图 7)

Input			Output	
V_{CANH}	V_{CANL}	$\|V_{ID}\|$	RXD	
-11.5 V	-12.5 V	1000 mV	L	V_{OL}
12.5 V	11.5 V	1000 mV		
-8.55 V	-9.45 V	900 mV		
9.45 V	8.55 V	900 mV		
-8.25 V	-9.25 V	500 mV	H	V_{OH}
9.25 V	8.25 V	500 mV		
-11.8 V	-12.2 V	400 mV		
12.2 V	11.8 V	400 mV		
Open	Open	X		

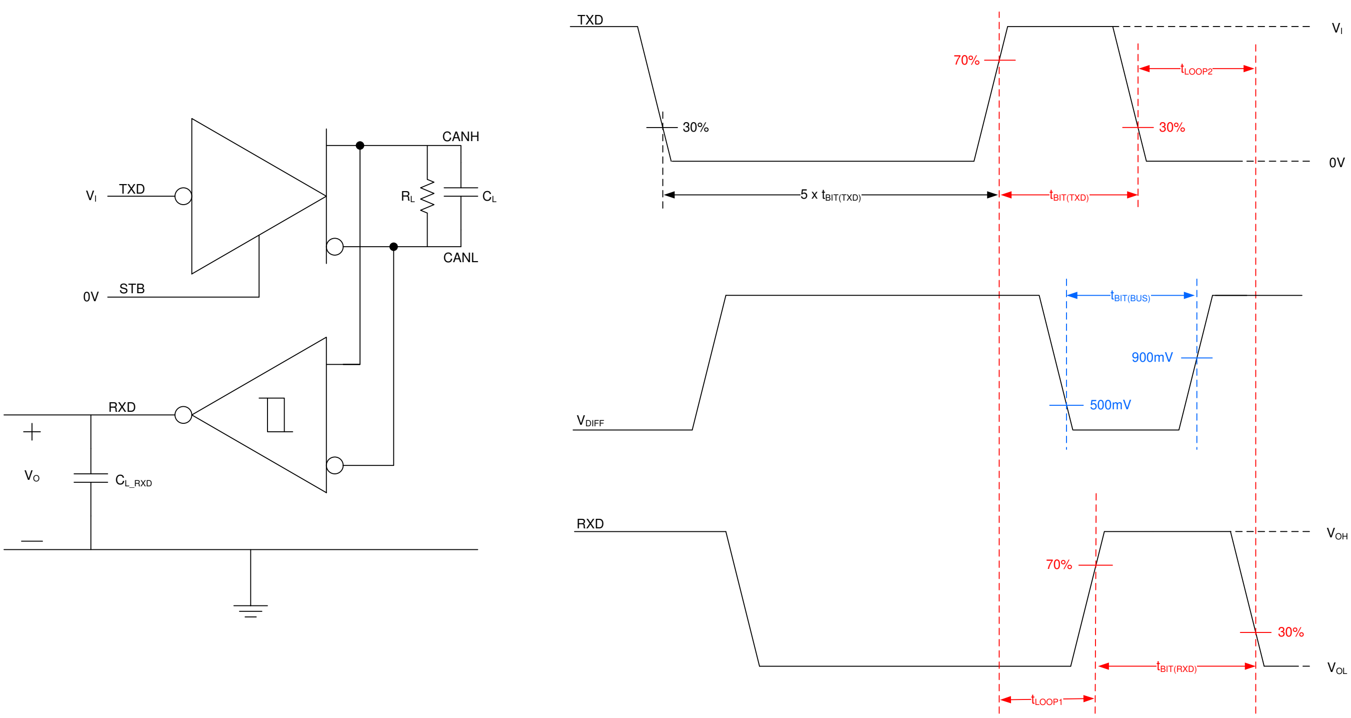


图 8. Transmitter and Receiver Timing Test Circuit and Measurement

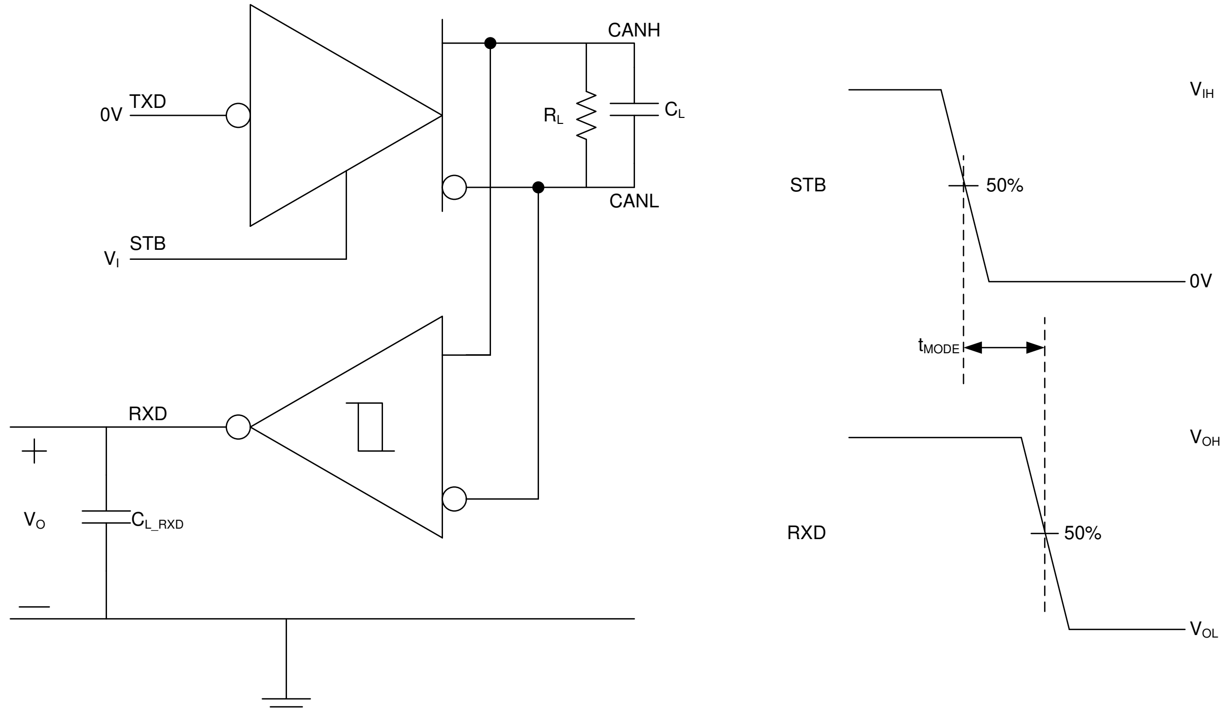


图 9. t_{MODE} Test Circuit and Measurement

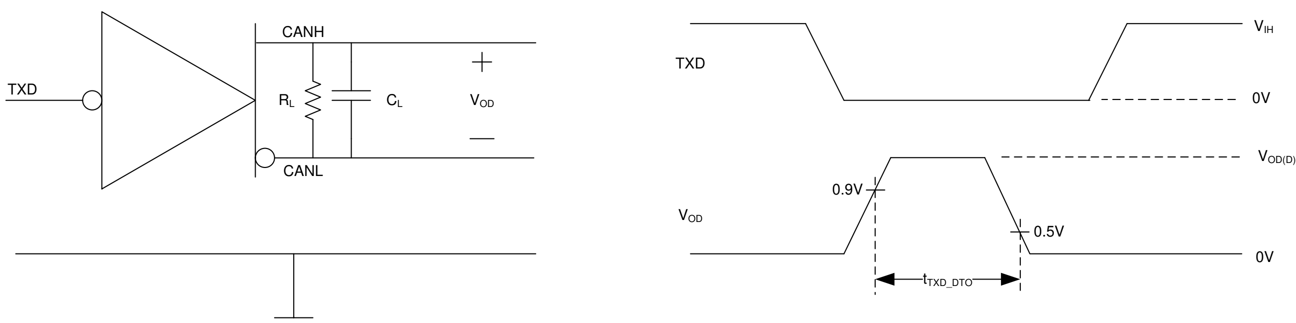


图 10. TXD Dominant Timeout Test Circuit and Measurement

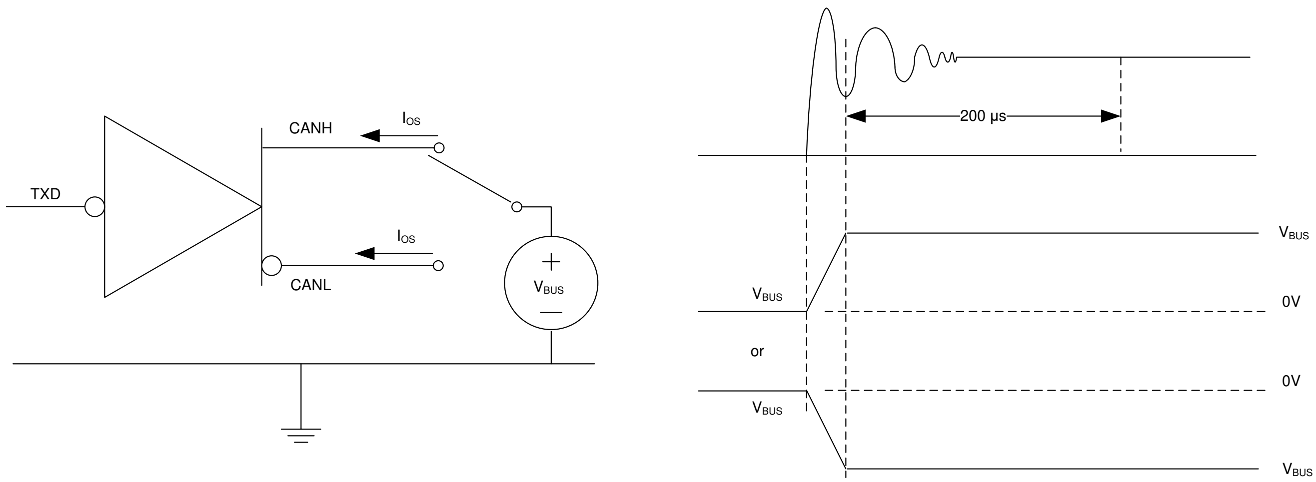


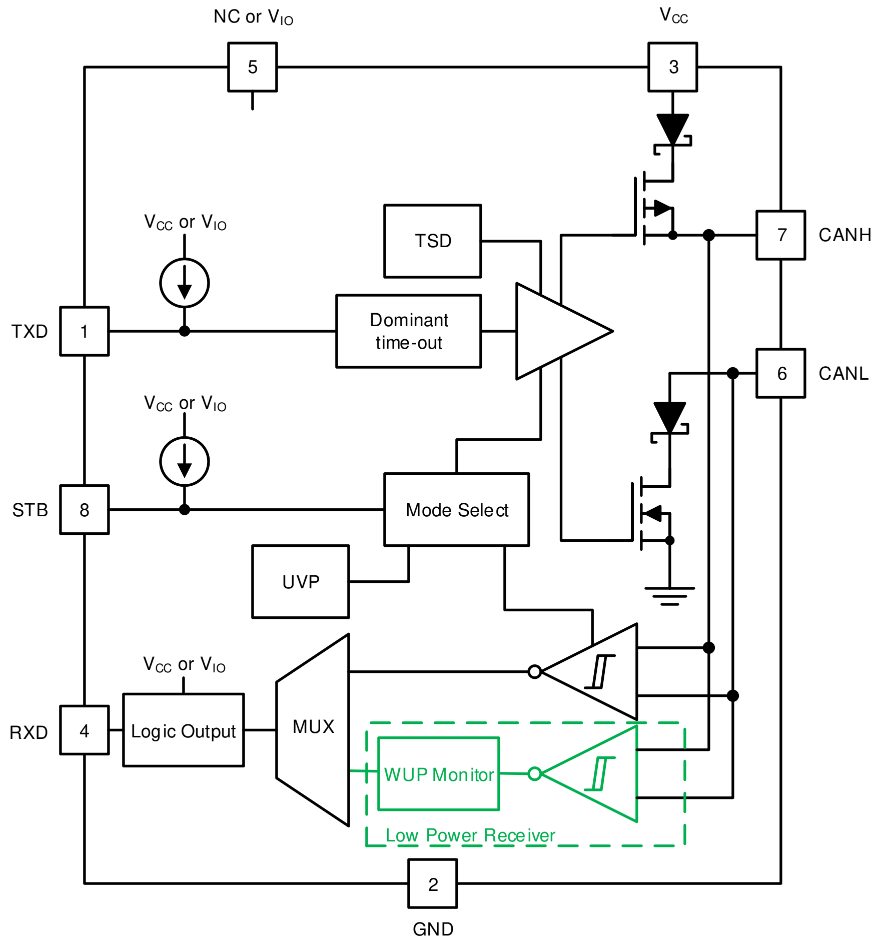
图 11. Driver Short-Circuit Current Test and Measurement

8 Detailed Description

8.1 Overview

The TCAN1044V meets or exceeds the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent industrial system requirements while also supporting CAN FD data rates up to 8 Mbps.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pin Description

8.3.1.1 TXD

TXD is the logic-level signal, referenced to from a CAN controller to the device.

8.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

8.3.1.3 V_{CC}

V_{CC} provides the 5-V nominal power supply to the CAN transceiver.

8.3.1.4 RXD

RXD is the logic-level signal, referenced to , from the TCAN1044V to a CAN controller. This pin is only driven once V_{IO} is present.

8.3.1.5 V_{IO}

The V_{IO} pin provides the digital IO voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports voltages from 1.7 V to 5.5 V providing the widest range of controller support.

8.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

8.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation than the STB pin can be tied directly to GND.

8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 图 12 and 图 13.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1044V transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See 图 12 and 图 13.

Feature Description (接下页)

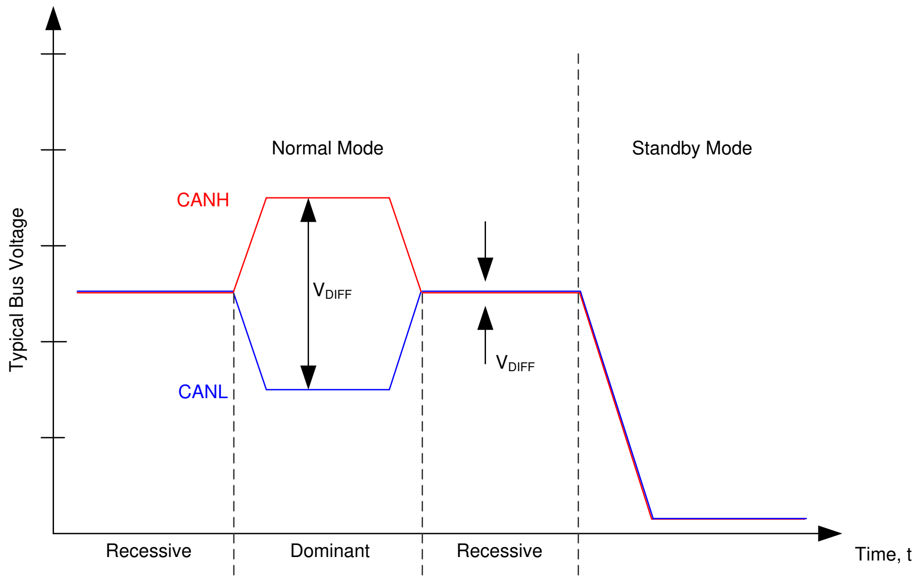
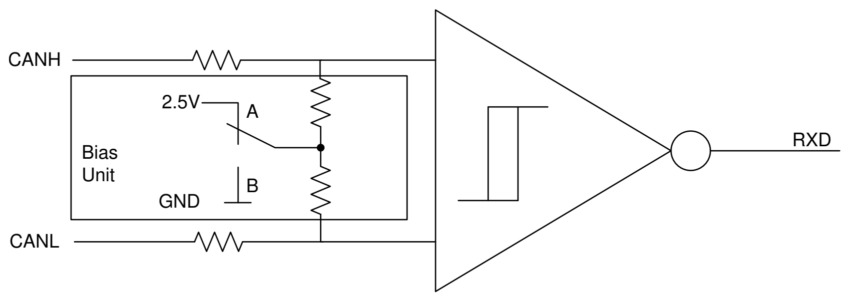


图 12. Bus States



A. Normal Mode

B. Standby Mode

图 13. Simplified Recessive Common Mode Bias Unit and Receiver

8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 公式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

Feature Description (接下页)

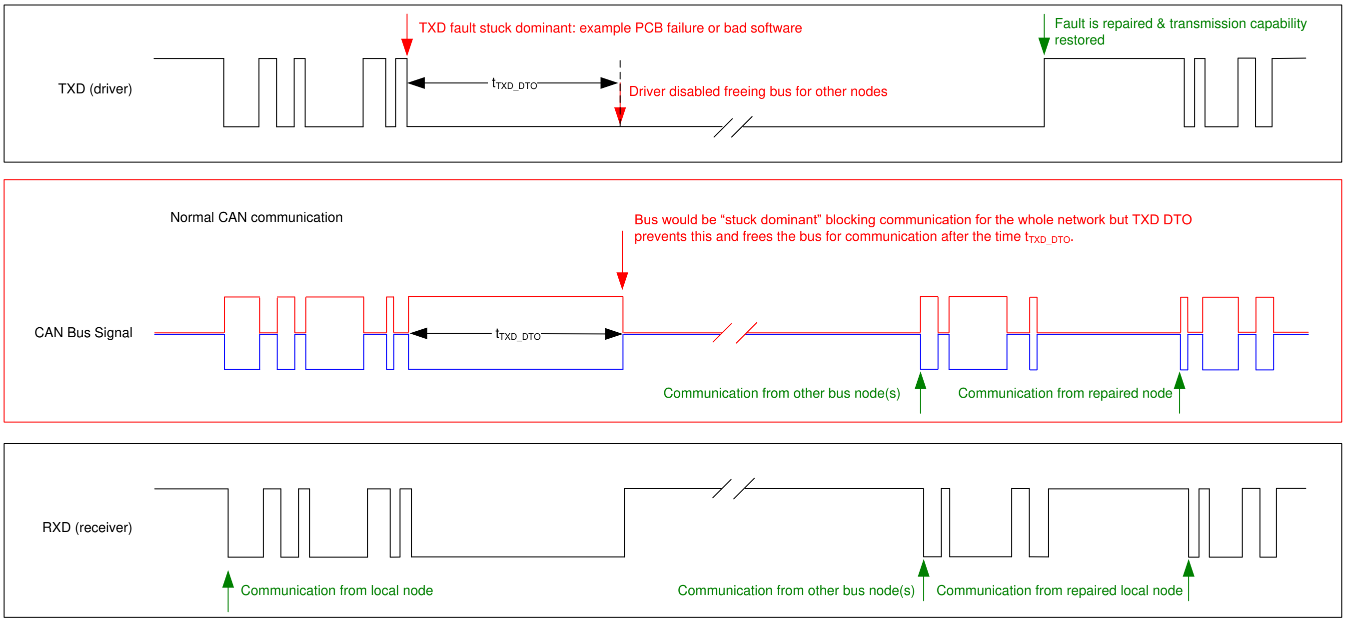


图 14. Example Timing Diagram for TXD Dominant Timeout

8.3.4 CAN Bus Short Circuit Current Limiting

The TCAN1044V has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using 公式 2.

$$I_{OS(AVG)} = \%\ Transmit \times [(\%\ REC\_Bits \times I_{OS(SS)\_REC}) + (\%\ DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%\ Receive \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

This short circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

Feature Description (接下页)

8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1044V exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. If the fault condition that caused the TSD fault is still present, the junction temperature may rise again and the device enters a TSD fault again. The TCAN1044V TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault. If there is prolonged exposure to a TSD fault condition the device reliability could be affected.

8.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

表 2. Undervoltage Lockout - TCAN1044V

V_{CC}	V_{IO}	Device State	Bus	RXD Pin
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: Standby mode	Biased to GND	V_{IO}: Remote wake request(1)
		STB = GND: Protected mode	High impedance	Recessive
> UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance
< UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance

(1) See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

Once an undervoltage condition is cleared and the supply has returned to a valid level the TCAN1044V transitions to normal mode after the t_{MODE} time has expired. The host controller should not attempt to send or receive messages until the t_{MODE} time has expired.

8.3.7 Unpowered Device

The TCAN1044V is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

8.3.8 Floating pins

The TCAN1044V has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open drain outputs are used an adequate external pull-up resistor must be used to ensure that the TXD output of the CAN controller maintains adequate bit timing to the input of the CAN transceiver. See 表 3 for details on pin bias conditions.

表 3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

8.4 Device Functional Modes

8.4.1 Operating Modes

The TCAN1044V has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin on the TCAN1044 device.

表 4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See section 8.3.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

8.4.2 Normal Mode

This is the normal operating mode of the TCAN1044V. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the bus pins. The receiver is translating the differential signal from to a digital output on the RXD output.

8.4.3 Standby Mode

This is the low-power mode of the TCAN1044V. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in 图 15. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see 图 12 and 图 13.

In standby mode, only the V_{IO} supply is required therefore the V_{CC} may be switched off for additional system level current savings.

8.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1044V supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1044V.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See 图 15 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1 Mbps triggers the filter in either bus state. Any CAN frame at 500 kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implement a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \le t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See 图 15 for the timing diagram of the wake up pattern with wake timeout feature.

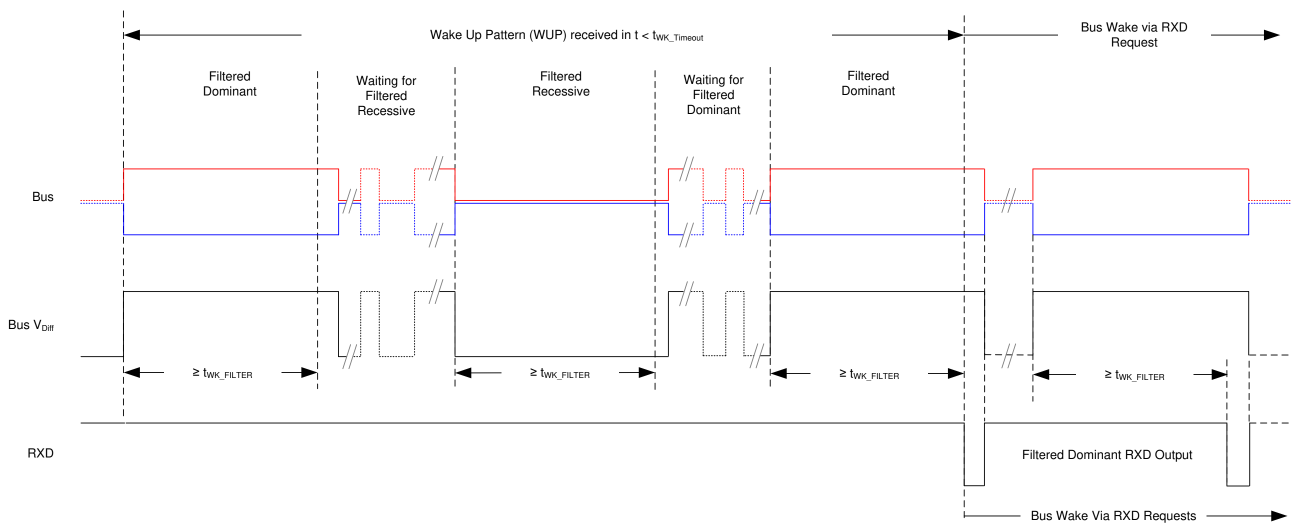


图 15. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

8.4.4 Driver and Receiver Function

The digital logic input and output levels for the TCAN1044V are CMOS levels with respect to V_{IO} for compatibility with protocol controllers having 1.8 V, 2.5 V, 3.3 V, or 5 V IO levels.

表 5. Driver Function Table

Device Mode	TXD Input[1]	Bus Outputs		Driven Bus State[2]
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	Hi-Z	Hi-Z	Biased recessive
Standby	X	Hi-Z	Hi-Z	Weak pull-down to ground

(1) X = irrelevant
(2) For bus state and bias see 图 12

表 6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9$ V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	High
Standby	$V_{ID} \geq 1.15$ V	Dominant	High Low if a remote wake event occurred See 图 15
	0.4 V < V_{ID} < 1.15 V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	High

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

The TCAN1044V transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. shows a typical application configuration for 5 V controller applications. The bus termination is shown for illustrative purposes.

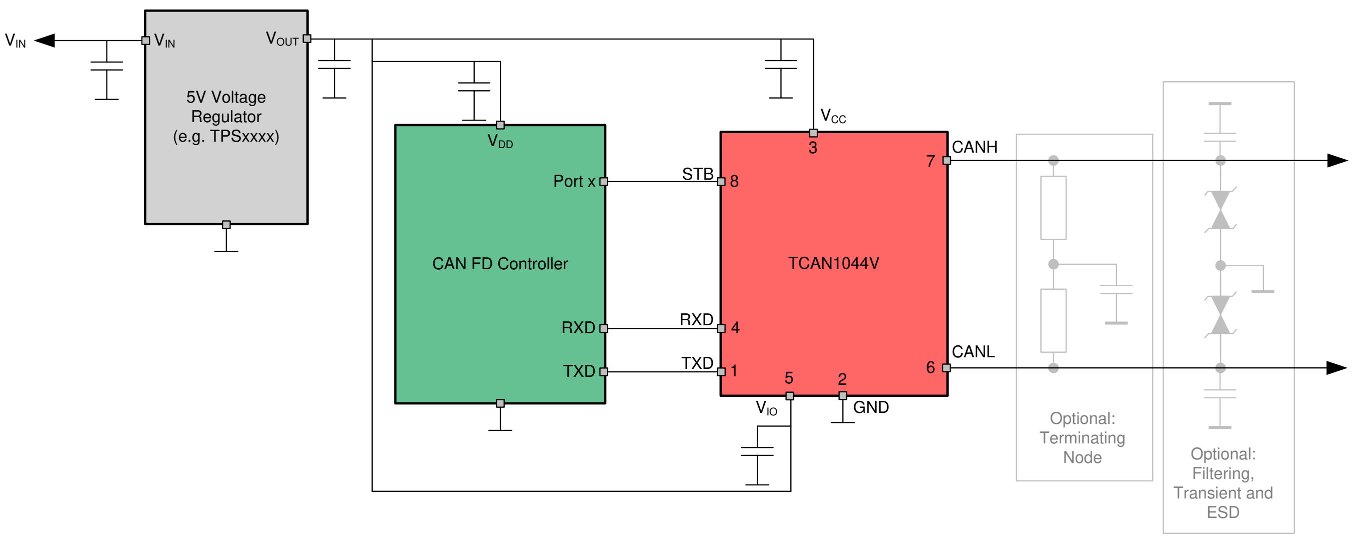


图 16. Transceiver Application Using 5 V IO Connections

9.2.1 Design Requirements

9.2.1.1 CAN Termination

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then split termination may be used, see 图 17. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

Typical Application (接下页)

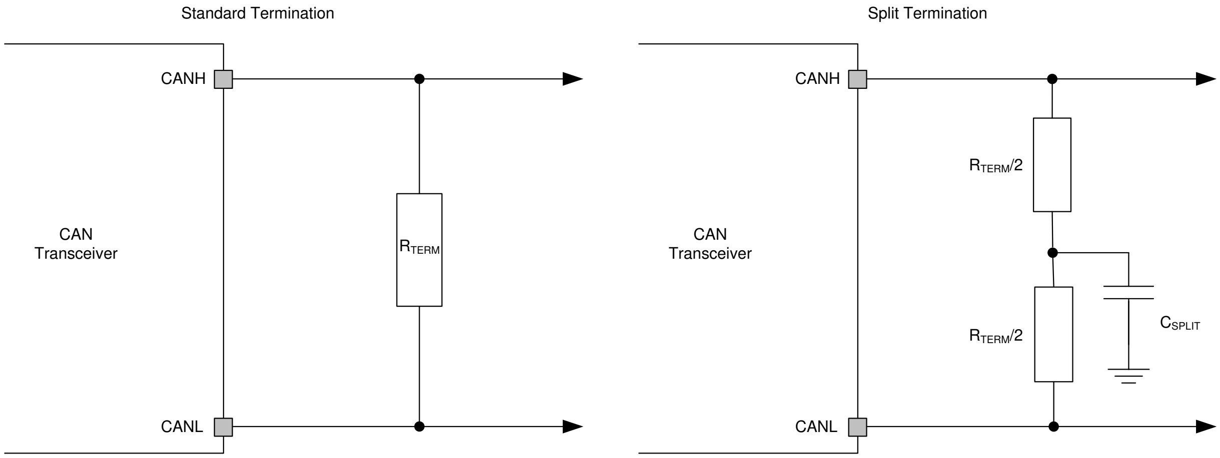


图 17. CAN Bus Termination Concepts

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1044V.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1044V is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1044V is a minimum of 40 kΩ. If 100 TCAN1044V transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1044V theoretically supports over 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

Typical Application (接下页)

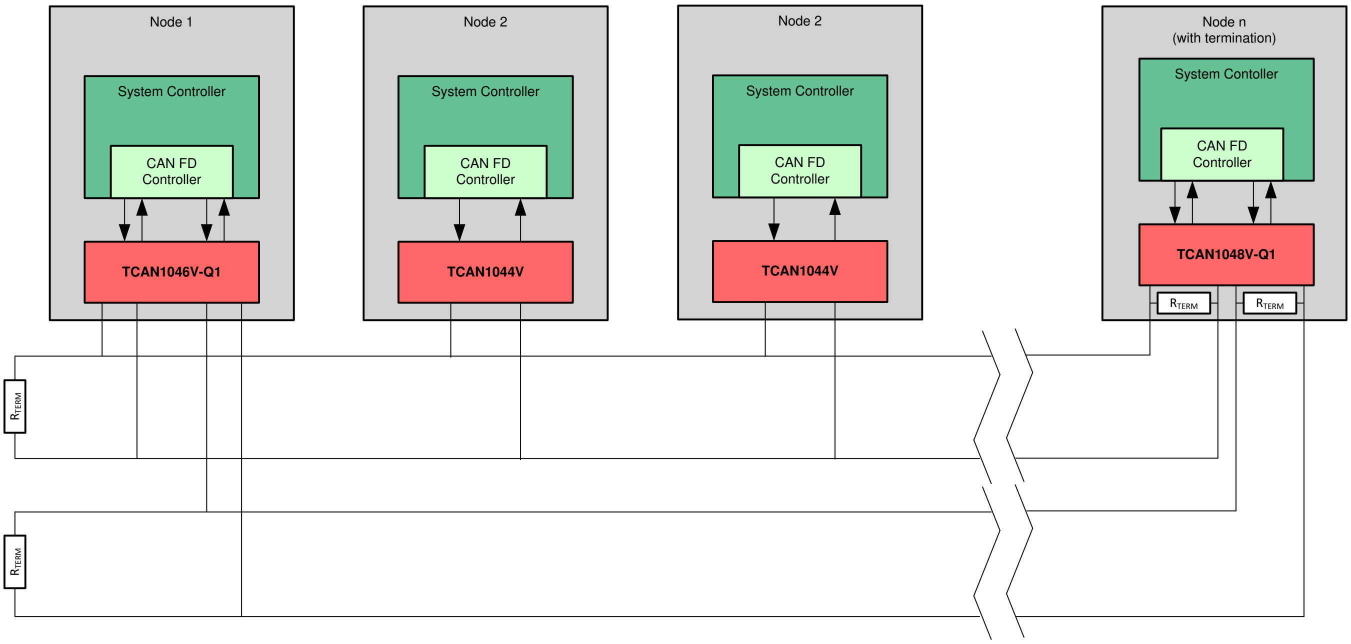
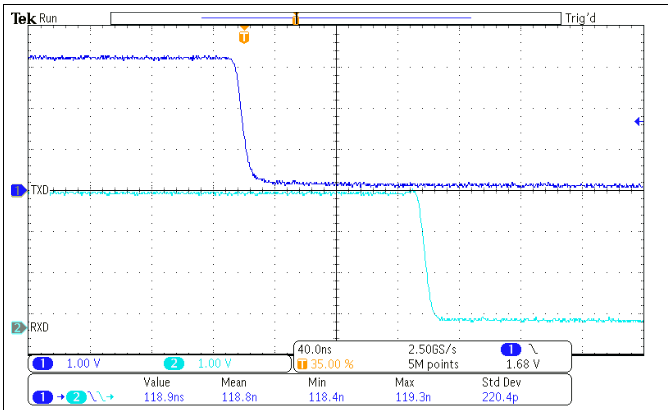


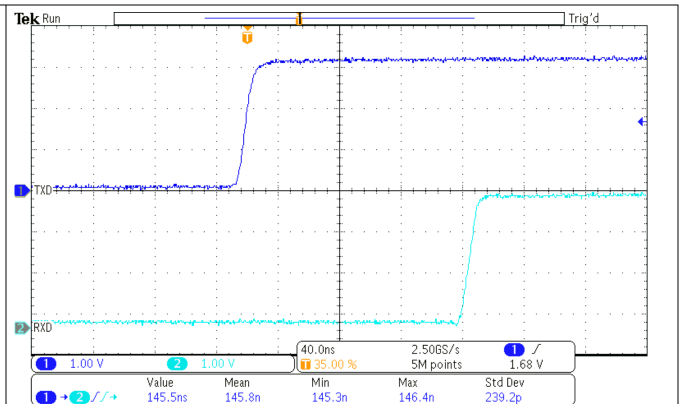
图 18. Typical CAN Bus

9.2.3 Application Curves



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

图 19. $t_{PROP(LOOP1)}$



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

图 20. $t_{PROP(LOOP2)}$

9.3 System Examples

The TCAN1044V CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8 V, 2.5 V, or 3.3 V application is shown in . The bus termination is shown for illustrative purposes.

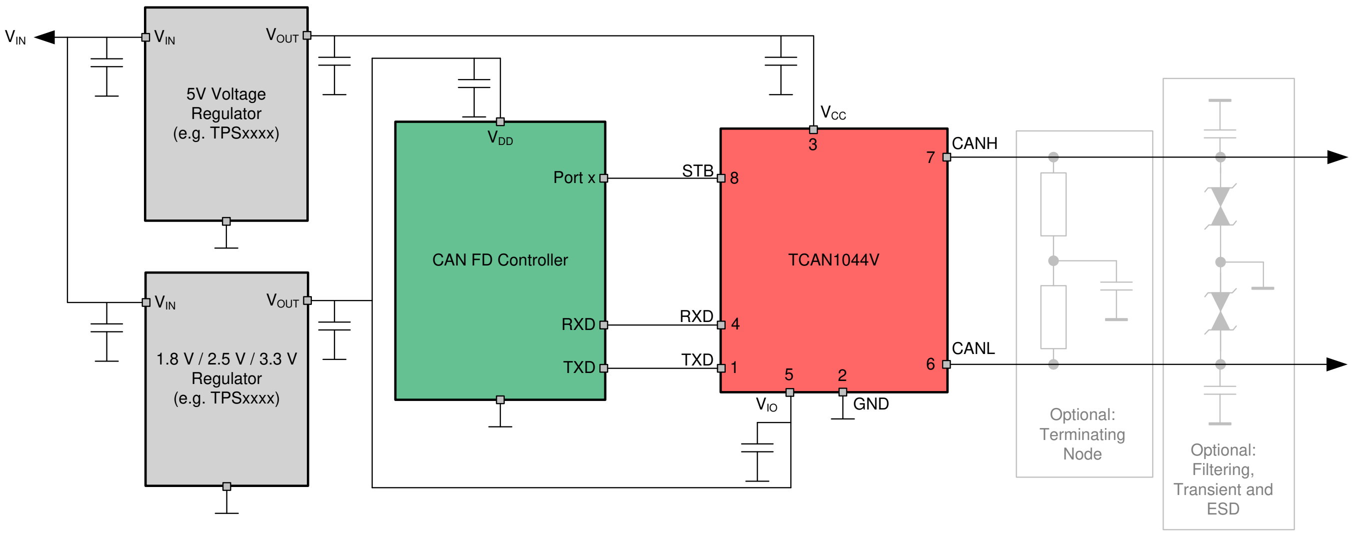


图 21. Typical Transceiver Application Using 1.8 V, 2.5 V, 3.3 V IO Connections

10 Power Supply Recommendations

The TCAN1044V transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The TCAN1044V implements an IO level shifting supply input, V_{IO}, designed for a range between 1.8 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver's main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100 nF, should be placed near the CAN transceiver's V_{IO} supply pin in addition to bypass capacitors.

11 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and industrial design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows a optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use V_{CC} and GND planes to provide low inductance. Note that high frequency current follows the path of least impedance and not the path of least resistance.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize trace and via inductance.
- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R2 and R3, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and 公式 2 for information on termination concepts and power ratings needed for the termination resistor(s).

11.2 Layout Example

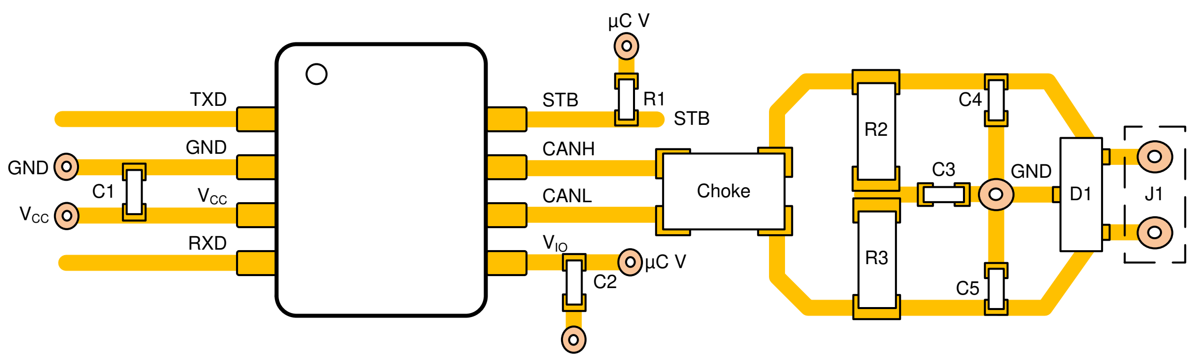


图 22. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **7.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TCAN1044V	单击此处	单击此处	单击此处	单击此处	单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 商标

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12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1044VDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27RF	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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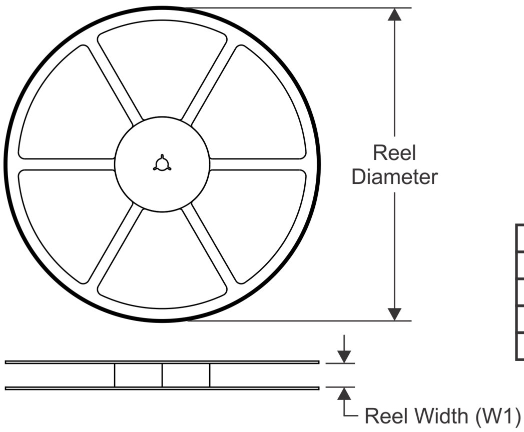
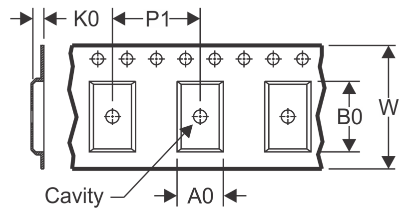
TAPE AND REEL INFORMATION

REEL DIMENSIONS

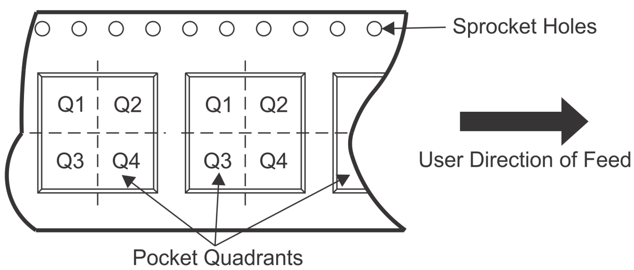


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

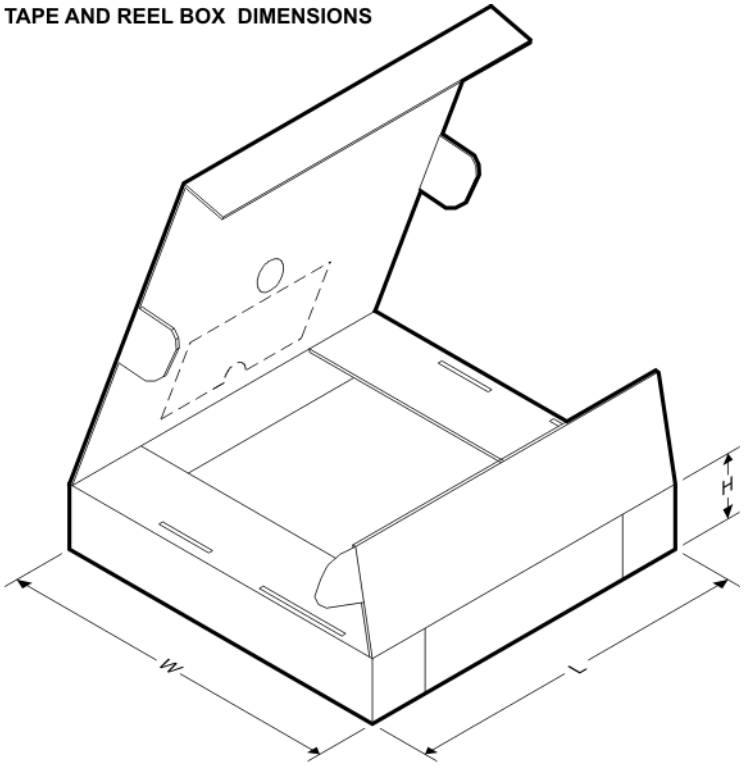
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1044VDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

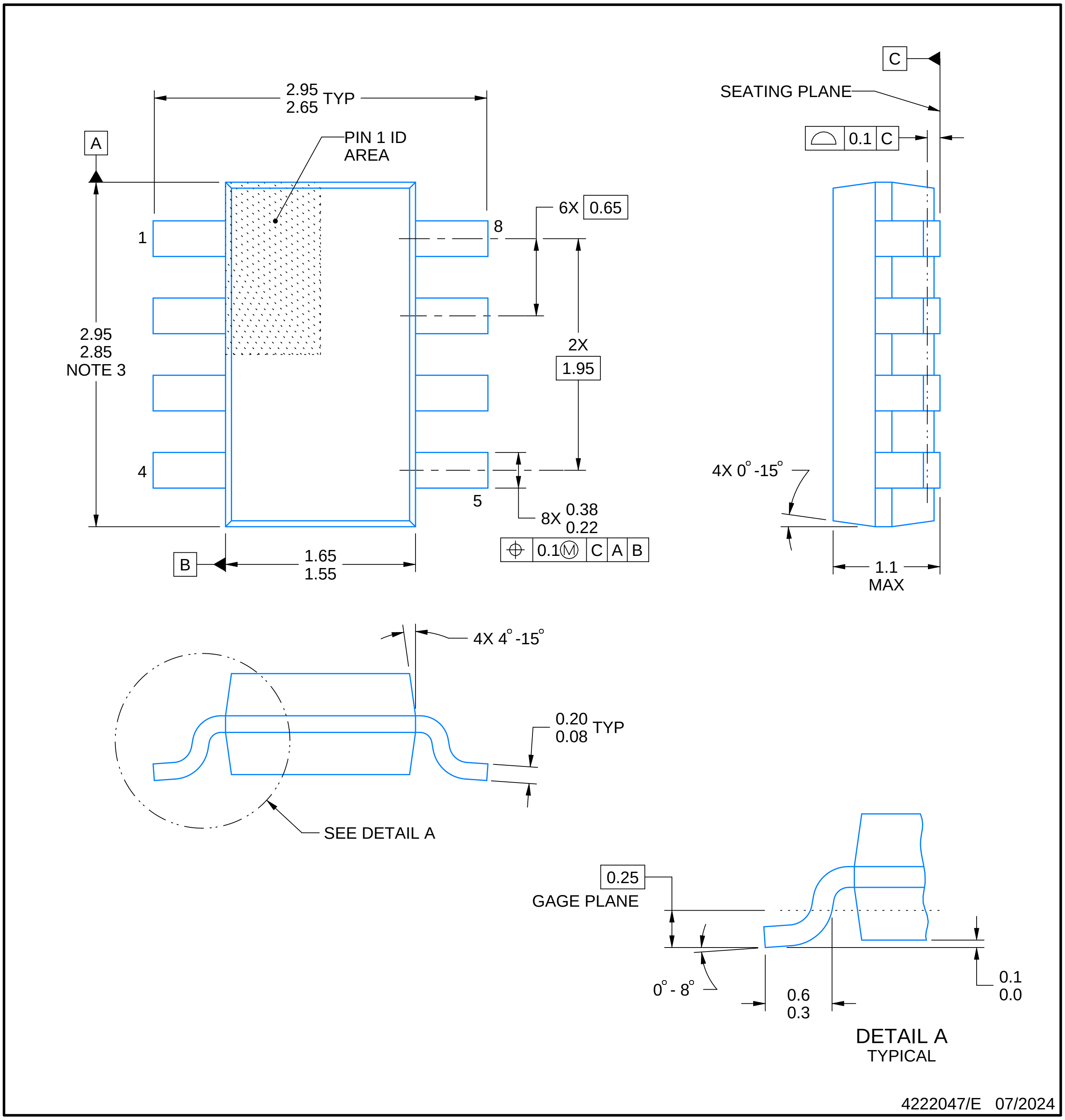
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1044VDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

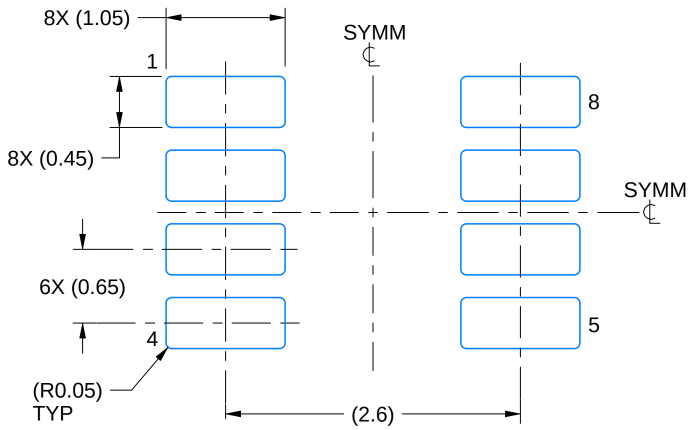
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

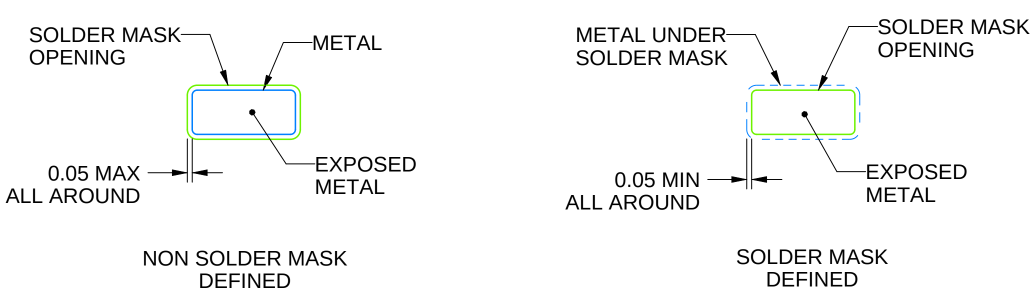


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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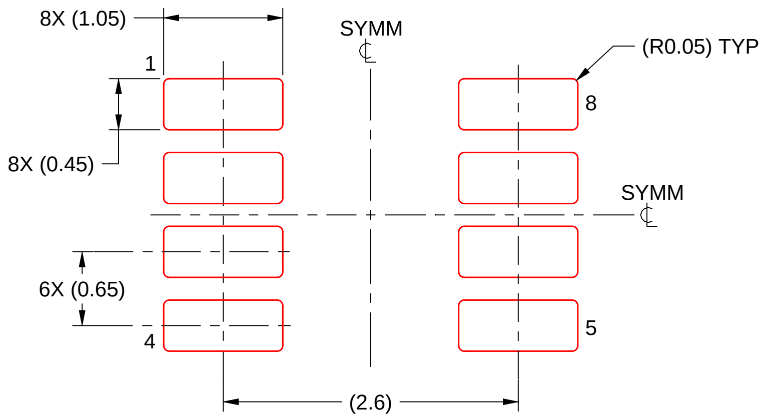
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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