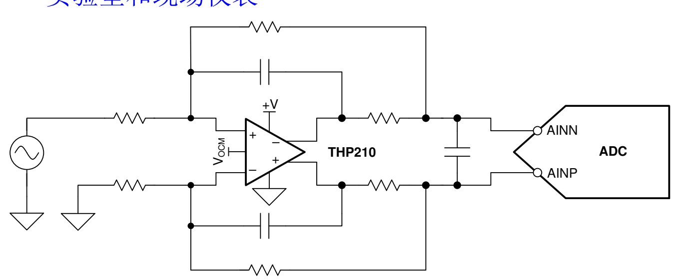
THP210 超低失调电压、高电压、低噪声、精密、全差分放大器

1 特性

- 输入失调电压：±40μV（最大值）
- 输入失调电压温漂：0.35μV/°C（最大值）
- 低电源电流：±18V 下为 950μA
- 低输入偏置电流：2nA（最大值）
- 低输入偏置电流温漂：15pA/°C（最大值）
- 增益带宽积：9.2MHz
- 差分输出压摆率：15V/μs
- 低输入电压噪声：1kHz 时为 3.7nV/√Hz
- 低 THD + N：10kHz 时为 -120dB
- 宽输入和输出共模范围
- 宽单电源工作电压范围：3V 至 36V
- 低电源电流断电特性：< 20μA
- 过载功率限制
- 电流限制
- 封装：8 引脚 VSSOP，8 引脚 SOIC
- 温度范围：–40°C 至 +125°C

2 应用

- 数据采集 (DAQ)
- 模拟输入模块
- 变电站自动化
- 半导体测试
- 实验室和现场仪表



精密、低噪声、低功耗、全差分放大器增益模块和接口

3 说明

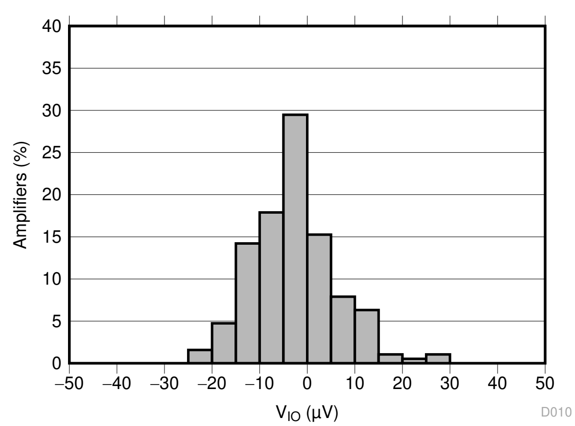
THP210 是一款超低失调电压、低噪声、高电压、精密、全差分放大器，可轻松过滤和驱动全差分信号链。THP210 还可用于将单端源转换为高分辨率模数转换器 (ADC) 所需的差分输出。双极性超级 ß 输入专为实现出色的失调电压、低噪声和 THD 而设计，可在极低的静态电流和输入偏置电流下产生极低的噪声系数。该器件专为要求低失调电压和功耗以及高信噪比 (SNR) 的信号调节电路而设计。

THP210 具有高压电源功能，支持高达 ±18V 的电源电压。高压差分信号链可通过该功能提高裕量和动态范围，而无需为差分信号的每个极性添加单独的放大器。极低的电压和电流噪声使得 THP210 可用于高增益配置，而对信号保真度的影响微乎其微。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
THP210	VSSOP (8)	3.00mm × 3.00mm
	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



低输入失调电压

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (October 2020) to Revision C (March 2021)	**Page**
• Changed PD pin description to clarify use of pin	3
• Changed Figure 6-1, *Input Offset Voltage Histogram*	8
• Changed Figure 6-2, *Input Offset Voltage Histogram*	8
• Changed Figure 6-19, *Output Impedance vs Frequency*	8
• Changed Y-axis unit from nV/ $\sqrt{HZ}$ to V/ $\sqrt{HZ}$ for Figure 9-5, *Calculated Noise Densities vs Gain Settings*	22
• Changed Y-axis unit from nV/ $\sqrt{HZ}$ to V/ $\sqrt{HZ}$ for Figure 9-6, *Calculated Noise Densities vs Gain Settings*	22

Changes from Revision A (May 2020) to Revision B (October 2020)	**Page**
• 更新了整个文档中的表格、图和交叉参考的编号格式。	1
• 添加了 D (SOIC-8) 封装和相关内容	1
• Changed Figure 7-1, *Differential Source to a Differential Gain of a 1-V/V Test Circuit*, for clarity	15
• Changed layout example circuit drawing for clarity	33

Changes from Revision * (February 2020) to Revision A (May 2020)	**Page**
• 将器件状态从预告信息（预发布）更改为量产数据（正在供货）	1

5 Pin Configuration and Functions

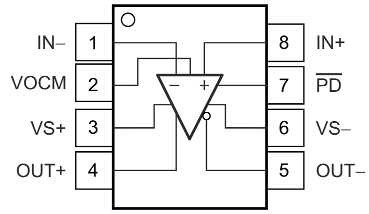


图 5-1. D (SOIC-8) and DGK (VSSOP-8) Packages, Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN –	1	I	Inverting (negative) amplifier input
IN+	8	I	Noninverting (positive) amplifier input
OUT –	5	O	Inverting (negative) amplifier output
OUT+	4	O	Noninverting (positive) amplifier output
$\overline{PD}$	7	I	Power down. $\overline{PD}$ = logic low = power off mode. $\overline{PD}$ = logic high = normal operation. The logic threshold is referenced to VS+. If power down is not needed, pull up $\overline{PD}$.
VOCM	2	I	Output common-mode voltage control input
VS –	6	I	Negative power-supply input
VS+	3	I	Positive power-supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply		40	V
		Dual supply		±20	V
	IN+, IN–, differential voltage[2]			±0.5	V
	IN+, IN–, VOCM, $\overline{PD}$, OUT+, OUT– voltage[3]		V_{VS-} – 0.5	V_{VS+} + 0.5	V
	IN+, IN– current		–10	10	mA
	OUT+, OUT– current		–50	50	mA
	Output short-circuit[4]			Continuous	
T_A	Operating temperature		–40	150	°C
T_J	Junction temperature		–40	175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins IN+ and IN– are connected with anti-parallel diodes in between the two terminals. Differential input signals that are greater than 0.5 V or less than –0.5 V must be current-limited to 10 mA or less.
(3) Input terminals are diode-clamped to the supply rails (VS+, VS–). Input signals that swing more than 0.5 V greater or less the supply rails must be current-limited to 10 mA or less.
(4) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	3		36	V
		Dual-supply	±1.5		±18	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		THP210 D (SOIC) 8 PINS	THP210 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.1	181.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.4	68.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.5	102.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.7	10.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.8	101.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S (dual supply) = ±1.5 V to ±18 V, V_{VOCM} = V_{ICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ[(1)], gain = –1 V/V, $\overline{VPD}$ = V_{VS+}, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input-referred offset voltage			10	±40	µV
		T_A = –40°C to +125°C			±75	
	Input offset voltage drift	T_A = –40°C to +125°C		0.1	±0.35	µV/°C
PSRR	Power-supply rejection ratio			±0.025	±0.25	µV/V
		T_A = –40°C to +125°C			±0.5	
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±2	nA
		T_A = –40°C to +125°C			±4	
	Input bias current drift	T_A = –40°C to +125°C		±2	±15	pA/°C
I_{OS}	Input offset current			±0.2	±1	nA
		T_A = –40°C to +125°C			±3	
	Input offset current drift	T_A = –40°C to +125°C		1	±10	pA/°C
NOISE						
e_n	Input differential voltage noise	f = 1 kHz		3.7		nV/√Hz
		f = 10 Hz		4		
		f = 0.1 to 10 Hz		0.1		$µV_{PP}$
e_i	Input current noise, each input	f = 1 kHz		300		fA/√Hz
		f = 10 Hz		400		
		f = 0.1 to 10 Hz		13.4		pA_{PP}
INPUT VOLTAGE						
	Common-mode voltage range	T_A = –40°C to +125°C	V_{VS-} + 1		V_{VS+} – 1	V
CMRR	Common-mode rejection ratio	V_{VS-} + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V		140		dB
		V_{VS-} + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V, V_S = ±18 V	126	140		
		V_{VS-} + 1 V ≤ V_{ICM} ≤ V_{VS+} – 1 V, V_S = ±18 V, T_A = –40°C to +125°C	120			
INPUT IMPEDANCE						
	Input impedance differential mode	V_{ICM} = 0 V		1 || 1		GΩ || pF

6.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S (dual supply) = ±1.5 V to ±18 V, V_{VOCM} = V_{ICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ [(1)], gain = –1 V/V, $V\overline{PD}$ = V_{VS+}, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = ±2.5 V, V_{VS-} + 0.2 V < V_O < V_{VS+} – 0.2 V	115	120		dB
		V_S = ±2.5 V, V_{VS-} + 0.3 V < V_O < V_{VS+} – 0.3 V, T_A = –40°C to +125°C	110	120		
		V_S = ±15 V, V_{VS-} + 0.6 V < V_O < V_{VS+} – 0.6 V	115	120		
		V_S = ±15 V, V_{VS-} + 0.6 V < V_O < V_{VS+} – 0.6 V, T_A = –40°C to +125°C	110	120		
FREQUENCY RESPONSE						
SSBW	Small-signal bandwidth	V_O = 100 mV_{PP}		7		MHz
GBP	Gain-bandwidth product	V_O = 100 mV_{PP}, gain = –10 V/V		9.2		MHz
FBP	Full-power bandwidth	V_O = 1 V_{PP}		2.4		MHz
SR	Slew rate	10-V step		15		V/µs
	Settling time	To 0.1% of final value, V_O = 10-V step		1		µs
		To 0.01% of final value, V_O= 10-V step		1.2		
THD+N	Total harmonic distortion and noise	Differential input, f = 1 kHz, V_O = 10 V_{PP}		–120		dB
THD+N	Total harmonic distortion and noise	Single-ended input, f = 1 kHz, V_O = 10 V_{PP}		–115		
THD+N	Total harmonic distortion and noise	Differential input, f = 10 kHz, V_O = 10 V_{PP}		–112		
	Total harmonic distortion and noise	Single-ended input, f = 10 kHz, V_O = 10 V_{PP}		–107		
HD2	Second-order harmonic distortion	Differential input, f = 1 kHz, V_O = 10 V_{PP}		–120		
		Single-ended input, f = 1 kHz, V_O = 10 V_{PP}		–126		
HD3	Third-order harmonic distortion	Differential input, f = 1 kHz, V_O = 10 V_{PP}		–120		
		Single-ended input, f = 1 kHz, V_O = 10 V_{PP}		–119		
	Overdrive recovery time	gain = –5 V/V, 2x output overdrive, dc-coupled		3.3		µs
Z_O	Open-loop output impedance	f = 100 kHz (differential)		14		Ω
C_{LOAD}	Capacitive load drive	Differential capacitive load, no output isolation resistors, phase margin = 30°		50		pF
OUTPUT						
V_{OL}	Negative output voltage swing from rail	V_S = ±2.5 V		100		mV
		V_S = ±2.5 V, T_A = –40°C to +125°C		100		
		V_S = ±18 V		230		
		V_S = ±18 V, T_A = –40°C to +125°C		270		
V_{OH}	Positive output voltage swing from rail	V_S = ±2.5 V		100		
		V_S = ±2.5 V, T_A = –40°C to +125°C		100		
		V_S = ±18 V		230		
		V_S = ±18 V, T_A = –40°C to +125°C		270		
I_{SC}	Short-circuit current			±31		mA

6.5 Electrical Characteristics (continued)

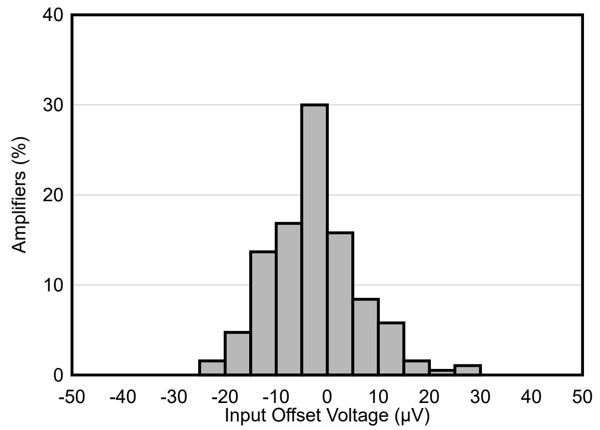
at T_A = 25°C, V_S (dual supply) = ±1.5 V to ±18 V, V_{VOCM} = V_{ICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ[1], gain = –1 V/V, $V\overline{PD}$ = V_{VS+}, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT COMMON-MODE VOLTAGE						
	Small-signal bandwidth from VOCM pin	V_{VOCM} = 100 mV_{PP}		2		MHz
	Large-signal bandwidth from VOCM pin	V_{VOCM} = 0.6 V_{PP}		5.7		
	Slew rate from VOCM pin	V_{VOCM} = 0.5-V step, rising		4.2		V/µs
		V_{VOCM} = 0.5-V step, falling		5.5		
	DC output balance	V_{VOCM} fixed midsupply (V_O = ±1 V)		78		dB
	VOCM Input voltage range	V_S = ±2.5 V	V_{VS-} + 1		V_{VS+} – 1	V
		V_S = ±18 V	V_{VS-} + 2		V_{VS+} – 2	
	VOCM input impedance			2.5 || 1		MΩ || pF
	VOCM offset from mid-supply	V_{VOCM} pin floating, V_O = V_{ICM} = 0 V		±1		mV
	VOCM common-mode offset voltage	V_{VOCM} = V_{ICM}, V_O = 0 V		±1	±6	
		V_{VOCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C			±10	
	VOCMcommon-mode offset voltage drift	V_{VOCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C		±20	±60	µV/°C
POWER SUPPLY						
I_Q	Quiescent operating current			0.95	1.05	mA
		T_A = –40°C to +125°C			1.4	
POWER DOWN						
$V_{\overline{PD}(HI)}$	Power-down enable voltage	T_A = –40°C to +125°C	V_{VS+} – 0.5			V
$V_{\overline{PD}(LOW)}$	Power-down disable voltage	T_A = –40°C to +125°C			V_{VS+} – 2.0	
	$\overline{PD}$ bias current	$V_{\overline{PD}}$ = V_{VS+} – 2 V		1	2	µA
	Powerdown quiescent current			10	20	µA
	Turn-on time delay	V_{IN} = 100 mV, Time to V_O = 90% of final value		10		µs
	Turn-off time delay	V_{IN} = 100 mV, Time to V_O = 10% of original value		15		

(1) R_L is connected differentially, from OUT+ to OUT–.

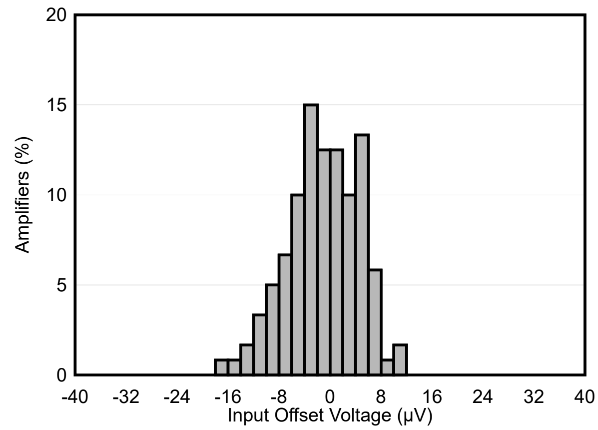
6.6 Typical Characteristics

at V_{VS} = ±15 V, T_A = 25°C, V_{VOCM} = V_{VICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, gain = –1 V/V, and $V_{\overline{PD}}$ = V_{VS+} (unless otherwise noted)



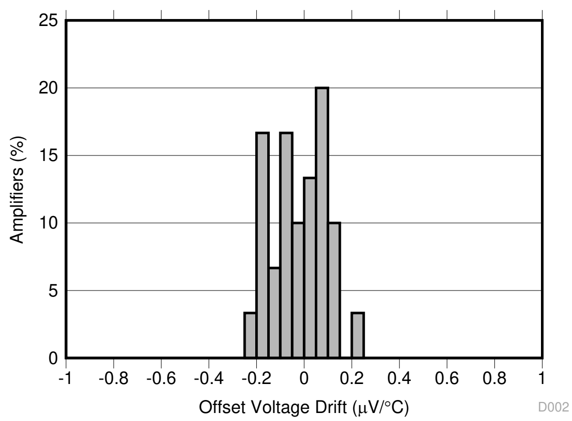
V_S = ±1.5 V, N = 190, mean = –2.66 µV, std dev = 8.81 µV

图 6-1. Input Offset Voltage Histogram



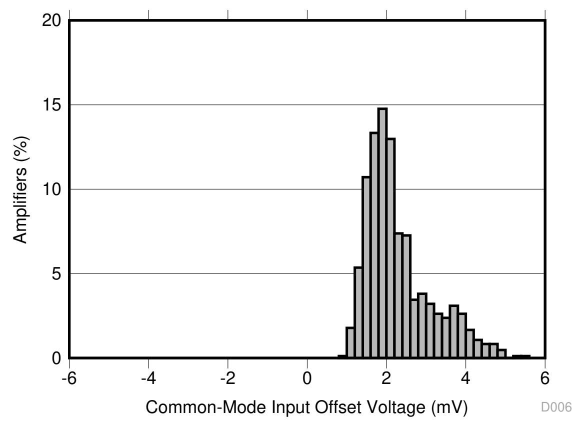
V_S = ±15 V, N = 120, mean = –1.13 µV, std dev = 5.61 µV

图 6-2. Input Offset Voltage Histogram



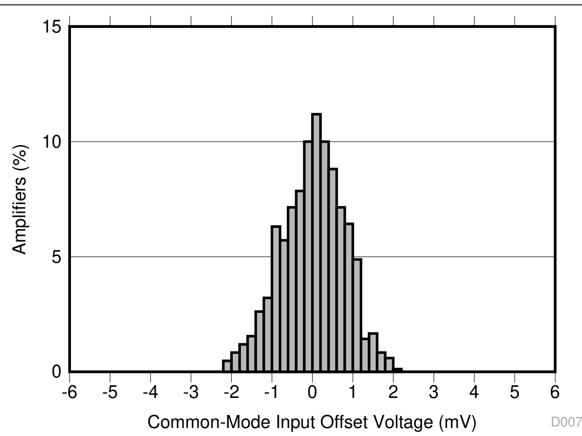
V_S = ±15 V

图 6-3. Input Offset Voltage Drift Histogram



V_S = ±18 V, VOCM = floating

图 6-4. Output Common-Mode Offset Voltage



V_S = ±18 V, VOCM = 0 V

图 6-5. Output Common Mode Voltage Offset

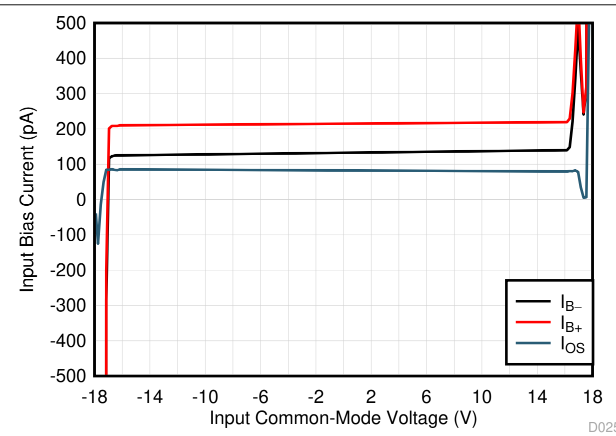


图 6-6. Input Bias Current vs Input Common-Mode Voltage

6.6 Typical Characteristics (continued)

at V_{VS} = ±15 V, T_A = 25°C, V_{VOCM} = V_{VICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, gain = –1 V/V, and $V_{\overline{PD}}$ = V_{VS+} (unless otherwise noted)

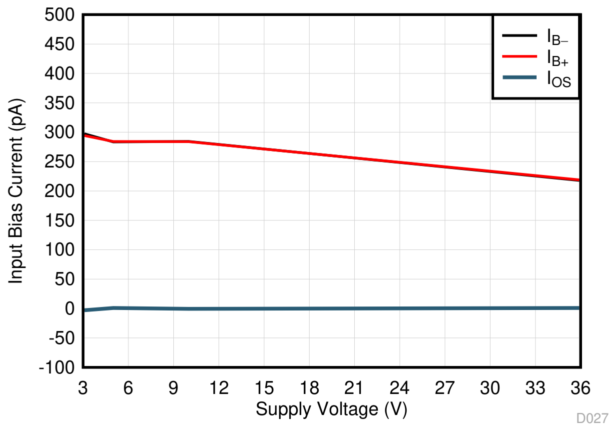


图 6-7. Input Bias Current vs Supply Voltage

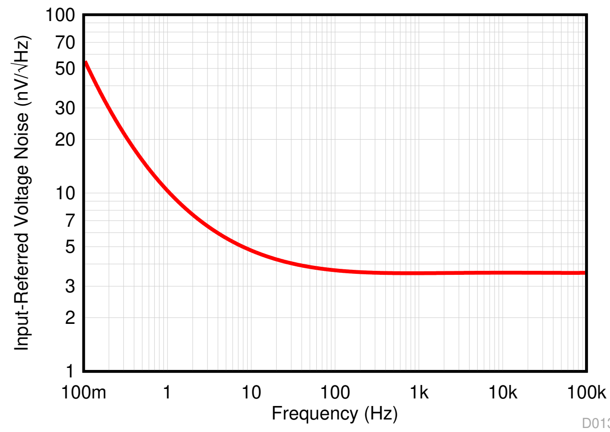


图 6-8. Input-Referred Voltage Noise vs Frequency

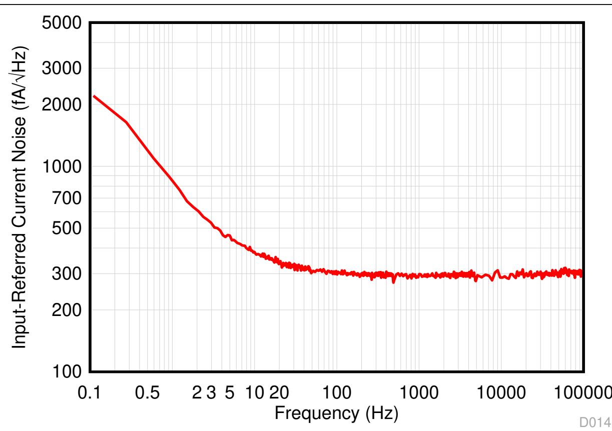
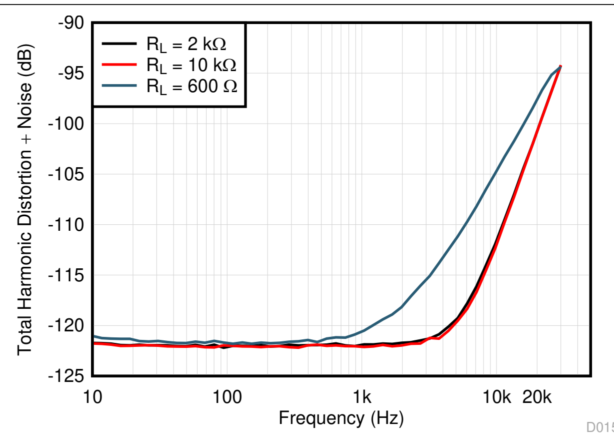
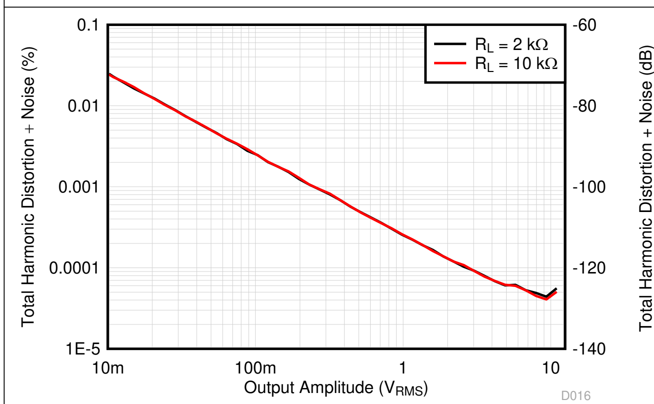


图 6-9. Current Noise vs Frequency



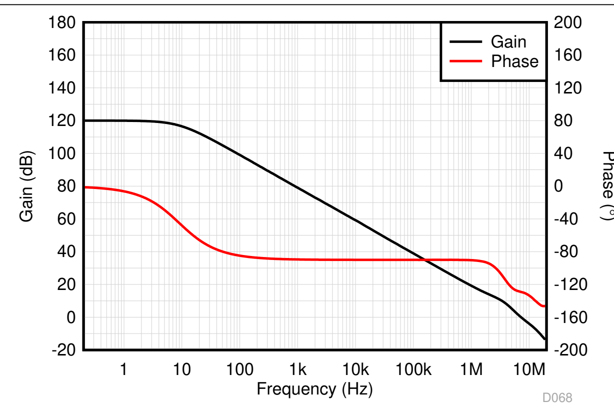
V_{OUT} = 3 V_{RMS}, V_S = ±15 V

图 6-10. Total Harmonic Distortion + Noise vs Frequency



f = 1 kHz, V_S = ±15 V

图 6-11. Total Harmonic Distortion + Noise vs Amplitude

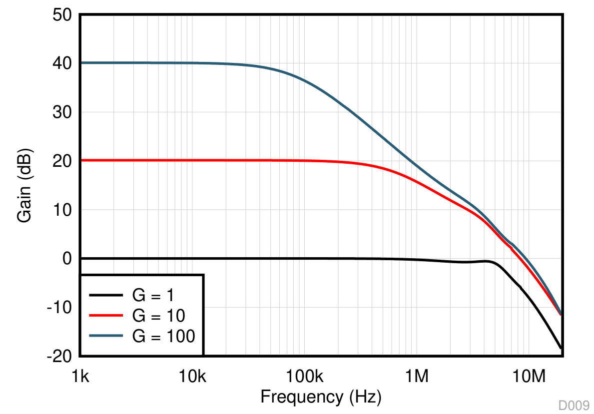


V_S = ±15 V, C_L = 50 pF

图 6-12. Open-Loop Gain vs Frequency

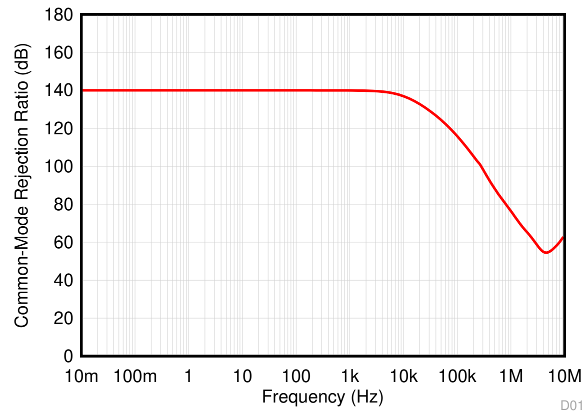
6.6 Typical Characteristics (continued)

at V_{VS} = ±15 V, T_A = 25°C, V_{VOCM} = V_{VICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, gain = –1 V/V, and $V_{\overline{PD}}$ = V_{VS+} (unless otherwise noted)



V_S = ±15 V, C_L = 50 pF

图 6-13. Closed-Loop Gain vs Frequency



V_S = ±15 V

图 6-14. Common-Mode Rejection Ratio vs Frequency

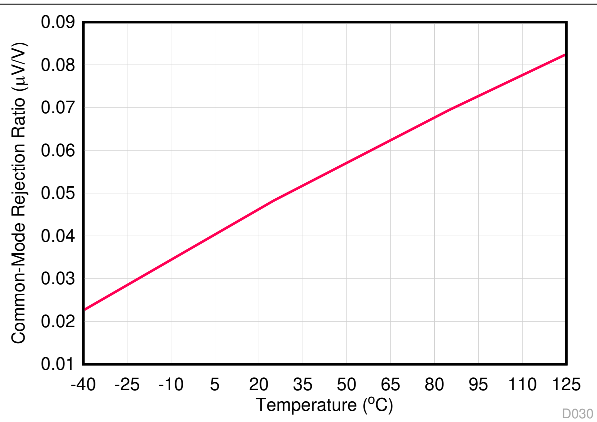
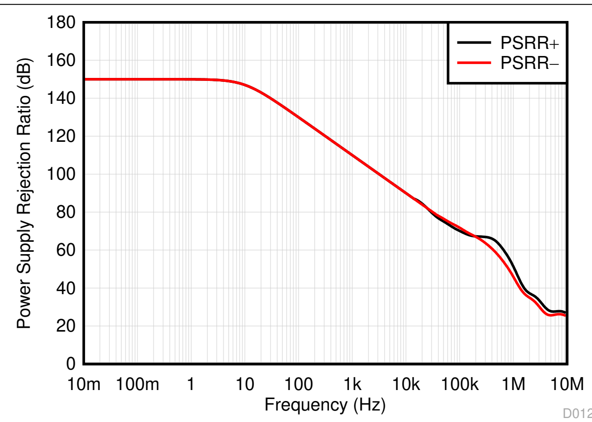


图 6-15. Common-Mode Rejection Ratio vs Temperature



V_S = ±15 V

图 6-16. Power-Supply Rejection Ratio vs Frequency

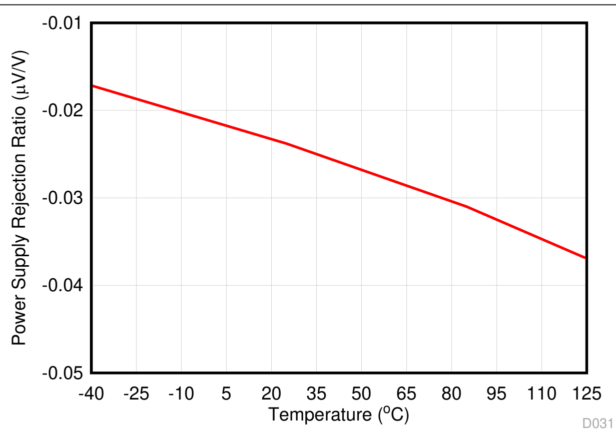
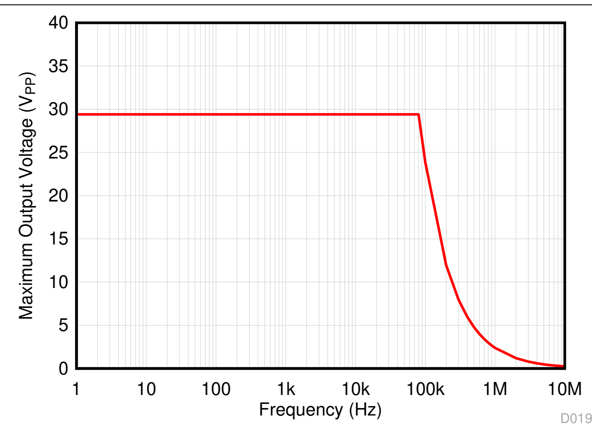


图 6-17. Power-Supply Rejection Ratio vs Temperature

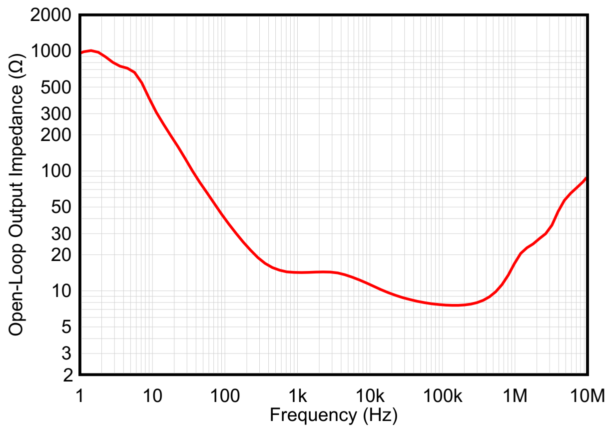


V_S = ±15 V

图 6-18. Maximum Output Voltage vs Frequency

6.6 Typical Characteristics (continued)

at V_{VS} = ±15 V, T_A = 25°C, V_{VOCM} = V_{VICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, gain = –1 V/V, and $V_{\overline{PD}}$ = V_{VS+} (unless otherwise noted)



V_S = ±15 V

图 6-19. Output Impedance vs Frequency

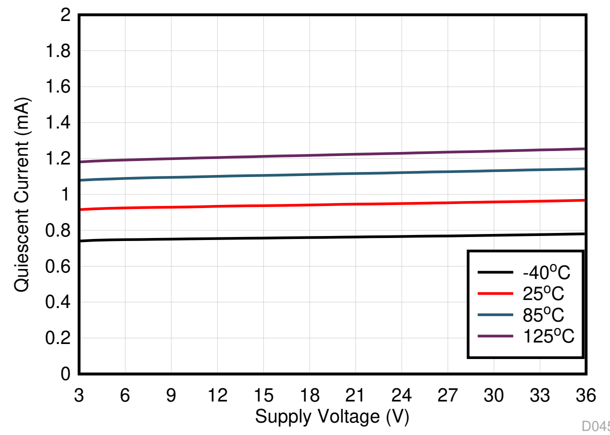


图 6-20. Quiescent Current vs Supply Voltage

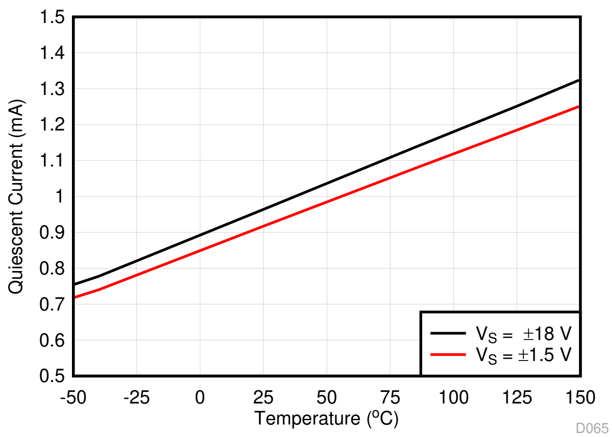


图 6-21. Quiescent Current vs Temperature

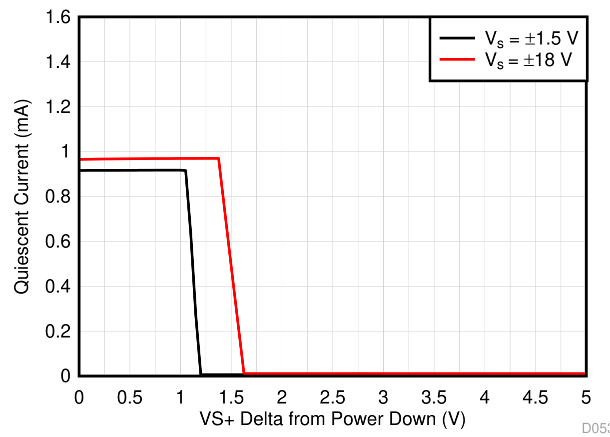


图 6-22. Quiescent Current vs Power-Down Delta From Supply Voltage

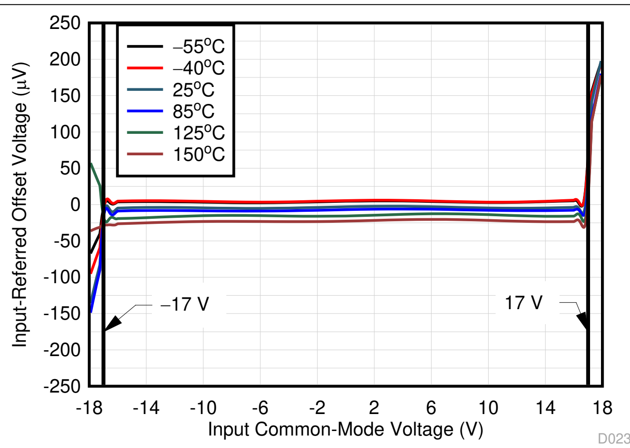


图 6-23. Input Offset Voltage vs Input Common-Mode Voltage

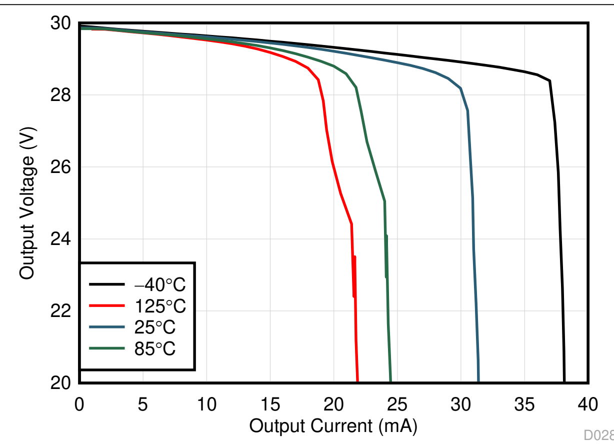
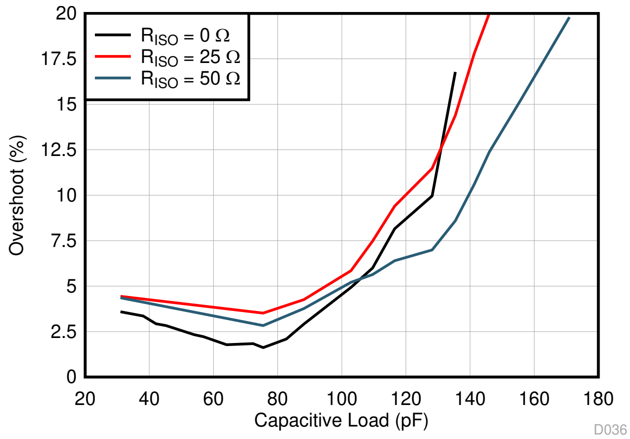


图 6-24. Output Voltage vs Output Current

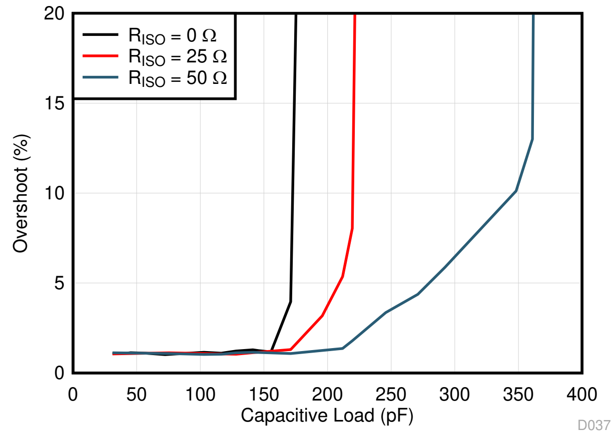
6.6 Typical Characteristics (continued)

at V_{VS} = ±15 V, T_A = 25°C, V_{VOCM} = V_{VICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, gain = – 1 V/V, and $V_{\overline{PD}}$ = V_{VS+} (unless otherwise noted)



A_V = 1

图 6-25. Small-Signal Overshoot vs Capacitive Load



A_V = 10

图 6-26. Small-Signal Overshoot vs Capacitive Load

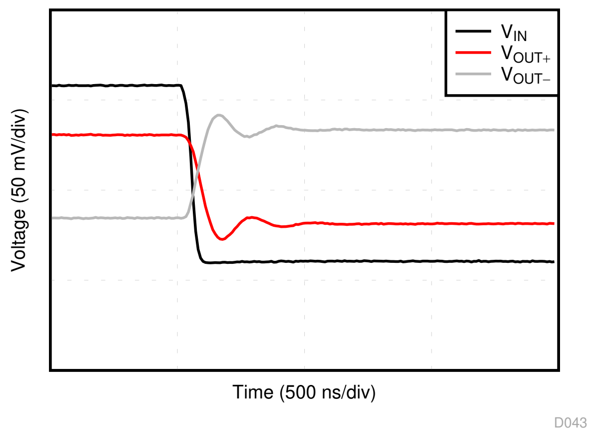


图 6-27. Small-Signal Step Response, Falling

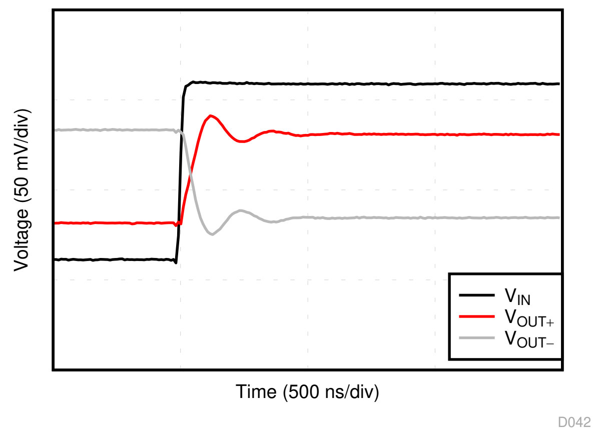


图 6-28. Small-Signal Step Response, Rising

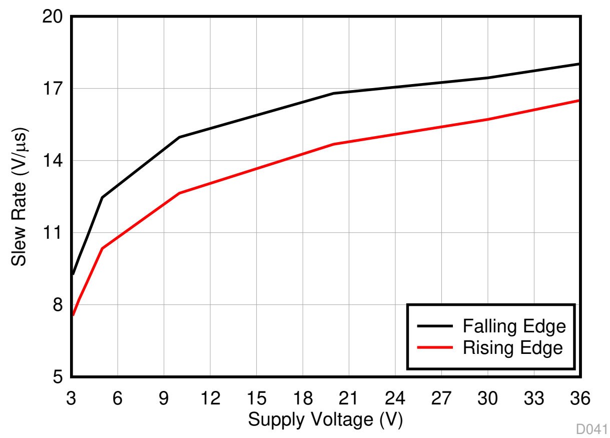


图 6-29. Output Slew Rate vs Supply Voltage

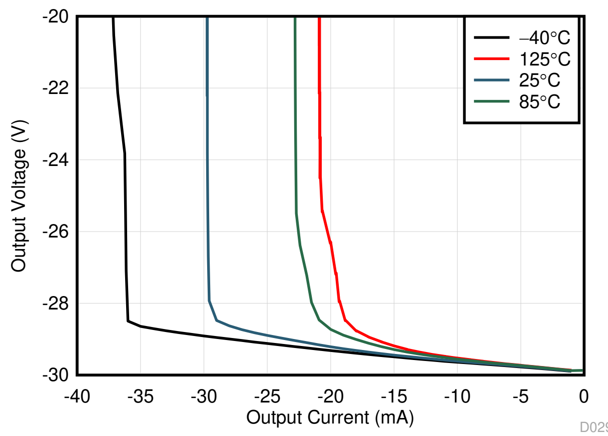


图 6-30. Output Voltage vs Output Current

6.6 Typical Characteristics (continued)

at V_{VS} = ±15 V, T_A = 25°C, V_{VOCM} = V_{VICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, gain = –1 V/V, and $V_{\overline{PD}}$ = V_{VS+} (unless otherwise noted)

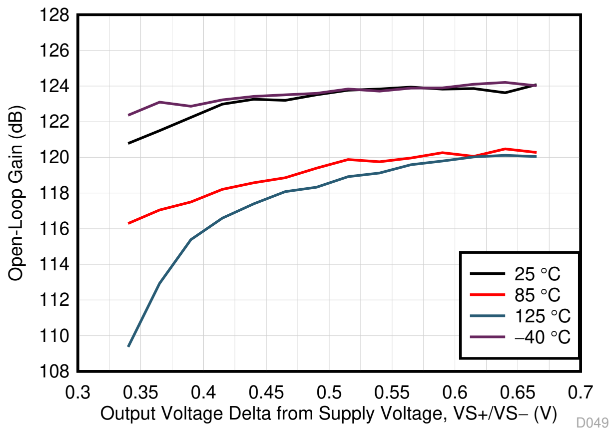


图 6-31. Open-Loop Gain vs Ouput Delta From Supply

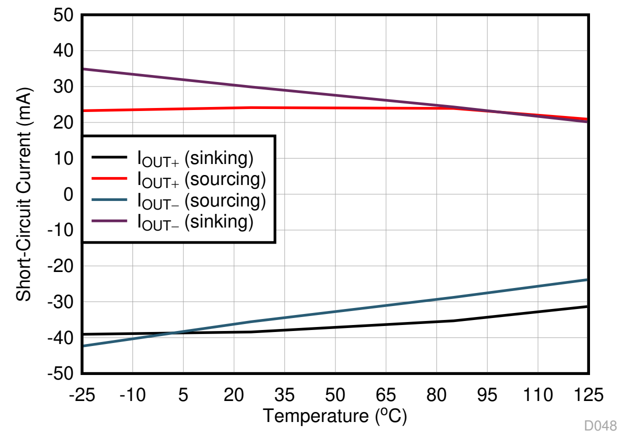


图 6-32. Short-Circuit Current vs Temperature

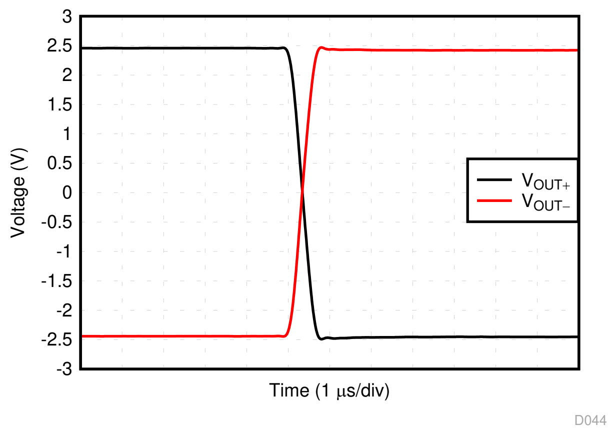


图 6-33. Large-Signal Step Response

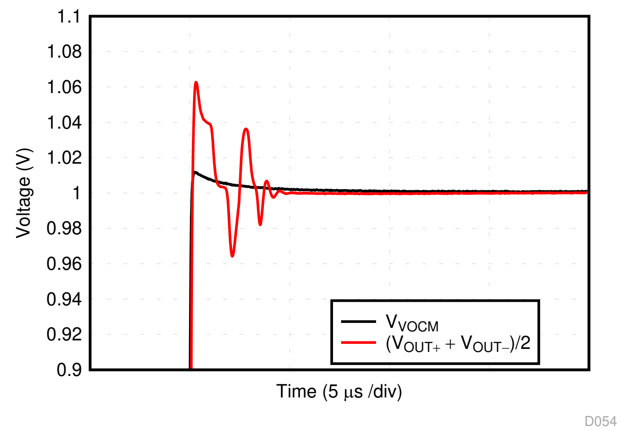


图 6-34. Output Common-Mode Step Response, Rising

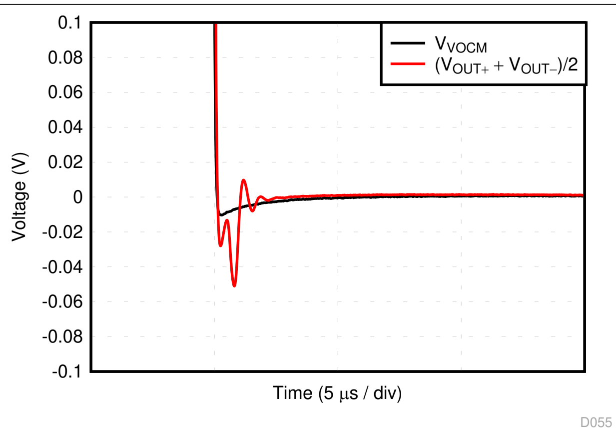


图 6-35. Output Common-Mode Step Response, Falling

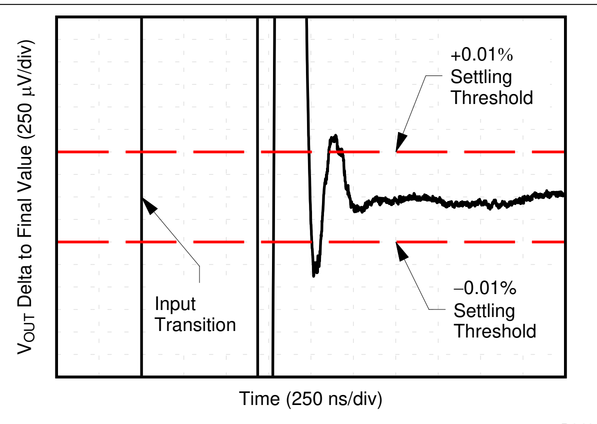


图 6-36. Output Settling Time to ±0.01%

6.6 Typical Characteristics (continued)

at V_{VS} = ±15 V, T_A = 25°C, V_{VOCM} = V_{VICM} = 0 V, R_F = 2 kΩ, R_L = 10 kΩ, gain = –1 V/V, and $V_{\overline{PD}}$ = V_{VS+} (unless otherwise noted)

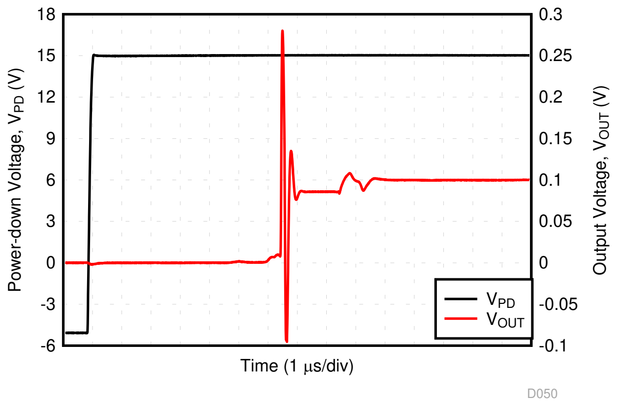


图 6-37. Power-Down Time ($\overline{PD}$ Low to High)

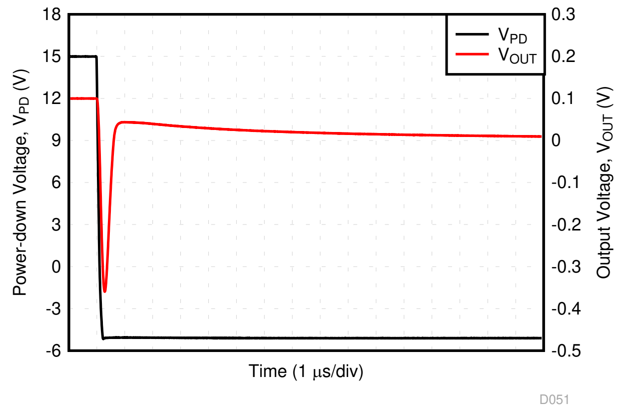


图 6-38. Power-Down Time ($\overline{PD}$ High to Low)

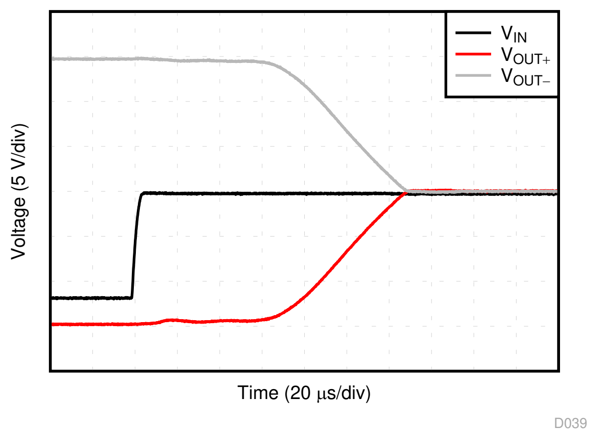


图 6-39. Output Negative Overload Recovery

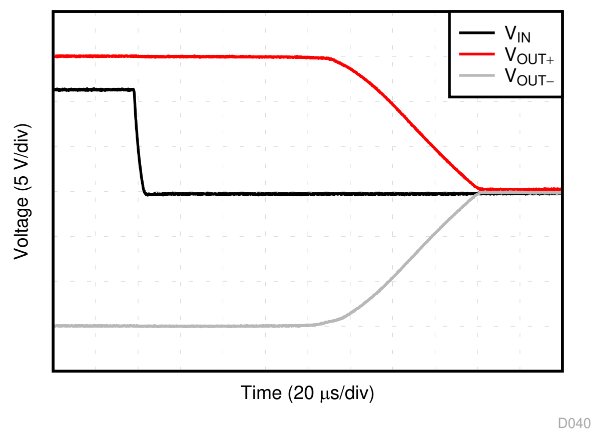


图 6-40. Output Positive Overload Recovery

7 Parameter Measurement Information

7.1 Characterization Configuration

The THP210 is a fully differential amplifier (FDA) configuration that offers high dc precision, very low noise and harmonic distortion in a single, low-power amplifier. The FDA is a flexible device where the main aim is to provide a purely differential output signal centered on a user-configurable, common-mode voltage that is usually matched to the input common-mode voltage required by an analog-to-digital converter (ADC). The circuit used for characterization of the differential-to-differential performance is seen in 图 7-1

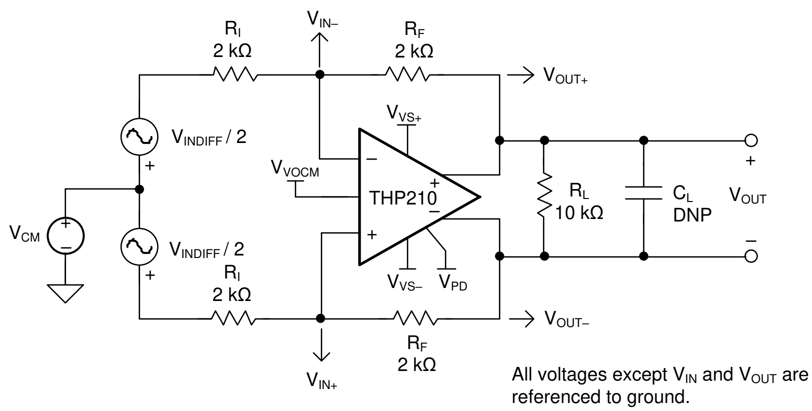


图 7-1. Differential Source to a Differential Gain of a 1-V/V Test Circuit

A similar circuit is used for single-ended to differential measurements, as shown in 图 7-2.

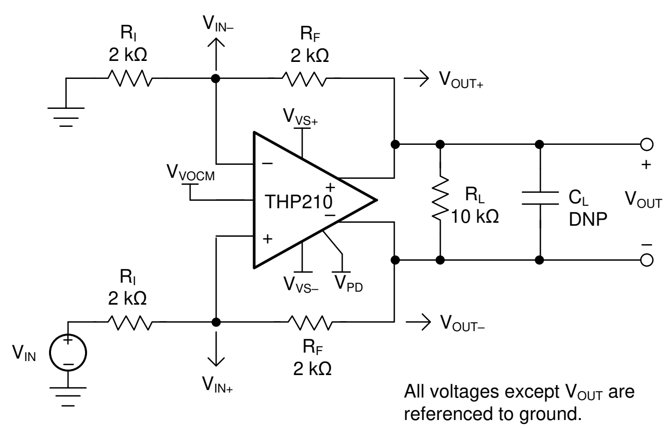


图 7-2. Single-ended Source to Differential Gain of 1-V/V Test Circuit

The characterization plots fix the R_F (R_{F1} = R_{F2}) value at 2 kΩ, unless otherwise noted. This value can be adjusted to match the system design parameters with the following considerations in mind:

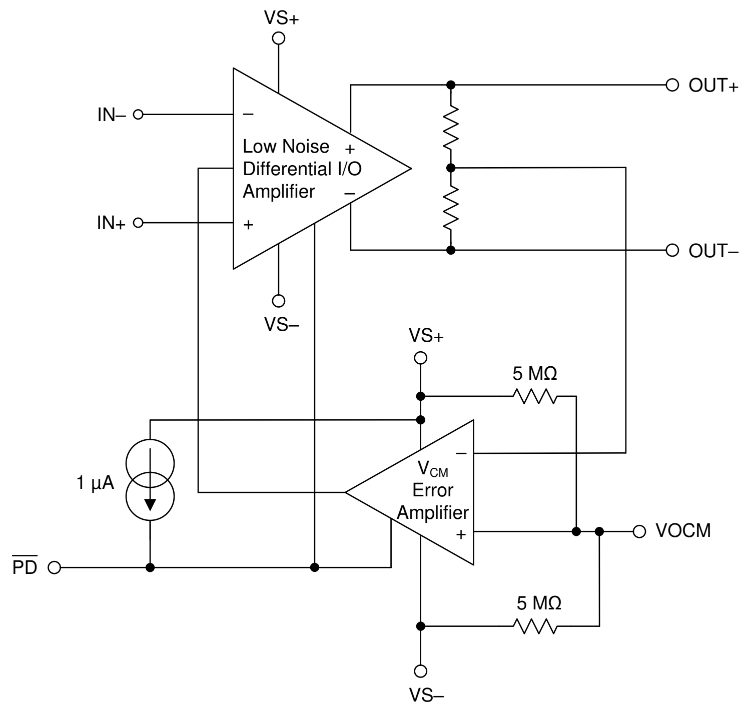
- The current required to drive RF from the peak output voltage to the input common-mode voltage add to the overall output load current. If the total current (current through R_F + current through R_L) exceeds the current limit conditions, the device enters a current limit, causing the output voltage to collapse.
- High feedback resistor values (R_F > 100 kΩ) interact with the amplifier input capacitance to create a zero in the feedback network. Compensation must be added to account for potential source of instability; see the TI Precision Labs FDA Stability Training for guidance on designing an appropriate compensation network.

8 Detailed Description

8.1 Overview

The THP210 is a low-noise, low-distortion fully-differential amplifier (FDA) that features Texas Instrument's super-beta bipolar input devices. Super-beta input devices feature very low input bias current as compared to standard bipolar technology. The low input bias current and current noise makes the THP210 an excellent choice for high-performance applications that require low-noise, differential-signal processing without significant current consumption. This device is also designed for analog-to-digital input circuits that require low offset and low noise in a single fully-differential amplifier. The THP210 features high-voltage capability, which allows the device to be used in ±15-V supply circuits without any additional voltage clamping or regulators. Because this device is unity-gain stable, the device allows high-voltage input signals to be attenuated to the low-voltage ADC domain without requiring additional compensation techniques.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Super-Beta Input Bipolar Transistors

The THP210 is designed on a modern bipolar process that features TI's super-beta input transistors. Traditional bipolar transistors feature excellent voltage noise and offset drift, but suffer a tradeoff in high input bias current (I_B) and high input bias current noise. Super-beta transistors offer the benefits of low voltage noise and low offset drift with an order of magnitude reduction in input bias current and reduction in input bias current noise. For many filter circuits, input bias current noise can dominate in circuits where higher resistance input resistors are used. The THP210 enables a fully-differential, low-noise amplifier design without restrictions of low input resistance at a power level unmatched by traditional single-ended amplifiers.

8.3.2 Power Down

The THP210 features a power-down circuit to disable the amplifier when a low-power mode is required by the system. In the power-down state, the amplifier outputs are in a high-impedance state, and the amplifier total quiescent current is reduced to less than 20 µA.

8.3.3 Flexible Gain Setting

The THP210 offers considerable flexibility in the configuration and selection of resistor values. Low input bias current and bias current noise allows for larger gain resistor values with minimal impact to noise or offset, see 节 9.1.3 for more details.

The design starts with the selection of the feedback resistor value. The 2-kΩ feedback resistor value used for the characterization curves is a good compromise among power, noise, and phase margin considerations. With the feedback resistor values selected (and set equal on each side), the input resistors are set to obtain the desired gain, with input impedance also set with these input resistors. Differential I/O designs provide an input impedance that is the sum of the two input resistors. Single-ended input to differential output designs present a more complicated input impedance. Most characteristic curves implement the single-ended to differential design as the more challenging requirement over differential-to-differential I/O designs.

8.3.4 Amplifier Overload Power Limit

During overload or fault conditions, many bipolar-based amplifiers draw significant (three to five times) quiescent current if the output voltage is clipped (meaning the output voltage becomes limited by the negative or positive supply rail).

The primary cause for this condition is that common-emitter output stages can consume excessive base current (up to 100x) when overdriven into saturation. In addition, the overload condition causes the feedback to be broken, which causes the slew boost to be permanently on. Depending on the slew boost circuit, this increases the tail current up to 4x.

The THP210 has an intelligent overload detection scheme that eliminates this problem, meaning that there is virtually no additional current consumption in the case of an overload event, represented in 图 8-1. The protection circuit continuously monitors both the input and output stages of the amplifier. 图 8-1 shows a measurements of the overload power limit behavior. If a large input voltage step (referred to as ΔV_{IN}) is detected, the protection circuit checks for the presence of a rapid change in the voltage at the output (referred to as ΔV_O). If the output is not changing because the output is clipped at supply rail, the protection circuit disables the slew-boost circuit and limit the base current of the predriver to prevent output saturation. After the overload condition is removed, the amplifier rapidly recovers to normal operating condition. 图 8-1 indicates that in case of an overloaded output the current consumption at the supply pins (referred to $I_{(VS+)}$ and $I_{(VS-)}$) does not exceed the limitations, and quickly recovers as soon as the overload condition has been removed.

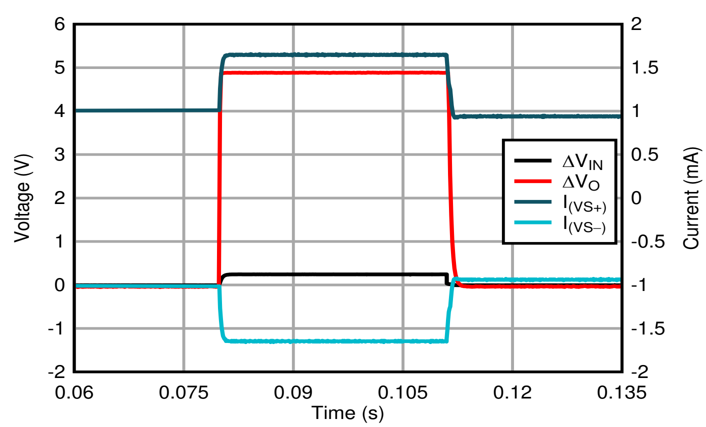


图 8-1. Supply Current Change With Overloaded Outputs

8.3.5 Unity Gain Stability

The stability of the amplifiers is of key importance when designing application circuits with fully differential amplifiers. This stability becomes especially important when driving capacitive loads, such as the input for successive-approximation-register (SAR) analog-to-digital converters (ADCs). A trade-off is made between the bandwidth of an amplifier and keeping power consumption low; in many cases, FDAs are not unity gain stable. Currently, many FDAs are primarily designed to support high-speed ADCs, and thus, are typically decompensated. This decompensation comes with the drawback that the noise performance degrades because of noise gain peaking. Additional components and compensation techniques are required to handle these challenges and prevent potential instability of the FDA. For detailed analysis of how stability is defined and affected, see TI Precision Labs – Fully Differential Amplifiers – FDA Stability and Simulating Phase Margin.

The THP210 is unity-gain stable; therefore, this device can be used in gain configurations with gains > 1, and also in attenuating configurations with gains < 1, without requiring compensation techniques and sacrificing dynamic performance. This device can be of prime use for applications that need to interface large input signals to the low-voltage ADC domain.

8.4 Device Functional Modes

The THP210 has two functional modes: normal operation and power-down. The power-down state is enabled when the voltage on the power-down pin is lowered to less than the power-down threshold. In the power-down state, the quiescent current is significantly reduced, and the output voltage is high-impedance. This high impedance can lead to the input voltages (VIN+ and VIN–) separating.

Internal ESD protection diodes remain present across the input pins in both operating and power-down mode. Large input signals during disable can forward-biasing the ESD protection diodes, thus producing a load current in the supply, even in power-down. See 节 *9.1.5* for guidance on power-down operation.

The VOCM control pin sets the output average voltage. If left open, VOCM defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal V_{CM} error amplifier. If floated to obtain a default midsupply reference for VOCM, an external decoupling capacitor must be added on the VOCM pin to reduce the otherwise high output noise for the internal high-impedance bias.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

Most applications for the THP210 strive to deliver the best dynamic range in a design that delivers the desired signal processing along with adequate phase margin for the amplifier. The following sections detail some of the design issues with analysis, and guidelines for improved performance.

9.1.1 I/O Headroom Considerations

The starting point for most designs is to assign an output common-mode voltage for the THP210. For ac-coupled signal paths, this voltage is often the default midsupply voltage to retain the most available output swing around the voltage centered at the V_{OCM} voltage. For dc-coupled signal paths, set this voltage to minimum of $V_{VS\pm}$ ±2 V at V_S = ± 18 V and $V_{VS\pm}$ ±1 V at V_S = ± 2.5 V respectively. For precision ADC drivers, this output becomes the input common mode voltage of the ADC.

From the target output V_{OCM}, the next step is to verify that the desired output differential peak-to-peak voltage (V_{OPP}) stays within the supplies. For any desired differential V_{OPP}, make sure that the absolute maximum voltage at the output pins swings with 方程式 1 and 方程式 2 and confirm that these expressions are within the supply rails minus the output headroom required for the RRO device.

$$V_{Omax} = V_{OCM} + \frac{V_{OPP}}{2} \tag{1}$$

$$V_{Omin} = V_{OCM} - \frac{V_{OPP}}{2} \tag{2}$$

Most designs do not run into an input range limit. However, using the approach shown in this section can allow a quick assessment of the input V_{ICM} range under the intended full-scale output condition. The TINA-TI ™ simulation software can be used to plot the input voltages under the intended swings and application circuit to verify that there is no limiting from this effect. Increasing the positive and negative supplies slightly in simulation is an easy way to discover the simulated swings that might be going out of range.

9.1.2 DC Precision Analysis

9.1.2.1 DC Error Voltage at Room Temperature

Good dc linearity allows the designer to minimize the total dc output error of the system. In particular, this error divides into two contributions: the initial error at the normal operating condition of 25°C, and the drift error over temperature. The main sources of these errors typically arise from:

- Voltage error due to the input offset voltage (V_{IO})
- Voltage error due to noninverting and inverting bias current (I_{B-}, I_{B+})
- The common-mode rejection ratio (CMRR) of the FDA
- Voltage error due to mismatch between input and output common-mode voltages (V_{VOCM} – V_{ICM})

One major source of error comes from the effect of mismatched resistor values and the ratios on the two sides of the FDA. For this analysis, this error term is neglected. The effects are described separately in *节 9.1.4*.

The THP210 super-beta input device features extremely-low input bias current, trimmed low input offset voltage, and the lowest offset drift over the full temperature operating range. These features allow the device to produce a negligible initial error band at 25°C, but also exceptional robust behavior over temperature. The red curve in 图 9-1 showcases a simulation of the total dc error voltage at 25°C versus different gain configurations based on the application configuration shown in 图 9-2.

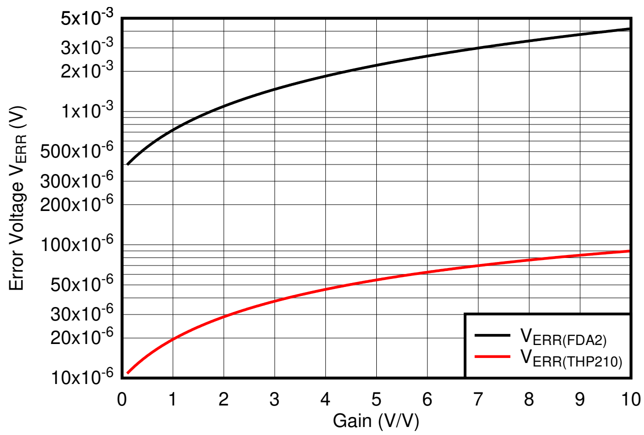


图 9-1. TINA-TI™ Software Simulation of DC Error Voltage at Different Gain Settings (Variable R_2)

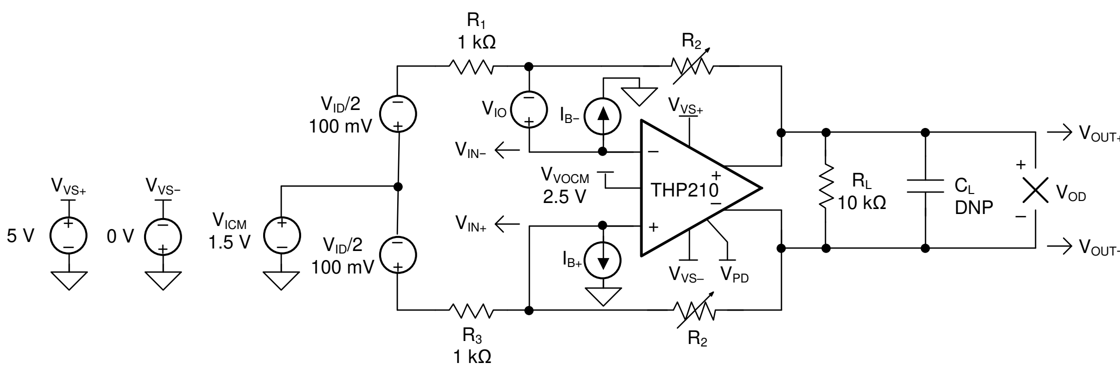


图 9-2. FDA DC Error Model

One use case at a differential input voltage of V_{ID} = 200 mV and a gain of 5 V/V (that corresponds to R_2 = 5 kΩ) reveals that the initial dc error of the THP210 is 4.5 µV. A comparable FDA2 with V_{IO} = 200 µV, I_B = 650 nA, and I_{IO} = 30 nA results in a 2.22-mV dc error voltage that results in a factor of approximately 500 higher dc error.

In addition, 图 9-3 shows that the absolute dc accuracy of the THP210 nearly adds an error voltage on the system. The dominant factors for the initial error band are mainly due to the feedback resistor mismatch that is not considered in the simulation plot.

9.1.2.2 DC Error Voltage Over Temperature

The THP210 offers excellent dc accuracy at room temperature. In many applications, calibration techniques are used to minimize the initial dc error; however, performing calibration over temperature is time-consuming and expensive.

The advanced drift specification of the THP210 helps to further mitigate the system error over temperature. 图 9-3 depicts the total error voltage at these given conditions:

- Circuit configuration as shown in 图 9-2
- Temperature range from –40°C to +125°C
- Resistor tolerance of 1%

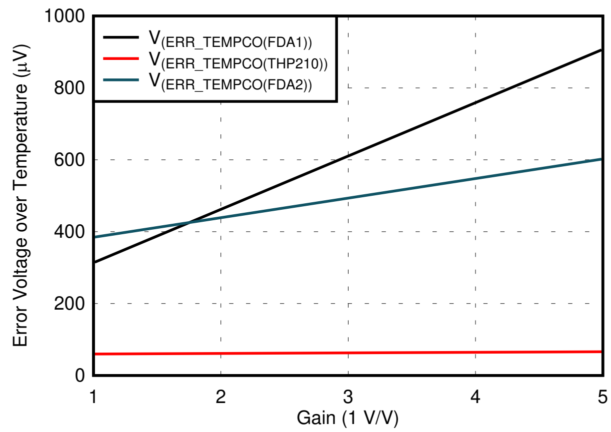


图 9-3. Calculation of Error Voltage Over Temperature at Different Gain Settings (Variable R_2)

The main contributors that are considered in this analysis are offset voltage drift, offset current drift, and bias current drift. As a result of the ultra-low bias current drift of 15 pA/°C, the impact of higher gain resistors and resistor tolerances marginally affects the error voltage with the THP210.

A use case at a gain of 5 V/V shows that the total dc error over temperature of the THP210 is at 66 µV, which is at least a factor of 10 smaller compared to existing, state-of-the-art FDAs.

9.1.3 Noise Analysis

An accurate output-noise calculation allows the designer to compare the performance of alternate FDA solutions. The combination of differential spot noise at the output pins of the FDA with any passive filtering to the ADC enables an accurate signal-to-noise ratio (SNR) calculation. This chapter incorporates key elements for an output noise analysis.

The first step in the output noise analysis is to reduce the application circuit to the simplest form with equal feedback and gain setting elements to ground. 图 9-4 shows the simplest analysis circuit with the FDA. This circuit considers the thermal resistor noise terms of the external feedback network and the intrinsic input voltage and current noise terms.

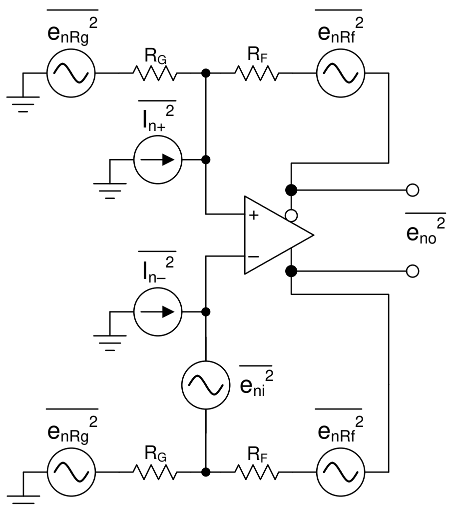


图 9-4. FDA Noise Analysis Circuit

The noise powers are shown in 图 9-4 for each term. When the R_F and R_G (or R_I) terms are matched on each side, the total differential output noise is the root sum squared (RSS) of these separate terms.

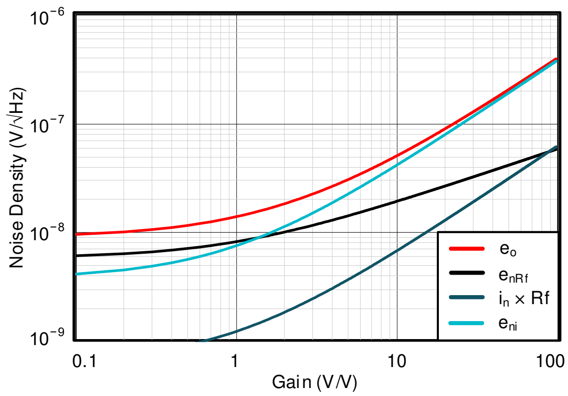
Using NG ≡ 1 + R_F / R_G as the noise gain, the total output noise density is given by 方程式 3. Each resistor noise term is a 4kT × R power (4kT = 1.6E-20 J at 290 K).

$$e_o = \sqrt{(e_{ni}NG)^2 + 2(i_N R_F)^2 + 2(4kTR_F NG)} \tag{3}$$

where:

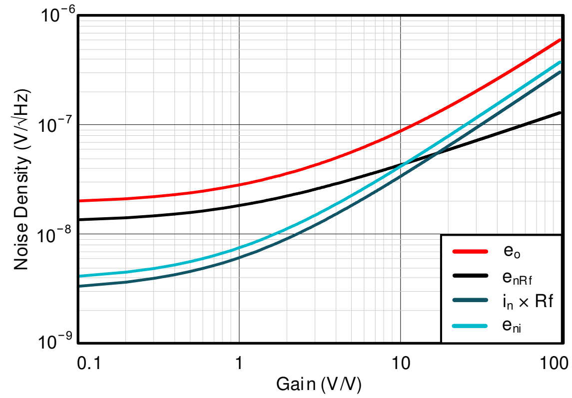
- e_{ni} is the differential input spot noise times the noise gain.
- i_n x R_F is the input current noise terms times the feedback resistor.
  Because there are two uncorrelated current noise terms, the power is two times one of them.
- e_{nRF} is the thermal output noise resulting from both the R_F and R_G resistors at twice the value for the output noise power of each side added together.

图 9-5 and 图 9-6 provide a graphical comparison of the described noise densities versus different gain settings. Each of the contributors are separately showcased in the graphs. As expected, lower feedback resistors (in this case, 2 kΩ) show that the dominant factor of the total output noise is the intrinsic voltage noise of the FDA (at gains > 2). For smaller gain settings, the thermal noise of the feedback resistors is dominating.



R_F = 2 kΩ

图 9-5. Calculated Noise Densities vs Gain Settings



R_F = 10 kΩ

图 9-6. Calculated Noise Densities vs Gain Settings

The advancement of the THP210 can be seen at higher feedback resistors (in this case 10 kΩ). Many FDAs exhibit an input current noise density in the range of some pA/$\sqrt{Hz}$ that, in cases for higher feedback resistors, dictate the noise behavior. As a result of the superior current noise density of 300 fA/$\sqrt{Hz}$ of the THP210, the overall output noise is mainly dominated by the thermal noise of the resistors (here, up to gains of approximately 15).

The total output voltage noise density is important when using FDAs as ADC input driver stages. To evaluate the compatibility between the input driver and the ADC from a noise perspective, compare the calculated RMS output noise of the FDA with the least-significant bit (LSB) of the desired ADC application, in respect to the effective number of bits (ENOB). 节 9.2.2 shows measurements of the THP210 in combination with state-of-the-art SAR ADCs, and indicates the performance that is achieved.

9.1.4 Mismatch of External Feedback Network

The common-mode rejection ratio (CMRR) is one of the key elements when designing with fully differential amplifiers. Although FDAs are designed to provide the best CMRR performance, poor selection of external gain setting resistors, as well as careless board layout techniques, significantly degrade CMRR performance.

In an ideal world, the resistors in a typical circuit, as shown in the test circuit 图 7-1, are chosen to be R_{F1} / R_{F2} = R_{I1}/R_{I2}. Mismatch between these ratios causes the differential output to depend on the input common-mode voltage (V_{VOCM}), and that in turn produces an offset and excess noise on the differential output. As mentioned in the previous section, the mismatch of the external resistor network primarily contributes to the dc error. Generally, a resistor mismatch of 0.1% and a ratio of 1 V/V results in a CMRR of 60 dB. The natural degradation of the external resistor network is minimized by the following guidelines:

- Consider input impedance matching, as shown in the *Input impedance matching with fully differential amplifiers* technical brief.
- Follow layout guidelines, as provided in 节 11.1.
- Use compensation techniques, as described in the *Improving PSRR and CMRR in Fully Differential Amplifiers* application report

Despite the mismatch of the external feedback network, the internal common-mode feedback amplifier regulates the outputs to remain balanced in amplitude and remain 180° out of phase. The output balance performance stays unaffected by the CMRR degradation.

9.1.5 Operating the Power-Down Feature

The power-down feature on the THP210 puts the device into a low power-consumption state, with quiescent current minimized. To force the device into the low-power state, drive the $\overline{PD}$ pin lower than the power-down threshold voltage (V_{VS+} – 2 V). Driving the $\overline{PD}$ pin lower than the power-down threshold voltage forces the internal logic to disable both the differential and common-mode amplifiers. The PD pin has an internal pullup current that allows the pin to be used in an open-drain MOSFET configuration without an additional pullup resistor, as seen in 图 9-7. In this configuration, the logic level can be referenced to the MOSFET, and the voltage at the $\overline{PD}$ pin is level-shifted to account for use with high supply voltages. Be sure to select an N-type MOSFET with a maximum B_{VDSS} greater than the total supply voltage.

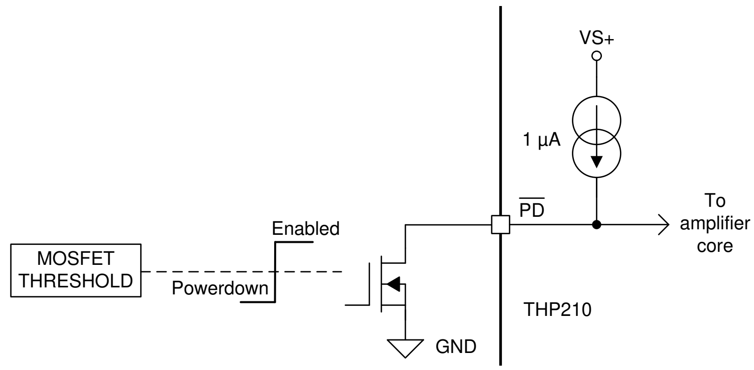


图 9-7. Power-Down ($\overline{PD}$) Pin Interface With Low-Voltage Logic Level Signals

For applications that do not use the power-down feature, tie the $\overline{PD}$ pin to the positive supply voltage.

When $\overline{PD}$ is low (device is in power down) the output pins is in a high-impedance state.

9.1.6 Driving Capacitive Loads

In most ADC applications, an FDA is required to drive capacitive load of an RC charge kickback filter. Other applications may require some other next-stage devices to be driven. The strong output stage of the THP210 drives higher capacitive loads compared to other FDAs. 图 6-25 implies that the small-signal overshoot is less then 20% at a direct capacitive load connection of 140 pF. To help avoid instability and drive higher capacitive loads, add a small resistor (referred to as isolation resistor R_{ISO} in both this plot and 图 6-26) at the outputs of the THP210 before the capacitive load.

9.1.7 Driving Differential ADCs

The THP210 provides a differential output interface to drive a variety of modern, high-performance ADCs. The following section describes the key elements that must be considered when designing a differential input driver for SAR ADCs.

9.1.7.1 RC Filter Selection (Charge Kickback Filter)

The sample-and-hold operating behavior of SAR ADCs causes charge transients at the input stage, and thus to the output stage of the amplifier. The RC filter helps to attenuate the sampling charge injection from the switched capacitor input stage of the ADC. A careful design is critical to meet linearity and noise performance of the ADC.

图 9-8 and 图 9-9 show a single-ended and differential filter approach, respectively.

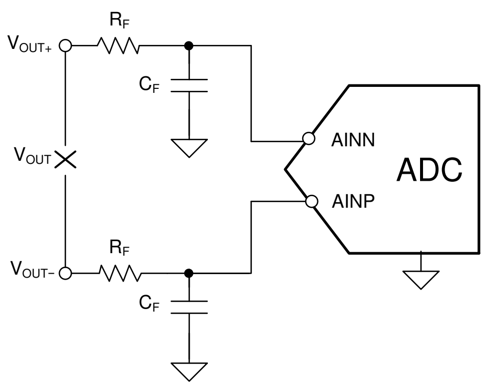


图 9-8. Single-Ended Filter

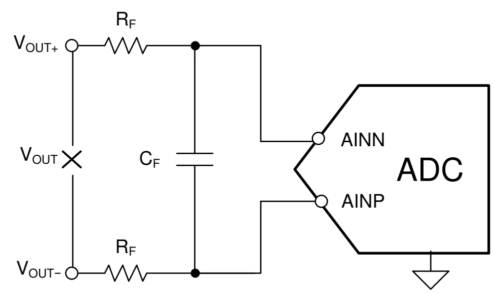


图 9-9. Differential Filter

Choose the capacitor to be at least 10 times larger than the specified value of the SAR ADC sampling capacitor. A trade-off must be considered for the isolation resistor, where a higher damping effect is achieved at higher values, and lower value provide better THD at the input of the ADC. To select the best RC combination, use the Analog Engineering Tool.

One important element to consider is that the small-signal bandwidth of the FDA (f_{SSBW_FDA}) determines what the cutoff frequency of the RC filter combination can be driven at the inputs of the ADC. Depending whether a single-ended filter or a differential filter is used the minimum required small-signal bandwidth of the FDA (f_{SSBW_FDA}) can be estimated by 方程式 4:

$$f_{SSBW\_FDA} > \frac{1}{2\pi \cdot SEL \cdot R_F \cdot C_F} \tag{4}$$

where:

- SEL = 1 for single-ended filter, SEL = 2 for differential filter

Driving higher capacitive loads degrades the phase margin of the FDA, and causes instability issues. Best practice is to perform a SPICE simulation using TINA-TI™ simulation software to confirm that the desired circuit is stable; that is, the FDA has more than a 45° phase margin.

9.1.7.2 Settling Time Driving the ADC Sample-and-Hold Operating Behavior

The RC filter between the amplifier and the ADC helps the amplifier drive the sampling capacitor during charging (acquisition) and discharging (conversion) times. During the acquisition time, if the amplifier has a load transient at the output, the time needed to recover (or settle) is commonly defined as the settling time. Typically, to achieve minimal distortion, the end value to settle is within ½ of the ADC least significant bit (LSB).

The specified settling time of the FDA is the time required for the amplifier to recover from transients caused at the THP210 output. Although the frequency response characteristics impact the settling time of the ADC application, these characteristics are not the key element to consider. The settling time of the FDA to react to load transients depends primarily on the output impedance of the amplifier at the required signal bandwidth. 方程式 5 calculates the settling time, considering the time constant of the RC combination:

$$t_{settle} = -\ln\left(\frac{1}{2^N \times SET}\right) \times \tau \tag{5}$$

where:

- N is the number of bits in the ADC application
- τ equals $R_F \times C_F$
- SET = 2 for a settling of ½ LSB, SET = 4 for a settling of ¼ LSB, and so on.

In order to verify whether the chosen RC filter combination fulfills the settling behavior, simulate the desired circuit with TINA-TI™ simulation software.

9.1.7.3 THD Performance

The input driver and the ADC both introduce harmonic distortion in the data acquisition block that generates undesired signals in the output harmonically related to the input signal. Total harmonic distortion (THD) can be very important in applications measuring ac signals. However, there are also ADC dc-measurement applications that are only concerned with SNR and linearity. To make sure that the total system distortion performance is not dominated by the front-end stage, the distortion of the driver circuitry must be at least 10 dB less than the distortion of the ADC, as shown in 方程式 6:

$$THD_{FDA} \leqslant THD_{ADC} - 10\ \text{dB} \tag{6}$$

The harmonic distortion of an FDA mainly relates to the open-loop linearity in the output stage corrected by the loop gain at the fundamental frequency. When the total load impedance decreases, including the effect of the feedback resistors loadings, the output stage open-loop linearity degrades, and thus worsens the harmonic distortion, as seen in 图 6-10.

Another effect that results from the RC filter is that the load impedance changes over frequency, which also influences the THD.

An additional dependency is given by the output voltage swing. Increasing the output voltage swing increases the nonlinearities of the open-loop output stage, thus degrading the harmonic distortion.

In summary, the harmonic distortion is negatively affected not only with decreasing load impedance and increasing output voltage swing, but also with increasing noise gain.

节 9.2.2 provides an measurement results of the THD performance using the THP210 and the ADS891x ADC series.

9.2 Typical Applications

9.2.1 MFB Filter

A common application use case for fully-differential amplifiers is to easily convert a single-ended signal into a differential signal to drive a differential input source, such as an ADC or class D amplifier. 图 9-12 shows an example of the THP210 used to convert a single-ended, low-voltage signal source, such as a small electric microphone, and deliver a low-noise differential signal that is common-mode shifted to the center of the ADC input range. A multiple-feedback (MFB) configuration is used to provide a Butterworth filter response, giving a 40-dB/decade cutoff with a –3-dB frequency of 30 kHz.

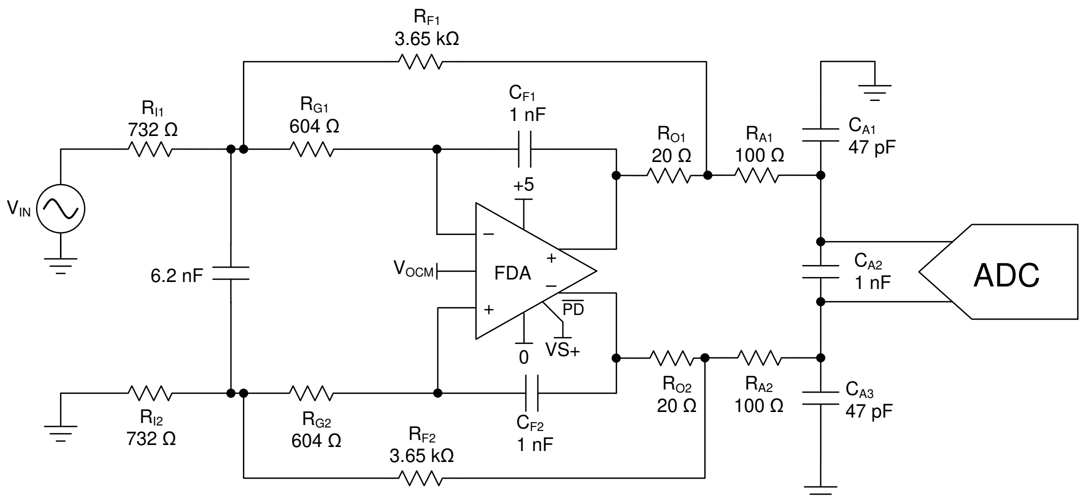


图 9-10. Example 30-kHz Butterworth Filter

9.2.1.1 Design Requirements

The requirements for this application are:

- Single-ended to differential conversion
- 5-V/V gain
- Active filter set to a Butterworth, 30-kHz response shape
- Output RC elements set by SAR input requirements (not part of the filter design)
- Filter element resistors and capacitors are set to limit added noise over the THP210

9.2.1.2 Detailed Design Procedure

The design proceeds using the techniques and tools suggested in the *Design Methodology for MFB Filters in ADC Interface Applications* application note. The process includes:

- Scale the resistor values to not meaningfully contribute to the output noise produced by the THP210.
- Select the RC ratios to hit the filter targets when reducing the noise gain peaking within the filter design.
- Set the output resistor to 10 Ω into a 1-nF differential capacitor.
- Add 47-pF common-mode capacitors to the load capacitor to improve common noise filtering.
- Inside the loop, add 20-Ω output resistors after the filter feedback capacitor to increase the isolation to the load capacitor.

9.2.1.3 Application Curve

The gain and phase plots are shown in 图 9-11. The MFB filter features a Butterworth responses feature very flat passband gain, with a 2-pole rolloff at 30 kHz to eliminate any higher-frequency noise from contaminating the signal chain and potentially alias back into the desired band.

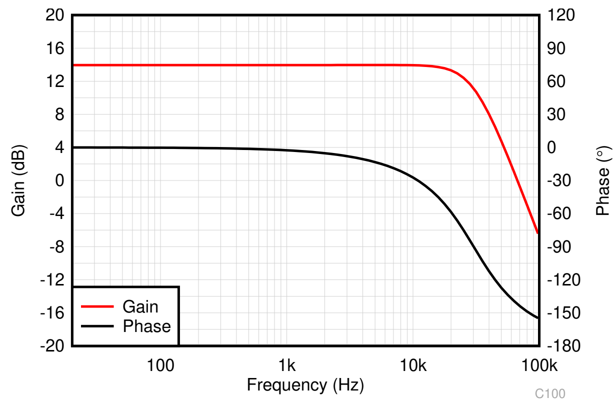


图 9-11. Gain and Phase Plot for a 30-kHz Butterworth Filter

9.2.2 ADS891x With Single-Ended RC Filter Stage

The application circuit in 图 9-12 shows the schematic of a complete reference driver circuit that generates a full-scale range of 4.5 V at the ADC using a unipolar supply voltage of 5 V. This circuit is used to measure the driving capability of the THP210 with the different variants of the ADS891x ADC.

To test the complete dynamic range of the circuit, the common-mode voltage V_{OCM} of the input of the ADC is established at a value of V_{REF} / 2. To exclude distortion caused by reference voltage V_{REF} and common-mode voltage V_{OCM} of the ADC, the test circuit uses the low-noise OPA2625 in an inverting gain configuration for V_{OCM}, and the high-precision, low-noise REF5050 for V_{REF}. See the ADS8910BEVM-PDK user's guide for more details.

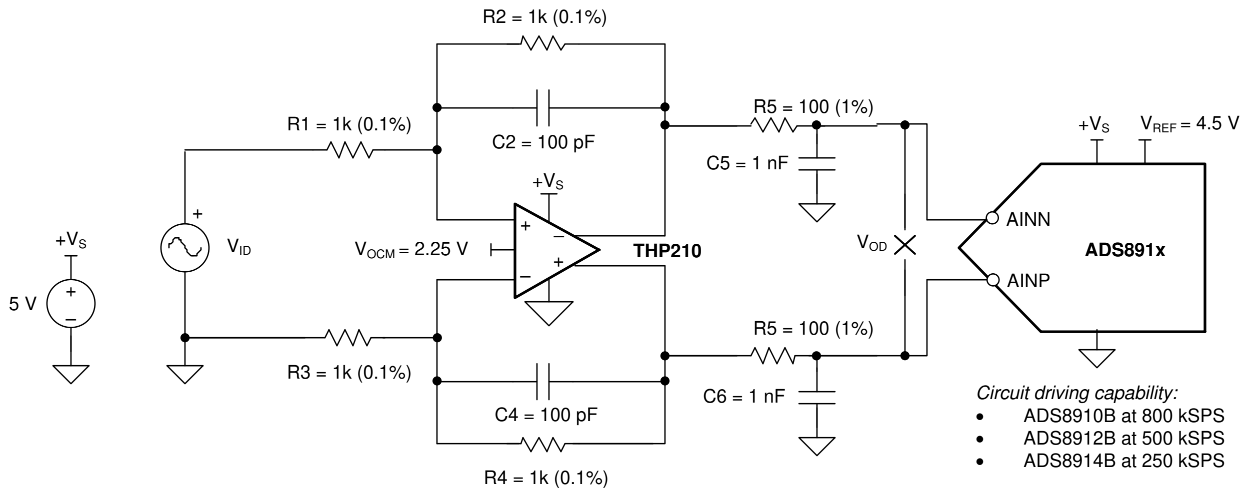


图 9-12. Driving ADS891x With Single-Ended RC Filter Stage

9.2.2.1 Design Requirements

The requirements for this application are:

- Differential to differential conversion
- Unipolar supply voltage of 5 V
- Full-scale range of ADC of FSR = ±4.5 V
- Input signal amplitude of V_{REF} – 0.4 dB
- Driver configuration in unity-gain buffer configuration (1-V/V gain)
- Circuit bandwidth $f_{(-3dB)}$ = 935 kHz
- Output RC elements set by SAR input requirements

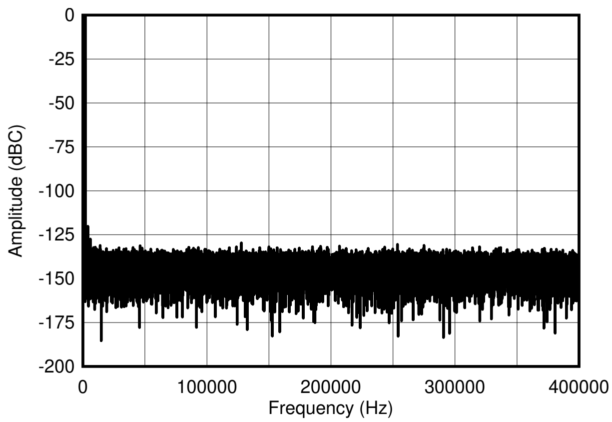
9.2.2.1.1 Measurement Results

The THP210 and the filter combination listed in 节 9.2.2.1 allow for the best trade-off between harmonic distortion and maintaining stability of the FDA. 表 9-1 and 图 9-13 through 图 9-15 showcase the device performance.

表 9-1. THP210 + ADS891x: FFT Data Summary

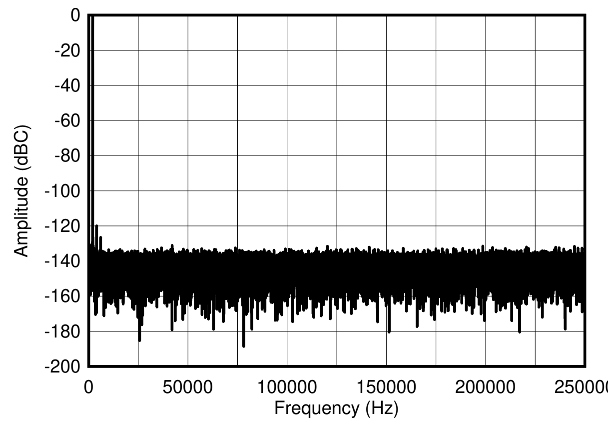
ADC VERSION	ADC SPECIFICATION	SAMPLING RATE	SNR	THD(1)	SINAD
ADS8910B	1-MSPS max, 18 bit	800 kSPS	100.37 dB	–118.4 dB	100.31 dB
ADS8912B	500 kSPS, 18 bit	500 kSPS	100.4 dB	–118.44 dB	100.33 dB
ADS8914B	250 kSPS, 18 bit	250 kSPS	100.37 dB	–118.72 dB	100.33 dB

(1) THD can further be improved by providing a bipolar power supply for more headroom for the negative voltage swing. In the given circuit, a negative supply of V_{S-} = 0.23 V improved the THD to –120.5 dB.



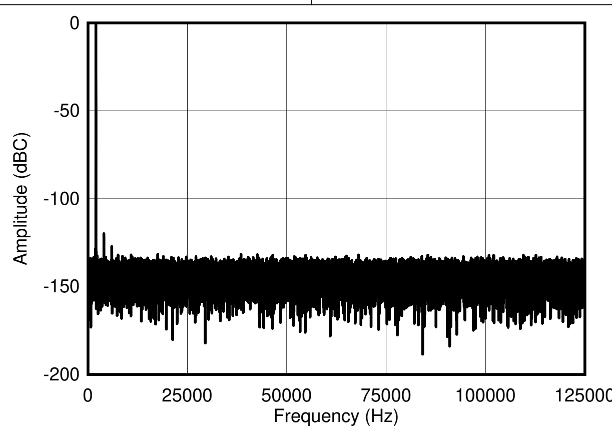
f_{IN} = 2 kHz, 100.37 dB SNR, –118.4 dB THD

图 9-13. Noise Performance FFT Plot: THP210 + ADS8910B, 800 kSPS, 18-Bit



f_{IN} = 2 kHz, 100.4 dB SNR, –118.44 dB THD

图 9-14. Noise Performance FFT Plot: THP210 + ADS8912B, 500 kSPS, 18-Bit



f_{IN} = 2 kHz, 100.37 dB SNR, –118.72 dB THD

图 9-15. Noise Performance FFT Plot: THP210 + ADS8914B, 250 kSPS, 18-Bit

9.2.3 Attenuation Configuration Drives the ADS8912B

Many applications require to level-shift high-voltage input signals down to the lower-voltage ADC domain. 图 9-16 shows an example of the THP210 used to attenuate a ±10-V differential signal to drive a differential SAR ADC with full-scale range of ±4.5V. The common-mode voltage is shifted to the center of the ADC input range. A multiple-feedback (MFB) configuration as described in 节 9.2.1 is used to provide a Butterworth filter response, giving a 40-dB/decade roll-off with a –3-dB frequency of 100 kHz. The THP210 is powered with a 5-V supply and a –0.232-V negative supply generated by the low-noise negative bias generator (LM7705) allowing additional headroom for output swing to GND with ultra-low distortion. Alternatively, the THP210 can be powered using a unipolar 5-V supply with good distortion performance.

The circuit is able to drive the ADS8912B 18-Bit SAR ADC at full throughput of 500-kSPS.

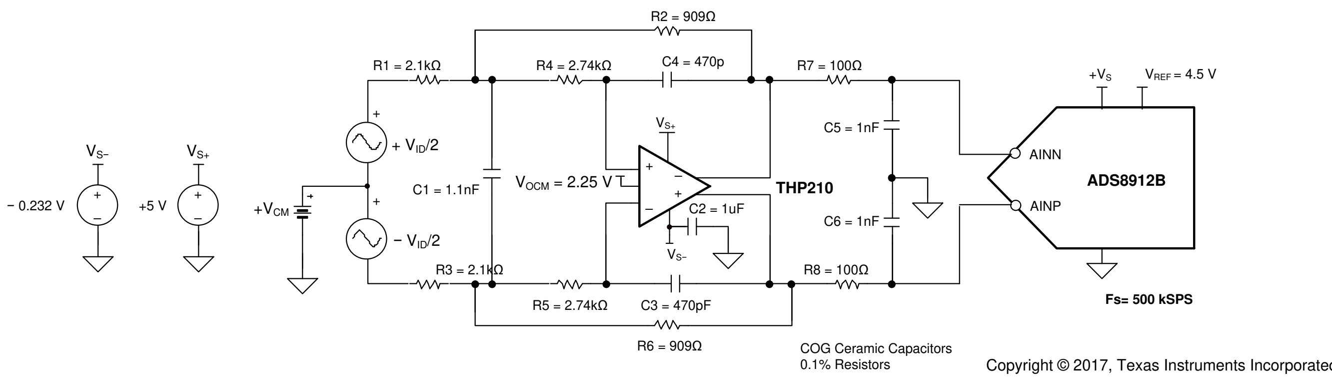


图 9-16. Driving ADS8912B in Attenuation Configuration of 0.4333 V/V

9.2.3.1 Design Requirements

The requirements for this application are:

- Differential to differential conversion
- Second order Butterworth filter with corner frequency of 100 kHz, offering flat frequency response
- Circuit accepts fully differential input signal of Vdiff = ± 10 V
- Circuit Attenuation is set to 0.433 V/V (–7.273 dB)
- Full-scale range of ADC of FSR = ±4.5 V
- Filter elements set to limit added noise over THP210 while maintaining circuit stability
- Output RC elements set by SAR input requirements

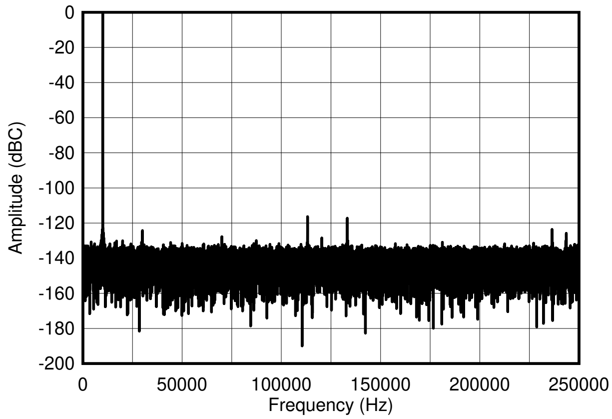
For a detailed design procedure, see 节 9.2.1.2.

9.2.3.1.1 Measurement Results

图 9-17 and 图 9-18 showcases the measured performance of the discussed circuit with SNR and THD results.

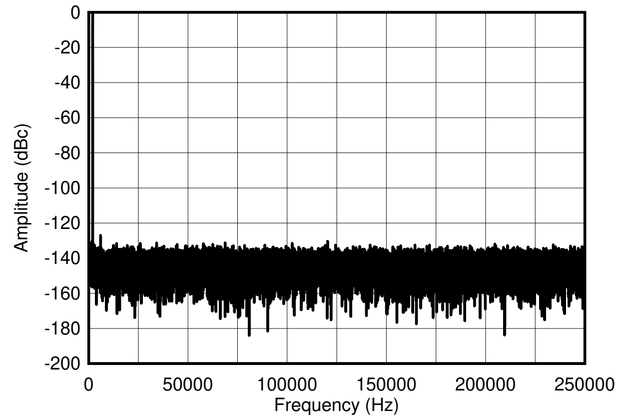
表 9-2. THP210 + ADS8912B in Attenuation – FFT Data Summary

ADC VERSION	ADC SPECIFICATION	SAMPLING RATE	INPUT SIGNAL	SNR	THD
ADS8912B	500 kSPS, 18 bit	500 kSPS	f_{IN} = 2 kHz	100.4 dB	– 124.2 dB
ADS8912B	500 kSPS, 18 bit	500 kSPS	f_{IN} = 10 kHz	99.1 dB	– 120.4 dB



f_{IN} = 10 kHz, 99.1-dB SNR, – 120.4-dB THD

图 9-17. Noise Performance FFT: THP210 + ADS8914B in Attenuation, 500 kSPS, 18 Bit, f_{IN} = 10 kHz



f_{IN} = 2 kHz, 100.4-dB SNR, – 124.2-dB THD

图 9-18. Noise Performance FFT: THP210 + ADS8914B in Attenuation, 500 kSPS, 18 Bit, f_{IN} = 2 kHz

10 Power Supply Recommendations

The THP210 operates from supply voltages of 3.0 V to 36 V (±1.5 V to ±18 V for dual supply). Connect ceramic bypass capacitors from both VS+ and VS – to GND.

11 Layout

11.1 Layout Guidelines

11.1.1 Board Layout Recommendations

- Keep differential signals routed together to minimize parasitic impedance mismatch.
- Connect a 0.1-µF capacitor to the supply nodes through a via.
- If no external voltage is used, connect a 0.1-µF capacitor to the VOCM pin.
- Keep any high-frequency nodes that can couple through parasitic paths away from the VOCM node.
- Clean the printed circuit board (PCB) after assembly to minimize any leakage paths from excess flux into the VOCM node.

11.2 Layout Example

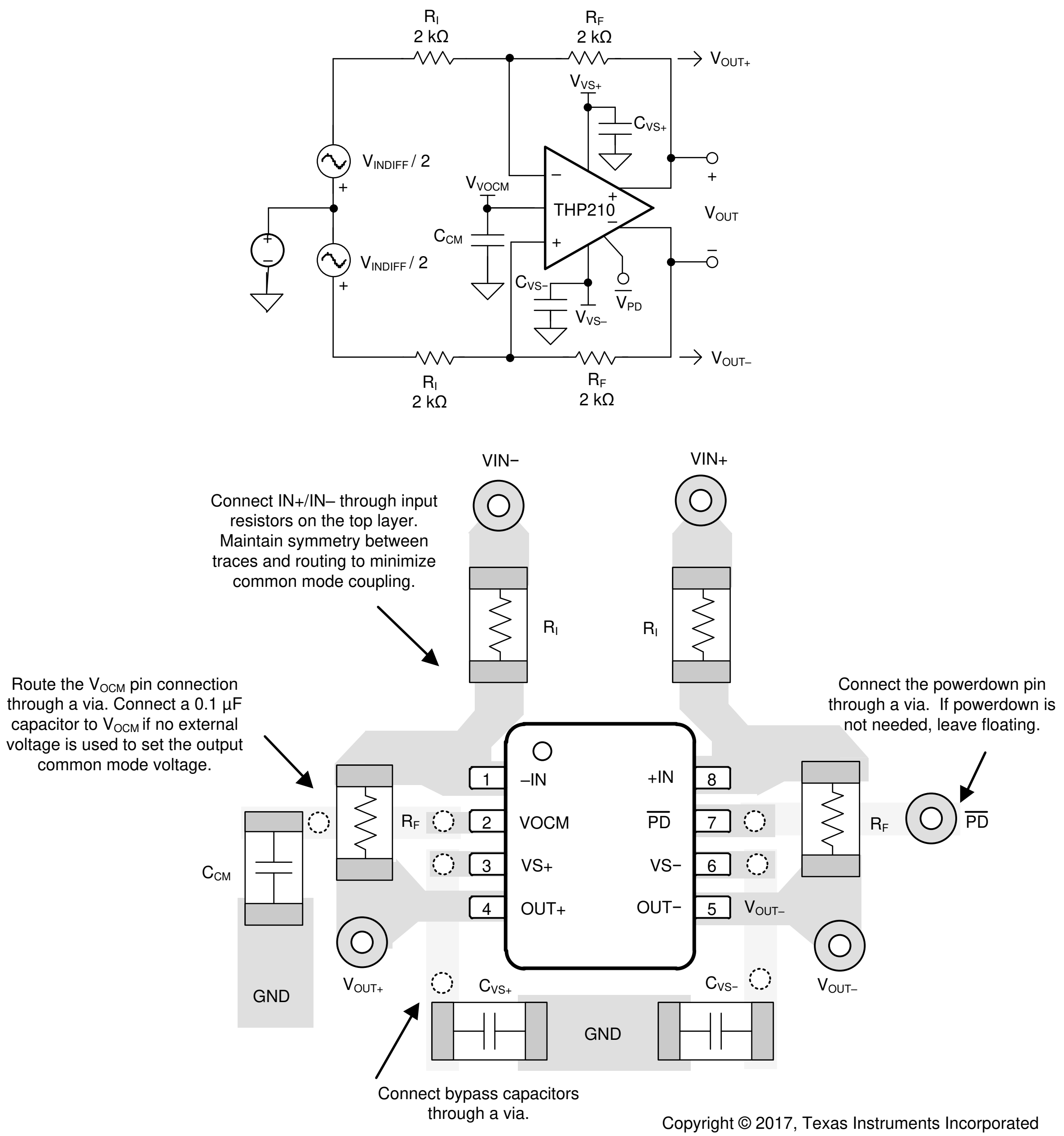


图 11-1. Example Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- THP210 TINA-TI™ Simulation Software model
- *TINA-TI Gain of 0.2 100kHz Butterworth MFB Filter*
- *TINA-TI 100kHz MFB filter LG test*
- *TINA-TI Differential Transimpedance LG Sim*

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA188 Precision, Zero-Drift, Rail-to-Rail Out, High-Voltage Instrumentation Amplifier* data sheet
- Texas Instruments, *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™* data sheet
- Texas Instruments, *OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers* data sheet
- Texas Instruments, *Design Methodology for MFB Filters in ADC Interface Applications* application report
- Texas Instruments, *Design for Wideband Differential Transimpedance DAC Output* application report

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THP210DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1237	Samples
THP210DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1237	Samples
THP210DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	THP210	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

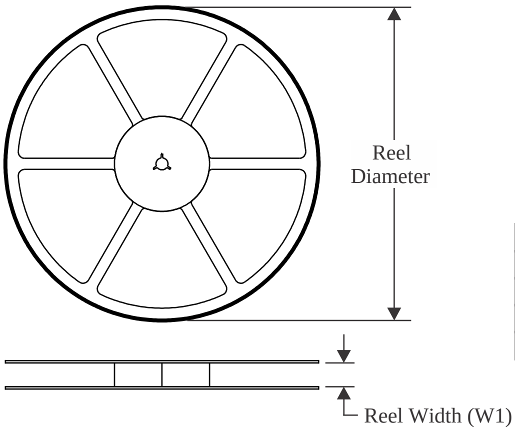
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

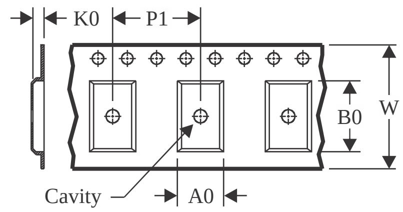
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

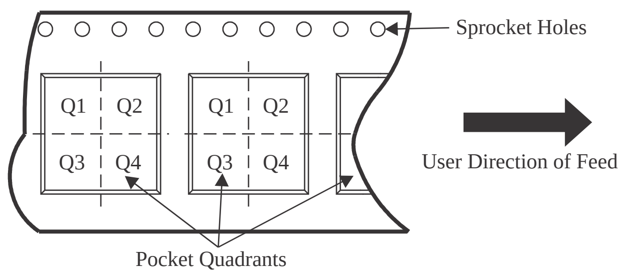
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





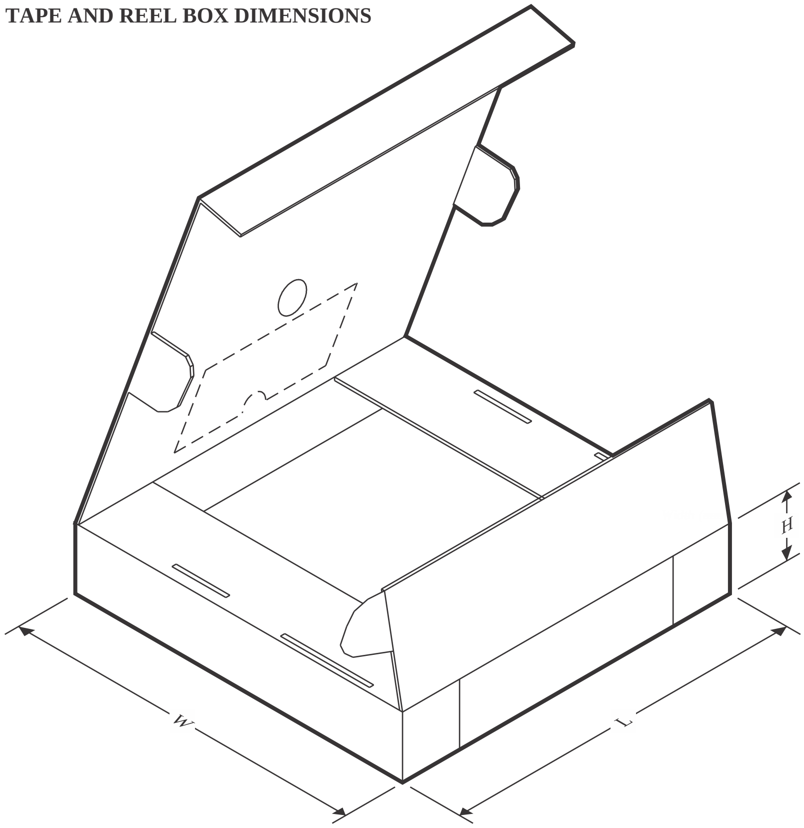
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THP210DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THP210DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THP210DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



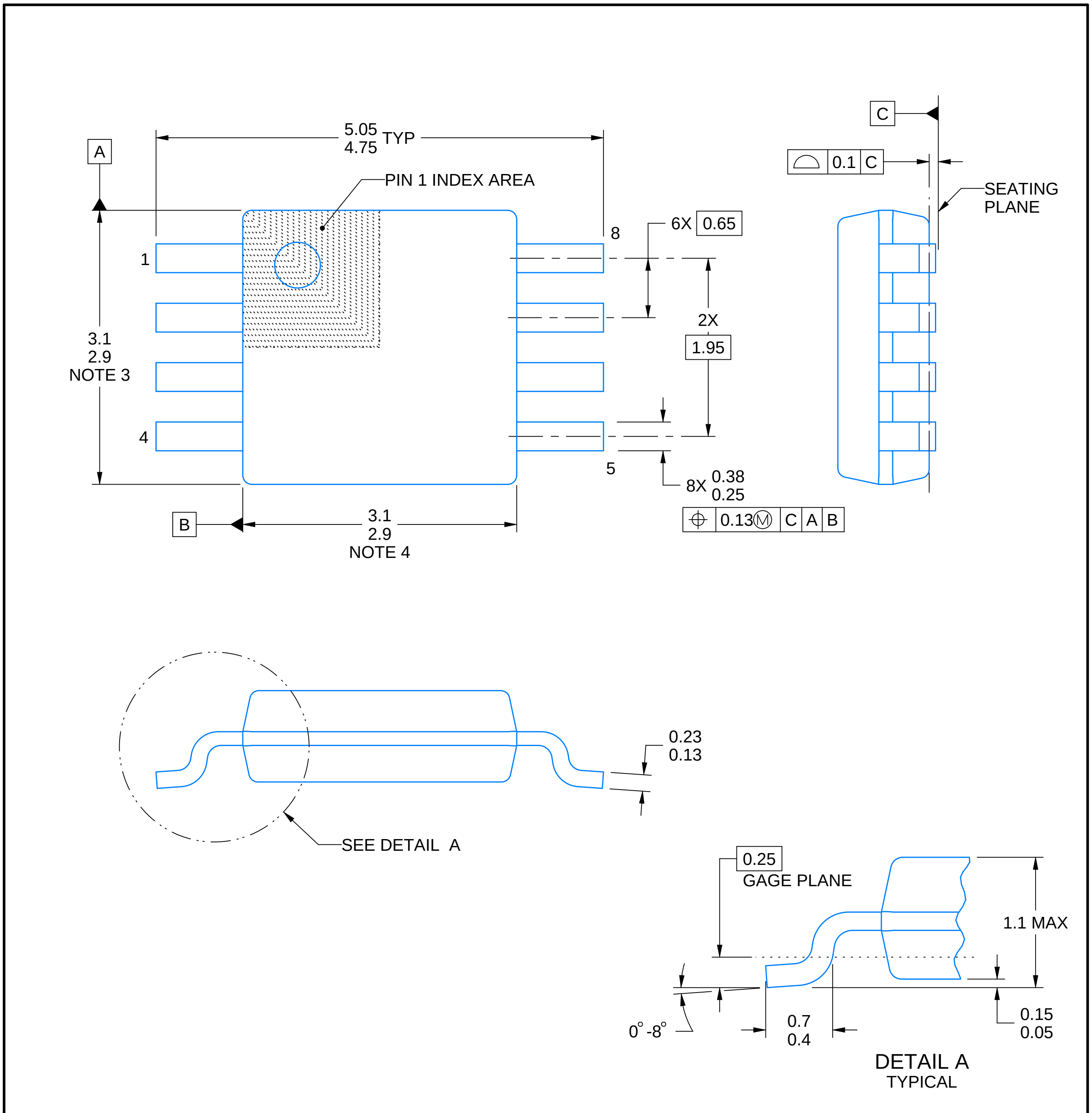
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THP210DGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
THP210DGKT	VSSOP	DGK	8	250	356.0	356.0	35.0
THP210DR	SOIC	D	8	2500	356.0	356.0	35.0

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

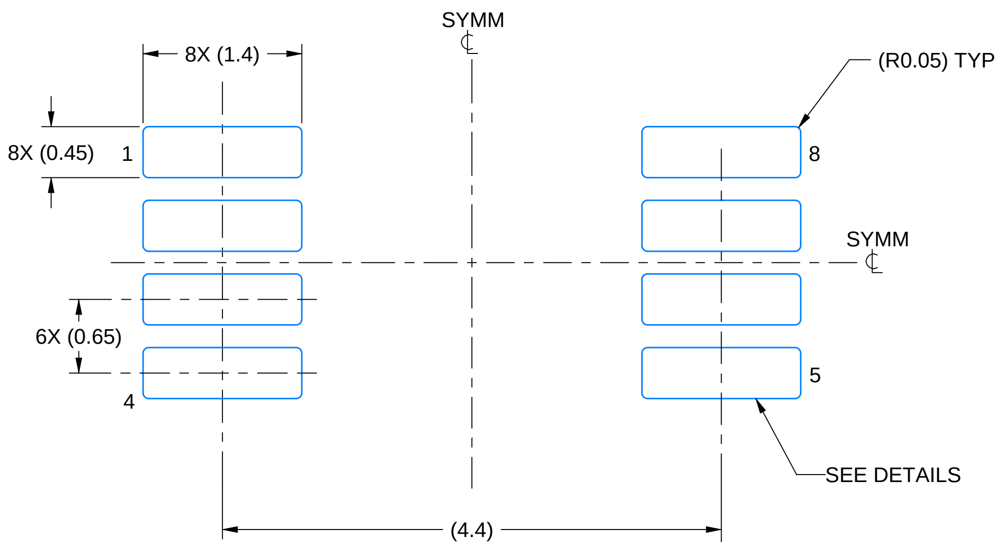


4214862/A 04/2023

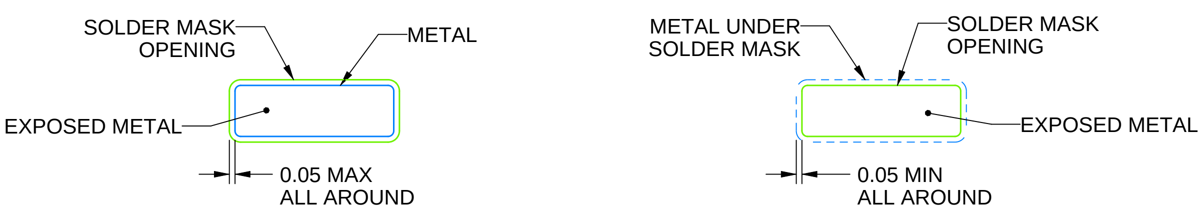
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK DEFINED (PREFERRED)

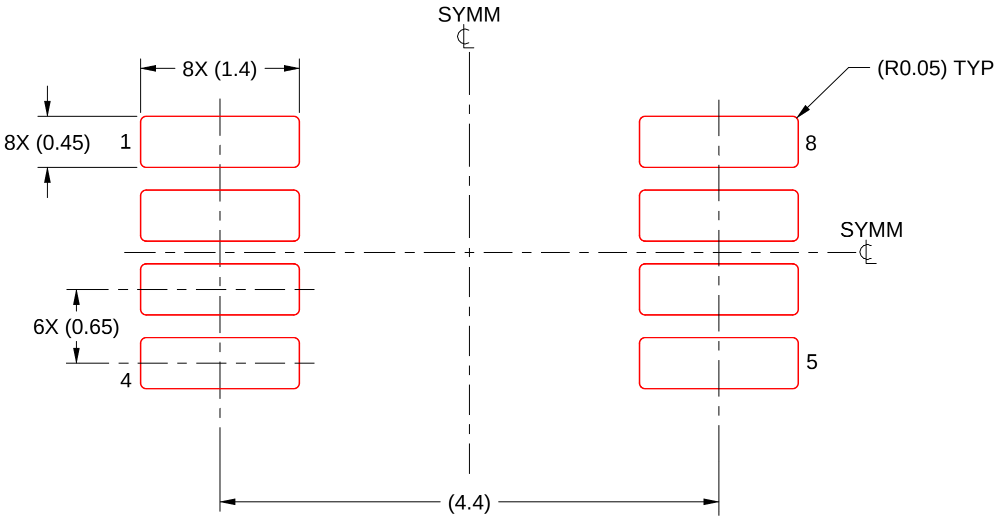
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

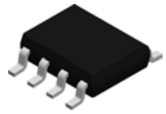


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

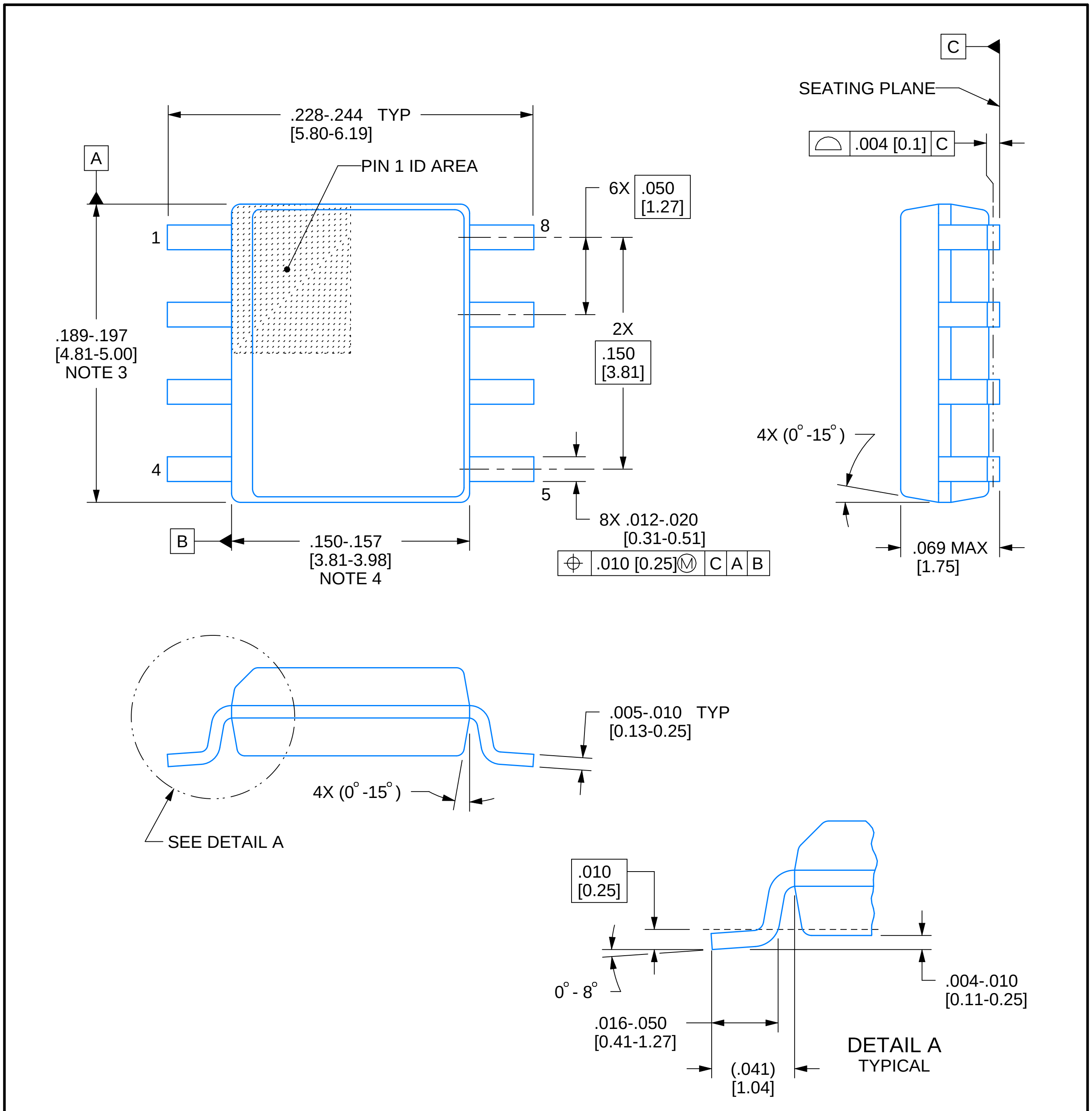


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

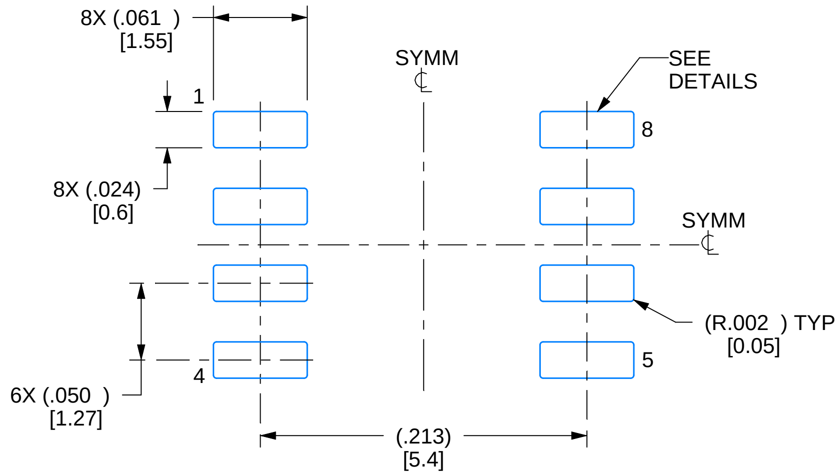
SMALL OUTLINE INTEGRATED CIRCUIT



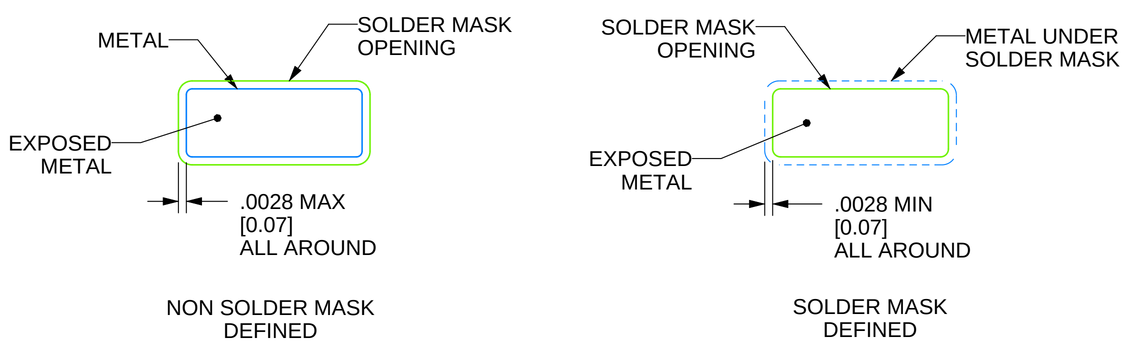
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

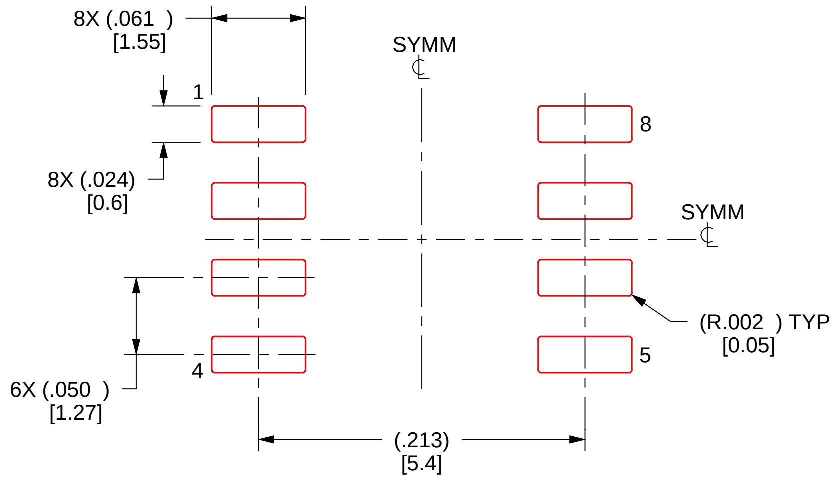


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265