THS3217 直流至 800MHz、差分转单端、DAC 输出放大器

1 特性

- 输入级：2V/V 的内部增益
  - 经缓冲的差分输入
  - 单端低阻抗输出
  - 全功率带宽：500MHz (2 V_{PP})
- 输出级：可从外部配置增益
  - 全功率带宽：500MHz (5 V_{PP})
  - 转换率：5000V/μs
  - 单刀双掷 (SPDT) 输入开关/多路复用器
- 完整信号路径：输入级 + 输出级
  - 二次谐波 (HD2)（20MHz，5V_{PP} 接至 100Ω 负载）：–60dBc
  - 三次谐波 (HD3)（20MHz，5V_{PP} 接至 100Ω 负载）：–75dBc
  - 10V_{PP} 输出接至 100Ω 负载，使用 ±6.5V 分离电源
  - 12V_{PP} 输出接至高容性负载，使用 15V 单电源
- 内部直流 (DC) 基准缓冲器，具有低阻抗输出
- 电源范围：
  - 分离电源：±4V 至 ±7.9V
  - 单电源：8V 至 15.8V

2 应用

- 数模转换器 (DAC) 输出放大器
- 宽带任意波形发生器 (AWG) 输出驱动器
- 前置驱动器接至 > 20V_{PP} 输出放大器 (THS3091)
- 适用于压电式元件的单电源、高容性负载驱动器

3 说明

THS3217 整合了连接互补电流输出数模转换器 (DAC) 时所需的关键信号链组件。此双级放大器系统极具灵活性，可广泛应用于各类系统中以提供低失真、直流耦合的差分转单端信号处理。输入级会对 DAC 电阻端进行缓冲，并以 2V/V 的固定增益对信号进行差分至单端转换。差分转单端输出可在外部直接使用，也可经 RLC 滤波器或衰减器连接至内部输出功率级 (OPS) 的输入端。宽带、电流反馈输出功率级可在外部为全部引脚灵活设置增益。

输出功率级同相输入内部连接有一个 2×1 多路复用器 (mux)，方便选择内部差分转单端级 (D2S) 输出或外部输入。

可选片上中间电压缓冲器提供了宽带、低输出阻抗电源，可在单电源运行期间通过信号路径级提供偏置。此功能可为运行电源电压最高为 15.8V 的 应用 提供非常简单的偏置方法。此缓冲器接外部输入后可实现直流纠错环路或简单的输出直流偏移功能。

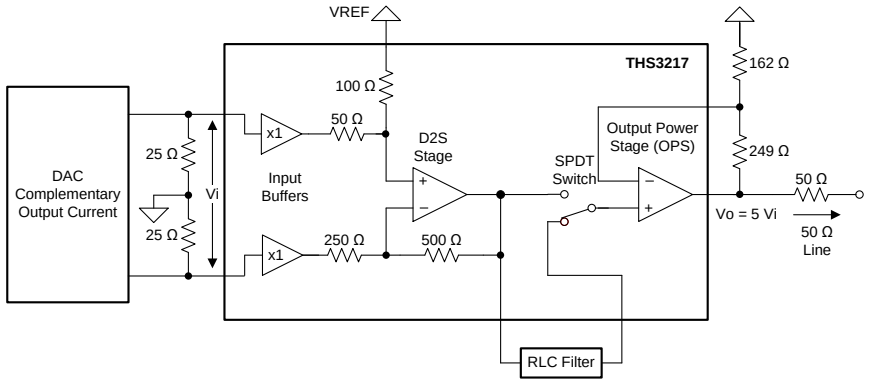
一款配套器件，THS3215，能够以更低的静态功率和带宽提供相同的功能 特性 。THS3217 和 THS3215 支持面向 AWG 应用的德州仪器 (TI) 新上市的高速 DAC，例如 DAC38J82。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
THS3217	VQFN (16)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

增益 = 5V/V，带可选外部滤波器的差分转单端线路驱动器



目录

4 修订历史记录

Changes from Revision A (February 2016) to Revision B **Page**

- Deleted open-loop transimpedance gain max value ... 7
- Deleted external to internal input offset voltage match min and max values ... 7
- Changed external to internal input offset voltage match test level from A to C ... 7
- Deleted dc output impedance min and max values ... 10
- Changed dc output impedance test level from A to C ... 10

Changes from Original (February 2016) to Revision A **Page**

- 已从“产品预览”更改为“量产数据” ... 1

5 Device Comparison Table

DEVICE	SMALL-SIGNAL BANDWIDTH 0.1 V_{PP} (A_V = 5 V/V)(1)	LARGE-SIGNAL BANDWIDTH 5V_{PP} (A_V = 5 V/V)	QUIESCENT CURRENT, Icc (±6-V SUPPLIES)	TOTAL HARMONIC DISTORTION (5 V_{PP}, R_{LOAD} = 100 Ω, 20 MHz)	CONTINUOUS OUTPUT CURRENT	PEAK OUTPUT CURRENT
THS3217	800 MHz	500 MHz	55 mA	–60 dBc	110 mA	175 mA
THS3215	350 MHz	250 MHz	35 mA	–50 dBc	80 mA	125 mA

(1) A_V is the voltage gain.

6 Pin Configuration and Functions

RGV Package
16-Pin VQFN
Top View

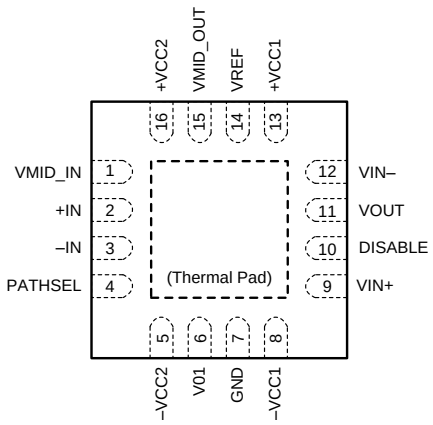


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VMID_IN	Input	DC reference buffer input
2	+IN	Input	Positive signal input to D2S
3	–IN	Input	Negative signal input to D2S
4	PATHSEL	Input	Internal SPDT switch control: low selects the internal path, and high selects the external path
5	–VCC2(1)	Power	Negative supply for input stage
6	VO1	Output	D2S external output
7	GND	Power	Ground for control pins reference
8	–VCC1(1)	Power	Negative supply for output stage
9	VIN+	Input	External OPS noninverting input
10	DISABLE	Input	Output power stage shutdown control: low enables the OPS, and high disables the OPS
11	VOUT	Output	OPS output
12	VIN–	Input	OPS inverting input
13	+VCC1(1)	Power	Positive supply for output stage
14	VREF	Input	DC offsetting input to D2S
15	VMID_OUT	Output	DC reference buffer output
16	+VCC2(1)	Power	Positive supply for input stage
Thermal Pad		—	Connect the thermal pad to GND for single-supply and split-supply operation. See *Thermal Considerations* section for more information.

(1) Throughout this document +V_{CC} refers to the voltage applied at the +VCC1 and +VCC2 pins, and –V_{CC} is the voltage applied at the –VCC1 and –VCC2 pins

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, $+V_{CC} – (–V_{CC})$		16.2	V
	Input/output	$(–V_{CC}) – 0.5$	$(+V_{CC}) + 0.5$	
	Differential input voltage (IN+ – IN–)		±8	
Current	Continuous input current (IN+, IN–, VMID_IN, VIN+, VIN–)(2)		±10	mA
	Continuous output current(2)		±30	
Temperature	Operating, T_A	–55	105	°C
	Junction, T_J	–45	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$+V_{CC}$	Positive supply voltage	4	6	7.9	V
$–V_{CC}$	Negative supply voltage	–4	–6	–7.9	V
T_A	Operating free-air temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS3217 RGV (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4	°C/W

(1) Thermal impedance reported with backside thermal pad soldered to heat spreading plane. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: D2S

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, A_V = 2 V/V, 25-Ω source impedance, input common-mode voltage (V_{IC}) = 0.25 V, external OPS input selected (PATHSEL ≥ 1.3 V), V_{REF} = GND, R_{LOAD} = 100 Ω, and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
AC PERFORMANCE (Power Stage Disabled: DISABLE pin ≥ 1.3 V) (2)						
Small-signal bandwidth (SSBW)	V_{OUT} = 250 mV_{PP}, peaking < 1.0 dB		800		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 2 V_{PP}		500		MHz	C
Bandwidth for 0.2-dB flatness	V_{OUT} = 2 V_{PP}		250		MHz	C
Slew rate (3)	V_{OUT} = 4-V step		2500		V/µs	C
Over- and undershoot	Input t_r = 1 ns, V_{OUT} = 2-V step		6%			C
Rise and fall time	Input t_r = 1 ns, V_{OUT} = 2-V step		1.2		ns	C
Settling time to 0.1%	Input t_r = 1 ns, V_{OUT} = 2-V step		5		ns	C
2nd-order harmonic distortion (HD2)	f = 20 MHz, V_{OUT}= 2 V_{PP}		–68		dBc	C
3rd-order harmonic distortion (HD3)	f = 20 MHz, V_{OUT}= 2 V_{PP}		–86		dBc	C
Output voltage noise	f > 200 kHz		18		nV/√Hz	C
Input current noise (each input)	f > 200 kHz		2.0		pA/√Hz	C
Output impedance	f = 20 MHz		0.8		Ω	C
DC PERFORMANCE (2)						
Differential to single-ended gain	±100-mV output	1.975	2.0	2.025	V/V	A
Differential to single-ended gain drift	T_J = –40°C to +125°C		–20	–24	ppm/°C	B
VREF input pin gain	Differential inputs = 0 V, V_{REF} = ±100 mV	0.985	1.0	1.015	V/V	A
VREF input pin gain drift	T_J = –40°C to +125°C		–70	–95	ppm/°C	B
Output offset voltage	T_J = 25°C	–35	±8	35	mV	A
	T_J = 0°C to 70°C	–43		40	mV	B
	T_J = –40°C to +125°C	–54		47	mV	B
Output offset voltage drift	T_J = –40°C to +125°C	-40	–115	–190	µV/°C	B
Input bias current – each input (4)	T_J = 25°C	–4	±2	4	µA	A
	T_J = 0°C to 70°C	–4.2		4.2	µA	B
	T_J = –40°C to +125°C	–4.3		4.5	µA	B
Input bias current drift	T_J = –40°C to +125°C	1	3	5	nA/°C	B
Input offset current	T_J = 25°C	–400	±50	400	nA	A
	T_J = 0°C to 70°C	–700		940	nA	B
	T_J = –40°C to +125°C	–1180		1600	nA	B
Input offset current drift	T_J = –40°C to +125°C	–12	±1	12	nA/°C	B
INPUTS (5)						
Common-mode input negative supply headroom	T_J = 25°C		1.8	1.9	V	A
	T_J = –40°C to +85°C			2.0	V	B
Common-mode input positive supply headroom	T_J = 25°C		1.3	1.4	V	A
	T_J = –40°C to +125°C			1.5	V	B
Common-mode rejection ratio (CMRR)	–1 V ≤ V_{IC} ≤ 3 V	47	55		dB	A
Input impedance differential mode	V_{CM} = 0 V		50 || 2.4		kΩ || pF	C
Input impedance common mode	V_{CM} = 0 V		90 || 2.4		kΩ || pF	C

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A≈ T_J≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information. DC limits tested with no self-heating. Add internal self heating to T_A for T_J.
(2) Output measured at pin 6.
(3) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (Vpeak / √2) × 2π × $f_{–3dB}$.
(4) Currents out of pin treated as a positive polarity.
(5) Applies to input pins 2 (IN+) and 3 (IN–).

Electrical Characteristics: D2S (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, A_V = 2 V/V, 25-Ω source impedance, input common-mode voltage (V_{IC}) = 0.25 V, external OPS input selected (PATHSEL ≥ 1.3 V), V_{REF} = GND, R_{LOAD} = 100 Ω, and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
OUTPUT (6)						
Output voltage headroom to either supply	T_J = 25°C	1.1	1.35	1.55	V	A
	T_J = –40°C to +125°C				V	B
Output current drive	T_J = 25°C, ±1.16 V_{PP}, R_{LOAD} = 20 Ω	50	70		mA	A
DC Output Impedance	Load current = ±20 mA		0.2	0.45	Ω	A
POWER SUPPLY (D2S Stage + Midsupply Buffer Only; Output Power Stage Disabled: DISABLE pin ≥ 1.3 V)						
Bipolar-supply operating range		±4.0	±6.0	±7.9	V	A
Single-supply operating range		8	12	15.8	V	B
Supply current	±6-V supplies	31	34	36	mA	A
Supply current temperature coefficient			7		µA/°C	C

(6) Output measured at pin 6.

7.6 Electrical Characteristics: OPS

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, D2S input common-mode voltage (V_{IC}) = 0.25 V, V_{REF} = GND, R_F = 249 Ω(1), R_G = 162 Ω, A_V = 2.5 V/V, OPS R_{LOAD} = 100 Ω, OPS enabled (DISABLE ≤ 0.7 V or floated), external OPS input selected (PATHSEL ≥ 1.3 V), and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (2)
AC PERFORMANCE (3)						
Small-signal bandwidth (SSBW)	V_{OUT} = 100 mV_{PP}, peaking < 1.0 dB		950		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 5 V_{PP}		500		MHz	C
Bandwidth for 0.2-dB flatness	V_{OUT} = 5 V_{PP}		110		MHz	C
Slew rate(4)	V_{OUT} = 5-V step		5500		V/µs	C
Over- and undershoot	Input t_r = 1 ns, V_{OUT} = 5-V step		8%			C
Rise and fall time	Input t_r = 1 ns, V_{OUT} = 5-V step		1.1		ns	C
Settling time to 0.1%	Input t_r = 1 ns, V_{OUT} = 5-V step		5		ns	C
2nd-order harmonic distortion (HD2)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–69		dBc	C
3rd-order harmonic distortion (HD3)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–73		dBc	C
Noninverting input voltage noise	f > 200 kHz		3.2		nV/√Hz	C
Noninverting input current noise	f > 200 kHz		2.8		pA/√Hz	C
Inverting input current noise	f > 200 kHz		30		pA/√Hz	C
Closed-loop ac output impedance	f = 20 MHz		0.40		Ω	C
DC PERFORMANCE (3)						
Open-loop transimpedance gain(1)	V_{OUT} = ±1 V, R_{LOAD}= 500-Ω	600	1200		kΩ	A
Closed-loop gain	0.1% external R_F and R_G resistors	2.495	2.515	2.53	V/V	A
INPUT						
External input offset voltage (pin 9 to pin12)	T_J = 25°C	–12	±2.5	12	mV	A
	T_J = 0°C to 70°C	–20		17	mV	B
	T_J = –40°C to +125°C	–31		24	mV	B
External input offset voltage drift (pin 9 to pin12)	T_J = –40°C to +125°C	-45	–115	–190	µV/°C	B
Internal input offset voltage (pin 6 to pin 12)	T_J = 25°C	–12	±2.5	12	mV	A
	T_J = 0°C to 70°C	–23		18	mV	B
	T_J = –40°C to +125°C	–35		27	mV	B
Internal input offset voltage drift (pin 6 to pin 12)	T_J = –40°C to +125°C	–70	–150	–235	µV/°C	B
External to internal input offset voltage match	T_J = 25°C		±1.2		mV	C
External noninverting input bias current (pin 9)(5)	T_J = 25°C	–5	±5	15	µA	A
	T_J = 0°C to 70°C	–5.2		15.4	µA	B
	T_J = –40°C to +125°C	–5.6		15.9	µA	B
External noninverting input bias current drift (pin 9)	T_J = –40°C to +125°C	–3	3	9	nA/°C	B
Inverting input bias current – either input selected(5)	T_J = 25°C	–40	±5	40	µA	A
	T_J = 0°C to 70°C	–51		46	µA	B
	T_J = –40°C to +125°C	–65		56	µA	B
Inverting input bias current drift	T_J = –40°C to +125°C	–250	–120	–10	nA/°C	B

(1) Output power stage includes an internal 18.5-kΩ feedback resistor. This internal resistor, in parallel with an external 249-Ω R_F and 162-Ω R_G, results in a gain of 2.5 V/V after including a nominal gain loss of 0.9935 V/V due to the input buffer and loop-gain effects.
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A≈ T_J≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information. DC limits tested with no self-heating. Add internal self heating to T_A for T_J.
(3) Output measured at pin 11.
(4) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (Vpeak / √2) × 2π × $f_{–3dB}$.
(5) Currents out of pin treated as a positive polarity.

Electrical Characteristics: OPS (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, D2S input common-mode voltage (V_{IC}) = 0.25 V, V_{REF} = GND, R_F = 249 Ω(1), R_G = 162 Ω, A_V = 2.5 V/V, OPS R_{LOAD} = 100 Ω, OPS enabled (DISABLE ≤ 0.7 V or floated), external OPS input selected (PATHSEL ≥ 1.3 V), and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (2)
Input headroom to either supply	T_J = 25°C		2.6	3.0	V	A
Common-mode rejection ratio (CMRR)		47	49		dB	A
Noninverting input resistance		17.6	18.5	22.4	kΩ	A
Noninverting input capacitance			3.3		pF	C
Open-loop inverting input impedance			42		Ω	C
OUTPUT(6)						
Output voltage headroom to either supply	R_{LOAD} = 500 Ω	1.1	1.3	1.4	V	A
Linear output current	T_J = 25°C, ±2.5 V into 26-Ω R_{LOAD}	95	120		mA	A
Peak output current	0-V output, R_{LOAD} < 0.2 Ω	135	170		mA	A
DC output impedance	0-V output, load current = ±40 mA		0.05	0.10	Ω	A
Internal R_F		17.6	18.5	22.4	kΩ	A
PATHSEL (Pin 4; Logic Reference = Pin 7 = GND)						
Input low logic level	Internal path selected	0.7	0.9		V	A
Input high logic level	External input selected at VIN (pin 9)		0.9	1.3	V	A
Input voltage range		–0.5		$+V_{CC}$	V	A
PATHSEL voltage when floated	Internal input from D2S selected	0	20	40	mV	A
Input pin bias current(7)	0-V input	0		4	µA	A
	3.3-V input	–150		–250	µA	A
Input pin impedance			18 || 1.5		kΩ || pF	C
Switching time	To 1% of final value		80		ns	C
Input switching glitch	Both inputs at GND		50		mV	C
Deselected input dc isolation	± 2-V input	70	80		dB	A
Deselected input ac isolation	2 V_{PP}, at 20-MHz input	55	65		dB	C
DISABLE (Pin 10; Logic Reference = Pin 7 = GND)						
Input low logic level		0.7	0.9		V	A
Input high logic level			0.9	1.3	V	A
Shutdown control voltage range		–0.5		$+V_{CC}$	V	B
Shutdown voltage when floated	Output stage enabled	0	20	40	mV	A
Input pin bias current(7)	0-V input	0		4	µA	A
	3.3-V input	–150		–250	µA	A
Input pin impedance			18 || 1.5		kΩ || pF	C
Switching time (turn on or off)	To 10% of final value		200		ns	C
Shutdown dc isolation (either input)	±2-V input	70	80		dB	A
Shutdown ac isolation (either input)	2 V_{PP} at 20-MHz input	55	65		dB	C
POWER SUPPLY						
Bipolar-supply operating range		±4.0	±6.0	±7.9	V	A
Single-supply operating range		8	12	15.8	V	B
Supply current (OPS only)	±6-V supplies	18.5	21	24.5	mA	A
Disabled supply current in OPS	±6-V supplies	2.0	2.4	3.0	mA	C
Logic reference current at pin 7(7)	Pins 4, 7, and 10 held at 0 V	200	280	380	µA	A

(6) Output measured at pin 11.
(7) Currents out of pin treated as a positive polarity.

7.7 Electrical Characteristics: D2S + OPS

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, D2S input V_{IC} = 0.25 V, Internal path selected to OPS (PATHSEL ≤ 0.7 V or floated), V_{REF} = GND, combined A_V = 5 V/V, D2S R_{LOAD}= 200 Ω, R_F = 249 Ω(1), R_G = 162 Ω (OPS A_V = 2.5 V/V), OPS enabled (DISABLE ≤ 0.7 V or floated), OPS R_{LOAD} = 100 Ω, and T_J ≈ 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (2)
AC PERFORMANCE (3)						
Small-signal bandwidth (SSBW)	V_{OUT} = 100 mV_{PP}, peaking < 1.5 dB		800		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 5 V_{PP}		500		MHz	C
Bandwidth for 0.2-dB flatness	V_{OUT} = 2 V_{PP}		100		MHz	C
Slew rate(4)	V_{OUT} = 8-V step		5000		V/µs	C
Over- and undershoot	Input t_r = 1 ns, V_{OUT} = 5-V step		8%			C
Rise and fall time	Input t_r = 1 ns, V_{OUT} = 5-V step		1.1		ns	C
Settling time to 0.1%	Input t_r = 1 ns, V_{OUT} = 5-V step		7		ns	C
2nd-order harmonic distortion (HD2)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–60		dBc	C
3rd-order harmonic distortion (HD3)	f = 20 MHz, V_{OUT}= 5 V_{PP}		–75		dBc	C
Output voltage noise	f > 200 kHz		45		nV/√Hz	C
DC PERFORMANCE (3)						
Total gain D2S to OPS output(1)	0.1% tolerance, dc, ±100-mV output test	4.92	5.02	5.12	V/V	A
POWER SUPPLY (Combined D2S, OPS, and Midscale Reference Buffer)						
Bipolar-supply operating range		±4.0	±6.0	±7.9	V	A
Single-supply operating range		8	12	15.8	V	B
Supply current	±6-V supplies	51	54	57	mA	A
Supply current temperature coefficient			10		µA/°C	C

(1) Output power stage includes an internal 18.5-kΩ feedback resistor. This internal resistor, in parallel with an external 249-Ω R_F and 162-Ω R_G, results in a gain of 2.5 V/V after including a nominal gain loss of 0.9935 V/V due to the input buffer and loop-gain effects.
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at T_A≈ T_J≈ 25°C; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(3) Output measured at pin 11.
(4) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (Vpeak / √2) × 2π × $f_{–3dB}$.

7.8 Electrical Characteristics: Midscale (DC) Reference Buffer

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, R_{LOAD} = 150 Ω at pin 15, and $T_J \approx 25^{\circ}C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
AC PERFORMANCE (Output measured at pin 15)						
Small-signal bandwidth (SSBW)	V_{OUT} = 100 mV_{PP}		400		MHz	C
Large-signal bandwidth (LSBW)	V_{OUT} = 1 V_{PP}		110		MHz	C
Slew rate (2)	V_{OUT} = 4-V step		250		V/µs	C
Input voltage noise	f > 200 kHz		4.4		nV/√Hz	C
Input current noise	f > 200 kHz		2.3		pA/√Hz	C
AC output impedance	f = 20 MHz		1.0		Ω	C
DC AND I/O PERFORMANCE (R_S = 25 Ω, and output measured at pin 15, unless otherwise noted)						
Buffer gain	V_I = ±1 V, R_{LOAD} = 200 Ω	.9985	0.999	1.001	V/V	A
Buffer gain drift	T_J = –40°C to +125°C		–1.5	–2.0	ppm/°C	B
Output offset from midsupply	Input floating, pin 1 open	–120	30	70	mV	A
Output offset voltage	T_J = 25°C, input driven to 0 V from 0-Ω source	–1.0	4.0	15	mV	A
Input offset voltage drift	T_J = –40°C to +125°C, input driven to 0 V	–4	3	10	µV/°C	B
Input bias current (3)	T_J = 25°C	–15	±1	15	µA	A
Input bias current drift	T_J = –40°C to +125°C	–8	–2	3	nA/°C	B
Input/output headroom to either supply	T_J = 25°C, gain change < 1%		1.1	1.4	V	A
Input impedance	Internal 50-kΩ divider resistors to each supply		22 || 1.5		kΩ || pF	C
Linear output current into resistive load	±2.25 V into 36 Ω	40	65		mA	A
DC output impedance	Load current = ±30 mA		0.21		Ω	C

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at $T_A \approx T_J \approx 25°C$; over temperature limits by characterization and simulation. (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information.
(2) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: $(V_{PEAK} / \sqrt{2}) \times 2\pi \times f_{–3dB}$.
(3) Currents out of pin treated as a positive polarity.

7.9 Typical Characteristics: D2S + OPS

at $+V_{CC}$ = 6 V, $–V_{CC}$ = –6 V, 25-Ω D2S source impedance , V_{IC} = 0.25 V, Internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 200 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5 V/V, OPS On (DISABLE = GND), and OPS R_{LOAD} = 100 Ω at pin 11 (unless otherwise noted)

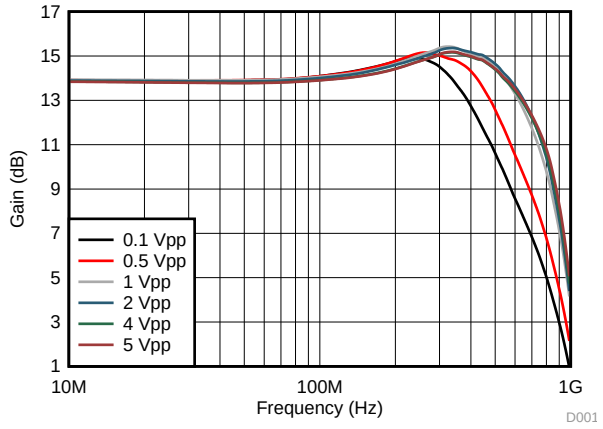


Figure 1. Frequency Response vs Output Voltage

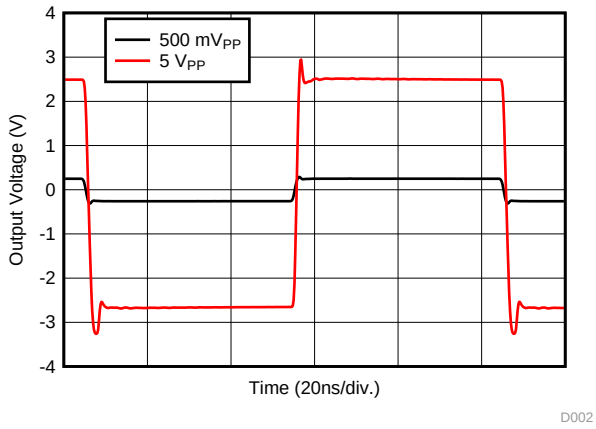


Figure 2. Small and Large Signal Step Response

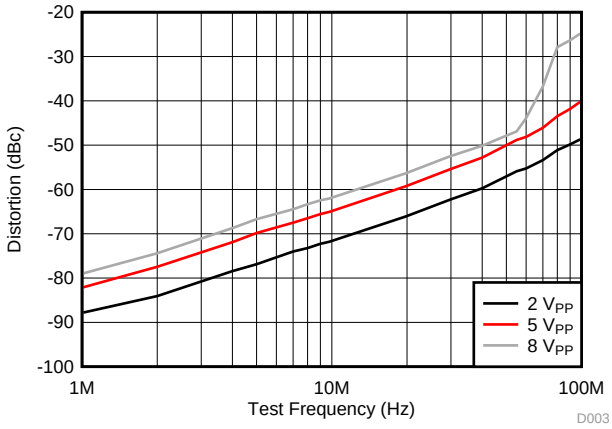


Figure 3. HD2 vs Frequency

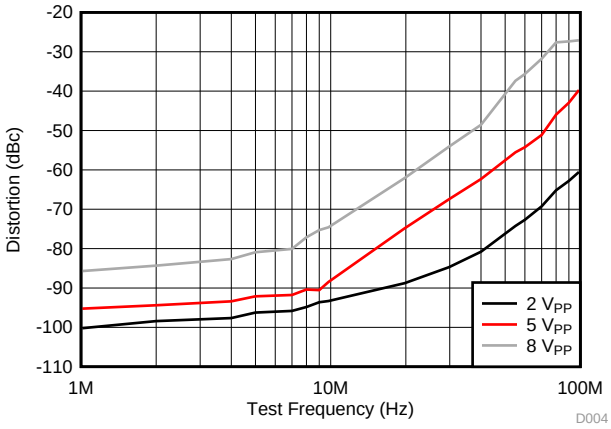
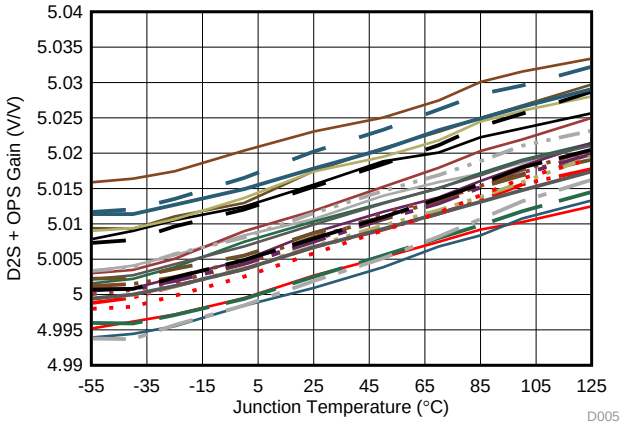
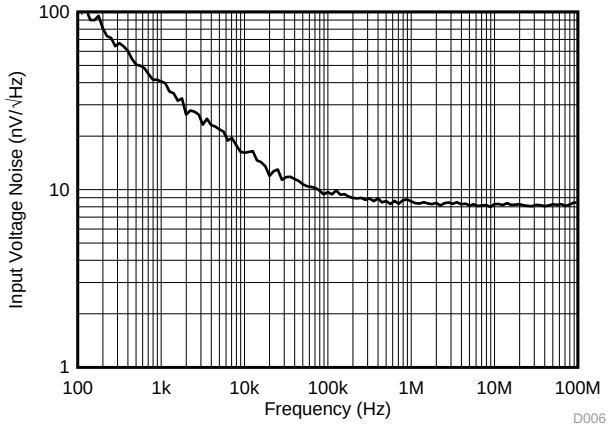


Figure 4. HD3 vs Frequency



26 units shown

Figure 5. Gain vs Temperature

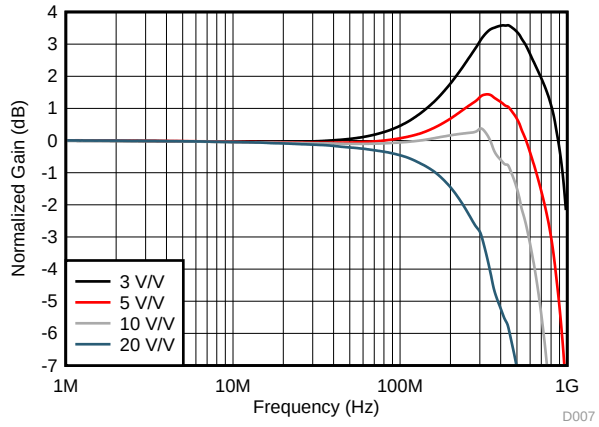


25-Ω source impedance on each D2S input

Figure 6. Input Referred Differential Noise

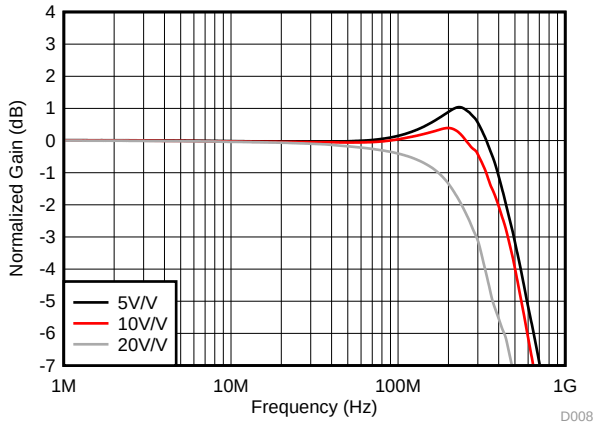
Typical Characteristics: D2S + OPS (continued)

at $+V_{CC}$ = 6 V, $-V_{CC}$ = –6 V, 25-Ω D2S source impedance , V_{IC} = 0.25 V, Internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 200 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5 V/V, OPS On (DISABLE = GND), and OPS R_{LOAD} = 100 Ω at pin 11 (unless otherwise noted)



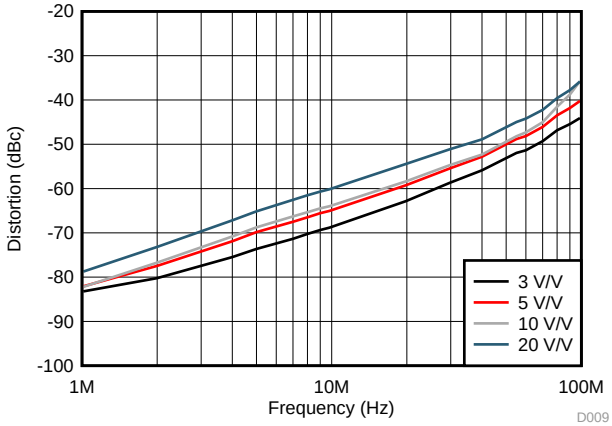
V_{OUT} = 500 mV_{PP}, see Table 2

Figure 7. Small-Signal Frequency Response vs Gain



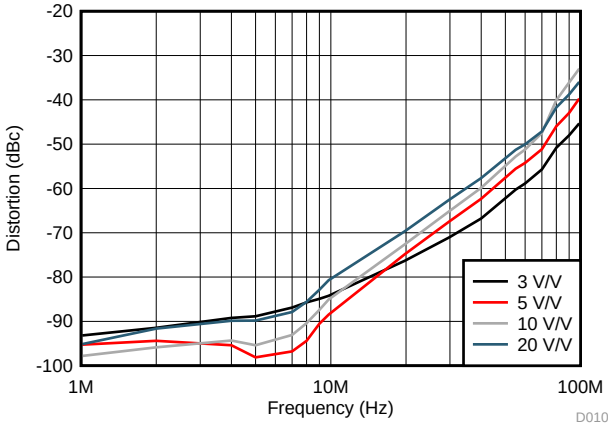
V_{OUT} = 5 V_{PP}, see Table 2

Figure 8. Large-Signal Frequency Response vs Gain



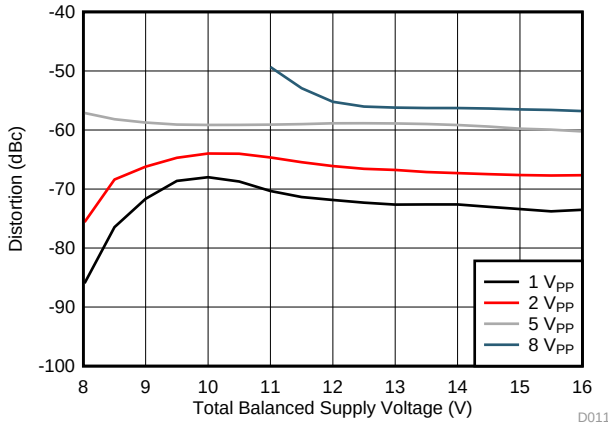
V_{OUT} = 5 V_{PP}

Figure 9. HD2 vs Gain



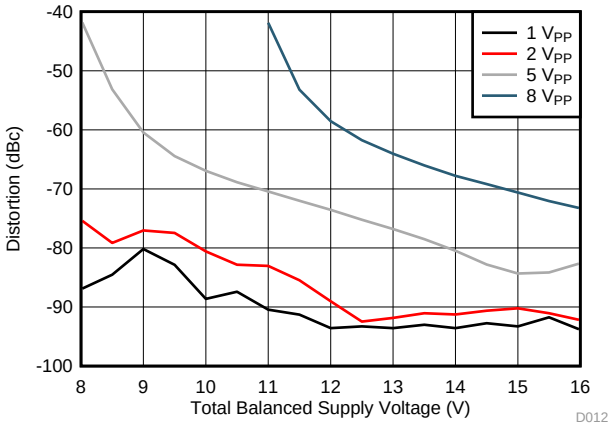
V_{OUT} = 5 V_{PP}

Figure 10. HD3 vs Gain



Test frequency = 20 MHz

Figure 11. HD2 vs Supply Voltage

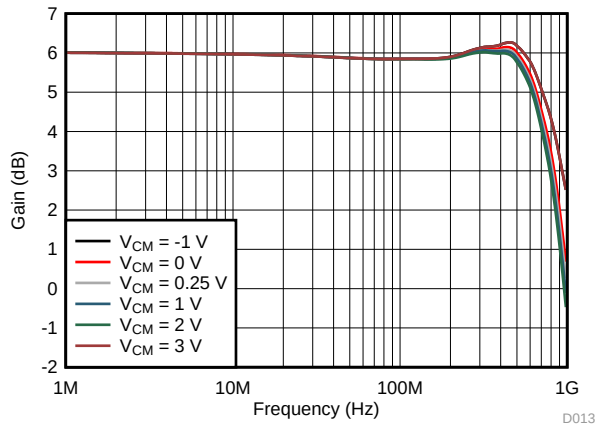


Test frequency = 20 MHz

Figure 12. HD3 vs Supply Voltage

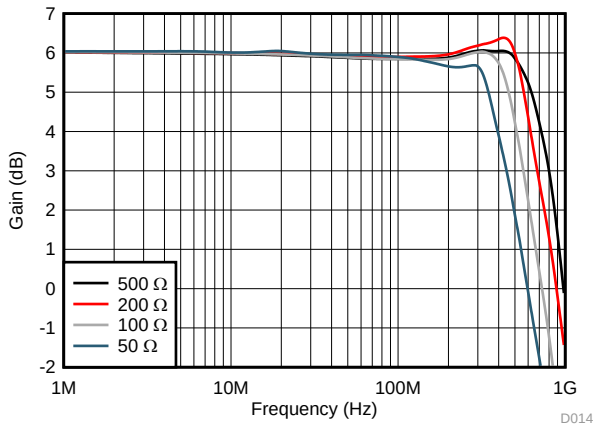
7.10 Typical Characteristics: D2S Only

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, fixed gain of 2 V/V, 25-Ω D2S source impedance, V_{IC} = 0.25 V, external path selected (PATHSEL = $+V_{CC}$), V_{REF} = GND, and D2S R_{LOAD} = 100 Ω at pin 6 (unless otherwise noted)



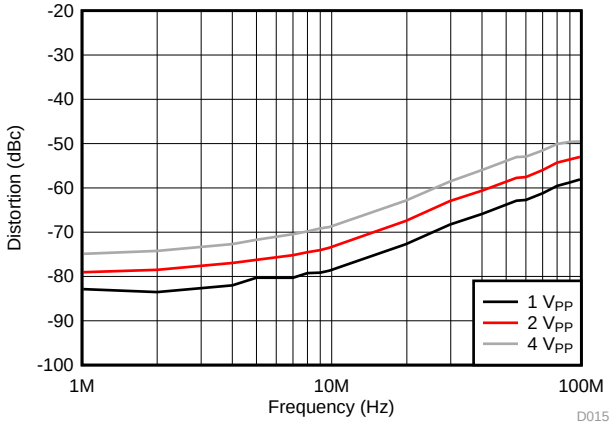
V_{OUT} = 250 mV_{PP}

Figure 13. Frequency Response vs Input Common-Mode Voltage



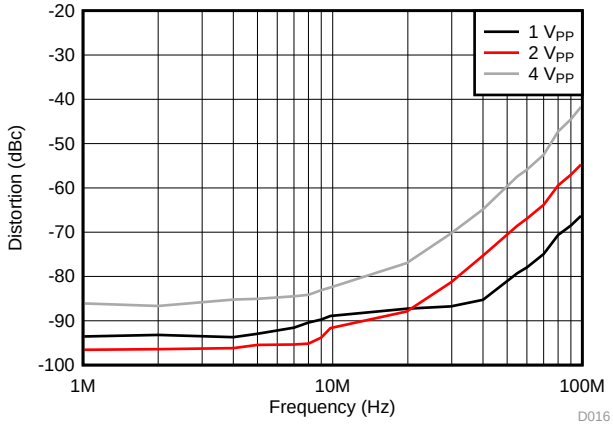
V_{OUT} = 2 V_{PP}

Figure 14. Frequency Response vs Load Resistance



R_{LOAD} = 200 Ω

Figure 15. HD2 vs Output Voltage



R_{LOAD} = 200 Ω

Figure 16. HD3 vs Output Voltage

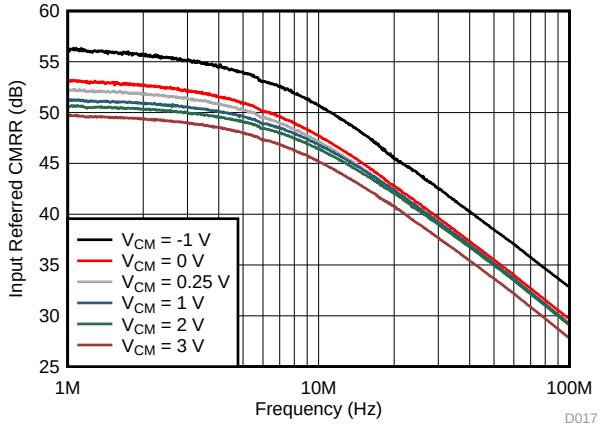


Figure 17. Common-Mode Rejection Ratio vs Input Common-Mode Voltage

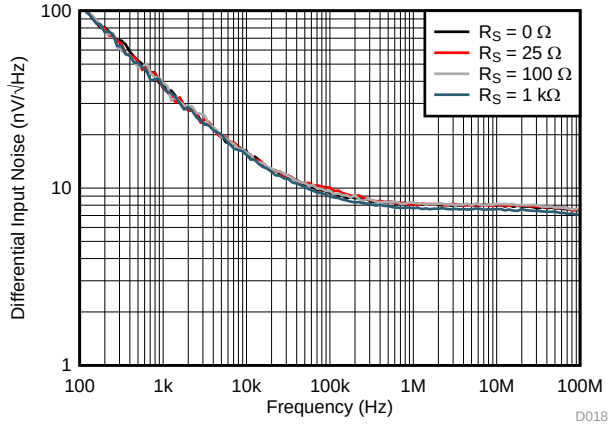
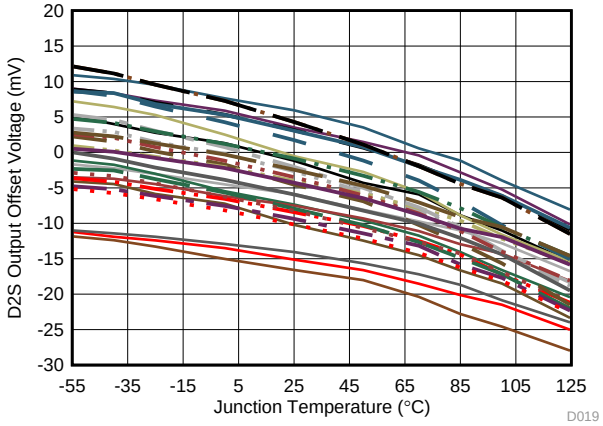


Figure 18. Differential Input Noise vs Source Impedance

Typical Characteristics: D2S Only (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, fixed gain of 2 V/V, 25-Ω D2S source impedance, V_{IC} = 0.25 V, external path selected (PATHSEL = $+V_{CC}$), V_{REF} = GND, and D2S R_{LOAD} = 100 Ω at pin 6 (unless otherwise noted)



30 units shown

Figure 19. Output DC Offset Voltage vs Die Temperature

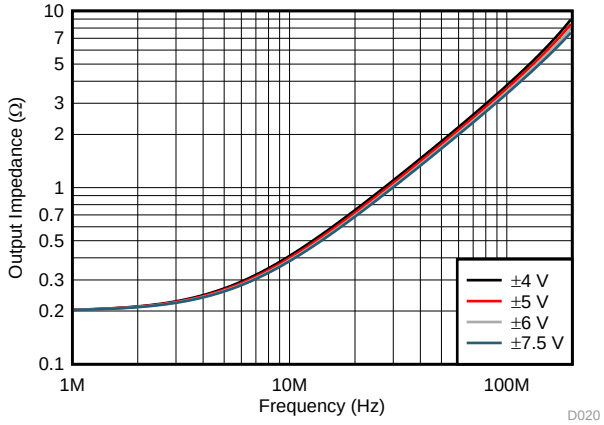
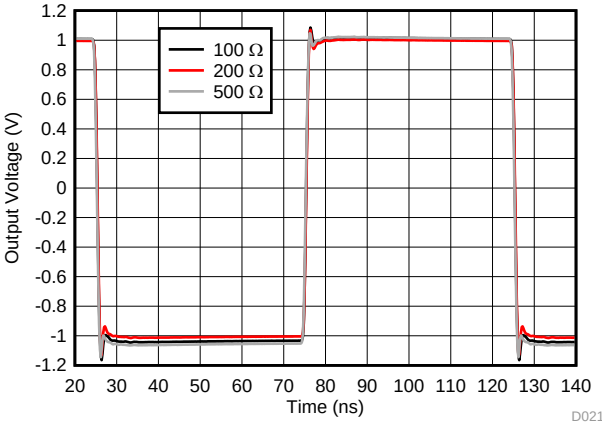
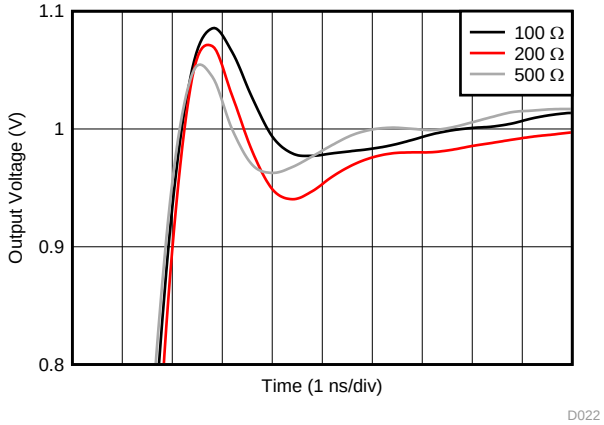


Figure 20. Output Impedance vs Supply Voltage



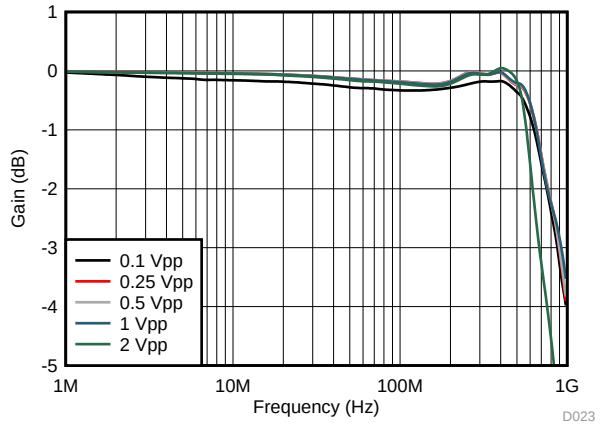
±1-V output pulse

Figure 21. Large-Signal Step Response vs Load Resistance



±1-V output pulse

Figure 22. Large-Signal Pulse Settling Response vs Load Resistance



25-Ω D2S source impedance on each input

Figure 23. VREF Input Pin Frequency Response

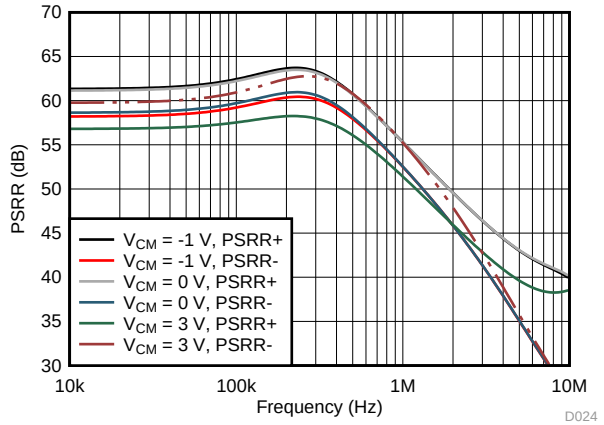
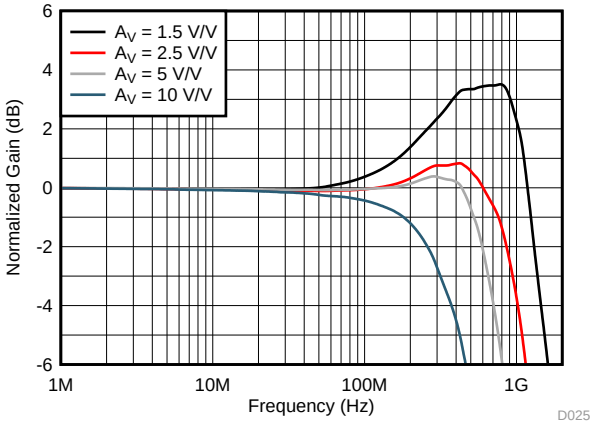


Figure 24. Simulated Power-Supply Rejection Ratio vs Input Common-Mode Voltage

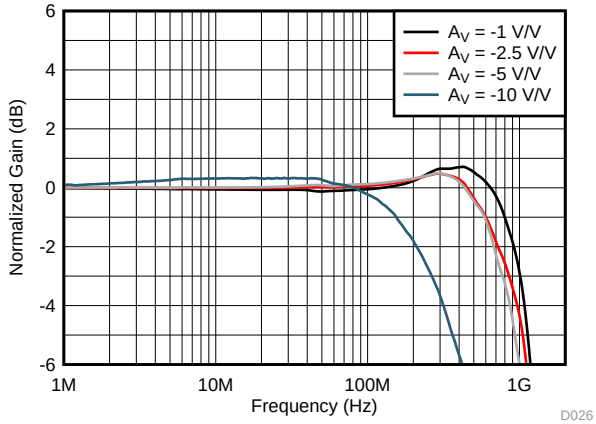
7.11 Typical Characteristics: OPS only

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), and external input path selected (PATHSEL = $+V_{CC}$) (unless otherwise noted)



V_{OUT} = 100 mV_{PP}, see Table 2 for R_F values vs gain

Figure 25. Frequency Response vs Noninverting Gain



V_{OUT} = 100 mV_{PP}, see Table 4 for R_F values vs gain

Figure 26. Frequency Response vs Inverting Gain

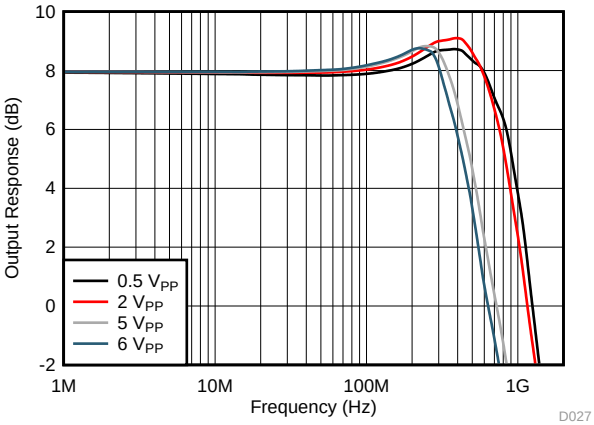
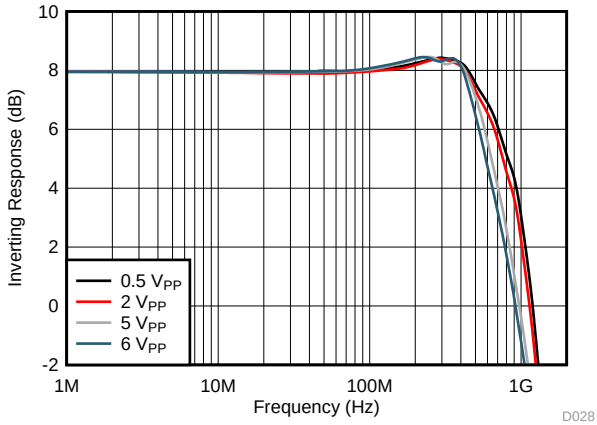


Figure 27. Noninverting Response vs Output Voltage



A_V = –2.5 V/V, see Table 4 for R_F value

Figure 28. Inverting Response vs Output Voltage

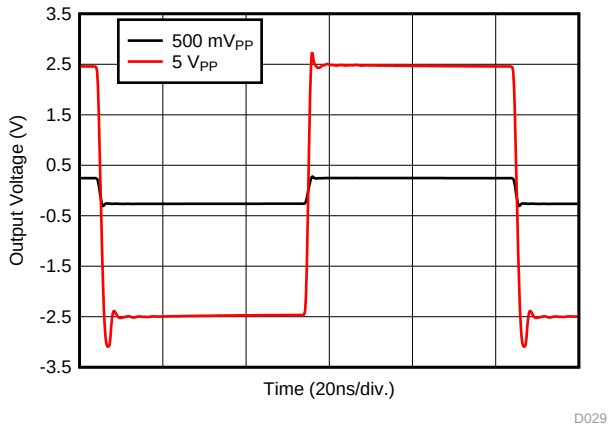
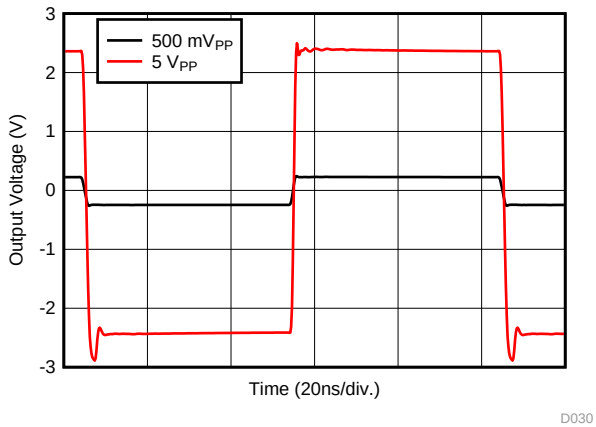


Figure 29. Noninverting Step Response



A_V = –2.5 V/V, see Table 4 for R_F value

Figure 30. Inverting Step Response

Typical Characteristics: OPS only (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), and external input path selected (PATHSEL = $+V_{CC}$) (unless otherwise noted)

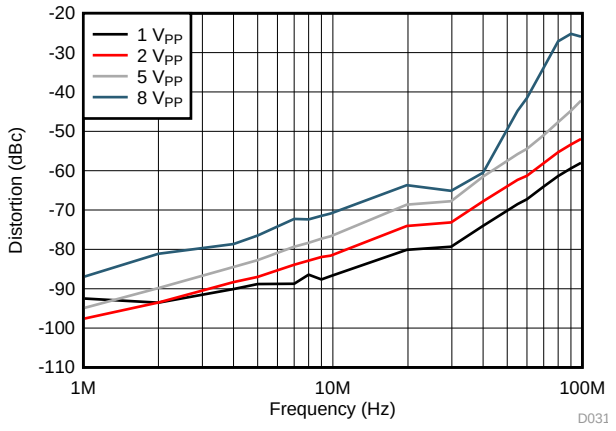


Figure 31. HD2 vs Output Voltage

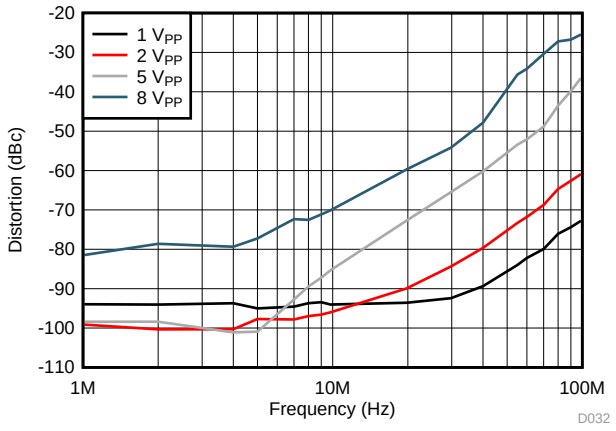
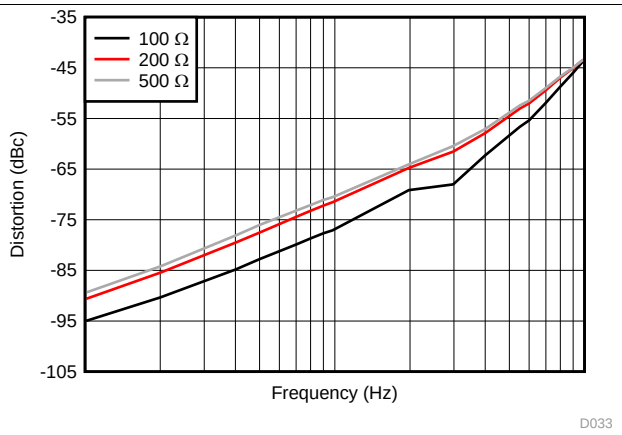
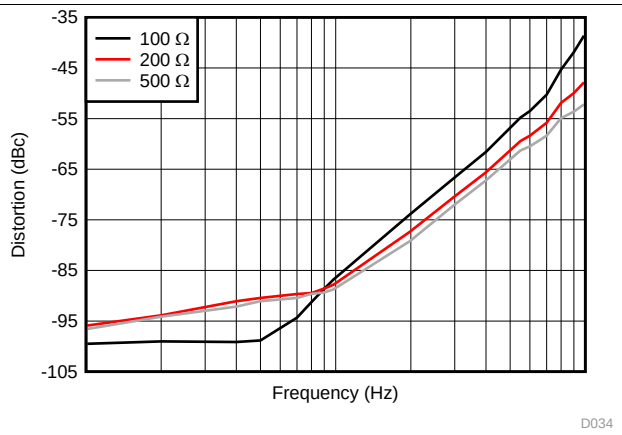


Figure 32. HD3 vs Output Voltage



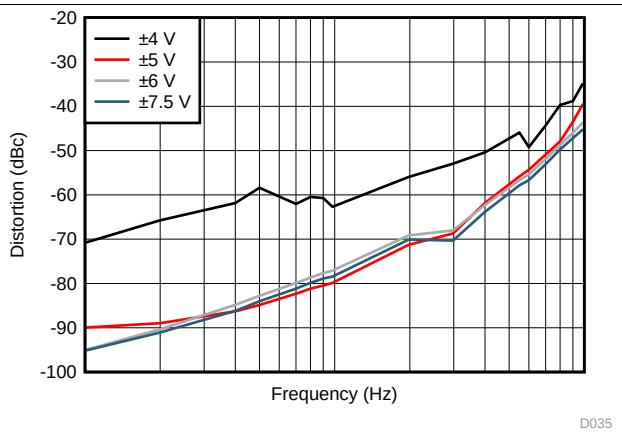
V_{OUT} = 5 V_{PP}

Figure 33. HD2 vs Load Resistance



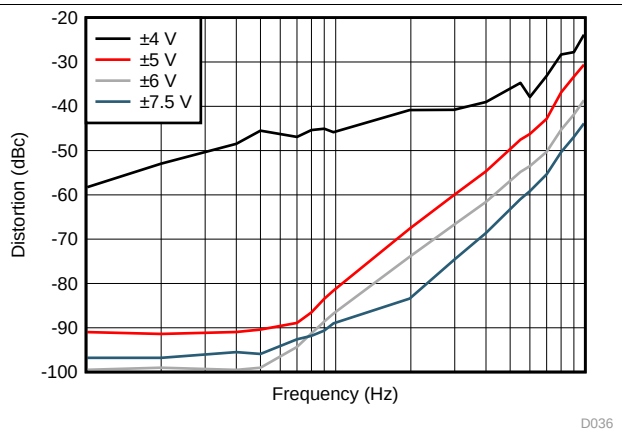
V_{OUT} = 5 V_{PP}

Figure 34. HD3 vs Load Resistance



V_{OUT} = 5 V_{PP}

Figure 35. HD2 vs Supply Voltage

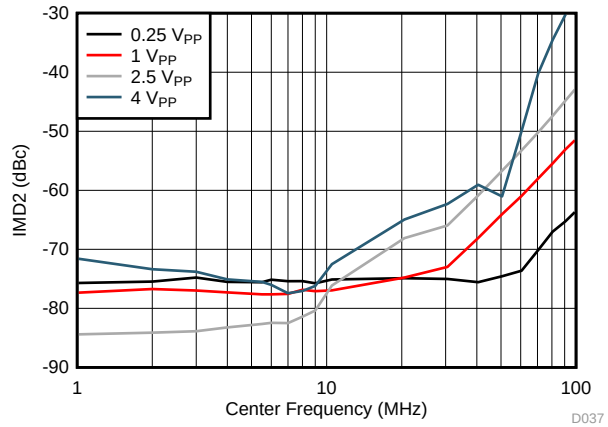


V_{OUT} = 5 V_{PP}

Figure 36. HD3 vs Supply Voltage

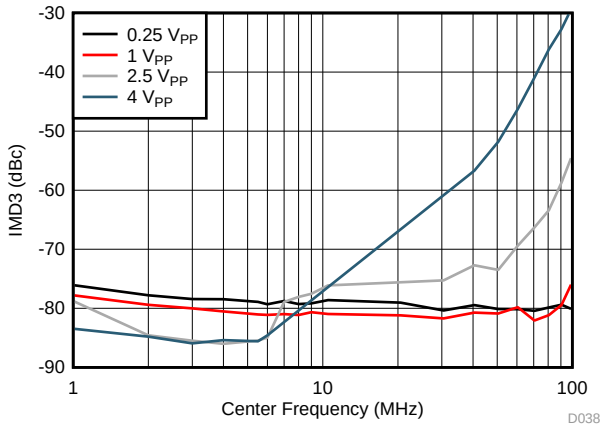
Typical Characteristics: OPS only (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), and external input path selected (PATHSEL = $+V_{CC}$) (unless otherwise noted)



±100-kHz tone separation, output voltage for each tone

Figure 37. IMD2 vs Output Voltage



±100-kHz tone separation, output voltage for each tone

Figure 38. IMD3 vs Output Voltage

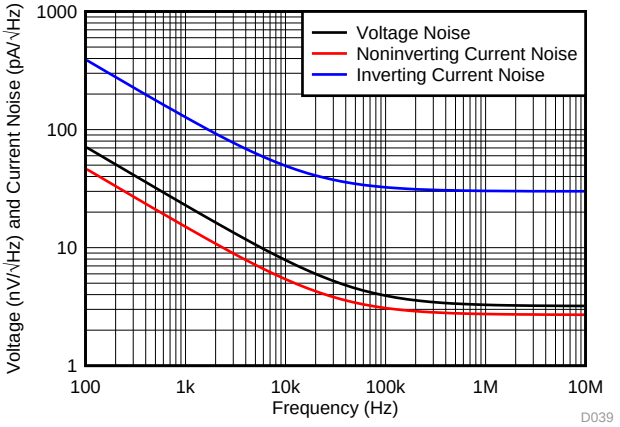
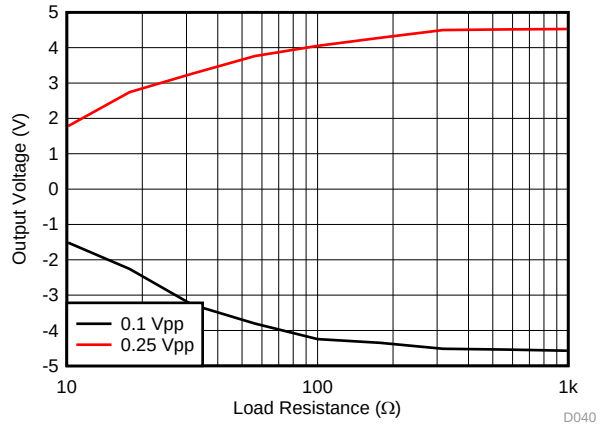
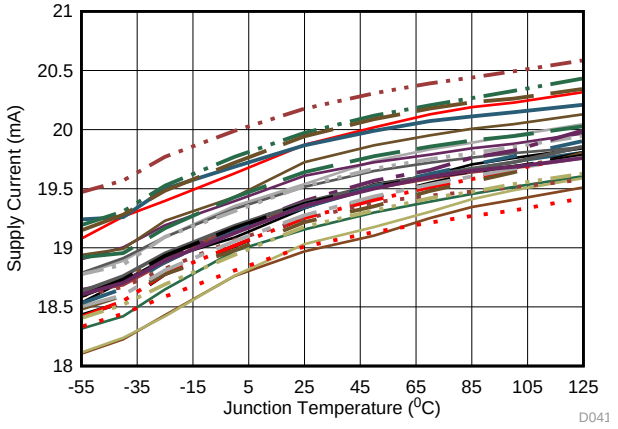


Figure 39. Input-Referred Spot Noise vs Frequency



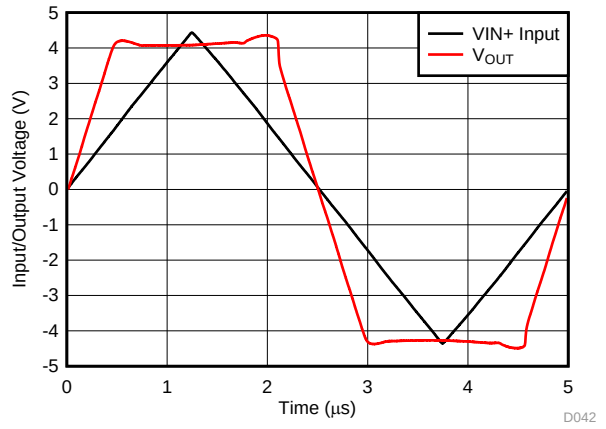
Output swing with better than 0.1% linearity

Figure 40. Linear Output Swing vs Load Resistance



30 units shown

Figure 41. Quiescent Supply Current vs Temperature

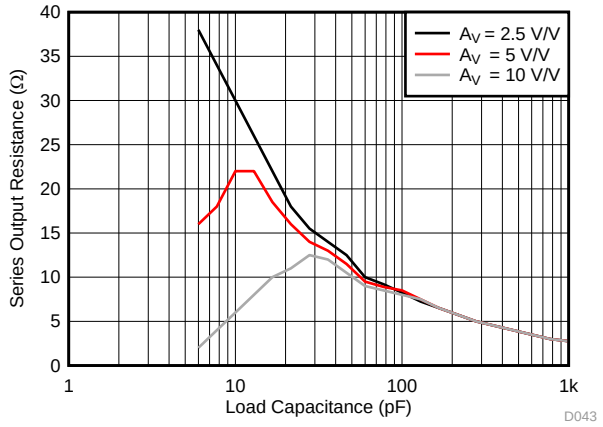


±4.5-V input triangular wave, OPS A_V = 2.5 V/V

Figure 42. Output Overdrive Response

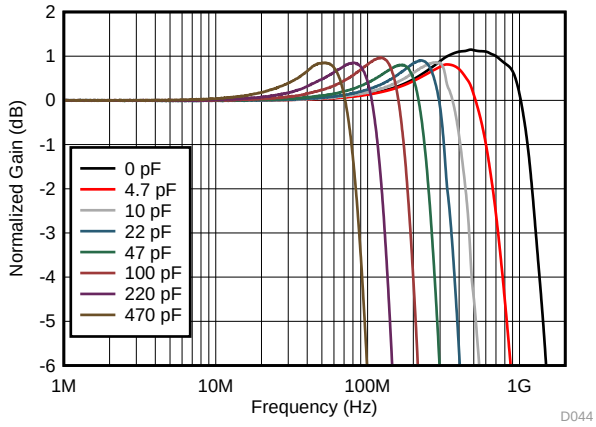
Typical Characteristics: OPS only (continued)

at $+V_{CC}$ = 6.0 V, $–V_{CC}$ = –6.0 V, 25-Ω D2S source impedance, V_{REF} = GND, R_F = 249 Ω, R_G = 162 Ω, OPS A_V = 2.5V/V, OPS R_{LOAD} = 100 Ω at pin 11, OPS enabled (DISABLE = GND), and external input path selected (PATHSEL = $+V_{CC}$) (unless otherwise noted)



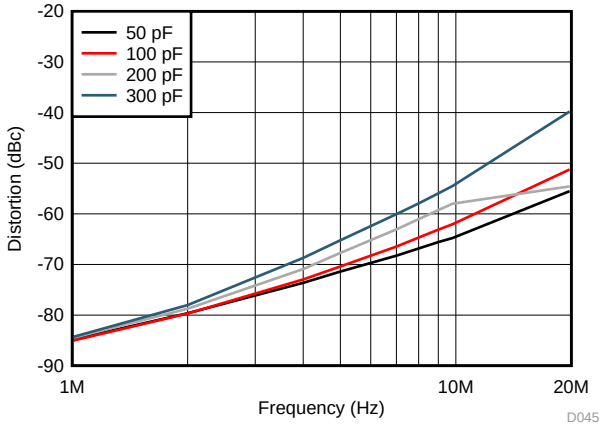
See Table 7 for R_F values vs OPS gain

Figure 43. Series Output Resistance vs Load Capacitance



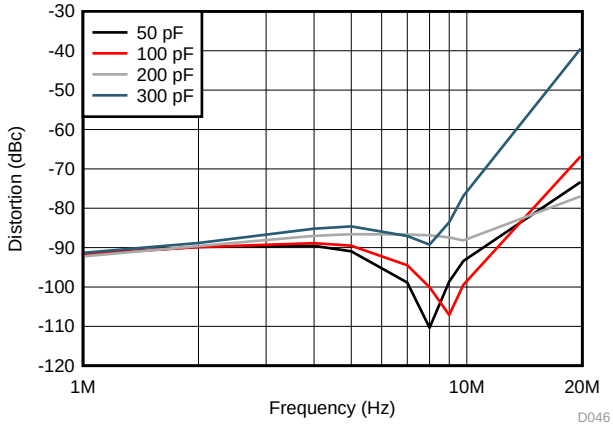
V_{OUT} = 500 mV_{PP}, see Figure 43 for R_S value

Figure 44. Frequency Response vs Load Capacitance



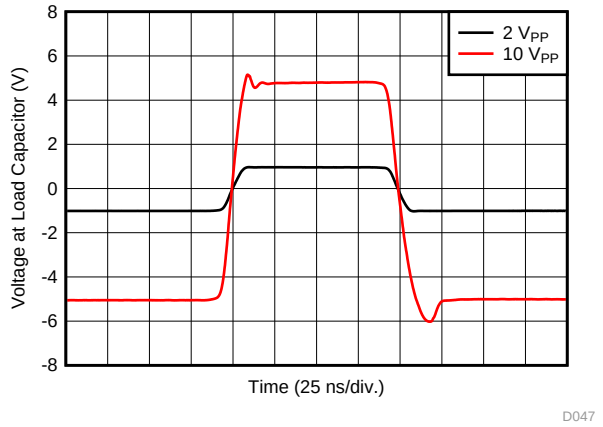
R_F = 205 Ω, A_V = 5 V/V, V_{OUT} = 10 V_{PP}, see Figure 43 for R_S value

Figure 45. HD2 vs Load Capacitance



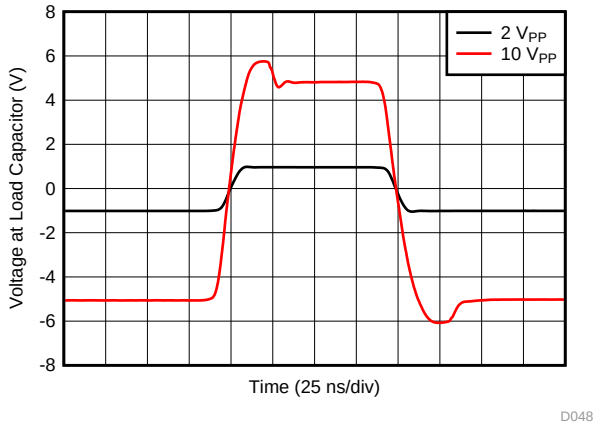
R_F = 205 Ω, A_V = 5 V/V, V_{OUT} = 10 V_{PP}, see Figure 43 for R_S value

Figure 46. HD3 vs Load Capacitance



C_{LOAD} = 200 pF, R_F = 205 Ω, A_V = 5 V/V, see Figure 43 for R_S value

Figure 47. Pulse Response



C_{LOAD} = 300 pF, R_F = 205 Ω, A_V = 5 V/V, see Figure 43 for R_S value.

Figure 48. Pulse Response

7.12 Typical Characteristics: Midscale (DC) Reference Buffer

at $+V_{CC}$ = 6.0 V, $-V_{CC}$ = –6.0 V, R_{LOAD} = 150 Ω, and $T_A \approx 25^{\circ}C$ (unless otherwise noted)

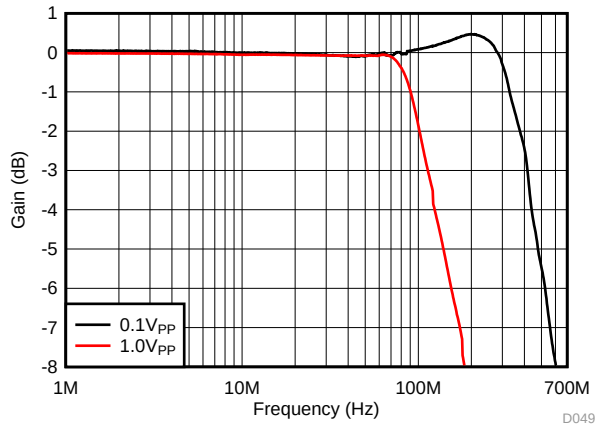


Figure 49. Frequency Response vs Output Voltage

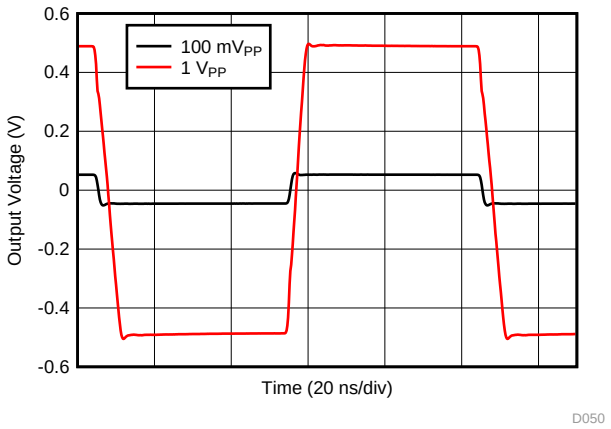


Figure 50. Step Response

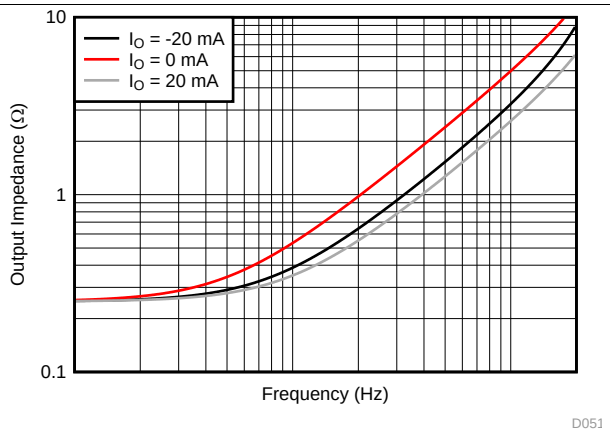


Figure 51. Buffer Output Impedance vs Load Current

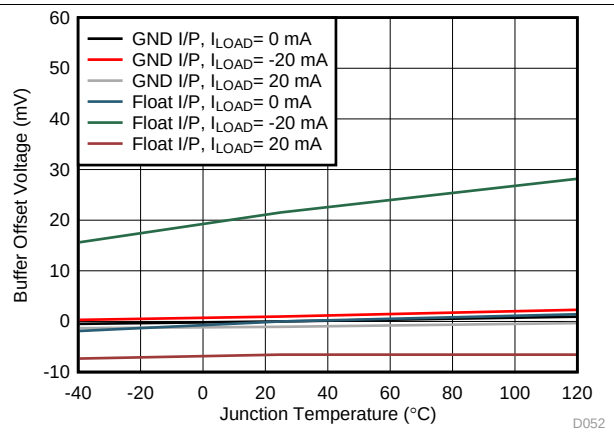
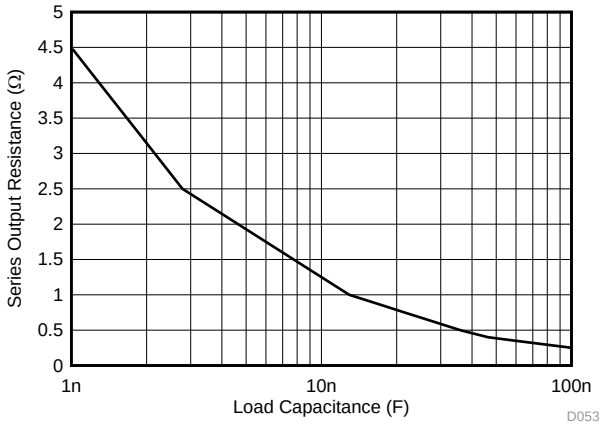
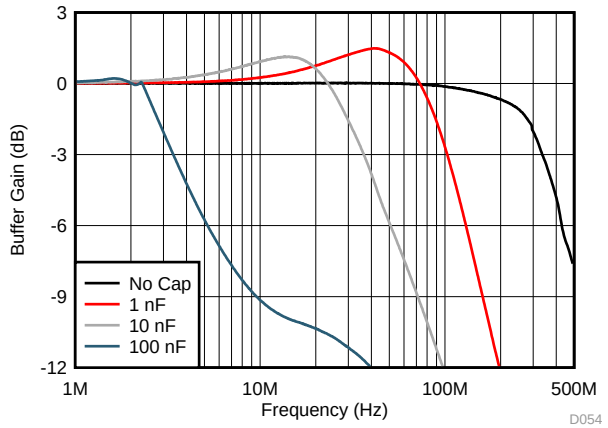


Figure 52. Buffer Output Offset vs Load Current (I_{LOAD})



R_{LOAD} = 150 Ω in parallel with C_{LOAD}, see the *Midscale Buffer R_{OUT} Versus C_{LOAD} Measurement* section for circuit setup

Figure 53. Series Output Resistance vs Capacitive Load

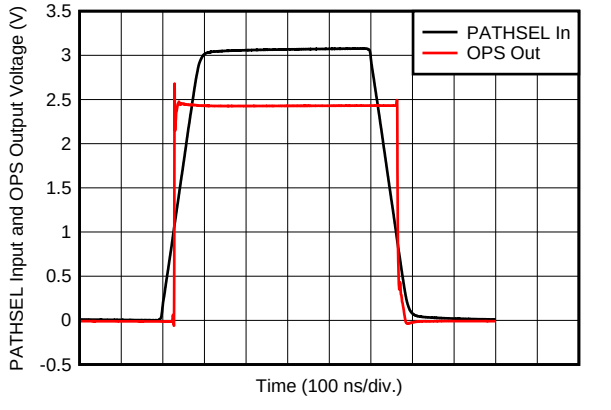


V_{OUT} = 100 mV_{PP}, R_{LOAD} = 150 Ω in parallel with C_{LOAD}, see *Midscale Buffer R_{OUT} Versus C_{LOAD} Measurement* for circuit setup

Figure 54. Frequency Response vs Capacitive Load

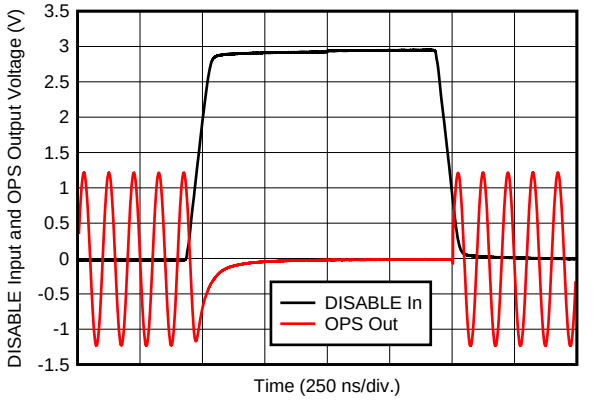
7.13 Typical Characteristics: Switching Performance

at $+V_{CC}$ = 6 V, $-V_{CC}$ = –6 V, 25-Ω D2S source impedance , V_{IC} = 0.25 V, Internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 200 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS On (DISABLE = GND), and OPS R_{LOAD} = 100 Ω at pin 11 (unless otherwise noted)



D2S Inputs: IN+ = IN– = GND, OPS input: VIN+ = 1 V

Figure 55. PATHSEL Switching Time



PATHSEL = high, OPS input: VIN+ = 1 V_{PP} , 10-MHz sine wave

Figure 56. OPS Enable and Disable Time

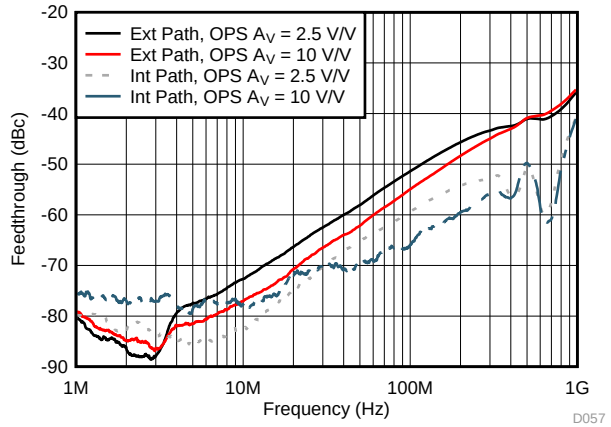


Figure 57. OPS Forward Feedthrough in Disable

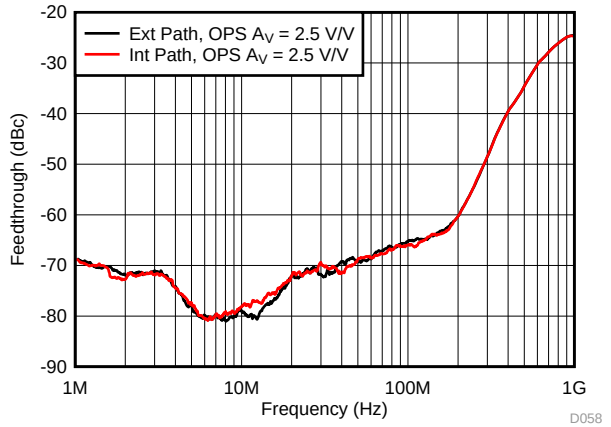
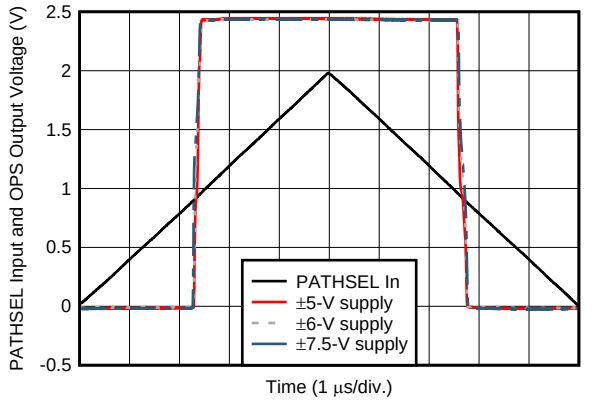
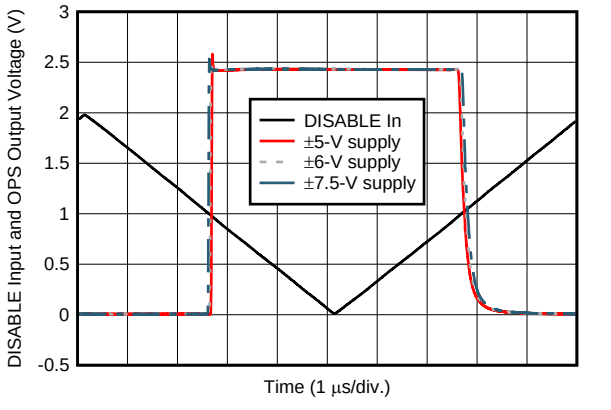


Figure 58. OPS Reverse Feedthrough in Disable



D2S inputs: IN+ = IN– = GND, OPS input: VIN+ = 1 V

Figure 59. PATHSEL Switching Threshold vs Power Supply

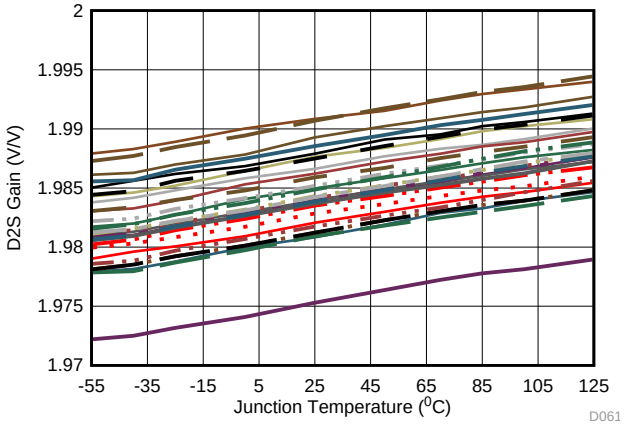


PATHSEL = high, OPS input: VIN+ = 1 V

Figure 60. OPS Shutdown Threshold vs Power Supply

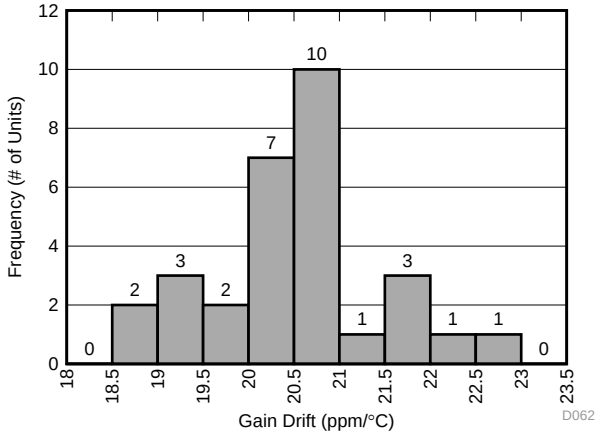
7.14 Typical Characteristics: Miscellaneous Performance

at $+V_{CC}$ = 6 V, $–V_{CC}$ = –6 V, 50-Ω D2S source impedance , V_{IC} = 0.25 V, internal path selected (PATHSEL = GND), V_{REF} = GND, D2S R_{LOAD} = 100 Ω at pin 6, R_F = 249 Ω, R_G = 162 Ω, OPS on (DISABLE = GND), and OPS R_{LOAD} = 100 Ω at pin 11 (unless otherwise noted)



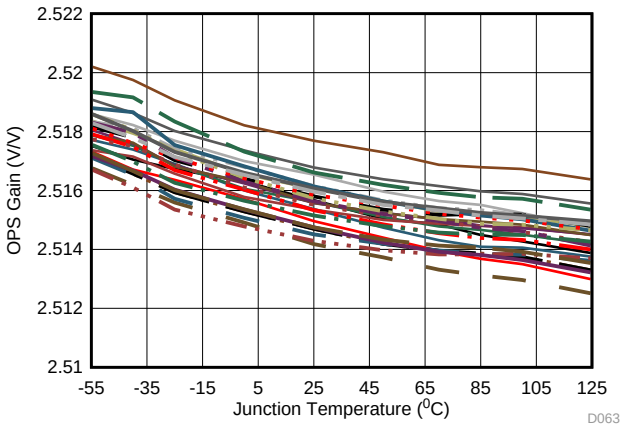
30 units shown

Figure 61. D2S Gain Over Temperature



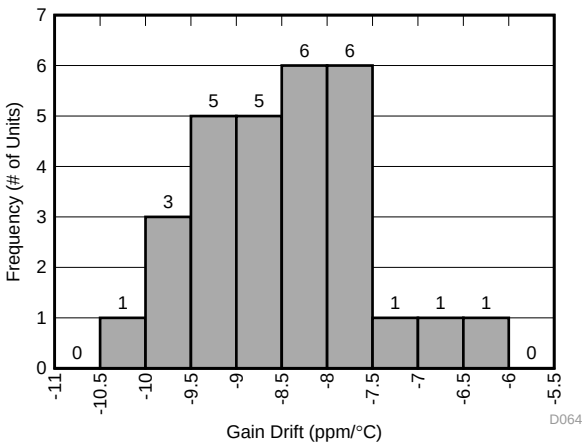
30 units from –40°C to +125°C

Figure 62. D2S Gain Drift Histogram



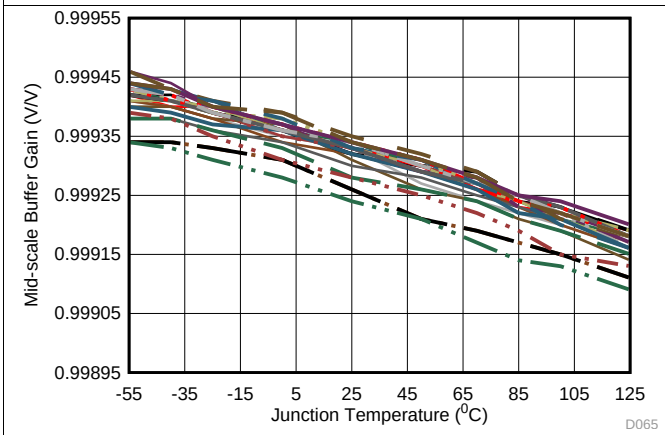
29 units shown

Figure 63. OPS Gain Over Temperature



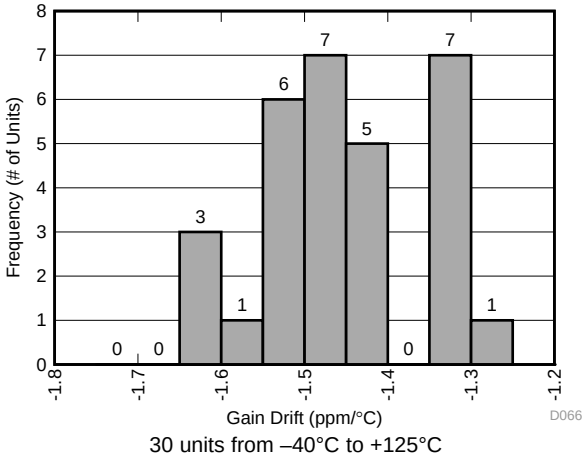
29 units from –40°C to +125°C

Figure 64. OPS Gain Drift Histogram



30 units shown

Figure 65. Midscale Buffer Gain Over Temperature



30 units from –40°C to +125°C

Figure 66. Midscale Buffer Gain Drift Histograms

8 Parameter Measurement Information

8.1 Overview

The THS3217 comprises three blocks of high-performance amplifiers. Each block requires both frequency-response and step-response characterization. The midscale buffer and OPS use standard, single-ended I/O test methods with network analyzers, pulse generators, and high-speed oscilloscopes. The differential to single-ended input stage (D2S) requires a wideband differential source for test purposes. All ac characterization tests were performed using the THS3217 evaluation module (EVM), the THS3217EVM, which offers many configuration options. For most of the D2S-only tests, the OPS was disabled. Figure 67 shows a typical configuration for an ac frequency-response test of the D2S.

The THS3217EVM includes unpopulated, optional, passive elements at the D2S inputs to implement a differential filter. These elements were not used in the D2S characterization and the two input pins were terminated to ground through 49.9-Ω resistors. DC test points are provided through 10-kΩ or 20-kΩ resistors on all THS3217 nodes. Figure 67 also shows the output network used to emulate a 200-Ω load resistance (R_{LOAD}) while presenting a 50-Ω source back to the D2S output pin. The R3 (= 169 Ω) and R4 (= 73.2 Ω) resistors combine with the 50-Ω network analyzer input impedance to present a 200-Ω load at VO1 (pin 6), The impedance presented from the input of the network analyzer back to the D2S output (VO1, pin 6) is 50-Ω. The 16.5-dB insertion loss intrinsic to this dc-coupled impedance network is removed from the characterization curves. The VREF pin was connected to GND for all the tests.

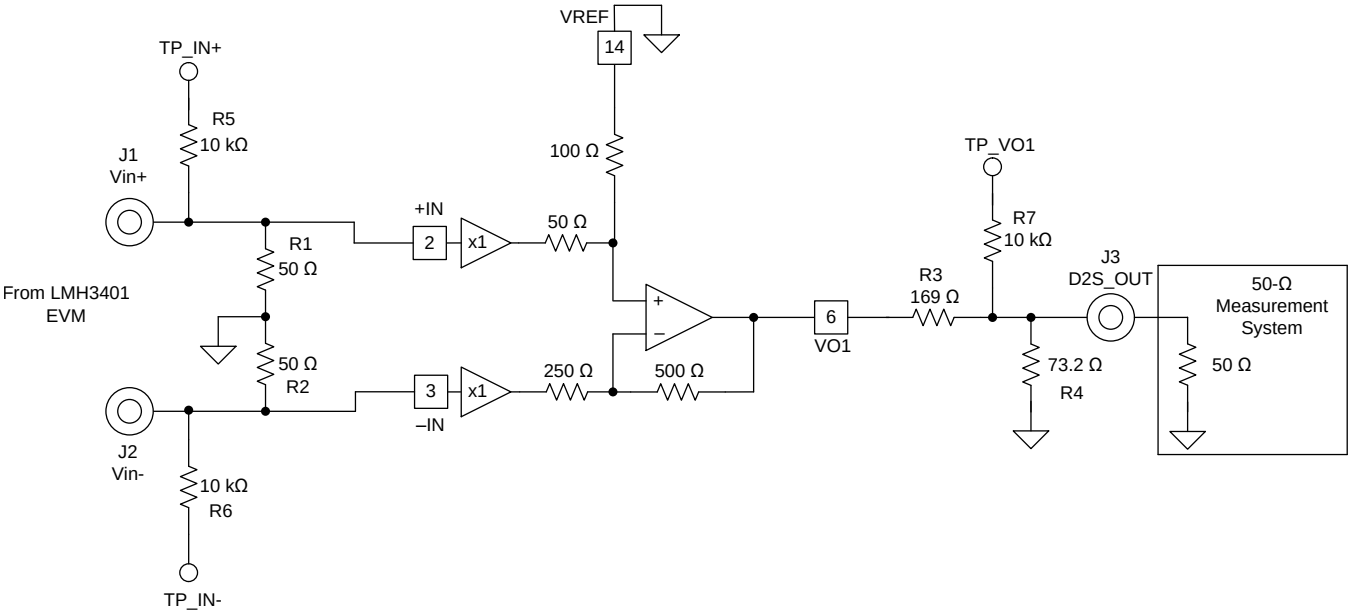


Figure 67. D2S Input and Output Interface Showing 50-Ω Differential Input, 200-Ω R_{LOAD} at VO1

8.2 Frequency Response Measurement

For D2S and full-signal path (D2S + OPS) characterization, the LMH3401, a very wideband, dc-coupled, single-ended to differential amplifier was used. The LMH3401EVM was used as an interface between a single-ended source and the differential input required by the D2S, shown in Figure 68. The LMH3401 provides an input impedance of 50 Ω, and converts a single-ended input to a differential output driving through 50-Ω outputs on each side to what is a 50-Ω termination at each input of the THS3217 D2S.

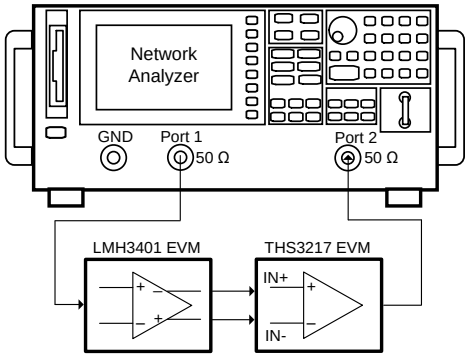


Figure 68. Frequency-Response Measurement: D2S and Full-Path (D2S + OPS) Circuit Configurations

The LMH3401 provides 7-GHz bandwidth with 0.1-dB flatness through 700 MHz. From the single-ended matched input (using active match through an internal 12.5-Ω resistor), the LMH3401 produces a differential output with 16-dB gain to the internal output pins. Building out to a 50-Ω source by adding external 40.2-Ω resistors on both differential outputs in series with the internal 10-Ω resistor, results in a net gain of 10 dB to the matched 50-Ω load on the THS3217EVM.

The maximum output swing test for the D2S stage is 4 V_{PP} (see Figure 15 and Figure 16). With a fixed gain of 2 V/V, the tests in Figure 15 and Figure 16 require a 2-V_{PP} differential input. In order to achieve the 2-V_{PP} differential swing at the D2S inputs, the LMH3401 internal outputs must drive a 4-V_{PP} differential signal around the V_{OCM} of the LMH3401. This LMH3401 single-to-differential preamplifier is normally operated with ±2.5-V supplies, and V_{OCM} set to ground. Under these conditions, the LMH3401 supports ±1.4 V on each internal output pin; well beyond the maximum required for THS3217 D2S characterization of ±1 V.

The output of the LMH3401EVM connects directly to the Vin+ (J1) and Vin- (J2) SMA connectors on the THS3217EVM, as shown in Figure 67. The physical spacing of the SMA connectors has been set to line up for a direct (no cabling) connection between the two different EVMs using SMA barrels. For THS3217 designs that must be evaluated before any DAC connection, consider using the LMH3401EVM as a gain of 10 dB, single-to-differential interface to the inputs of the D2S stage. This setup allows single-ended sources to generate differential output signals through the combined LMH3401EVM to THS3217EVM configuration. The D2S, small-signal, frequency-response curves over input common-mode voltage (see Figure 13) were generated by adjusting the LMH3401 voltage supplies and maintaining V_{OCM} at midsupply to preserve input headroom on the LMH3401. In order to make single-ended, frequency-response measurements, the configuration shown in Figure 69 was used.

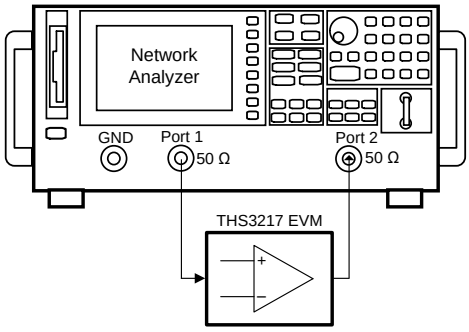


Figure 69. Frequency-Response Measurement: OPS Inverting and Noninverting, Midscale Buffer, and VREF Circuit Configurations

8.3 Harmonic Distortion Measurement

The distortion plots for all stages used a filtered high-frequency function generator to generate a very low-distortion input signal. The LMH3401 interface was used when testing the D2S and the full-signal path (D2S+OPS) harmonic distortion performance. Running the filtered signal through the LMH3401, as shown in Figure 70, provided adequate input signal purity because of the approximately –100-dBc harmonic distortion performance through 100 MHz. In order to test the harmonic-distortion performance of the OPS and midscale buffer, the configuration shown in Figure 71 was used.

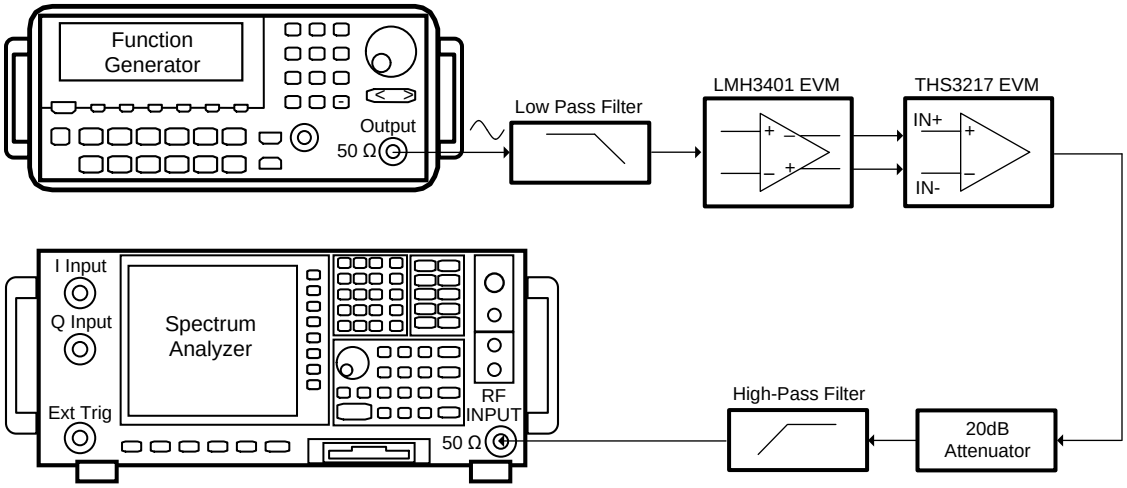


Figure 70. Harmonic-Distortion Measurement: D2S and Full-Path (D2S + OPS) Circuit Configurations

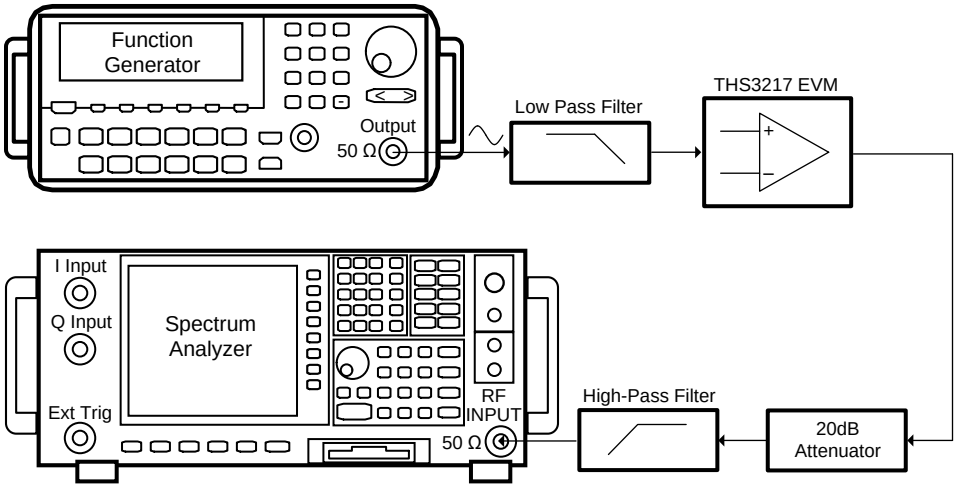


Figure 71. Harmonic-Distortion Measurement: OPS Inverting and Noninverting and Midscale Buffer Circuit Configurations

8.4 Noise Measurement

All the noise measurements were made using a very low-noise, high-gain bandwidth LMH6629 as a low-noise preamplifier to boost the output noise from the THS3217 before measurement on a spectrum analyzer, as shown in Figure 72. The 0.69-nV/√Hz input-voltage noise specification of the LMH6629 provides flat gain of 20 V/V through 100 MHz with its ultrahigh, 6.3-GHz gain bandwidth product. The D2S and OPS noise was measured with the common-mode voltage at GND.

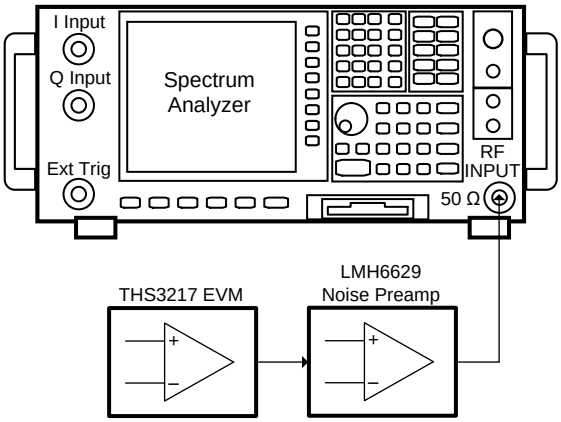


Figure 72. Noise Measurement Using LMH6629 Preamplifier

8.5 Output Impedance Measurement

Output impedance measurement for the three stages under different conditions were performed as a small-signal measurement calibrated to the device pins using an impedance analyzer. Calibrating the measurement to the device pins removes the THS3217EVM parasitic resistance, inductance, and capacitance from the measured data.

8.6 Step-Response Measurement

Generating a clean, fast, differential-input step for time-domain testing presents a considerable challenge. A multichannel pulse generator with adjustable rise and fall times was used to generate the differential pulse to drive D2S inputs in Figure 21. A high-speed scope was used to digitize the pulse response.

8.7 Feedthrough Measurement

In order to test the forward feedthrough performance of the OPS in the disabled state, the circuit shown in Figure 73 was used. The PATHSEL pin was driven low to select the internal path between the D2S and OPS. A 100-mV_{PP}, swept-frequency, sinusoidal signal was applied at the VREF pin and the output signal was measured at the OPS output pin (VOUT). The transfer function from VREF to the output of the D2S at VO1 has a gain of 0 dB, as shown in Figure 23. The results shown in Figure 57 account for the 6-dB loss due to the doubly-terminated OPS output, and therefore report the forward feedthrough between VOUT and VO1 at different OPS gains. The D2S inputs were grounded through 50-Ω resistors for this test.

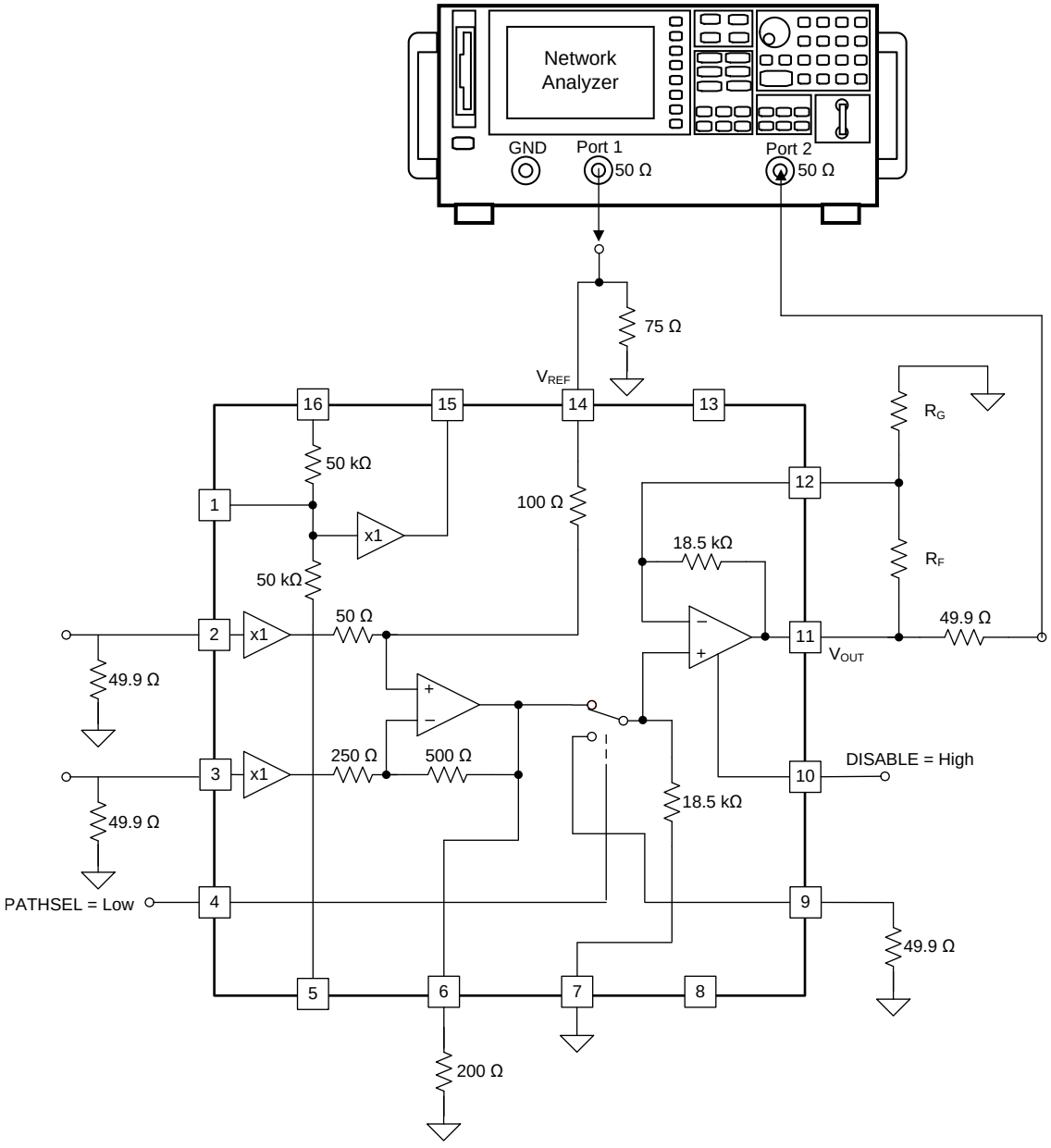


Figure 73. Forward-Feedthrough Test Circuit

Feedthrough Measurement (continued)

In order to test the reverse feedthrough performance of the OPS in its disabled state, the circuit shown in Figure 74 was used. The PATHSEL pin was driven high to select the external path to the OPS noninverting pin, VIN+. A 100-mV_{PP}, swept-frequency, sinusoidal signal was applied at the VIN+ pin and the output signal was measured at the D2S output pin (VO1). The results shown in Figure 58 account for the 16.5-dB loss due to the D2S termination, and the test reports the reverse feedthrough between the VO1 and VIN+ pins. The D2S inputs were grounded through 50-Ω resistors for this test.

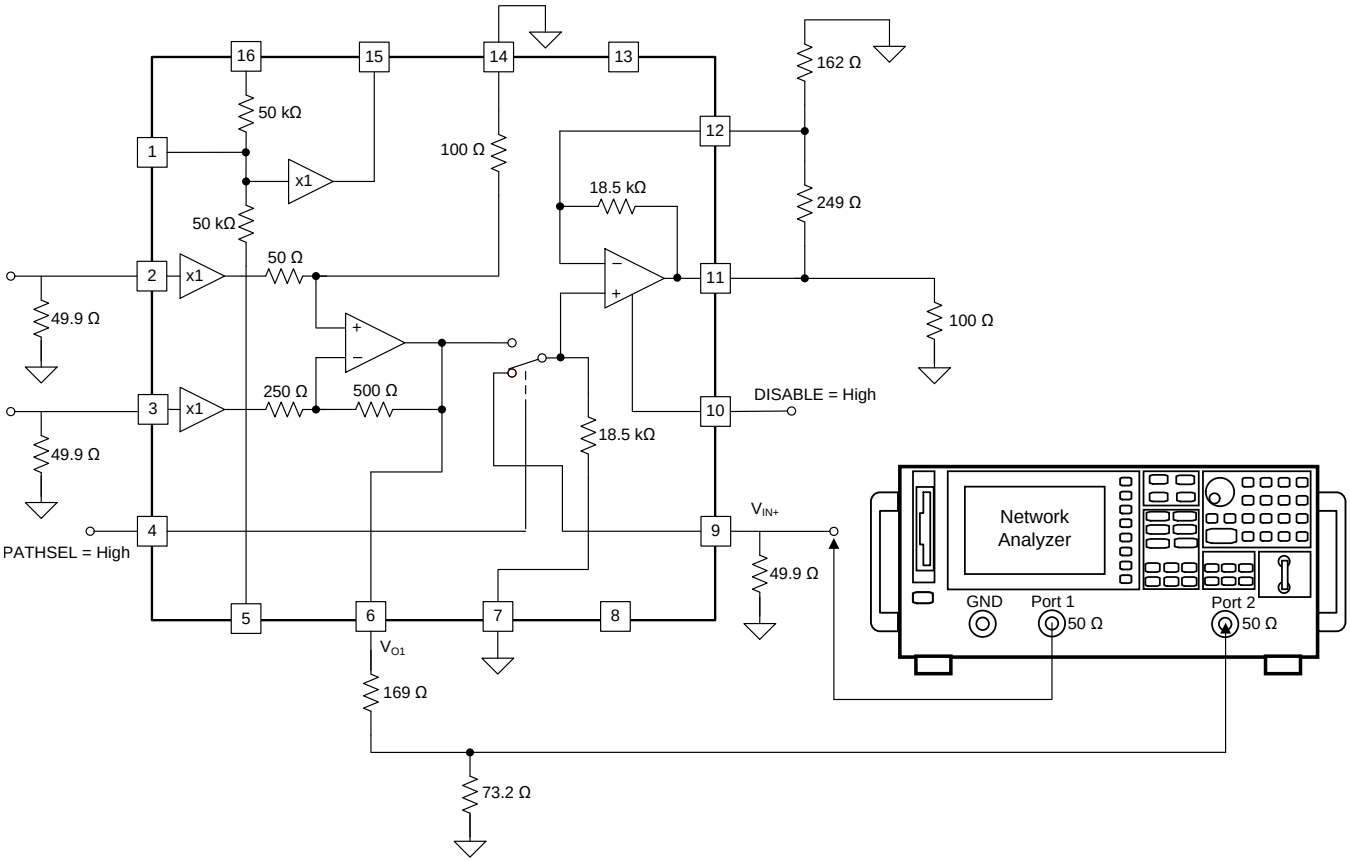


Figure 74. Reverse-Feedthrough Test Circuit

8.8 Midscale Buffer R_{OUT} Versus C_{LOAD} Measurement

For the tests in Figure 53 and Figure 54, the circuit shown in Figure 75 was used. The 150-Ω load circuit configured as shown, provides a 50-Ω path from the network analyzer back to the output of the buffer. As shown in Figure 75, place R_{OUT} below the load capacitor to improve the phase margin for the closed-loop buffer output, while adding 0-Ω dc impedance into the line connected to the VREF pin.

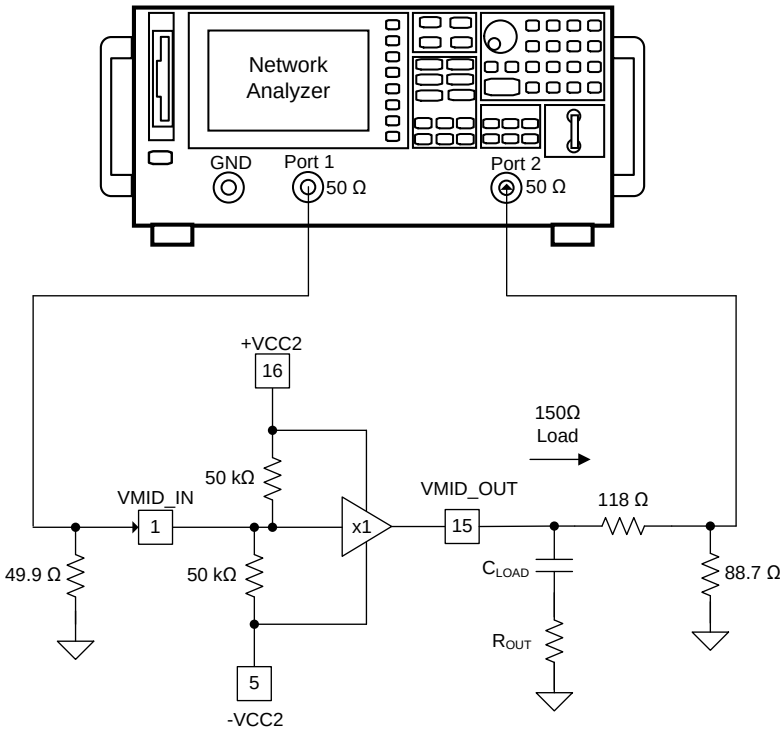


Figure 75. R_S Versus C_{LOAD} Measurement Circuit

9 Detailed Description

9.1 Overview

The THS3217 is a differential-input to single-ended output amplifier system that provides the necessary functional blocks to convert a differential output signal from a wideband DAC to a dc-coupled, single-ended, high-power output signal. The THS3217 typically operates using balanced, split supplies. Signal swings through the device can be adjusted around ground at several points within the device. Single-supply operation is also supported an ac-coupled signal path. The THS3217 supply voltage ranges from ±4.0 V to ±7.9 V. The two internal logic gates rely on a logic reference voltage at pin 7 that is usually tied to ground for any combination of power-supply voltages. The DISABLE control (pin 10) turns the output power stage (OPS) off to reduce power consumption when not in use.

A differential-to-single-ended stage (D2S) provides a high input impedance for a high-speed DAC (plus any reconstruction filter between the DAC and THS3217) operating over a common-mode input voltage range from –1 V to +3.0 V. This range is intended to support either current sourcing or current sinking DACs. The D2S is internally configured to reject the input common-mode voltage and convert the differential inputs to a single-ended output at a fixed gain of 2 V/V (6 dB).

An uncommitted, on-chip, wideband, unity-gain buffer is provided (between pins 1 and 15) to drive the VREF pin. The buffer offers extremely broad bandwidth to achieve very-low output impedance to high frequencies (Figure 51). The buffer does not provide a high full-power bandwidth because of a relatively low slew rate. The buffer stage includes a default midsupply bias resistor string of 50-kΩ each to set the default input to midsupply. This 25-kΩ Thevinin impedance is easily overridden with an external input source, but is intended to provide a midsupply bias for single-supply operation. The buffer amplifier that drives the VREF pin has two functions:

- Provides an easy-to-interface, dc-correction, servo-loop input
- Can be used as an offset injection point for the D2S output

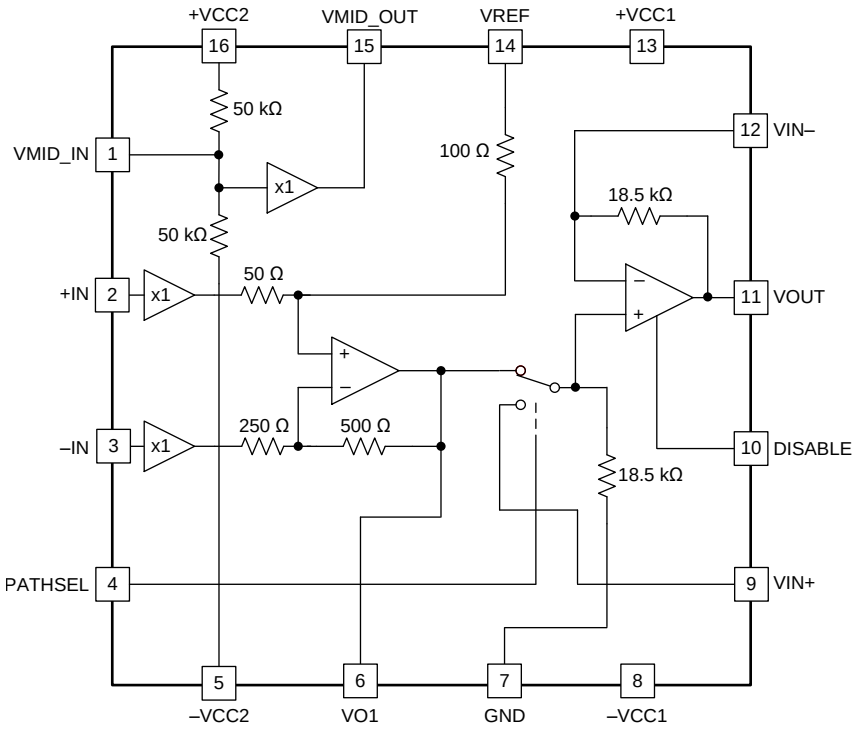
The final OPS provides one of the highest-performance, current-feedback amplifiers available for line-driving applications. The 950-MHz SSBW stage provides 5000 V/µs of slew-rate, sufficient to drive a 5-V_{PP} output with 500-MHz bandwidth. In addition, the OPS is able to drive a very-high continuous and peak output current sufficient to drive the most demanding loads at very high speeds. A unique feature added to the OPS is a 2 × 1 input multiplexer at the noninverting input. The PATHSEL control (pin 4) is used to select the appropriate signal path to the OPS noninverting input. One of the multiplexer select paths passes the internal D2S output directly to the OPS. The other select path accepts an external input to the OPS at VIN+ (pin 9). This configuration allows the D2S output, available at VO1 (pin 6), to pass through an external RLC filter and back into the OPS at VIN+ (pin 9).

If the OPS does not require power for certain application configurations, a shutdown feature has been included to reduce power consumption. For designs that do not use the OPS at all, two internal fixed resistors are included to define the operating points for the disabled OPS. An approximate 18.5-kΩ resistor to the logic reference (pin 7) from VIN+ (pin 9), and an approximate 18.5-kΩ, fixed, internal feedback resistor are included to hold the OPS pin voltages in range if no external resistors are used around the OPS. These resistors must be included in the design calculations for any external network.

Two sets of power supply-pins have been provided for both the positive and negative supplies. Pin 5 (–VCC2) and pin 16 (+VCC2) power the D2S and midscale buffer stages, while pin 8 (–VCC1) and pin 13 (+VCC1) supply power to the OPS. The supply rails are connected internally by antiparallel diodes. Externally, connect power first to the OPS, then connect back on each side with a π-filter (ferrite bead + capacitor) to the input-stage supply pins (see Figure 90). Do not use mismatched supply voltages on either the positive or negative sides because the supplies are internally connected through the antiparallel diodes. Imbalanced positive and negative supplies are acceptable, however.

When the OPS is disabled, the output pin goes to high impedance. However, do not connect two OPS outputs from different devices together and select them as a *wired-or* multiplexer. Although the high-impedance output is disabled, the inverting node is still available through the feedback resistor, and can load the active signal. The signal path through the inverting node typically degrades the distortion on the desired active signal in a wired-or multiplexer configuration using CFA amplifiers.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Differential to Single-Ended Stage (D2S) With Fixed Gain of 2-V/V (Pins 2, 3, 6 and 14)

This buffered-amplifier stage isolates the DAC output nodes from the differential to single-ended conversion. Presenting two high-impedance inputs allows the DAC to operate in its best configuration independent of subsequent operations. The two very wideband input buffers hold an approximately constant response shape over a wide input common-mode operating voltage. Figure 13 shows 6 dB of gain with 0.5-dB flatness through 500 MHz over the intended –1-to +3-V input common-mode range. In this case, the VREF pin is grounded, forcing the D2S output to be centered on ground for any input common-mode voltage. For the D2S-only tests, a 100-Ω load is used to showcase the performance of this stage directly driving a doubly-terminated cable. The wide input common-mode range of the D2S satisfies the required compliance voltage over a wide range of DAC types. Most current sourcing DACs require an average dc compliance voltage on their outputs near ground. Current sinking DACs require an average dc compliance voltage near their positive supply voltage for the analog section. The 3-V maximum common-mode range is intended to support DAC supplies up to 3.3 V, where the average output operating current pulls down from 3.3 V by the termination impedance from the supply. For instance, a 20-mA tail current DAC must level shift from a 3.3-V bias on the output resistors down to 3 V or lower. This DAC-to-THS3217 configuration requires at least a 300-mV dc level shift with half the tail current in each side, implying a 30-Ω load impedance to the supply on each side of the 20-mA reference current.

The overriding limits to the input common-mode operating range are due to the input buffer headroom. Over temperature, the D2S input headroom specification is 2 V to the negative supply and 1.5 V to the positive supply. Therefore, operation at a 3-V input common-mode voltage requires at least a 4.5-V positive supply, where 5 V is a more conservative minimum.

While DAC outputs rarely have any common-mode signal present (unless the reference current is being modulated), the D2S does a reasonable job of rejecting input common-mode signals over frequency. Figure 17 shows the CMRR to decrease above 10 MHz. For current-sinking DACs coming from a positive supply voltage, any noise on the positive supply looks like an input common-mode signal. Keeping the noise small at higher frequencies reduces the possibility of feedthrough to the D2S output due to the decreasing CMRR at higher frequencies. A current-sinking DAC uses pull-up resistors to the voltage supply to convert the DAC output current to a voltage. Make sure that the DAC voltage supply has been properly decoupled through a ferrite bead and capacitor, π-filter network similar to the supply decoupling for the THS3217 shown in Figure 90.

Feature Description (continued)

The D2S provides a differential gain of 6 dB. The gain is reasonably precise using internal resistor matching with extremely low gain drift over temperature (see Figure 61 and Figure 62). The single-ended D2S output signal can be placed over a wide range of dc offset levels using the VREF pin. The VREF pin shows a precise gain of 1 V/V to the D2S output. Grounding VREF places the first stage output centered on ground (with some offset voltage). For best ac performance through the D2S, anything driving the VREF pin must have a very wide bandwidth with very low output impedance over frequency while driving a 150-Ω load. The on-chip midscale buffer provides these features (see Figure 51). When a dc offset (or other small-level ac signal) must be applied to the VREF pin, buffer the signal through the midscale buffer stage. Maintain the total range of the dc offset plus signal swing within the available output swing range of the D2S. The headroom to the supplies is a symmetric ±1.65 V (max) over temperature. Therefore, on the minimum ±4-V supply, the D2S operates over a ±2.35-V output range. At the maximum ±7.9-V supply, a ±6.25-V output range is supported. At the higher swings, account for available linear output current, including the current into the internal feedback resistor load of approximately 500-Ω.

Figure 76 shows the internal structure of the D2S functional block. It consists of two internal stages:

1. The first stage consists of two wideband, closed-loop, fixed gain of 1 V/V buffers to isolate the requirements of the complementary DAC output from the difference operation of the D2S.
2. The second stage is a wideband CFA configured as a difference amplifier, operating in a fixed gain of 2 V/V, performing the differential to single-ended conversion.

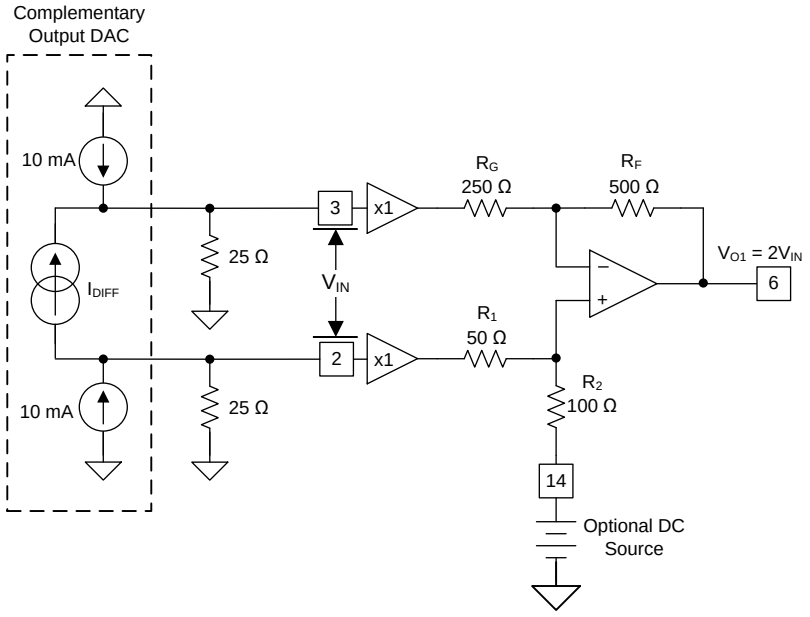


Figure 76. D2S Operating Example

The CFA design offers the best, full-power bandwidth versus supply current, with moderate noise and dc precision. Figure 76 shows a typical current-sourcing DAC with a 20-mA total tail current. The tail current is split equally between the 25-Ω termination resistors to produce a dc common-mode voltage and a differential ac current signal. This example sets the input common-mode voltage at 0.25 V, and is also the *compliance* voltage of the DAC. The 25-Ω termination resistors shown here are typically realized as a 50-Ω matched reconstruction (or Nyquist) filter between the DAC and the THS3217 buffer inputs for most AWG applications. The DAC signal is further amplified by 6 dB in the second stage for a net transimpedance gain of 100-Ω to the D2S output at VO1. This configuration produces a 2-V_{PP} output for the 20-mA reference current assumed in the example of Figure 76. The input common-mode voltage is cancelled on the two sides of the op amp circuit to give a ground referenced output. Any voltage applied to the VREF pin has a gain transfer function of 1 V/V to VO1, independent of the signal path, as long as the source impedance of VREF is very low at dc and over frequency.

Feature Description (continued)

The IN+ buffer output drives a 150-Ω load with VREF grounded. Any source driving VREF must have the ability to drive a 150-Ω load with low output impedance across frequency. For differential input signals, the IN– buffer drives a 150-Ω active load. The active load is realized by a combination of the 250-Ω R_G resistor and the inverted and attenuated signal present at the inverting terminal of the difference amplifier stage. If only IN– is driven (with IN+ at a dc fixed level), the load is 250 Ω.

The resistor values around the D2S difference amplifier are derived in the following sequence, as shown in Figure 77:

1. Select the feedback resistor value to set the response shape for the wideband CFA stage. The 500-Ω design used here was chosen as a compromise between loading and noise constraints.
2. Set the input resistor on the inverting input side to give the desired single-sided gain for that path. Setting R_G= 250-Ω results in a gain of –2 V/V from the buffered signal (–V) to the output of the difference amplifier.
3. Solve the required attenuation to the noninverting input to get a matched gain magnitude for the signal provided at the buffer output (+V) on the noninverting path. If α = R2 / (R1 + R2), as shown in Figure 77, then the solution for α is shown in Equation 2:

$$\alpha\left(1+\frac{R_F}{R_G}\right)=2 \tag{1}$$

$$\alpha=\frac{2}{3}=\frac{R1}{(R1+R2)} \tag{2}$$

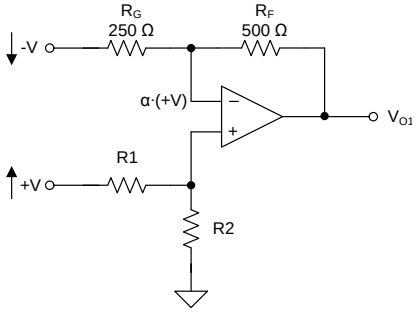


Figure 77. D2S Impedance Analysis

4. After solving the attenuation from the buffer output to the amplifier noninverting input, set the impedance (R1 + R2). It is preferable to have the two first stage buffer outputs drive the same load impedance to match nonlinearity in their outputs in order to improve even-order harmonic distortion. The load impedance from –V to R_G has an active impedance because of the inverted and attenuated version of the input signal appearing at the inverting amplifier node from the +V input signal. Assuming a positive input signal into the +V path, an attenuated version of the signal appears at the amplifier summing junction side of R_G, while the inverted version of the signal appears on the input side of R_G.

The impedance seen at node –V in Figure 77 is derived in Equation 3 by solving for the V/I expression across R_G.

$$Z_i=\frac{R_G}{(1+\alpha)}=\frac{250\ \Omega}{1+\frac{2}{3}}=150\ \Omega \tag{3}$$

For load balancing, (R1 + R2) = 150 Ω while the attenuation is α. More generally, all the terms are now available to solve for R2, as shown in Equation 4:

$$R2=R_G\frac{\alpha}{(\alpha+1)}=250\ \Omega\frac{\frac{2}{3}}{1+\frac{2}{3}}=100\ \Omega \tag{4}$$

R1 is then simply (Z_i- R2) = 50 Ω.

Feature Description (continued)

This analysis for matched gains and buffer loads can be applied to a more general discrete design using different target gains and starting R_F values. It is clearly useful to have the attenuation and buffer loading accurately controlled. Therefore, it is very important to control the impedance at the VREF pin to be as low as possible. For instance, using the midscale buffer to drive the VREF pin only adds 0.21 Ω dc impedance in series with R2. This low dc output impedance can only be delivered with a closed-loop buffer design. For discrete implementations of this D2S, consider the BUF602 buffer and LMH6702 wideband CFA amplifier. For even better dc and ac output impedance in the buffers (and possibly better gain), use a closed-loop, dual, wideband op amp like the OPA2889 for lower frequency applications, or the OPA2822 for higher frequency. These unity gain stable op amps can be used as buffers offering different performance options along with the LMH6702 wideband CFA over the design point chosen for the THS3217.

After gain matching is achieved in the single op amp differential stage, the common-mode input voltage is cancelled to the output, and the VREF input voltage is amplified by 1 V/V to the output. The analysis circuit is shown in Figure 78, where VREF is shown grounded at the R2 element.

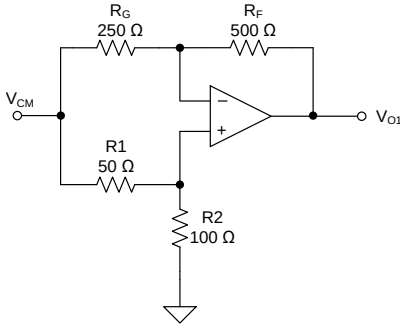


Figure 78. D2S Common-Mode Cancellation

The gain magnitudes are equal on each side of the differential inputs; therefore, the common-mode inputs achieve the same gain magnitude, but opposite phase, resulting in common-mode signal cancellation. The inverting path gain is $V_{CM} \times (R_F / R_G)$. The noninverting path gain is $V_{CM} \times \alpha \times (1 + R_F / R_G)$. Using Equation 5:

$$\alpha = \frac{\frac{R_F}{R_G}}{\left(1 + \frac{R_F}{R_G}\right)} \tag{5}$$

the noninverting path gain becomes $+V_{CM} \times R_F / R_G$, and adding that result to the inverting path signal cancels to zero. Slight gain mismatches reduce this rejection to the 55-dB typical CMRR, with a 47-dB tested minimum. The 47-dB minimum over the 3-V maximum common mode input range adds another ±13.4-mV worst-case D2S output offset term to the specified maximum ±35-mV output offset with 0-V input common-mode voltage. The polarity of the gain mismatch is random.

The VREF pin input voltage (V_{REF}) generates a gain of 1 V/V using the analysis shown in Figure 79

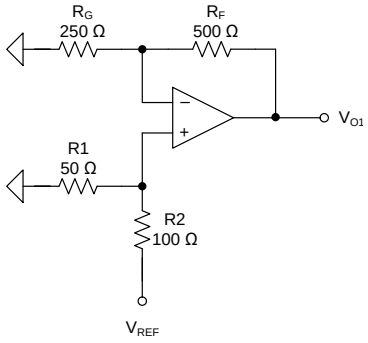


Figure 79. Gain Transfer Function from VREF to VO1

Feature Description (continued)

The gain from VREF to VO1 is shown in Equation 6:

$$V_{REF}\frac{R1}{(R1+R2)}\left(1+\frac{R_F}{R_G}\right)=V_{O1} \tag{6}$$

Getting both R1 and (R1 + R2) in terms of R_G and the target attenuation, α simplifies, as shown in Equation 7:

$$\frac{R1}{(R1+R2)}=\frac{R_G\frac{1-\alpha}{1+\alpha}}{R_G\frac{1}{1+\alpha}}=(1-\alpha) \tag{7}$$

Putting Equation 7 back into the gain expression(Equation 6), and expanding out gives:

$$V_{REF}(1-\alpha)\left(1+\frac{R_F}{R_G}\right)=V_{O1} \tag{8}$$

Recall that in order to get differential gain balance, $\alpha = -(R_F / R_G)$. Putting that into Equation 8 reduces the expression to $V_{O1} = V_{REF}$, a gain of 1 V/V. This gain is very precise as shown in the *D2S Electrical Characteristics* table, where the tested dc limits are 0.985 V/V to 1.015 V/V.

The D2S output offset and drift are largely determined by the internal elements. The only external consideration is the dc source impedance at the two buffer inputs. With low source impedance, the D2S output offset is tested to be within ±35 mV, that becomes a maximum ±17 mV input differential offset specification. Assuming the dc source impedances are closely matched, the mismatch in the two input bias currents adds another input offset term for higher source impedances. The input bias offset current is limited in test to be < ±0.40 µA. This error term does not rise to add more than ±1 mV input differential offset until the dc source impedance exceeds 2.5 kΩ. A high dc source impedance most commonly occurs in an input ac-coupled, single-supply application, where dc offsets are less critical.

The absolute input bias currents modifies the common-mode input voltage if the dc source resistance is too large. That term is tested to a limit of ±4 µA on each input. To move the input common mode voltage by ±100 mV, the dc source impedance must exceed 25 kΩ. This added input common-mode voltage is cancelled by the D2S at the output (VO1, pin6).

The D2S output noise is largely fixed by the internal elements. The D2S shows a differential input voltage noise of 9 nV/√Hz, and a current noise of 2 pA/√Hz on each input. Higher termination resistors increase this source noise, as given by Equation 9, where R_t is the dc termination impedance at each buffer input. The D2S has a 1/f corner at approximately 30 kHz (see Figure 18).

$$e_{i\_diff}=\sqrt{(9nV)^2+2(4kTR_t)+2(2pA\times R_t)^2} \tag{9}$$

The total differential input noise is dominated by the differential voltage noise. For instance, evaluating this expression for R_t = 200 Ω on each input, increases the total differential input noise to 9.4 nV/√Hz, only slightly greater than the 9 nV/√Hz for the D2S with 0-Ω source R_t on each input. If higher final output SNR is desired, consider generating as much input swing as the DAC can support, but increase the termination impedance. It is possible that a lower tail current with higher R_t will yield improved SNR at the D2S input. This differential input noise appears at the D2S output times a gain of 2 V/V.

$$e_{out\_diff}=2\times e_{i\_diff} \tag{10}$$

9.3.2 Midscale (DC) Reference Buffer (Pin 1 and Pin 15)

This optional block can be completely unconnected and not used if the design does not require this feature. Internal 50-kΩ resistors to the power supplies bias the input of the buffer to the midpoint of the supplies used. The internal resistors set a midsupply operating point when the buffer is not used, as well as a default midsupply point at the buffer output to be used in other stages for single-supply, ac-coupled applications.

Feature Description (continued)

The buffer provides a very wideband, low output-impedance when used to drive the VREF pin (see Figure 51). To provide this low broadband impedance, the closed-loop midscale (dc) reference buffer offers a very broadband SSBW, but only a modest large-signal bandwidth (LSBW); see Figure 49. This path is not normally intended to inject a wideband signal, but can be used for lower-amplitude signals. Driving the buffer output into the VREF pin allows a wideband small-signal term to be added into the D2S along with the signal from the differential inputs.

The midscale (or dc) reference buffer injects an offset voltage to the output offset of the D2S when it drives the VREF pin. The offset has very low drift, but consider the effect of the input bias current times the dc source impedance at VMID_IN (pin 1). When used as a default midsupply reference for single-supply operation, the input to this buffer is just the average of the total power supplies though a 25-kΩ source impedance. Add an external capacitor to filter the supply and the 50-kΩ internal resistors. A 1-µF capacitor on pin 1 adds a 6-Hz pole to the noise sources. If lower noise at lower frequencies is required, implement a midscale divider with external, lower-valued resistors in parallel with the internal 50-kΩ values.

If the midscale buffer drive the VREF pin, another noise term is added to Equation 9 and Equation 10. The midscale buffer 4.4-nV/√Hz voltage noise is amplified by 0 dB, and adds (RMS) a negligible impact to the total D2S output noise. The biggest impact comes when the internal default 50-kΩ dividers are used. Be sure to decouple pin 1 with at least a 1-µF capacitor in the application to reduce the noise contribution through this path. Figure 80 is the simulation circuit where the only change is to add or remove the 1-µF capacitor.

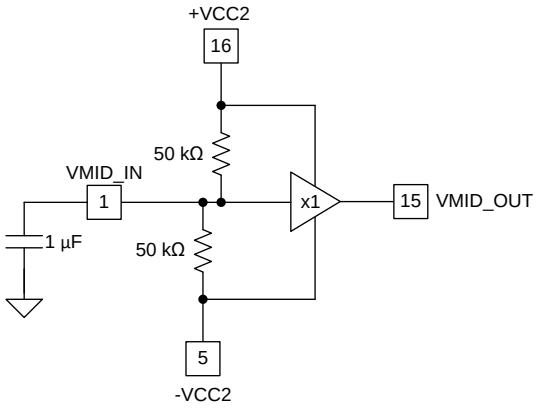


Figure 80. Midscale Buffer Noise Model

Figure 81 shows the simulated output noise for the midscale buffer using the internal 50-kΩ divider with and without a 1-µF capacitor on pin 1.

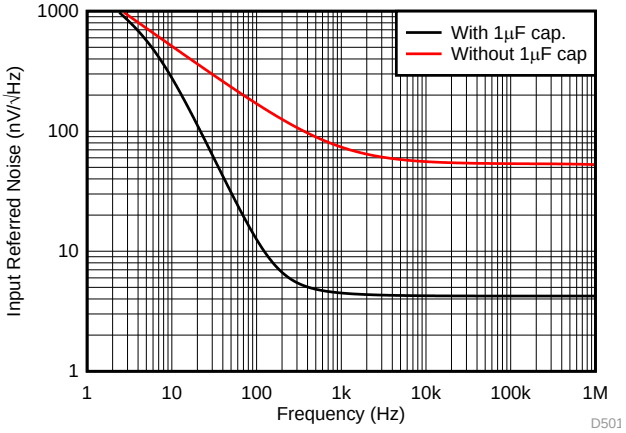


Figure 81. Buffer-Output Noise Comparison With and Without the 1-µF Bypass Capacitor on Pin 1

Feature Description (continued)

In the flat region, the 1-µF capacitor reduces the midscale buffer output spot noise from approximately 55 nV/√Hz to 4.4 nV/√Hz. If the noise below 100 Hz is unacceptable, either add a low-noise buffer to drive this input, or add lower-value resistors externally to set up the midsupply bias. Also, consider the noise impact of any reference voltage source driving the midscale buffer path.

9.3.3 Output Power Stage (OPS) (Pins 4, 7, 9, 10, 11, and 12)

This wideband current-feedback amplifier (CFA) provides a flexible output driver with several unique features. The OPS can be left unused if the specific application only uses the D2S alone, or a combination of the D2S with an off-chip power driver. If left unused, simply tie DISABLE (pin 10) and PATHSEL (pin 4) to the positive supply. This logic configuration turns the OPS off and opens up the external and internal OPS noninverting input paths. An internal fixed 18.5-kΩ resistor holds the external input pin at the logic reference voltage on pin 7. Additionally, the OPS output is connected to the inverting input through another internal 18.5-kΩ resistor when no external resistors are installed on pins 9, 11, or 12. Disabling the OPS saves approximately 21 mA of supply current from the nominal total 54 mA with all stages operating on ±6-V supplies.

The noninverting input to the OPS provides two possible paths controlled by the PATHSEL logic control, pin 4. With the logic reference (pin 7) at ground, floating pin 4 or controlling it to a voltage < 0.7 V connects the input path directly to the internal D2S output. Tying pin 4 to the positive supply, or controlling it to a logic level > 1.3 V, connects the input path to the external input at pin 9. The intent for this switched input is to allow an external filter to be inserted between the D2S output and OPS inputs when needed, and bypass the filter when not. Alternatively, this switched input also allows a completely different signal path to be inserted at the OPS input, independent of that available at the internal D2S output.

In situations where the D2S output at pin 6 is switched into another off-chip power driver, the OPS can be disabled using pin 10. With the logic reference (pin 7) at ground, floating pin 10, or controlling it to a voltage < 0.7 V, enables the OPS. Tying pin 10 to the positive supply, or controlling it to a logic level > 1.3 V, disables the OPS.

Operation of the wideband, current-feedback OPS requires an external feedback resistor and a gain element. After configuring, the OPS can amplify the D2S output through either the noninverting path, or be configured as an inverting amplifier stage using the external OPS input at pin 9 as a dc reference.

One of the first considerations when designing with the OPS is determining the external resistor values as a function of gain in order to hold the best ac performance. The loop gain (LG) of a CFA is set by the internal open-loop transimpedance gain from the inverting error current to the output, and the effective feedback impedance to the inverting input. The nominal internal open-loop transimpedance gain and phase are shown in Figure 82.

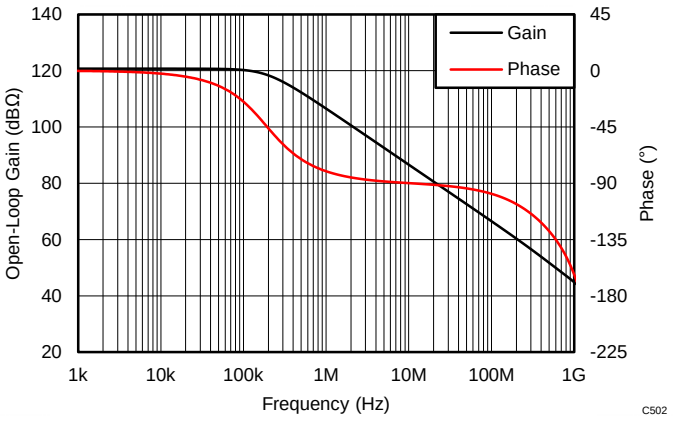


Figure 82. Simulated OPS Z_{OL} Gain And Phase

Feature Description (continued)

The feedback transimpedance (Z_{OPT}) can be approximated as shown in Equation 11, where R_i is the open-loop, high-frequency impedance into the inverting node of the OPS. For a detailed derivation of Equation 11, see *Setting Resistor Values to Optimize Bandwidth* section in the OPA695 datasheet (SBOS293).

$$Z_{OPT} \approx R_F + \left(1 + \frac{R_F}{R_G}\right) R_i \tag{11}$$

As the signal gain is varied, hold Z_{OPT} approximately constant to hold the ac response constant over gain. Holding Z_{OPT} constant is a requirement to solve for R_F. An example of the THS3217 OPS R_F derivation is shown in Equation 12:

$$R_F = 351\ \Omega - \left(1 + \frac{R_F}{R_G}\right) \times 42\ \Omega \tag{12}$$

The calculations are complicated by the internal feedback resistor value of approximately 18.5-kΩ. After the external R_F is approximately set by the constant bandwidth consideration, the R_G must be set considering the other gain error terms. From the noninverting input of a CFA op amp, the total gain to the output includes a loss through the input buffer stage (described by the CMRR) and the loop gain (LG) loss set by the typical dc open-loop transimpedance gain and the feedback transimpedance. Extract the buffer gain from the VIN+ input to the VIN– input from the CMRR using Equation 13. This gain loss only applies to the noninverting mode of operation and can be neglected in inverting mode operation.

$$\beta = \left(1 - 10^{\frac{-CMRR}{20}}\right) = \text{Buffer Gain CFA} \tag{13}$$

The OPS has a typical CMRR of 49 dB (buffer gain, β = 0.9965) with a tested minimum of 47 dB (minimum buffer gain of 0.9955). The dc LG adds to the gain error. The LG is given by Equation 14 where the typical design gain of 2.5 V/V value is also shown (the 245 Ω shown for R_F is the external 249-Ω feedback resistor in parallel with the internal 18.5-kΩ feedback resistor).

$$LG = \frac{Z_{OL}}{\left(R_F + NG \times R_i\right)} = \frac{1\ M\Omega}{\left(245\ \Omega + 2.5 \times 42\ \Omega\right)} = 2857 \tag{14}$$

The closed-loop output impedance with a heavy load also adds a minor gain loss that is neglected here. The total noninverting gain is then set by Equation 15 (remember to include the internal R_F in this analysis. The $R_{F'}$ shown here is the parallel combination of the internal and external feedback resistors).

$$A_V^+ = \beta \times \left(1 + \frac{R_F}{R_G}\right) \times \frac{LG}{\left(1 + LG\right)} \tag{15}$$

Using nominal values for each term at the specified R_F = 249 Ω and R_G = 162 Ω gives the gain calculation in Equation 16, yielding a nominal gain very close to 2.5 V/V.

$$A_V^+ = 0.9965 \times \left(1 + \frac{245.7}{162}\right) \times \frac{2857}{1 + 2857} = 2.507 \tag{16}$$

Testing the total gain spread with the internal variation in buffer gain, open-loop transimpedance gain, internal feedback resistor, and ±1% external resistor variation gives a worst-case gain spread of 2.49 V/V to 2.51 V/V. The gain error is primarily dominated by the external 1% resistors. For the tighter tolerance shown in Table 2, use 0.1% precision resistors.

Feature Description (continued)

At very low gains (< 1.5 V/V) parasitic LC effects at the inverting input render a flat frequency response impossible. Looking then at gains from 1.5 V/V and up, a table of nominally recommended R_F and R_G values is shown in Table 2. Do not operate the OPS in noninverting gains of less than 2.5 V/V for large output signals because the limited slew-rate of the CFA input buffer causes signal degradation. Table 2 accounts for the nominal gain losses described previously, and uses standardized resistor values to minimize the nominal gain-error to target gain. The calculation also restricts the solution to a minimum R_G = 20 Ω. The gain calculations include the nominal buffer gain loss, the loop-gain effect, and the nominal internal feedback resistor = 18.5 kΩ.

Table 2. Optimized R_F Values for Different OPS Noninverting Signal Gains

TARGET GAIN (V/V)	MEASURED SSBW (MHz)	BEST R_F (Ω)	BEST R_G (Ω)	CALCULATED GAIN		GAIN ERROR (%)
				(V/V)	(dB)	
1.5	1400	294	562	1.505	3.551	0.3
2	—	274	267	1.998	6.013	–0.1
2.5	950	249	162	2.500	7.960	0
3	—	232	113	3.008	9.566	0.3
3.5	—	205	80.6	3.493	10.863	–0.2
4	—	182	59	4.028	12.103	0.7
4.5	—	165	46.4	4.495	13.055	–0.1
5	652	140	34.8	4.960	13.910	–0.8
5.5	—	121	26.7	5.467	14.754	–0.6
6	—	113	22.1	6.043	15.624	0.7
6.5	—	115	20.5	6.532	16.301	0.5
7	—	121	20	6.965	16.859	–0.5
7.5	—	133	20	7.553	17.563	0.7
8	—	143	20	8.043	18.108	0.5
8.5	—	154	20	8.580	18.670	0.9
9	—	162	20	8.971	19.057	–0.3
9.5	—	174	20	9.557	19.606	0.6
10	315	187	20.5	9.966	19.970	–0.3

The measured bandwidths in Table 2 come from Figure 25 using the resistor values in the table and a 100-Ω load. Plotting the R_F value versus gain gives the curve of Figure 83. The curve shows some ripple due to the standard value resistors used to minimize the target dc gain error.

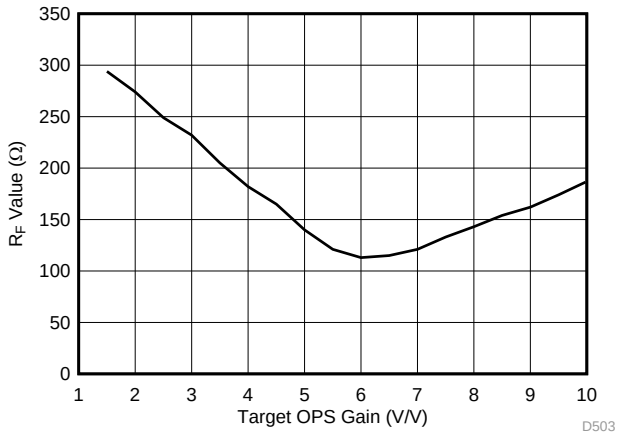


Figure 83. Suggested External R_F Value vs Noninverting Gain for the OPS

Using R_F values greater than the recommended values in Table 2 band-limits the response, whereas using less than the recommended R_F values peaks the response. Using the values shown in Table 2 results in an approximately constant SSBW (see Figure 25. Holding a more constant loop-gain over the external gain setting also acts to hold a more constant output impedance profile, as shown in Figure 84. The swept-frequency, closed-loop, output impedance is shown for gains of 2.5 V/V, 5 V/V, and 10 V/V using the R_F and R_G values of Table 2. The first two steps do a good job of delivering the same (and very low) output impedance over frequency, while the gain of 10 V/V shows the expected higher closed-loop output impedance due to the reduced loop-gain and bandwidth.

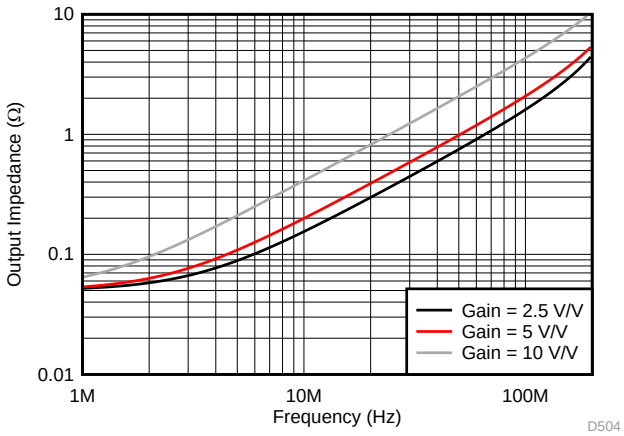


Figure 84. OPS Closed-Loop Output Impedance vs Gain Setting

Reducing the R_F value with increasing gain also helps minimize output noise versus a fixed R_F design. See Figure 39 for the three noise terms for the OPS. The total output noise calculation is shown in Equation 17:

$$e_o = \sqrt{\left(e_{ni}^2 + 4kTR_S + \left(i_{bn}R_S\right)^2\right)NG^2 + \left(i_{bi}R_F\right)^2 + \left(4kTR_F\right)NG} \quad (17)$$

where

- R_S is the source impedance on the noninverting input. If the OPS is driven from the D2S stage directly using the internal path, $R_S \approx 0\ \Omega$.
- $NG = (1 + R_F / R_G)$ for the design point.
- The flat-band noise numbers for the OPS are:
  - $E_{ni} = 3.2\ nV/\sqrt{Hz}$
  - $I_{bn} = 2.7\ pA/\sqrt{Hz}$
  - $I_{bi} = 30\ pA/\sqrt{Hz}$

Using the values of R_F and R_G listed in Table 2, a swept gain output- and input-referred noise estimate is computed, as shown in Table 3. In this sweep, R_S = 0 Ω. The input-referred noise (E_{ni}) in Table 2 is at the noninverting input of the OPS. To refer the noise to the D2S differential inputs, divide the output noise by two if there is no interstage loss. Dividing the E_{ni} column by 2 V/V shows that the OPS noise contribution is negligible when referred to the D2S inputs, where the 9-nV/√Hz differential input noise dominates. Operating with higher feedback resistors in the OPS quickly increases the output noise due to the inverting input current noise term. Although increasing R_F improves phase margin (for example, when driving a capacitive load), be careful to check the total output noise using Equation 17.

Table 3. Total Input- and Output-Referred Noise of the OPS Versus Gain

TARGET GAIN (V/V)	BEST R_F (Ω)	BEST R_G (Ω)	E_{O} (nV/√Hz)	E_{in} (nV/√Hz)
1.5	294	562	10.4	6.9
2	274	267	11.3	5.6
2.5	249	162	12.3	4.9
3	232	113	13.5	4.5
3.5	205	80.6	14.7	4.2
4	182	59	15.9	4.0
4.5	165	46.4	17.2	3.8
5	140	34.8	18.6	3.7
5.5	121	26.7	20.0	3.6
6	113	22.1	21.4	3.6
6.5	115	20.5	22.9	3.5
7	121	20	24.4	3.5
7.5	133	20	25.9	3.5
8	143	20	27.4	3.4
8.5	154	20	29.0	3.4
9	162	20	30.5	3.4
9.5	174	20	32.1	3.4
10	187	20.5	33.6	3.4

Operating the OPS as an inverting amplifier is also possible. When driving the OPS directly from the D2S to the R_G resistor, use the values shown in Table 2 for the noninverting mode to achieve good results. Note that the R_G resistor is the load for the D2S stage. Operating with the D2S driving an R_G < 80 Ω increases the harmonic distortion of the D2S. In that case, scaling R_F and R_G up to reduce the loading may result in better system performance at the cost of a lower OPS bandwidth. Driving the D2S output at pin 6 into the OPS in an inverting mode allows for the option to select the external input of the OPS, and drive another signal or dc level into the noninverting input at pin 9. In order to reduce layout parasitics, consider splitting the R_G resistor in two, with the first half close to pin 6 and the second half close to pin 12. Splitting R_G in this manner places the trace capacitance inside the two resistors keeping both active nodes more stable. Also, open up the ground and power planes under the trace, if possible.

Using the PS to receive and amplify a signal in the inverting mode with a matched terminating impedance, requires another resistor to ground (R_M) along with R_G. This R_M resistor is shown in Figure 85 for a 50-Ω matched input impedance design.

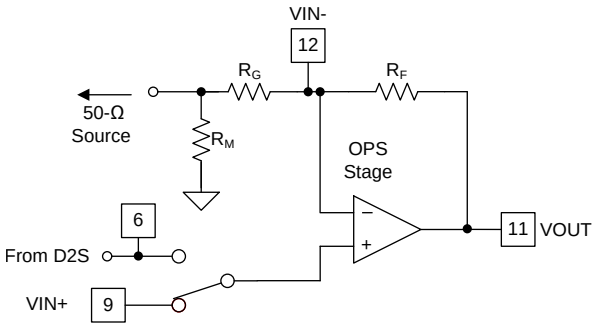


Figure 85. Inverting OPS Operation With Matched Input Impedance

Table 4 gives the recommended external resistor values versus gain for the inverting gain mode with input matching configuration. Table 4 solves for the required R_F to simultaneously allow the gain, input impedance (50 Ω), and feedback transimpedance to be controlled to the optimum target values. The table includes the effect of the internal 18.5-kΩ feedback resistor, and minimizes the RMS error to input impedance target (Z_I) and overall gain.

Table 4. Resistor Values Versus Gain for the Inverting OPS Configuration

TARGET GAIN (V/V)	MEASURED SSBW (MHz)	BEST R_F (Ω)	BEST R_G (Ω)	BEST R_M (Ω)	CALCULATED GAIN		GAIN ERROR (%)	Z_I (Ω)	Z_I ERROR (%)
					(V/V)	(dB)			
1	1000	280	274	60.4	1.002	0.022	0.250	49.490	–1.019
1.5	—	255	169	71.5	1.506	3.554	0.376	50.243	0.486
2	—	249	124	84.5	2.000	6.019	–0.014	50.254	0.508
2.5	860	237	93.1	107	2.490	7.924	–0.403	49.784	–0.433
3	—	226	75	150	3.013	9.581	0.444	50.000	0.000
3.5	—	226	63.4	237	3.491	10.859	–0.258	50.019	0.039
4	—	221	54.9	604	4.010	12.064	0.259	50.326	0.651
4.5	—	226	49.9	Open	4.525	13.111	0.545	49.90	–0.200
5	760	249	49.9	Open	4.985	13.953	–0.301	49.90	–0.200
5.5	—	274	49.9	Open	5.485	14.784	–0.264	49.90	–0.200
6	—	301	49.9	Open	6.026	15.601	0.434	49.90	–0.200
6.5	—	324	49.9	Open	6.486	16.240	–0.208	49.90	–0.200
7	—	348	49.9	Open	6.967	16.861	–0.472	49.90	–0.200
7.5	—	374	49.9	Open	7.487	17.487	–0.167	49.90	–0.200
8	—	402	49.9	Open	8.048	18.114	0.600	49.90	–0.200
8.5	—	422	49.9	Open	8.448	18.536	–0.607	49.90	–0.200
9	—	449	49.9	Open	8.989	19.074	–0.123	49.90	–0.200
9.5	—	475	49.9	Open	9.509	19.563	0.100	49.90	–0.200
10	260	499	49.9	Open	9.990	19.991	–0.100	49.90	–0.200

At higher gains, R_M increases to larger values, and the resistor is excluded from the circuit. The resulting input impedance of the network is resistor R_G. From that point, R_F simply increases to get higher gains, thereby rapidly reducing the SSBW. However, below a gain of –5 V/V, the inverting design with the values shown in Table 4 holds a more constant SSBW versus the noninverting mode (see Figure 26).

9.3.3.1 Output DC Offset and Drift for the OPS

The OPS provides modest dc precision with typical and maximum dc error terms in Table 5. The input offset voltage applies to either input path with very little difference between the internal and external paths.

Table 5. Typical Offset and Bias Current Values for the OPS

PARAMETER	TYPICAL	MINIMUM	MAXIMUM	UNIT
V_{IO}	±1	–12	12	mV
I_{bn}	5	–5	15	µA
I_{bi}	±5	–40	40	µA

Selecting the internal path results in no source resistance for I_{bn}, so that term drops out. When the external path is selected, a dc source impedance may be present, so the I_{bn} term creates another error term, and adds to the total output offset.

Stepping through an example design for the OPS output dc offset using the external path with a low insertion loss filter shown in Figure 92, along with its R_F and R_G values, gives the following results:

- R_S for the I_{bn} term = 34 Ω || 249 Ω = 30 Ω. (dc source impedance for the filter design)
- R_F including the internal 18.5 kΩ resistor = 249 Ω || 18.5 kΩ = 245.7 Ω
- Resulting gain with the 130-Ω R_G element = 2.89 V/V

Table 6 shows the typical and worst-case output error terms. Note that a positive current out of the noninverting input gives a positive output offset term, whereas a positive current out of the inverting input gives a negative output term.

Table 6. Output Offset Voltage Contribution From Various Error Terms at 25°C

ERROR TERM	TYPICAL	MINIMUM	MAXIMUM	UNIT
$I_{bn} \times R_S \times A_V$	0.433	–0.43	1.29	mV
$V_{IO} \times A_V$	±2.89	–34.68	34.68	mV
$I_{bi} \times R_F$	±1.22	–9.83	9.83	mV
Total error	–3.67 to +4.54	–44.94	45.8	mV

The input offset voltage dominates the error terms. The worst-case numbers are calculated by adding the individual errors algebraically, but is rarely seen in practice. None of the OPS input dc error terms are correlated. To compute output drift numbers, use the same gains shown in Table 6 with the specified drift numbers.

The OPS PATHSEL control responds extremely quickly with low-switching glitches, as shown in Figure 86. For this test, the D2S input is set to GND, and the output of the D2S is connected to the external OPS input. The PATHSEL switch is then toggled at 10 MHz. The results show the offset between the internal and external paths as well matched.

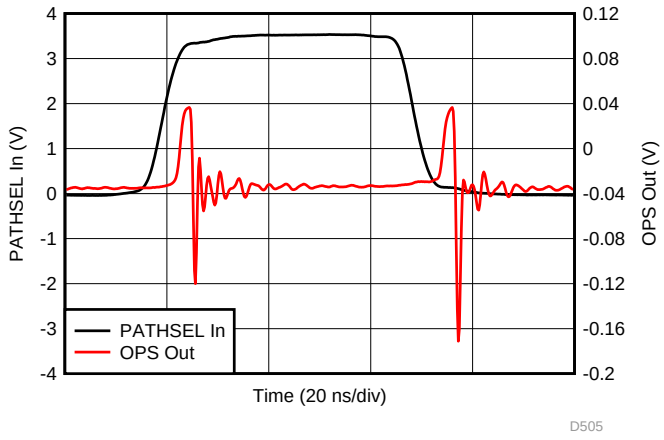


Figure 86. OPS Path-Select Switching Glitch

The OPS includes a disable feature that reduces power consumption from approximately 21 mA to 2.4 mA. The logic controls are intended to be ground-referenced regardless of the power supplies used. The logic reference (GND, pin 7) is normally grounded and also provides a connection to the internal 18.5-kΩ resistor on pin 9 (default bias to pin 7). Operating in a single-supply configuration with $–V_{CC}$ at GND and the external OPS input (pin 9) floated, places pin 9 internally at $–V_{CC}$ = GND. Driving the external OPS input (pin 9) from a source within the operating range overrides the bias to $–V_{CC}$. However, if the application requires pin 9 to be floated in a single-supply operation, consider centering the voltage on pin 9 with an added 18.5-kΩ external resistor to the $+V_{CC}$ supply.

If the disable feature is not needed, simply float or ground DISABLE (pin 10) to hold the OPS in the enabled state. Increasing the voltage on the DISABLE pin greater than 1.3 V disables the OPS and reduces the current to approximately 2.4 mA. If the OPS is unused in the application, it can be disabled by tying pin 10 to $+V_{CC}$, even up to the maximum operating supply of 15.8 V in a single-supply design.

Do not move the logic threshold away from those set by the logic ground at pin 7. If a different logic swing level is required, and pin 7 is biased to a different voltage, be sure the source can sink the typical 280 µA coming out of pin 7. Also recognize that the 18.5-kΩ bias resistor on the external OPS input (pin 9) is connected to pin 7 voltage internally.

As shown in Figure 56, the OPS enables in approximately 100 ns from the logic threshold at 1.0 V while disabling to a final value in approximately 500 ns.

9.3.3.2 OPS Harmonic Distortion (HD) Performance

The OPS in the THS3217 provides one of the best HD solutions available through high power levels and frequencies. Figure 31 and Figure 32 show the swept-frequency HD2 and HD3, where the second harmonic is clearly the dominant term over the third harmonic. Typical wideband CFA distortion is reported only through 2-V_{PP} output while Figure 31 and Figure 32 provide sweeps at 5 V_{PP} and 8 V_{PP} into a 100-Ω load. These curves normally show a 20-dB per decade rise with frequency due to loop-gain roll-off. At the highest 8-V_{PP} swing, the onset of slew rate limited HD is seen at approximately 40 MHz. The required output signal slew rate at 8 V_{PP} and 40 MHz is 4 V_{PEAK} × 2π × 40 MHz = 1000 V/µs. The output signal requires 1/5 of the available slew rate that will take the HD2 off the 20-dB per decade rate in the –50-dBc operating region shown. A slight shift in the HD3 slope is also seen around 40 MHz for 8-V_{PP} output in Figure 32.

The distortion performance is extremely robust as a function of R_{LOAD} (see Figure 33 and Figure 34). Normally, heavier loads degrade the distortion performance, as seen for the HD3 in Figure 34. However, the HD2 actually improves slightly going from a 200-Ω load to a 100-Ω load.

One of the key advantages offered by the CFA design in the OPS is that the distortion performance holds approximately constant over gain, as seen in the full-path distortion measurements of Figure 7 and Figure 8. Here, the D2S provides a fixed gain of 2 V/V driving a 200-Ω interstage load and using the internal path to drive the OPS at gains from 1.5 V/V to 10 V/V. Holding the loop-gain approximately constant by adjusting the feedback R_F value with gain results in vastly improved performance versus a voltage-feedback-based design.

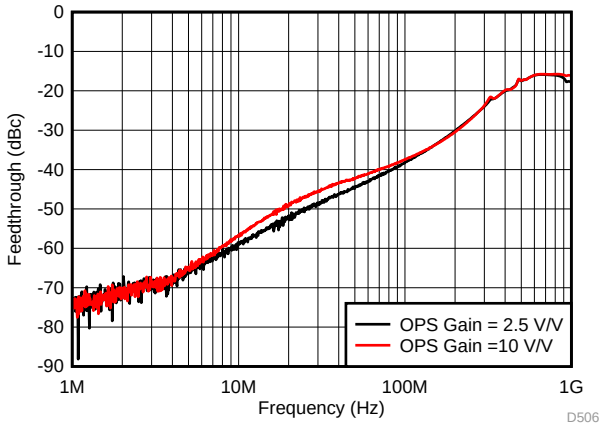
Testing a 5-V_{PP} output from the OPS with the supplies swept from the minimum ±4 V to ±7.5 V in Figure 35 and Figure 36 show:

1. The 1.5-V headroom on ±4-V supplies and ±2.5-V output voltage results in degraded performance. At the lower supplies, target lower output swings for improved linearity performance.
2. The HD2 does not change significantly with supply voltages above ±5 V. The HD3 does improve slightly at higher supply-voltage settings.

From these plots at ±7.5-V supplies, a 5-V_{PP} output into 100-Ω load shows better than –60-dBc HD2 and HD3 performance through 50 MHz. This exceptional performance is available with the OPS configured as a standalone amplifier. Combining this performance with the D2S stage (see Figure 3 and Figure 4) degrades the distortion due to the D2S and OPS harmonics combining in phase, and internal coupling between the stages. With the D2S and OPS running together at a final 5-V_{PP} output and 50 MHz, the HD2 drops to –50 dBc, and HD3 to –58 dBc on ±6-V supplies. Lower output swings for the combined stages provide much lower distortion. The 2-V_{PP} output curves on Figure 3 and Figure 4 show –57 dBc for HD2, and a remarkable –76 dBc for HD3 at 50 MHz.

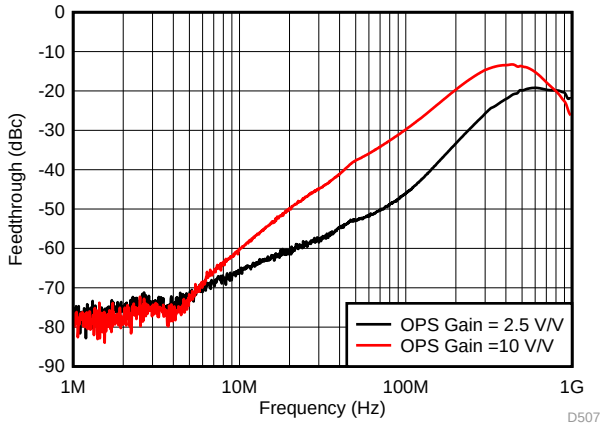
9.3.3.3 Switch Feedthrough to the OPS

The OPS has two logic control pins, giving four combinations of states; therefore, various feedthrough effects must be considered. Figure 57 and Figure 58 show the feedthrough of the switches with the OPS disabled. With the OPS enabled, the signal feedthrough from the deselected input to the OPS output is shown in Figure 87 and Figure 88 at different closed-loop OPS gains. The results are shown for a 100-mV_{PP} signal at the deselected input and are not normalized to the gain of the OPS. Adding a low-pass filter between the DAC and the D2S inputs helps reduce the feedthrough at higher frequencies.



PATHSEL < 0.7 V,
100-mV_{PP} signal to VIN (pin 9)

Figure 87. Forward Feedthrough With OPS Enabled, Internal Path Selected



PATHSEL > 1.3 V,
100-mV_{PP} signal to VREF (pin 14) with D2S inputs grounded

Figure 88. Forward Feedthrough With OPS Enabled, External Path Selected

9.3.3.4 Driving Capacitive Loads

The OPS can drive heavy capacitive loads very well as shown in Figure 43 to Figure 48. All high-speed amplifiers benefit from the addition of an external series resistor to isolate the load capacitor from the feedback loop. Not having the series isolation resistor often leads to response peaking and possibly oscillation. If frequency response flatness under capacitive load is the design goal, all CFA type amplifiers benefit by operating with slightly higher R_F values. Targeting a slightly higher feedback transimpedance increases the nominal phase margin before the capacitive load acts to decrease it. Using a higher RF value has the effect of achieving good flatness across a range of capacitive loads using lower external series resistor values. Although the suggested R_F and R_G values of Table 7 apply when driving a 100-Ω load, if the intended load is capacitive (for example, a passive filter with a shunt capacitor as the first element, another amplifier, or a Piezo element), use the values reported in Table 7 as a starting point. The values in Table 7 were used to generate Figure 43 and Figure 44. The results come from a nominal total feedback transimpedance target of 405 Ω (versus 351 Ω used for Table 4), and includes the internal 18.5-kΩ resistor in the design. Table 7 finds the least error to target gain in the selection of standard resistor values, and limits the minimum R_G to 20 Ω. The gains calculated here put 18.5-kΩ in parallel with the reported external standard value R_F.

Table 7. Suggested R_F and R_G Over Gain When Driving a Capacitive Load

TARGET GAIN (V/V)	BEST R_F (Ω)	BEST R_G (Ω)	CALCULATED GAIN		GAIN ERROR (%)
			(V/V)	(dB)	
1.5	348	681	1.501	3.529	0.077
2	332	324	2.011	6.070	0.575
2.5	309	205	2.491	7.927	–0.361
3	287	143	2.987	9.506	–0.420
3.5	267	105	3.520	10.930	0.565
4	249	82.5	3.992	12.024	–0.200
4.5	226	63.4	4.535	13.131	0.776
5	205	51.1	4.979	13.943	–0.419
5.5	178	39.2	5.505	14.815	0.085
6	158	31.6	5.961	15.506	–0.652
6.5	137	24.9	6.460	16.204	–0.621
7	121	20.0	7.004	16.907	0.058
7.5	130	20.0	7.451	17.444	–0.652
8	140	20.0	7.948	18.005	–0.652
8.5	154	20.5	8.457	18.544	–0.509
9	162	20.0	9.041	19.124	0.452
9.5	174	20.5	9.426	19.486	–0.780
10	182	20.0	10.034	20.030	0.341

As the capacitive load or amplifier gain increases, lower series resistor values can be used to hold a flat response (see Figure 43). See Figure 44 for the measured SSBW shapes for various capacitive loads configured with the suggested series resistor from the output of the OPS and the R_F and R_G values suggested in Table 7 for a gain of 2.5 V/V. This measurement includes a 200-Ω shunt resistor in parallel with the capacitive load as a measurement path.

Figure 45 and Figure 46 demonstrate the OPS harmonic distortion performance when driving a range of capacitive loads. These show suitable performance for large-signal, piezo-driver applications. If voltage swings higher than 12 V_{PP} are required, consider driving the OPS output into a step-up transformer. The high peak-output current for the OPS supports very fast charging edge rates into heavy capacitive loads, as shown in the step response plots (see Figure 47 and Figure 48). This peak current occurs near the center of the transition time driving a capacitive load. Therefore, the I × R drop to the capacitive load through the series resistor is at a maximum at midtransition, and back to zero at the extremes (low dV/dT points).

9.3.4 Digital Control Lines

The THS3217 provides two logic input lines that provide control over the input path to the OPS and the OPS power disable feature; both are referenced to GND (pin 7). The control logic defaults to a logic-low state when the pins are externally floated. Pin 7 must have a dc path to some reference voltage for correct operation. Float the two logic control lines to enable the OPS and select the internal path connecting the D2S internal output to the OPS noninverting input. Figure 89 shows a simplified internal schematic for either logic control input pin.

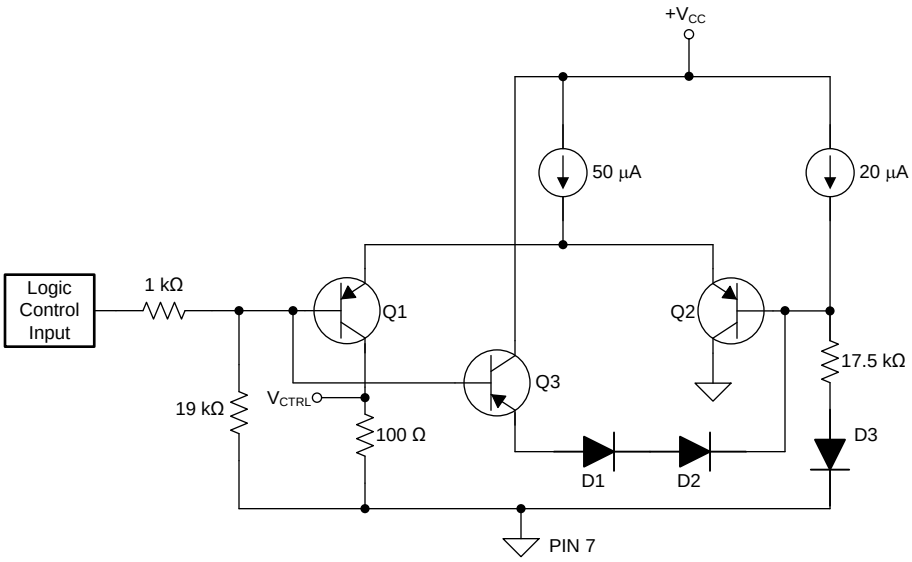


Figure 89. Logic Control Internal Schematic

The Q2 branch of the differential pair sets up a switch threshold approximately 1 V greater than the voltage applied to pin 7 (GND). If the control input is floating or < 0.7 V, the differential-pair tail current diverts to the 100-Ω detector load, and results in an output voltage (V_{CTRL}, shown in Figure 89) that activates the desired mode. The floated pin default voltage is the PNP base current into the 19-kΩ resistor. As the control pin voltage rises above 1.3 V, the differential-pair current is completely diverted away from the 100 Ω side, thus switching states.

This unique design allows the logic control inputs to be connected to a single-supply as high as 15.9 V, in order to hold the inputs permanently high, while still accepting a low ground-referenced logic swing for single-supply operation. The NPN transistor (Q3) and two diodes (D1 and D2) act as a clamp to prevent large voltages from appearing across the differential stage.

When the OPS is disabled, both input paths to the OPS are also opened up regardless of the state of PATHSEL (pin 4).

9.4 Device Functional Modes

Any combination of the three internal blocks can be used separately, or in various combinations. The following sections describe the various functional modes of the THS3217.

9.4.1 Full-Signal Path Mode

The full-signal path from the D2S to the OPS is available in various options. Three options are described in the following subsections.

9.4.1.1 Internal Connection With Fixed Common-Mode Output Voltage

The most basic operation is to ground the VREF pin, and use the internal connection from the D2S to the OPS to provide a differential to single-ended, high-power driver. Figure 90 shows the characterization circuit used for the combined performance specifications.

Device Functional Modes (continued)

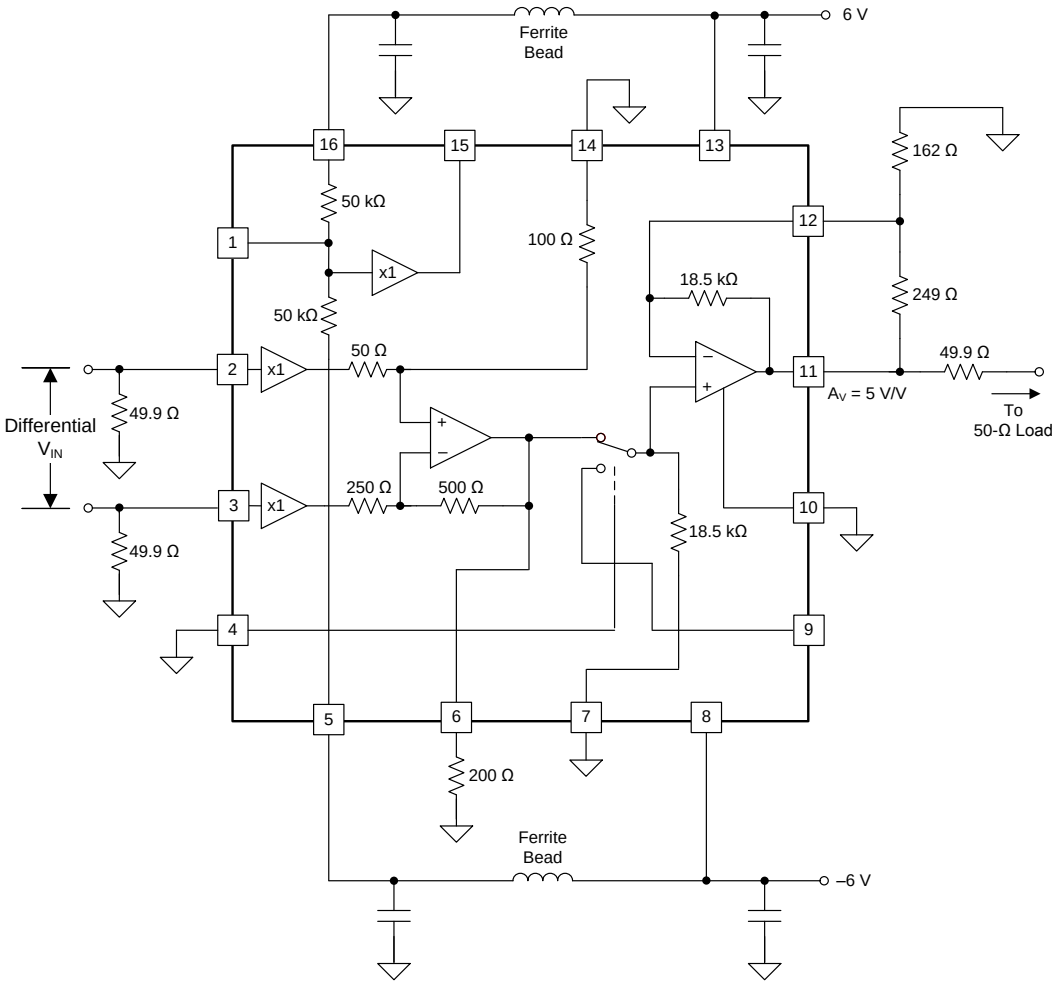


Figure 90. Differential to Single-Ended, Gain of 5-V/V Configuration

This configuration shows the test circuit used to generate Figure 1. Some of the key features in this basic configuration include:

1. The power supplies are brought into the OPS first, then back to the input stage through a π-filter comprised of a ferrite bead and local decoupling caps on –VCC2 and +VCC2, pins 5 and 16, respectively (see the *Power Supply Recommendations* section for more information).
2. The two logic lines are grounded. This logic configuration (with pin 7 grounded) selects the internal path from the D2S to OPS, and enables the OPS.
3. The external I/O pins of the midscale buffer are left floating.
4. The VREF pin is grounded, thus setting the D2S output common-mode voltage at VO1 (pin 6) to ground.
5. The D2S external output is loaded with a 200-Ω resistor to ground. Lighter loading on the VO1 pin (versus the 100 Ω used to characterize the D2S only) results in increased frequency response peaking. Heavier loading degrades the D2S distortion performance.
6. The external OPS input at pin 9 is left floating. However, it is internally tied to ground by the internal 18.5-kΩ resistor.
7. The feedback resistor in the OPS is set to the parallel combination of the external 249-Ω resistor and the internal 18.5-kΩ resistor. This 245.7-Ω total R_F with the 162-Ω R_G resistor gives a gain of approximately 2.5 V/V (7.98 dB) in the OPS stage
8. The input D2S gives a gain of 2 V/V (6 dB), and along with the 2.5 V/V (7.98 dB) from the OPS, gives an overall gain of 5 V/V (13.98 dB) with > 700 MHz of SSBW (see Figure 1).

Device Functional Modes (continued)

9.4.1.2 Internal Connection With Adjustable Common-Mode Output Voltage

The simplest modification to this starting configuration is using the midscale buffer to drive the VREF pin with either a dc or ac source into VMID_IN (pin 1), shown in Figure 91.

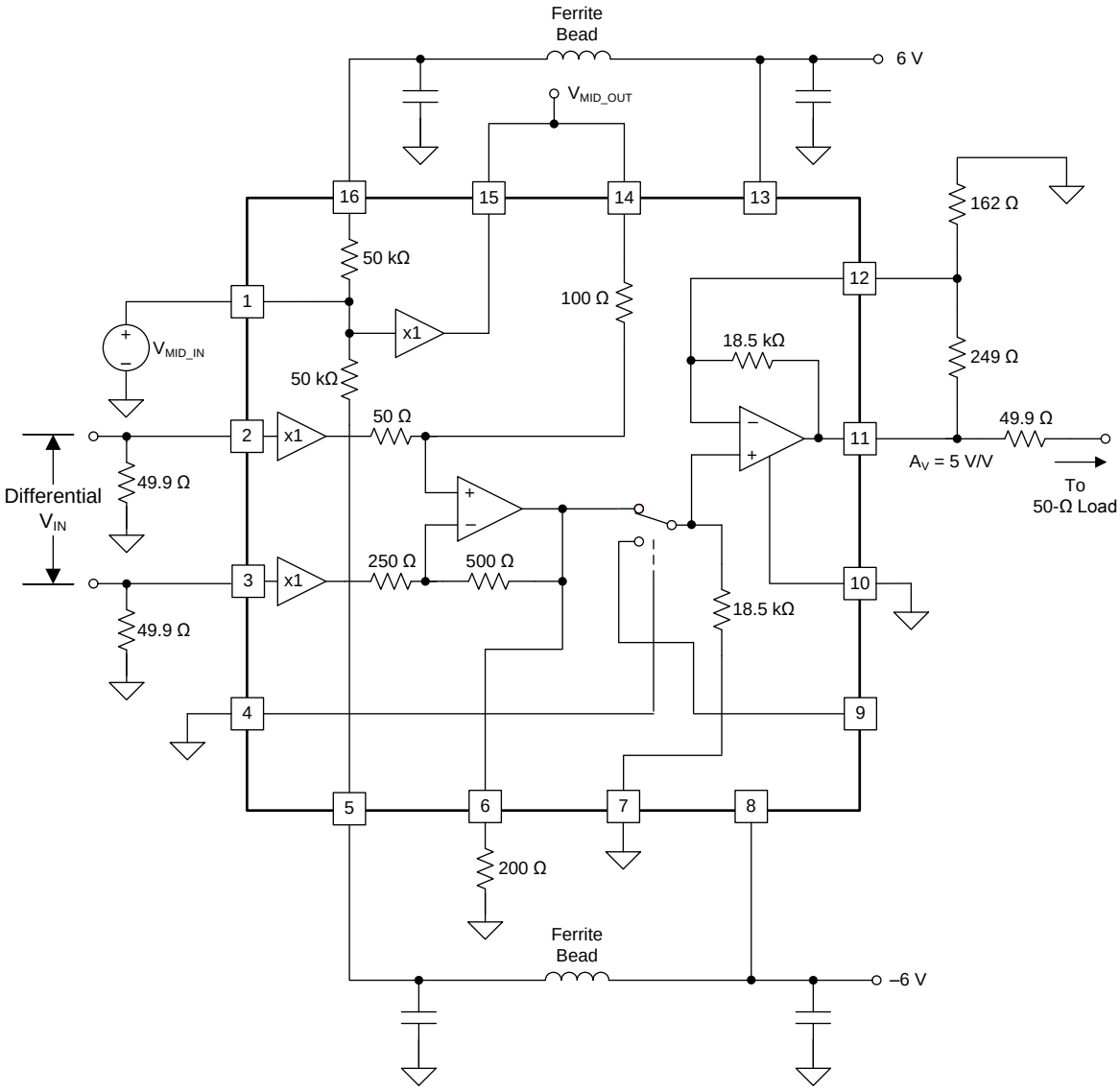


Figure 91. Differential to Single-Ended, Gain of 5-V/V Configuration With VREF Driven by the Midscale Buffer

The VREF input can be used to offset the output of the D2S that will then be amplified by the OPS. The total dc offset at the output of the OPS can also be corrected by adjusting the voltage at VMID_IN (pin 1). The on-chip midscale buffer can be used as a low-impedance source to drive the correction voltage to the VREF pin. A wideband small-signal source can also be summed into this path with a gain of 1 V/V to the D2S output pin. Figure 49 shows the midscale buffer to have an extremely flat response through 100 MHz for < 100-mV_{PP}swings, while 1 V_{PP} can be supported through 80 MHz with a flat response.

From this point on, the diagrams are simplified to not show the power-supply elements. However, the supplies are required by any application, as described in the *Application and Implementation* section.

Device Functional Modes (continued)

9.4.1.3 External Connection

In the configuration shown in Figure 92, the bias to PATHSEL (pin 4) is changed in order to select the external input of the OPS. The external D2S output drives a low insertion loss, third-order Bessel filter. The filter in this example is designed with a low frequency insertion loss of 1.2 dB and f_{-3dB} = 140 MHz, and results in an additional insertion loss of 1 dB at 100 MHz. The OPS gain is slightly increased to recover the filter loss, in order to give an input to output gain of 5 V/V. Using an interstage filter between the D2S and the OPS improves the step response by reducing the overshoot.

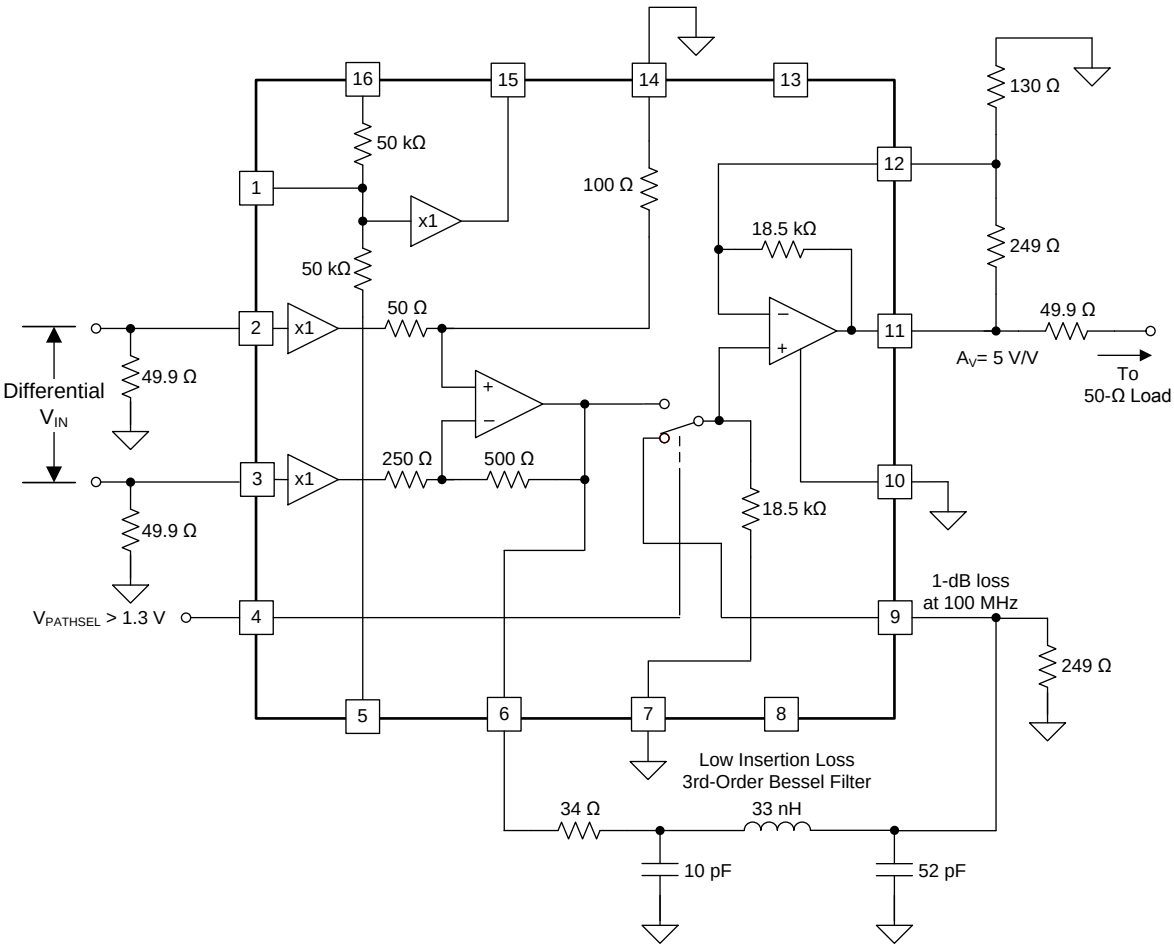


Figure 92. External Path Configuration With Interstage Low-Pass Filter

Device Functional Modes (continued)

9.4.2 Dual-Output Mode

The D2S stage can also be used to directly drive a doubly-terminated line, as shown in Figure 93. In addition, the OPS amplifies the internal D2S output by 5 V/V. The internal path to the OPS is selected with PATHSEL (pin 4) at ground, and the OPS gain is increased to 5 V/V. A 2-V_{PP} output at VO1 produces a 10-V_{PP} output at VOUT (pin 11). This 10-V_{PP} swing requires higher supply operation to provide sufficient headroom in the OPS output stage in order to preserve signal integrity. A power supply of ±7.5 V provides adequate headroom.

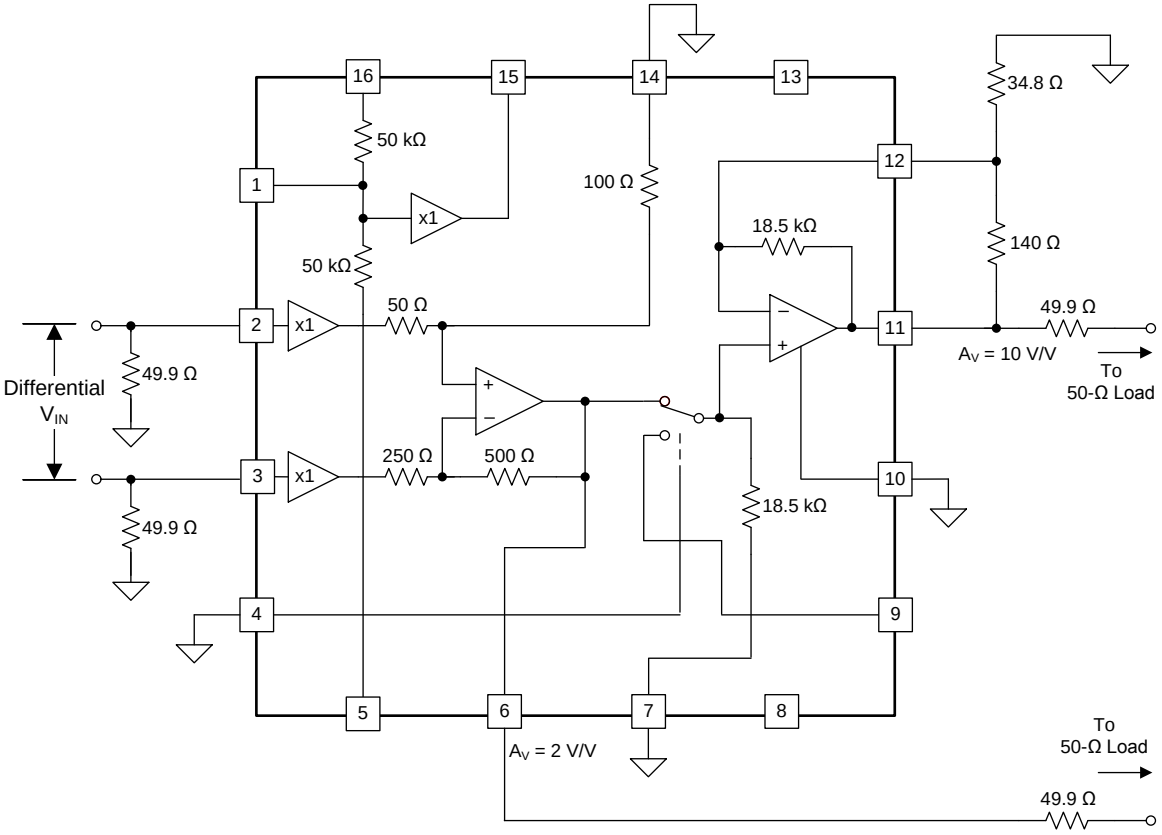


Figure 93. Dual-Output Mode

A simple modification to the circuit in Figure 93 is to disable the OPS, and switch to the external input path by taking both logic lines (pin 4 and pin 10) high. The D2S output at VO1 is then used either directly or through a filter to an even higher power driver like the ±15-V THS3091.

Device Functional Modes (continued)

9.4.3 Differential I/O Voltage Mode

Having two amplifiers available also allows a simple differential I/O implementation with independent output common-mode control, as shown in Figure 94. In this configuration, the D2S provides one side of the differential output, while simultaneously driving the OPS configured in an inverting gain of –1 V/V to provide the differential output on the other side. The output at VMID_OUT biases the external noninverting input, VIN+ (pin 9). This circuit configuration places the differential input to the output filter at a common-mode voltage, V_{MID_OUT}.

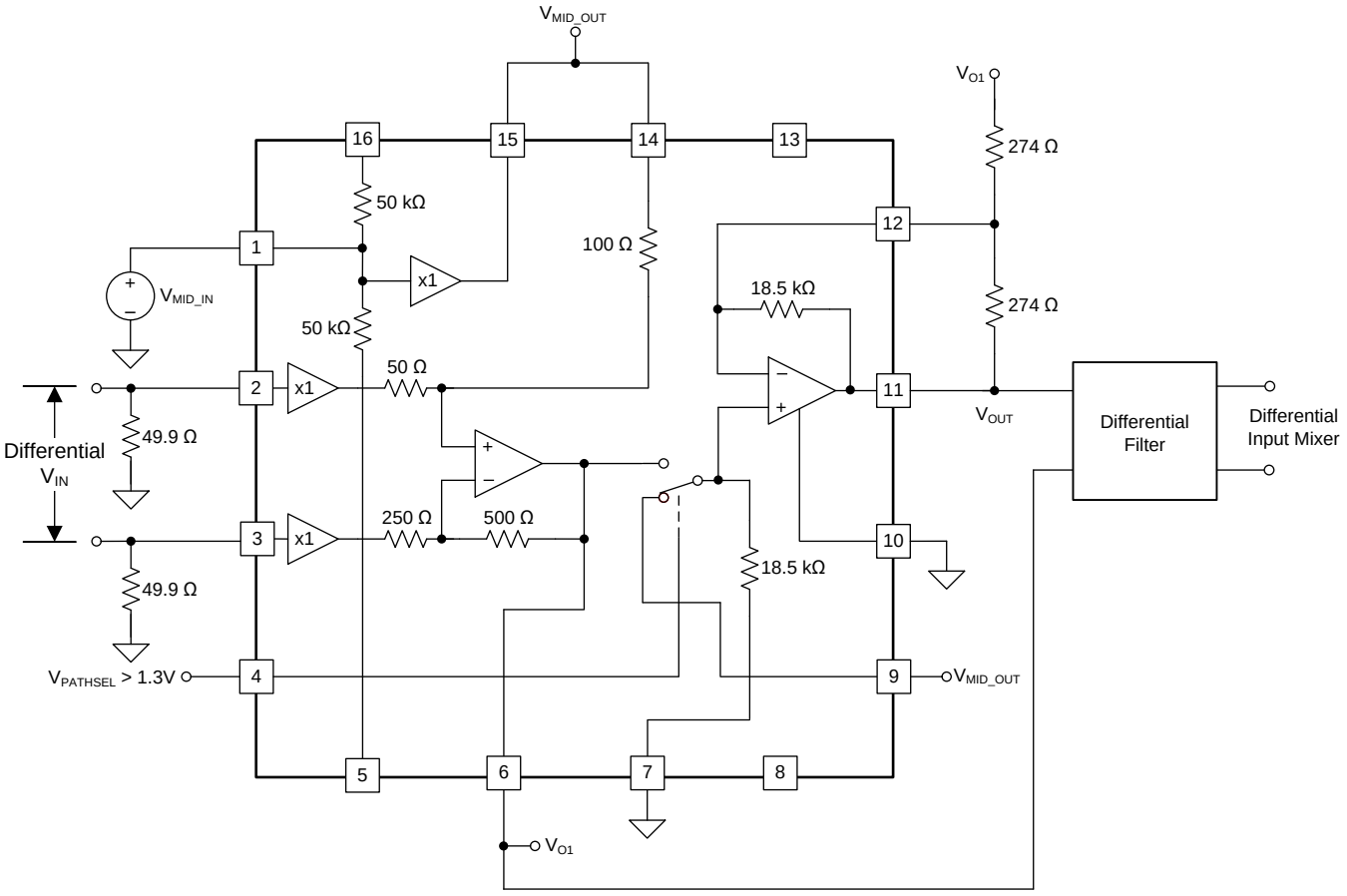


Figure 94. Differential I/O Configuration With Independent Output Common-Mode Voltage Control

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Typical Applications

The five example designs presented show a good, but not comprehensive, range of the possible solutions that the THS3217 provides. Numerous more configurations are clearly possible to the creative designer.

10.1.1.1 High-Frequency, High-Voltage, Dual-Output Line Driver for AWGs

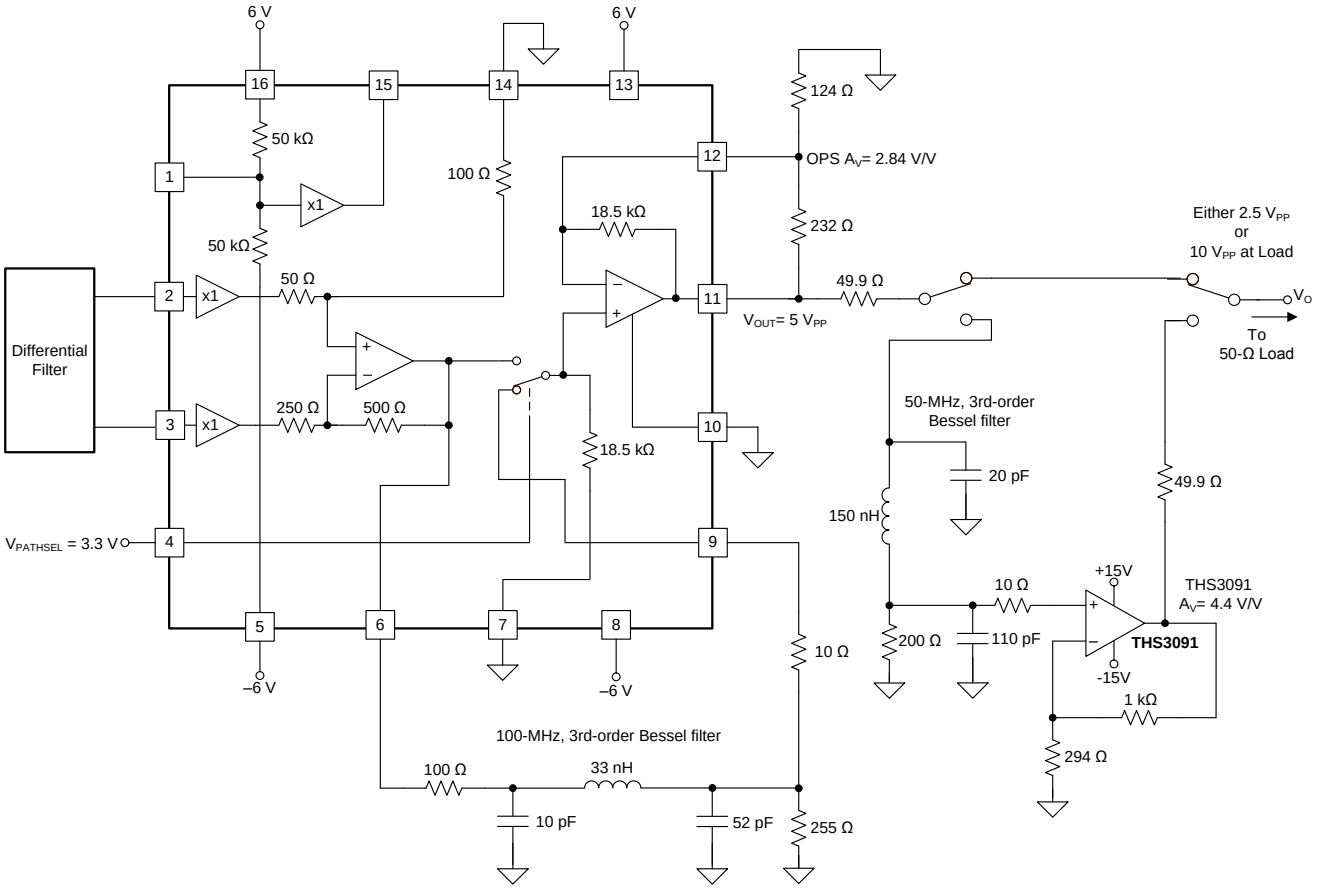


Figure 95. Dual-Channel Design: 5 V_{PP} at THS3217 Output and 20 V_{PP} at THS3091 Output

10.1.1.1.1 Design Requirements

For this design example, use the parameters listed in Table 8 as the input parameters.

Table 8. Dual-Output Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
High-frequency, THS3217 channel	5-V_{PP}, 100-MHz bandwidth
High-voltage, THS3091 channel	20-V_{PP}, 40-MHz bandwidth

10.1.1.1.2 Detailed Design Procedure

The THS3217 is well suited for high-speed, low-distortion arbitrary waveform generator (AWG) applications commonly used in laboratory equipment. In this typical application, a high-speed, complementary-current-output DAC is used to drive the D2S. The OPS of the THS3217 easily drives a 100-MHz, 2.5-V_{PP} signal into a matched 50-Ω load. When a larger output signal is required, consider using the THS3091 as the final driver stage.

A passive RLC filter is commonly used on DAC outputs to reduce the high-frequency content in the DAC steps. The filtering between the DAC output and the input to the D2S reduces higher-order DAC harmonics from feeding into the internal OPS path when the external input path is selected. Feedthrough between the internal and external OPS paths increases with increasing frequency; however, the input filter rolls off the DAC harmonics before the harmonics couple to VOUT (pin 10) through the deselected OPS signal path. Figure 96 shows an example of a doubly-terminated differential filter from the DAC to the THS3217 D2S inputs at pins 2 and 3.The DAC is modeled as two, fixed, 10-mA currents and a differential, ac-current source. The 10-mA dc midscale currents set up the average common-mode voltage at the DAC outputs and D2S inputs at 10 mA × 25 Ω = 0.25 V_{CM}. The total voltage swing on the DAC outputs is 0 V to 0.5 V.

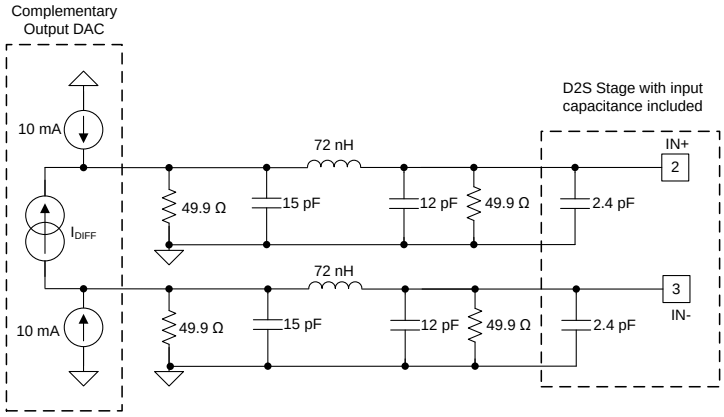


Figure 96. 200-MHz Butterworth Filter Between DAC and D2S Inputs

Some of the guidelines to consider in this filter design are:

1. The filter cutoff is adjusted to hit a standard value in the standard high-frequency, chip inductors kits.
2. The required filter output capacitance is reduced from the design value of 14.4 pF to 12 pF to account for the D2S input capacitance of 2.4 pF, as reported in the *D2S Electrical Characteristics* table.
3. The capacitor at the DAC output pins must also be reduced by the expected DAC output pin capacitance. The DAC output capacitance is often specified as 5 pF, but is usually much lower. Contact the DAC manufacturer for an accurate value.

Figure 97 shows the TINA-simulated filter response for the input-stage filter. The low-frequency 34-dBΩ gain is due to the 50-Ω differential resistance at the DAC output terminals. At 400 MHz, this filter is down 16 dB from the 50-Ω level; it is also very flat through 100 MHz.

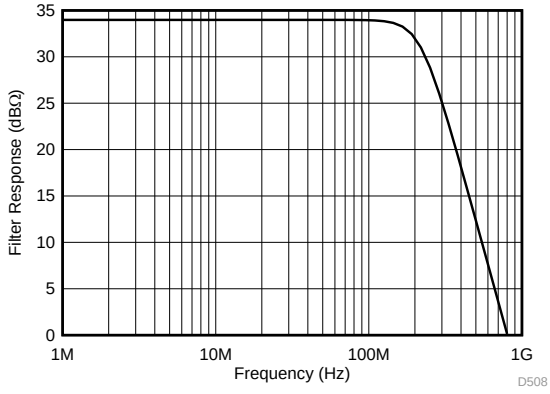


Figure 97. Simulated, Differential-Input Filter Response

In the example design of Figure 95, a 100-MHz, third-order Bessel filter is placed between the D2S output and the external OPS input. Another 50-MHz, third-order Bessel filter is placed at the input of a very-high, output-swing THS3091 stage. A double-pole, double-throw (DPDT) relay selects the THS3091 path when the internal OPS path is selected in the THS3217. Figure 95 shows this design. The key operational considerations in this design include:

1. When the external OPS path is selected, the 2-V_{PP} maximum D2S output swing experiences a 1.1-dB insertion loss from the interstage filter between VO1 (pin 6) and VIN+ (pin 9). A standard value inductor is used and the 255-Ω termination accounts for the internal 18.5-kΩ element. The 10-Ω resistor at pin 9 isolates the OPS input from the 52-pF filter capacitor. To recover the insertion loss and produce a maximum 5-V_{PP} output, the OPS gain is set to 2.84 V/V. When the interstage filter path is selected, the two DPDT relays pass the OPS output on directly from the 49.9-Ω output matching resistor to V_O, and the THS3091 can be disabled to conserve power.
2. To deliver 20 V_{PP} at the V_O output, select the THS3091 path. Select the internal OPS path to bypass the 100-MHz filter (1.1-dB insertion loss) in order to give a maximum 5.7-V_{PP} output at VOUT (pin 11). The two DPDT relays switch position, and the 49.9 Ω at the OPS output becomes part of the 50-MHz, third-order Bessel filter into the THS3091 stage. This filter has a 2-dB insertion loss requiring a gain of 4.4 V/V in the THS3091 to deliver 20 V_{PP} from the OPS output.
3. Figure 98 and Figure 99 show the frequency response and harmonic distortion performance of the dual output-voltage system. The frequency response is normalized to 0 dB to make bandwidth comparisons easier.

10.1.1.1.3 Application Curves

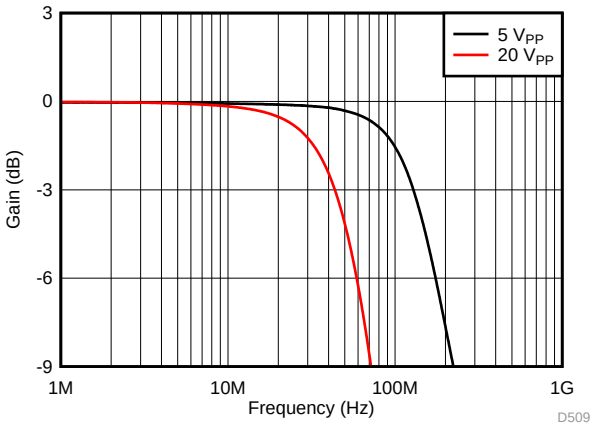


Figure 98. Frequency Response of the 5-V_{PP} and 20-V_{PP} Channels

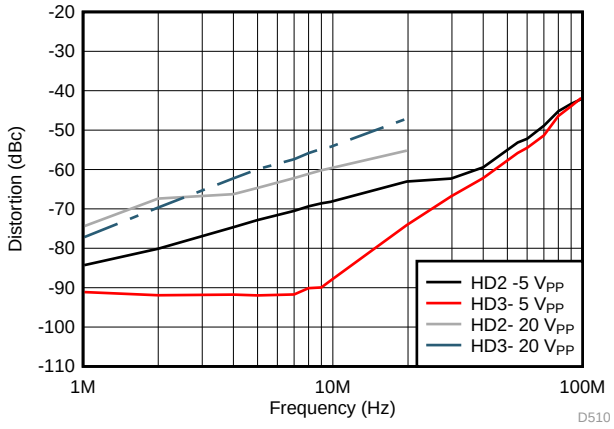


Figure 99. Harmonic Distortion Performance of the 5-V_{PP} and 20-V_{PP} Channels

10.1.1.2 High-Voltage Pulse-Generator

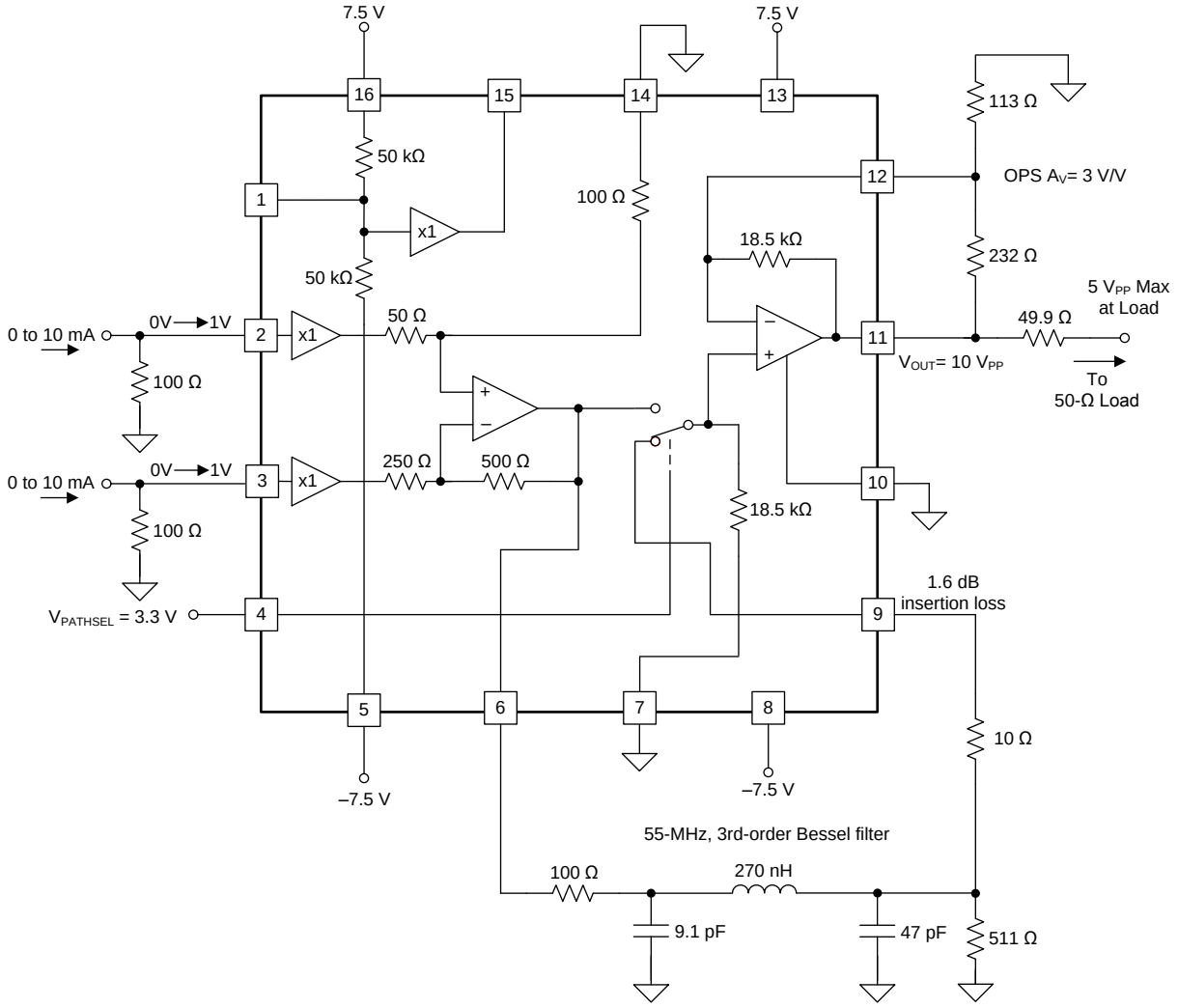


Figure 100. Driving a 10-V_{PP} Pulse Output into a 100-Ω Load With a 55-MHz External Interstage Bessel Filter

10.1.1.2.1 Design Requirements

To design a high-voltage, high-speed pulse generator with minimum overshoot, use the parameters listed in Table 8 as the input parameters.

Table 9. Pulse-Generator Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Power supply	±7.5 V
Pulse frequency	10 MHz
Pulse output voltage	10 V_{PP}

10.1.1.2.2 Detailed Design Procedure

Figure 100 shows an example design using the THS3217 to deliver a 10-V_{PP} maximum voltage from a DAC input, and includes an example external, third-order, interstage Bessel filter. Some of the salient considerations for this design include:

1. Reduced DAC output current with increased termination. This example is intended to be used with a current-sourcing DAC with an output compliance voltage of at least 1 V on a 0.5-V common-mode voltage. The 10-mA, single-ended, DAC tail current produces a 0-V to 1-V swing on each 100-Ω termination. The resulting 2-V_{PP} differential DAC signal produces a higher SNR signal at the THS3217 inputs.
2. The midscale buffer is not used. The VREF pin is grounded to set the inputs to a 4-V_{PP} ground-centered maximum output swing at VO1 (pin 6). The external input to the OPS is selected by setting PATHSEL to 3.3 V (anything over 1.3 V is adequate, or tie this pin to +V_{CC} for fixed, external-path operation).
3. The interstage Bessel filter is –0.3-dB flat through 20 MHz, with only 1.6 dB of insertion loss. The filter is designed to be low insertion-loss with relatively high resistor values. The filter uses standard inductor values. The capacitors are also standard-value, and slightly off from the exact filter solution. The final resistor to ground is designed for 500 Ω, but increased here to a standard 511 Ω externally to account for the internal 18.5-kΩ resistor on the external OPS input pin to GND. To isolate the last 47-pF filter capacitor from the OPS input stage, a 10-Ω series resistor is added close to the pin 9 input.
4. The filter adds 1.6 dB of insertion loss that is recovered, to achieve a 10-V_{PP} maximum output by designing the OPS for a gain of 3 V/V. Looking at Table 7, this gain setting requires the 232-Ω external R_F and 113-Ω R_G to ground for best operation.
5. For 10-V_{PP} maximum output, using the ±7.5-V supplies shown here gives adequate headroom in the OPS output stage. The operating maximum supply of 15.8 V requires a 5% tolerance on these ±7.5-V supplies.
6. The Bessel filter gives a very low overshoot full-scale output step-response, as shown in the 10-MHz, ±5-V square wave of Figure 102. The frequency response of the system is shown in Figure 101.

10.1.1.2.3 Application Curves

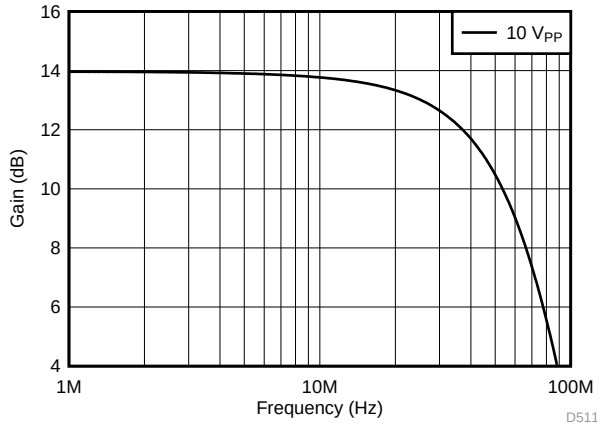


Figure 101. Frequency Response of the System With the Interstage Bessel Filter

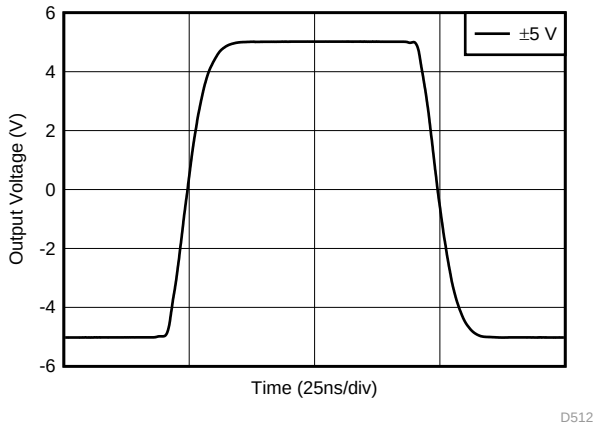


Figure 102. Pulse Response of the System With the Interstage Bessel Filter

10.1.1.3 Single-Supply, AC-Coupled, Piezo Element Driver

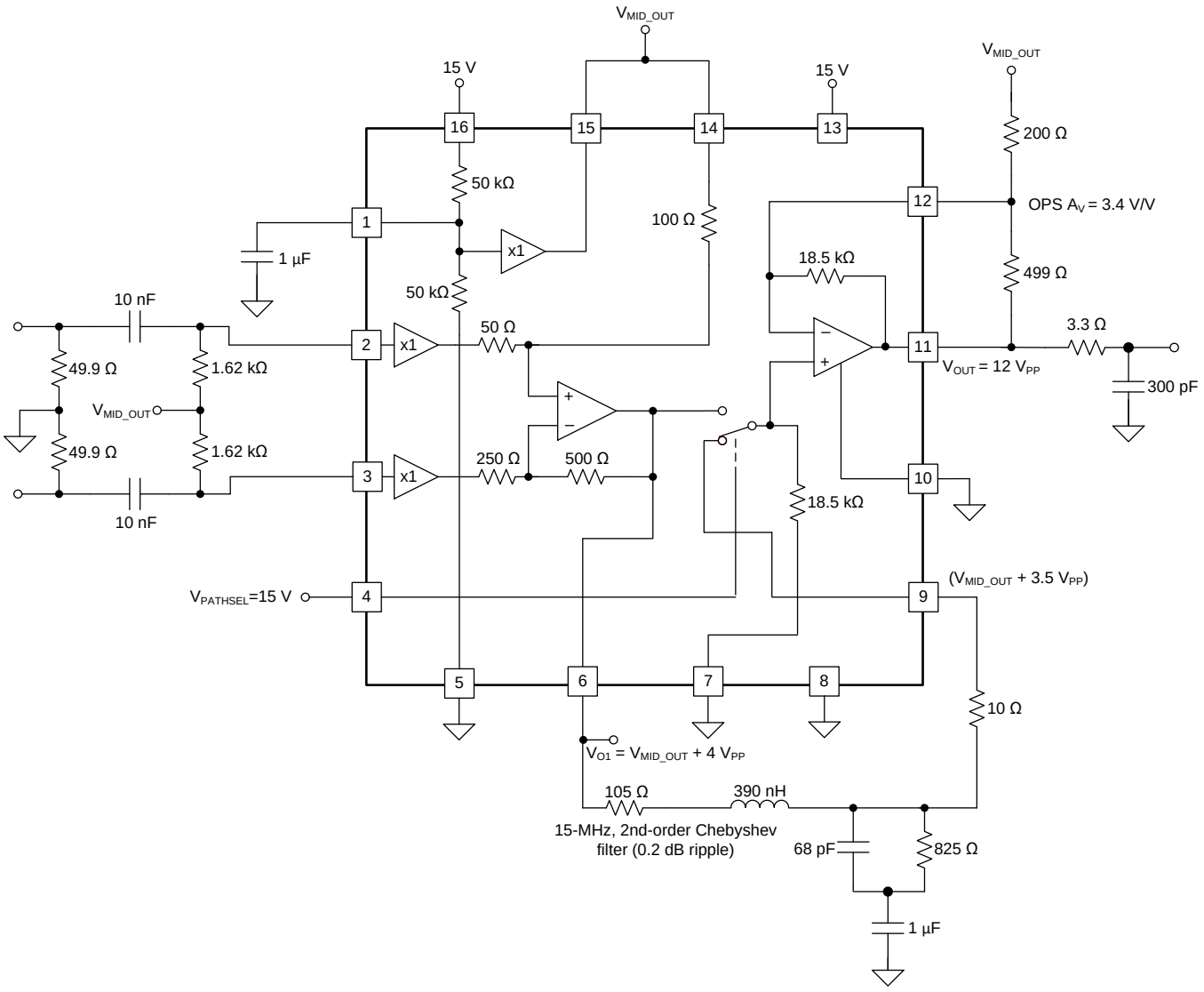


Figure 103. Single-Supply, Heavy Capacitive-Load Driving

10.1.1.3.1 Design Requirements

The very-high peak output current and slew rate of the THS3217 OPS make it particularly suitable for driving heavy capacitive loads, such as the piezo elements used in continuous wave (CW) applications that require high-amplitude, sinusoidal-type excitations. The driver is quickly disabled during the receive time when the output TR switch is moved to receive mode. Figure 103 shows an example design using the internal midscale buffer to bias all the stages to midsupply on a single 15-V design. There are many elements to this example that also apply to any single-supply application. The key points here are:

1. The differential DAC input signal is ac-coupled to the D2S input, and the termination resistors are scaled up and biased to midsupply using the output of the midscale buffer, VMID_OUT (pin 15). The 10-nF blocking capacitors before the 1.62 kΩ termination resistors set the high-pass pole at 10 kHz.
2. The internal divider resistors of the midscale buffer are decoupled using a 1-µF capacitor on VMID_IN (pin 1). Use of the capacitor improves both noise and PSRR through the reference buffer stage. In turn, the noise injected by the bias source is reduced at the various places the buffer output is used.
3. V_{MID_OUT} is also applied to the VREF input (pin 14) to hold the D2S output centered on the single 15-V supply. There is minimal dc current into VREF (pin 14) because the D2S input buffers operate at the same common-mode voltage, V_{MID_OUT}.

4. The D2S output is dc biased at midsupply and delivers two times the differential swing applied at its inputs. Assuming 2 V_{PP} at the D2S inputs implies 4 V_{PP} at the D2S output pins. Lower input swings are supported with the gain in the OPS adjusted to meet the desired output maximum.
5. The filter in Figure 103 is a 0.2-dB ripple, second-order Chebyshev filter at 15 MHz. If the desired maximum frequency is 12 MHz, for instance, this filter is attenuating the HD2 and HD3 out of the D2S by approximately 3 dB and 5 dB, respectively. Increased attenuation can be provided with higher-order filters, but this simple filter does a good job of band-limiting the high-frequency noise from the D2S outputs before the noise gets into the OPS stage.
6. The dc bias voltage at VO1 drives a small dc current into the 18.5-kΩ resistor to ground at the OPS external input, VIN+ (pin 9). The error voltage due to the bias current will level-shift the dc voltage at the OPS noninverting input through the 105-Ω filter resistor. This offset will be amplified by the OPS gain since its R_G element is referenced to the V_{MID} output with a dc gain of 3.4 V/V.
7. The logic lines are still referenced to ground in this single-supply application. The external path to the OPS is selected by connecting PATHSEL (pin 4) to $+V_{CC}$. DISABLE (pin 10) is grounded in this example in order to hold the OPS on. If the disable feature is required by the application, drive the OPS using a standard logic control driver. Note that the midscale buffer output still drives R_G and R_F to midsupply in this configuration with the OPS disabled.
8. The R_G element can be ac coupled to ground through a capacitor to operate at midsupply. Figure 103 shows the midscale buffer driving R_G, thus eliminating the need for an added capacitor. Using a blocking capacitor moves the dc gain to 1 V/V. The voltage on the external, noninverting input of the OPS sets the dc operating point. Use of a blocking capacitor also lightens the load on the midscale buffer output, and eliminates the bias on R_G when the OPS is disabled.
9. Piezo element drivers operate in a relatively low-frequency range; therefore, the OPS R_F is scaled up even further than the values suggested in Table 7. An increased R_F allows R_G to also be scaled up, thereby reducing the load on the midscale buffer, and allow a lower series output resistor to be used into the 300-pF capacitive load.
10. The peak charging current into the capacitive load occurs at the peak dV/dT point. Assuming a 12-MHz sinusoid at 12 V_{PP} requires a peak output current from the OPS of 6 $V_{PEAK} \times 2\pi \times 12$ MHz × 300 pF = 135 mA. This result matches the rated minimum peak output current of the OPS.

Using a very low series resistor limits the waveform distortion due to the I × R drop at the peak charging point around the sinusoidal zero crossing. The 135 mA through 3.3 Ω causes a 0.45-V peak drop to the load capacitance around zero crossing. The voltage drop across the series output resistor increases the apparent third harmonic distortion at the capacitive load. Figure 45 and Figure 46 show 10-V_{PP} distortion sweeps into various capacitor loads. The results shown in these figures are for the OPS only because the results set the harmonic distortion performance in this example.

10.1.1.4 Output Common-Mode Control Using the Midscale Buffer as a Level Shifter

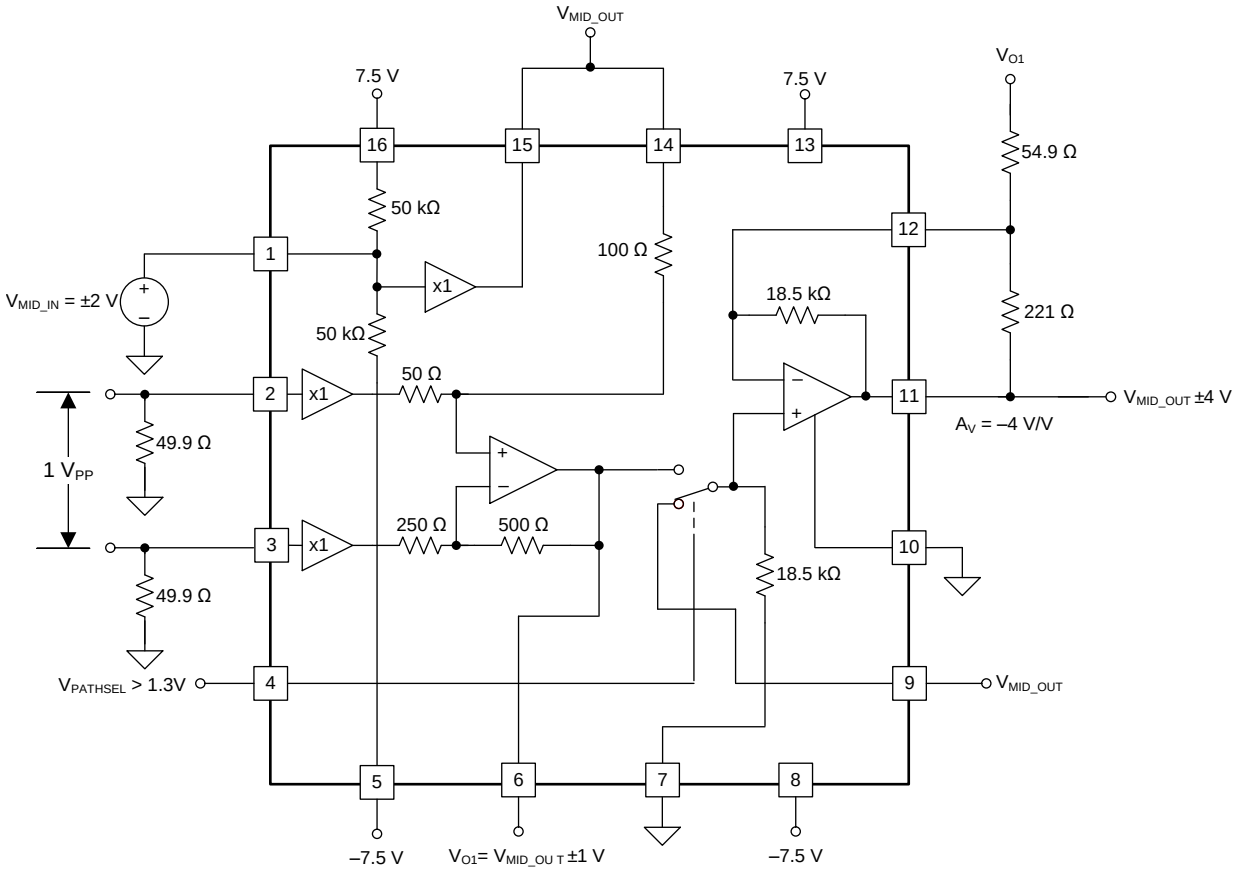


Figure 104. Adding an Output DC Offset Using the Midscale Buffer

10.1.1.4.1 Design Requirements

An easy way to insert a dc offset into the signal channel (without sacrificing any of the DAC dynamic range) is to apply the desired offset at VMID_IN and use it to bias VREF (pin 14) and VIN+ (pin 9). An example is shown in Figure 104. This example shows a relatively low maximum differential input of 1 V_{PP} on any compliance voltage required by the DAC. Other configuration options include:

1. The D2S output is offset using a dc input at VMID_IN (pin 1). Although shown here as ±2 V, the dc offset expands to ±3.5 V when using ±7.5-V supplies.
2. Connecting VMID_OUT to the VREF input places the D2S output at the dc offset voltage along with a gain of 2 V/V version of the differential input voltage. The stated range of ±2 V, along with the ±0.5 V out of the upper input buffer, requires a peak output current from VMID_OUT of 2.5 V / 150 Ω = 16.7 mA. This value is well below the rated minimum linear output current of 40 mA.
3. The dc offset voltage is then applied to the external OPS input. Connecting the circuit in this manner results in no additional dc gain between the D2S and OPS outputs, while it continues to retain the signal gain of the OPS configured as an inverting amplifier. The values of R_F and R_G in this application example are derived from Table 4. The OPS is setup for a gain of –4 V/V in this example. Using the resistor values from Table 4 results in the widest bandwidth for the OPS; however, the R_G = 54.9 Ω resistor presents a heavy load to the D2S output. In such cases, scaling up the resistors in the OPS helps reduce the loading on the D2S output at the expense of reduced OPS bandwidth.
4. No filtering is shown in this example; however, introducing filtering in the OPS R_G path is certainly possible. In such cases, the R_G element is also the filter termination resistor. Any filtering adds some insertion loss that can be recovered in the OPS stage.

10.1.1.5 Differential I/O Driver With independent Common-Mode Control

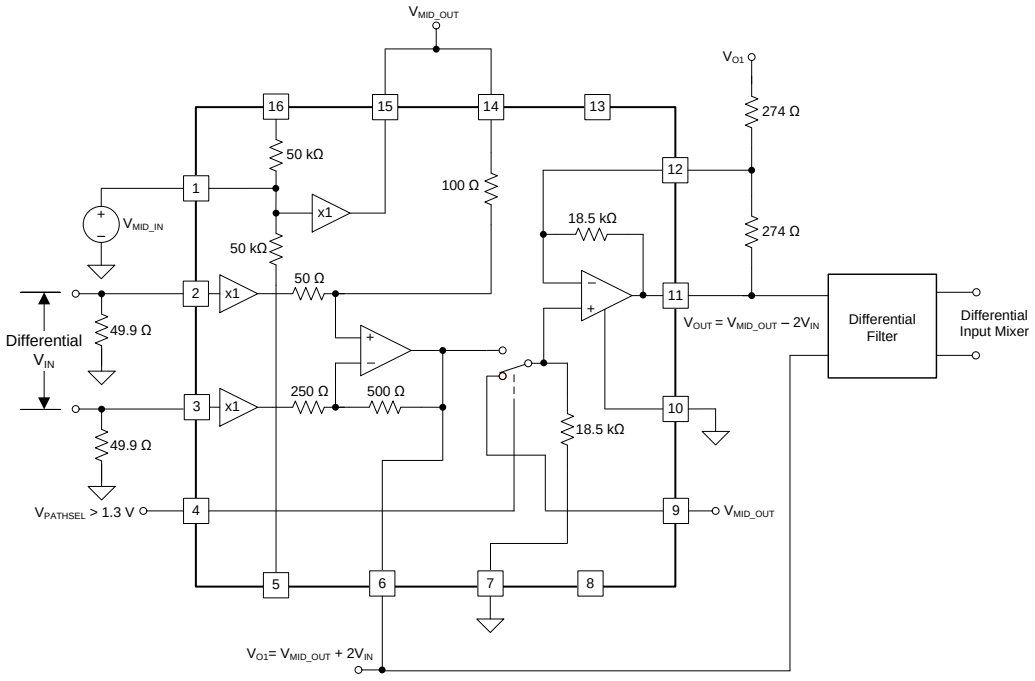


Figure 105. Differential I/O Line Driver

10.1.1.5.1 Design Requirements

Certain applications require the differential DAC output voltage to be level-translated from one common-mode (compliance) level to a differential output at a different common-mode level. The THS3217 performs this function directly using the very flexible blocks provided internally. Figure 105 shows an example of such an application, where the differential gain is always 4 V/V. The differential gain is fine-tuned down by setting the insertion loss in the differential post-filter. The considerations critical to this application include:

1. The input is dc-coupled with the appropriate termination impedance required by the DAC. Use a high-frequency, antialiasing filter at the input to limit DAC feedthrough in the deselected OPS internal input.
2. The output common-mode control is set with the voltage applied to the VMID buffer input at VMID_IN (pin 1). The circuit is configured so that the output at VMID_OUT (pin 15) drives both VREF (pin 14), in order to set the D2S dc output voltage, and VIN+ (pin 9).
3. The D2S output available at VO1 (pin 6) provides one side of the differential-output, and is dc-biased at V_{MID_OUT}. This VO1 also drives the R_G resistor for the OPS in an inverting gain of –1 V/V. The dc bias level at the R_G input and the V+ input of the OPS are the same voltage; therefore, no level shift through the OPS occurs. The OPS outputs an inverted version of the D2S output signal at the same common-mode voltage (V_{MID_OUT}). The wideband, differential signal with independent output common-mode voltage control can now be applied to a differential filter and on to the next stage.
4. Make sure that the differential filter only has differential resistors and capacitors. Termination resistors to ground level shift the input common-mode voltage, while differential resistors transfers the desired V_{MID_OUT} directly through the filter.
5. If the desired V_{MID_OUT} + differential signal combined clips in the OPS or D2S stages, offset the supplies to gain headroom. For instance, if a 5-V output common-mode voltage is required with a 10-V_{PP} differential signal, the OPS and D2S must deliver 2.5-V to 7.5-V output swings. The D2S has the higher headroom requirement at 1.55 V (max). Operating the THS3217 with –5 V and +10 V supplies stays within the rated maximum of 15.8 V total supply range, and provide adequate headroom for the positive offset swing requirement. Note that the logic lines are still referenced to GND by pin 7. Tying PATHSEL (pin 4) to $+V_{CC}$ holds this design in the external path mode required.

11 Power Supply Recommendations

The THS3217 typically operates on balanced, split supplies. The specifications and characterization plots use ±6 V in most cases. The full operating range for the THS3217 spans ±4 V to ±7.9 V. The input and output stages have separate supply pins that are isolated internally.

The recommended external supply configuration brings $\pm V_{CC}$ into the output stage first, then back to the input stage connections through a π-filter comprised of ferrite beads and added decoupling capacitors at +VCC2 (pin 16) and –VCC2 (pin 5). Figure 106 shows an example decoupling configuration.

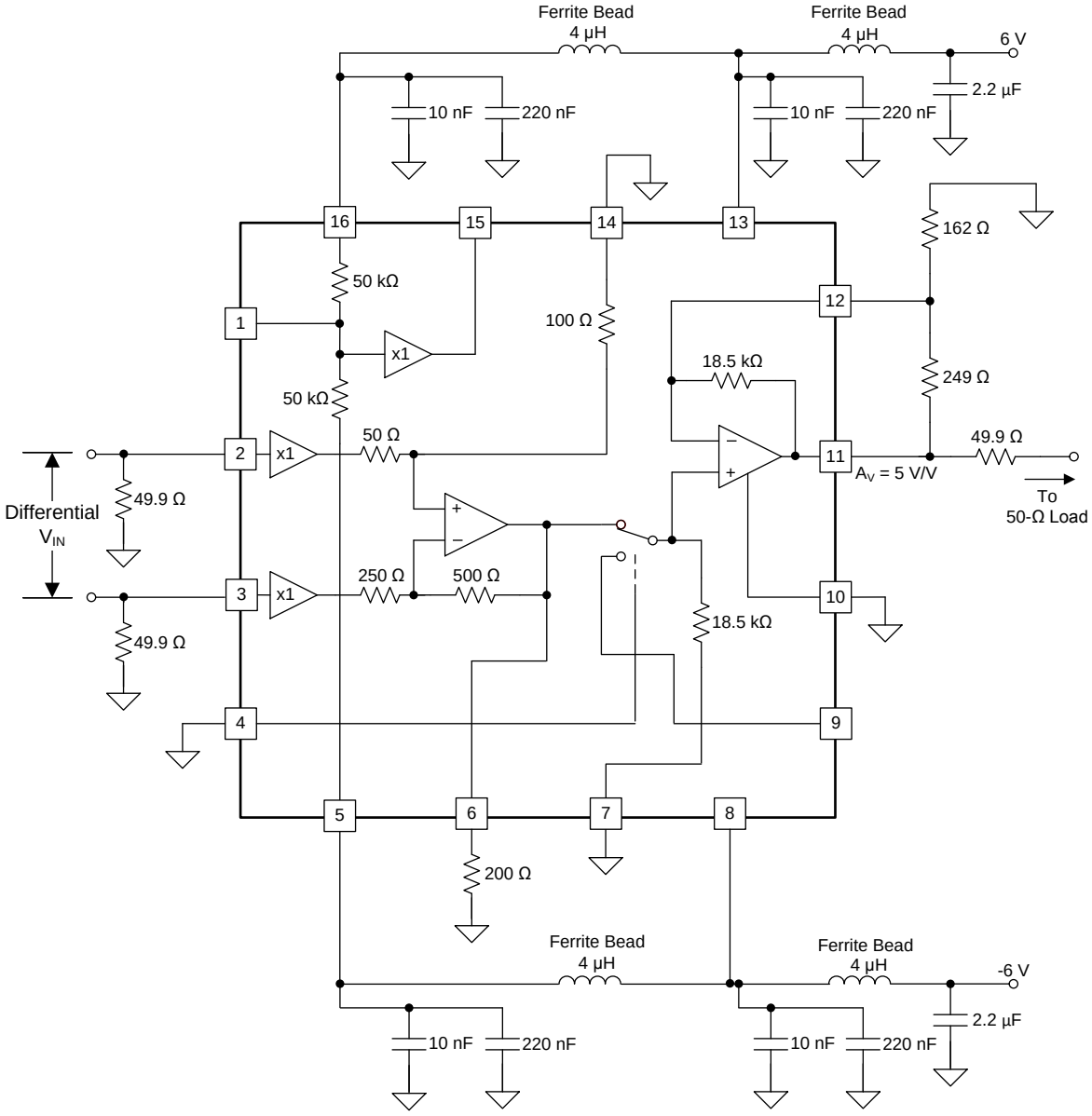


Figure 106. Recommended Power-Supply Configuration

The ferrite bead acts to break the feedback loop from the output stage load currents back into the D2S and midscale buffer stages. Operate the two positive supply pins and the two negative supply pins at the same voltage. Using separate sources on the two pins risks forward-biasing the on-chip parallel diodes connecting the two supply inputs together. +VCC1 (pin 13) and +VCC2 (pin 16) have two parallel diodes that are normally off if the voltage at the two pins are equal. The same is true for –VCC1 (pin 8) and –VCC2 (pin 5).

The THS3217 provides considerable flexibility in the supply voltage settings. The overriding consideration is always satisfying the required headroom to the supplies on all the I/O paths. The logic controls on PATHSEL (pin 4) and DISABLE (pin 10) are intended to operate ground referenced regardless of supplies used. The ground connection on pin 7 is used to set the reference.

Power savings are certainly possible by operating with only the minimum required supplies for the intended swings at each of the pins. For instance, consider an example design operating with a current-sinking DAC with the input common-mode voltage at 3 V, with an output swing at the D2S output of ±1 V. Looking at just the D2S stage under these conditions, the minimum positive supply is 3 V_{CM} + the maximum input headroom of 1.5 V to the positive supply, resulting in a minimum 4.5-V supply for this operation. The ±1-V output at VO1 (pin 6) along with the D2S output headroom sets the minimum negative supply voltage. The maximum 1.65-V headroom gives a possible minimum negative supply of –2.65 V. However, the minimum operating total of 8 V increases the negative supply to –3.5 V.

If the ±1-V swing is then amplified by the OPS, the output swing and headroom requirements set the minimum operating supply. For instance, if the OPS is operating at a gain of 2.5 V/V, the ±2.5-V output requires a maximum headroom of 1.4 V to either supply. Achieving a 1.4-V headroom requires a minimum balanced supply of ±3.9 V. However, the input stage overrides the positive side because the required minimum is 4.5 V, while the negative increases to –3.9 V. This example of absolute minimum supplies saves power. Using a typical 56-mA quiescent current for all stages, going to the minimum 8.4 V total across the device, uses 470 mW of quiescent power versus the 672 mW if a simple ±6-V supply is applied. However, ac performance degrades with the lower headroom. For more power-sensitive applications, consider adjusting the supplies to the minimum required on each side.

11.1 Thermal Considerations

The internal power for the THS3217 is a combination of its quiescent power and load power. The quiescent power is simply the total supply voltage times the supply current. This current is trimmed to reduce power dissipation variation and minimize variations in the ac performance. At a ±7.5-V supply, the maximum supply current of 57 mA dissipates 855 mW of quiescent power. The worst-case load power occurs if the output is at ½ the single-sided supply voltage driving a dc load. Placing a ±3.75-V dc output into 100 Ω adds another 37.5 mA × 3.75 V = 140 mW of internal power. This total of approximately 1 W of internal dissipation requires the thermal pad be connected to a good heat-spreading ground plane to hold the internal junction temperatures below the rated maximum of 150°C.

The thermal impedance is approximately 45 °C/W with the thermal pad connected. For 1 W of internal power dissipation there is a 45°C (approximate) rise in the junction temperature from ambient. Designing for the intended 85°C maximum ambient temperature results in a maximum junction temperature of 130°C.

12 Layout

12.1 Layout Guidelines

High-speed amplifier designs require careful attention to board layout in order to achieve the performance specified in the data sheets. Poor layout techniques can lead to increased parasitics from the board and external components resulting in suboptimal performance, and also instability in the form of oscillations. The THS3217 evaluation module (EVM) serves as a good reference for proper, high-speed layout methodology. The EVM includes numerous extra elements needed for lab characterization, and also additional features that are useful in certain applications. These additional components can be eliminated on the end system if not required by the application. General suggestions for the design and layout of high-speed, signal-path solutions include:

1. Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened on all of the ground and power planes around those pins. On other areas of the board continuous ground and power planes are preferred for signal routing with matched impedance traces for longer runs.
2. Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins. Higher value capacitors (2.2 µF) are required, but may be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Follow the power-supply guidelines recommended in the *Power Supply Recommendations* section.
3. Careful selection and placement of external components preserve the high-frequency performance of the THS3217. Use low-reactance type resistors. Surface-mount resistors work best, and allow a tighter overall layout. Keep the printed circuit board (PCB) trace length as short as possible. Never use wire-bound type resistors in a high-frequency application. The output pin and inverting input pins are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Place other network components, such as input termination resistors, close to the gain-setting resistors.
4. When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces. On differential lines, like those on the D2S inputs, match the routing in order to minimize common-mode noise effects and improve HD2 performance.
5. The input summing junction of the OPS is very sensitive to parasitic capacitance. Connect the R_G element into the summing junction with minimal trace length to the device pin side of the resistor. The other side of R_G can have more trace length if needed to the source or to ground. For best results, do not socket a high-speed part like the THS3217. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3217 directly onto the board.

12.2 Layout Example

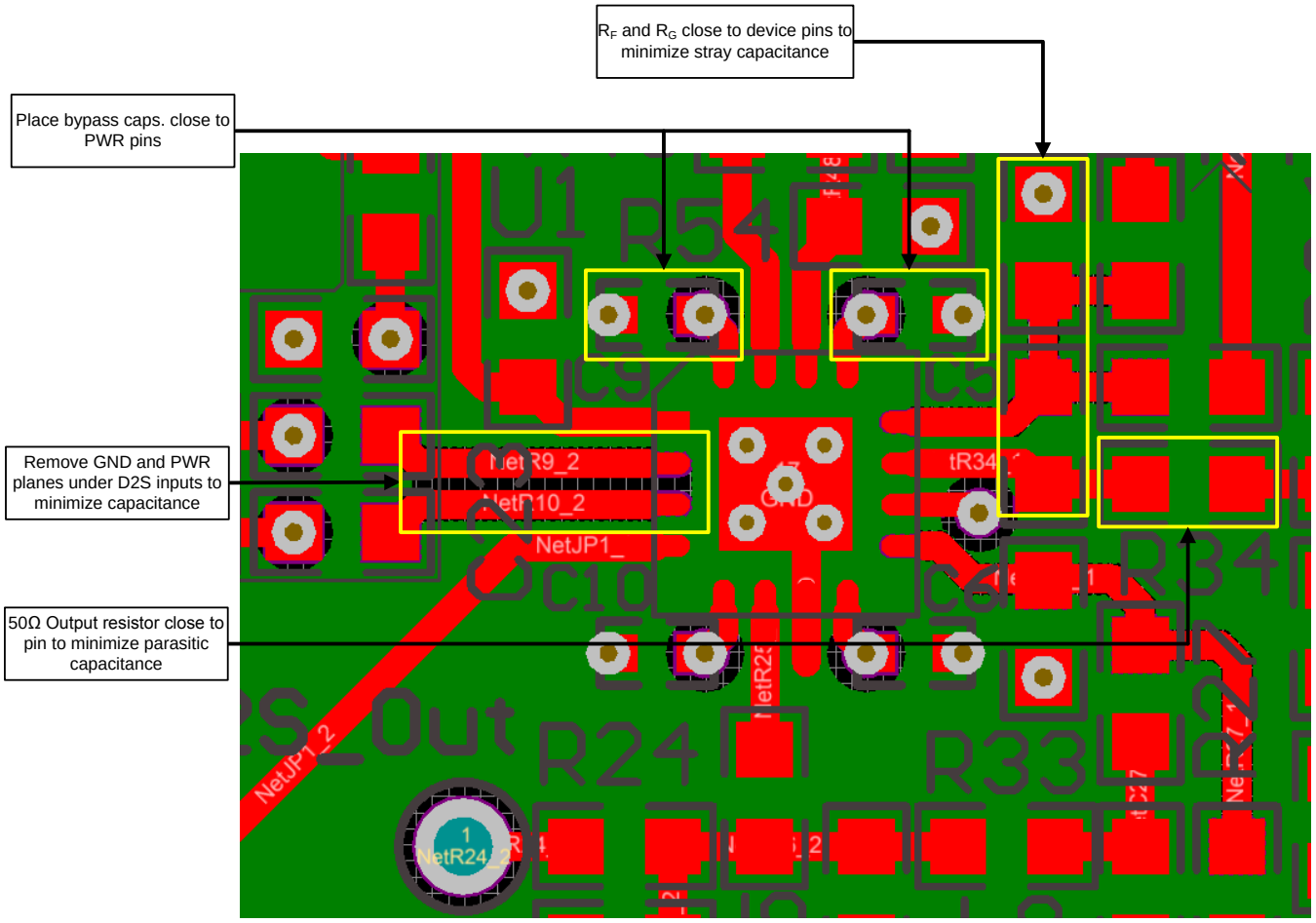


Figure 107. Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 开发支持

13.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

13.2 文档支持

13.2.1 相关文档

相关文档如下：

- 《THS3217EVM 用户指南》，SBOU161
- *《电压反馈运放与电流反馈运放》*，SLVA051
- *《电流反馈放大器的分析与补偿》*，SLOA021
- *《电流反馈放大器：审阅、稳定性分析以及 应用》*，SBOA081
- *《电流反馈放大器的稳定性处理》*，SBOA095

13.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3217IRGVR	ACTIVE	VQFN	RGV	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS3217 IRGV	Samples
THS3217IRGVT	ACTIVE	VQFN	RGV	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS3217 IRGV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

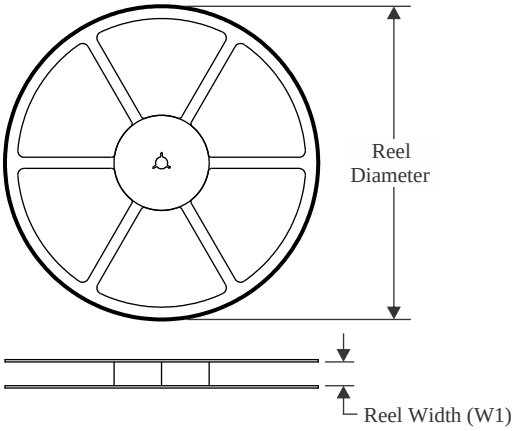
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

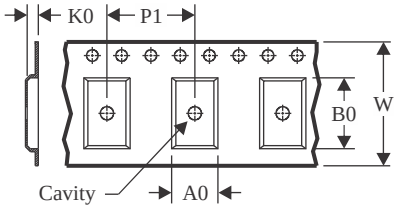
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

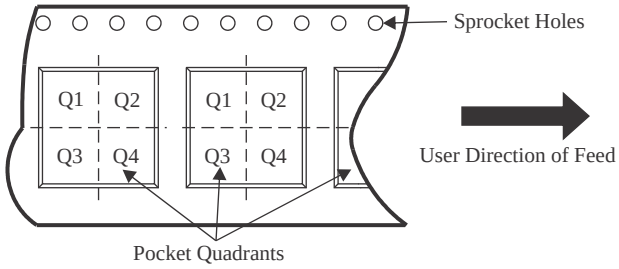


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

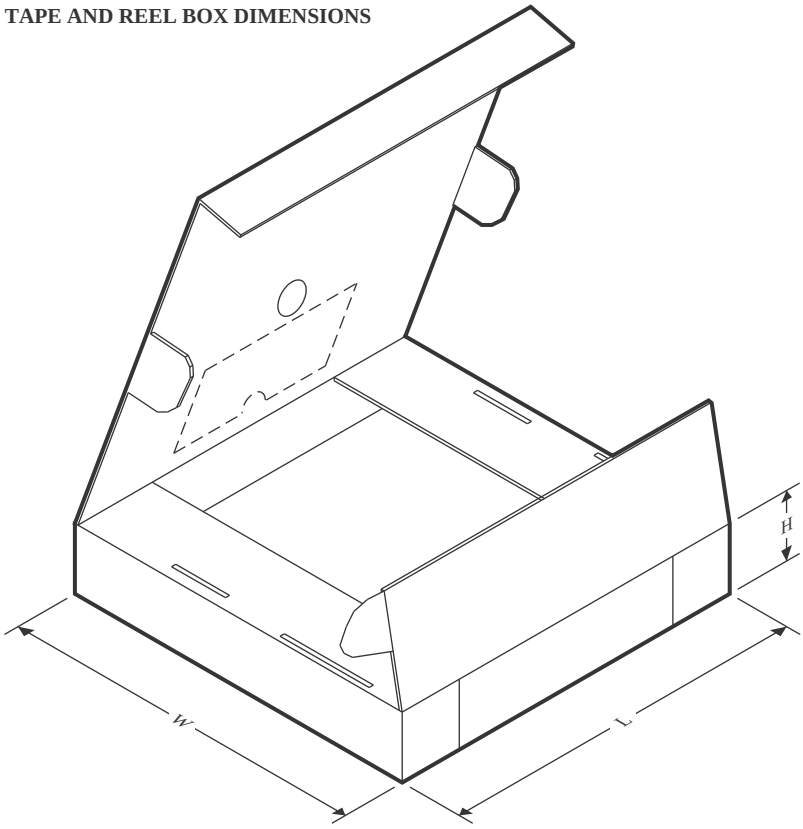
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3217IRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
THS3217IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3217IRGVR	VQFN	RGV	16	2500	346.0	346.0	33.0
THS3217IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

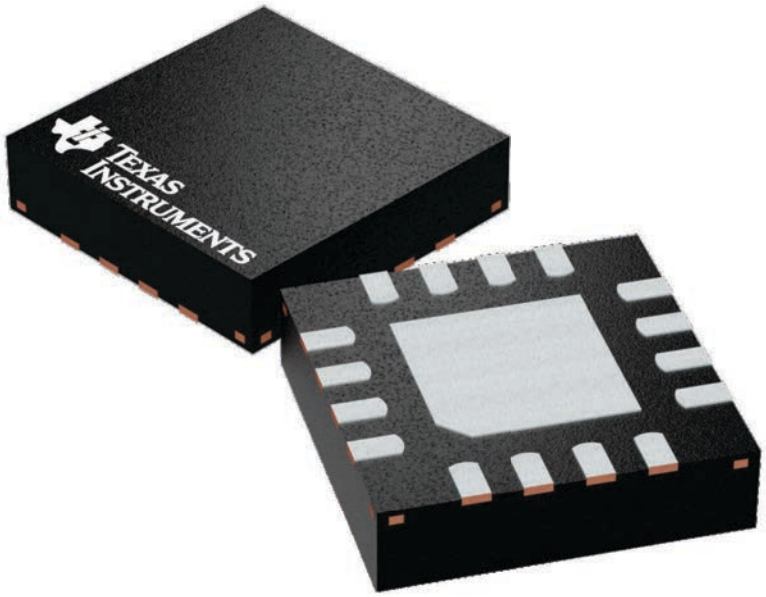
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

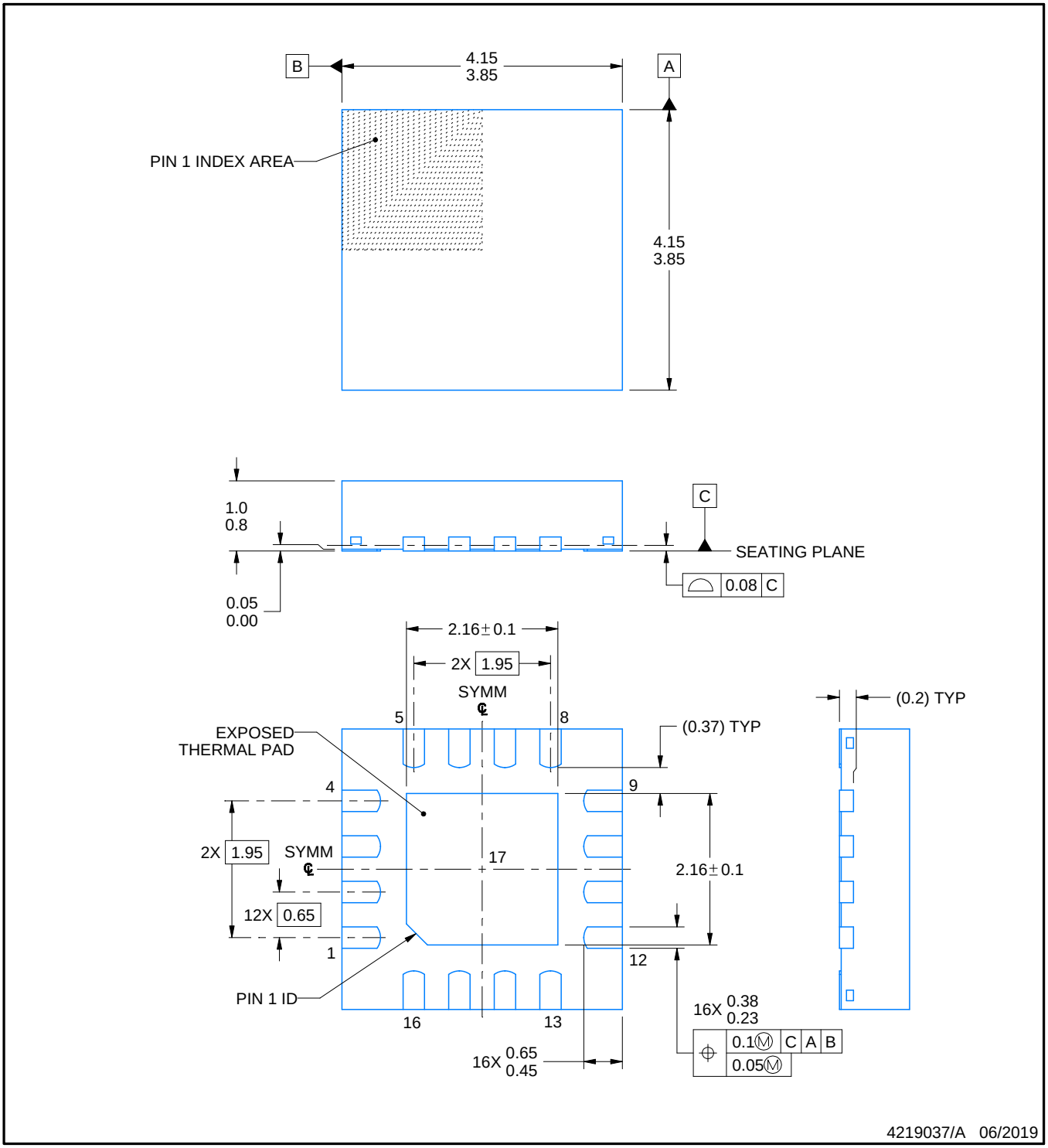
4224748/A

RGV0016A

PACKAGE OUTLINE

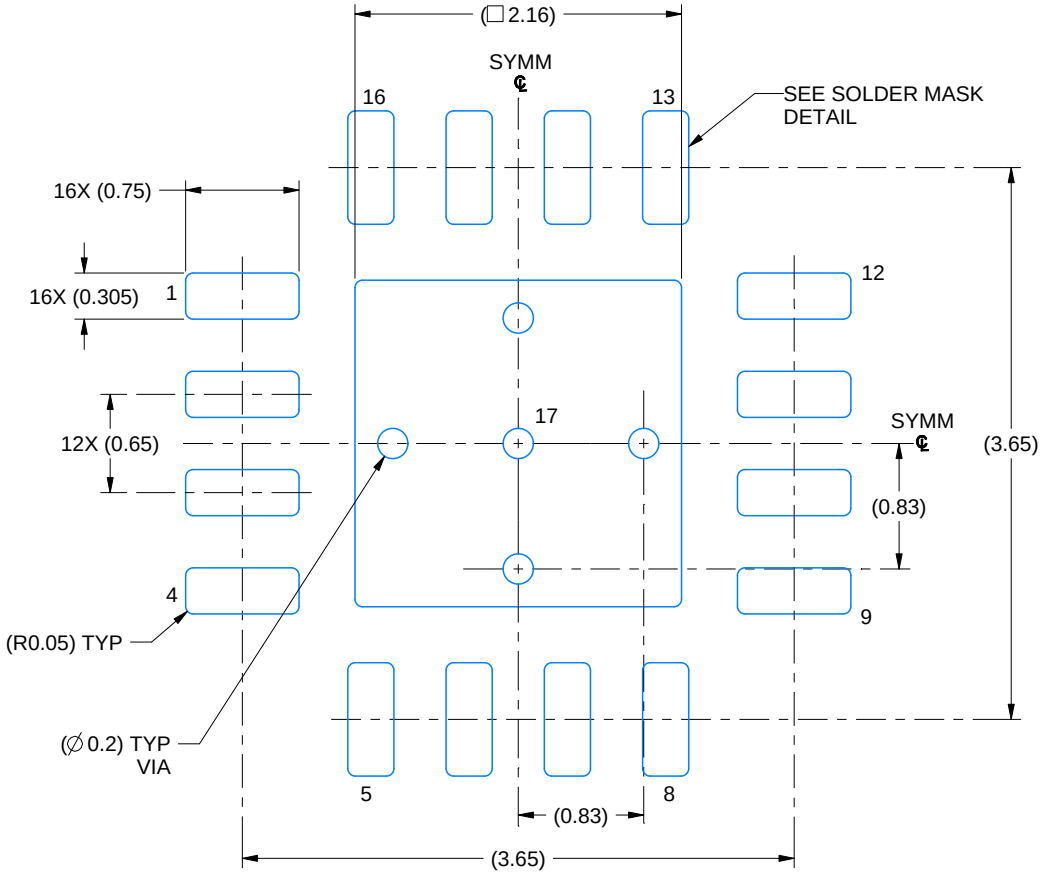
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

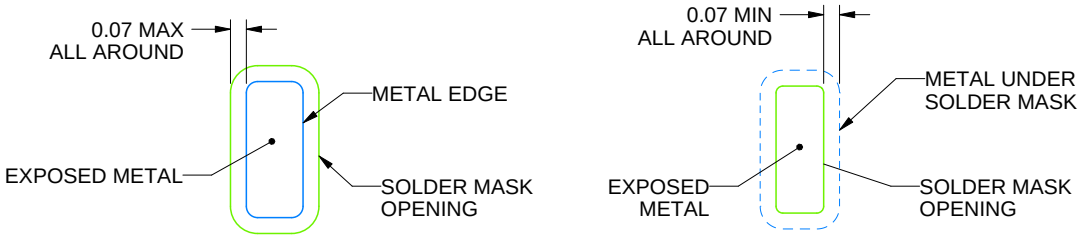


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

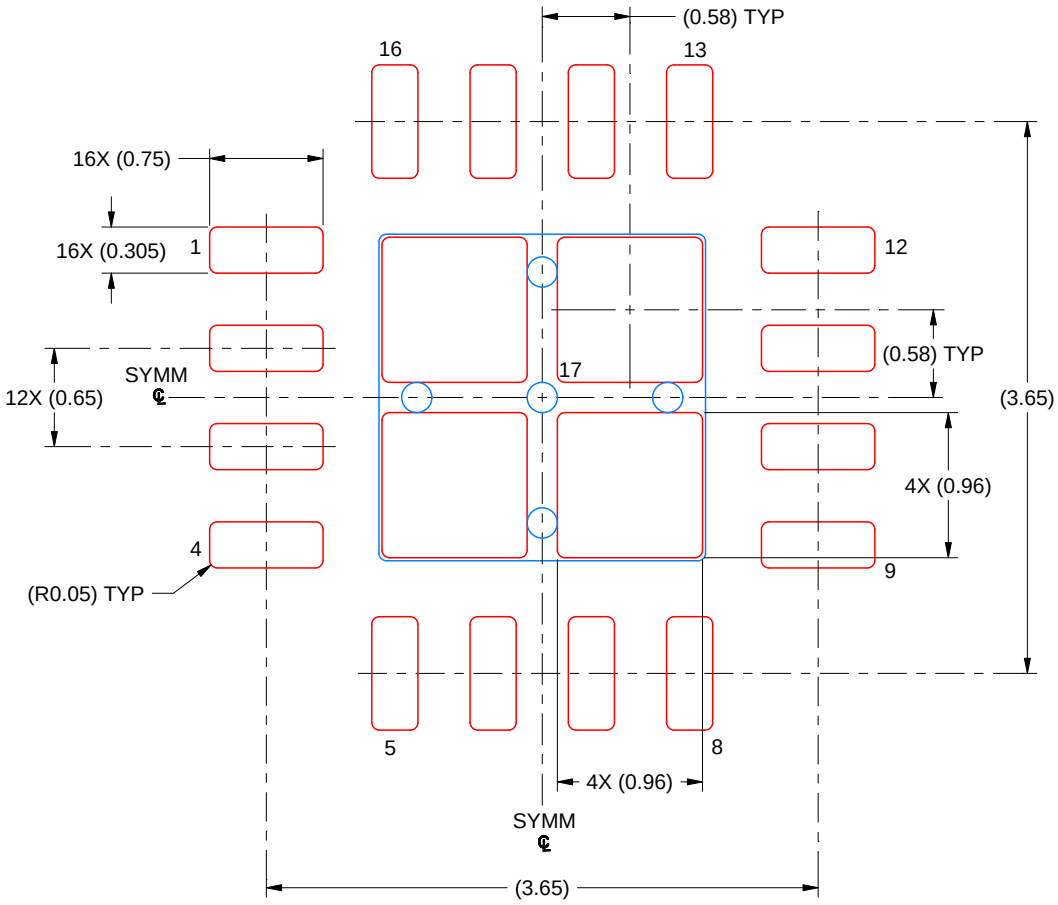
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219037/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219037/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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