

TLC3702-EP 双通道微功耗 LinCMOS 电压比较器

1 特性

- 受控基线
 - 一个封测厂，一个制造厂
- 工作温度范围为 -55°C 至 125°C
- 推挽 CMOS 输出在没有上拉电阻器的情况下驱动容性负载， $I_O = \pm 8\text{mA}$
- 功耗极低：5V 时典型值为 $100\mu\text{W}$
- 快速响应时间： $t_{PLH} = 2.7\mu\text{s}$ (典型值)，具有 5mV 过驱动
- 单电源运行：4V 至 16V
- 片上 ESD 保护

2 说明

TLC3702-EP 包含两个独立的微功耗电压比较器，这些比较器由单电源供电运行、并与现代 HCMOS 逻辑系统兼容。这些芯片在功能上与 LM339 类似，但使用二十分之一的功率来实现类似的响应时间。推挽式 CMOS 输出级直接驱动容性负载，无需使用功耗上拉电阻器即可实现规定的响应时间。消除上拉电阻器不仅可以降低功耗，还可以节省布板空间和元件成本。输出级也完全符合 TTL 要求。

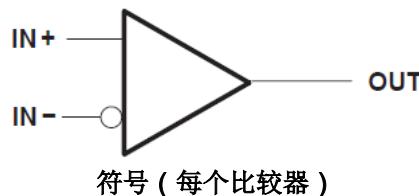
德州仪器 (TI) LinCMOS 工艺为标准 CMOS 工艺提供了高质量模拟性能。除了在不牺牲速度的情况下低功耗、高输入阻抗和低偏置电流等标准 CMOS 优势外，LinCMOS 工艺还在宽差分输入电压下提供极为稳定的输入失调电压。该特性旨在构建可靠的 CMOS 比较器。

器件信息

T _A	封装 (1)	可订购器件型号 (2)	正面标识
-55°C 至 125°C	SOP- D	TLC3702MDREP	3702ME

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 \times 宽) 为标称值，并包括引脚 (如适用)。



本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本 (控制文档)。

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Pin Configuration and Functions

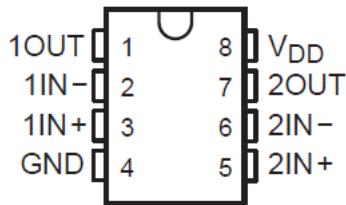


图 3-1. D Package (Top View)

表 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1 -	2	I	Inverting input pin of comparator 1
IN1 +	3	I	Noninverting input pin of comparator 1
V -	4	—	Negative (low) supply
IN2 +	5	I	Noninverting input pin of comparator 2
IN2 -	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V +	8	—	Positive supply

3 Specifications

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{DD}	Supply voltage range ⁽²⁾	-0.3	18	V
V_{ID}	Differential input voltage ⁽³⁾		$\pm V_{DD}$	V
V_I	Input voltage range	-0.3	V_{DD}	V
V_O	Output voltage range	-0.3	V_{DD}	V
I_I	Input current		± 5	mA
I_O	Output current (each output)		± 20	mA
	Total supply current into V_{DD}		40	mA
	Total current out of GND		40	mA
T_A	Operating free-air temperature range	-55	125	°C
	Storage temperature range	-65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground.

(3) Differential voltages are at IN+ with respect to IN-.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4	5	16	V
V_{IC}	Common-mode input voltage	0		$V_{DD} - 1.5$	V
T_A	Operating free-air temperature	-55		125	°C

3.3 Electrical Characteristics

at specified operating free-air temperature, $V_{DD} = 5V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		T _A	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{DD} = 5V$ to 10V, $V_{IC} = V_{ICRmin}$, See ⁽²⁾		25°C		1.2	15	mV
				-55°C to 125°C			10	
I _{IO}	Input offset current	$V_{IC} = 2.5V$		25°C		1		pA
				125°C			15	nA
I _{IB}	Input bias current	$V_{IC} = 2.5V$		25°C		5		pA
				125°C			30	nA
V _{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD} - 1$			V
				-55°C to 125°C	0 to $V_{DD} - 1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C		84		dB
				125°C		83		
				-55°C		82		
k _{SVR}	Supply-voltage rejection ratio	$V_{DD} = 5V$ to 10V		25°C		85		dB
				125°C		85		
				-55°C		82		
V _{OH}	High-level output voltage	$V_{ID} = 1V$,	I _{OH} = -4mA	25°C		4.5	4.7	V
				125°C		4.2		
V _{OL}	Low-level output voltage	$V_{ID} = -1V$,	I _{OH} = -4mA	25°C		210	300	mV
				125°C			500	
I _{OH}	Short-circuit current (Sourcing)			25°C		15	30	mA
I _{OL}	Short-circuit current (Sinking)			25°C		15	30	mA
I _{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		18	40	μA
				-55°C to 125°C			90	

(1) All characteristics are measured with zero common-mode voltage unless otherwise noted.

(2) The offset voltage limits given are the maximum values required to drive the output up to 4.5V or down to 0.3V.

3.4 Switching Characteristics

$V_{DD} = 5V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output ⁽¹⁾	$f = 10kHz$, $C_L = 50pF$	Overdrive = 2mV		4.5		μs
			Overdrive = 5mV		2.7		
			Overdrive = 10mV		1.9		
			Overdrive = 20mV		1.4		
			Overdrive = 40mV		1.1		

3.4 Switching Characteristics (续)

$V_{DD} = 5V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output ⁽¹⁾	$V_I = 1.4V$ step at IN+		1.1			μs
		$f = 10kHz$, $C_L = 50pF$	Overdrive = 2mV	4			
			Overdrive = 5mV	2.3			
			Overdrive = 10mV	1.5			
			Overdrive = 20mV	0.95			
			Overdrive = 40mV	0.65			
		$V_I = 1.4V$ step at IN+		0.15			
t_f	Fall time	$f = 10kHz$, $C_L = 50pF$	Overdrive = 50mV	50			ns
t_r	Rise time	$f = 10kHz$, $C_L = 50pF$	Overdrive = 50mV	125			ns

(1) Simultaneous switching of inputs causes degradation in output response.

3.5 Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_S = 12\text{V}$, $R_{\text{PULLUP}} = 2.5\text{k}$, $C_L = 20\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

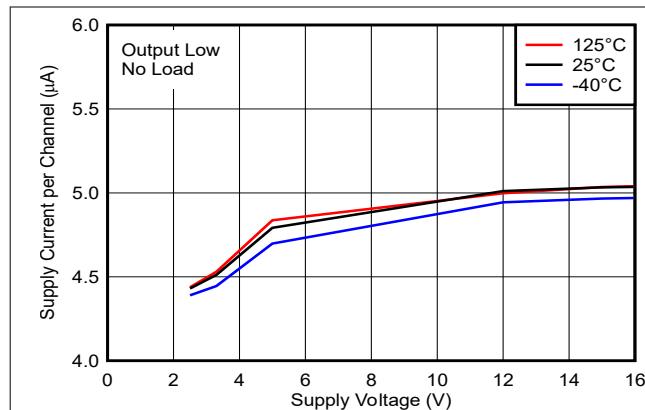


图 3-1. Supply Current per Channel vs. Supply Voltage, Output Low

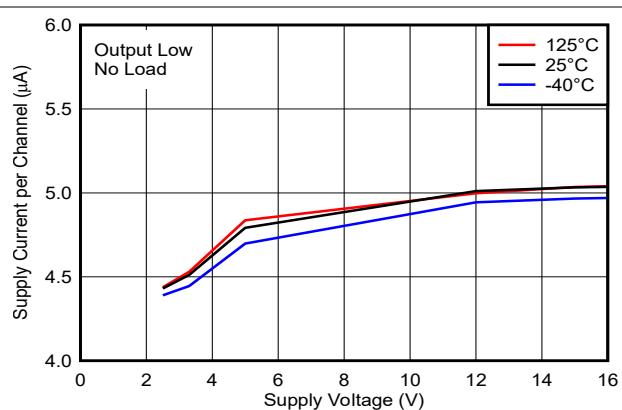


图 3-2. Supply Current per Channel vs. Supply Voltage, Output High

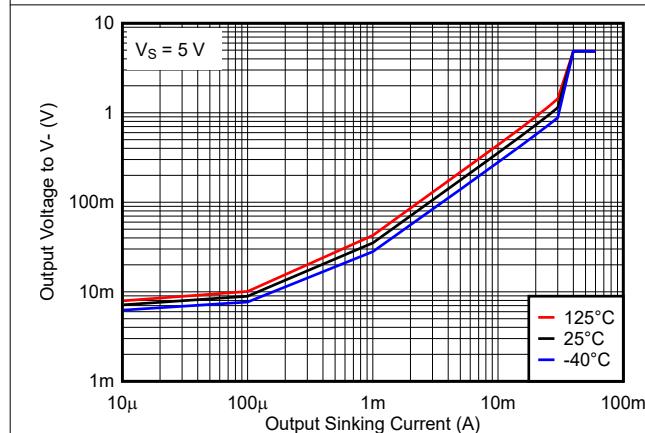


图 3-3. Output Voltage vs. Output Sinking Current, 5V

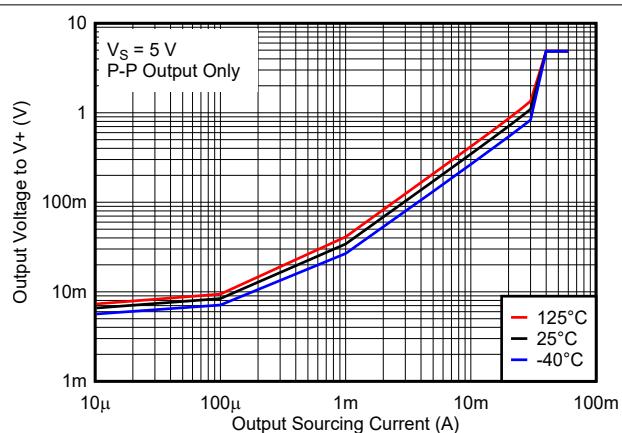


图 3-4. Output Voltage vs. Output Sourcing Current, 5V

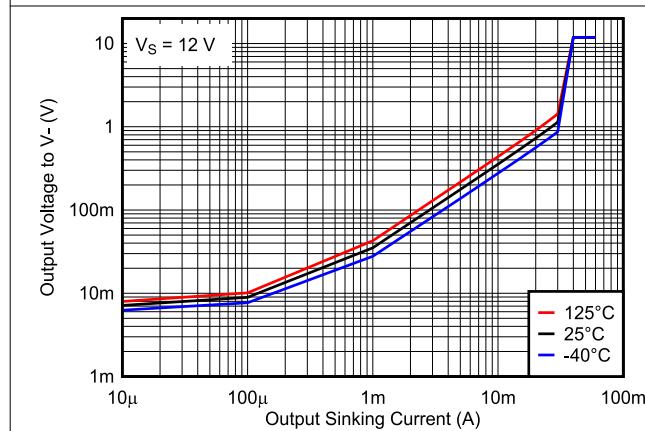


图 3-5. Output Voltage vs. Output Sinking Current, 12V

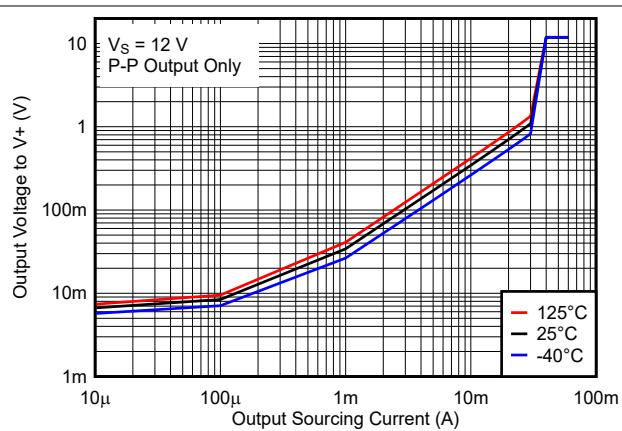


图 3-6. Output Voltage vs. Output Sourcing Current, 12V

3.5 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_S = 12\text{V}$, $R_{\text{PULLUP}} = 2.5\text{k}$, $C_L = 20\text{pF}$, $V_{\text{CM}} = 0\text{V}$, $V_{\text{UNDERDRIVE}} = 100\text{mV}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

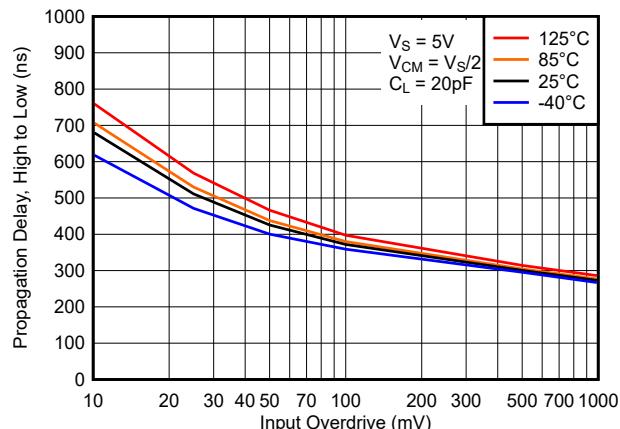


图 3-7. Propagation Delay, High to Low, 5V

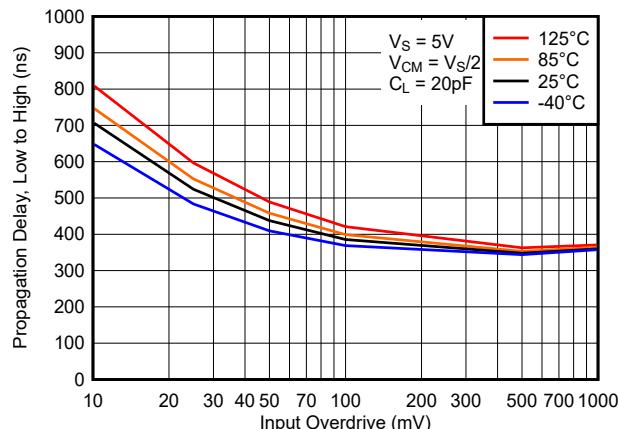


图 3-8. Propagation Delay, Low to High, 5V

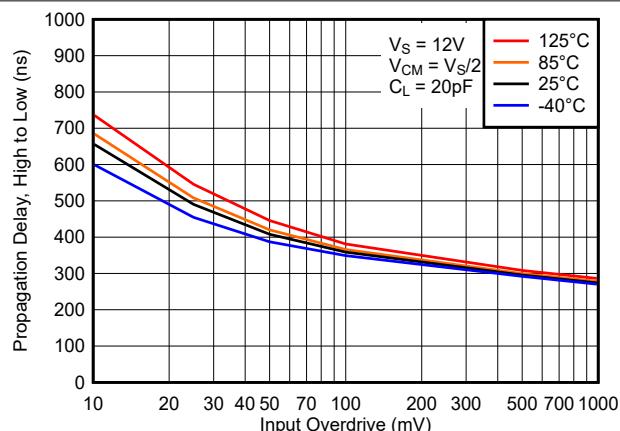


图 3-9. Propagation Delay, High to Low, 12V

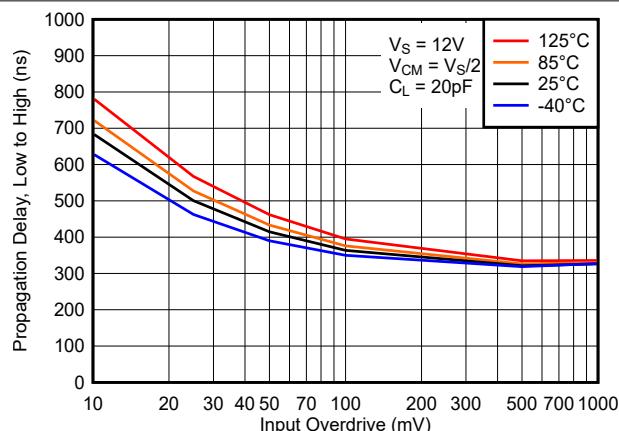


图 3-10. Propagation Delay, Low to High, 12V

4 Detailed Description

4.1 Overview

The TLC3702-EP device is a micro-power comparator with push-pull output. Operating down to 4V while only consuming only 5 μ A per channel, the TLC3702-EP is excellent for power conscious applications.

4.2 Functional Block Diagrams

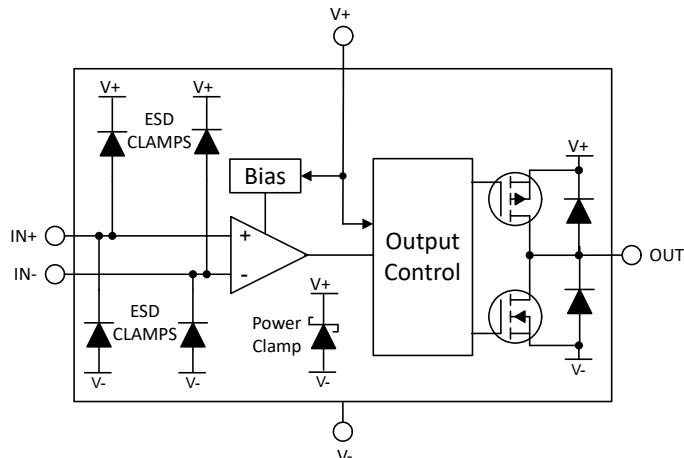


图 4-1. Block Diagram

4.3 Feature Description

The TLC3702-EP comparator consists of a CMOS differential pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The output consists of a push-pull output stage capable of sinking current with a negative differential input voltage and sourcing current with a positive differential input.

4.4 Device Functional Modes

4.4.1 Input

The TLC3702-EP input voltage range extends from V- to 1.5V below V+ over the full temperature range. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

4.4.2 ESD Protection

The TLC3702-EP input and output ESD protection contains a conventional diode-type "upper" ESD clamp between the I/O pins and V+, and a "lower" ESD clamp between the I/O pins and V-. The inputs or output must not exceed the supply rails by more than 300mV. TI does not recommend applying signals to the inputs with no supply voltage.

When the inputs are connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limiting the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

4.4.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on its own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the

specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage.

4.4.4 Push-Pull Output

The TLC3702-EP features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the opposite supply rail (V_+ when output "low" or V_- when output "High") can result in thermal runaway and eventual device destruction at high ($>12V$) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

4.4.5 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in [图 4-2](#). This curve is a function of three components: V_{TH} , V_{OS} , and V_{HYST} :

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-} . This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

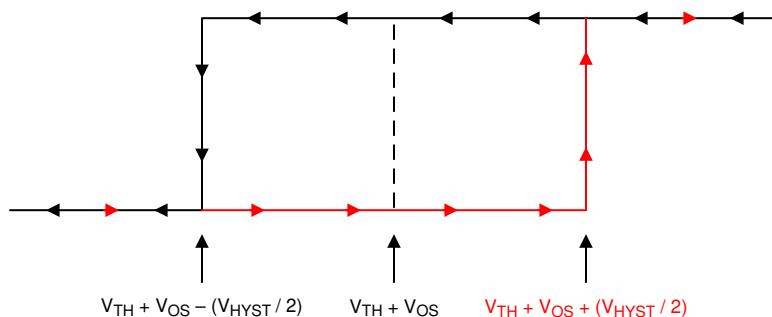


图 4-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "[Comparator with and without hysteresis circuit](#)".

4.4.5.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown below.

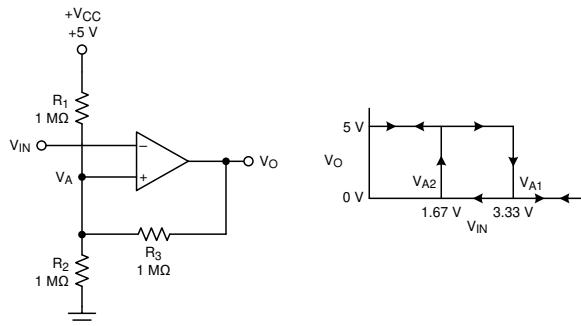


图 4-3. Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

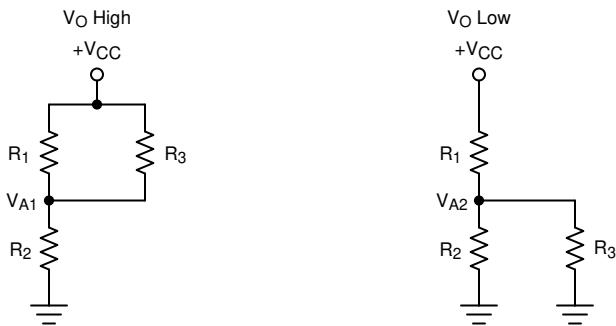


图 4-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A , the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R1 \parallel R3$ in series with $R2$, as shown above on the left.

The equation below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than V_A , the output voltage is low. In this case, the three network resistors can be presented as $R2 \parallel R3$ in series with $R1$, as shown above on the right.

Use the equation below to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The equation below defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

4.4.5.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in [图 4-5](#).

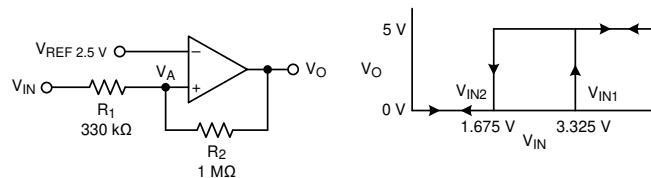


图 4-5. Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in [图 4-6](#).

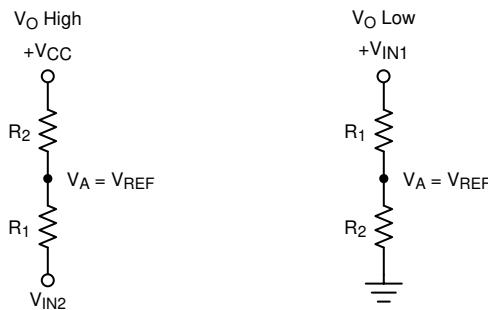


图 4-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF} , the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use [方程式 4](#) to calculate V_{IN1} .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When V_{IN} is greater than V_{REF} , the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2} . Use [方程式 5](#) to calculate V_{IN2} .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2} , as shown in [方程式 6](#).

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

5 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

5.1 Application Information

5.1.1 Basic Comparator Definitions

5.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the [图 5-1](#) example below, if V_{IN} is less than V_{REF} , the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF} , the output voltage (V_O) is at logic high (V_{OH}). [表 5-1](#) summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 5-1. Output Conditions

Inputs Condition	Output
$IN+ > IN-$	HIGH (V_{OH})
$IN+ = IN-$	Indeterminate (chatters - see Hysteresis)
$IN+ < IN-$	LOW (V_{OL})

5.1.1.2 Propagation Delay

There is a delay between when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in [图 5-1](#) and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called overdrive (V_{OD}) and underdrive (V_{UD}) voltage levels (see section below).

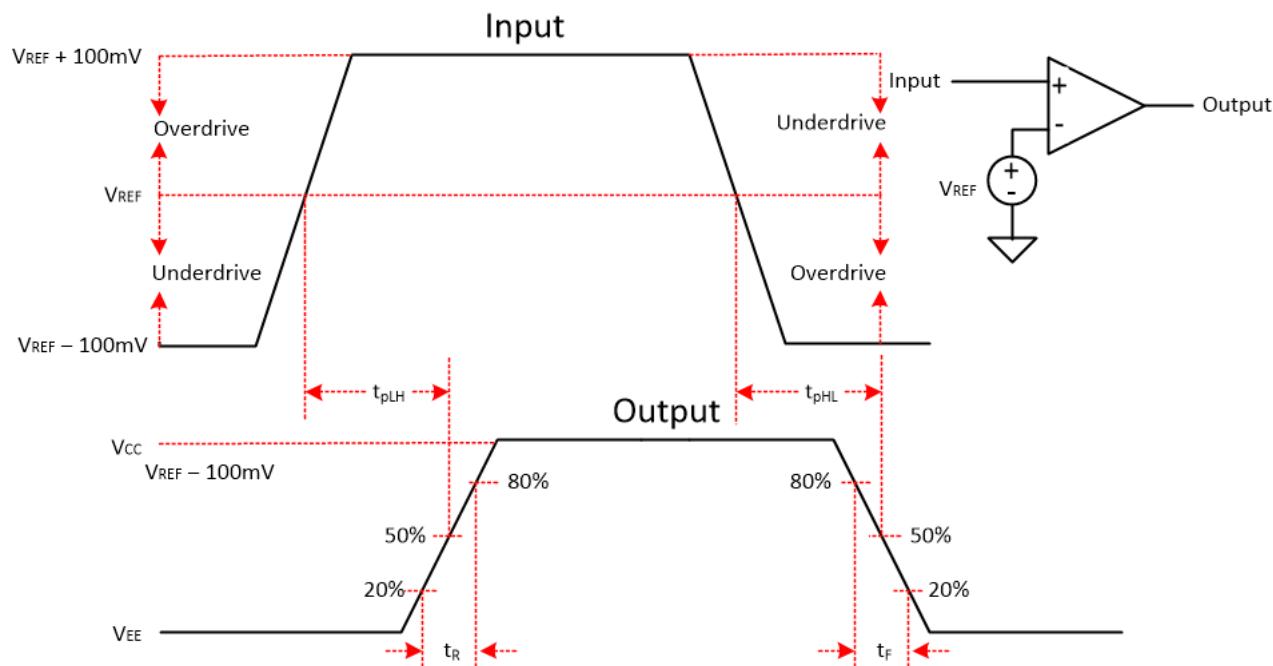


图 5-1. Comparator Timing Diagram

5.1.1.3 Overdrive and Underdrive Voltage

The overdrive voltage, V_{OD} , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the [图 5-1](#) example. Similarly, underdrive voltage, V_{UD} , is how far below REF the input starts. The overdrive and underdrive voltages influence the propagation delay (t_p). See curves in the Typical Characteristics section for more details. The smaller the overdrive voltage, the longer the propagation delay, particularly when <100 mV. If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes propagation delay to increase. This is particularly important in applications where rail-to-rail input swings are present at the comparator inputs. The result can be skewed propagation delay (difference between t_{pLH} and t_{pHL}). As a low power comparator, do not use this comparator family if variation in propagation delay is critical.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

5.2 Typical Applications

5.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. The figure below shows a simple window comparator circuit monitoring a 24V PLC power supply.

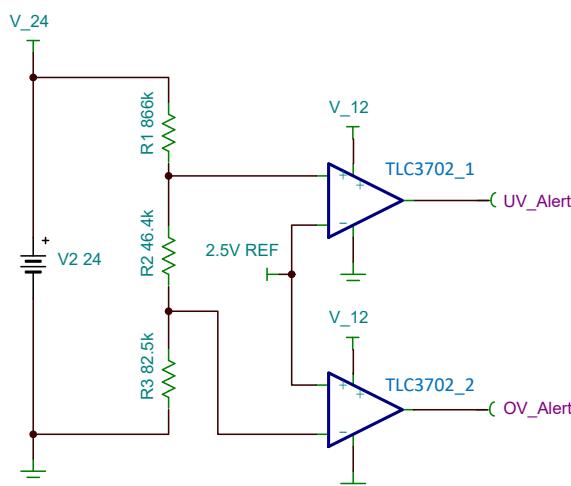


图 5-2. Window Comparator

5.2.1.1 设计要求

对于此设计，请遵循以下设计要求：

- 当 24V 电源低于 19.2V 时的 UV_Alert (逻辑低电平输出)
- 当 24V 电源高于 30V 时的 OV_Alert (逻辑低电平输出)
- 电阻器串中消耗的电流为 30uA
- 比较器由 5V 电源供电
- 采用 2.5V 外部基准

5.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLC3702-EP is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, OV_Alert and UV_Alert nets are pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from $2.5V / 30uA$ which is approximately 83.3kohms.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from $(2.5V / 19.2uA) - R3$ which is approximately 46.9kohms.

Lastly, the value of R1 is calculated from $1Mohm - (R2 + R3)$ which is approximately 870kohms. Please note that standard 1% resistor values were selected for the circuit

The respective comparator outputs (OV_Alert and UV_Alert) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.

5.2.1.3 Application Curve

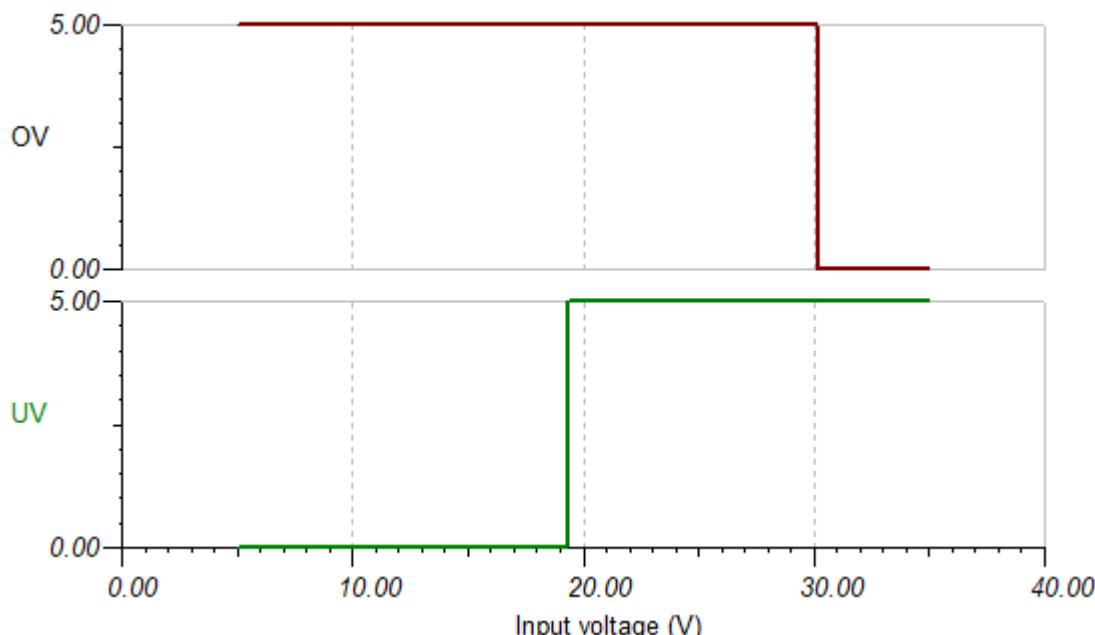


图 5-3. Window Comparator Results

5.3 Power Supply Recommendations

Due to the fast output edge rates, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at each device with a low ESR $0.1\mu F$ ceramic bypass capacitor directly between V+ pin and ground pins. Narrow, peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies (V+ and V-), or "single" supplies (V+ and GND), with GND applied to the V- pin. Input signals must stay within the specified input range (between V+ and V-) for either type. Note that with a "split" supply the output swings "low" (V_{OL}) to V- potential and not GND.

5.4 Layout

5.4.1 Layout Guidelines

For accurate comparator applications, a clean, stable power supply is important to minimize output glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V+ and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V+ or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (≤ 100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

5.4.2 Layout Example

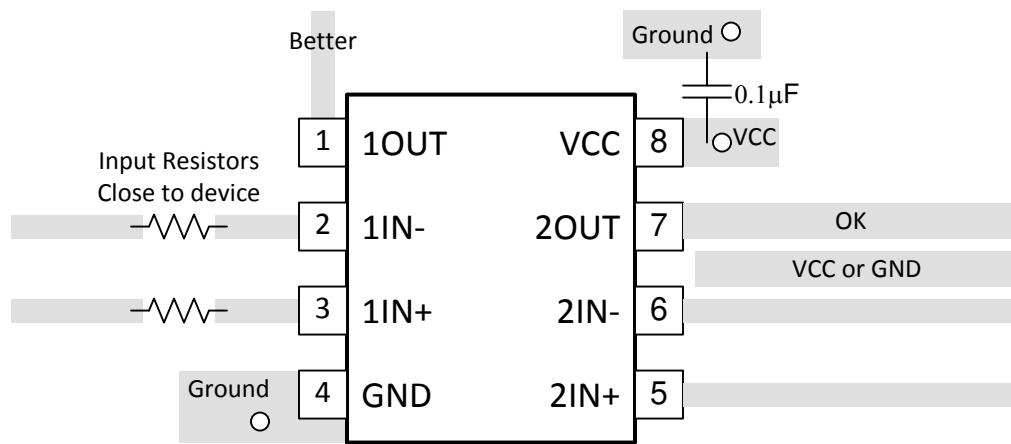


图 5-4. Dual Layout Example

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

6.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 **通知** 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.3 支持资源

[TI E2E™ 中文支持论坛](#)是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

6.4 Trademarks

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6.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

7 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (March 2025) to Revision B (June 2025)	Page
• 更新了特性.....	1

Changes from Revision * (July 2002) to Revision A (March 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 更新了整个数据表以反映新裸片——最小值最大值规格不变.....	1

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC3702MDREP	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3702ME
TLC3702MDREP.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3702ME
V62/03643-01XE	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3702ME

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC3702-EP :

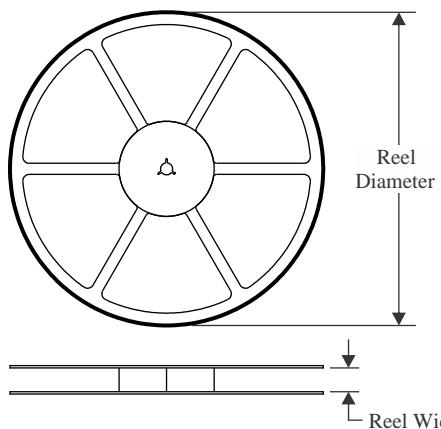
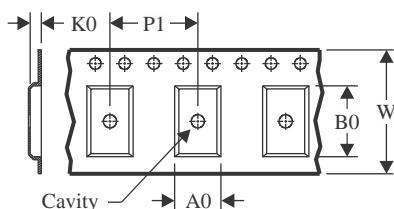
- Catalog : [TLC3702](#)

- Automotive : [TLC3702-Q1](#)

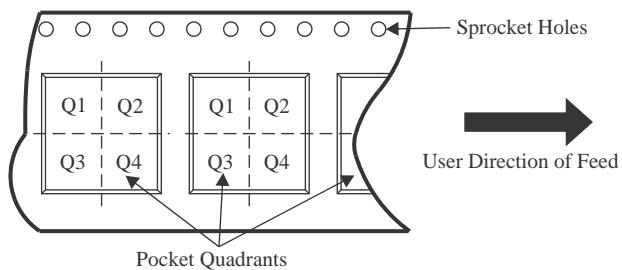
- Military : [TLC3702M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

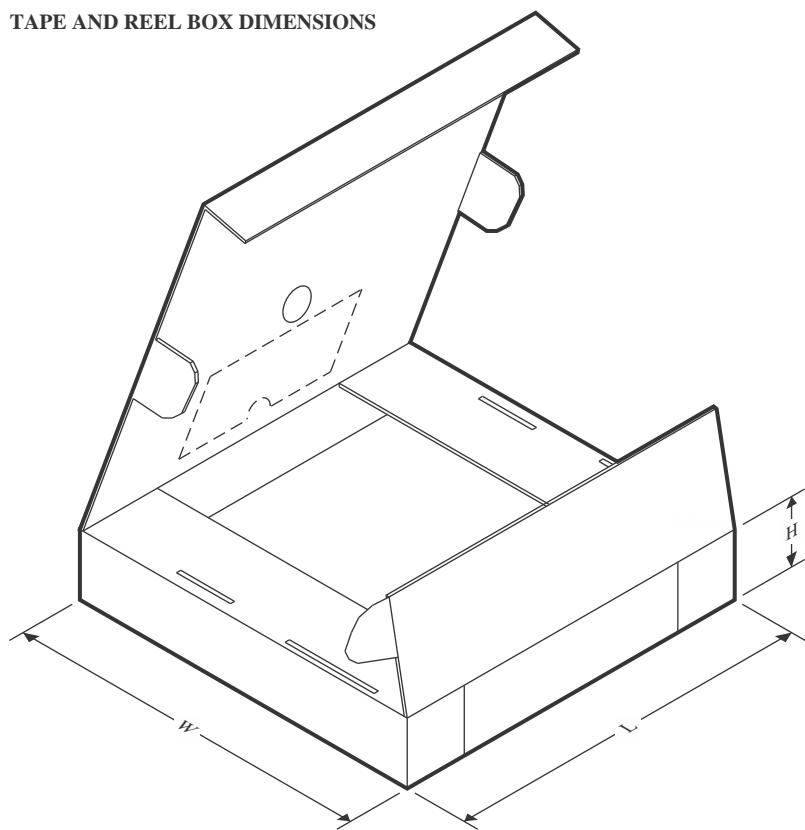
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3702MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3702MDREP	SOIC	D	8	2500	353.0	353.0	32.0

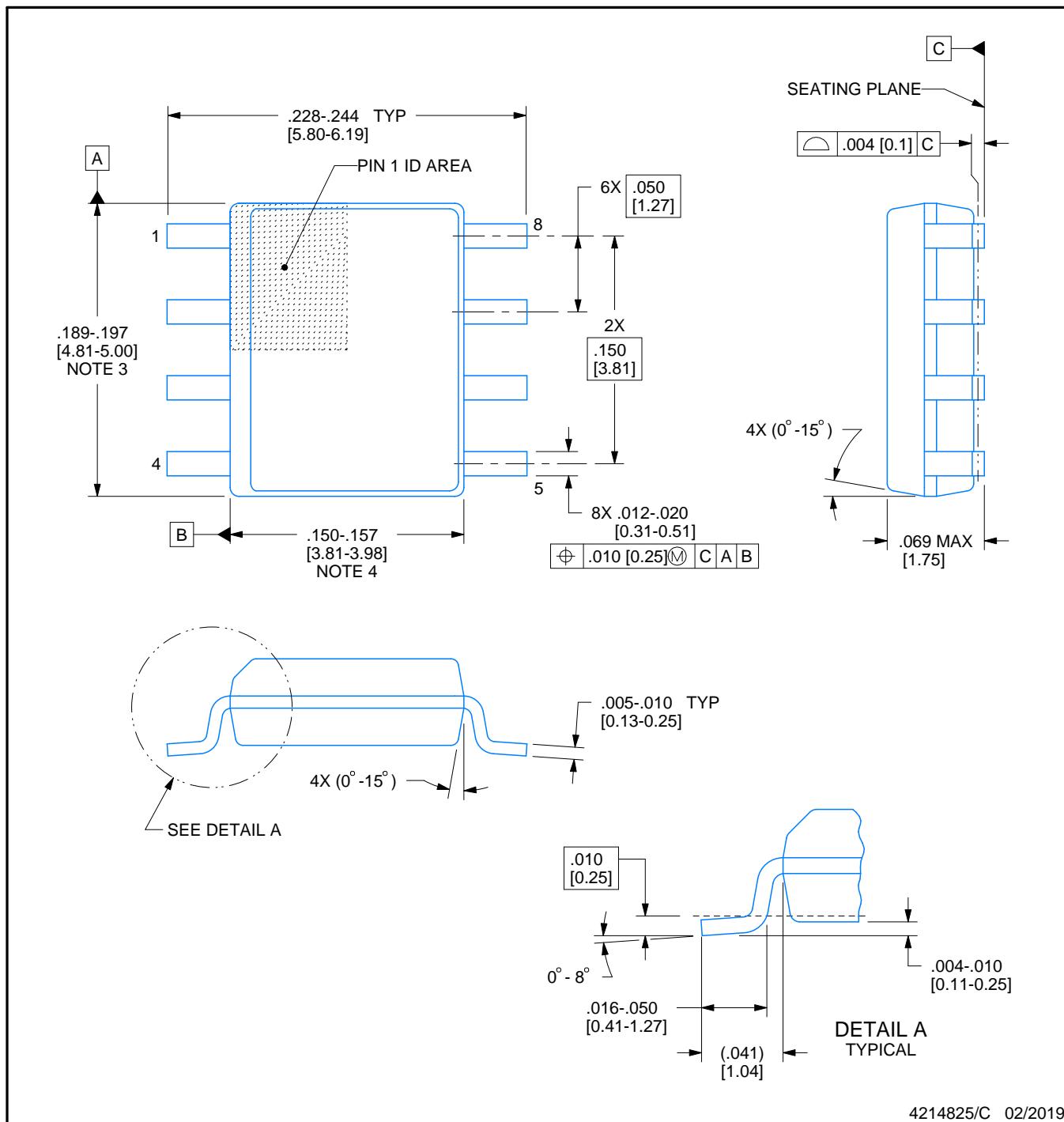


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

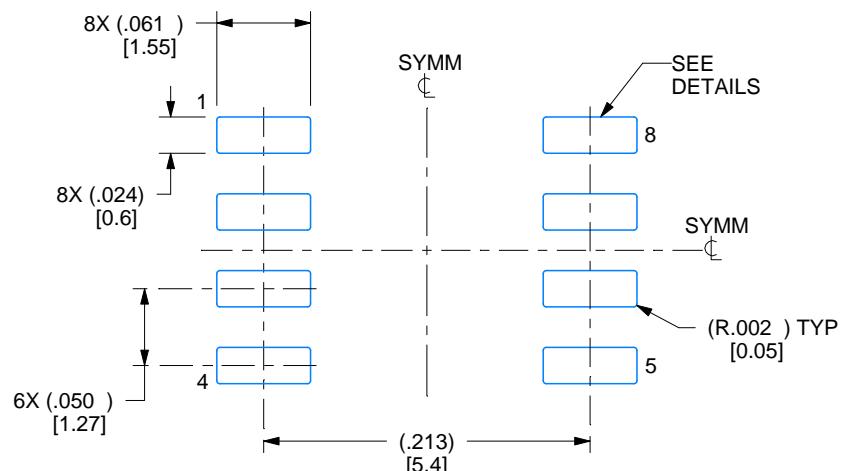
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

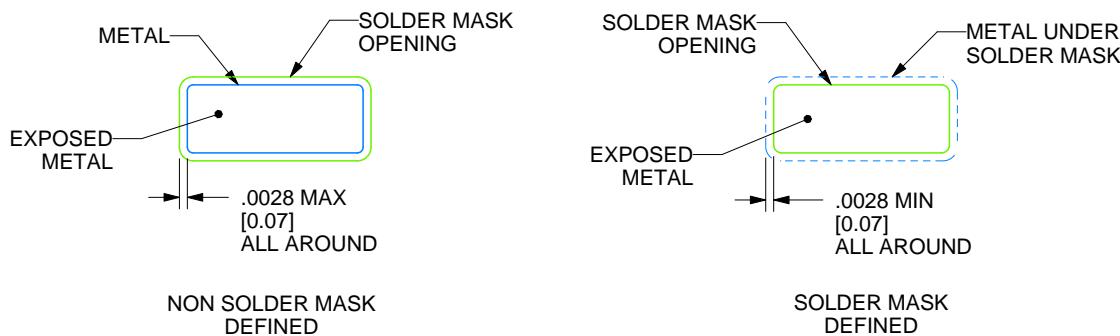
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

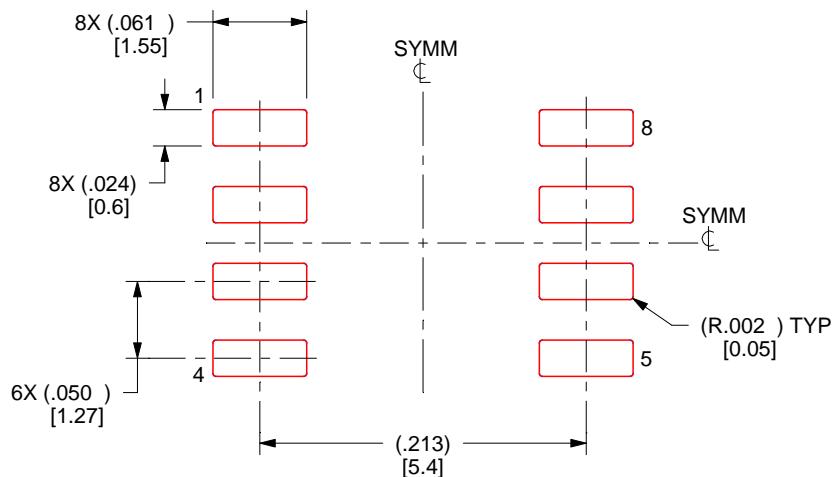
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月