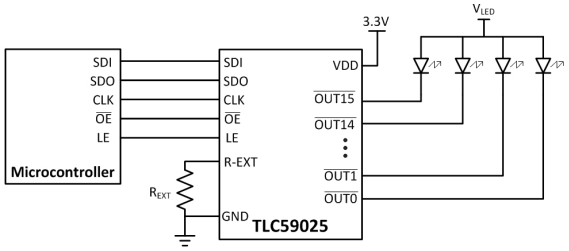
TLC59025 低功耗 16 通道恒流下沉式 LED 驱动器

1 特性

- 16 个恒流输出通道
- 业界通用的 IOUT 与外部电阻比匹配
- 恒定的输出电流不随负载电压变化而变化
- 输出电流精度：
  - 通道间：< ±5%（最大值）
  - IC 间：< ±6%（最大值）
- 恒定输出电流范围：3mA 至 45mA
- 可通过外部电阻器调节输出电流
- 可实现快速的输出电流响应，$\overline{OE}$（最小值）：100ns
- 30MHz 时钟频率
- 施密特触发器输入
- 3.0V 至 5.5V 电源电压
- 热关断可提供过热保护
- ESD 性能：1kV HBM

2 应用

- 游戏机/娱乐
- 通用 LED 应用
- LED 显示系统
- 标牌 LED 照明
- 白色家电



典型应用图

3 说明

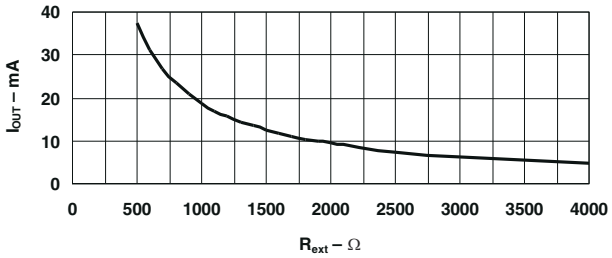
TLC59025 器件适用于 LED 显示和 LED 照明应用。TLC59025 包含一个 16 位移位寄存器和数据锁存器，它们将串行输入数据转换为并行输出格式。TLC59025 输出级有 16 个稳流端口，可提供均匀且恒定的电流，从而驱动各种变频型号的 LED。TLC59025 用于 LED 显示应用（例如 LED 面板）的系统设计中，具有出色的灵活性和器件性能。用户可通过外部电阻 R_{ext} 将输出电流从 3mA 调节到 45mA，从而灵活地控制 LED 的光强度。TLC59025 在输出端口可提供最高 17V 的电压。另外，30MHz 的高时钟频率可满足大容量数据传输的系统要求。

串行数据通过 SDI 传送到 TLC59025，在移位寄存器中移位，然后通过 SDO 传送出去。LE 可以将移位寄存器中的串行数据锁存到输出锁存器。$\overline{OE}$ 使输出驱动器可以灌入电流。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLC59025	SSOP (24)	8.65mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



I_{OUT} 和 R_{EXT} 对比

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (February 2015) to Revision C (February 2021)	Page
• 更新了整个文档的表、图和交叉参考的编号格式	1
• Updated "T_J" to "T_A" in *Electrical Characteristics for 3-V Input Voltage* table	5
• Updated "T_J" to "T_A" in *Electrical Characteristics for 5.5-V Input Voltage* table	6
• Added note to *Constant Current* section	13

Changes from Revision A (March 2013) to Revision B (February 2015)	Page
• 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1
• 删除了 *订购信息* 表	1

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5 Pin Configuration and Functions

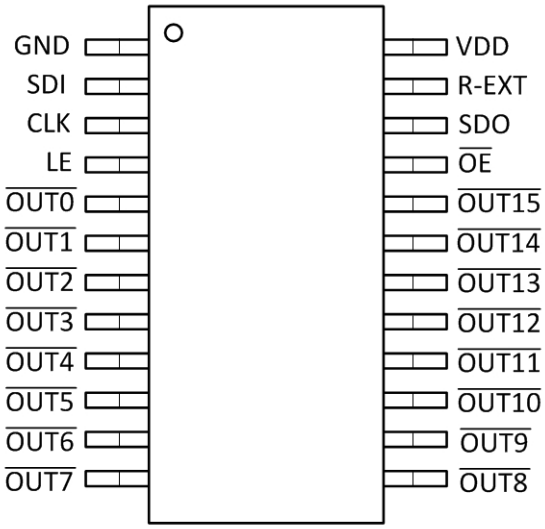

图 5-1. DBQ Package 24-Pin SSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK	3	I	Clock input for data shift on rising edge
GND	1	—	Ground for control logic and current sink
LE	4	I	Data strobe input Serial data is transferred to the respective latch when LE is high. The data is latched when LE goes low. LE has an internal pulldown resistor.
$\overline{OE}$	21	I	Output enable When $\overline{OE}$ is active (low), the output drivers are enabled. When $\overline{OE}$ is high, all output drivers are turned OFF (blanked). $\overline{OE}$ has an internal pullup resistor.
$\overline{OUT0}$	5	O	Constant-current output
$\overline{OUT1}$	6	O	Constant-current output
$\overline{OUT2}$	7	O	Constant-current output
$\overline{OUT3}$	8	O	Constant-current output
$\overline{OUT4}$	9	O	Constant-current output
$\overline{OUT5}$	10	O	Constant-current output
$\overline{OUT6}$	11	O	Constant-current output
$\overline{OUT7}$	12	O	Constant-current output
$\overline{OUT8}$	13	O	Constant-current output
$\overline{OUT9}$	14	O	Constant-current output
$\overline{OUT10}$	15	O	Constant-current output
$\overline{OUT11}$	16	O	Constant-current output
$\overline{OUT12}$	17	O	Constant-current output
$\overline{OUT13}$	18	O	Constant-current output
$\overline{OUT14}$	19	O	Constant-current output
$\overline{OUT15}$	20	O	Constant-current output
R-EXT	23	I	Input used to connect an external resistor (R_{ext}) for setting output currents

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SDI	2	I	Serial-data input to the Shift register
SDO	22	O	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	24	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	0	7	V
V_I	Input voltage	– 0.4	V_{DD} + 0.4	V
V_O	Output voltage	– 0.5	20	V
I_{OUT}	Output current		45	mA
I_{GND}	GND terminal current		750	mA
T_J	Operating virtual-junction temperature	– 40	150	°C
T_{stg}	Storage temperature	– 55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		3	5.5	V
V_O	Output voltage			17	V
V_{IH}	Input voltage		0.7 × V_{DD}	V_{DD} + 0.4	V
V_{IL}	Output voltage		GND	0.3 × V_{DD}	V
I_{OUT}	Output current	$V_O \geqslant 0.6$ V	3		mA
		$V_O \geqslant 1.0$ V		45	mA
I_{OH}	High-level output current, source		– 1		mA
I_{OL}	Low-level output current, sink		1		mA
T_A	Operating free-air temperature		– 40	125	°C

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6.4 Thermal Information

THERMAL METRIC (1)			TLC59025 DBQ (SSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Mounted on JEDEC 1-layer board (JESD 51-3), No airflow	99.8	°C/W
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow	61	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 3-V Input Voltage

V_{DD} = 3 V, T_A = – 40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{leak}	Output leakage current	V_{OH} = 17 V	T_A = 25°C			0.5	µA
			T_A = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = – 1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 1440 Ω			13		mA
	Output current error, die-die	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1440 Ω, T_A = 25°C			±3%	±6%	
	Output current error, channel-to-channel	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1440 Ω, T_A = 25°C			±1.5%	±5%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 720 Ω			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 720 Ω, T_A = 25°C			±3%	±6%	
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 720 Ω, T_A = 25°C			±1.5%	±5%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V, I_O = 13 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 13 mA to 45 mA			±1		
	Pullup resistance	$\overline{OE}$			500		kΩ
	Pulldown resistance	LE			500		kΩ
T_{sd}	Overtemperature shutdown (1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
I_{DD}	Supply current	R_{ext} = Open			7	10	mA
		R_{ext} = 1440 Ω			9	12	
		R_{ext} = 720 Ω			11	13	
C_{IN}	Input capacitance	V_I = V_{DD} or GND, CLK, SDI, SDO, $\overline{OE}$				10	pF

(1) Specified by design

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6.6 Electrical Characteristics for 5.5-V Input Voltage

V_{DD} = 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{leak}	Output leakage current	V_{OH} = 17 V	T_A = 25°C			0.5	µA
			T_A = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 1440 Ω			13		mA
	Output current error, die-die	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1440 Ω, T_A = 25°C			±3%	±6%	
	Output current error, channel-to-channel	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1440 Ω, T_A = 25°C			±1.5%	±5%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 720 Ω			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 720 Ω, T_A = 25°C			±3%	±6%	
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 720 Ω, T_A = 25°C			±1.5%	±5%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V , I_O = 26 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 13 mA to 45 mA			±1		
	Pullup resistance	$\overline{OE}$			500		kΩ
	Pulldown resistance	LE			500		kΩ
T_{sd}	Overtemperature shutdown (1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
I_{DD}	Supply current	R_{ext} = Open			9	11	mA
		R_{ext} = 1440 Ω			12	14	
		R_{ext} = 720 Ω			14	16	
C_{IN}	Input capacitance	V_I = V_{DD} or GND, CLK, SDI, SDO, $\overline{OE}$				10	pF

(1) Specified by design

6.7 Power Dissipation Ratings

				MIN	MAX	UNIT
P_D	Power dissipation	Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, T_A = 25°C, T_J = 125°C	DBQ package		1.6	W

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6.8 Timing Requirements

V_{DD} = 3 V to 5.5 V (unless otherwise noted)

			MIN	MAX	UNIT
$t_{w(L)}$	LE pulse duration		15		ns
$t_{w(CLK)}$	CLK pulse duration		15		ns
$t_{w(OE)}$	$\overline{OE}$ pulse duration		300		ns
$t_{su(D)}$	Setup time for SDI		3		ns
$t_{h(D)}$	Hold time for SDI		2		ns
$t_{su(L)}$	Setup time for LE		5		ns
$t_{h(L)}$	Hold time for LE		5		ns
f_{CLK}	Clock frequency	Cascade operation		30	MHz

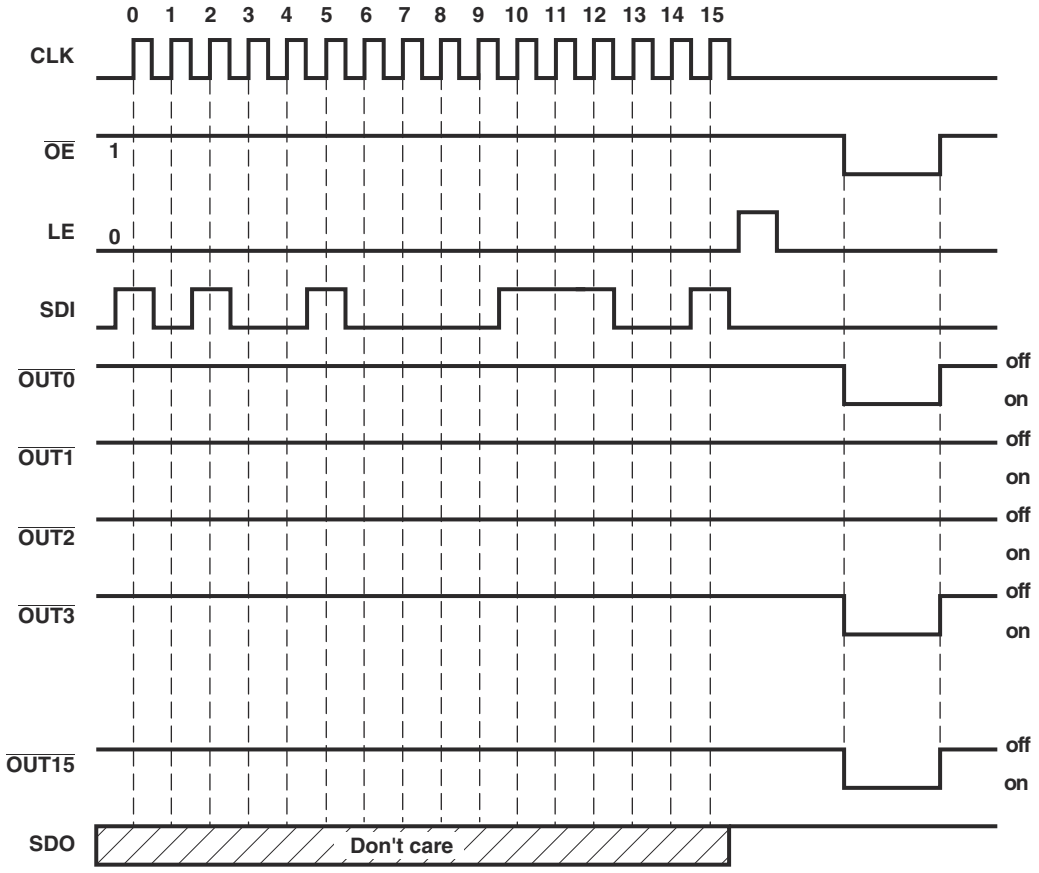

图 6-1. Timing Diagram

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6.9 Switching Characteristics for 3-V Input Voltage

V_{DD} = 3 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	V_{IH} = V_{DD}, V_{IL} = GND, R_{ext} = 720 Ω, V_L = 4 V, R_L = 88 Ω, C_L = 10 pF	30	45	60	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$		30	45	60	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		30	45	60	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			30	40	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$		40	65	100	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$		40	65	100	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		40	65	100	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			30	40	ns
$t_{w(CLK)}$	Pulse duration, CLK		15			ns
$t_{w(L)}$	Pulse duration LE		15			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$		300			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
t_r	Rise time, CLK (1)				500	ns
t_f	Fall time, CLK (1)				500	ns
t_{or}	Rise time, outputs (off)		35	50	70	ns
t_{of}	Rise time, outputs (on)		15	50	120	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

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6.10 Switching Characteristics for 5.5-V Input Voltage

V_{DD} = 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 720 Ω, V_L = 4 V, R_L = 88 Ω, C_L = 10 pF	20	35	55	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$		20	35	55	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		20	35	55	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$		15	28	42	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$		15	28	42	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		15	28	42	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		10			ns
$t_{w(L)}$	Pulse duration LE		10			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$		200			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
t_r	Rise time, CLK (1)				500	ns
t_f	Fall time, CLK (1)				500	ns
t_{or}	Rise time, outputs (off)		25	45	65	ns
t_{of}	Rise time, outputs (on)		7	12	20	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

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6.11 Typical Characteristics

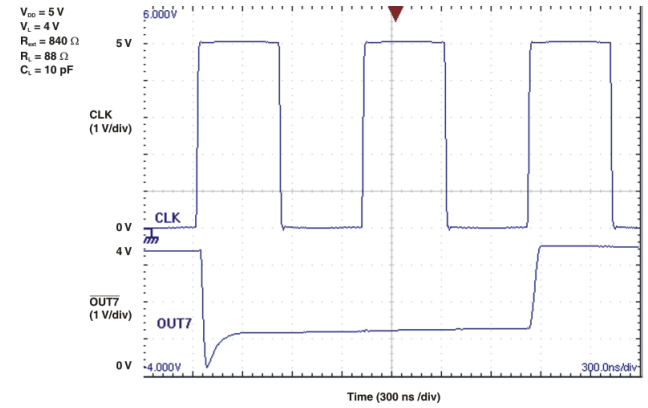

图 6-2. CLK to $\overline{OUT7}$

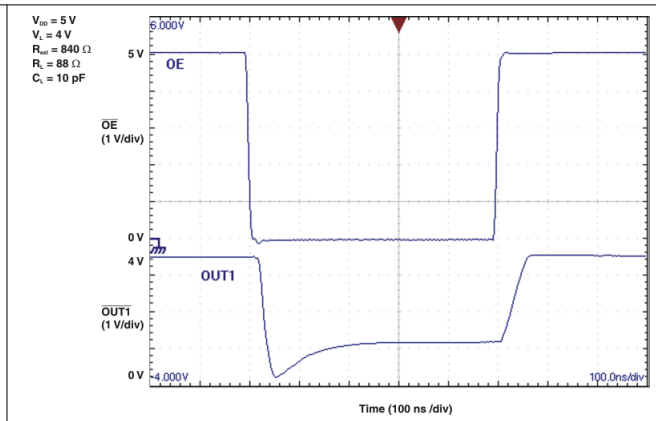

图 6-3. $\overline{OE}$ to $\overline{OUT1}$

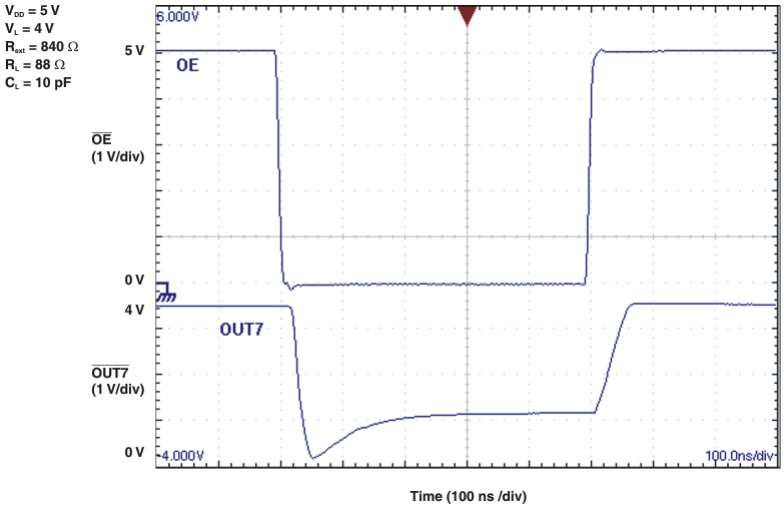

图 6-4. $\overline{OE}$ to $\overline{OUT7}$

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7 Parameter Measurement Information

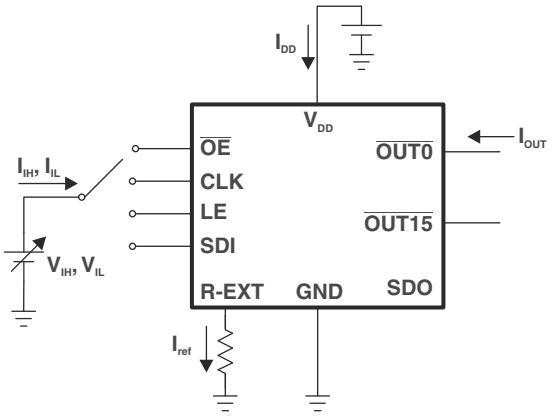

图 7-1. Test Circuit for Electrical Characteristics

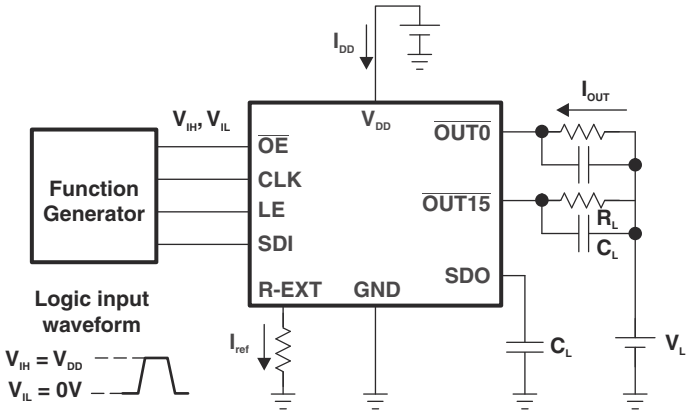

图 7-2. Test Circuit for Switching Characteristics

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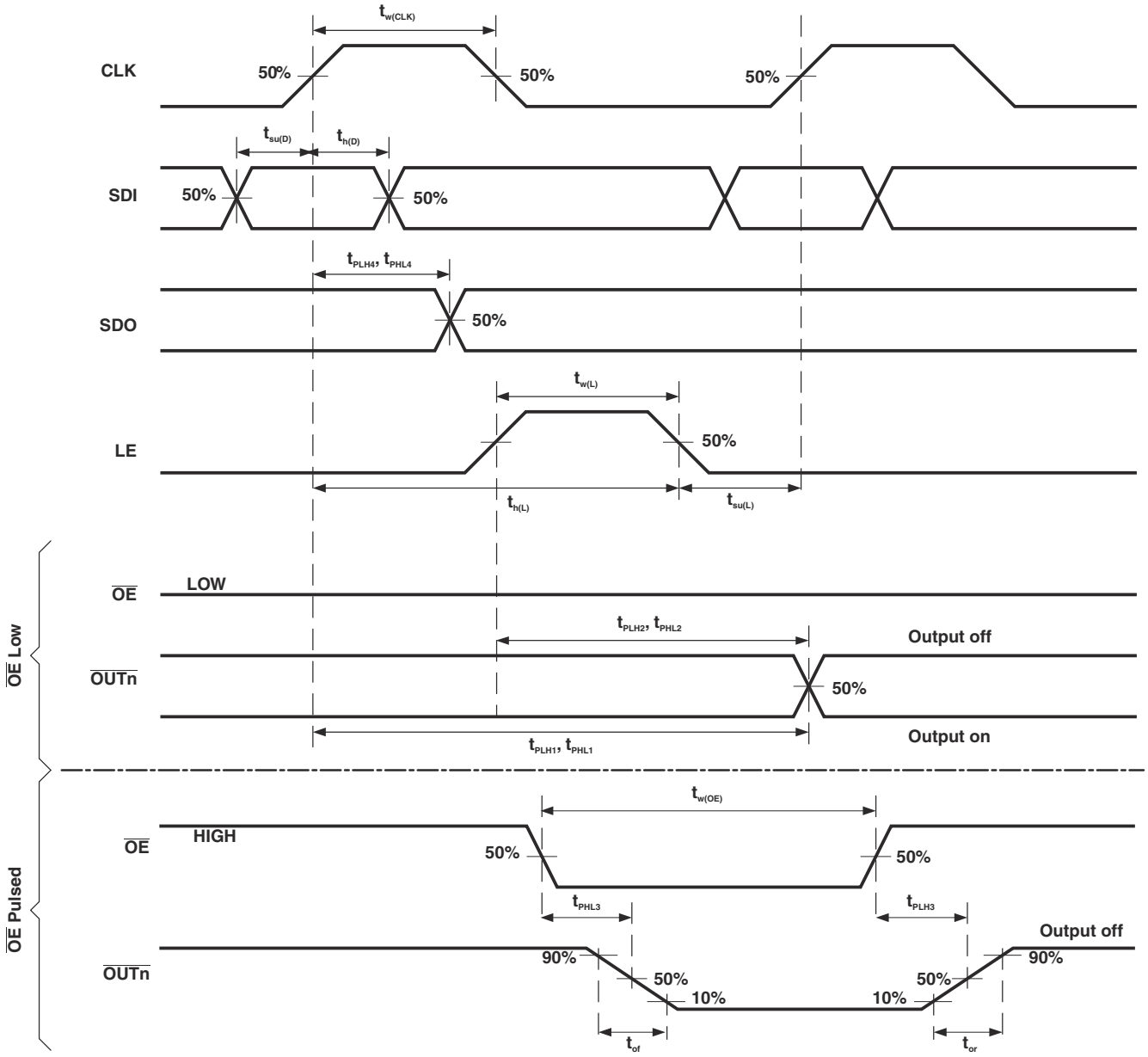

图 7-3. Normal Mode Timing Waveforms

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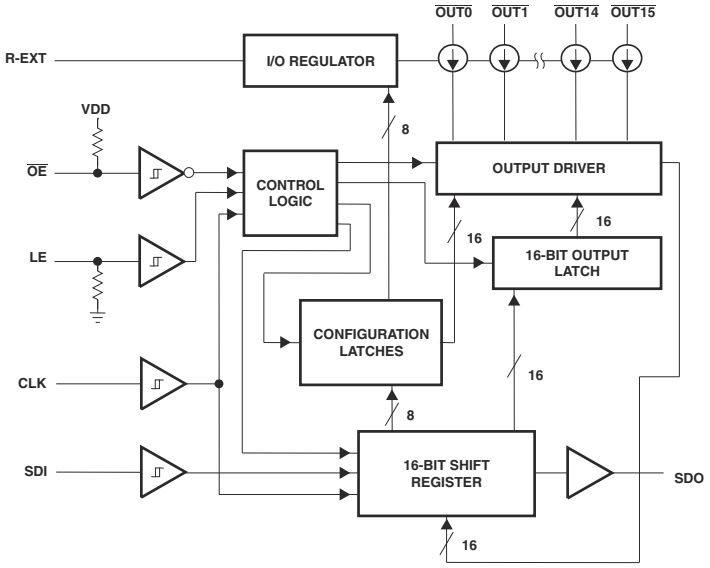
8 Detailed Description

8.1 Overview

The TLC59025 is a 16-channel LED driver designed for LED displays and LED lighting applications. The TLC59025 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC59025 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (for example, LED panels), the TLC59025 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor, R_{EXT}, which gives flexibility in controlling the light intensity of LEDs. TLC59025 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Constant Current

In LED display applications, TLC59025 provides nearly no current variations from channel to channel and from IC to IC. While $I_{OUT} \leqslant 45$ mA, the maximum current skew between channels is less than ±5% and between ICs is less than ±6%.

Note

When the TLC59025 is used in very low current applications, reduced current accuracy can be expected. For example, current accuracy is estimated to degrade to as much as ±10% when Iout = 1.7 mA.

8.4 Device Functional Modes

表 8-1 lists the functional modes for the TLC59025.

表 8-1. Truth Table in Normal Operation

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$... $\overline{OUT15}$... $\overline{OUT15}$	SDO
↑	H	L	Dn	Dn...Dn – 7...Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14
↑	H	L	Dn + 2	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2...Dn – 5...Dn – 13	Dn – 13

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表 8-1. Truth Table in Normal Operation (continued)

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$... $\overline{OUT15}$... $\overline{OUT15}$	SDO
↓	X	H	Dn + 3	off	Dn – 13

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Turning on the LEDs

To turn on an LED connected to one of the outputs of the device, the output must be pulled low. To do this, the SDI signal must let the device know which outputs should be activated. Using the rising edge of CLK, the logic level of the SDI signal latches the desired state of each output into the shift register. Once this is complete, the LE signal must be toggled from low to high then back to low. Once /OE is pulled down, the corresponding outputs will be pulled low and the LEDs will be turned on. The below diagram shows outputs 0, 3, 4, 5, 10, 13, and 15 being activated.

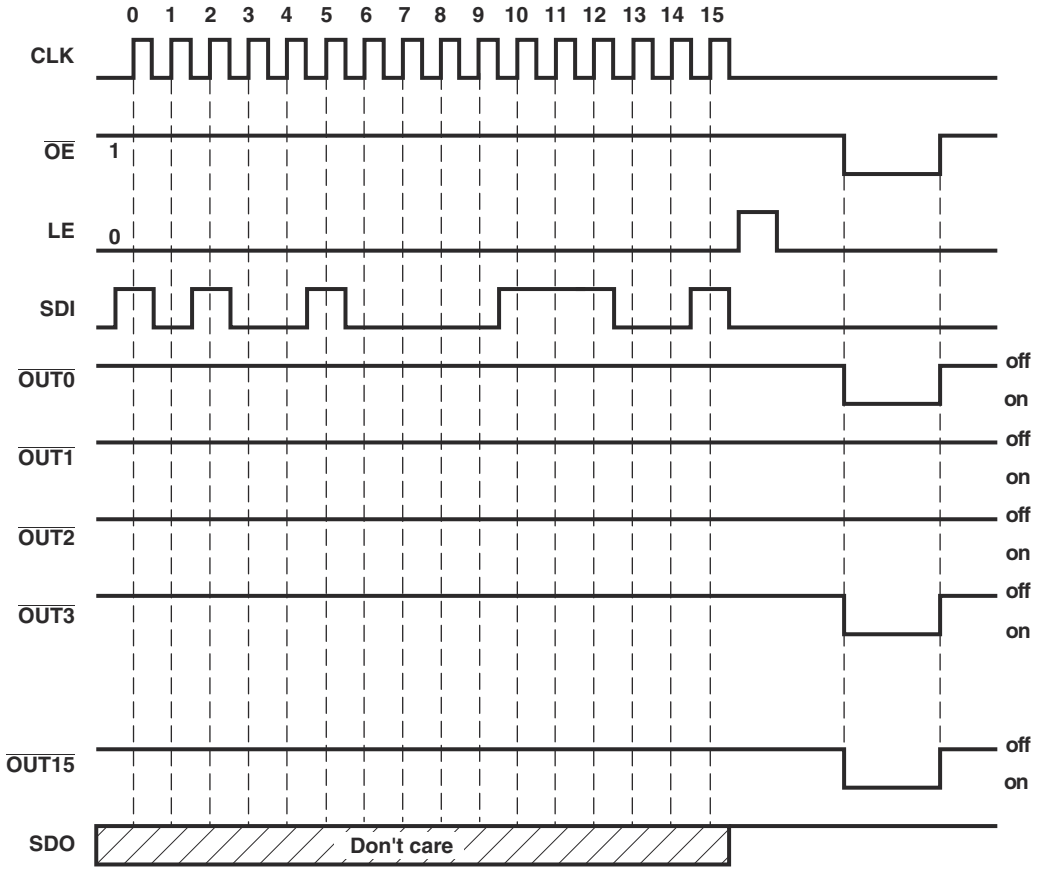

图 9-1. Timing Diagram

9.2 Typical Application

This application shows how to calculate the output current for $\overline{OUT0}$ through $\overline{OUT15}$.

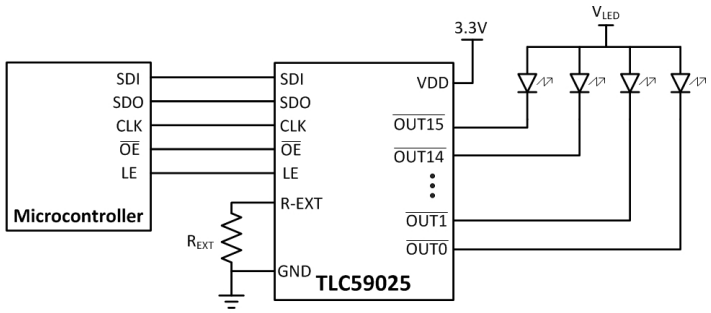

图 9-2. Typical Application Diagram

9.2.1 Design Requirements

For the following design procedure, the input voltage (V_{DD}) is between 3 V and 5.5 V.

9.2.2 Detailed Design Procedure

9.2.2.1 Adjusting Output Current

TLC59025 sets I_{OUT} based on the external resistor R_{EXT}. Users can follow the below formula to calculate the target output current $I_{OUT,target}$ in the saturation region:

$I_{OUT,target} = (1.21\ V / R_{EXT}) \times 15.5$

Where R_{EXT} is the external resistance connected between R-EXT and GND. Using this equation, the output current is calculated to be approximately 26 mA at 720 Ω and 13 mA at 1440 Ω.

9.2.3 Application Curve

The default relationship after power on between $I_{OUT,target}$ and R_{EXT} is shown in 图 9-3.

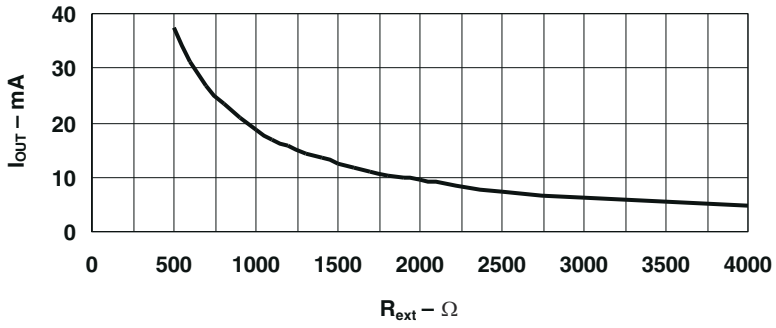

图 9-3. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

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10 Power Supply Recommendations

The TLC59025 is designed to operate with a VDD range between 3 V and 5.5 V.

11 Layout

11.1 Layout Guidelines

The SDI, CLK, SDO, LE, and $\overline{OE}$ signals should all be kept from potential noise sources.

All traces carrying power through the LEDs should be wide enough to handle necessary currents.

All LED current passes through the device and into the ground node. There must be a strong connection between the device ground and the circuit board ground.

11.2 Layout Example

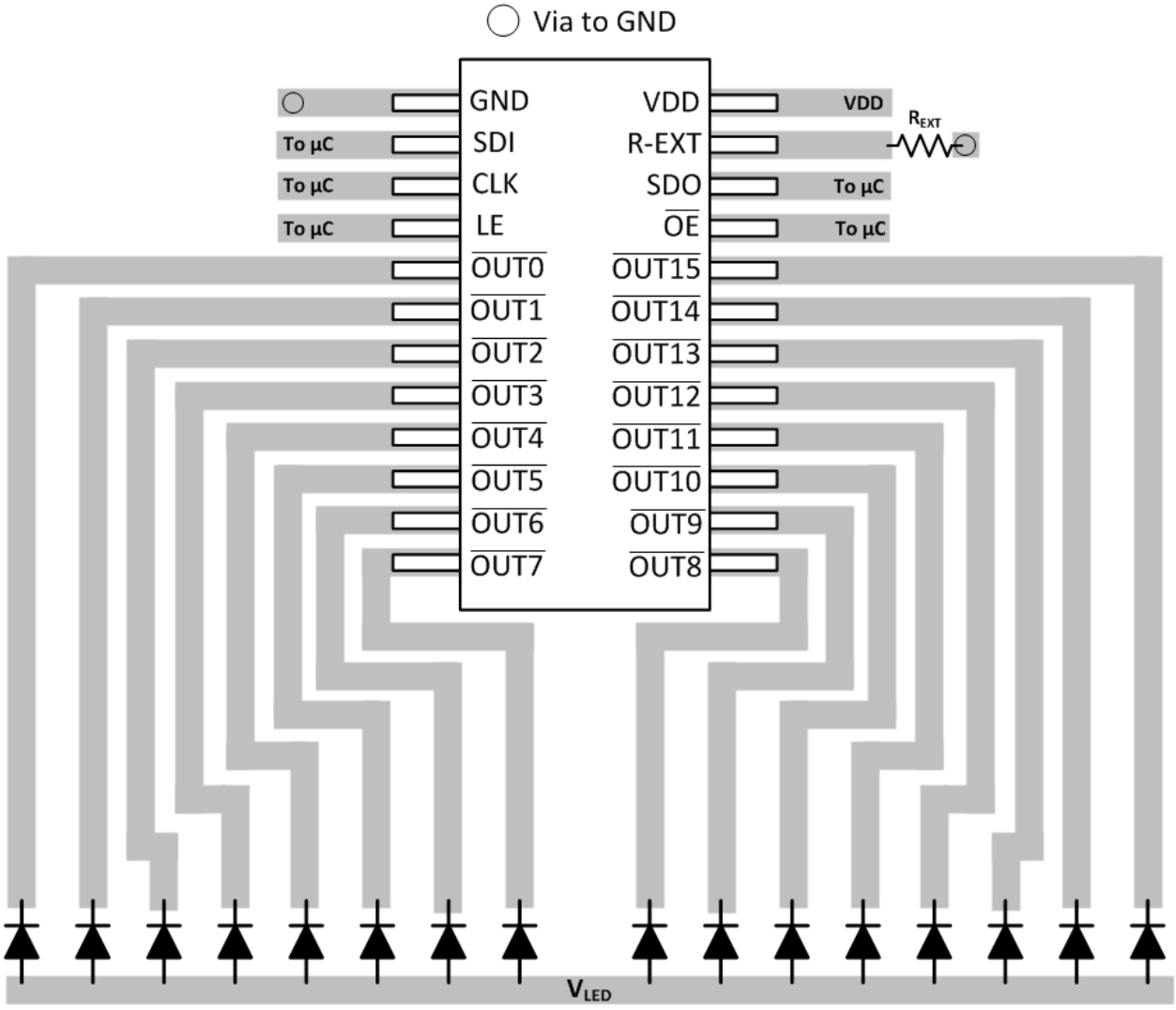

图 11-1. Layout Recommendation

12 Device and Documentation Support

12.1 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59025IDBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC59025I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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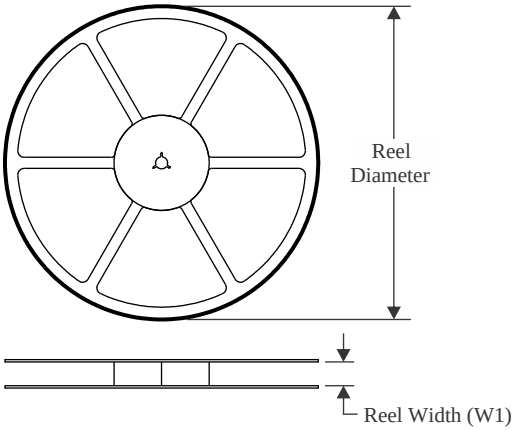
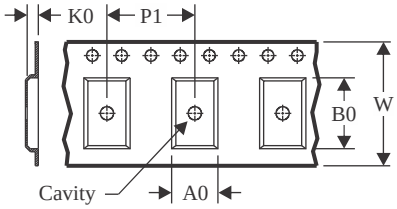
TAPE AND REEL INFORMATION

REEL DIMENSIONS

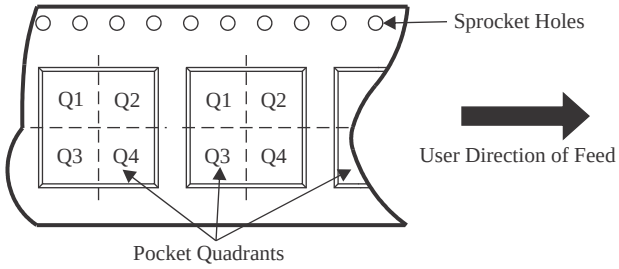


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

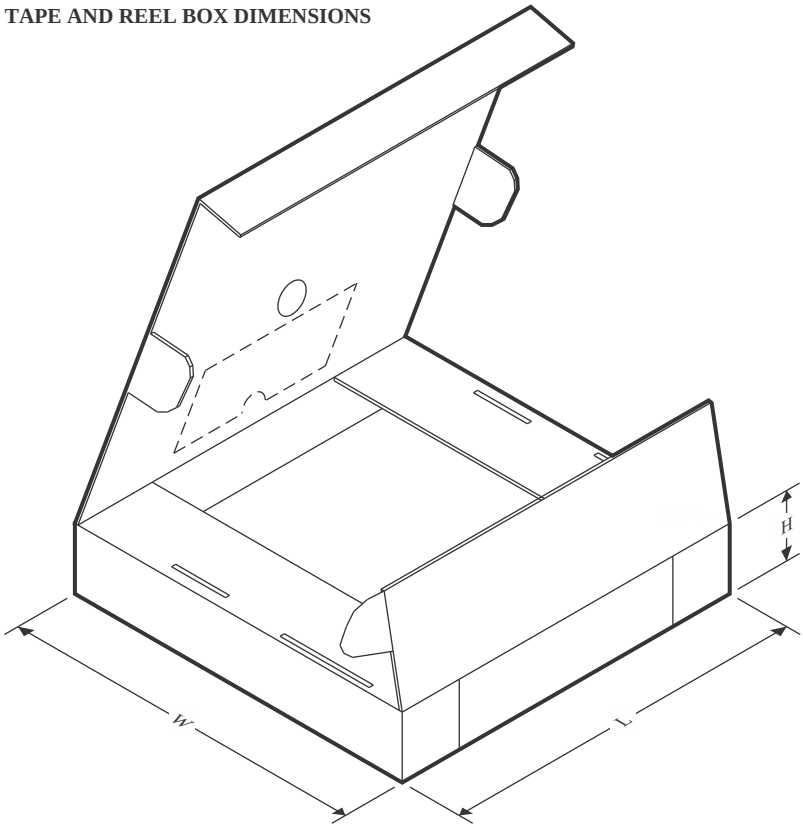
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59025IDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

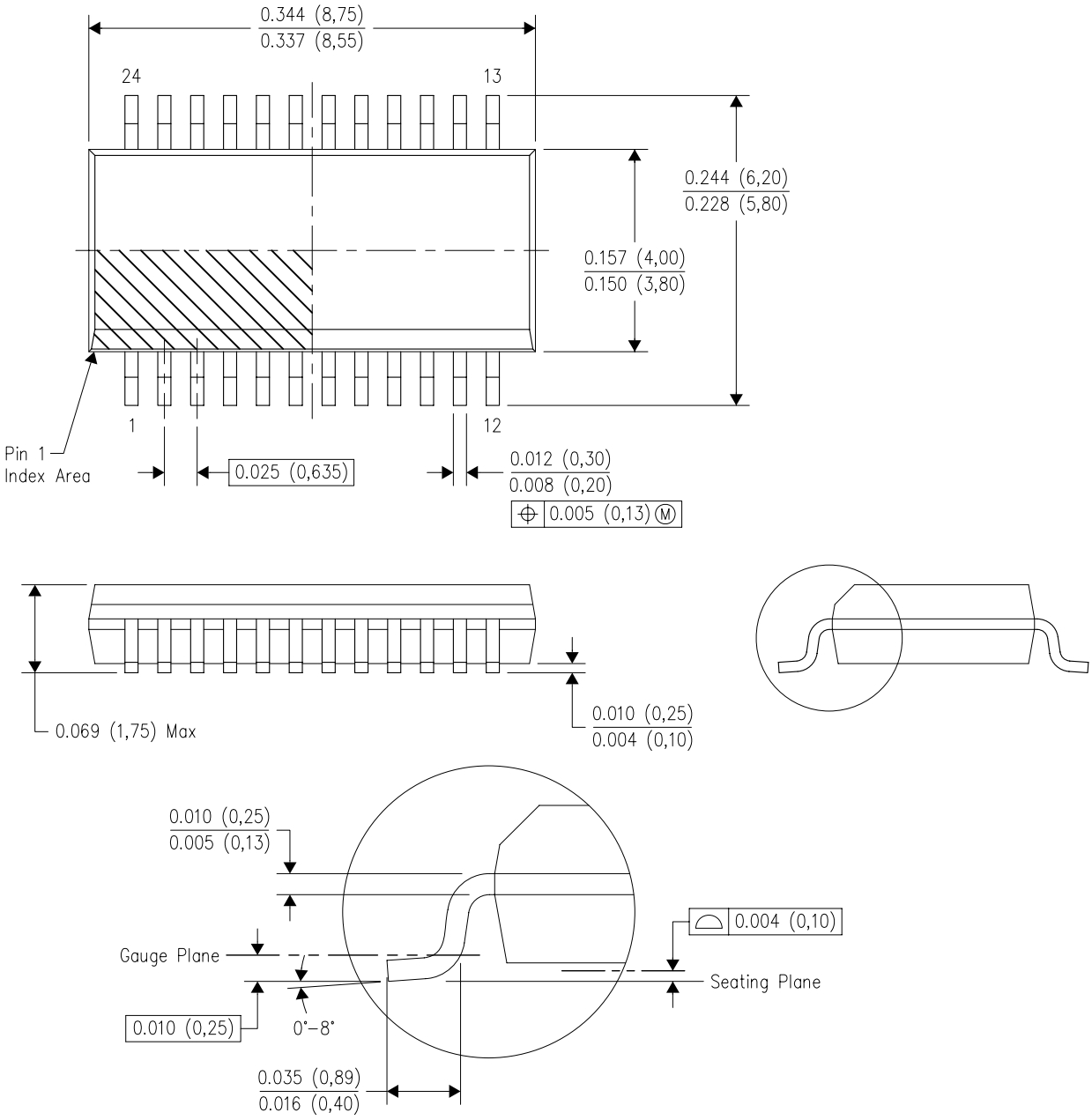
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59025IDBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

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