TLC69637-Q1 汽车 100mA、48 通道 LED 驱动器，配备集成振荡器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 1 级：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM 分类等级 H1C
  - 器件 CDM 分类等级 C4B
- 功能安全型
  - 可提供用于功能安全系统设计的文档
- 48 个集成的电流吸收器
  - 可编程的 16 位 PWM/混合调光
  - 可编程的 7 位模拟点校正 (DC)
  - 最大输出电流/电压：100mA/16V
- 集成的 33MHz 振荡器
  - 500Hz 的 16 位 PWM 输出
  - 采用增强频谱 (ES) PWM 时，刷新率大于 20KHz
- 高速通信
  - 串行外设接口 (SPI)
  - 数据速率高达 17Mbps
- 电源效率优化
  - 自适应余量电压控制 (AHVC)
  - 器件节电模式 (PSM)
- 降低 EMI
  - 接口：可编程缓冲器驱动能力
  - 电流吸收器：相移/展频
- 保护和诊断
  - LED：开路/短路检测/运行状况检查
  - 电流吸收器：相邻引脚短路/运行状况检查
  - 接口：CRC/命令错误/超时错误
  - 器件：欠压/ISET 超出范围/热关断

2 应用

- 汽车中心信息显示屏
- 汽车仪表组显示屏
- 汽车抬头显示

3 说明

TLC69637-Q1 是一款 LED 驱动器，它具有 48 条恒定电流吸收器通道，可提供高达 16 位的独立像素级 LED PWM 控制。每条通道还实施额外的 7 位点校正 (DC) 以控制峰值电流。每个器件通过串行外设接口 (SPI) 共享数据流，其最多支持 511 个器件的连接。该接口与同一组中的 LED 驱动器软件兼容，可根据 LED 电流和 LED 总数应用于不同的应用场景。

为了优化整体系统电源效率，该器件配备了自适应余量电压控制 (AHVC) 方案，用于优化每条通道和每个器件的余量电压。只需要将菊花链最后一个器件的 OUT47 引脚编程为 FB 引脚，即可优化来自 DC/DC 的 LED 电源电压。

TLC69637-Q1 配备了 LED、电流吸收器、通信和器件的诊断功能。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TLC69637-Q1	VQFN (56) 可湿性侧面	8mm × 8mm
	HTSSOP (56)	14mm × 6.1mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

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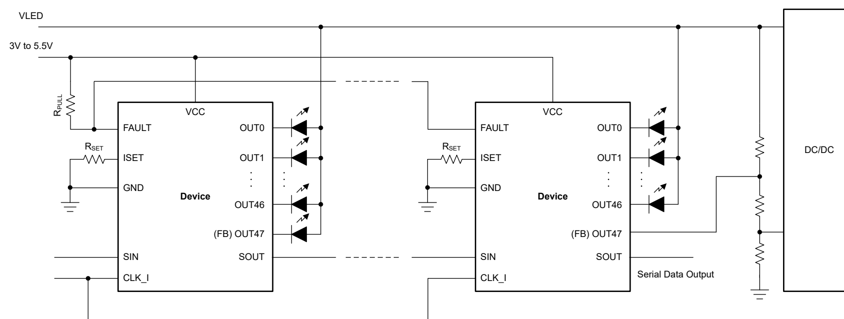

简化版原理图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

English Data Sheet: SNVSCZ1

ADVANCE INFORMATION

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4 器件比较

<table>
<tr><th>器件型号</th><th>通道编号</th><th>最大值通道电流</th><th>功能安全分类</th><th>接口</th><th>软件兼容</th></tr>
<tr><td>TLC69621-Q1 [(1)]</td><td>8</td><td rowspan="3">60mA</td><td rowspan="6">功能安全型</td><td rowspan="6">SPI</td><td rowspan="6">组 1</td></tr>
<tr><td>TLC69624-Q1 [(1)]</td><td>24</td></tr>
<tr><td>TLC69627-Q1</td><td>48</td></tr>
<tr><td>TLC69631-Q1 [(1)]</td><td>8</td><td rowspan="3">100mA</td></tr>
<tr><td>TLC69634-Q1 [(1)]</td><td>24</td></tr>
<tr><td>TLC69637-Q1</td><td>48</td></tr>
<tr><td>TLC69622-Q1 [(1)]</td><td>8</td><td rowspan="3">60mA</td><td rowspan="6">符合功能安全标准</td><td rowspan="6">SPI</td><td rowspan="6">组 2</td></tr>
<tr><td>TLC69625-Q1 [(1)]</td><td>24</td></tr>
<tr><td>TLC69628-Q1</td><td>48</td></tr>
<tr><td>TLC69632-Q1 [(1)]</td><td>8</td><td rowspan="3">100mA</td></tr>
<tr><td>TLC69635-Q1 [(1)]</td><td>24</td></tr>
<tr><td>TLC69638-Q1</td><td>48</td></tr>
<tr><td>TLC69623-Q1 [(1)]</td><td>8</td><td rowspan="3">60mA</td><td rowspan="6">符合功能安全标准</td><td rowspan="6">CSI</td><td rowspan="6">组 3</td></tr>
<tr><td>TLC69626-Q1 [(1)]</td><td>24</td></tr>
<tr><td>TLC69629-Q1</td><td>48</td></tr>
<tr><td>TLC69633-Q1 [(1)]</td><td>8</td><td rowspan="3">100mA</td></tr>
<tr><td>TLC69636-Q1 [(1)]</td><td>24</td></tr>
<tr><td>TLC69639-Q1</td><td>48</td></tr>
</table>

(1) 产品预发布

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ADVANCE INFORMATION

5 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

5.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

6 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

日期	修订版本	注释
2025 年 1 月	*	预告信息发布

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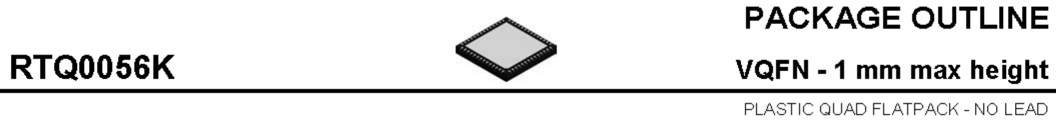
7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

ADVANCE INFORMATION



B
8.1
7.9
A
PIN 1 INDEX AREA
8.1
7.9
0.1 MIN
(0.13)
SECTION A-A
TYPICAL
1.0
0.8
C
SEATING PLANE
0.05
0.00
0.08 C
2X 6.5
EXPOSED
THERMAL PAD
SYMM
15
28
14
29
2X 6.5
SYMM
57
A A
6.6±0.1
(0.2) TYP
52X 0.5
1
56
43
42
56X 0.3
0.2
PIN 1 ID
(45° X 0.3)
56X 0.5
0.3
0.1 Ⓜ C A B
0.05 Ⓜ C
4230533/A 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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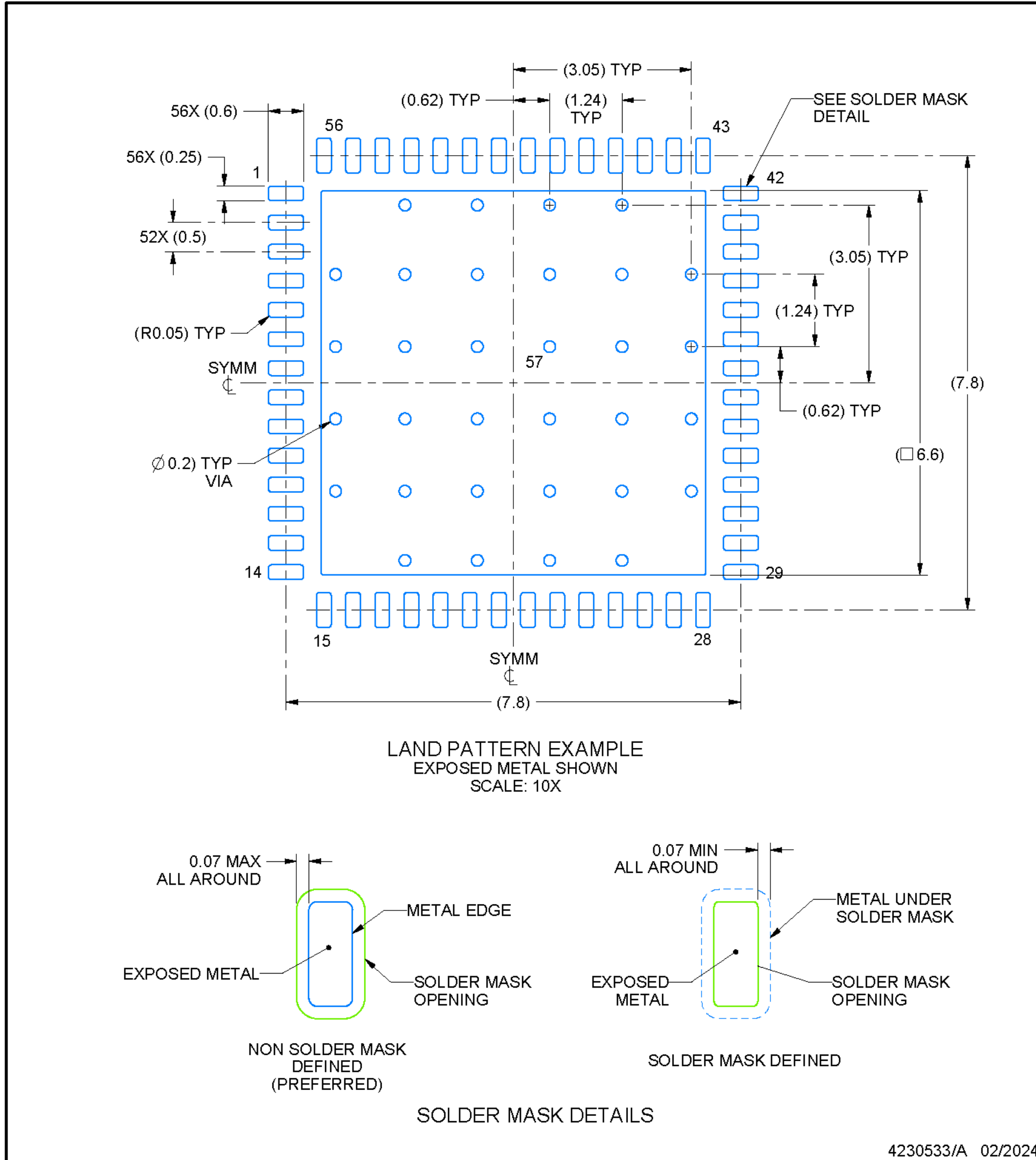

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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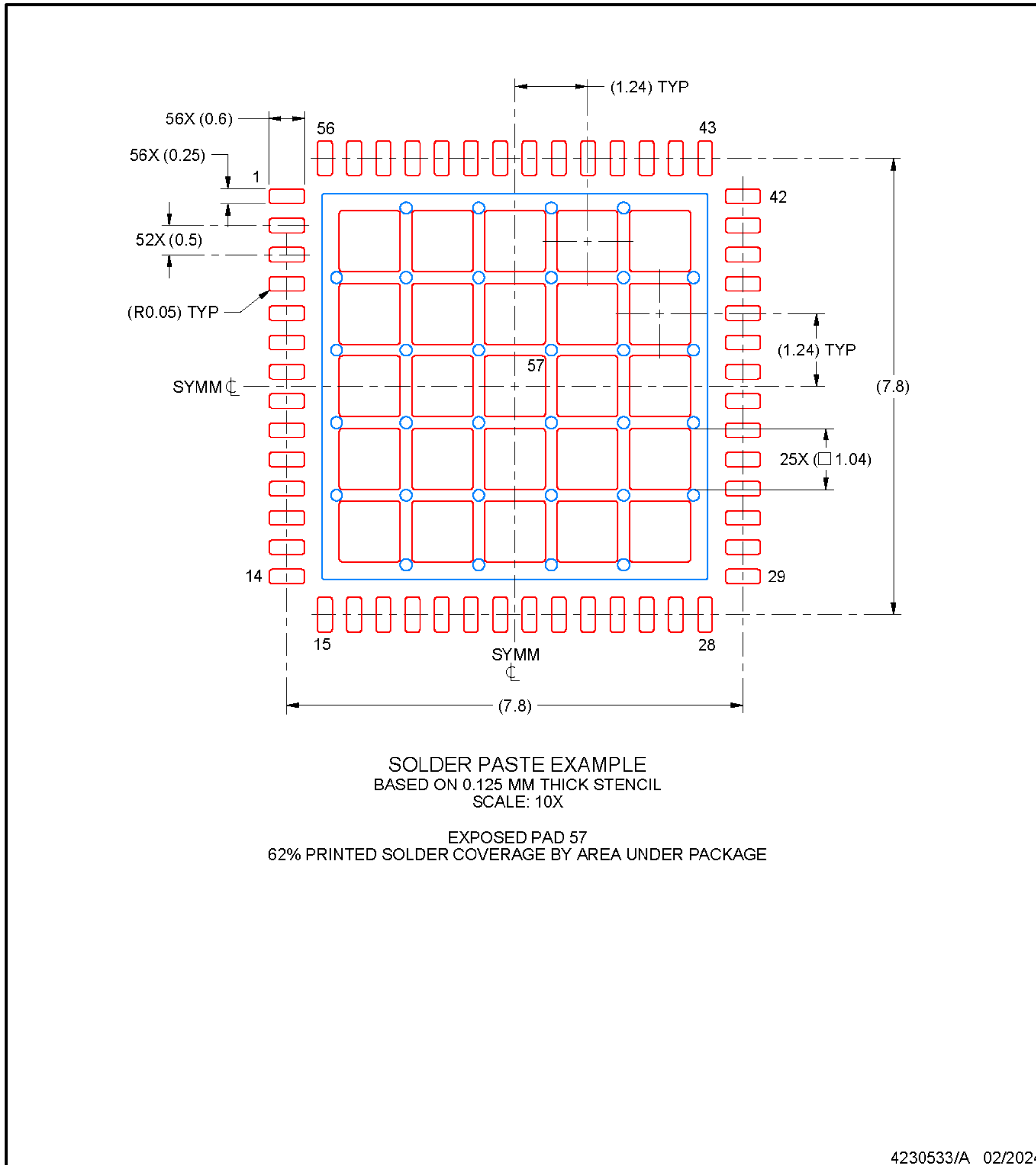
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RTQ0056K **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230533/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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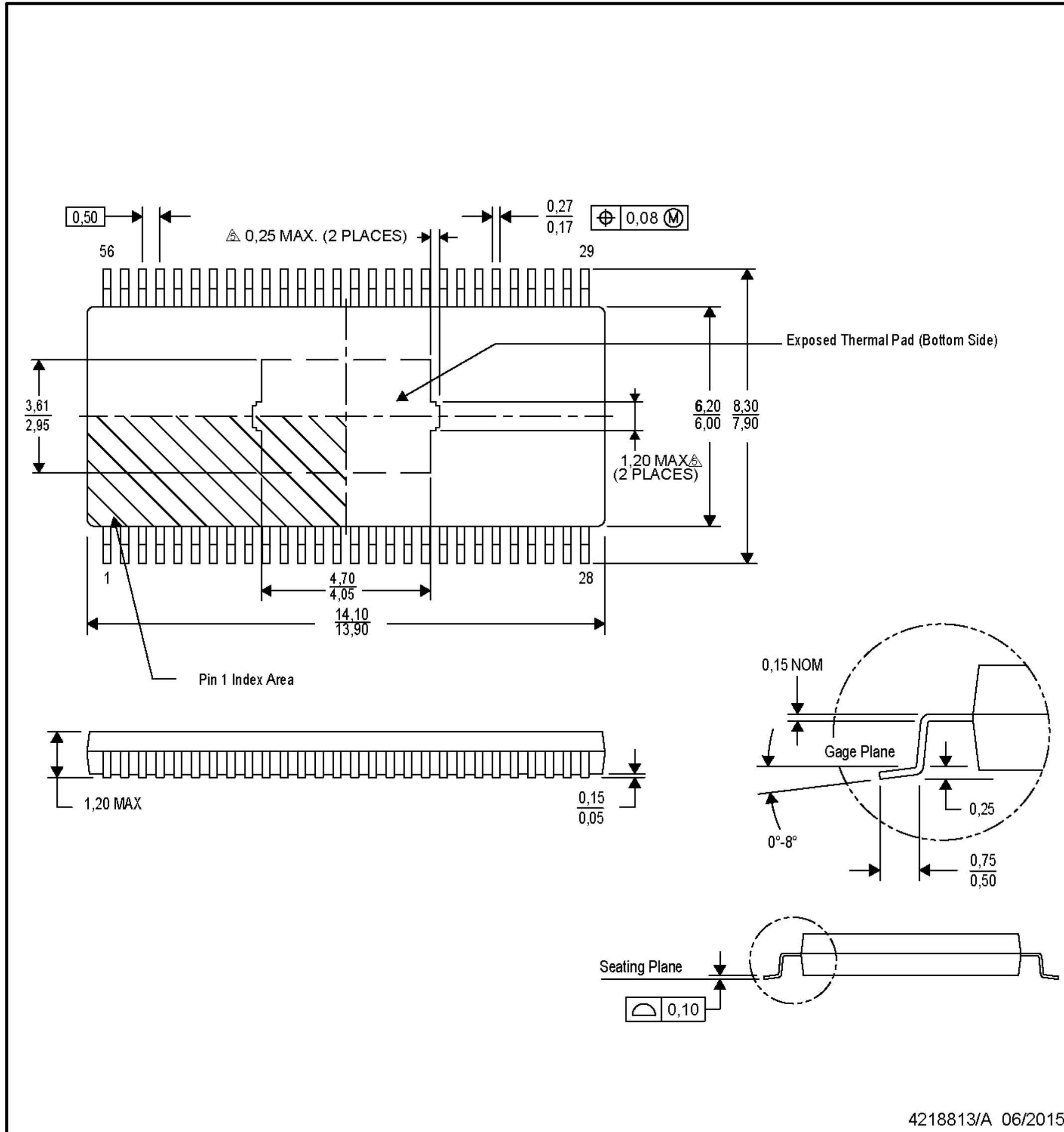
PACKAGE OUTLINE

DCA0056F

HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP



PowerPAD is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This package falls within JEDEC MO-153.
5. Keep- out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or completely absent on some devices.

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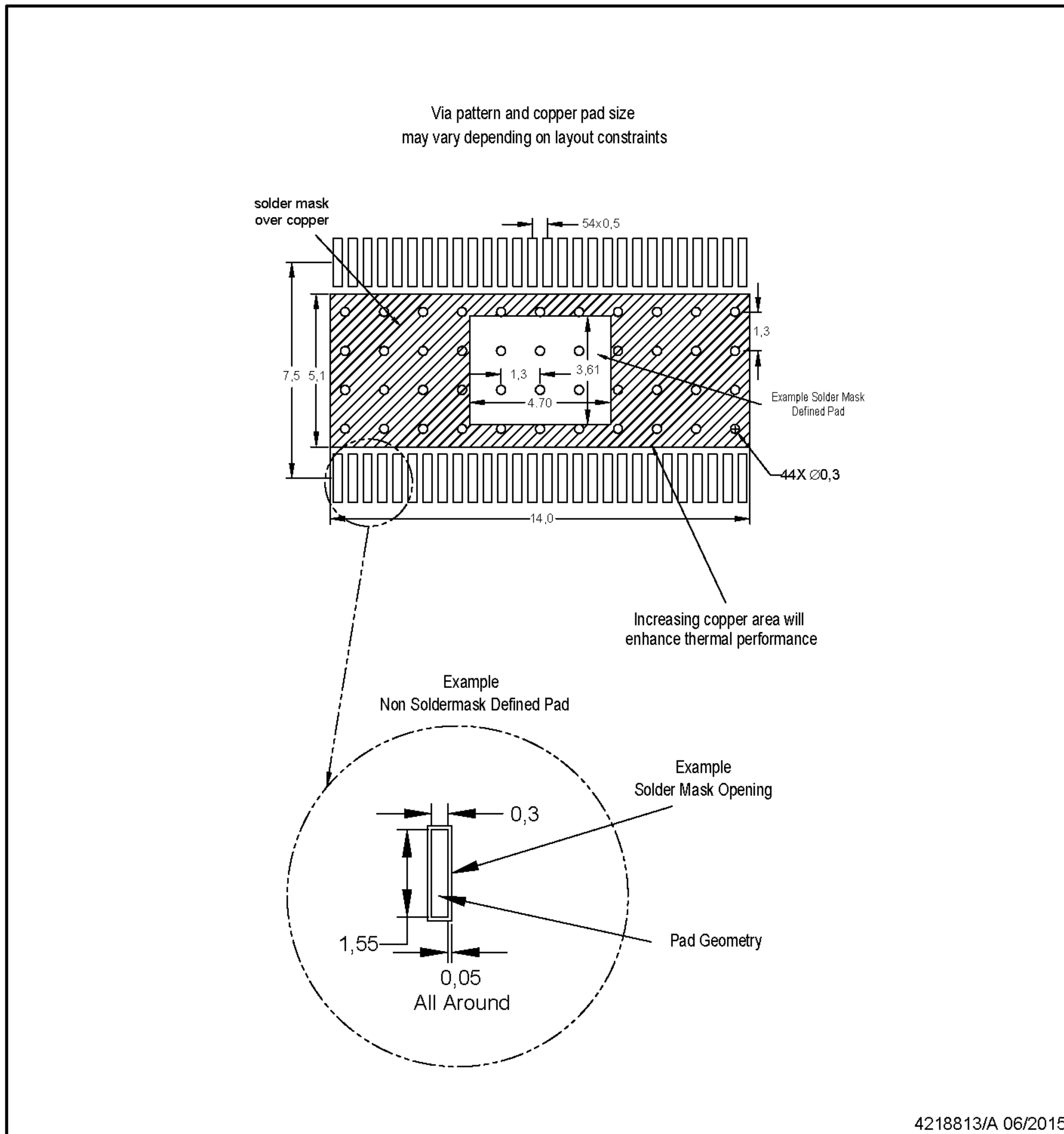
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DCA0056F HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP



4218813/A 06/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, Powerpad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

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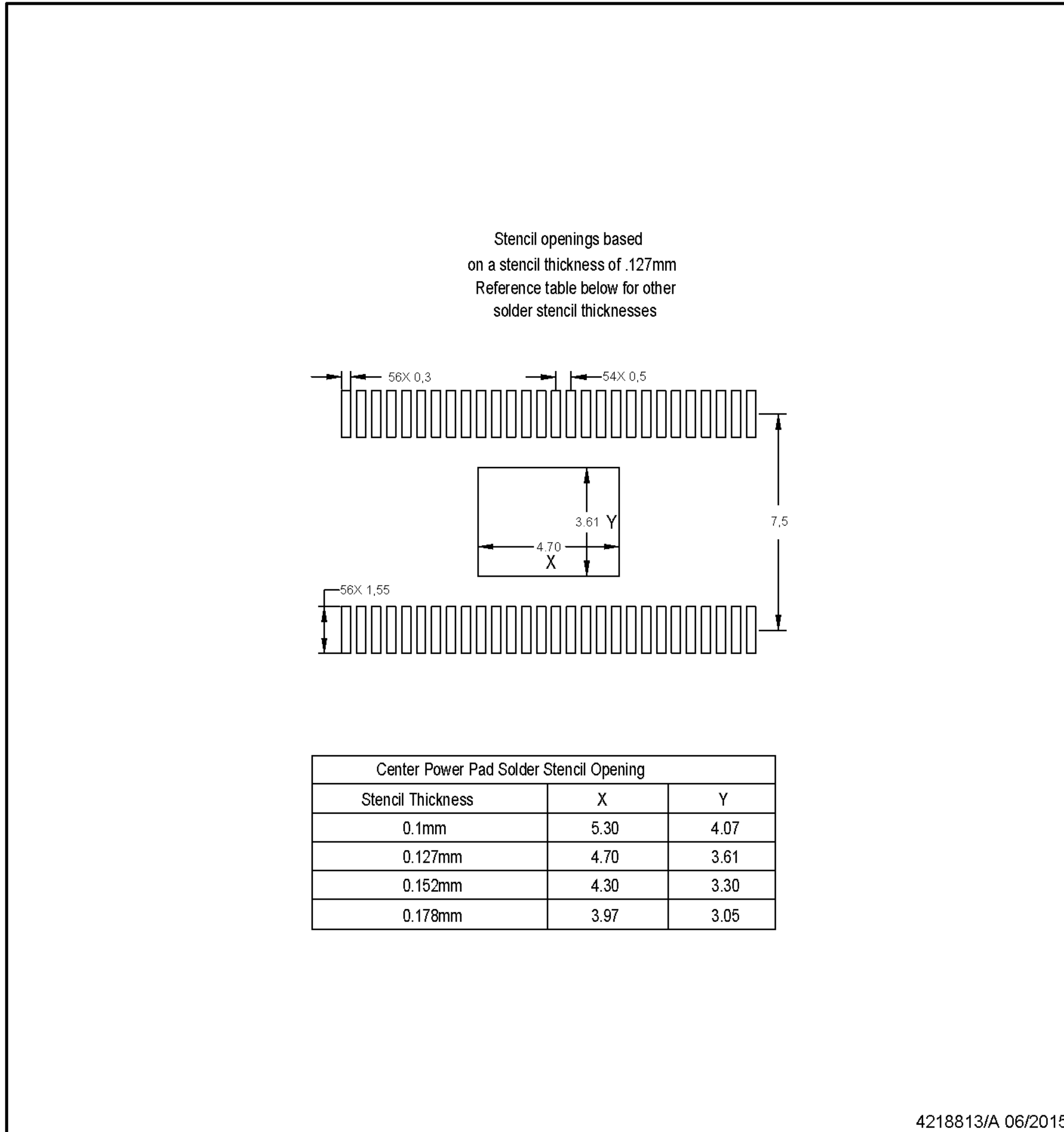

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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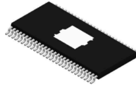
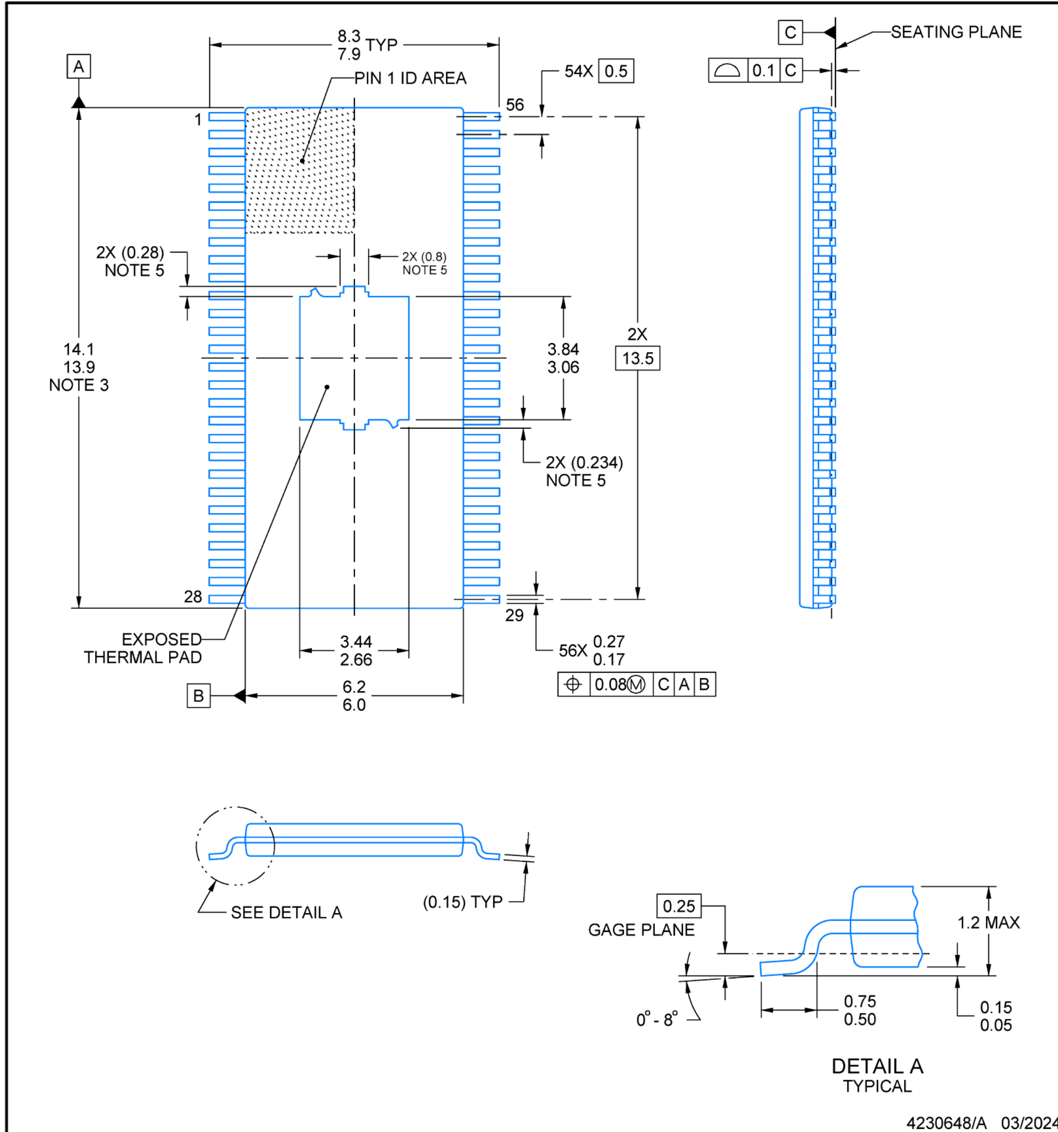


PACKAGE OUTLINE

DFD0056D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not present.
6. This package incorporates an exposed thermal pad that is designed to be attached directly to an external heat sink. This optimizes the heat transfer from the integrated circuit (IC).

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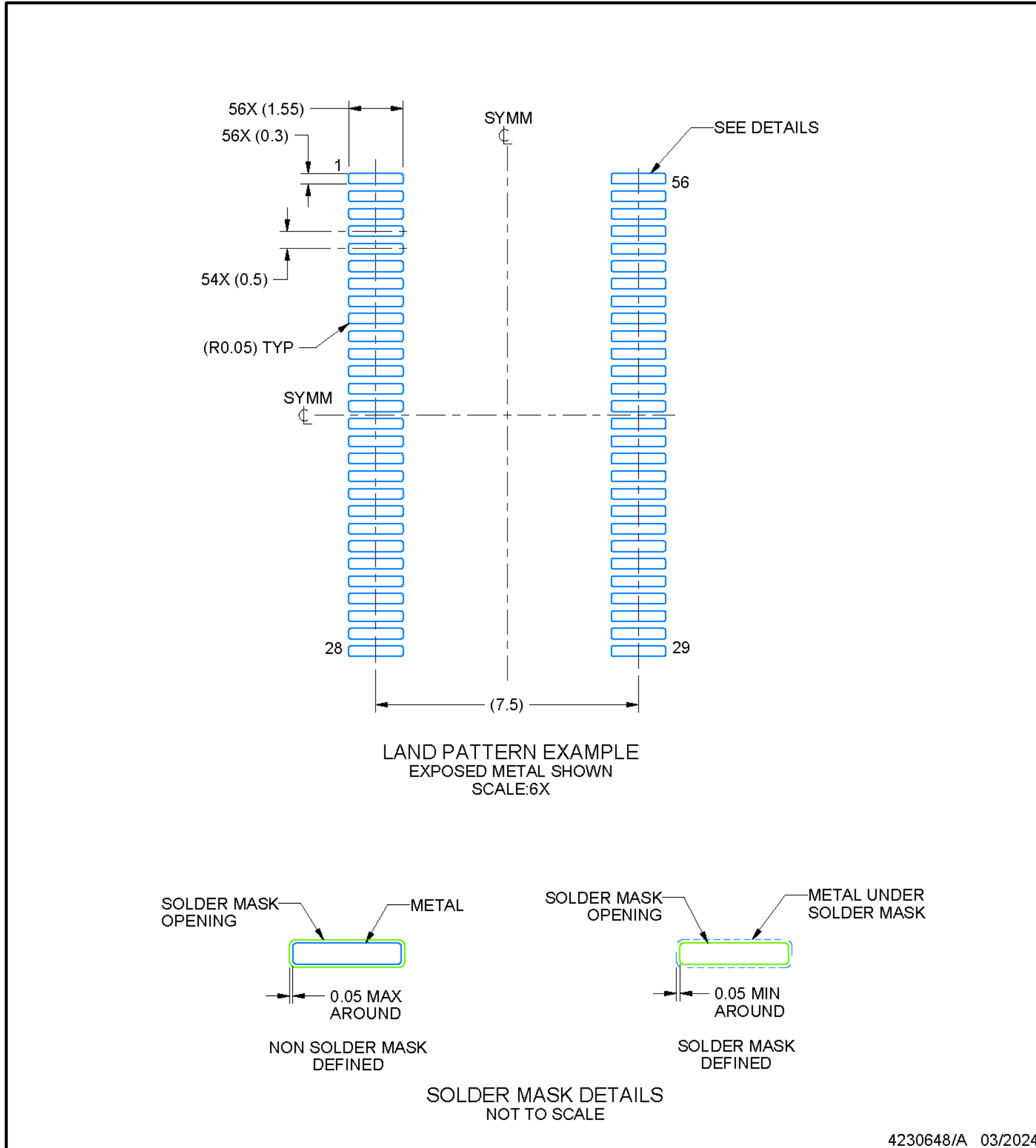
EXAMPLE BOARD LAYOUT

DFD0056D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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ADVANCE INFORMATION

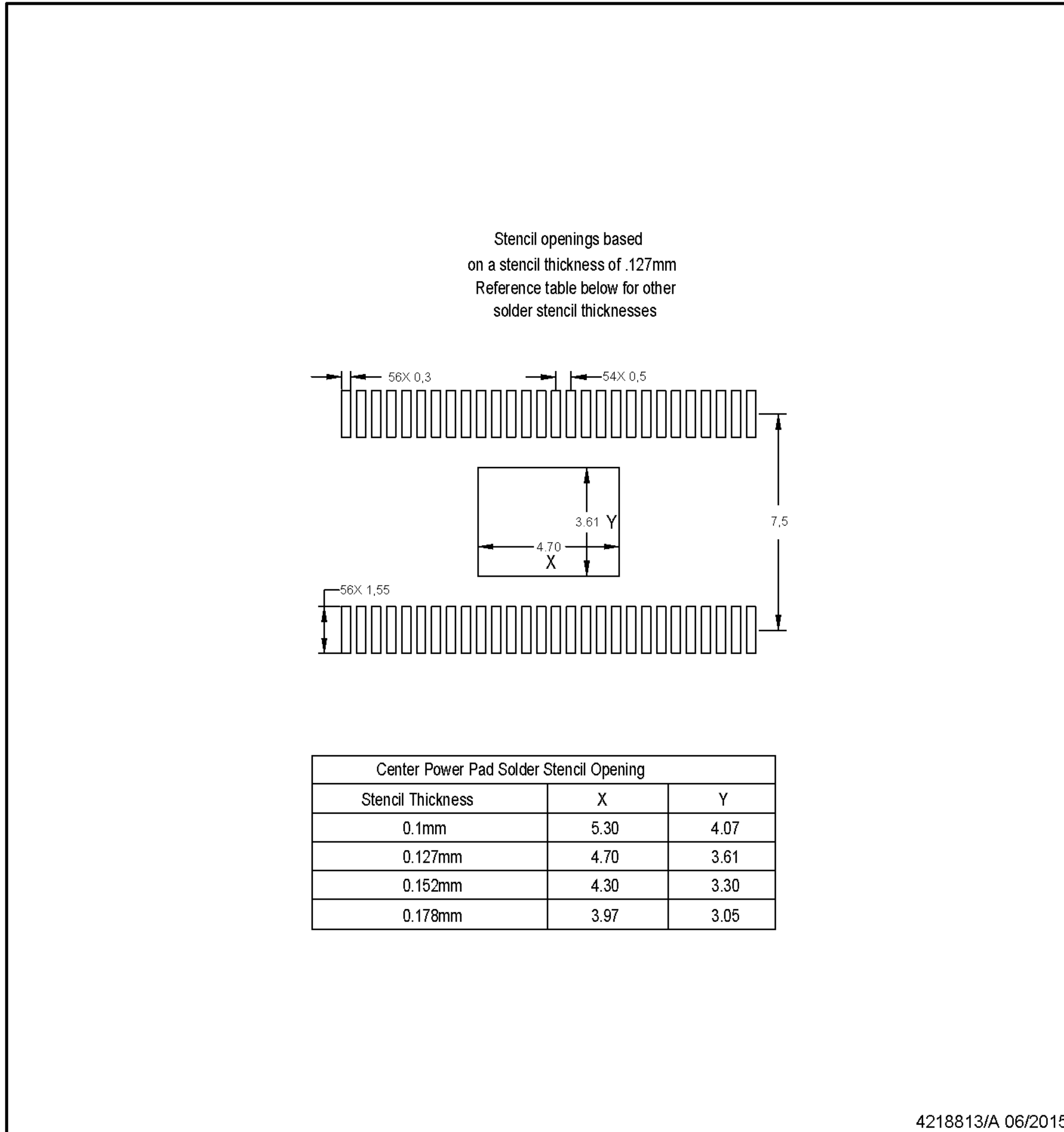
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DCA0056F

HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

4218813/A 06/2015

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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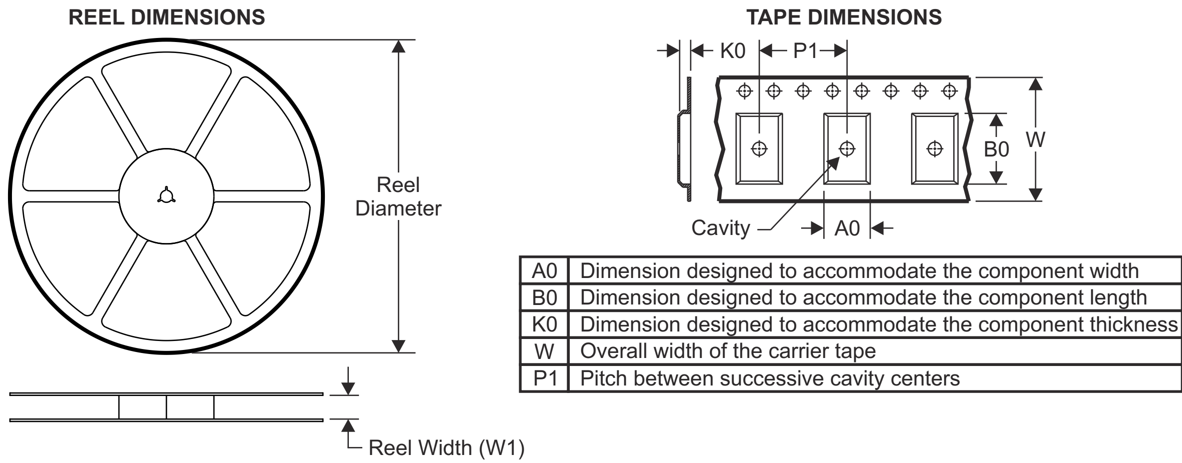
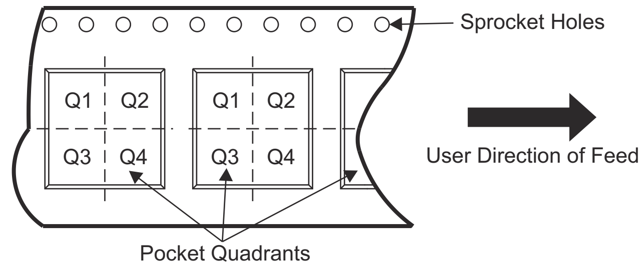
7.1 卷带包装信息



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



器件	封装类型	封装图	引脚	SPQ	卷带直径 (mm)	卷带宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限
TLC69637QDCARQ1	HTSSOP	DCA	56	2500	330	24.4	8.6	15.6	1.8	12	24	Q1
TLC69637QRTQRQ1	VQFN	RTQ	56	3500	330	16.4	8.3	8.3	1.1	12	16	Q2
TLC69637QDFDRQ1	HTSSOP	DFD	56	2500	330	24.4	8.9	14.7	1.4	12	24	Q1

ADVANCE INFORMATION

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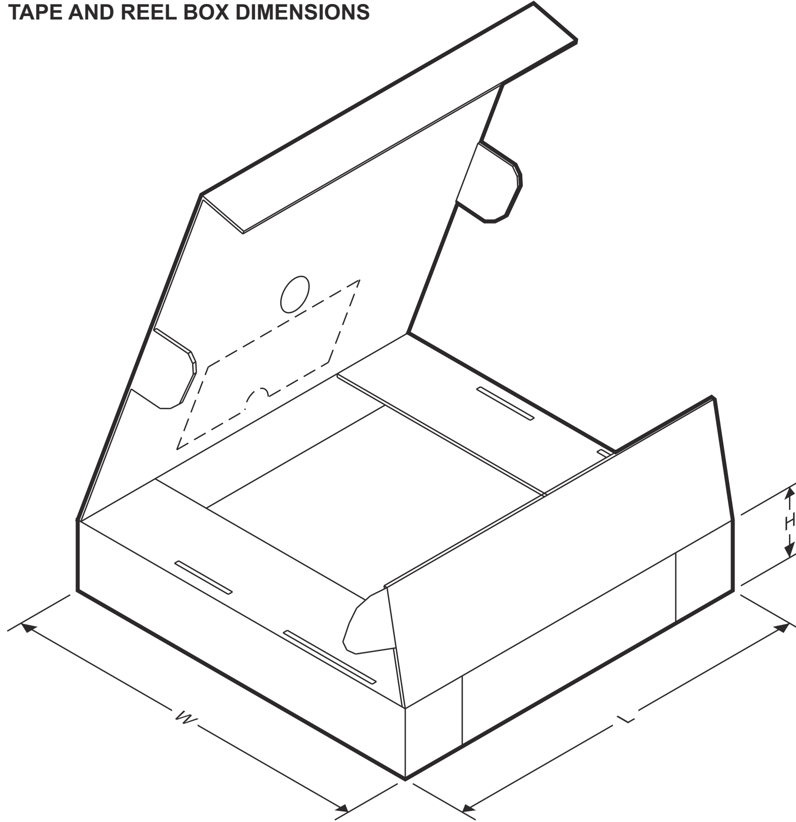
ADVANCE INFORMATION



器件	封装类型	封装图	引脚	SPQ	长度 (mm)	宽度 (mm)	高度 (mm)
TLC69637QDCARQ1	HTSSOP	DCA	56	2500	367	367	45
TLC69637QRTQRQ1	VQFN	RTQ	56	3500	367	367	35
TLC69637QDFDRQ1	HTSSOP	DFD	56	2500	350	350	43

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLC69637QRTQRQ1	ACTIVE	QFN	RTQ	56	3500	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

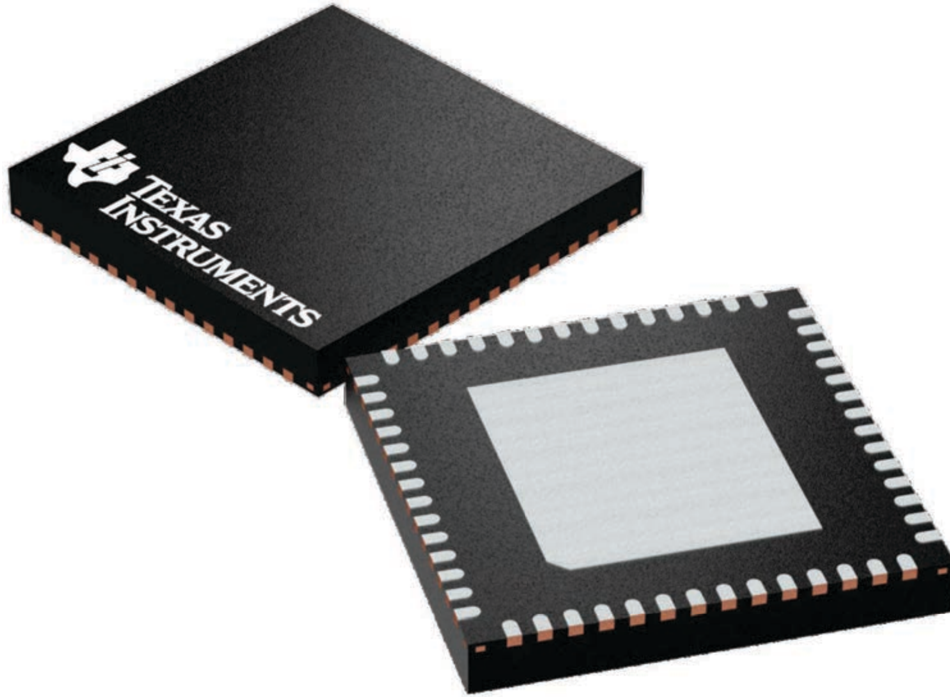
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

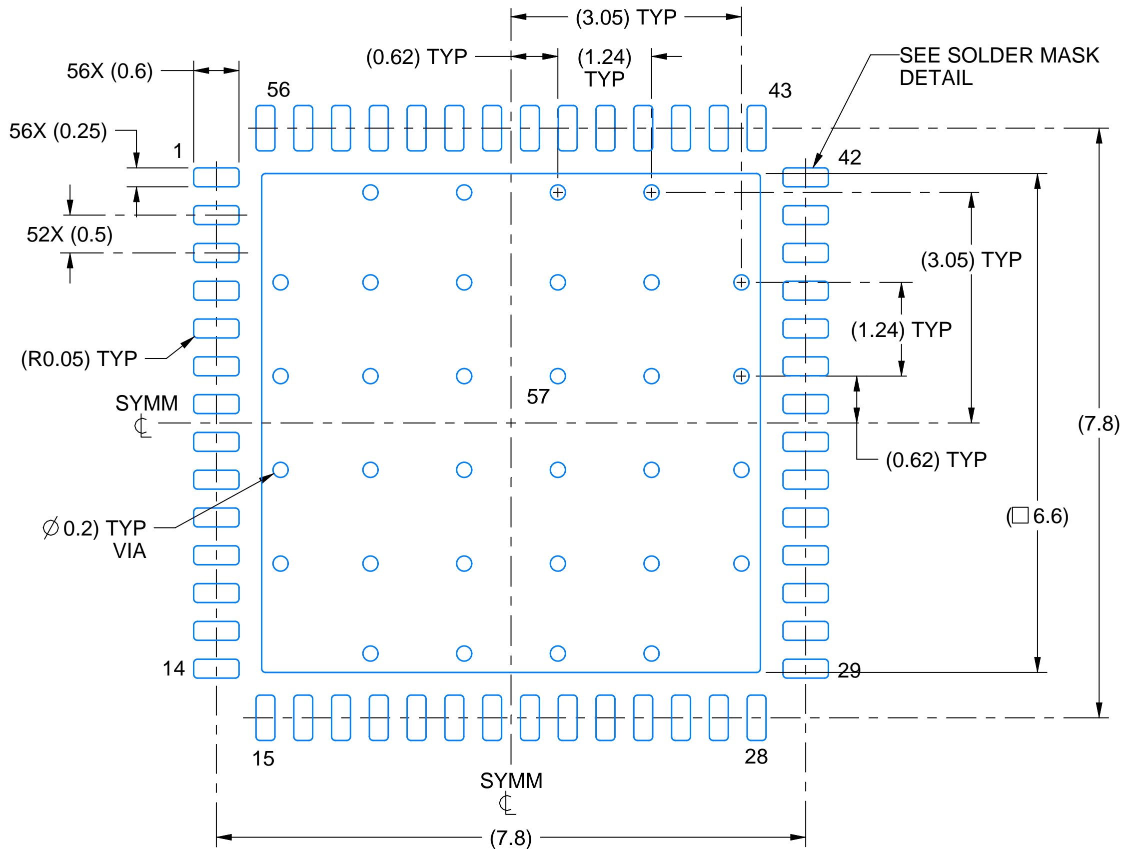


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

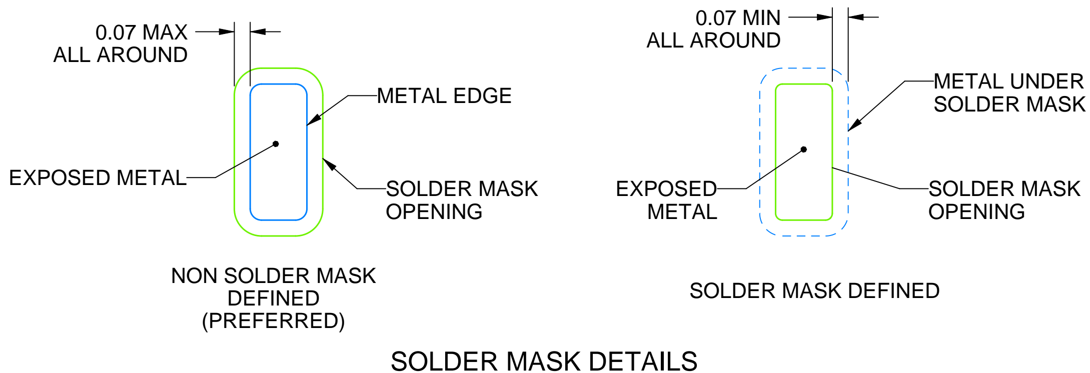
4224653/A

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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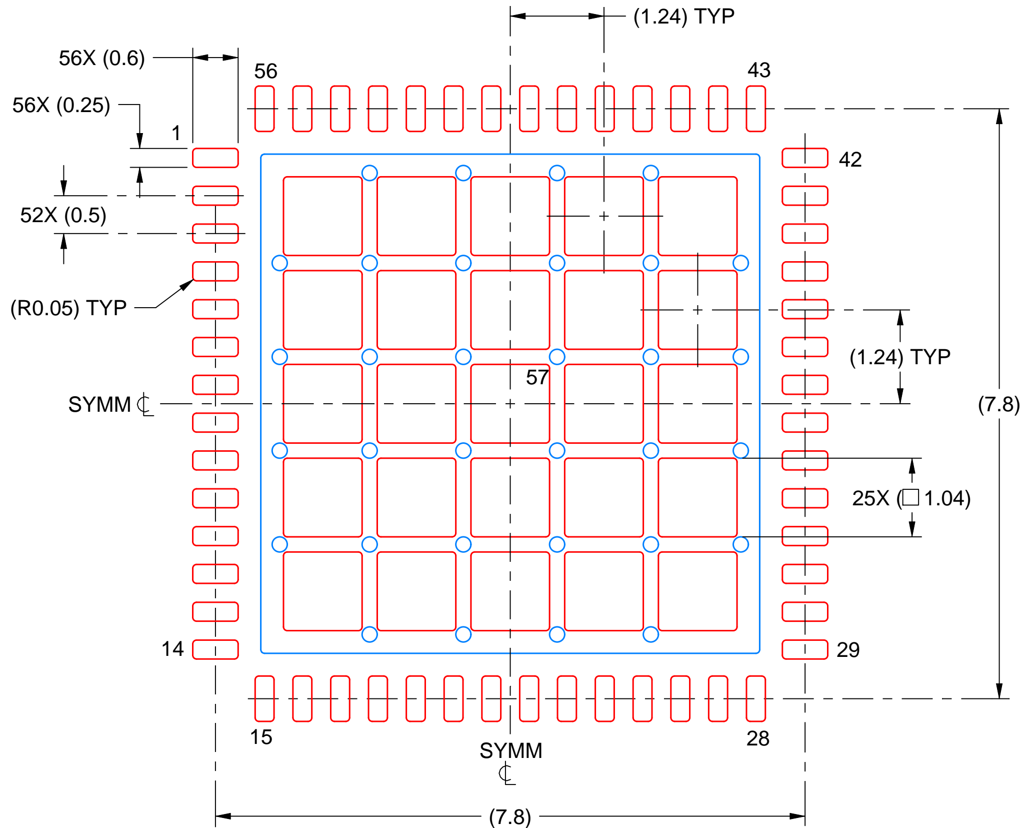
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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