TLC69639-Q1 汽车级 100mA、48 通道 LED 驱动器，配备集成振荡器、高级诊断功能和级联串行接口

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 1 级：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM 分类等级 H1C
  - 器件 CDM 分类等级 C4B
- 符合功能安全标准
  - 专为功能安全应用开发
  - 有助于使 ISO 26262 系统设计满足 ASIL B 级别要求的文档
- 48 个集成的电流吸收器
  - 可编程的 16 位 PWM/混合调光
  - 可编程的 7 位模拟点校正 (DC)
  - 最大输出电流、电压：100mA，16V
- 集成的 33MHz 振荡器
  - 500Hz 的 16 位 PWM 输出
  - 采用增强频谱 (ES) PWM 时，刷新率大于 20KHz
- 高速通信
  - 级联串行接口 (CSI)
  - 数据速率高达 17Mbps
- 电源效率优化
  - 自适应余量电压控制 (AHVC)
  - 器件节电模式 (PSM)
- 降低 EMI
  - 接口：可编程缓冲器驱动能力
  - 电流吸收器：相移/展频
- 保护和诊断
  - LED：开路/短路检测/运行状况检查
  - 电流吸收器：相邻引脚短路/运行状况检查
  - 接口：CRC/命令错误/超时错误/通信看门狗
  - 器件：欠压/ISET 超出范围/热关断/存储器 CRC/OTP CRC/OSC 看门狗

2 应用

- 汽车中心信息显示器
- 汽车仪表组显示器
- 汽车抬头显示器

3 说明

TLC69639-Q1 是一款 LED 驱动器，它具有 48 条恒定电流吸收器通道，可提供高达 16 位的独立像素级 LED PWM 控制。每条通道还实施额外的 7 位点校正 (DC) 以控制峰值电流。每个器件通过级联串行接口 (CSI) 共享数据流，其最多支持 511 个器件的连接。该接口与同一组中的 LED 驱动器软件兼容，可根据 LED 电流和 LED 总数应用于不同的应用场景。

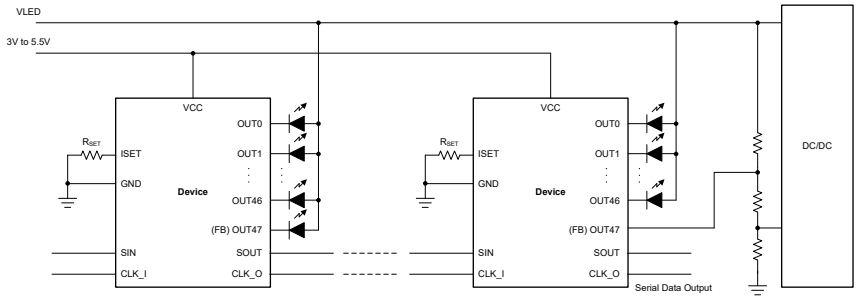
为了优化整体系统电源效率，该器件配备了自适应余量电压控制 (AHVC) 方案，用于优化每条通道和每个器件的余量电压。只需要将菊花链最后一个器件的 OUT47 引脚编程为 FB 引脚，即可优化来自 DC/DC 的 LED 电源电压。

TLC69639-Q1 配备了 LED、电流吸收器、通信和器件的诊断功能。

封装信息

器件型号	封装(1)	封装尺寸(2)
TLC69639-Q1	RTQ（VQFN，56）可湿性侧面	8mm × 8mm
	DCA（HTSSOP，56）	14mm × 8.1mm
	DFD（HTSSOP，56）	

(1) 有关更多信息，请参阅 节 7。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化版原理图

内容

4 器件比较

器件型号	通道编号	最大值通道电流	功能安全分类	接口	软件兼容
TLC69621-Q1 (1)	8	60mA	功能安全型	SPI	组 1
TLC69624-Q1 (1)	24				
TLC69627-Q1	48				
TLC69631-Q1 (1)	8	100mA			
TLC69634-Q1 (1)	24				
TLC69637-Q1	48				
TLC69622-Q1 (1)	8	60mA	符合功能安全标准	SPI	组 2
TLC69625-Q1 (1)	24				
TLC69628-Q1	48				
TLC69632-Q1 (1)	8	100mA			
TLC69635-Q1 (1)	24				
TLC69638-Q1	48				
TLC69623-Q1 (1)	8	60mA	符合功能安全标准	CSI	组 3
TLC69626-Q1 (1)	24				
TLC69629-Q1	48				
TLC69633-Q1 (1)	8	100mA			
TLC69636-Q1 (1)	24				
TLC69639-Q1	48				

(1) 产品预发布

5 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

5.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (January 2025) to Revision A (August 2025)	Page
• 将文档状态从“预告信息”更改为“量产数据”	1

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

封装选项附录

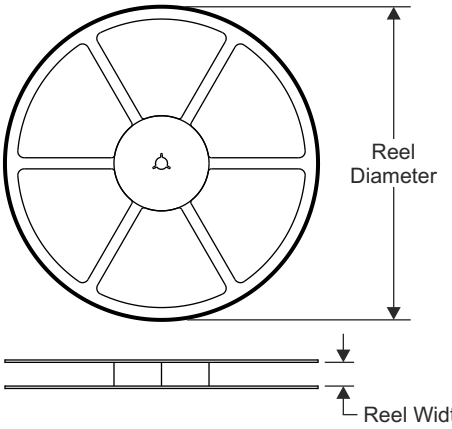
封装信息

可订购器件型号	状态 (1)	材料类型 (2)	封装 | 引脚	包装数量 | 包装	RoHS (3)	引脚镀层/焊球材料 (4)	MSL 等级/回流焊峰值温度 (5)	工作温度 (°C)	器件标识 (6)
TLC69639QDCARQ1	有效	生产	HTSSOP (DCA) | 56	2500 | LARGE T&R	是	NIPDAU	2 级-260C-1 年	-40 至 125	TLC69639Q1
TLC69639QDFDRQ1	有效	生产	HTSSOP (DFD) | 56	2500 | LARGE T&R	是	NIPDAU	2 级-260C-1 年	-40 至 125	69639Q
TLC69639QRTQRQ1	有效	生产	VQFN (RTQ) | 56	3500 | LARGE T&R	是	NIPDAU	2 级-260C-1 年	-40 至 125	69639Q1

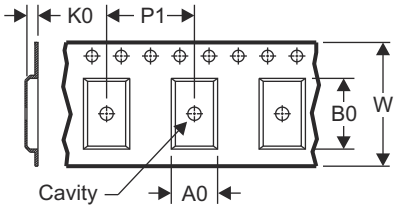
(1) **状态：**有关状态的详细信息，请参阅我们的产品生命周期。
(2) **材料类型：**指定时，预量产器件是原型/试验器件，尚未获批或发布以进行全面生产。测试和最终工艺（包括但不限于质量保证、可靠性测试以及/或工艺鉴定）可能尚未完成，并且本器件可能会进一步更改，也可能中断研发。即使可供订购，所购器件仍将可能在结算时被取消，并且所购器件仅可用于早期内部评估。这些器件一经售出，概不提供任何保修。
(3) **RoHS 值：**是、否、RoHS 豁免。有关更多信息和值定义，请参阅“TI RoHS 声明”。
(4) **引脚镀层/焊球材料：**器件可能有多种材料镀层选项。各镀层选项用垂直线隔开。如果铅镀层/焊球值超出最大列宽，则会折为两行。
(5) **MSL 等级/回流焊峰值温度：**湿敏等级等级和峰值焊接（回流焊）温度。如果器件具有多个湿敏等级，则仅显示符合 JEDEC 标准的最低等级。有关将器件安装到印刷电路板上时采用的实际回流焊温度，请参阅装运标签。
(6) **器件标识：**器件上可能还有与徽标、批次跟踪代码信息或环境分类相关的其他标识。
如有多个器件标识，将用括号括起来。不过，器件上仅显示括号中以“~”隔开的其中一个器件标识。如果某一行缩进，说明该行续接上一行，这两行合在一起表示该器件的完整器件标识。

7.1 卷带包装信息

REEL DIMENSIONS

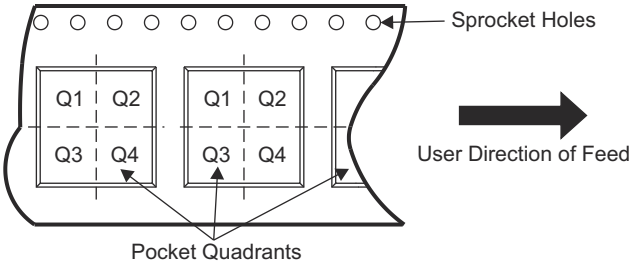


TAPE DIMENSIONS



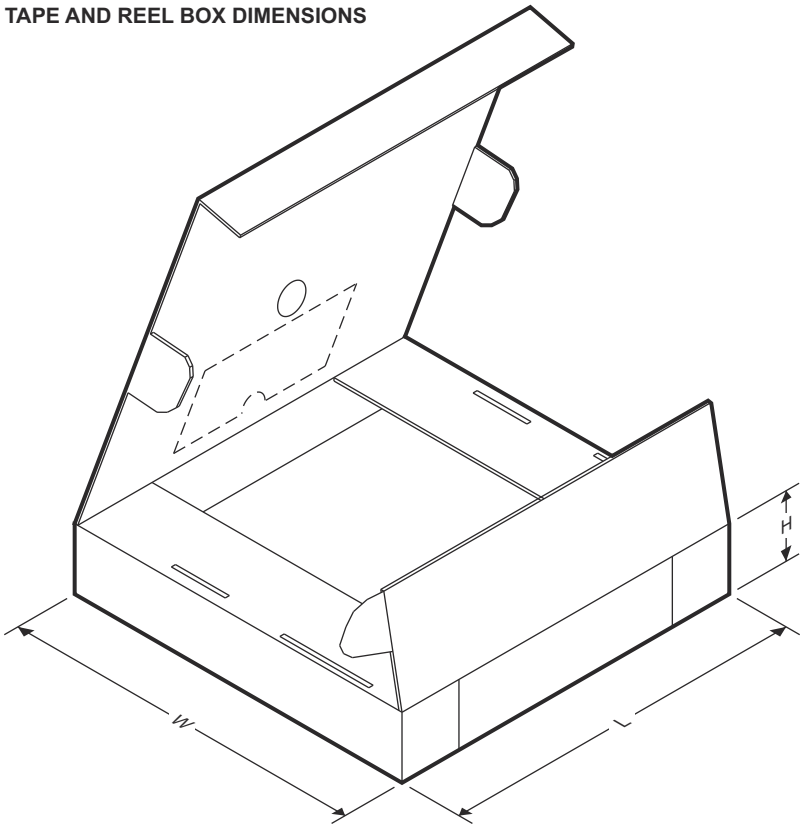
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



器件	封装类型	封装图	引脚	SPQ	卷带直径 (mm)	卷带宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1象限
TLC69639QDCARQ1	HTSSOP	DCA	56	2500	330	24.4	8.6	15.6	1.8	12	24	Q1
TLC69639QRTQRQ1	VQFN	RTQ	56	3500	330	16.4	8.3	8.3	1.1	12	16	Q2
TLC69639QDFDRQ1	HTSSOP	DFD	56	2500	330	24.4	8.9	14.7	1.4	12	24	Q1

TAPE AND REEL BOX DIMENSIONS



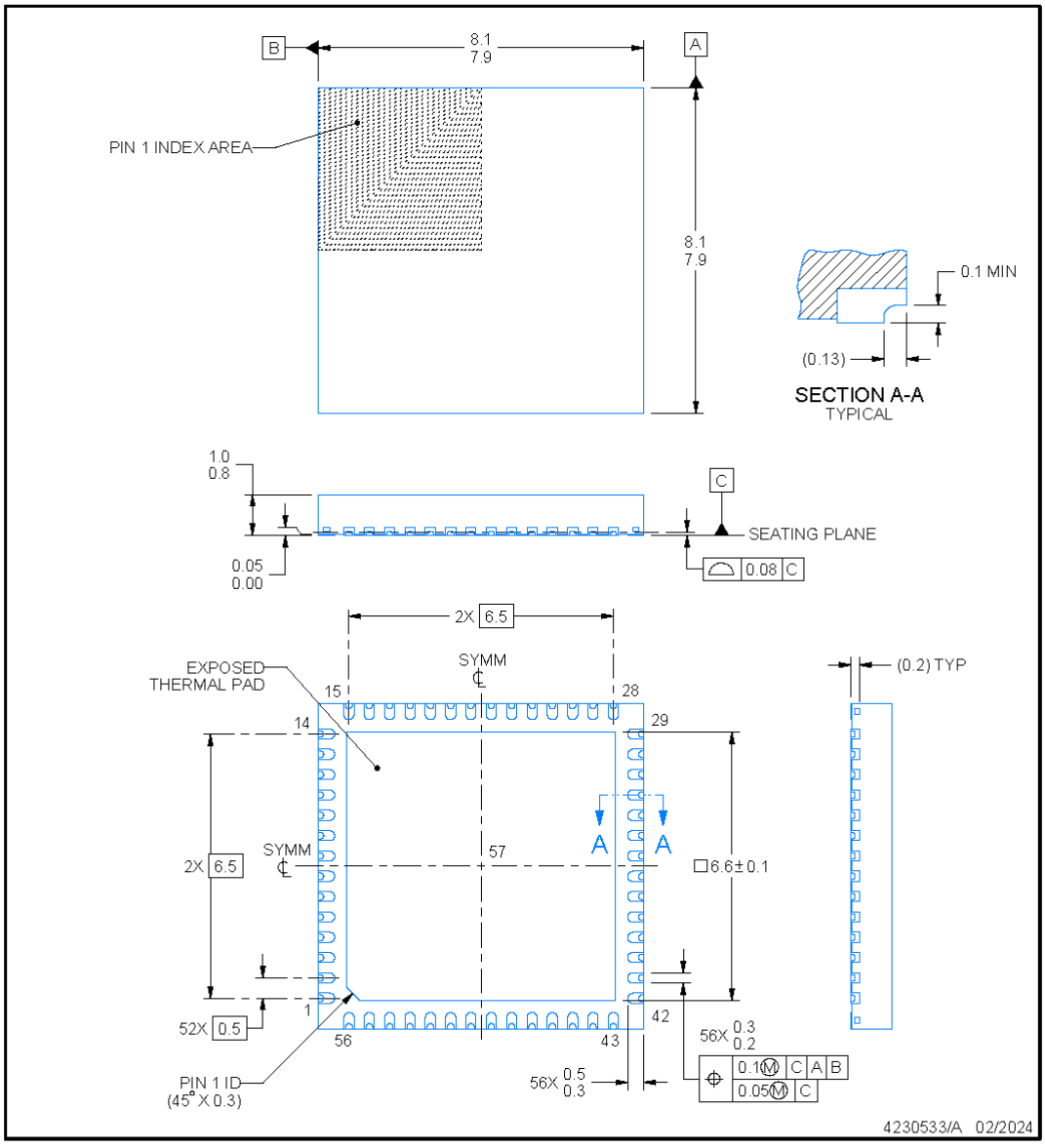
器件	封装类型	封装图	引脚	SPQ	长度 (mm)	宽度 (mm)	高度 (mm)
TLC69639QDCARQ1	HTSSOP	DCA	56	2500	367	367	45
TLC69639QRTQRQ1	VQFN	RTQ	56	3500	367	367	35
TLC69639QDFDRQ1	HTSSOP	DFD	56	2500	350	350	43

PACKAGE OUTLINE

RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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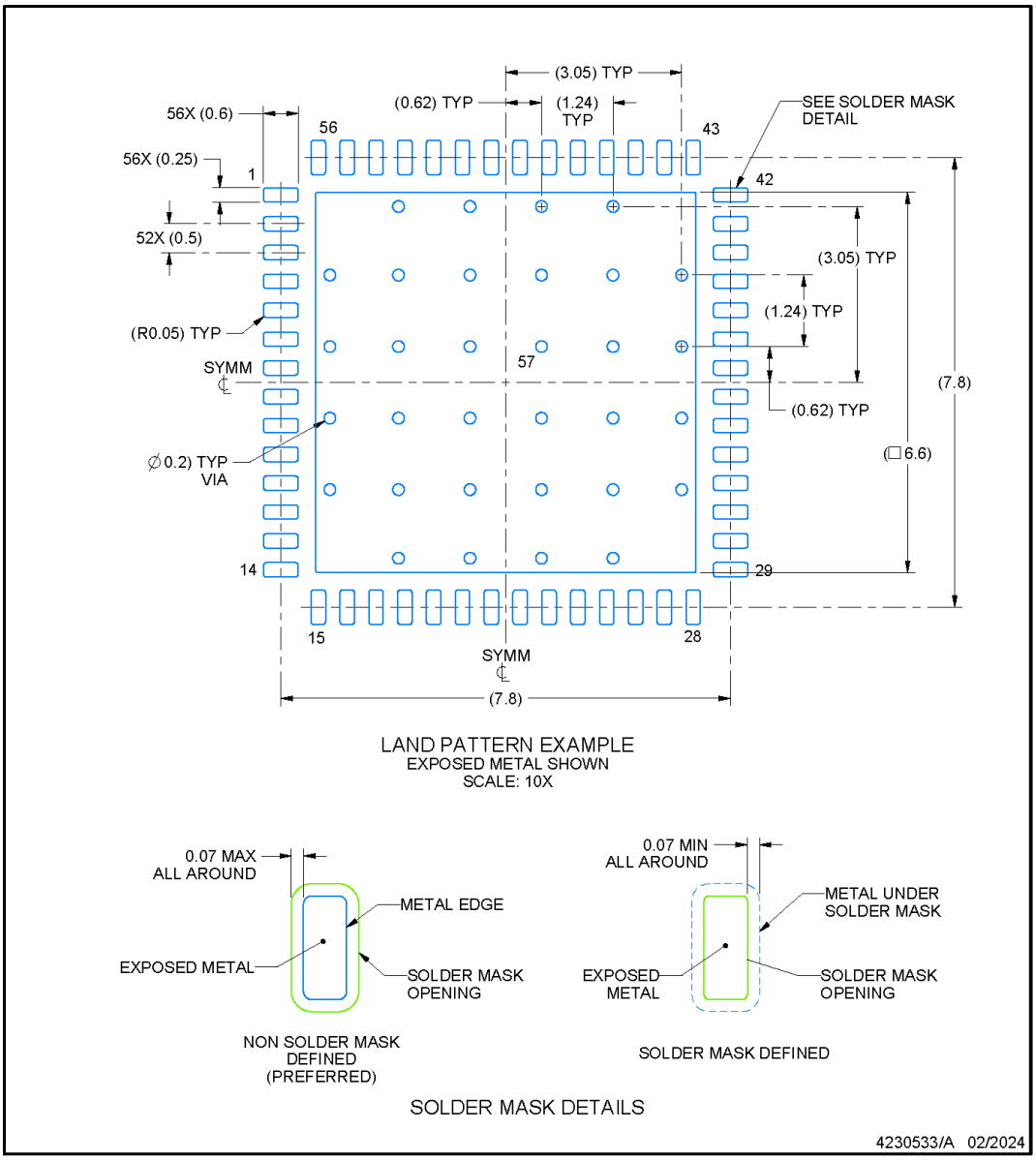
EXAMPLE BOARD LAYOUT

RTQ0056K — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



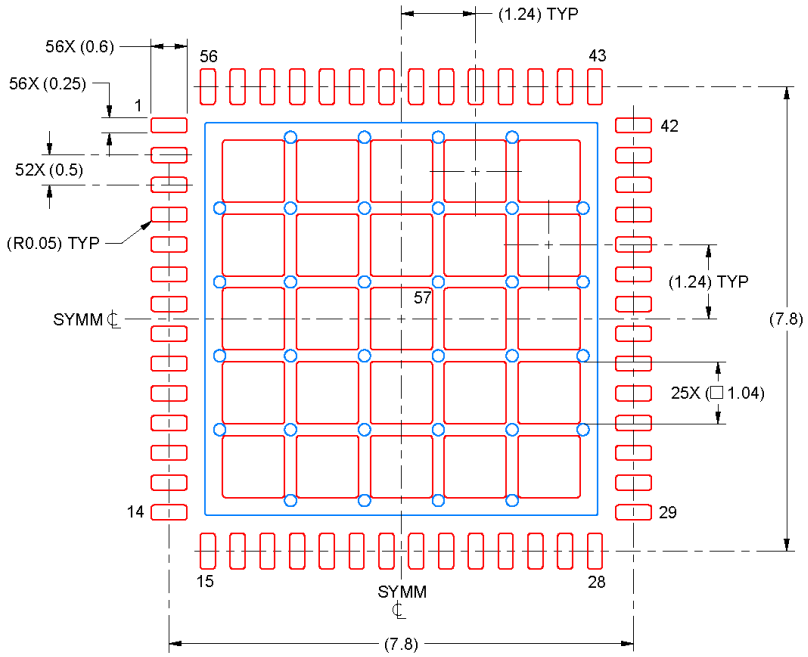
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTQ0056K — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230533/A 02/2024

NOTES: (continued)

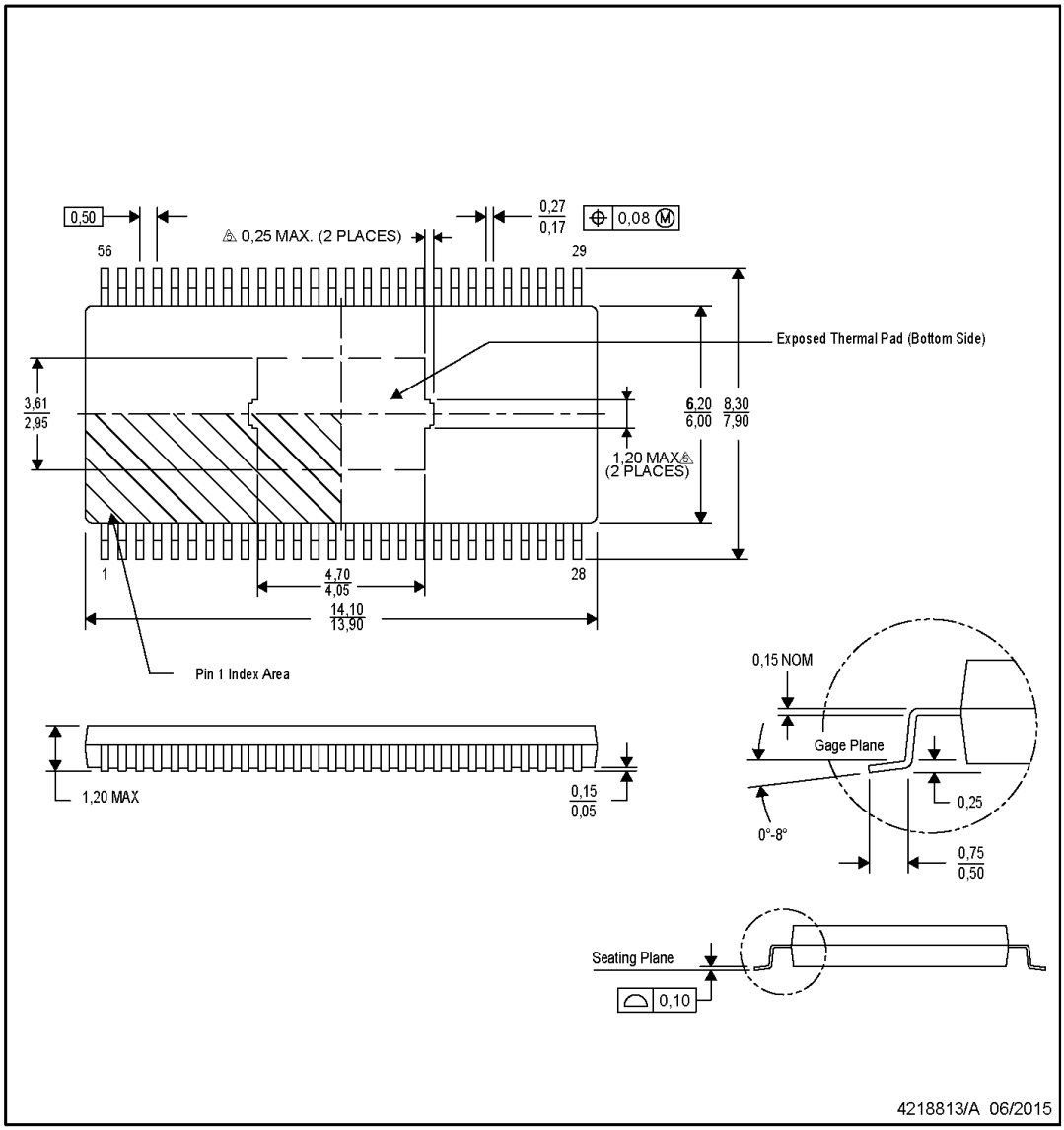
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCA0056F

HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP



PowerPAD is a trademark of Texas Instruments

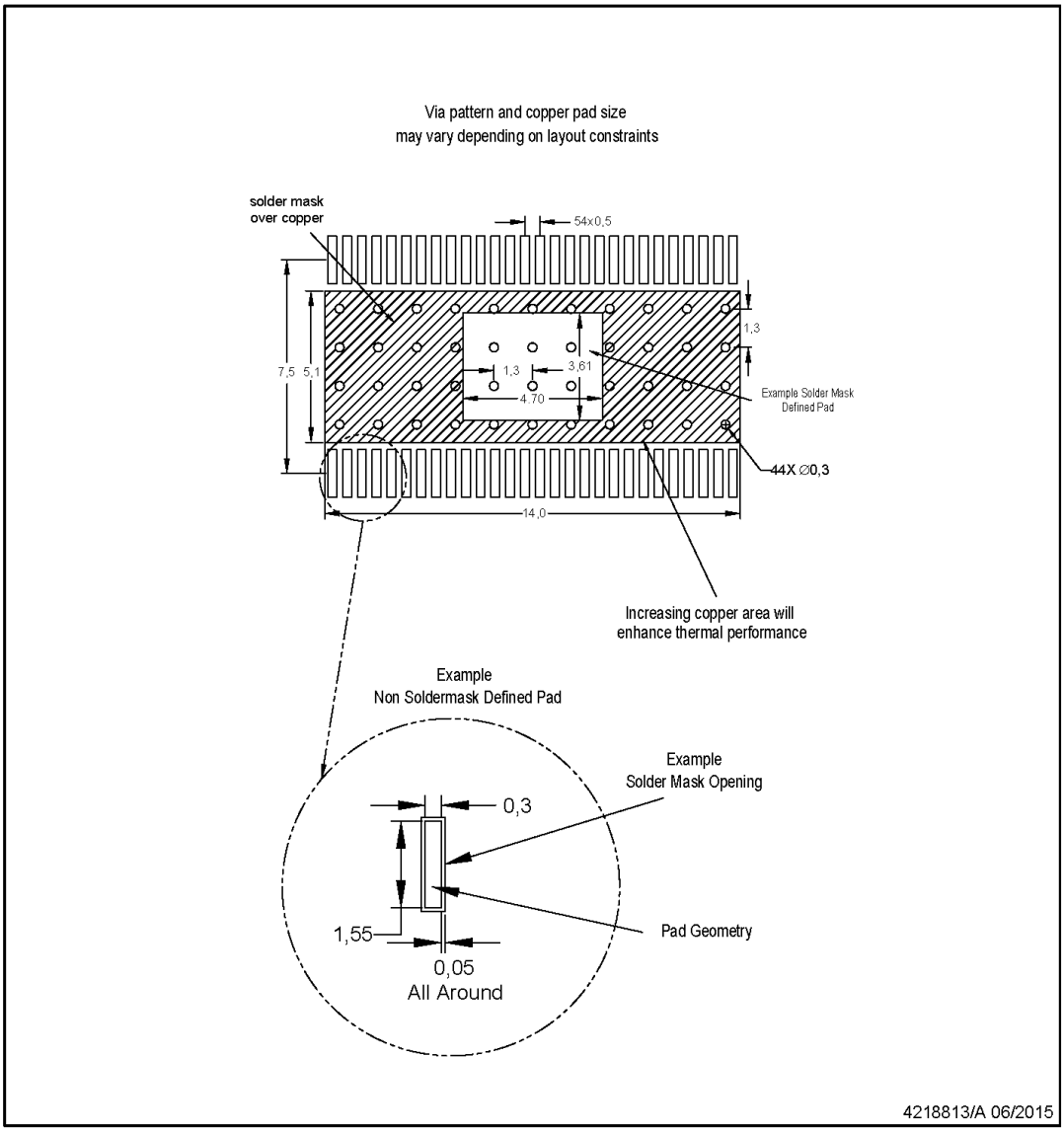
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This package falls within JEDEC MO-153.
5. Keep- out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or completely absent on some devices.

EXAMPLE BOARD LAYOUT

DCA0056F — **HTSSOP - 1.2 mm max height**

PowerPAD™ HTSSOP



NOTES: (continued)

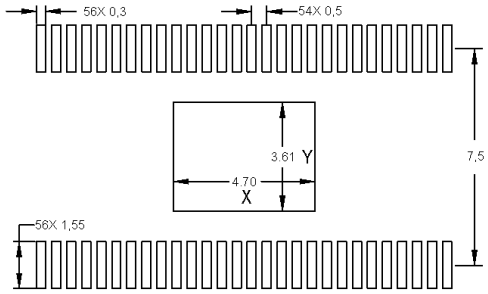
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, Powerpad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

DCA0056F — **HTSSOP - 1.2 mm max height**

PowerPAD™ HTSSOP

Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

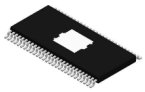
4218813/A 06/2015

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

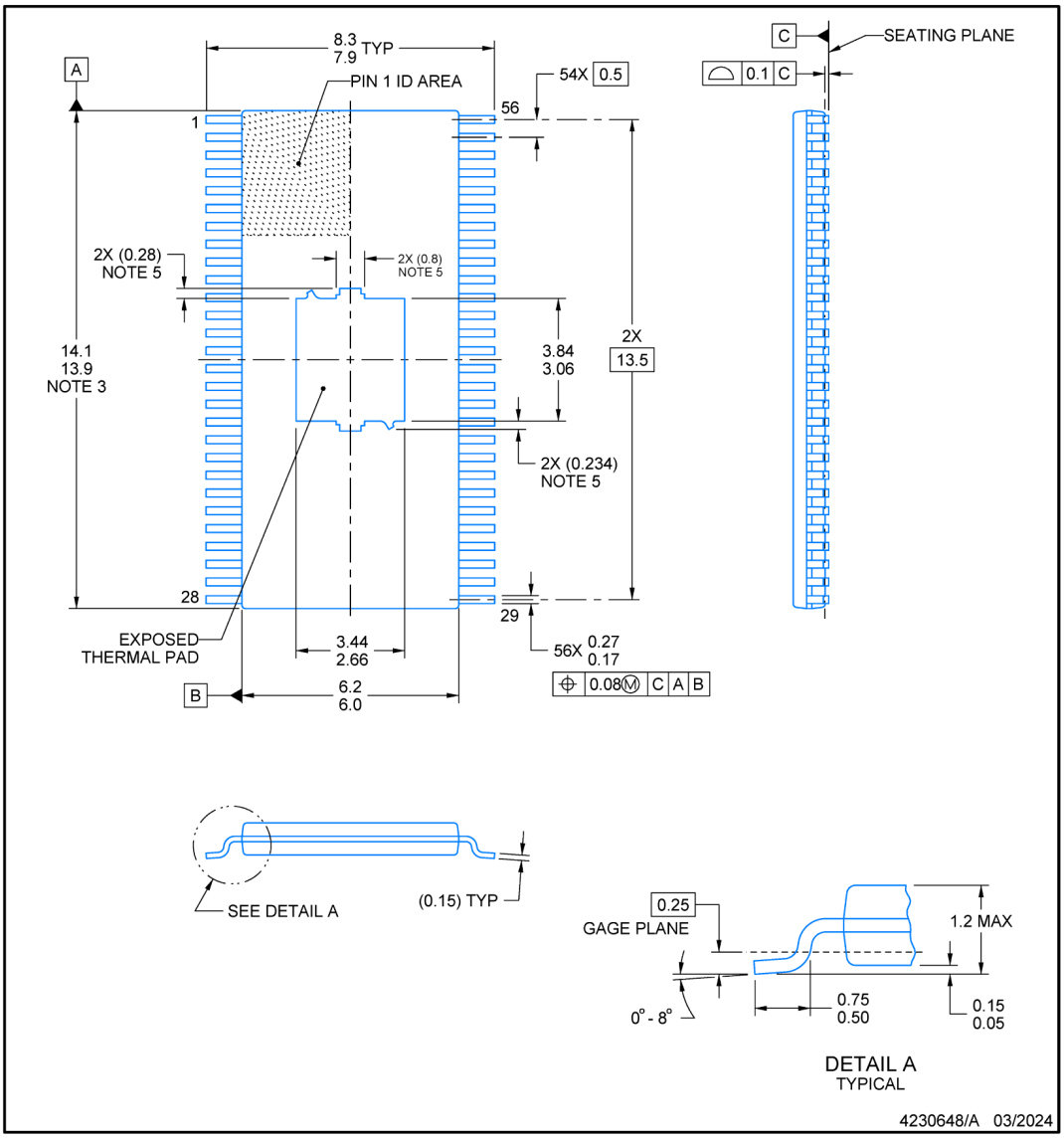
PACKAGE OUTLINE

DFD0056D



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not present.
6. This package incorporates an exposed thermal pad that is designed to be attached directly to an external heat sink. This optimizes the heat transfer from the integrated circuit (IC).

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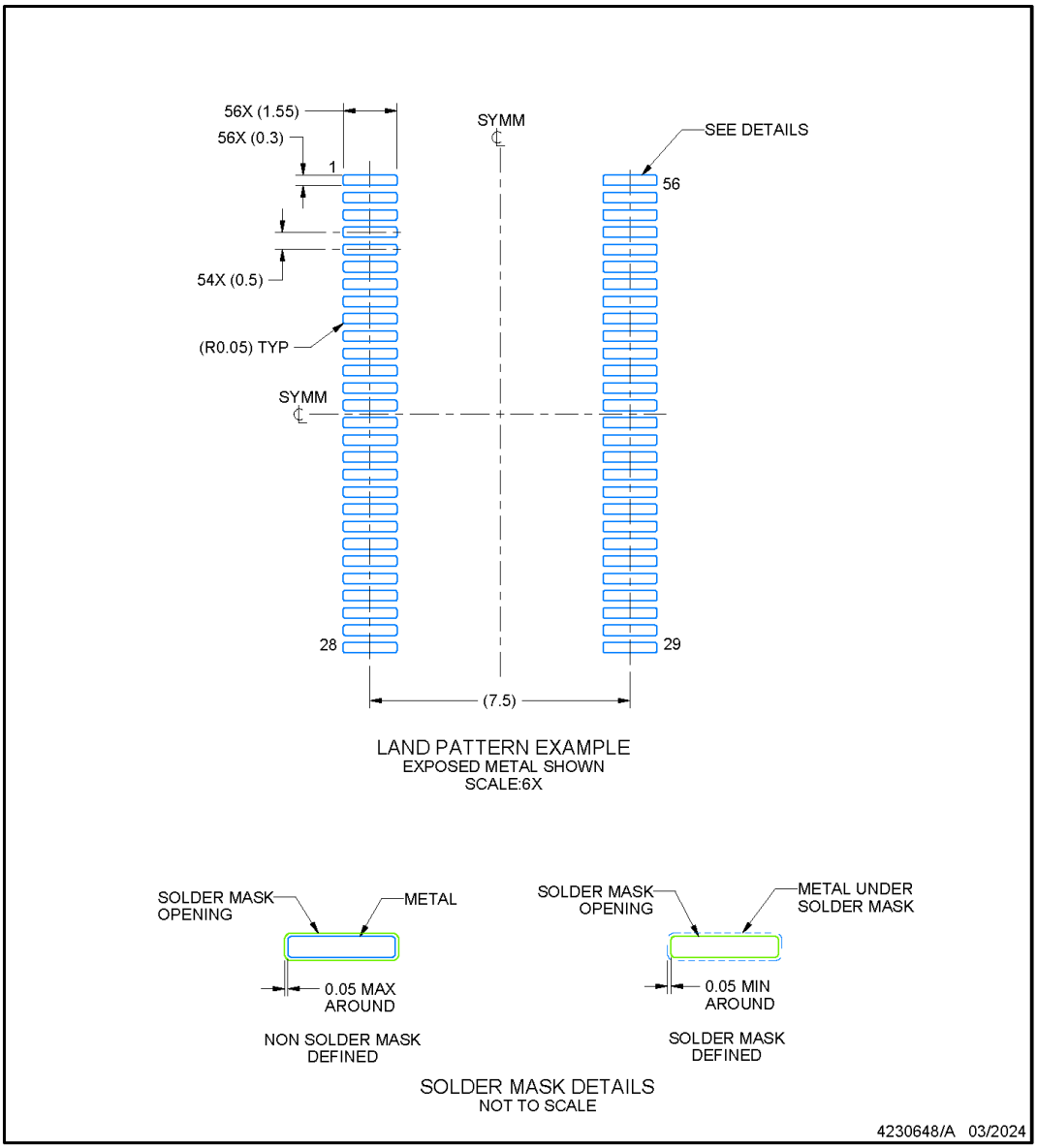
EXAMPLE BOARD LAYOUT

DFD0056D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

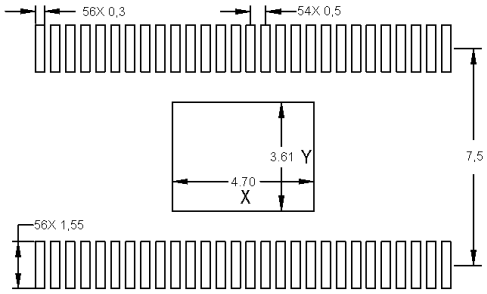
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCA0056F — **HTSSOP - 1.2 mm max height**

PowerPAD™ HTSSOP

Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

4218813/A 06/2015

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC69639QDCARQ1	Active	Production	HTSSOP (DCA) | 56	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC69639Q1
TLC69639QRTQRQ1	Active	Production	QFN (RTQ) | 56	3500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	69639Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

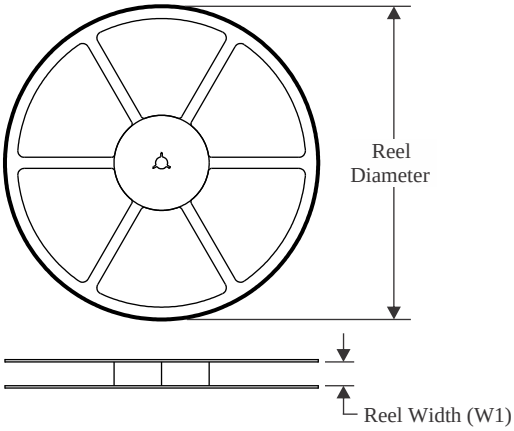
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

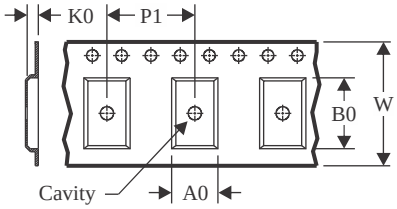
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

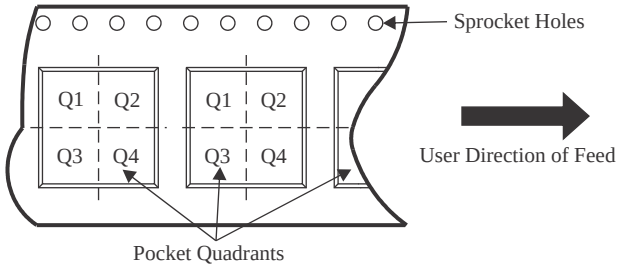


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

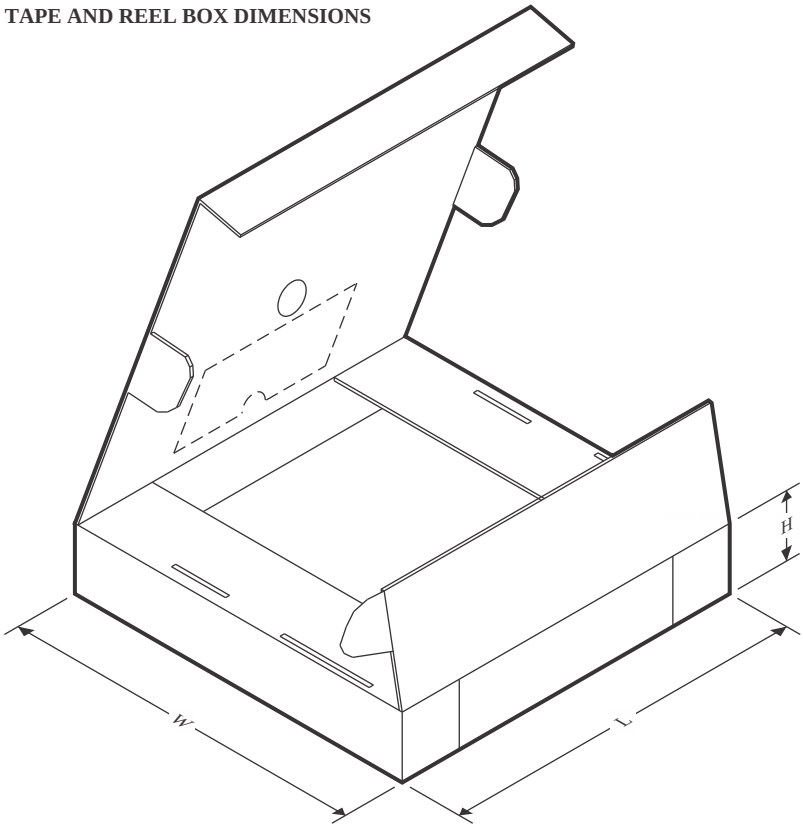
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

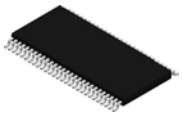
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC69639QDCARQ1	HTSSOP	DCA	56	2500	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
TLC69639QRTQRQ1	QFN	RTQ	56	3500	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC69639QDCARQ1	HTSSOP	DCA	56	2500	356.0	356.0	45.0
TLC69639QRTQRQ1	QFN	RTQ	56	3500	360.0	360.0	36.0

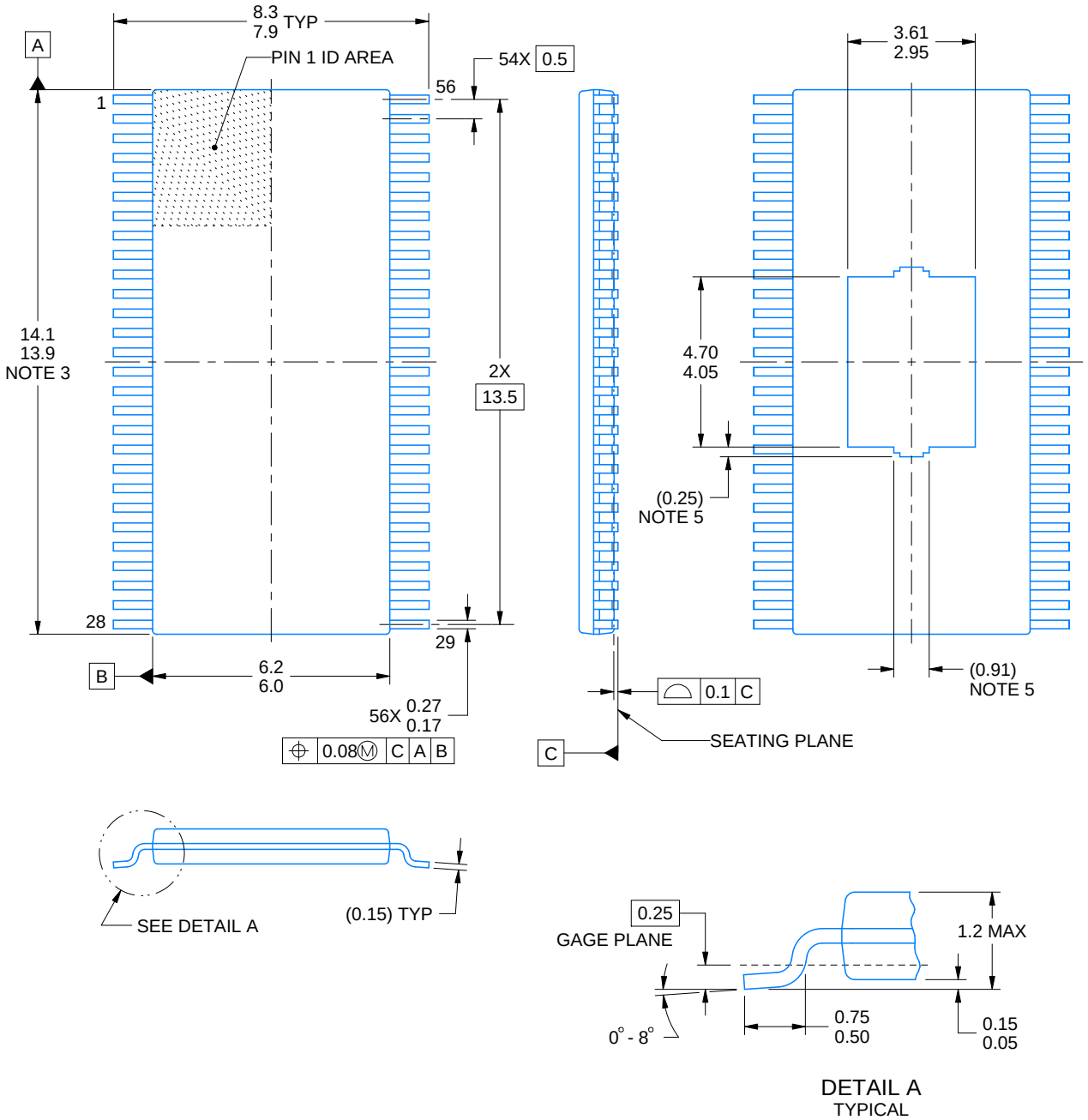


PACKAGE OUTLINE

DCA0056F

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

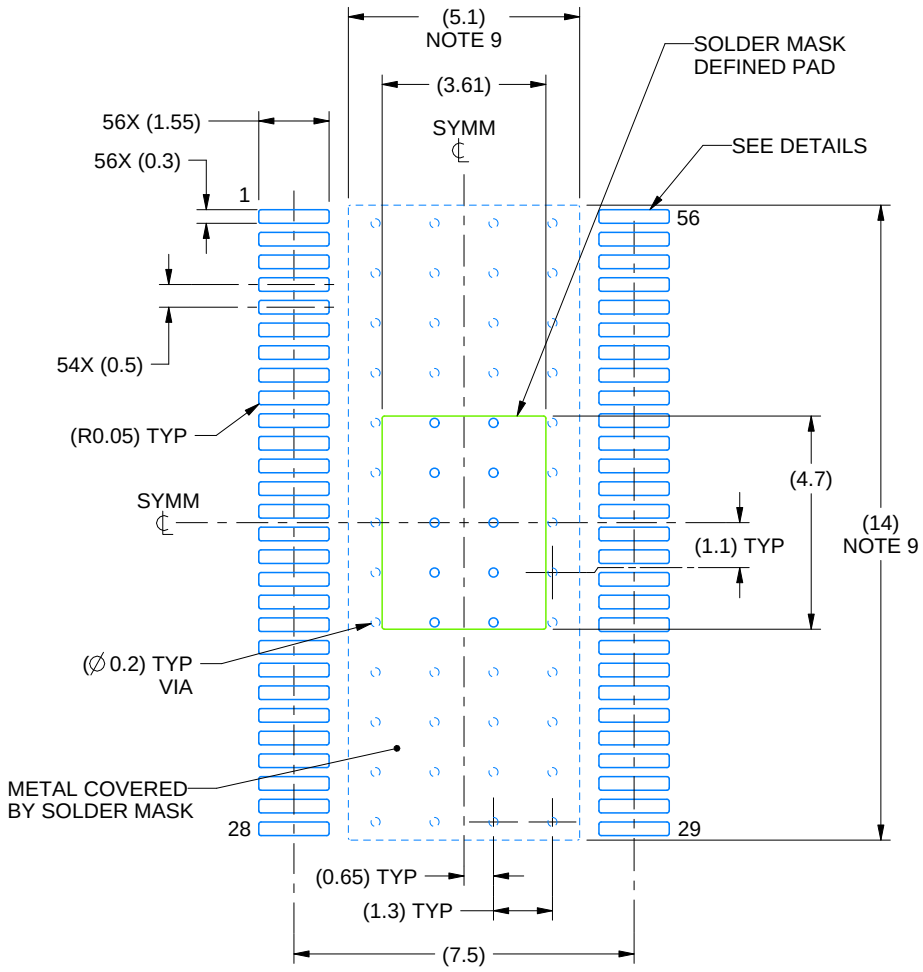


4218813/A 12/2024

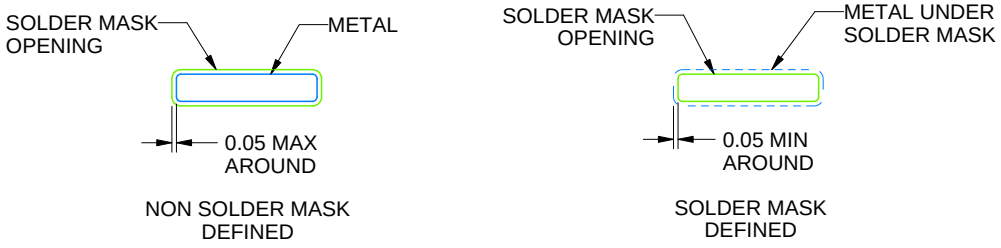
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not present.



LAND PATTERN EXAMPLE
SCALE:6X

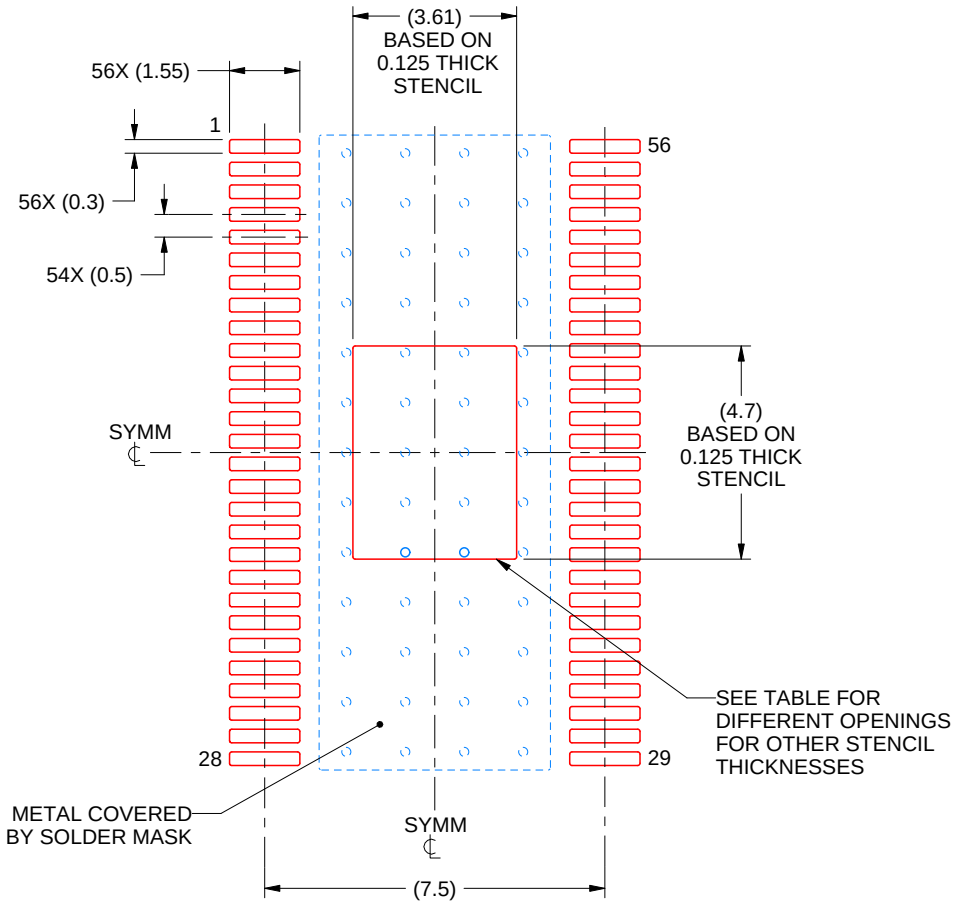


SOLDER MASK DETAILS
NOT TO SCALE

4218813/A 12/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

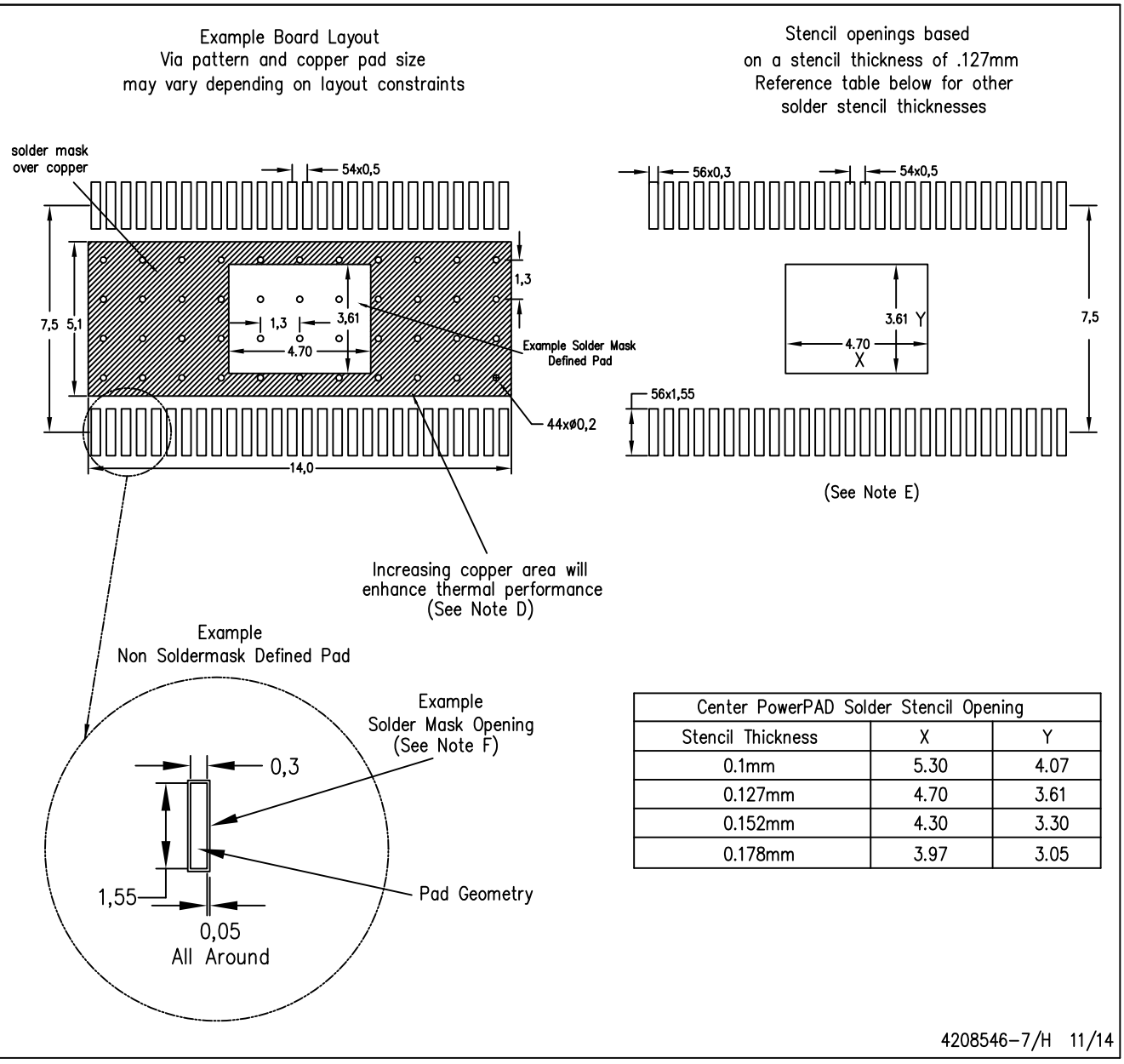
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.04 X 5.25
0.125	3.61 X 4.70 (SHOWN)
0.15	3.30 X 4.29
0.175	3.95 X 3.97

4218813/A 12/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

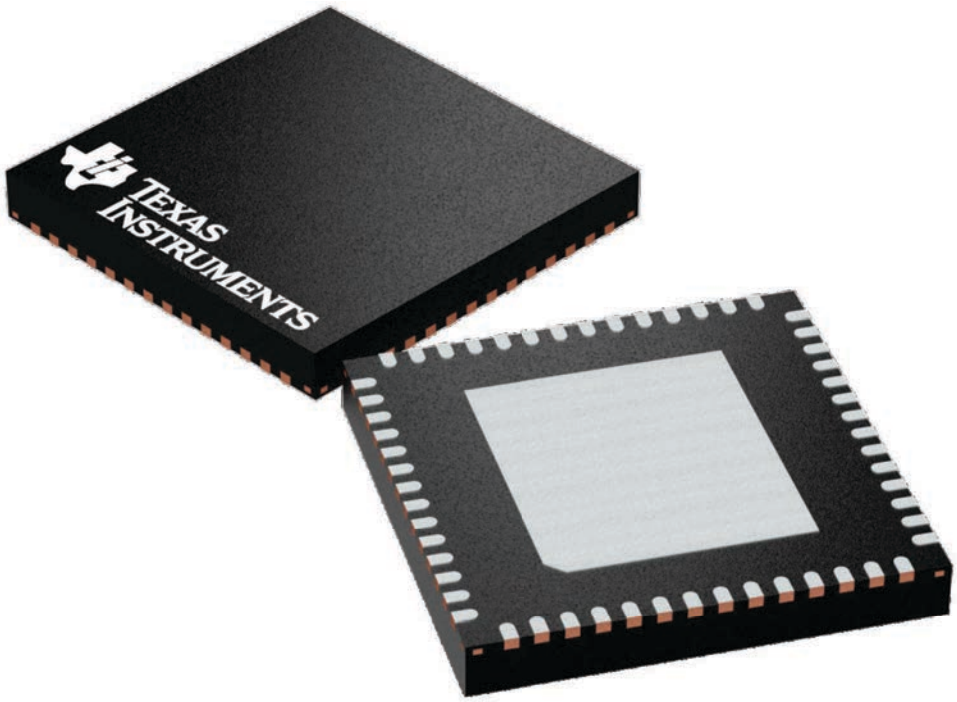
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

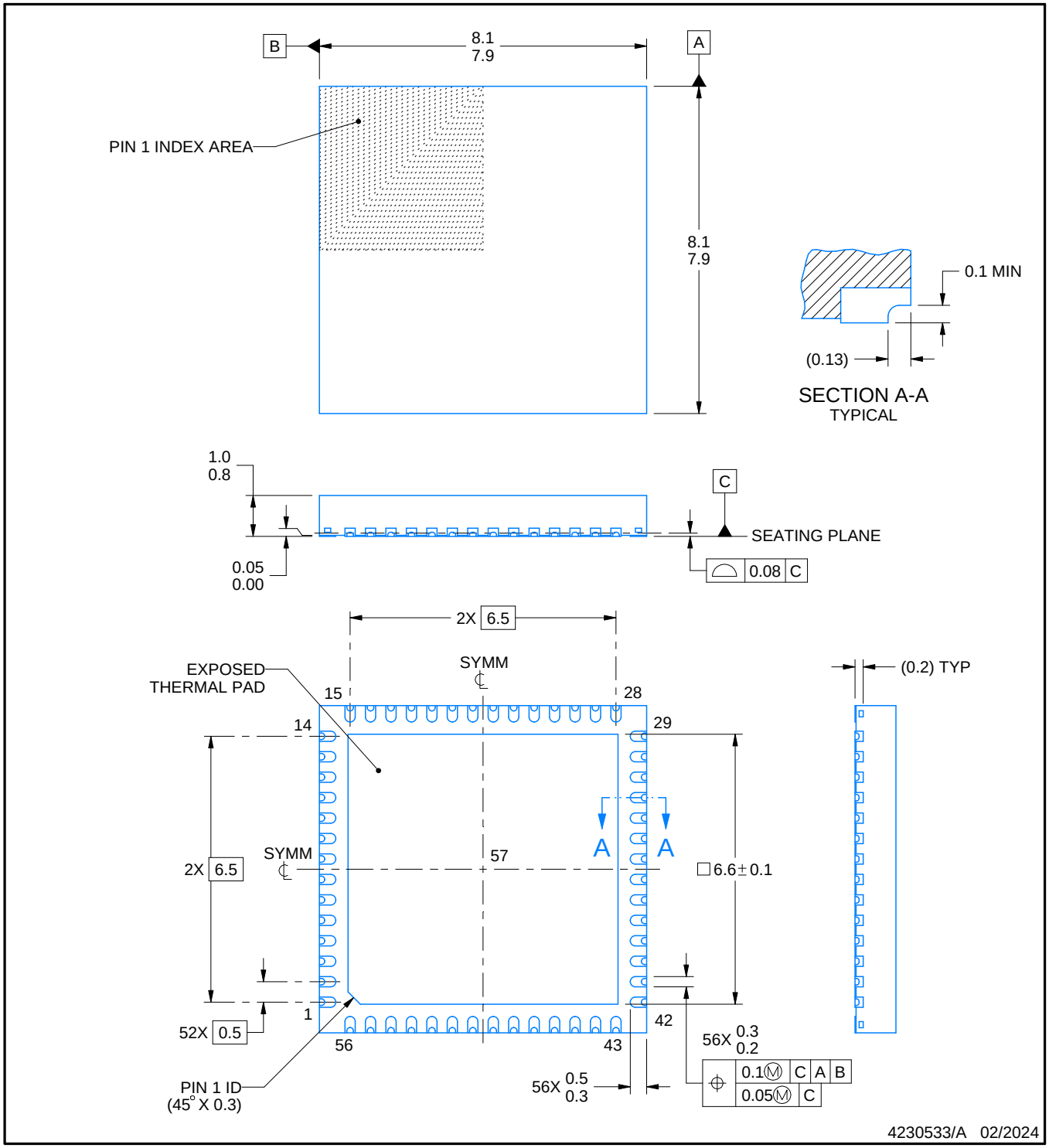
4224653/A

PACKAGE OUTLINE

RTQ0056K

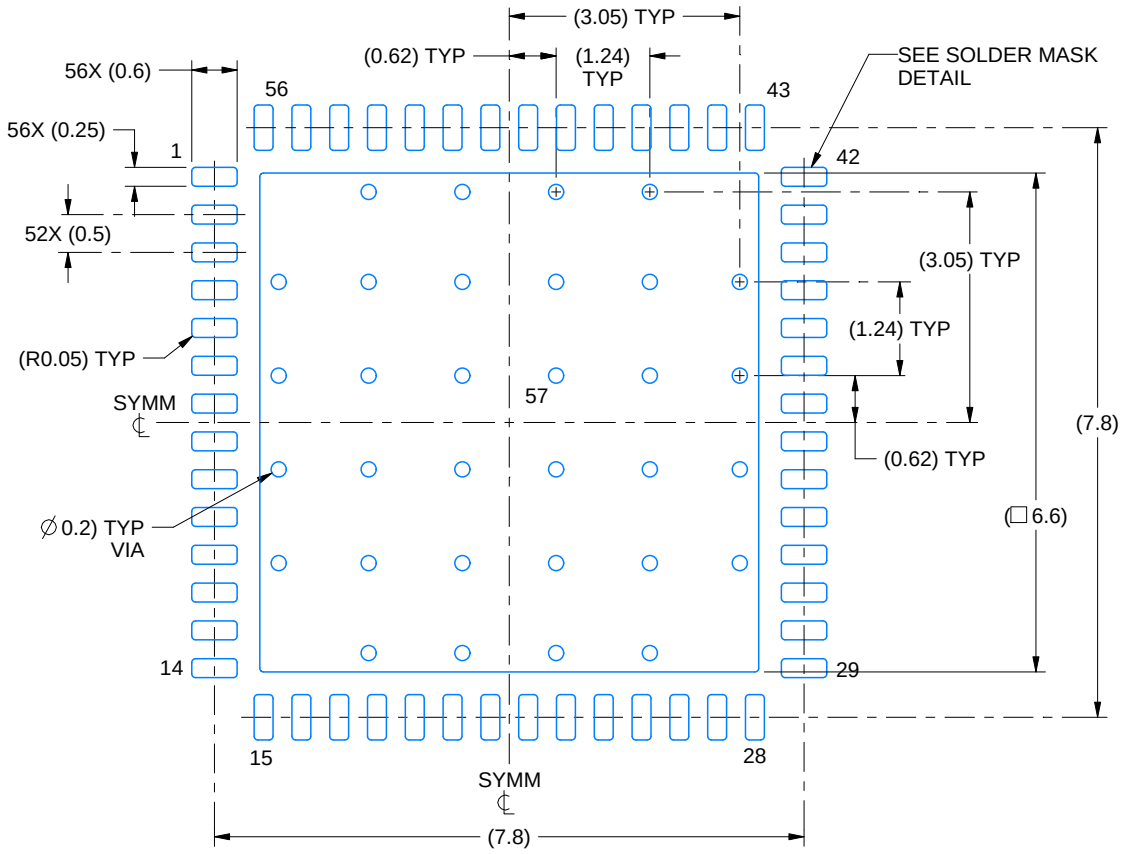
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

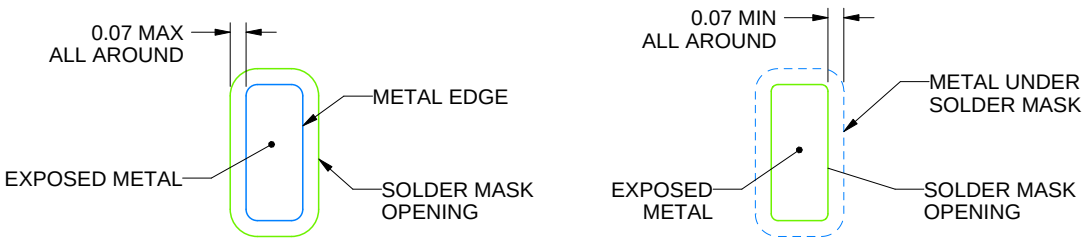


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

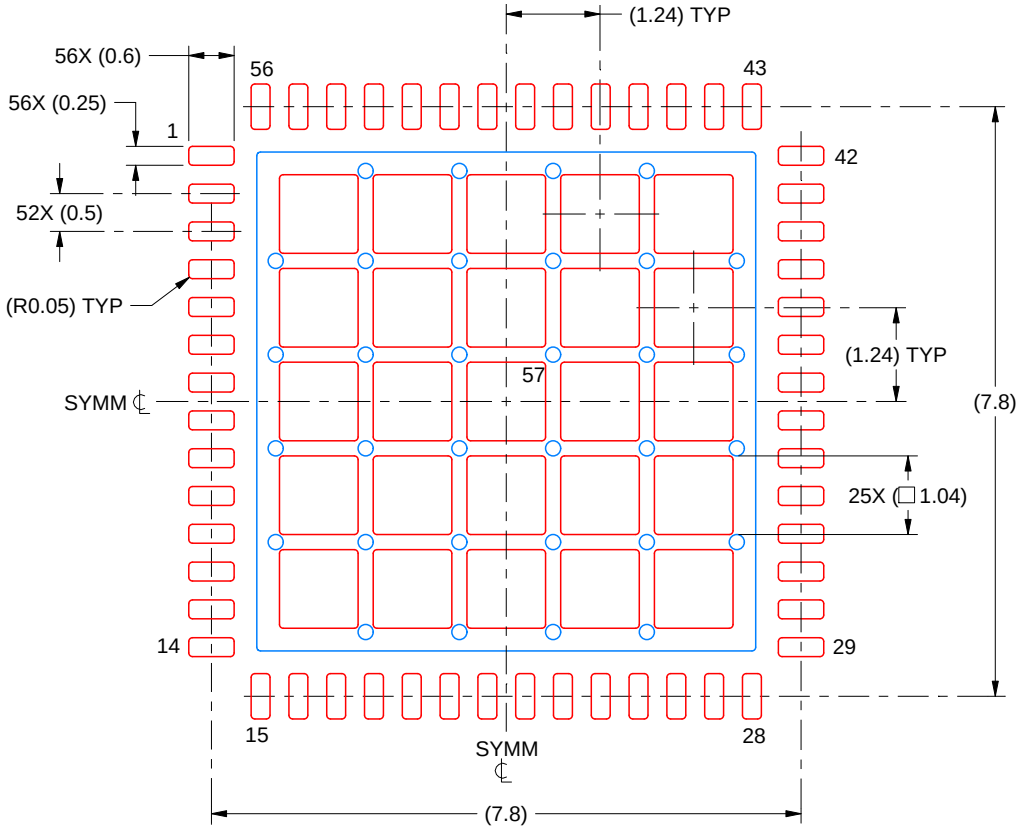


SOLDER MASK DETAILS

4230533/A 02/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230533/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月