参考文献

TLC69699-Q1 适用于 TLC696xx-Q1 器件系列的汽车级 SPI 兼容型连接

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 1 级：–40°C 至 +125°C 环境温度
  - 器件 HBM 分类等级 H3A
  - 器件 CDM 分类等级 C5
- 功能安全型：
  - 可提供用于功能安全系统设计的文档
- 工作电压 V_{CC} 范围：2.5V 至 5.5V
- SPI 外设
  - 数据传输速率高达 20MHz
  - 支持多个外设和一个控制器
- 连续时钟串行接口 (CCSI) 控制器和外设
  - 数据传输速率高达 20MHz
  - 用于增强 EMI 性能的可编程时钟抖动
- 诊断
  - 开漏 FAULT 引脚
  - SPI 通信丢失检测
  - 用于 SPI 通信的 CRC
  - 连续时钟看门狗
  - CCSI 数据完整性
- 数据就绪中断指示数据可用性

2 应用

- TLC696x0/1/2/4/8-Q1 SPI 兼容型连接

3 说明

TLC69699-Q1 SPI 兼容型连接支持使用标准 SPI 控制器控制 TLC696xx-Q1 器件系列。该器件具有一个内部振荡器，用于生成 TLC696xx-Q1 器件系列所需的连续时钟。可以将抖动添加到连续时钟以增强 EMI 性能。传输的数据与连续时钟对齐，以保持 CCSI 接口的时序要求。

TLC69699-Q1 整合了 TLC696xx-Q1 菊花链和 TLC69699-Q1 内部的故障报告。向 TLC696xx-Q1 菊花链传输的寄存器和亮度数据受 TLC69699-Q1 的 CRC 保护。此外，数据线和连续时钟线均由 TLC69699-Q1 提供卡滞故障保护。

封装信息

器件型号	封装[1]	封装尺寸[2]
TLC69699-Q1	SOT-23-THN (14)	4.20mm x 2.00mm
	WSON (12) 可湿性侧面	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值。

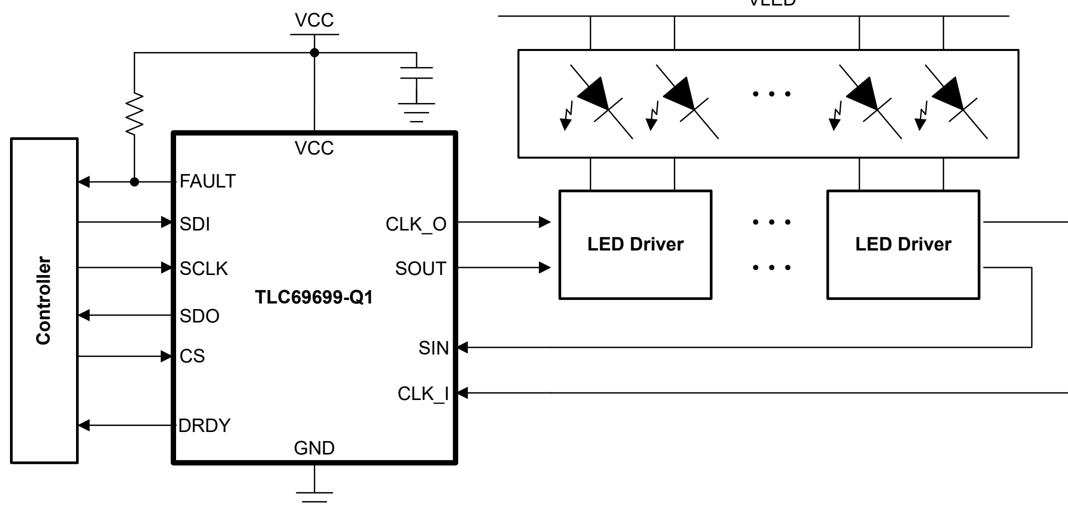


图 3-1. 典型应用图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

内容

1 特性 1
2 应用 1
3 说明 1
4 器件比较 3
5 引脚配置和功能 3
6 器件和文档支持 4
6.1 器件支持 4
6.2 文档支持 4
6.3 接收文档更新通知 4
6.4 支持资源 4
6.5 商标 4
6.6 静电放电警告 4
6.7 术语表 4
7 修订历史记录 4
8 机械、封装和可订购信息 4
8.1 卷带包装信息 5
8.2 机械数据 7

Copyright © 2024 Texas Instruments Incorporated

4 器件比较

表 **4-1.** 器件比较

器件型号	材料	封装
TLC69699-Q1	TLC69699QDYYRQ1	SOT-23-THN (14)
	TLC69699QDRRRQ1	WSON (12)

5 引脚配置和功能

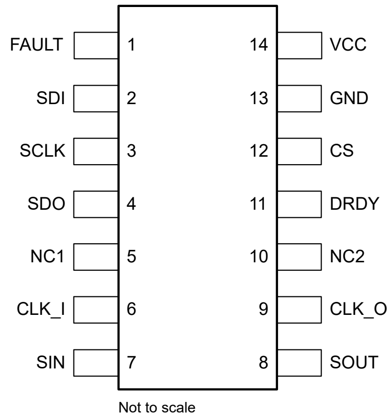


图 **5-1. TLC69699-Q1 DYY** 封装 **14** 引脚 **SOT-23-THN** 顶视图

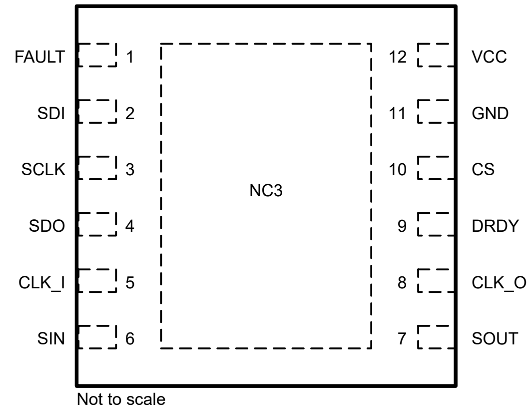


图 **5-2. TLC69699-Q1 DRR** 封装 **12** 引脚 **WSON**（带有外露散热焊盘）顶视图

表 **5-1.** 引脚功能

引脚			类型(1)	说明
名称	DYY 编号	DRR 编号		
FAULT	1	1	O	故障指示引脚
SDI	2	2	I	SPI 串行数据输入
SCLK	3	3	I	SPI 串行时钟输入
SDO	4	4	O	SPI 串行数据输出
NC1	5	-	NC	无连接。可用于信号路由。
CLK_I	6	5	I	CCSI 连续时钟输入
SIN	7	6	I	CCSI 串行数据输入
SOUT	8	7	O	CCSI 串行数据输出
CLK_O	9	8	O	CCSI 串行时钟输出
NC2	10	-	NC	无连接。可用于信号路由。
DRDY	11	9	O	数据就绪中断。
CS	12	10	I	SPI 片选
GND	13	11	G	接地引脚（必须接地）
VCC	14	12	P	VCC 电源输入
NC3	-	外露焊盘	NC	无连接。需要与除接地以外的任何信号进行电气隔离。

(1) I = 输入，O = 输出，G = 接地，P = 电源，NC = 无连接。

6 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

6.1 器件支持

6.2 文档支持

6.2.1 相关文档

6.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

6.5 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

6.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

7 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

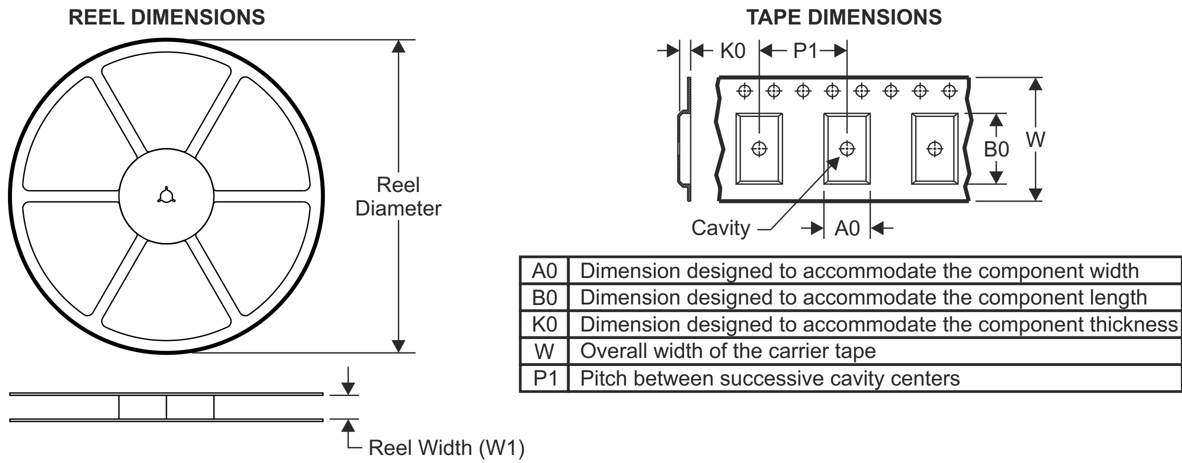
日期	修订版本	注释
2024 年 10 月	*	初始发行版

8 机械、封装和可订购信息

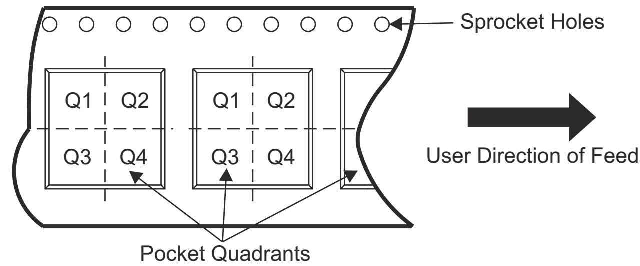
以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

Copyright © 2024 Texas Instruments Incorporated

8.1 卷带包装信息



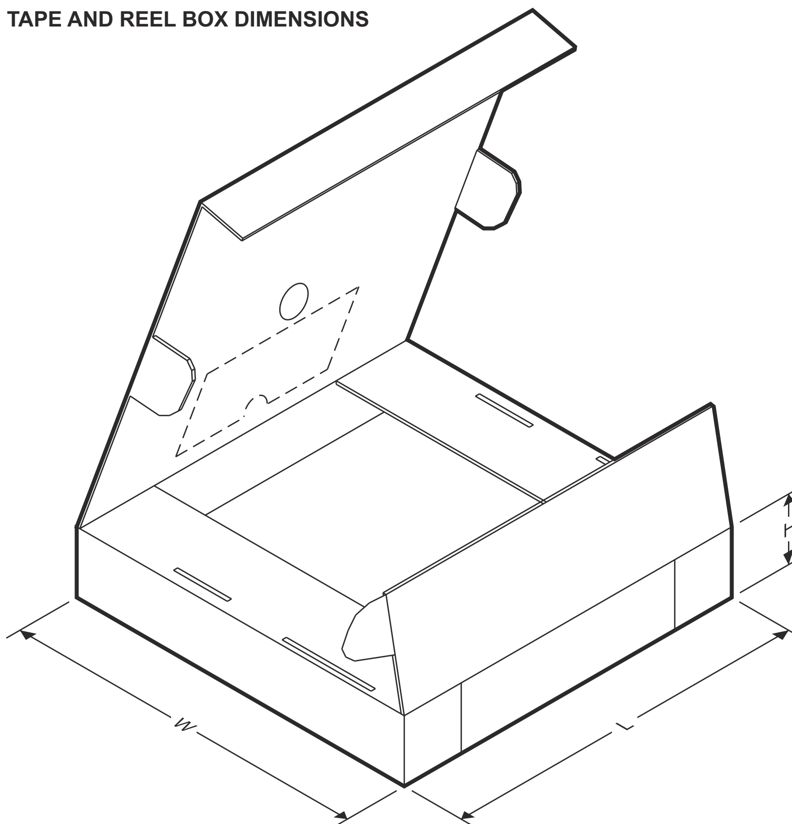
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



器件	封装类型	封装图	引脚	SPQ	卷带直径 (mm)	卷带宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限
TLC69699QDYYRQ1	SOT-23-THN	DYY	14									
TLC69699QDRRRQ1	WSON	DRR	12									

Copyright © 2024 Texas Instruments Incorporated

TAPE AND REEL BOX DIMENSIONS



器件	封装类型	封装图	引脚	SPQ	长度 (mm)	宽度 (mm)	高度 (mm)
TLC69699QDYYRQ1	SOT-23-THN	DYY	14				
TLC69699QDRRRQ1	WSON	DRR	12				

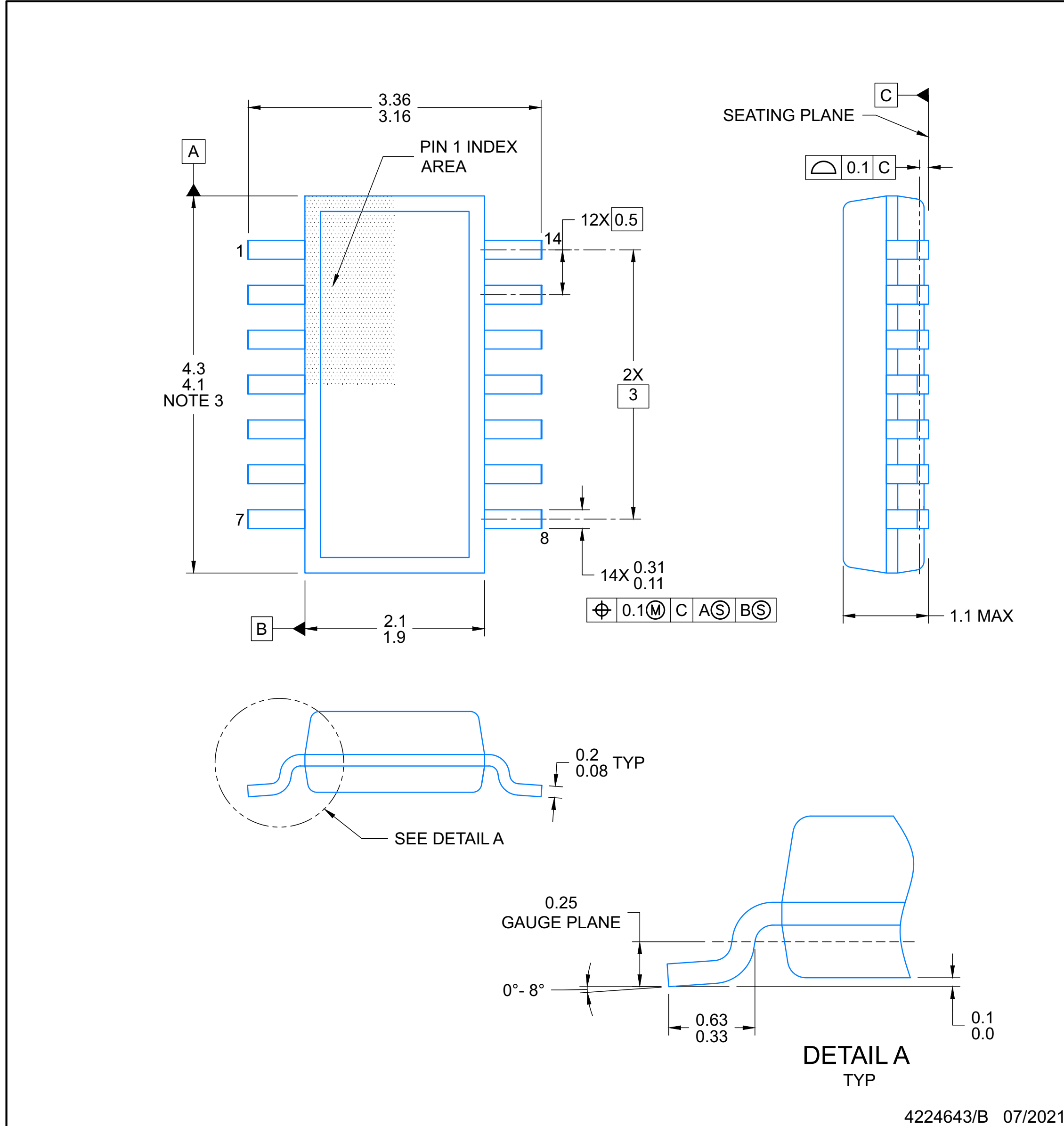
Copyright © 2024 Texas Instruments Incorporated

8.2 机械数据

PACKAGE OUTLINE

DYY0014A **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES:

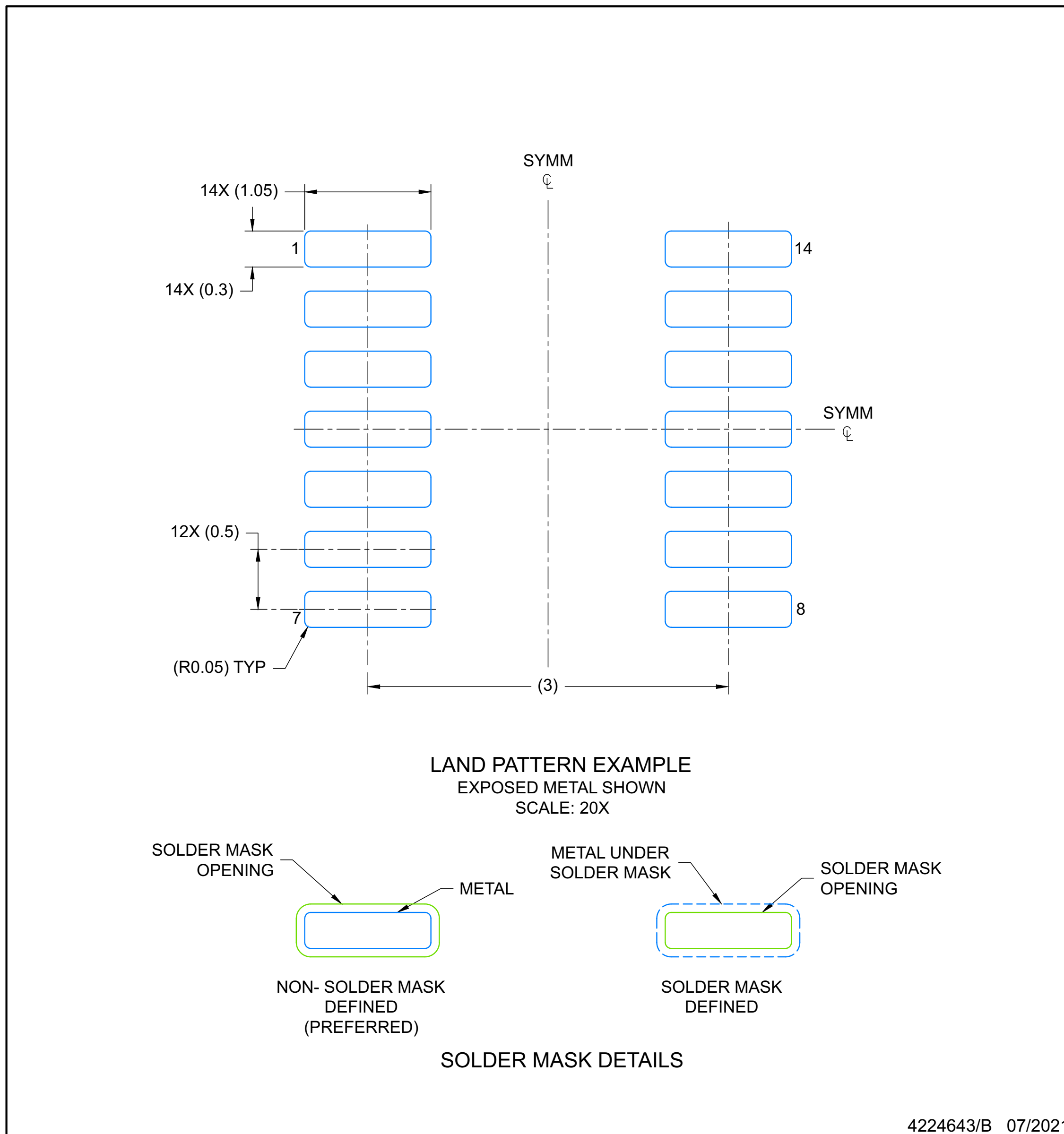
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

Copyright © 2024 Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

DYY0014A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4224643/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS INSTRUMENTS
www.ti.com

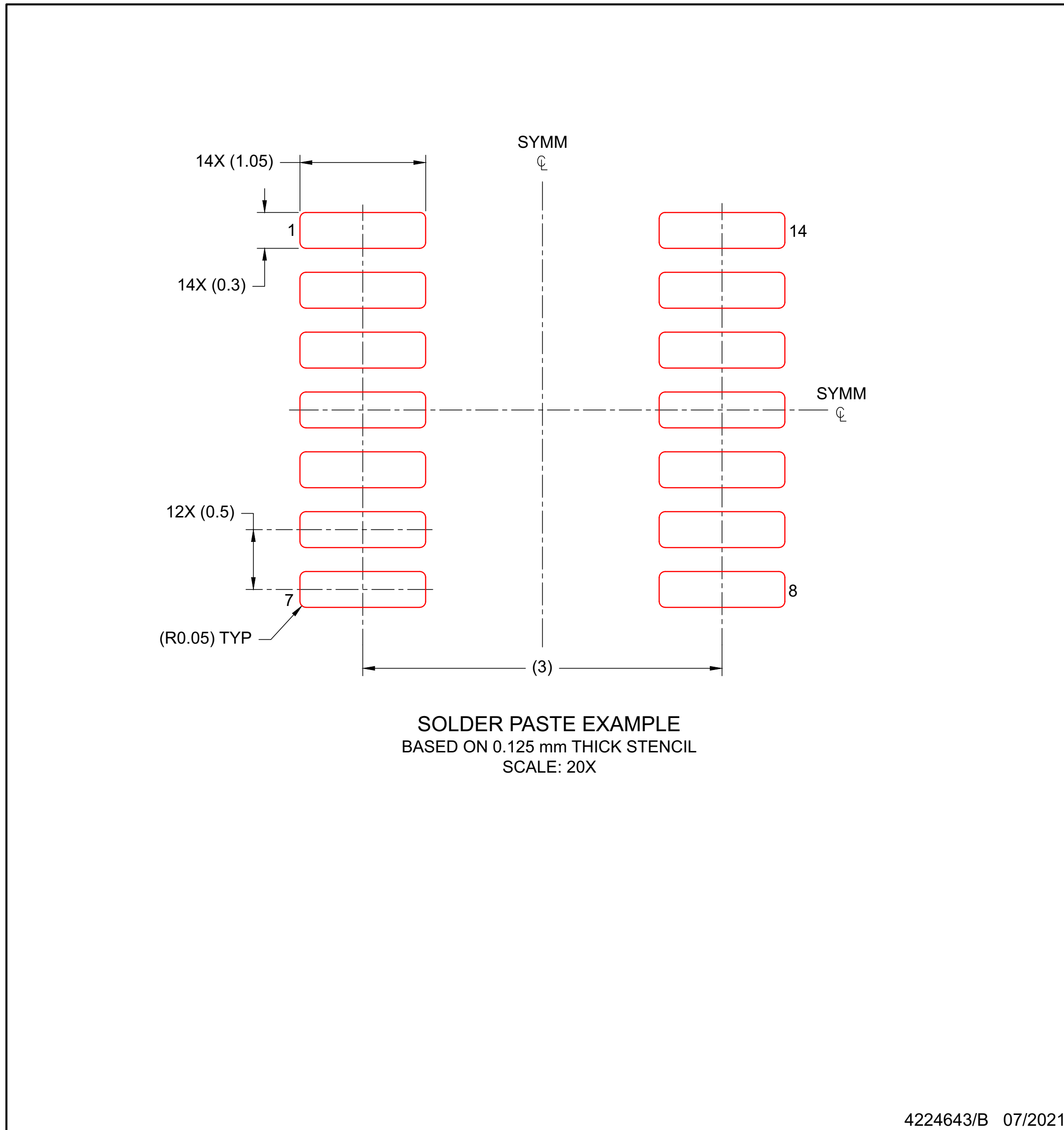
Copyright © 2024 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

DYY0014A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Texas Instruments
www.ti.com

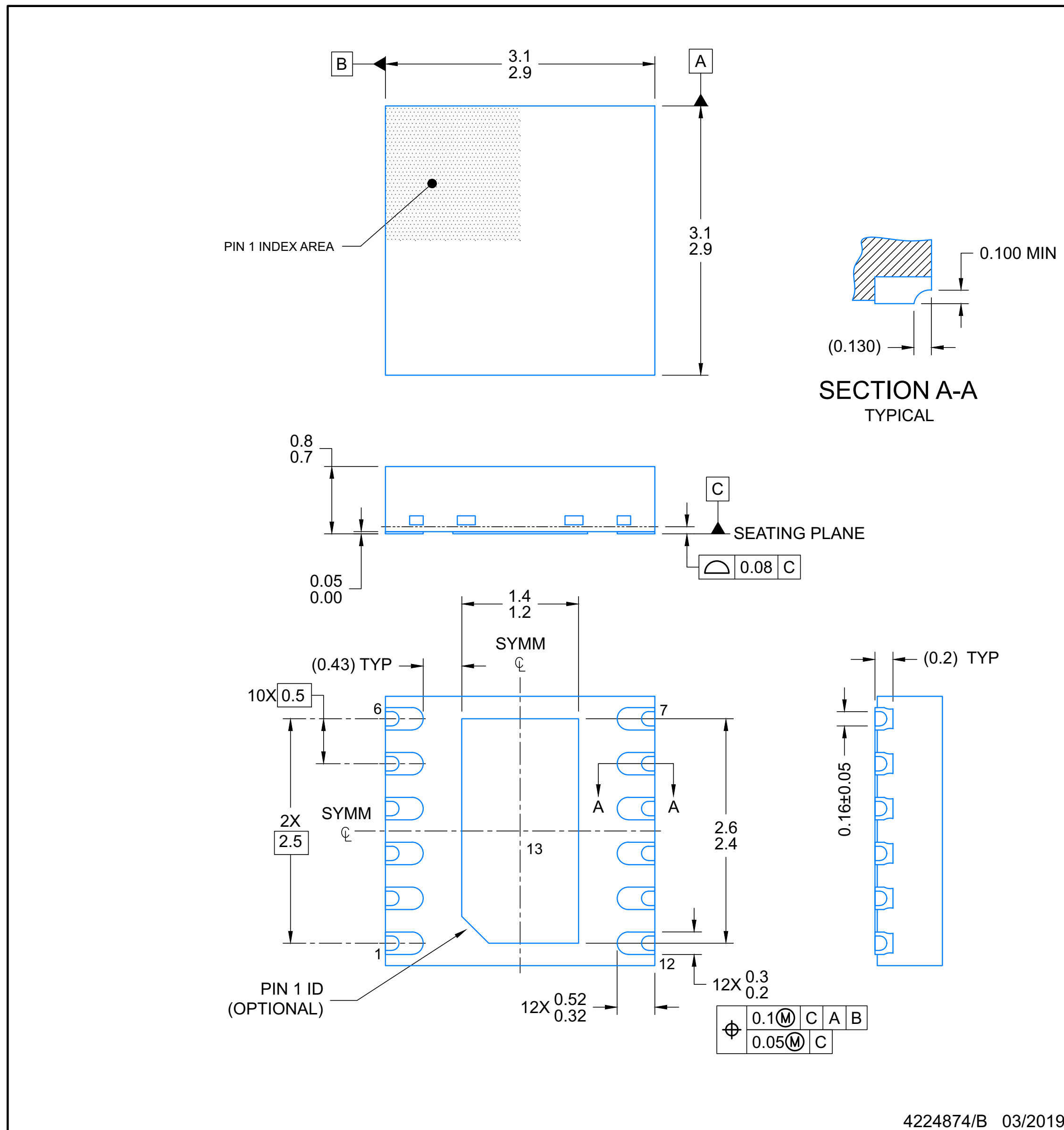
Copyright © 2024 Texas Instruments Incorporated

PACKAGE OUTLINE

DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

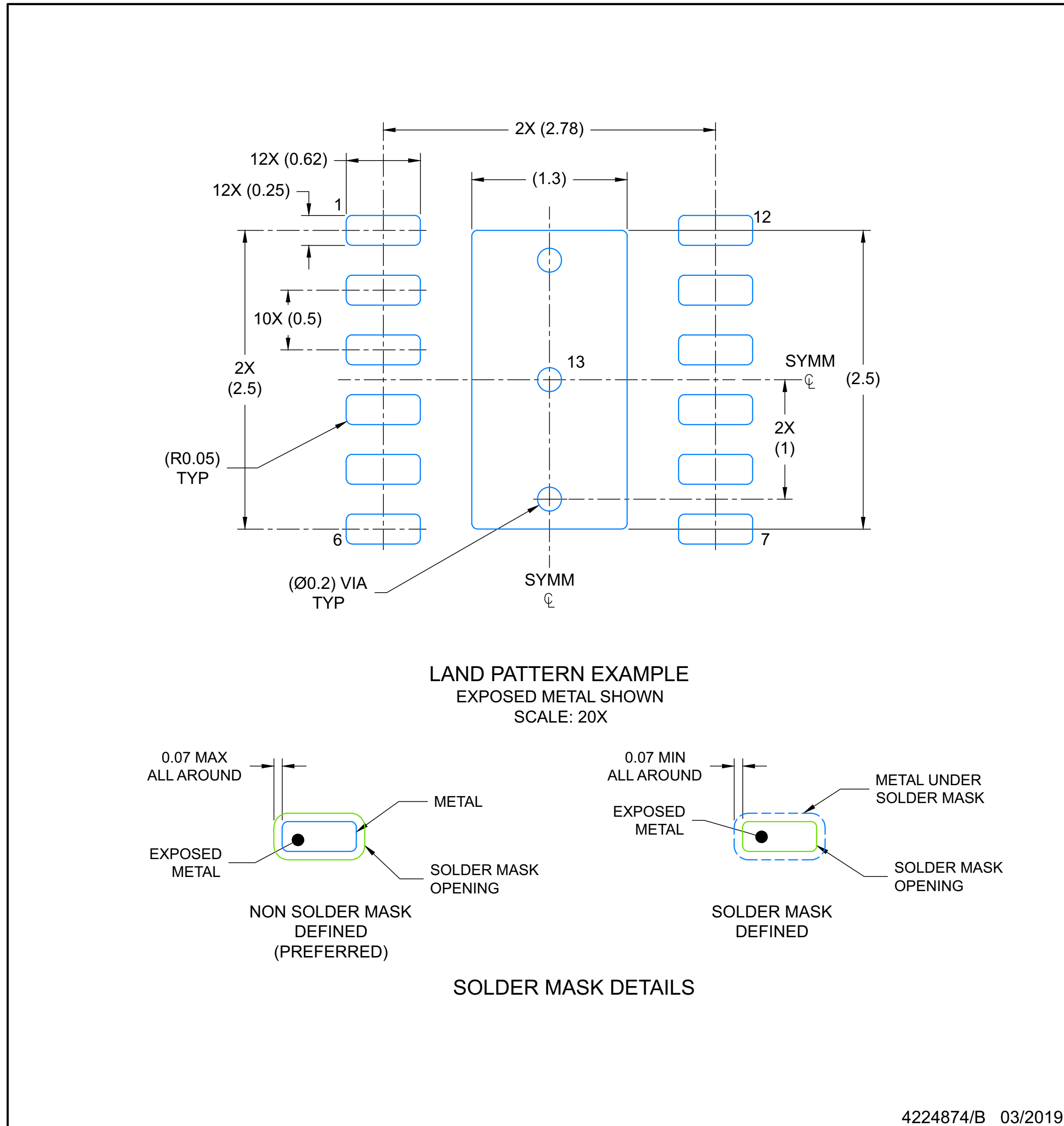
Copyright © 2024 Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

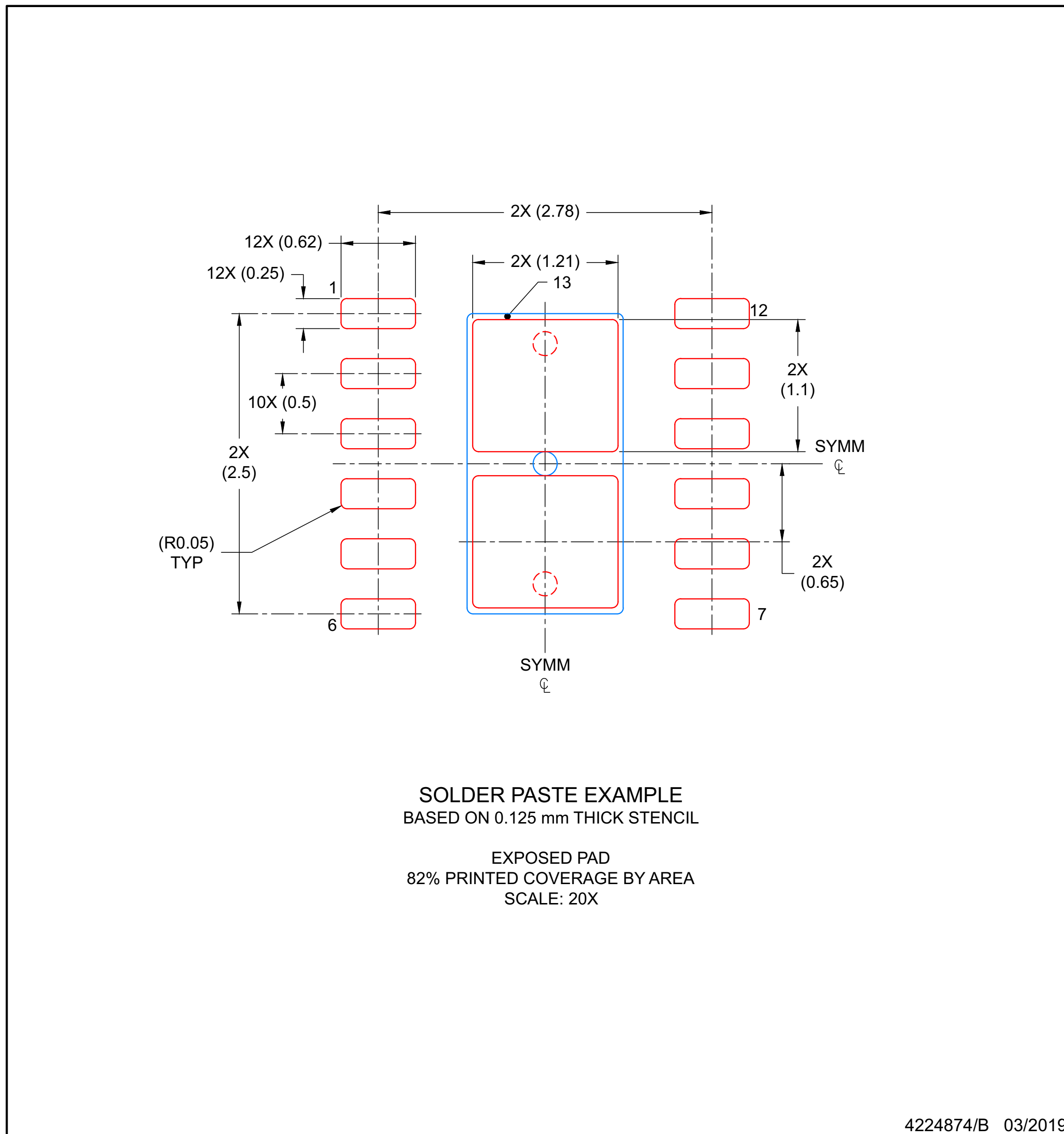
Copyright © 2024 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

4224874/B 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC69699QDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9699NQ	Samples
TLC69699QDYYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	69699TQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

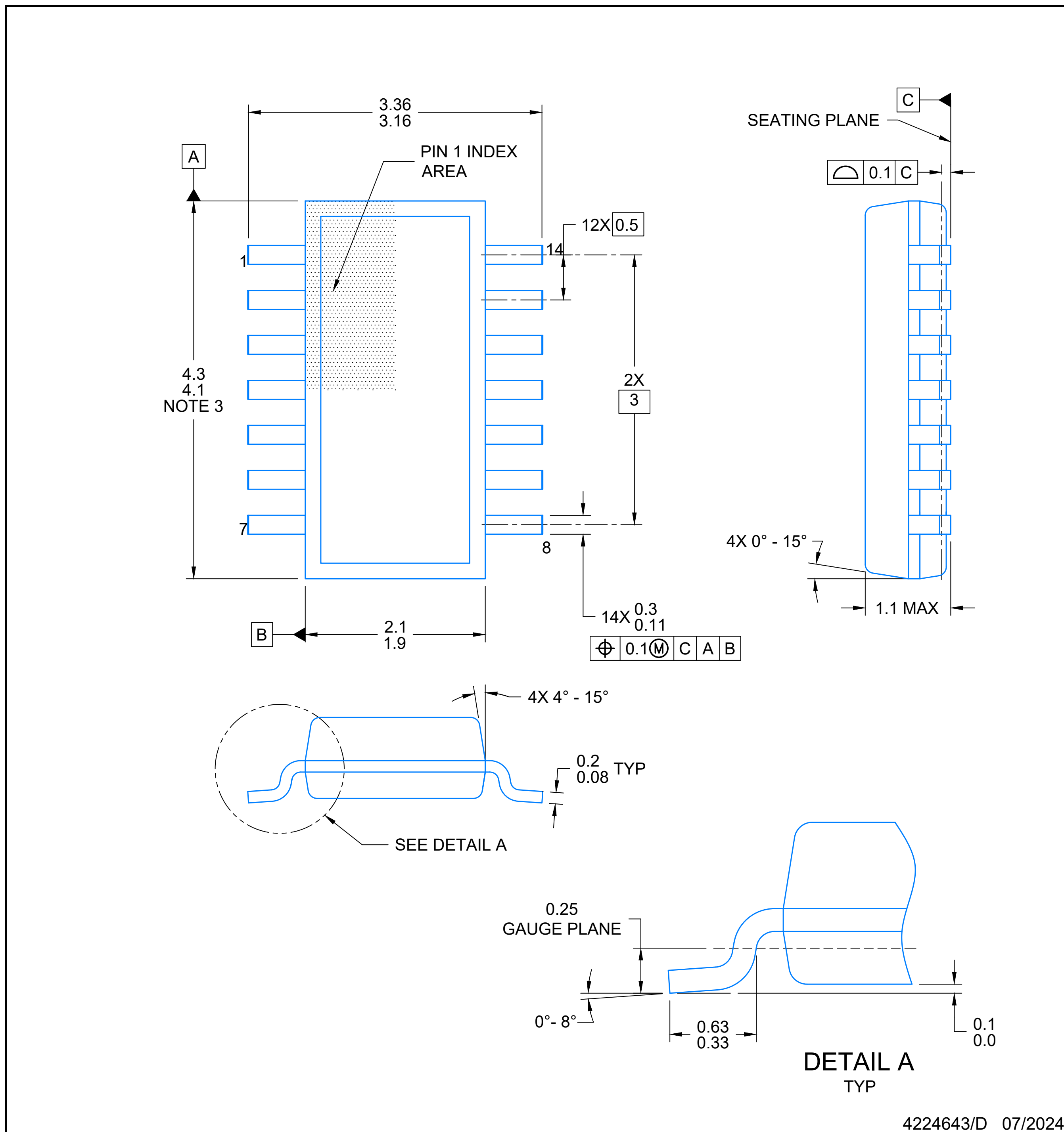
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

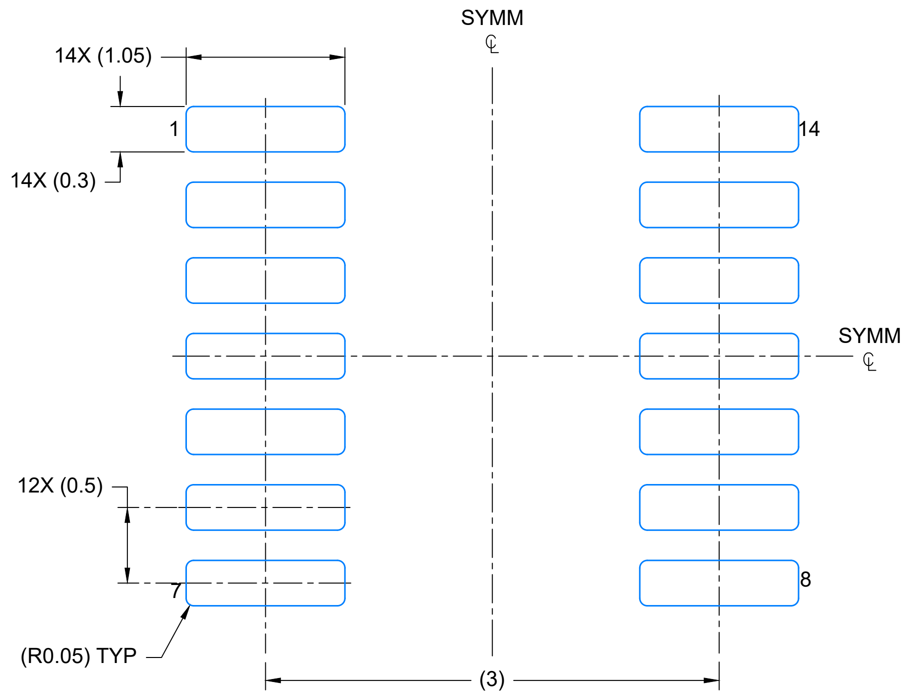
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

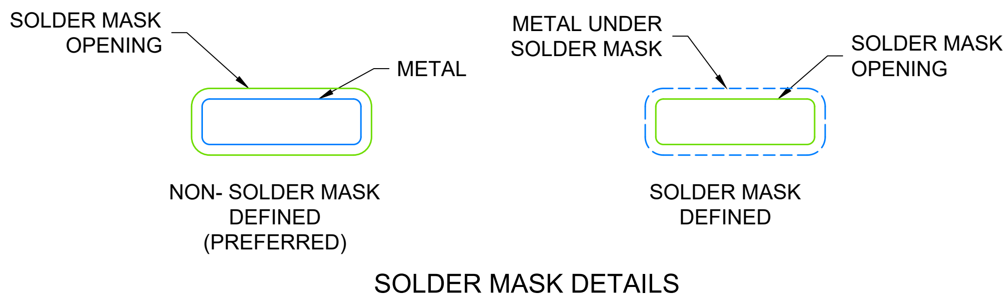


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

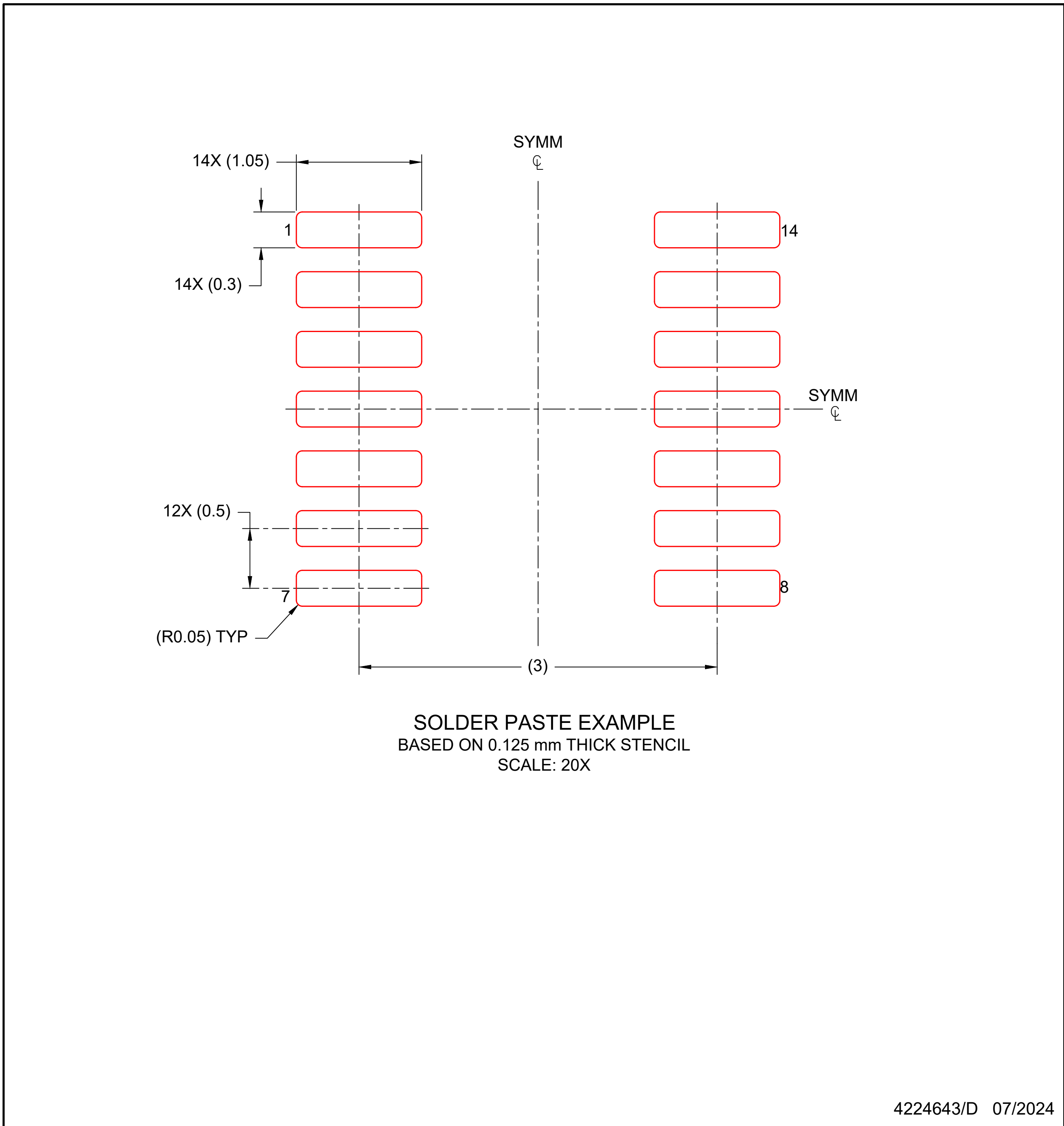


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

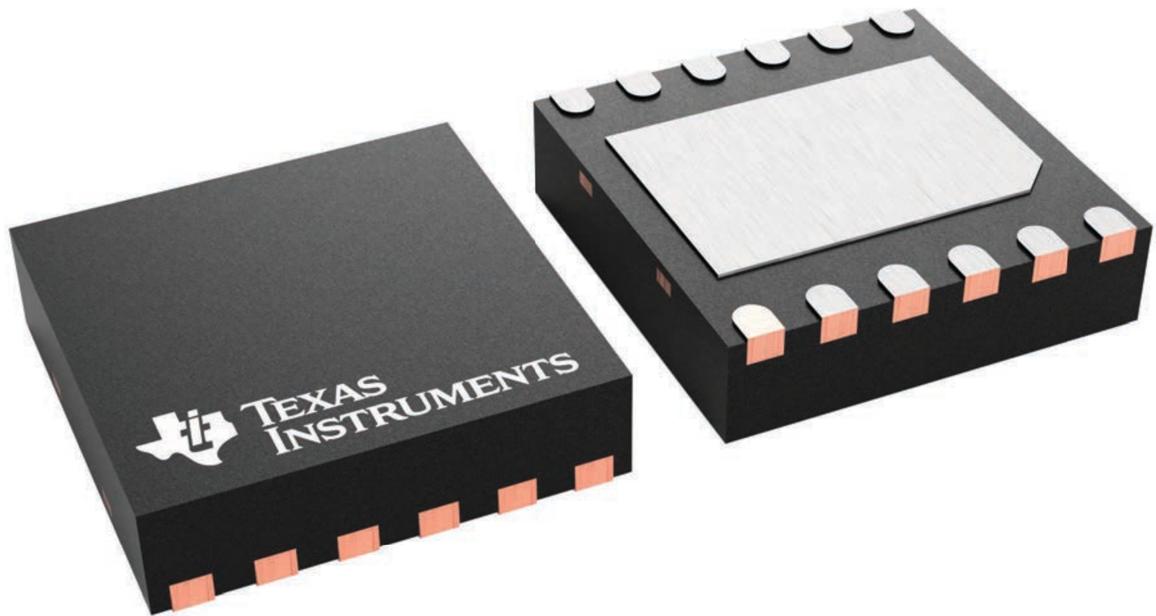
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

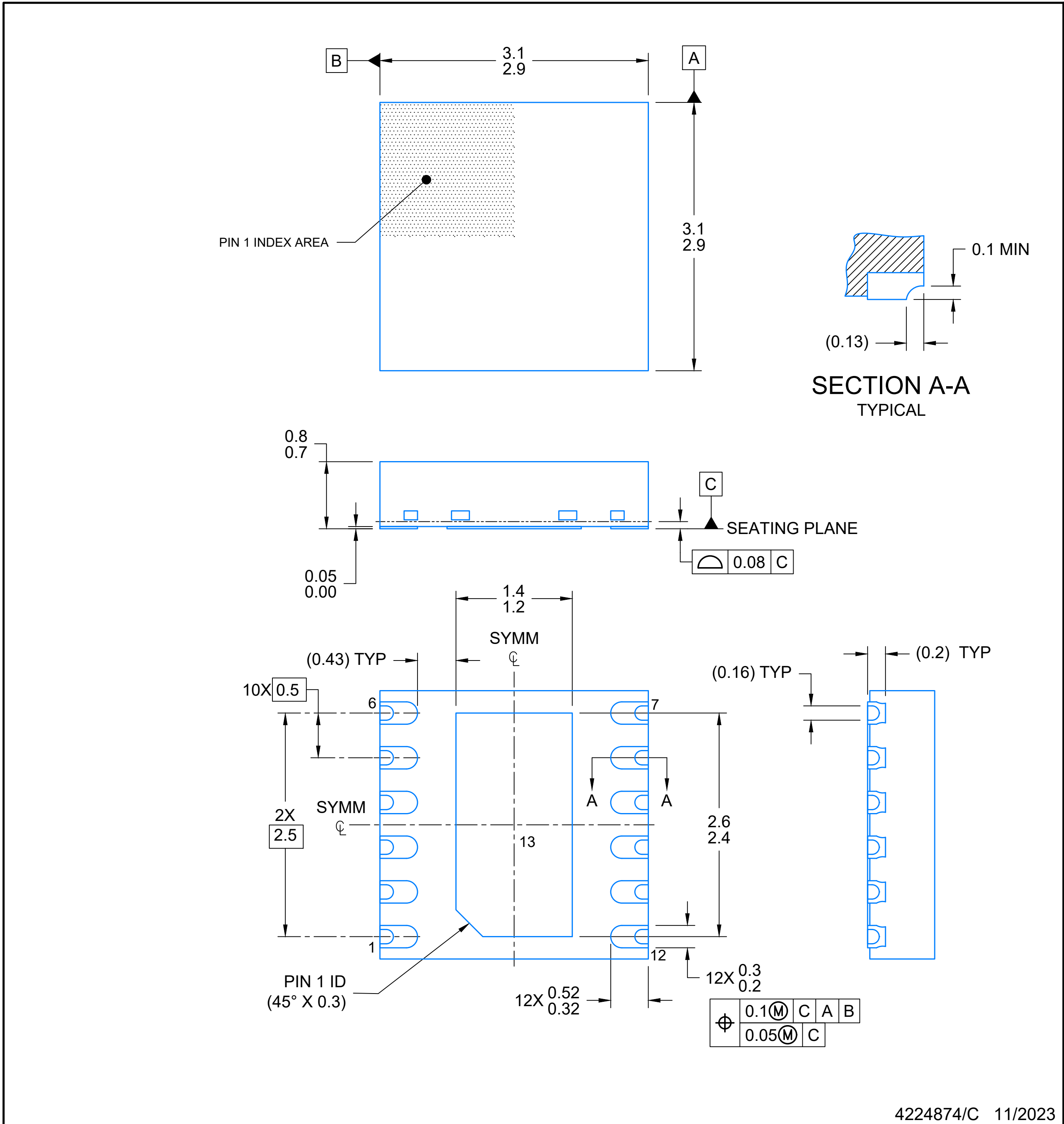


NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

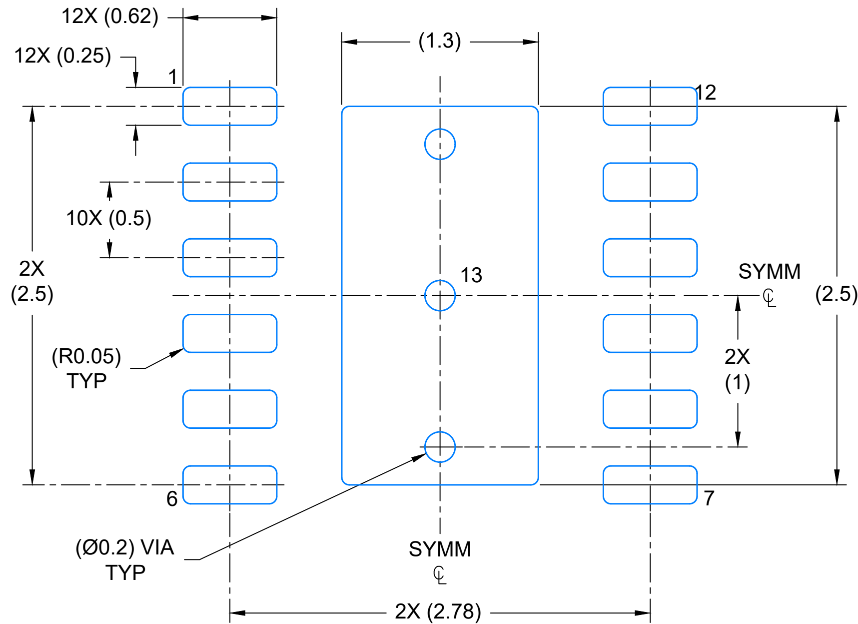
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



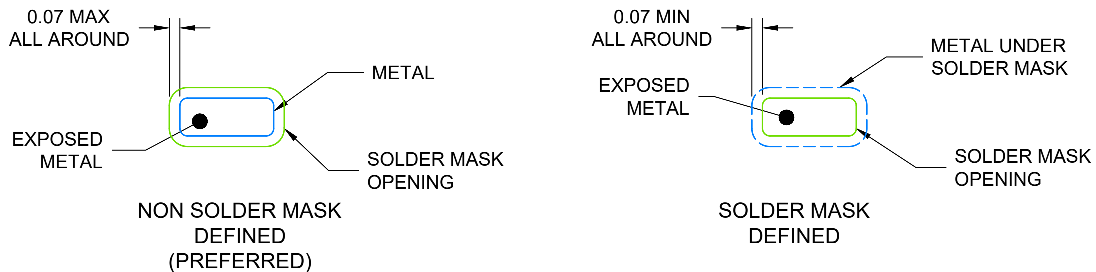


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

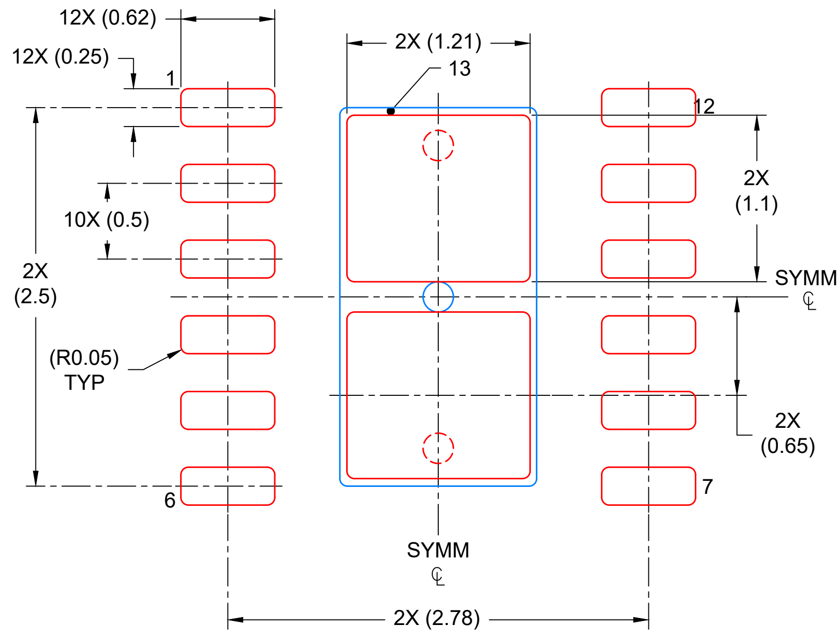


SOLDER MASK DETAILS

4224874/C 11/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

4224874/C 11/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024，德州仪器 (TI) 公司