TLV1704-SEP 采用增强型航天塑料的 2.2V 至 36V 耐辐射微功耗四路比较器

1 特性

- VID V62/18613
- 耐辐射
  - 单粒子闩锁 (SEL) 在 125°C 下的抗扰度可达 43MeV-cm^2/mg
  - 在 30 krad(Si) 的条件下无 ELDRS
  - 每个晶圆批次的 RLAT 总电离剂量 (TID) 高达 20krad(Si)
- 增强型航天塑料
  - 受控基线
  - 金线
  - NiPdAu 铅涂层
  - 一个组装和测试基地
  - 一个制造基地
  - 支持军用（ –55°C 至 125°C ）温度范围
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性
  - 采用增强型模塑化合物实现低释气
- 电源电压范围：2.2V 至 36V 或 ±1.1V 至 ±18V
- 低静态电流：每个比较器 55µA
- 输入共模范围包括两个电源轨
- 低传播延迟：560ns
- 低输入失调电压：300µV
- 集电极开路输出：
  - 最多可高出负电源电压 36V 且不受电源电压影响
- 小型封装：
  - 四通道：TSSOP-14

2 应用

- 命令和数据处理 (C&DH)
- 飞行器驾驶舱显示屏
- 飞行控制单元
- 卫星电力系统 (EPS)

3 说明

TLV1704-SEP（四路）器件具有宽电源电压范围、轨到轨输入、低静态电流和低传播延迟。凭借符合行业标准且在极小型封装内集成的上述特性，此类器件成为当前市场中的最佳通用比较器。

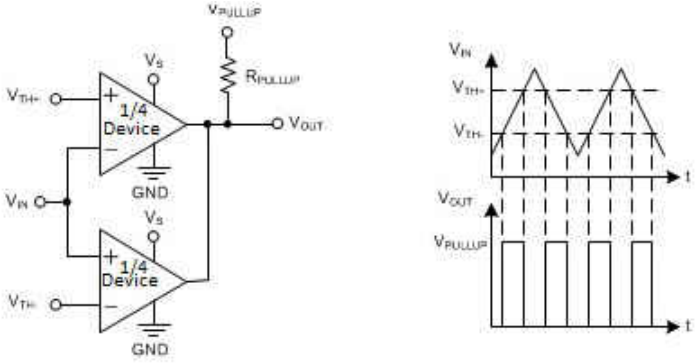
集电极开路输出带来了能够将输出拉至任意电压轨（最多可高出负电源 36V）且不受 TLV1704-SEP 电源电压影响的优势。

此器件是一款微功耗比较器。低输入失调电压、低输入偏置电流、低电源电流和集电极开路配置使 TLV1704-SEP 器件能够灵活处理从简单电压检测到驱动单个继电器的大部分应用。

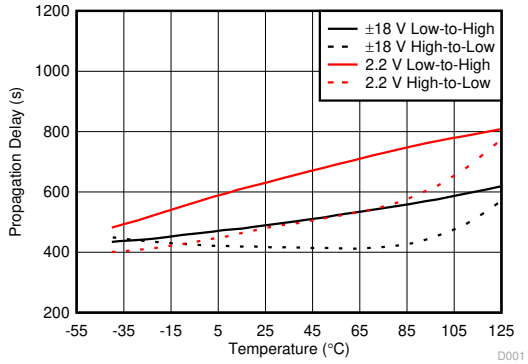
器件信息

器件型号	等级(1)	封装
TLV1704AMPWTPSEP	20krad(Si) RLAT	TSSOP (14)
TLV1704AMPWPSEP		

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



TLV1704-SEP 用作窗口比较器



稳定传播延迟与温度

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (November 2018) to Revision A (November 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将标题从“抗辐射”更新为“耐辐射”	1
• 使用链接更新了“应用”部分	1

5 Pin Configuration and Functions

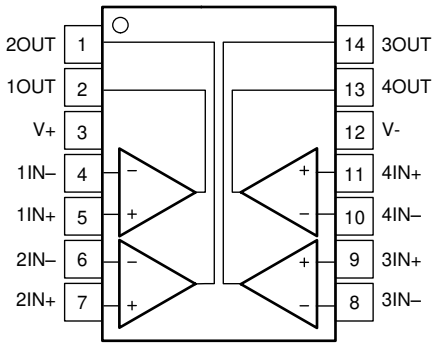


图 5-1. TLV1704-SEP PW Package 14-Pin TSSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	—	I	Noninverting input.
1IN+	5	I	Noninverting input, channel 1.
2IN+	7	I	Noninverting input, channel 2.
3IN+	9	I	Noninverting input, channel 3.
4IN+	11	I	Noninverting input, channel 4.
IN –	—	I	Inverting input.
1IN –	4	I	Inverting input, channel 1.
2IN –	6	I	Inverting input, channel 2.
3IN –	8	I	Inverting input, channel 3.
4IN –	10	I	Inverting input, channel 4.
OUT	—	O	Output.
1OUT	2	O	Output, channel 1.
2OUT	1	O	Output, channel 2.
3OUT	14	O	Output, channel 3.
4OUT	13	O	Output, channel 4.
V+	3	—	Positive (highest) power supply.
V –	12	—	Negative (lowest) power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			40 (±20)	V
Signal input pins	Voltage(2)	(V_S –) – 0.5	(V_S+) + 0.5	V
	Current(2)		±10	mA
Output short-circuit(3)		Continuous		mA
Operating Junction temperature, T_J		–55	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground; one comparator per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_S = (V_S+) – (V_S –)	2.2 (±1.1)		36 (±18)	V
Specified temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV1704-SEP PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = –55°C to 125°C, V_S = 2.2 V to 36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C, V_S = 2.2 V		±0.5	±3.5	mV
		T_A = 25°C, V_S = 36 V		±0.3	±2.5	mV
		T_A = –55°C to 125°C			±5.5	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –55°C to 125°C		±4	±20	µV/°C
PSRR	Power-supply rejection ratio	T_A = 25°C		15	100	µV/V
		T_A = –55°C to 125°C		20		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –55°C to 125°C	(V–)		(V+)	V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		5	15	nA
		T_A = –55°C to 125°C			20	nA
I_{OS}	Input offset current	T_A = 25°C		0.5		nA
C_{LOAD}	Capacitive load drive		See 节 6.7			
OUTPUT						
V_O	Voltage output swing from rail	I_O ≤ 4 mA, input overdrive = 100 mV, V_S = 36 V			1100	mV
		I_O = 0 mA, input overdrive = 100 mV, V_S = 36 V			700	mV
I_{SC}	Short circuit sink current	T_A = 25°C		20		mA
	Output leakage current	V_{IN+} > V_{IN-}, T_J = 25°C		70		nA
POWER SUPPLY						
V_S	Specified voltage range		2.2		36	V
I_Q	Quiescent current (per channel)	I_O = 0 A, T_A = 25°C		55	75	µA
		I_O = 0 A, T_A = –55°C to 125°C			100	µA

6.6 Switching Characteristics

at T_A = –55°C to 125°C, V_S = 2.2 V to 36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL}	Propagation delay time, high-to-low	Input overdrive = 100 mV, T_A = 25°C		460		ns
t_{pLH}	Propagation delay time, low-to-high	Input overdrive = 100 mV, T_A = 25°C		560		ns
t_R	Rise time	Input overdrive = 100 mV, T_A = 25°C		365		ns
t_F	Fall time	Input overdrive = 100 mV, T_A = 25°C		240		ns

6.7 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)

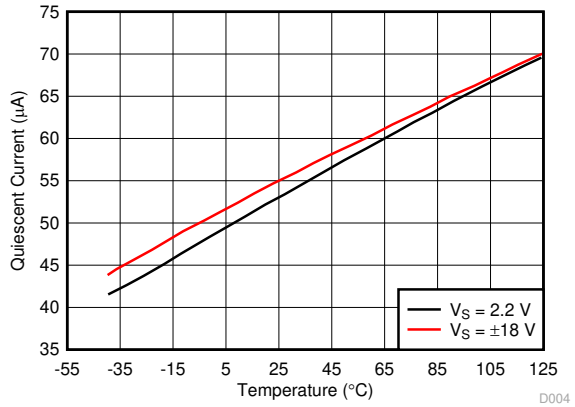


图 6-1. Quiescent Current vs Temperature

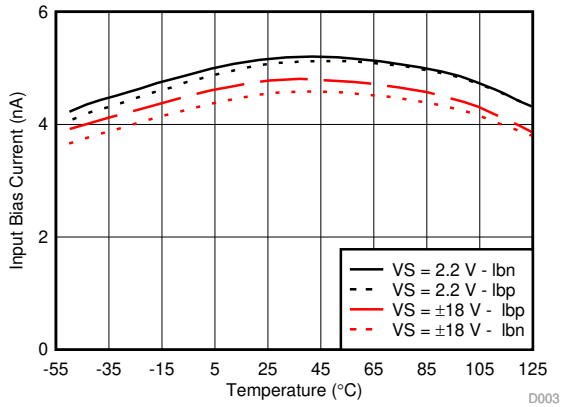


图 6-2. Input Bias Current vs Temperature

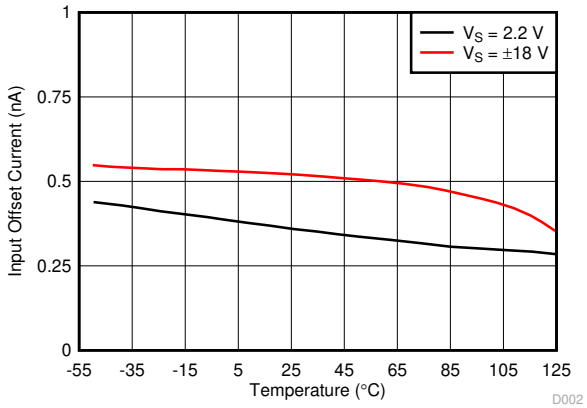


图 6-3. Input Offset Current vs Temperature

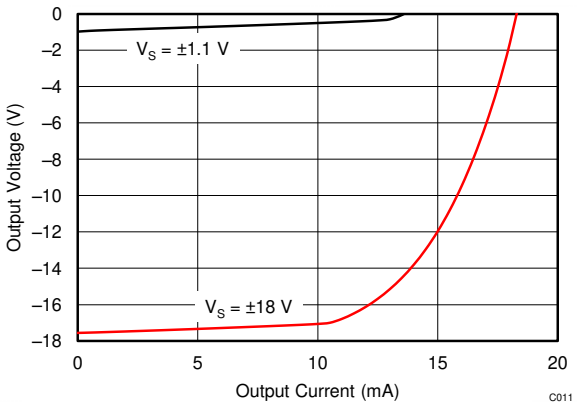
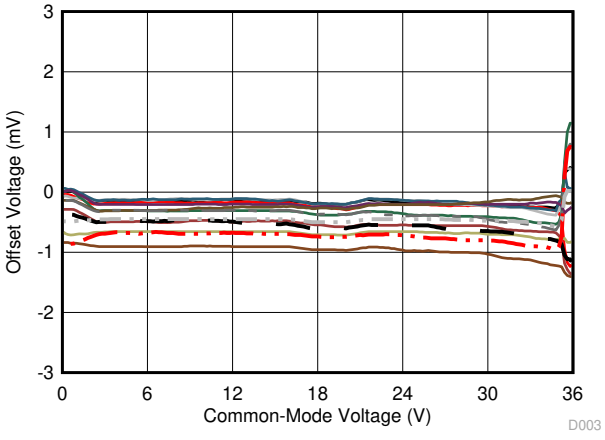
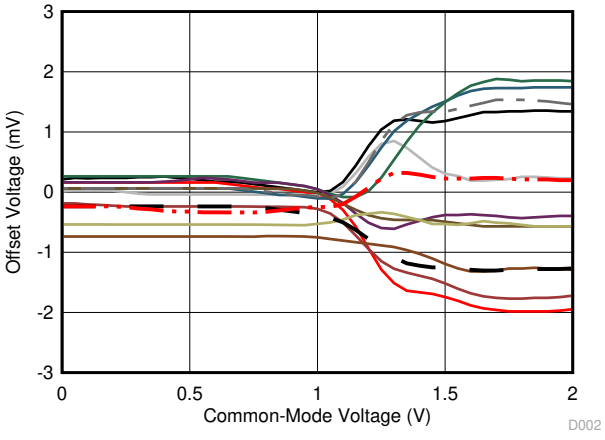


图 6-4. Output Voltage vs Output Current



V_S = ±18 V　　14 typical units shown

图 6-5. Offset Voltage vs Common-Mode Voltage

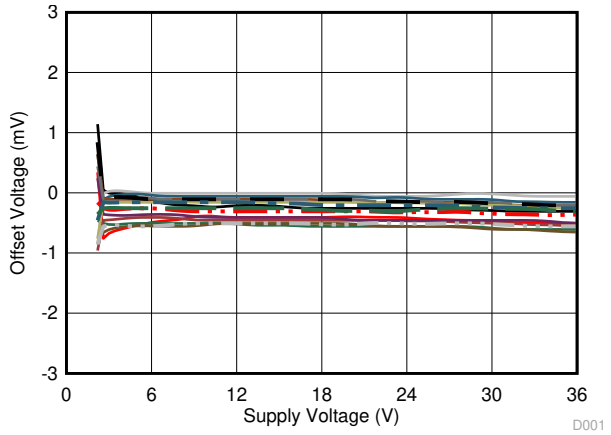


V_S = 2.2 V　　13 typical units shown

图 6-6. Offset Voltage vs Common-Mode Voltage

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



16 typical units shown

图 6-7. Offset Voltage vs Supply Voltage

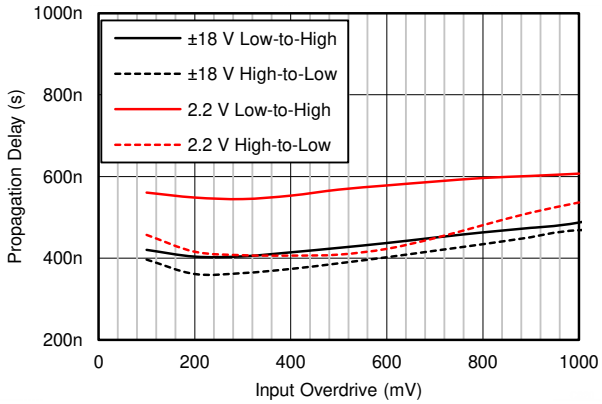


图 6-8. Propagation Delay vs Input Overdrive

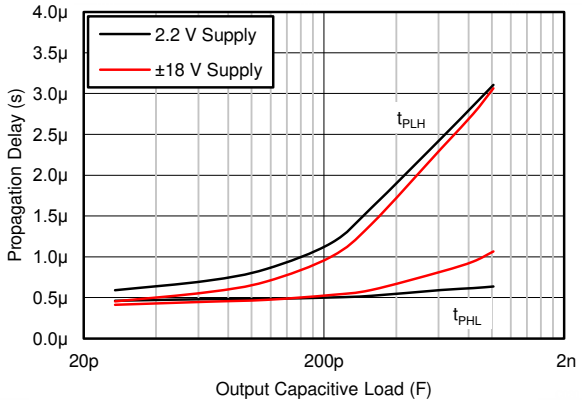
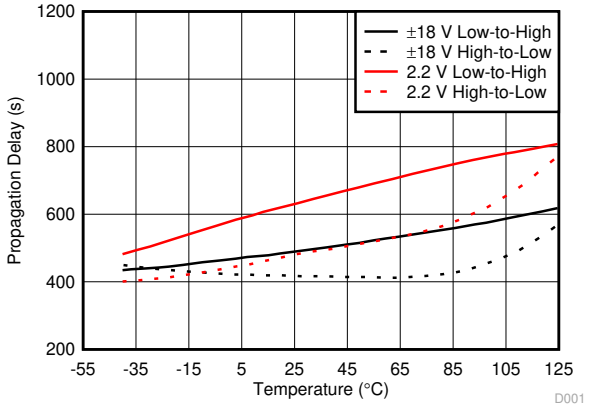
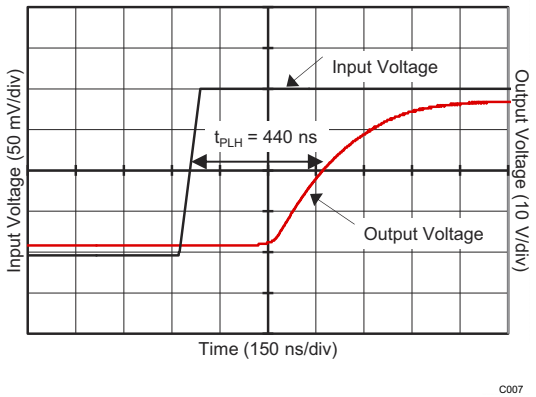


图 6-9. Propagation Delay vs Capacitive Load



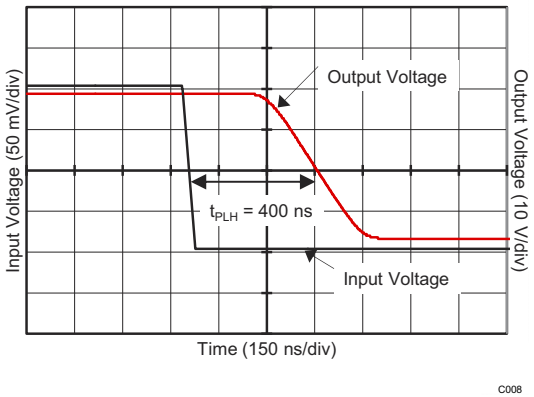
V_{OD} = 100 mV

图 6-10. Propagation Delay vs Temperature



V_S = 36 V Overdrive = 100 mV

图 6-11. Propagation Delay (T_{pLH})

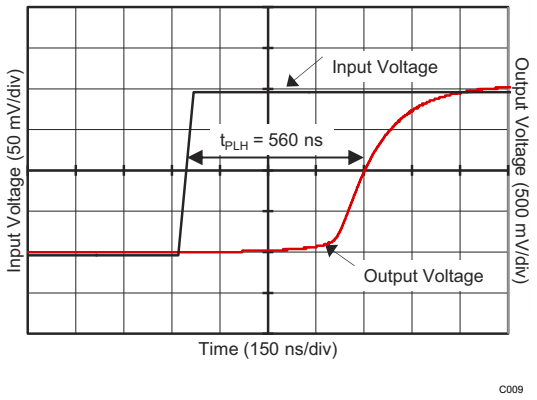


V_S = 36 V Overdrive = 100 mV

图 6-12. Propagation Delay (T_{pHL})

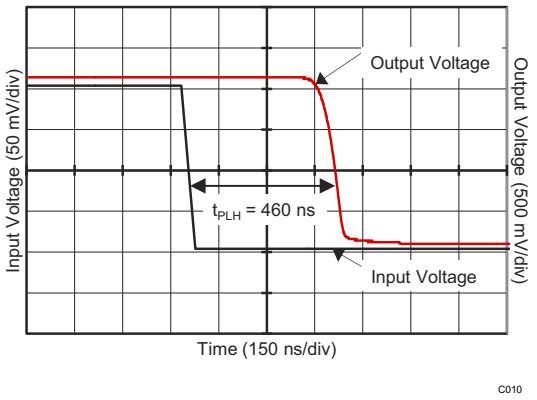
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1 kΩ, and input overdrive = 100 mV (unless otherwise noted)



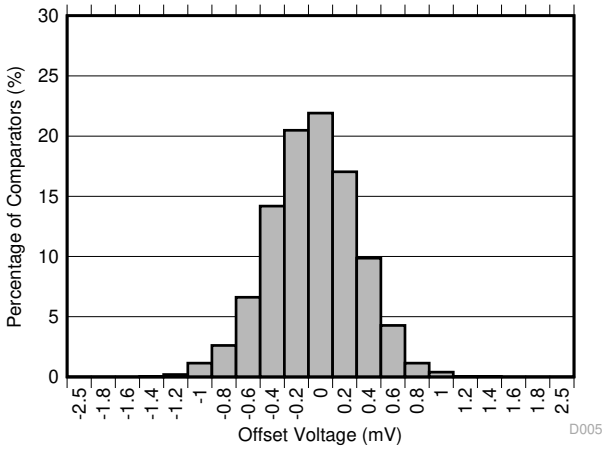
V_S = 2.2 V Overdrive = 100 mV

图 6-13. Propagation Delay (T_{pLH})



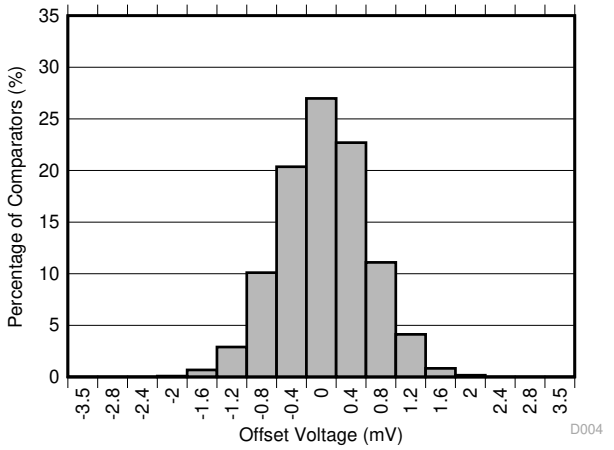
V_S = 2.2 V Overdrive = 100 mV

图 6-14. Propagation Delay (T_{pHL})



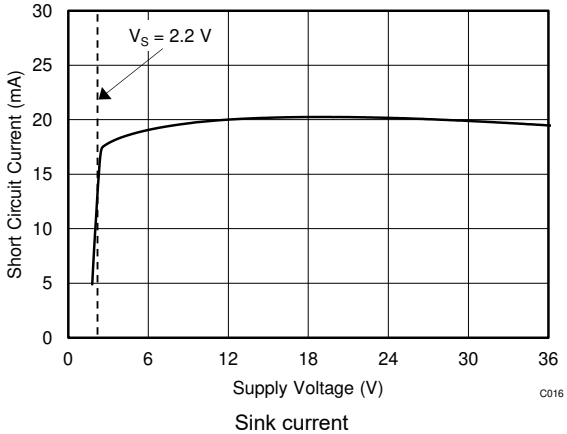
V_S = ±18 V Distribution taken from 2524 comparators

图 6-15. Offset Voltage Production Distribution



V_S = 2.2 V Distribution taken from 2524 comparators

图 6-16. Offset Voltage Production Distribution



Sink current

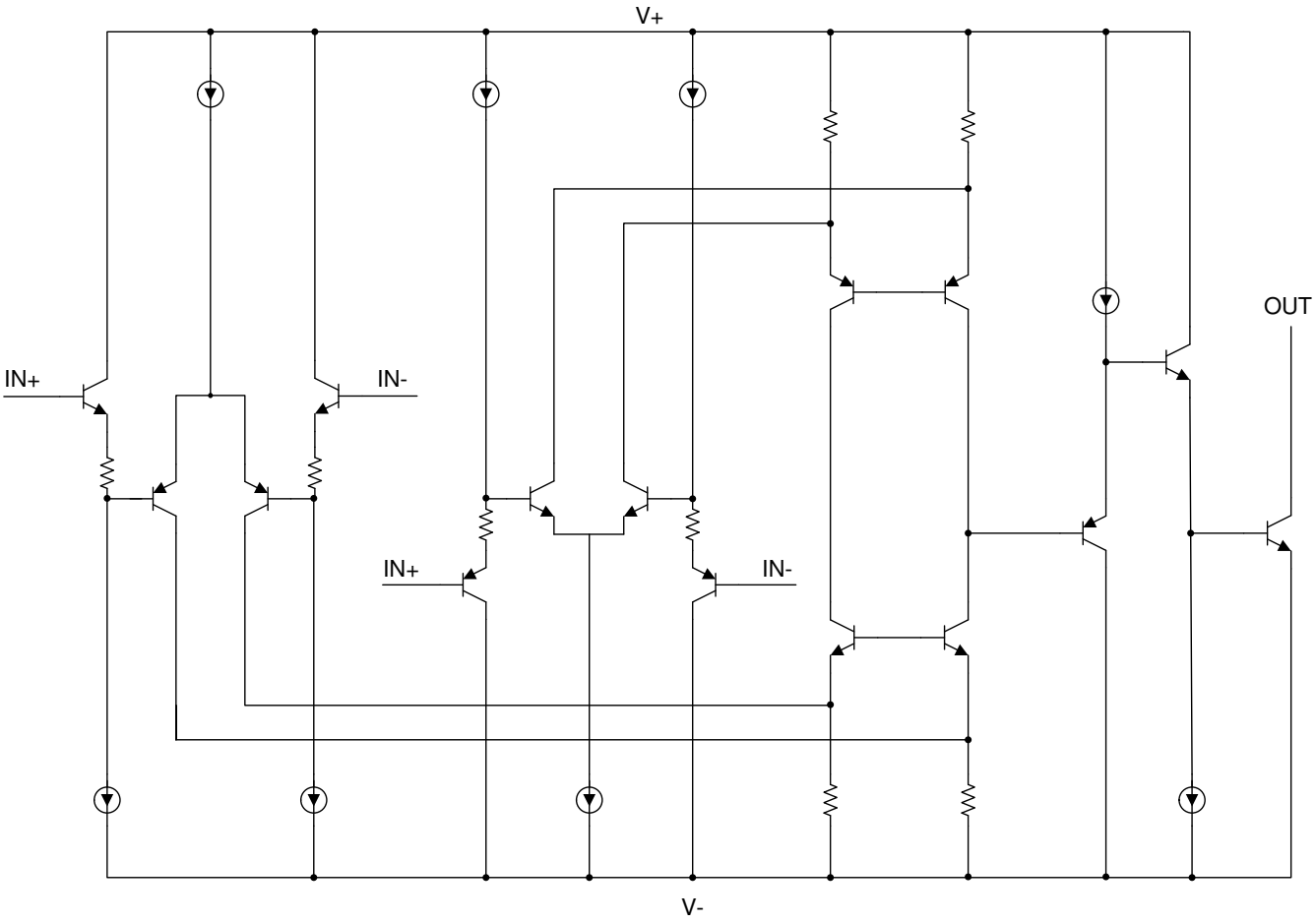
图 6-17. Short-Circuit Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The TLV1704-SEP comparator features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open-collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 µA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Comparator Inputs

The TLV1704-SEP device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV1704-SEP device is designed to prevent phase inversion when the input pins exceed the supply voltage. 图 7-1 shows the TLV1704-SEP device response when input voltages exceed the supply, resulting in no phase inversion.

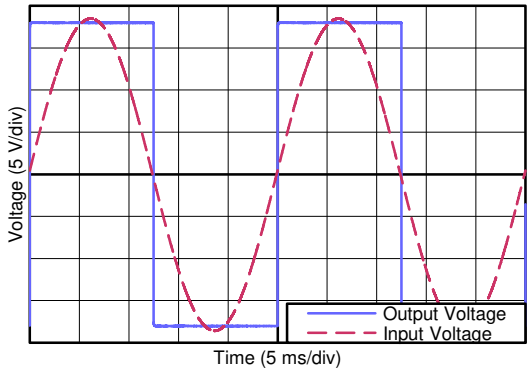


图 7-1. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

7.4 Device Functional Modes

7.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV1704-SEP device. The REF3333, as shown in 图 7-2, provides a 3.3-V reference voltage with low drift and only 3.9 μA of quiescent current.

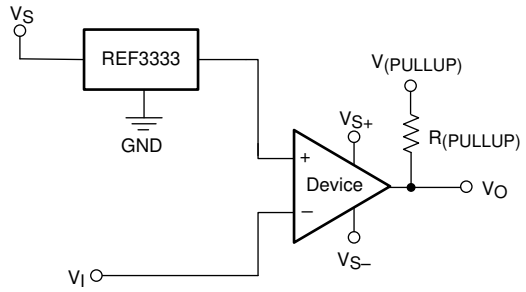


图 7-2. Reference Voltage for the TLV1704-SEP

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TLV1704-SEP device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

8.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

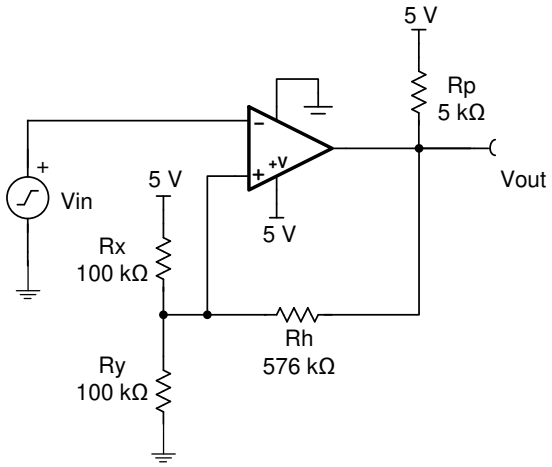


图 8-1. Comparator Schematic With Hysteresis

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V ±0.1 V
- Upper threshold (VH) = 2.7 V ±0.1 V
- VH – VL = 2.4 V ±0.1 V
- Low-power consumption

8.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

图 8-1 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if Rh > 100 Rp.

When the output is at a logic high (5 V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above VH = 2.7 V to cause the output to transition to logic low (0 V).

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below VL = 2.3 V to cause the output to transition to logic high (5 V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

8.2.3 Application Curve

图 8-2 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

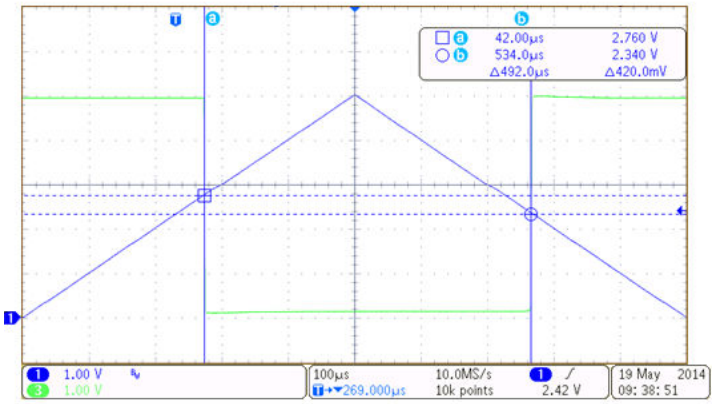


图 8-2. TLV1701 Upper and Lower Threshold With Hysteresis

8.3 Power Supply Recommendations

The TLV1704-SEP device is specified for operation from 2.2 V to 36 V (±1.1 to ±18 V); many specifications apply from –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the 节 *6.7* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the 节 *6.1*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the 节 *8.4.1* section.

8.4 Layout

8.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1704-SEP device.
- To minimize supply noise, place a decoupling capacitor (0.1- μ F ceramic, surface-mount capacitor) as close as possible to V_S as shown in 图 8-3.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

8.4.2 Layout Example

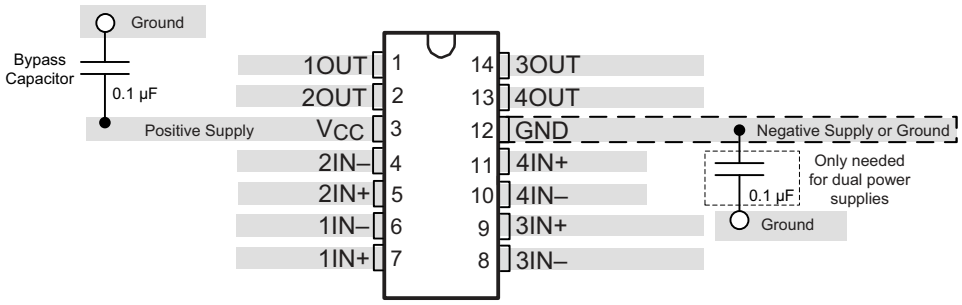


图 8-3. Comparator Board Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- *Precision Design, Comparator with Hysteresis Reference Design*, TIDU020
- *REF33xx 3.9-μA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/°C Drift Voltage Reference*, SBOS392

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1704AMPWPSEP	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
TLV1704AMPWTPSEP	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE-T	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV1704-SEP :

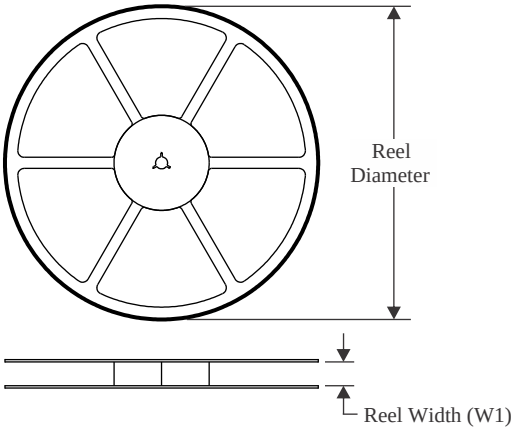
- Automotive : TLV1704-Q1

NOTE: Qualified Version Definitions:

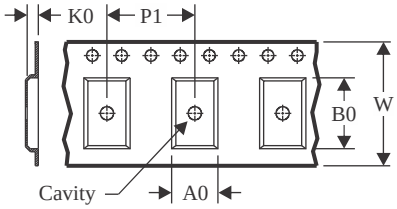
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

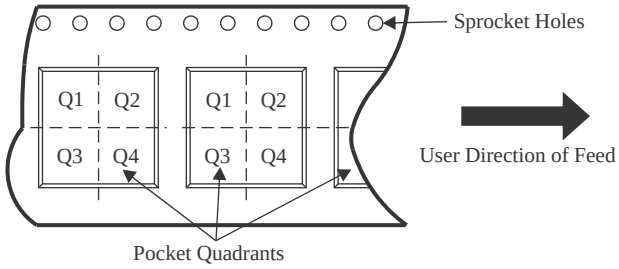


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

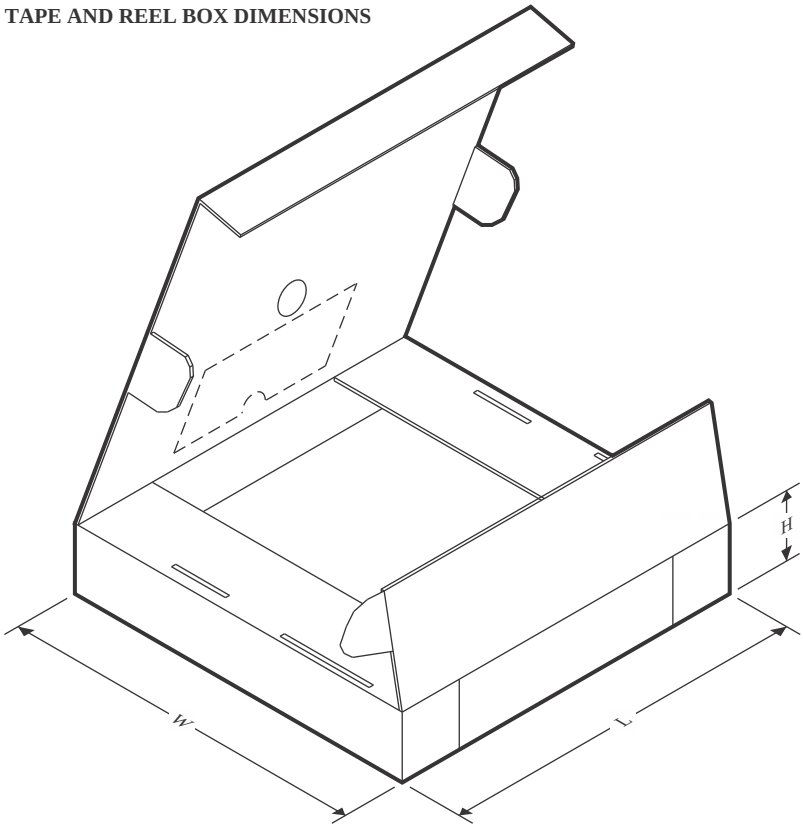
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1704AMPWTPSEP	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

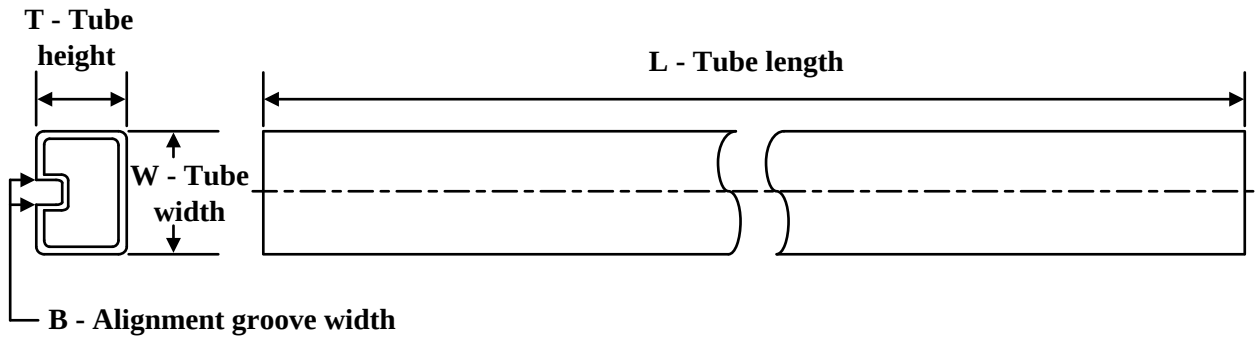
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1704AMPWTPSEP	TSSOP	PW	14	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

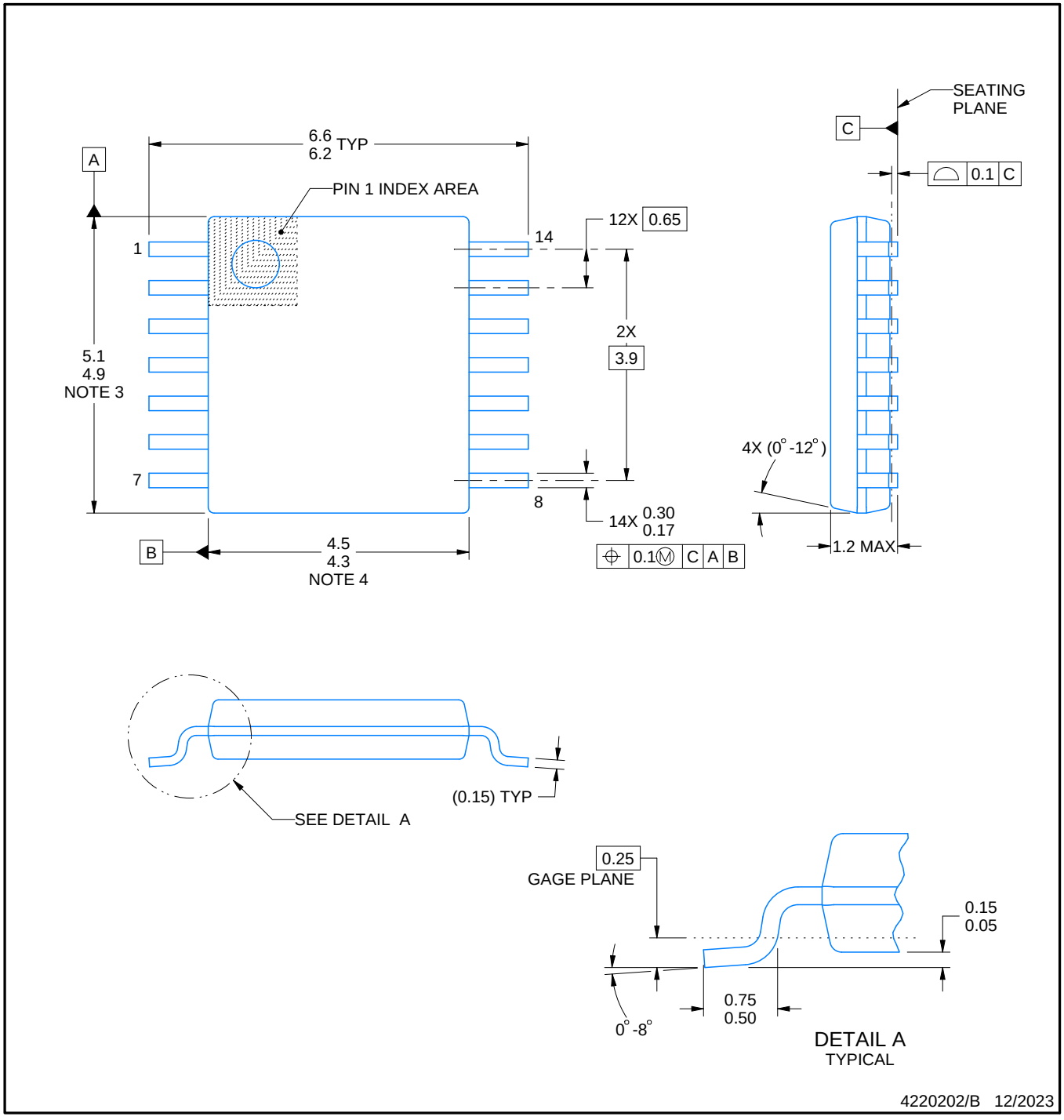
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV1704AMPWPSEP	PW	TSSOP	14	90	530	10.2	3600	3.5
V62/18613-01XE-T	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

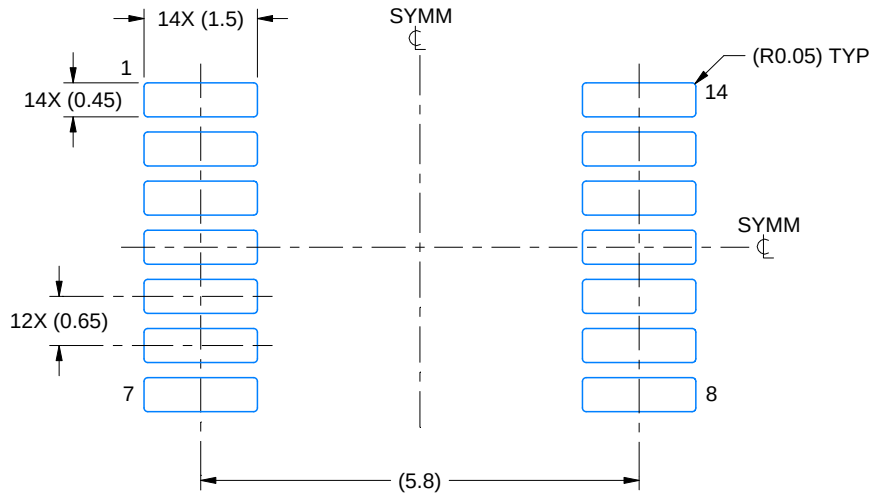
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

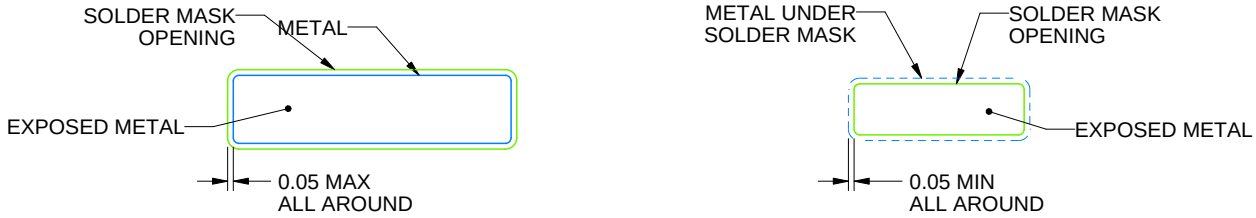


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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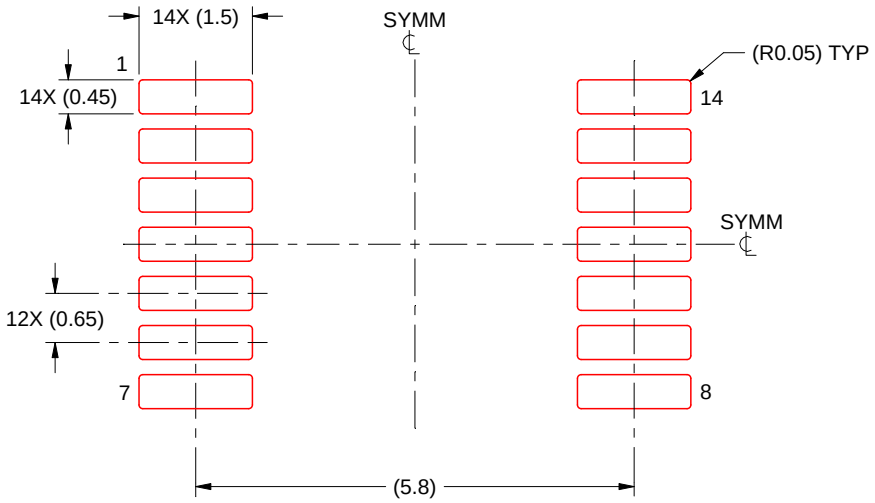
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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