

# TLV2241, TLV2242, TLV2244 FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

SLOS329C – JULY 2000 REVISED - NOVEMBER 2000

- **Micropower Operation . . . 1  $\mu$ A/Channel**
- **Rail-to-Rail Input/Output**
- **Gain Bandwidth Product . . . 5.5 kHz**
- **Supply Voltage Range . . . 2.5 V to 12 V**
- **Specified Temperature Range**
  - $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  . . . **Commercial Grade**
  - $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  . . . **Industrial Grade**
- **Ultrasmall Packaging**
  - **5-Pin SOT-23 (TLV2241)**
  - **8-Pin MSOP (TLV2242)**
- **Universal OpAmp EVM**

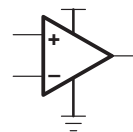
## description

The TLV224x family of single-supply operational amplifiers offers very low supply current of only 1  $\mu$ A per channel.

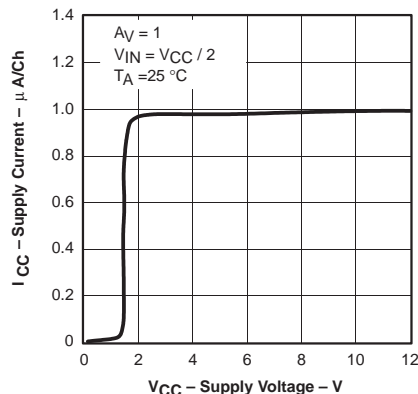
The low supply current is coupled with extremely low input bias currents enabling them to be used with mega- $\Omega$  resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 600  $\mu$ V, CMRR of 100 dB, and minimum open loop gain of 100 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 12 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 12 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micropower microcontrollers available today including TI's MSP430.

Operational Amplifier



SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE



FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES					UNIVERSAL EVM
		PDIP	SOIC	SOT-23	TSSOP	MSOP	
TLV2241	1	8	8	5	—	—	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2242	2	8	8	—	—	8	
TLV2244	4	14	14	—	14	—	

SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V <sub>DD</sub> (V)	V <sub>IO</sub> (mV)	BW (MHz)	SLEW RATE (V/ $\mu$ s)	I <sub>DD</sub> (PER CHANNEL) ( $\mu$ A)	RAIL-TO-RAIL
TLV240x‡	2.5–16	0.390	0.005	0.002	0.880	I/O
TLV224x	2.5–12	0.600	0.005	0.002	1	I/O
TLV2211	2.7–10	0.450	0.065	0.025	13	O
TLV245x	2.7–6	0.020	0.22	0.110	23	I/O
TLV225x	2.7–8	0.200	0.2	0.12	35	O

† All specifications are typical values measured at 5 V.

‡ This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# TLV2241, TLV2242, TLV2244

## FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

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### TLV2241 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	SOT-23‡ (DBV)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 $\mu$ V	TLV2241CD	—	—	—
-40°C to 125°C		TLV2241ID	TLV2241DBV	VBEI	TLV2241IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2241CDR).

‡ This package is available in a 250 piece mini-reel. To order this package, add a T suffix to the part number (e.g., TLV2241DBVT). This package is also available in a 3000 piece reel, add a R suffix to the part number (e.g., TLV2241DBVR).

### TLV2242 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	MSOP† (DGK)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 $\mu$ V	TLV2242CD	—	—	—
-40°C to 125°C		TLV2242ID	TLV2242IDGK	xxTIALE	TLV2242IP

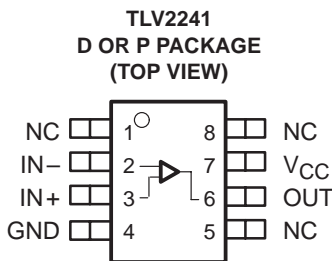
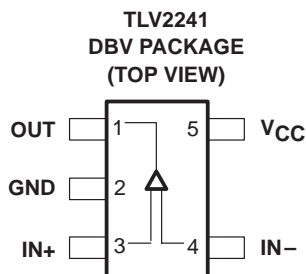
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2242CDR).

### TLV2244 AVAILABLE OPTIONS

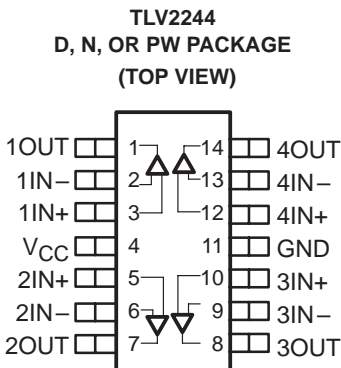
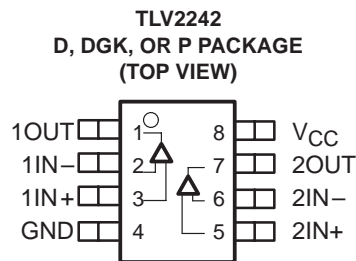
T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	3000 $\mu$ V	TLV2244CD	—	—
-40°C to 125°C		TLV2244ID	TLV2244IN	TLV2244IPW

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2244CDR).

### TLV224x PACKAGE PINOUTS



NC – No internal connection



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	16.5 V
Differential input voltage, $V_{ID}$	$\pm V_{CC}$
Input current, $I_I$ (any input)	$\pm 10$ mA
Output current, $I_O$	$\pm 10$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Maximum junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

**DISSIPATION RATING TABLE**

PACKAGE	$\Theta_{JC}$ (°C/W)	$\Theta_{JA}$ (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

**recommended operating conditions**

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$	Single supply	2.5	12	V
	Split supply	$\pm 1.25$	$\pm 6$	
Common-mode input voltage range, $V_{ICR}$		0	$V_{CC}$	V
Operating free-air temperature, $T_A$	C-suffix	0	70	°C
	I-suffix	–40	125	



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electrical characteristics at recommended operating conditions,  $V_{CC} = 2.7, 5 \text{ V}$ , and  $12 \text{ V}$  (unless otherwise noted)†‡

### dc performance

PARAMETER		TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = V_{CC}/2 \text{ V}$ , $V_{IC} = V_{CC}/2 \text{ V}$ , $R_S = 50 \Omega$	25°C	600	3000		$\mu\text{V}$
			Full range		4500		
$\alpha V_{IO}$	Offset voltage drift		25°C	3			$\mu\text{V}/^\circ\text{C}$
CMRR	Common-mode rejection ratio	$V_{IC} = 0 \text{ to } V_{CC}$ , $R_S = 50 \Omega$	$V_{CC} = 2.7 \text{ V}$	25°C	55	100	dB
				Full range	50		
			$V_{CC} = 5 \text{ V}$	25°C	60	100	
				Full range	53		
			$V_{CC} = 12 \text{ V}$	25°C	60	100	
				Full range	55		
AVD	Large-signal differential voltage amplification	$V_{CC} = 2.7 \text{ V}$ , $V_{O(pp)} = 1 \text{ V}$ , $R_L = 500 \text{ k}\Omega$	25°C	100	400	V/mV	
			Full range	30			
			$V_{CC} = 5 \text{ V}$ , $V_{O(pp)} = 3 \text{ V}$ , $R_L = 500 \text{ k}\Omega$	25°C	250		1000
				Full range	100		
			$V_{CC} = 12 \text{ V}$ , $V_{O(pp)} = 6 \text{ V}$ , $R_L = 500 \text{ k}\Omega$	25°C	700		1500
				Full range	120		

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

### input characteristics

PARAMETER		TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$I_{IO}$	Input offset current	$V_O = V_{CC}/2 \text{ V}$ , $V_{IC} = V_{CC}/2 \text{ V}$ , $R_S = 50 \Omega$	25°C	25	250		pA
			Full range	TLV224xC	300		
				TLV224xI	400		
$I_{IB}$	Input bias current	$V_O = V_{CC}/2 \text{ V}$ , $V_{IC} = V_{CC}/2 \text{ V}$ , $R_S = 50 \Omega$	25°C	100	500		pA
			Full range	TLV224xC	550		
				TLV224xI	1000		
$r_{i(d)}$	Differential input resistance		25°C	300		$\text{M}\Omega$	
$C_{i(c)}$	Common-mode input capacitance	$f = 100 \text{ kHz}$	25°C	3		pF	

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

‡ Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.



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electrical characteristics at recommended operating conditions,  $V_{CC} = 2.7, 5 \text{ V}$ , and  $12 \text{ V}$  (unless otherwise noted)<sup>†</sup> (continued)

**output characteristics**

PARAMETER	TEST CONDITIONS	$T_A$ <sup>†</sup>	MIN	TYP	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IC} = V_{CC}/2$ , $I_{OH} = -2 \mu\text{A}$	$V_{CC} = 2.7 \text{ V}$	25°C	2.65	2.68	V
			Full range	2.63		
		$V_{CC} = 5 \text{ V}$	25°C	4.95	4.98	
			Full range	4.93		
		$V_{CC} = 12 \text{ V}$	25°C	11.95	11.98	
			Full range	11.93		
	$V_{IC} = V_{CC}/2$ , $I_{OH} = -50 \mu\text{A}$	$V_{CC} = 2.7 \text{ V}$	25°C	2.62	2.65	
			Full range	2.6		
		$V_{CC} = 5 \text{ V}$	25°C	4.92	4.95	
			Full range	4.9		
		$V_{CC} = 12 \text{ V}$	25°C	11.92	11.95	
			Full range	11.9		
$V_{OL}$ Low-level output voltage	$V_{IC} = V_{CC}/2$ , $I_{OL} = 2 \mu\text{A}$	25°C		90	150	mV
		Full range			180	
	$V_{IC} = V_{CC}/2$ , $I_{OL} = 50 \mu\text{A}$	25°C		180	230	
		Full range			260	
$I_O$ Output current	$V_O = 0.5 \text{ V}$ from rail	25°C		$\pm 200$		$\mu\text{A}$

<sup>†</sup> Full range is 0°C to 70°C for the C suffix and -40°C to 125°C for the I suffix. If not specified, full range is -40°C to 125°C.

**power supply**

PARAMETER	TEST CONDITIONS	$T_A$ <sup>†</sup>	MIN	TYP	MAX	UNIT
$I_{CC}$ Supply current (per channel)	$V_O = V_{CC}/2$	$V_{CC} = 2.7 \text{ V}$ or $5 \text{ V}$	25°C	980	1200	nA
			Full range		1500	
		$V_{CC} = 12 \text{ V}$	25°C	1000	1250	
			Full range		1550	
PSRR Power supply rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC} = 2.7$ to $5 \text{ V}$ , $V_{IC} = V_{CC}/2 \text{ V}$ , No load,	TLV224xC	25°C	70	100	dB
			Full range	65		
		TLV224xI	Full range	60		dB
	$V_{CC} = 5$ to $12 \text{ V}$ , $V_{IC} = V_{CC}/2 \text{ V}$ , No load	25°C	70	100	dB	
		Full range	70			

<sup>†</sup> Full range is 0°C to 70°C for the C suffix and -40°C to 125°C for the I suffix. If not specified, full range is -40°C to 125°C.

<sup>‡</sup> Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.



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**electrical characteristics at recommended operating conditions,  $V_{CC} = 2.7, 5 \text{ V}$ , and  $12 \text{ V}$  (unless otherwise noted)† (continued)**

**dynamic performance**

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 500 \text{ k}\Omega$ ,	$C_L = 100 \text{ pF}$	$25^\circ\text{C}$		5.5		kHz
SR	Slew rate at unity gain	$V_{O(pp)} = 0.8 \text{ V}$ ,	$R_L = 500 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$	$25^\circ\text{C}$		2		V/ms
$\phi M$	Phase margin	$R_L = 500 \text{ k}\Omega$ ,	$C_L = 100 \text{ pF}$	$25^\circ\text{C}$		60		
	Gain margin					15		dB
$t_s$	Settling time	$V_{CC} = 2.7 \text{ or } 5 \text{ V}$ , $V(\text{STEP})_{PP} = 1 \text{ V}$ , $A_V = -1$ ,	$C_L = 100 \text{ pF}$ , $R_L = 100 \text{ k}\Omega$	$25^\circ\text{C}$		1.84		ms
					0.1%		6.1	
					0.01%		32	

**noise/distortion performance**

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_n$	Equivalent input noise voltage	$f = 10 \text{ Hz}$	$25^\circ\text{C}$		800		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100 \text{ Hz}$			500		
$I_n$	Equivalent input noise current	$f = 100 \text{ Hz}$			8		$\text{fA}/\sqrt{\text{Hz}}$

† Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.



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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			<b>FIGURE</b>
$V_{IO}$	Input offset voltage	vs Common-mode input voltage	1, 2, 3
$I_{IB}$	Input bias current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
$I_{IO}$	Input offset current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
CMRR	Common-mode rejection ratio	vs Frequency	10
$V_{OH}$	High-level output voltage	vs High-level output current	11, 13, 15
$V_{OL}$	Low-level output voltage	vs Low-level output current	12, 14, 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	17
$Z_o$	Output impedance	vs Frequency	18
$I_{CC}$	Supply current	vs Supply voltage	19
PSRR	Power supply rejection ratio	vs Frequency	20
$A_{VD}$	Differential voltage gain	vs Frequency	21
	Phase	vs Frequency	21
	Gain-bandwidth product	vs Supply voltage	22
SR	Slew rate	vs Free-air temperature	23
$\phi_m$	Phase margin	vs Capacitive load	24
	Gain margin	vs Capacitive load	25
	Voltage noise over a 10 Second Period		26
	Large-signal voltage follower		27, 28, 29
	Small-signal voltage follower		30
	Large-signal inverting pulse response		31, 32, 33
	Small-signal inverting pulse response		34
	Crosstalk	vs Frequency	35

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## TYPICAL CHARACTERISTICS

**INPUT OFFSET VOLTAGE  
vs  
COMMON-MODE INPUT  
VOLTAGE**

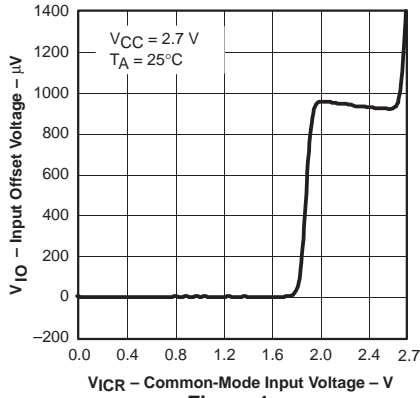


Figure 1

**INPUT OFFSET VOLTAGE  
vs  
COMMON-MODE INPUT  
VOLTAGE**

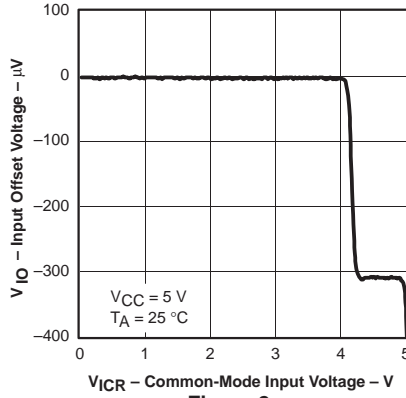


Figure 2

**INPUT OFFSET VOLTAGE  
vs  
COMMON-MODE INPUT  
VOLTAGE**

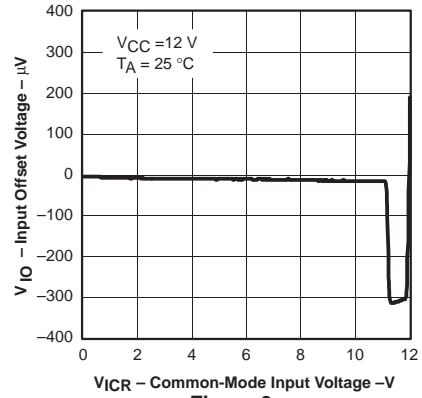


Figure 3

**INPUT BIAS / OFFSET CURRENT  
vs  
FREE-AIR TEMPERATURE**

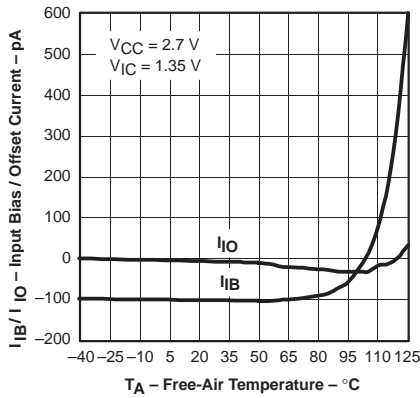


Figure 4

**INPUT BIAS / OFFSET CURRENT  
vs  
COMMON MODE INPUT  
VOLTAGE**

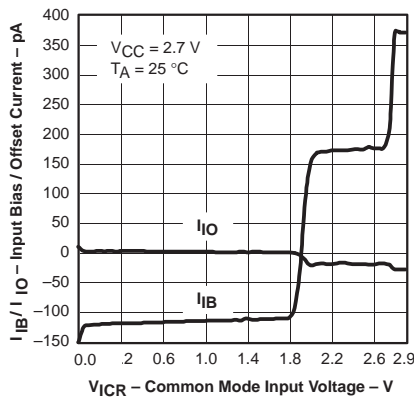


Figure 5

**INPUT BIAS / OFFSET CURRENT  
vs  
FREE-AIR TEMPERATURE**

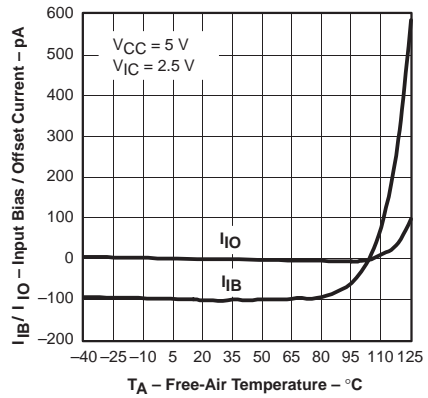


Figure 6

**INPUT BIAS / OFFSET CURRENT  
vs  
COMMON-MODE INPUT  
VOLTAGE**

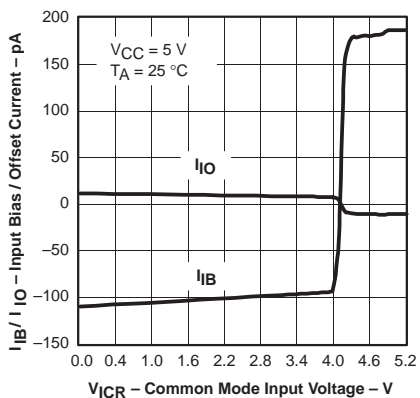


Figure 7

**INPUT BIAS / OFFSET CURRENT  
vs  
FREE-AIR TEMPERATURE**

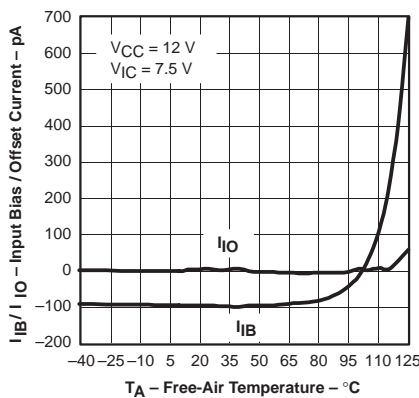


Figure 8

**INPUT BIAS / OFFSET CURRENT  
vs  
COMMON-MODE INPUT  
VOLTAGE**

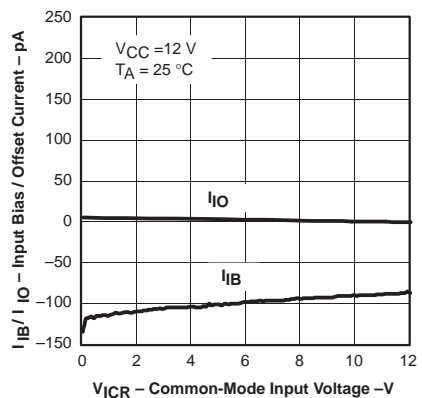


Figure 9





TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO  
 vs  
 FREQUENCY

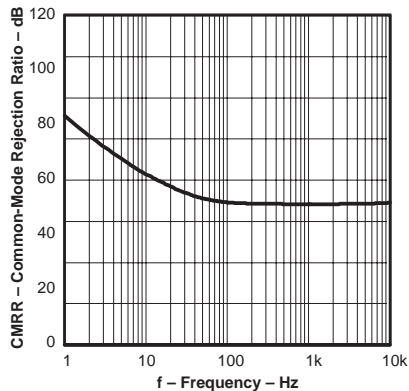


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE  
 vs  
 HIGH-LEVEL OUTPUT CURRENT

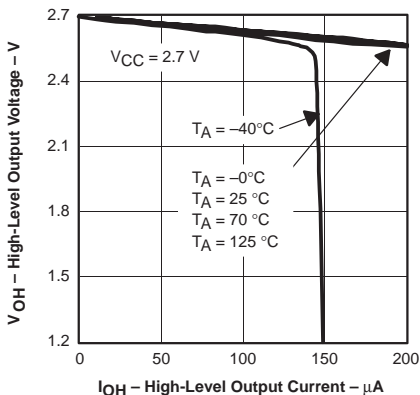


Figure 11

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT



Figure 12

HIGH-LEVEL OUTPUT VOLTAGE  
 vs  
 HIGH-LEVEL OUTPUT CURRENT

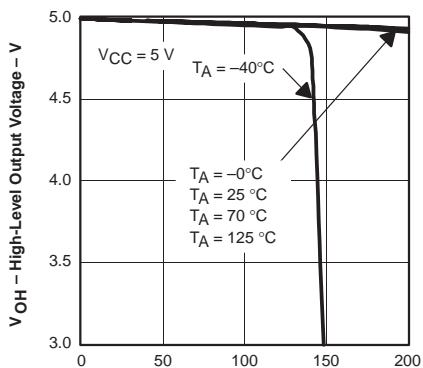


Figure 13

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

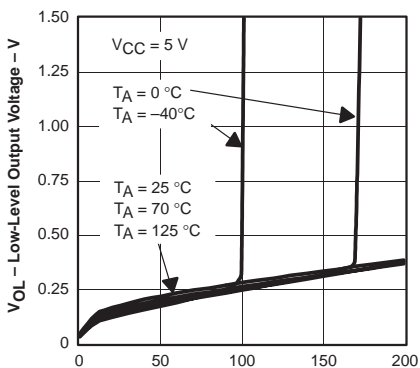


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE  
 vs  
 HIGH-LEVEL OUTPUT CURRENT

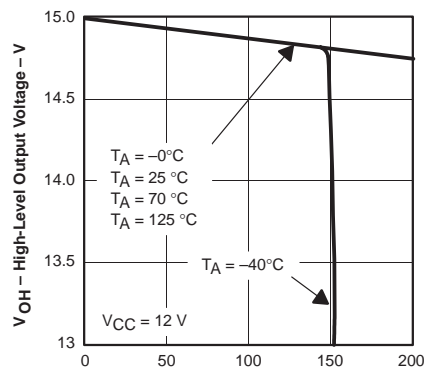


Figure 15

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

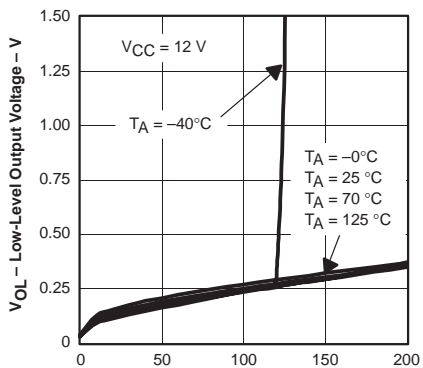


Figure 16

OUTPUT VOLTAGE  
 PEAK-TO-PEAK  
 vs  
 FREQUENCY

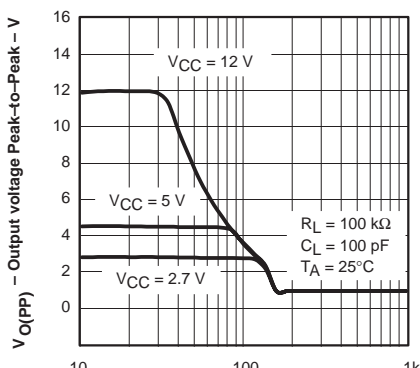


Figure 17

OUTPUT IMPEDANCE  
 vs  
 FREQUENCY

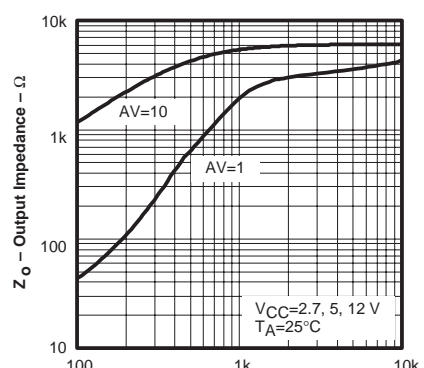
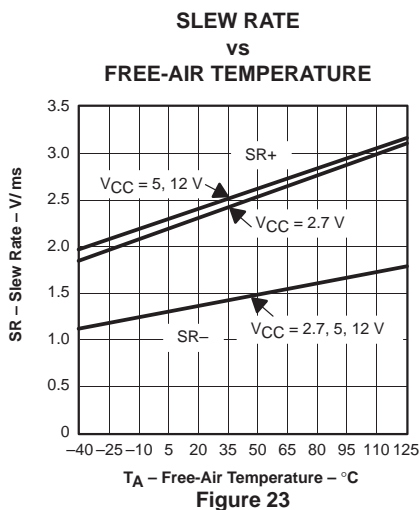
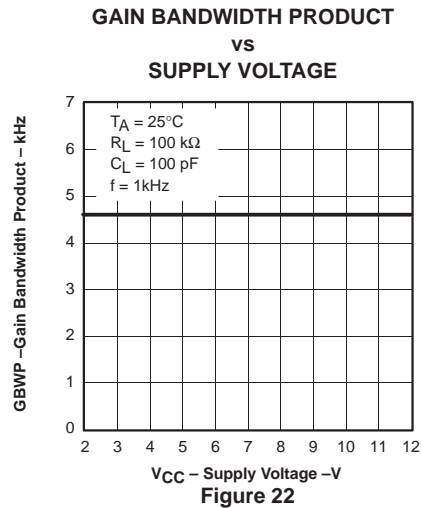
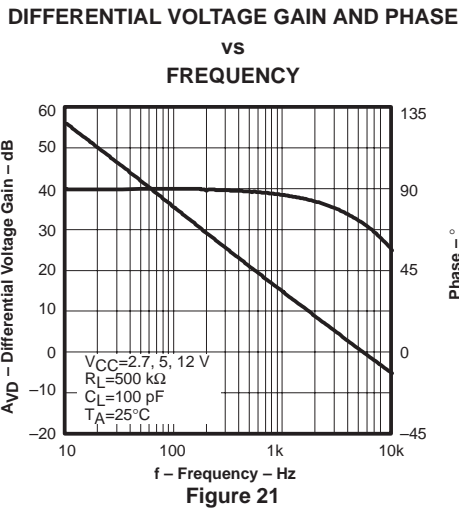
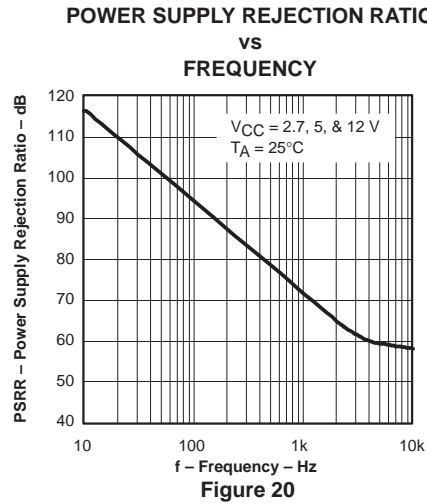
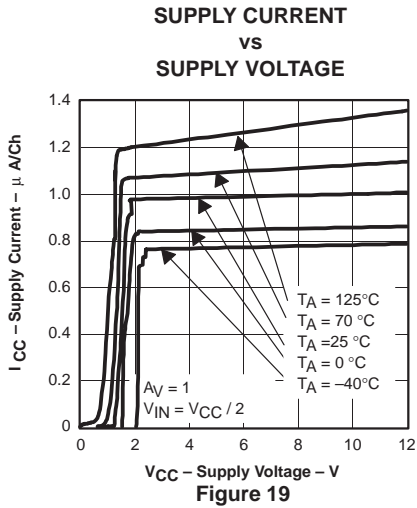


Figure 18

# TLV2241, TLV2242, TLV2244 FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

SLOS329C – JULY 2000 REVISED - NOVEMBER 2000

## TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

GAIN MARGIN  
 VS  
 CAPACITIVE LOAD

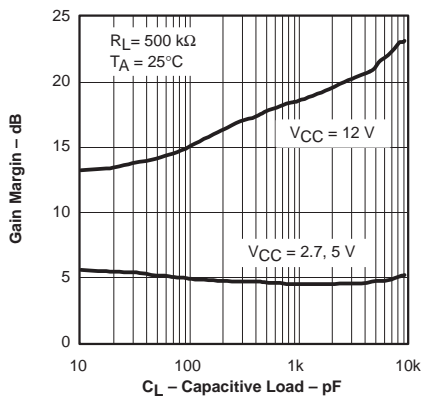


Figure 25

VOLTAGE NOISE  
 OVER A 10 SECOND PERIOD

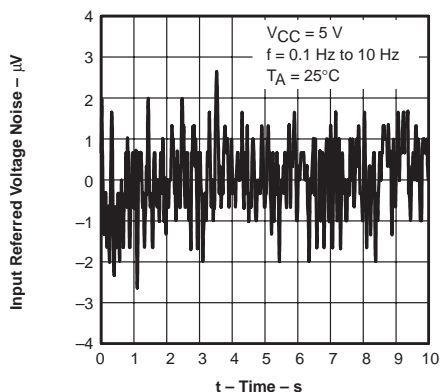


Figure 26

LARGE SIGNAL FOLLOWER  
 PULSE RESPONSE

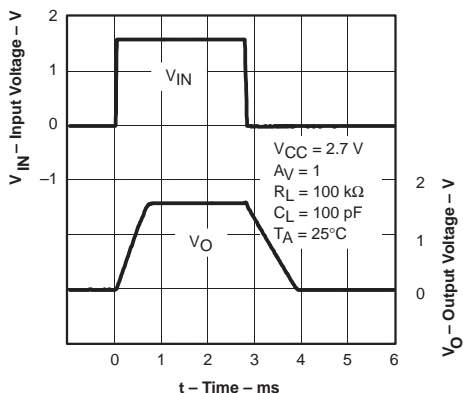


Figure 27

LARGE SIGNAL FOLLOWER  
 PULSE RESPONSE

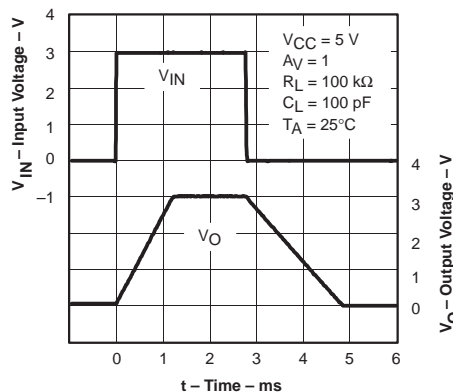


Figure 28

LARGE SIGNAL FOLLOWER  
 PULSE RESPONSE



Figure 29

SMALL SIGNAL FOLLOWER  
 PULSE RESPONSE

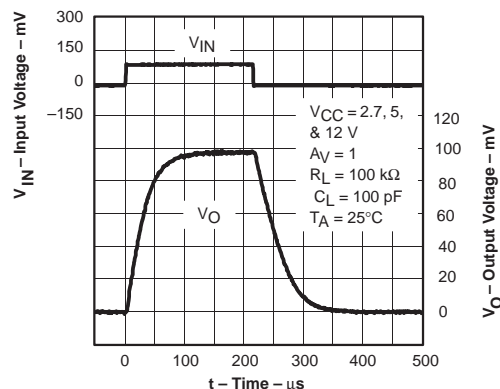


Figure 30

# TLV2241, TLV2242, TLV2244 FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

SLOS329C – JULY 2000 REVISED - NOVEMBER 2000

## TYPICAL CHARACTERISTICS

**LARGE SIGNAL INVERTING  
PULSE RESPONSE**

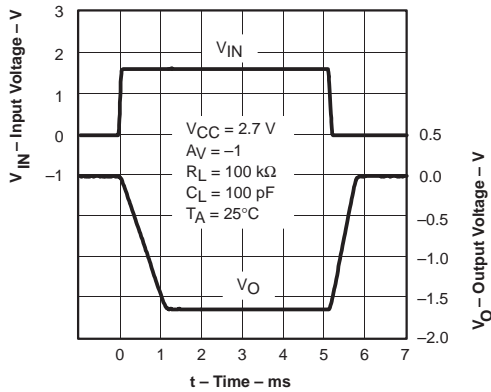


Figure 31

**LARGE SIGNAL INVERTING  
PULSE RESPONSE**

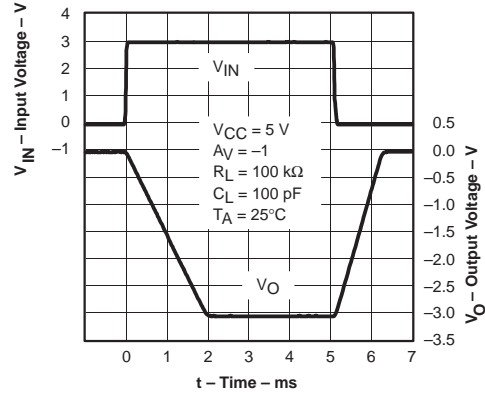


Figure 32

**LARGE SIGNAL INVERTING  
PULSE RESPONSE**

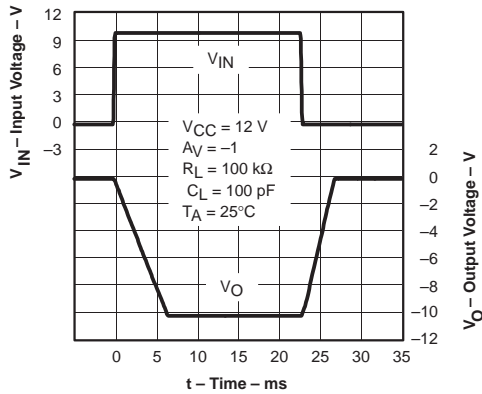


Figure 33

**SMALL SIGNAL INVERTING  
PULSE RESPONSE**

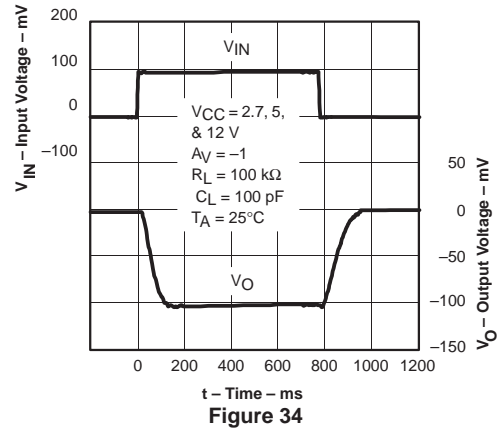


Figure 34

### CROSTALK vs FREQUENCY

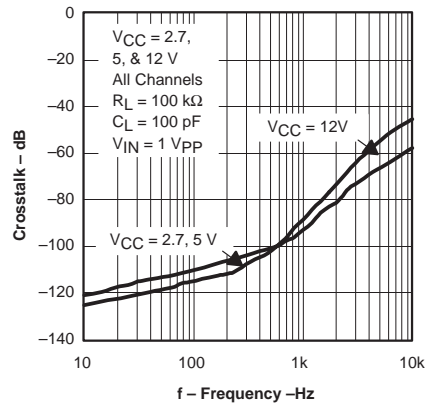
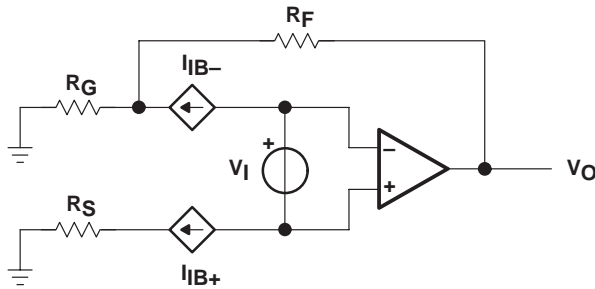


Figure 35

APPLICATION INFORMATION

offset voltage

The output offset voltage, ( $V_{OO}$ ) is the sum of the input offset voltage ( $V_{IO}$ ) and both input bias currents ( $I_{IB}$ ) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

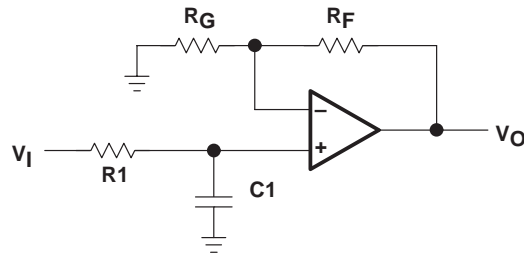


$$V_{OO} = V_{IO} \left( 1 + \left( \frac{R_F}{R_G} \right) \right) \pm I_{IB+} R_S \left( 1 + \left( \frac{R_F}{R_G} \right) \right) \pm I_{IB-} R_F$$

Figure 36. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 37).

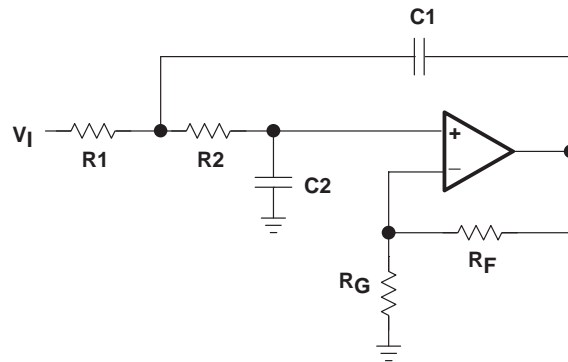


$$f_{-3dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_O}{V_I} = \left( 1 + \frac{R_F}{R_G} \right) \left( \frac{1}{1 + sR_1 C_1} \right)$$

Figure 37. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



$R_1 = R_2 = R$   
 $C_1 = C_2 = C$   
 $Q = \text{Peaking Factor}$   
 (Butterworth  $Q = 0.707$ )

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left( 2 - \frac{1}{Q} \right)}$$

Figure 38. 2-Pole Low-Pass Sallen-Key Filter

## APPLICATION INFORMATION

### circuit layout considerations

To achieve the levels of high performance of the TLV224x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8- $\mu$ F tantalum capacitor in parallel with a 0.1- $\mu$ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- $\mu$ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- $\mu$ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

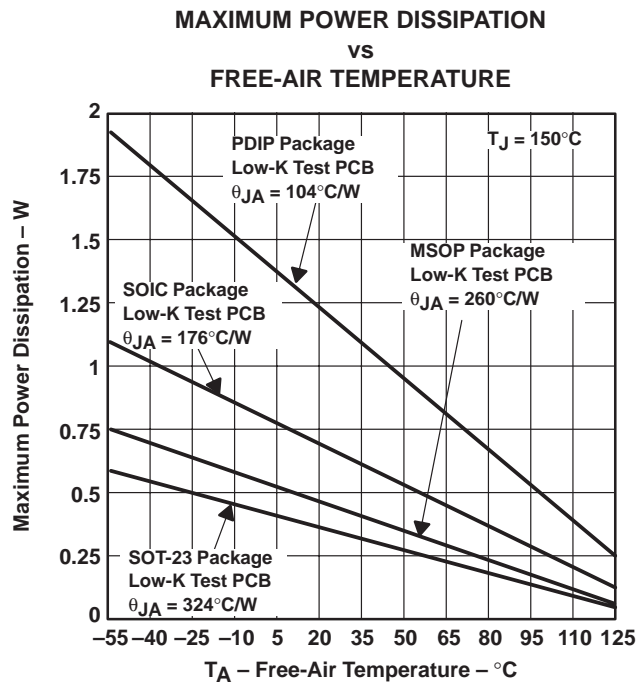
general power dissipation considerations

For a given  $\theta_{JA}$ , the maximum power dissipation is shown in Figure 39 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- $P_D$  = Maximum power dissipation of THS224x IC (watts)
- $T_{MAX}$  = Absolute maximum junction temperature (150°C)
- $T_A$  = Free-ambient air temperature (°C)
- $\theta_{JA}$  =  $\theta_{JC} + \theta_{CA}$
- $\theta_{JC}$  = Thermal coefficient from junction to case
- $\theta_{CA}$  = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 39. Maximum Power Dissipation vs Free-Air Temperature

# TLV2241, TLV2242, TLV2244 FAMILY OF 1- $\mu$ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

SLOS329C – JULY 2000 REVISED - NOVEMBER 2000

## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 40 are generated using the TLV224x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

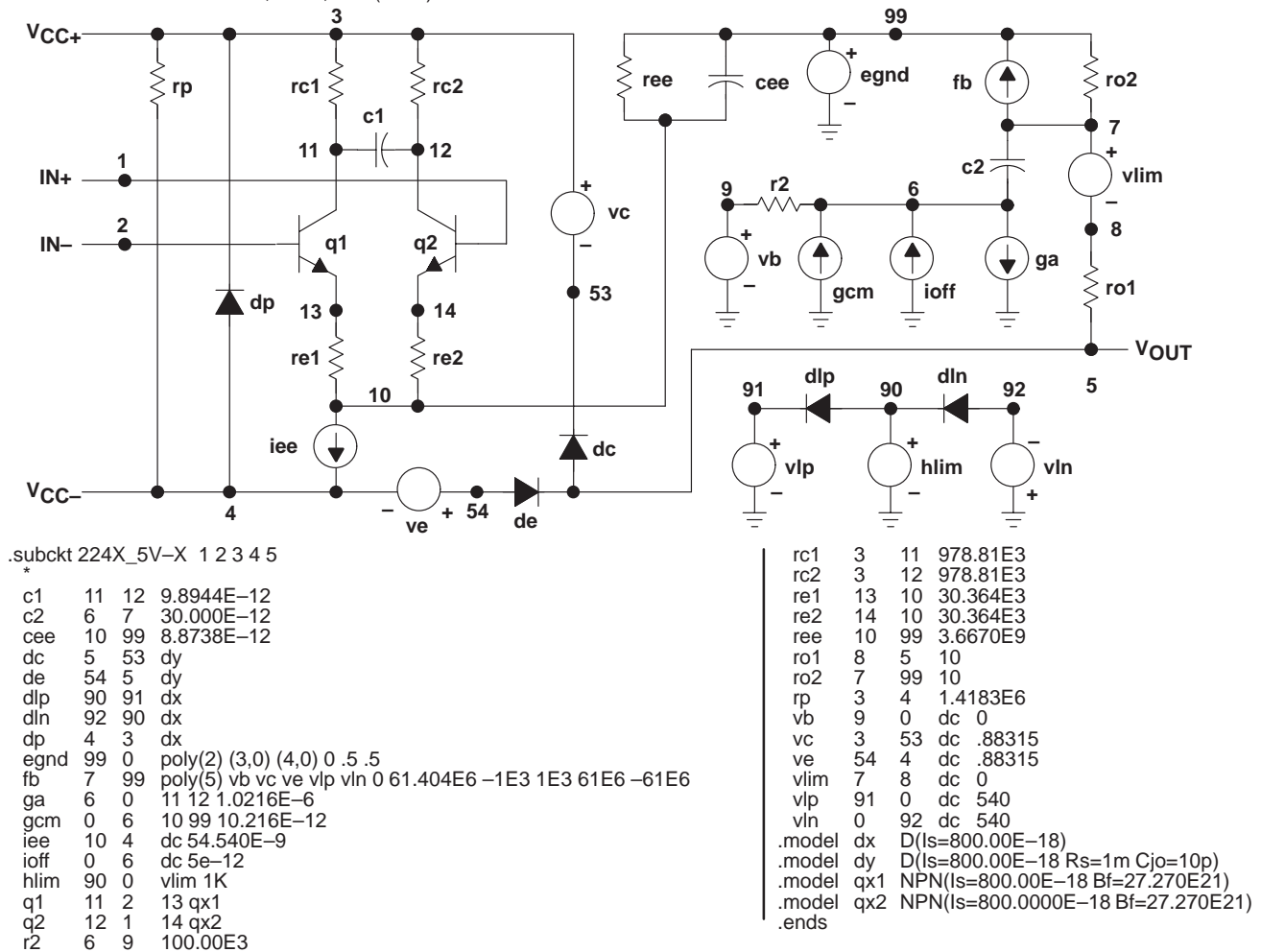


Figure 40. Boyle Macromodels and Subcircuit

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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2241ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	2241I	
TLV2241IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	VBEI	<a href="#">Samples</a>
TLV2241IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	VBEI	<a href="#">Samples</a>
TLV2241IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2241I	<a href="#">Samples</a>
TLV2241IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2241I	<a href="#">Samples</a>
TLV2242CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	<a href="#">Samples</a>
TLV2242CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2242C	<a href="#">Samples</a>
TLV2242ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	<a href="#">Samples</a>
TLV2242IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	<a href="#">Samples</a>
TLV2242IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALE	<a href="#">Samples</a>
TLV2242IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2242IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2242I	<a href="#">Samples</a>
TLV2242IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2242I	<a href="#">Samples</a>
TLV2244ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	<a href="#">Samples</a>
TLV2244IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2244I	<a href="#">Samples</a>
TLV2244IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	<a href="#">Samples</a>
TLV2244IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2244I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2241IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2241IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2242CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2242IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2242IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2244IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2244IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2241IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2241IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2242CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2242IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2242IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2244IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2244IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2241IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2242CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2242CD	D	SOIC	8	75	507	8	3940	4.32
TLV2242ID	D	SOIC	8	75	507	8	3940	4.32
TLV2242ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2242IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2244ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2244IPW	PW	TSSOP	14	90	530	10.2	3600	3.5



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

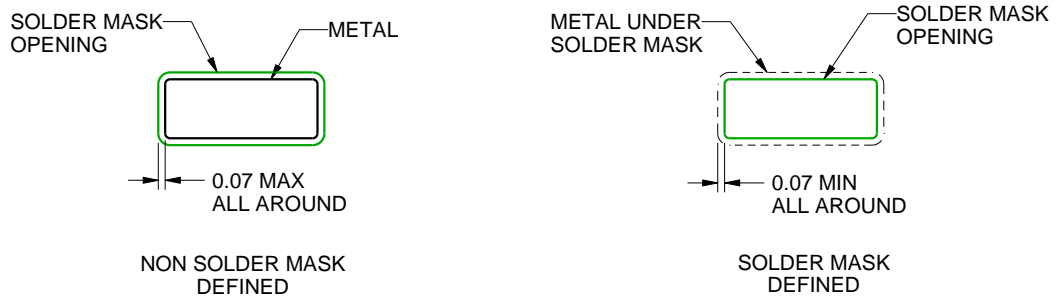
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.





D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

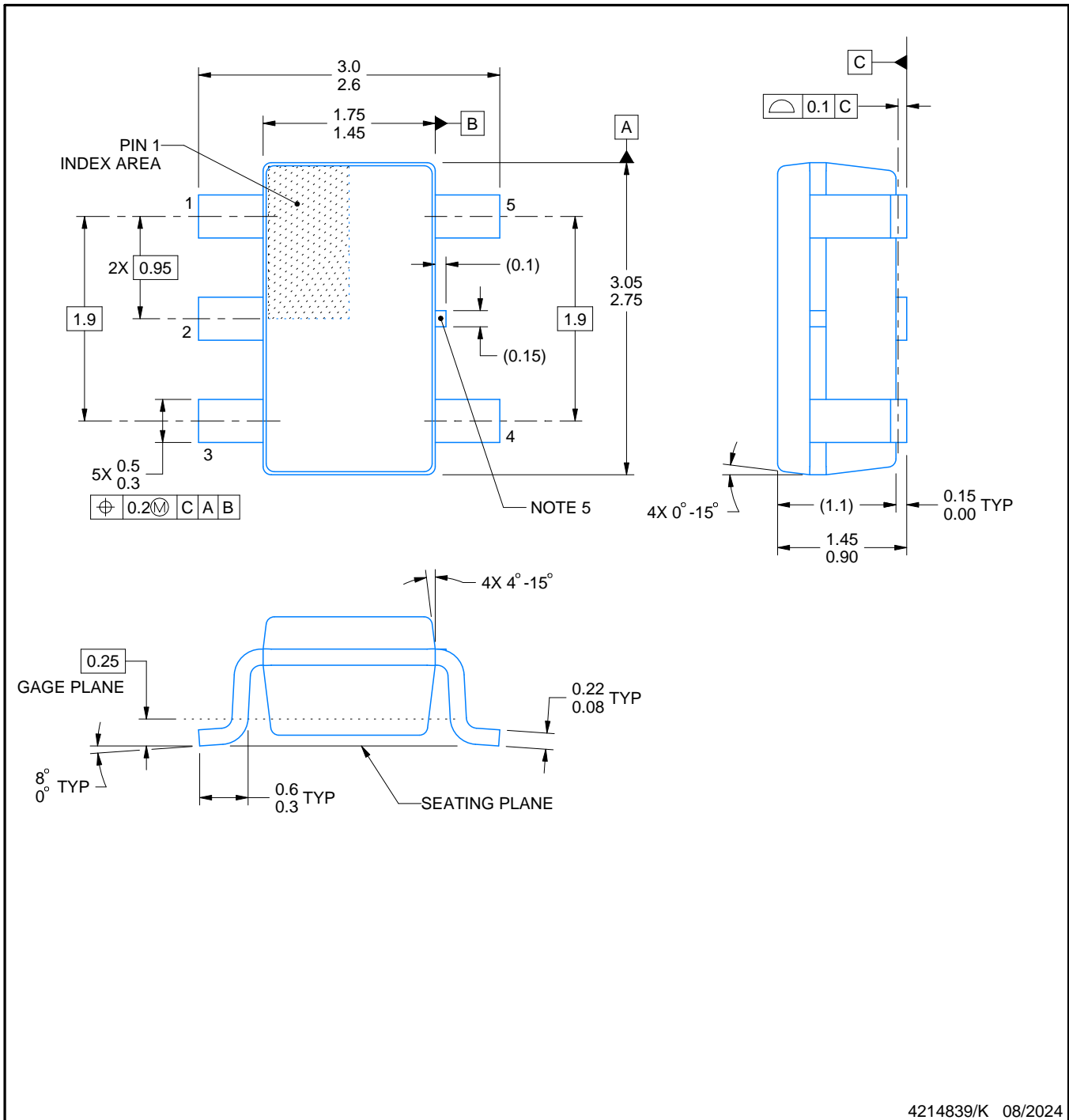
# DBV0005A



# PACKAGE OUTLINE

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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