TLV360x-Q1 具有 2.5ns 传播延迟的 325MHz 高速比较器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C3
- 快速传播延迟：2.5 ns
- 低过驱动分散：600 ps
- 高切换频率：325 MHz
- 窄脉宽检测功能：1.25ns
- 推挽式输出
- 宽电源电压范围：2.4 V 至 5.5 V
- 输入共模范围超出两个电源轨 200 mV
- 低输入失调电压：±5mV
- 输出端已知启动条件
- TLV3603 特定功能：
  - 可调迟滞控制引脚
  - 锁存功能
- 封装：TLV3601 (SC70-5)、(SOT23-5)、TLV3603 (SC70-6)、

  TLV3602 (VSSOP-8)、(WSON-8)
- 提供功能安全
  - 可提供用于功能安全系统设计的文档 [TLV3601/2-Q1]
  - 可帮助进行功能安全系统设计的文档 [TLV3603-Q1]

2 应用

- 直流/直流转换器
- 逆变器和电机控制
- 燃料电池控制单元 (FCCU)
- 电池管理系统 (BMS)
- 机械扫描激光雷达
- 音频放大器

3 说明

TLV360x 是一款 325MHz 高速比较器，具有轨到轨输入和 2.5ns 的传播延迟。这两款比较器可快速响应，并具有宽工作电压范围，非常适合激光雷达、测距仪和线路接收器中的窄信号脉冲检测和数据与时钟恢复应用。

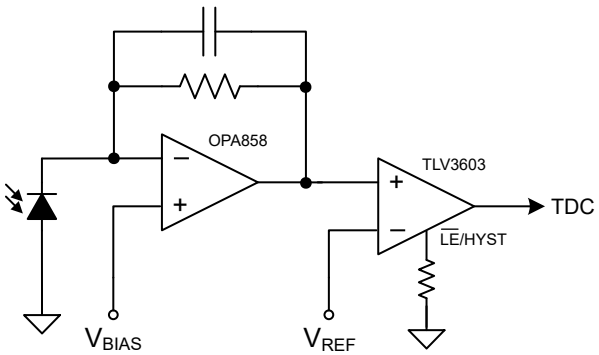
与替代高速差分输出比较器相比，TLV360x 系列的推挽（单端）输出可以简化 I/O 接口的板对板布线并节省相关成本，同时能够降低功耗。它们可以直接连接下游电路中的大多数现行数字控制器和 IO 扩展器。

TLV3601-Q1 采用微型 5 引脚 SC70 和 SOT23 封装，因此非常适合空间受限的设备，这些设备受益于比较器的快速响应时间。TLV3603-Q1 采用 6 引脚 SC70 封装，速度和大小与 TLV3601-Q1 保持相同，同时提供可调迟滞控制和输出锁存功能等附加特性。TLV3602-Q1 是 TLV3601-Q1 的双通道版本，采用 8 引脚 VSSOP 和 WSON 封装。

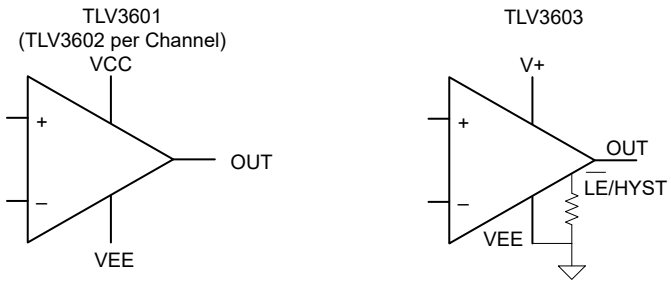
器件信息

器件型号	封装 (1)	封装尺寸（标称值）
TLV3601-Q1	SC70 (5)	1.25mm × 2.00mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV3603-Q1	SC70 (6)	1.25mm × 2.00mm
TLV3602-Q1	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)（预发布）	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



TLV3603 应用电路



功能方框图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (July 2022) to Revision D (August 2022) — **Page**

- 删除了 TLV3602-Q1 VSSOP 封装的“预发布”状态 1

Changes from Revision B (November 2021) to Revision C (July 2022) — **Page**

- 为 TLV3602-Q1 添加了 VSSOP 和 WSON 封装选项 (处于“预发布”状态) 1
- 删除了 TLV3601-Q1 SOT-23 封装的“预发布”状态 1

Changes from Revision A (August 2021) to Revision B (November 2021) — **Page**

- 从 TLV3603-Q1 中删除了“预发布” 1
- 添加了 TLV3601-Q1 的 DBV 封装预发布选项 1
- Added typical performance curves 10

Changes from Revision * (June 2021) to Revision A (August 2021) — **Page**

- 量产数据发布 1

5 Pin Configuration and Functions

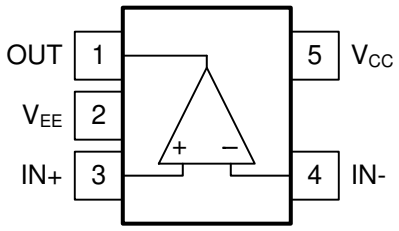


图 5-1. DCK, DBV Package
5-Pin SC70, SOT-23
Top View

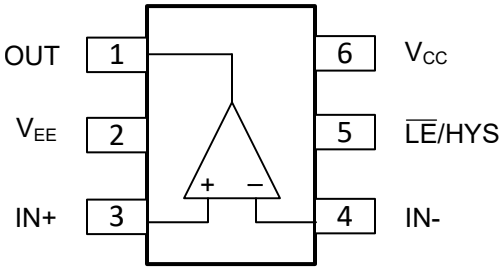


图 5-2. DCK Package
6-Pin SC70
Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	TLV3601	TLV3603		
IN+	3	3	I	Non-inverting input
IN –	4	4	I	Inverting input
OUT	1	1	O	Output (Push-pull)
V_{EE}	2	2	I	Negative power supply
V_{CC}	5	6	I	Positive power supply
$\overline{LE}$/HYS	-	5	I	Adjustable hysteresis control and latch

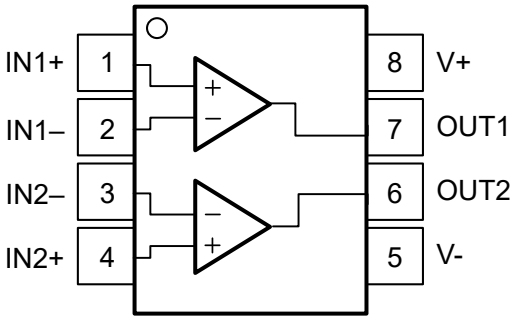


图 5-3. TLV3602 DGK, DSG Packages
8-Pin VSSOP, WSON

表 5-2. Pin Functions: TLV3602 (Dual)

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2 –	3	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	7	O	Output, channel 1
OUT2	6	O	Output, channel 2
V-	5	P	Negative (lowest) supply or ground
V+	8	P	Positive (highest) supply
Thermal PAD		-	Connect directly to V- pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	–0.3	6	V
Input Voltage (IN+, IN–)(2)	V_{EE} – 0.3	V_{CC} + 0.3	V
Differential Input Voltage (V_{DI} = IN+ – IN–)	–(V_{CC} – V_{EE} + 0.3)	+ (V_{CC} – V_{EE} + 0.3)	V
Output Voltage (OUT)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Current into Input pins (IN+, IN–, $\overline{LE}$/HYS)(2)		±10	mA
Current into Output pins (OUT)(3)		±50	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 50 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
TLV3601(DCK), TLV3603				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
TLV3601(DBV)				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	
TLV3602				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	2.4	5.5	V
Input Voltage Range (IN+, IN–)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC		TLV3601 DBV (SOT-23) 5 PINS	TLV3601 DCK (SC70) 5 PINS	TLV3602 DGK (VSSOP) 8 PINS	TLV3602 DSG (WSON) 8 PINS	TLV3603 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.5	187.5	170.5	64.9	165.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.7	139.2	61.7	83.9	129.1	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	5.5	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	65.8	92.4	32.0	58.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	43.0	8.9	2.1	39.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.1	65.5	90.8	32.0	58.7	°C/W

6.5 Electrical Characteristics

V_{CC} = 2.5, 3.3 and 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, C_L = 5 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input offset voltage	T_A = –40°C to +125℃	–5	±0.5	5	mV
dV_{IO}/dT	Input offset voltage drift			±3.0		µV/°C
V_{CM}	Input common mode voltage range	T_A = –40℃ to +125℃	V_{EE} – 0.2		V_{CC} + 0.2	V
V_{HYST} (TLV3601)	Input hysteresis voltage	T_A = –40℃ to +125℃	1.5	3	5(1)	mV
C_{IN}	Input capacitance			1		pF
R_{DM}	Input differential mode resistance			67		kΩ
R_{CM}	Input common mode resistance			5		MΩ
I_B	Input bias current	T_A = –40℃ to +125℃		1	5	uA
I_{OS}	Input offset current			±0.03		uA
CMRR	Common-mode rejection ratio	V_{CM} = V_{EE} – 0.2V to V_{CC} + 0.2V		80		dB
PSRR	Power-supply rejection ratio	V_{CC} = 2.4 to 5.5V		80		dB
DC Output Characteristics						
V_{OH}	Output high voltage from V_{CC}	I_{SOURCE} = 1 mA T_A = –40℃ to +125℃		60	80	mV
V_{OL}	Output low voltage from V_{EE}	I_{SINK} = 1 mA T_A = –40℃ to +125℃		60	80	mV
I_{SC_SOURCE}	Output Short-Circuit Current - Source	T_A = –40℃ to +125℃	10	30		mA
I_{SC_SINK}	Output Short-Circuit Current - Sink	T_A = –40℃ to +125℃	10	30		mA
Power Supply						
I_{CC} (TLV3601)	quiescent current	Output being high T_A = –40℃ to +125℃		4.9	7	mA
I_{CC} (TLV3602)	quiescent current per channel	Output being high T_A = –40℃ to +125℃		4.9	7	mA
I_{CC} (TLV3603)	quiescent current	Output being high T_A = –40℃ to +125℃		5.7	7.8	mA
$V_{POR\ (postive)}$	Power-On Reset Voltage			2.1		V
AC Characteristics						
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV		2.5	3.5(1)	ns
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV T_A = –40℃ to +125℃			4.5(1)	ns
Δt_{PD} (TLV3602 only)	Channel-to-channel propagation delay skew(2)	V_{CM} = V_{CC}/2, $V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		24		ps
$t_{CM\_DISPERSION}$	Common dispersion	V_{CM} varied from V_{EE} to V_{CC}		80		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10 mV to 125 mV		600		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Underdrive varied from 10mV to 125 mV		330		ps
t_R	Rise time	10% to 90%		0.75		ns
t_F	Fall time	90% to 10%		0.75		ns
t_{JITTER}	RMS Jitter	V_{IN} = 100mV$_{P-P}$, f_{IN} = 100MHz, Jitter BW = 10Hz – 50MHz		4		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV$_{PP}$ Sine Wave, When output high reaches 90% of V_{CC} - V_{EE} or output low reaches 10% of V_{CC} - V_{EE}		325		MHz
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		1.25		ns

6.5 Electrical Characteristics (continued)

V_{CC} = 2.5, 3.3 and 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, C_L = 5 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Latching/Adjustable Hysteresis						
V_{HYST}	Input hysteresis voltage	V_{HYST} = Logic High		0		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = Floating		3		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 150 kΩ		30		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 56 kΩ		60		mV
V_{IH_LE}	$\overline{LE}$ pin input high level	T_A = –40℃ to +125℃	V_{EE} + 1.5			V
V_{IL_LE}	$\overline{LE}$ pin input low level	T_A = –40℃ to +125℃			V_{EE} + 0.35	V
I_{IH_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{CC} T_A = –40℃ to +125℃			15	uA
I_{IL_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{EE}, T_A = –40℃ to +125℃			40	uA
t_{SETUP}	Latch setup time			–1.4		ns
t_{HOLD}	Latch hold time			7.2		ns
t_{PL}	Latch to OUT delay			7		ns

(1) Ensured by characterization
(2) Differential propagation delay is defined as the larger of the two:
Δ tPDLH = tPDLH(MAX) – tPDLH(MIN)
Δ tPDHL = tPDHL(MAX) – tPDHL(MIN)
where (MAX) and (MIN) denote the maximum and minimum values of a given measurement across the different comparator channels.

6.6 Timing Diagrams

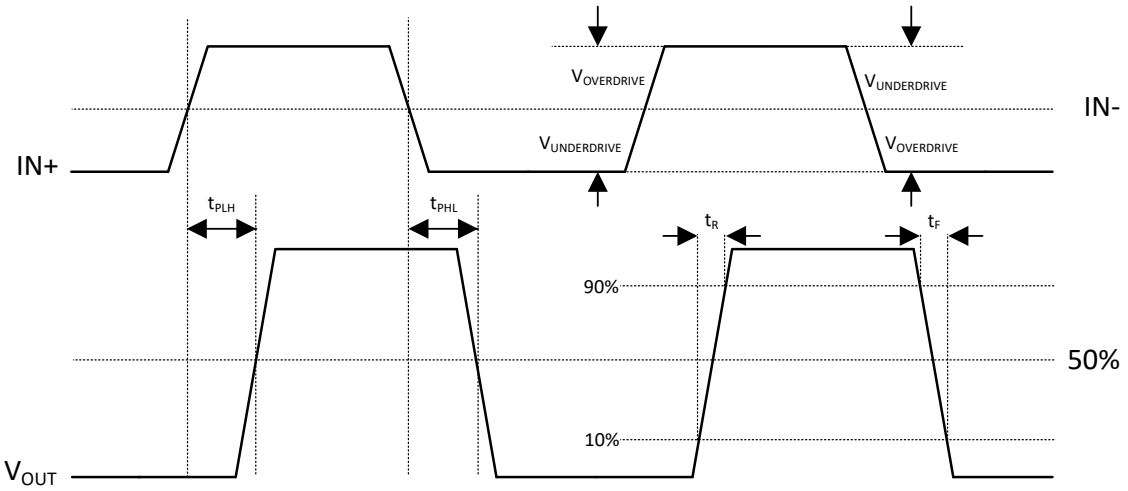


图 6-1. General Timing Diagram

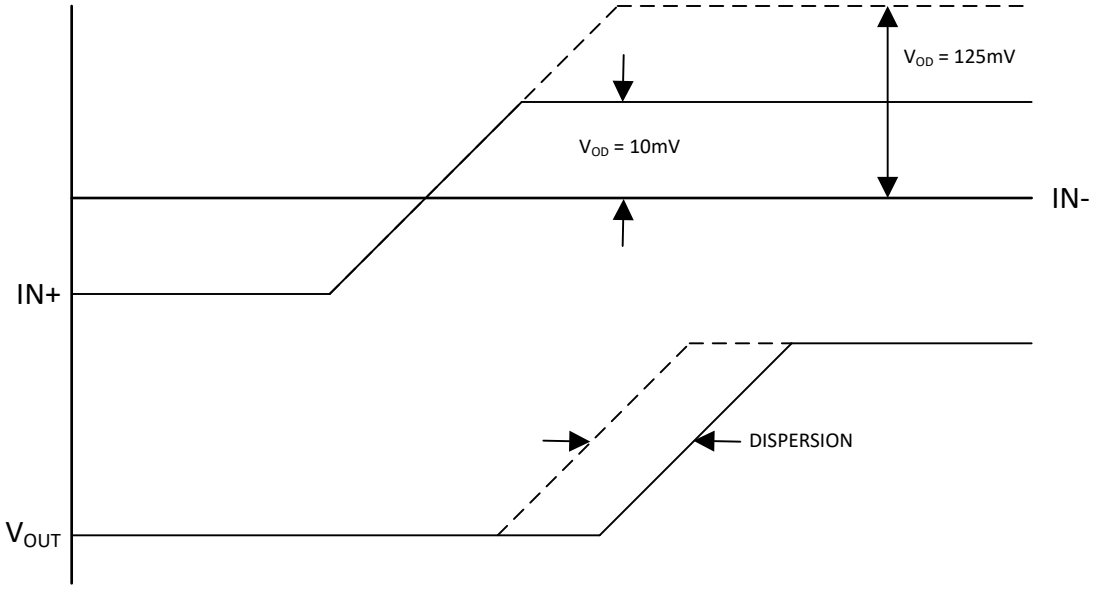


图 6-2. Overdrive Dispersion

6.7 Typical Characteristics

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

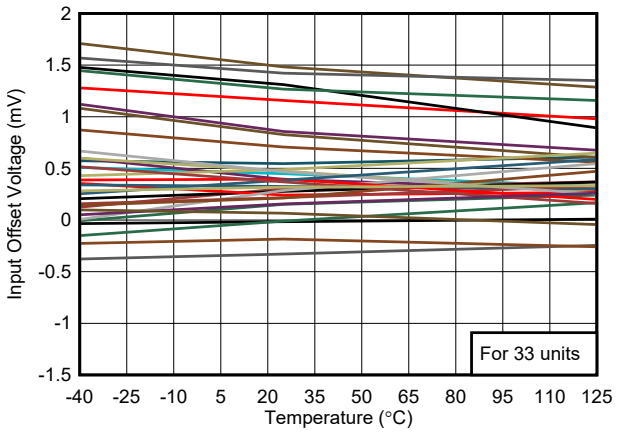


图 6-3. TLV3601 Offset vs. Temperature

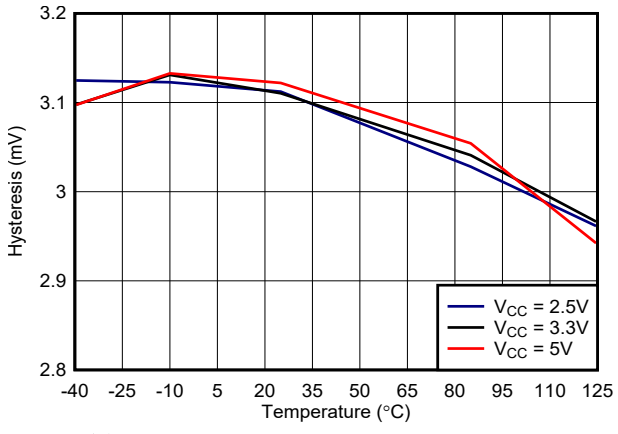


图 6-4. TLV3601 Hysteresis vs. Temperature

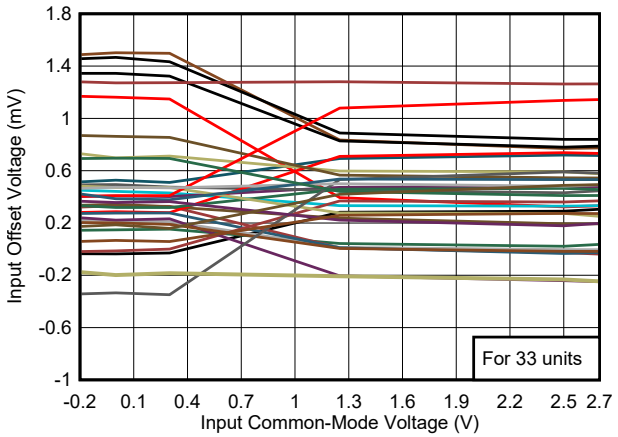


图 6-5. TLV3601 Offset vs. Common-Mode, 2.5 V

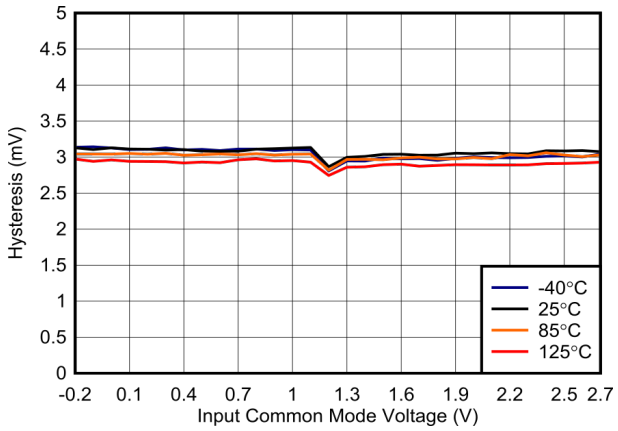


图 6-6. TLV3601 Hysteresis vs. Common-Mode, 2.5 V

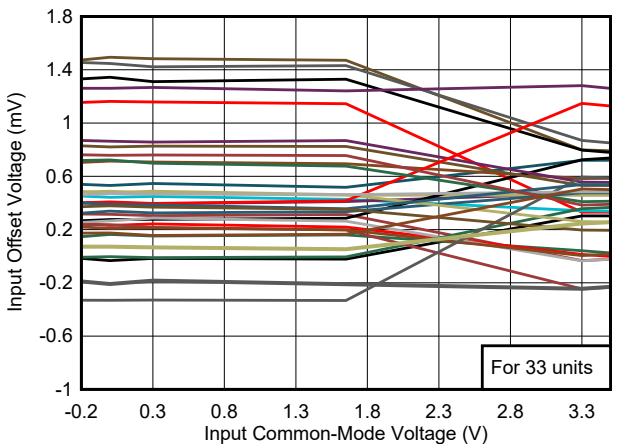


图 6-7. TLV3601 Offset vs. Common-Mode, 3.3 V

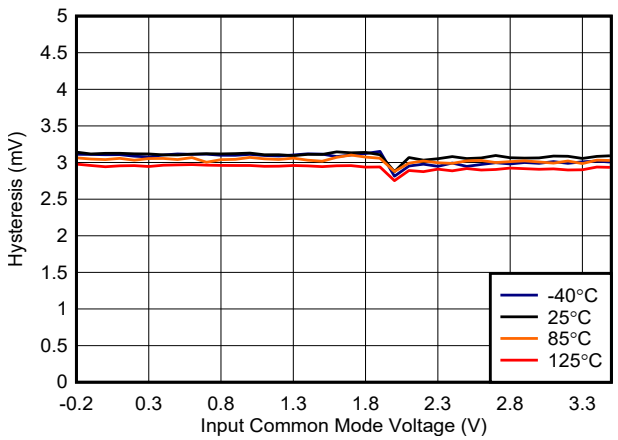


图 6-8. TLV3601 Hysteresis vs. Common-Mode, 3.3 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

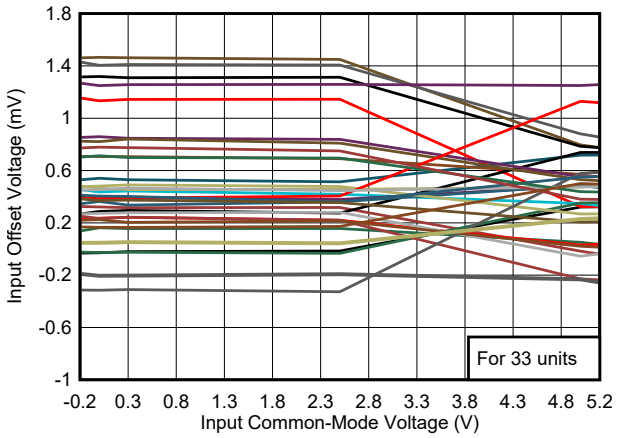


图 6-9. TLV3601 Offset vs. Common-Mode, 5 V

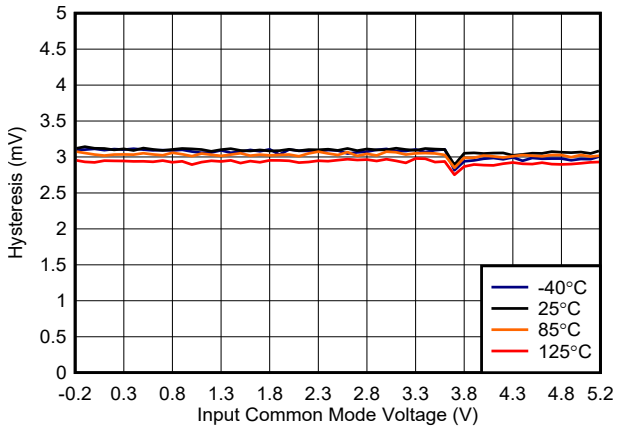


图 6-10. TLV3601 Hysteresis vs. Common-Mode, 5 V

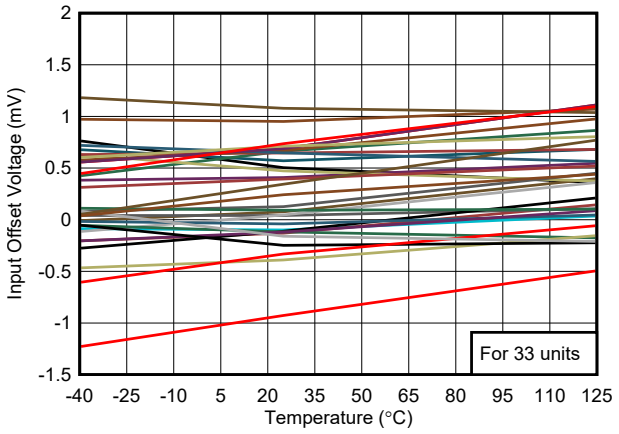


图 6-11. TLV3603 Offset vs. Temperature

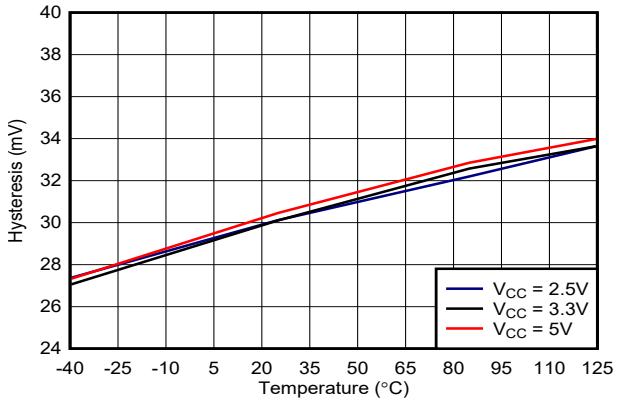


图 6-12. TLV3603 Hysteresis vs. Temperature

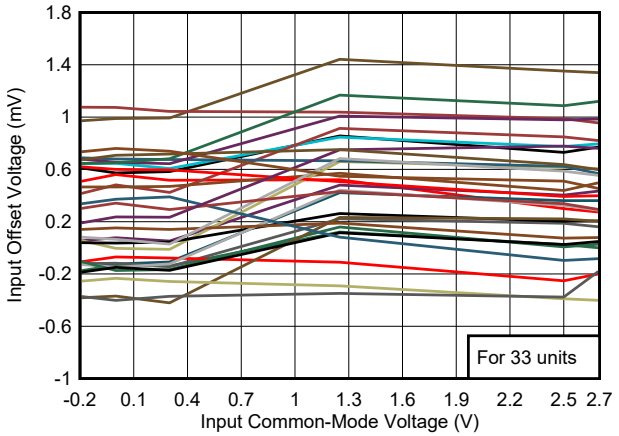


图 6-13. TLV3603 Offset vs. Common-Mode, 2.5 V

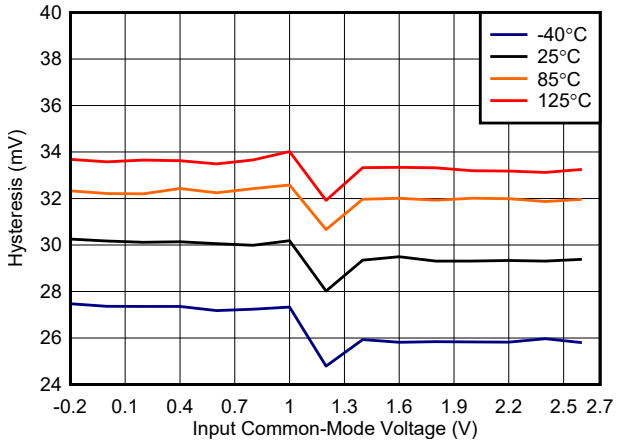


图 6-14. TLV3603 Hysteresis vs. Common-Mode, 2.5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

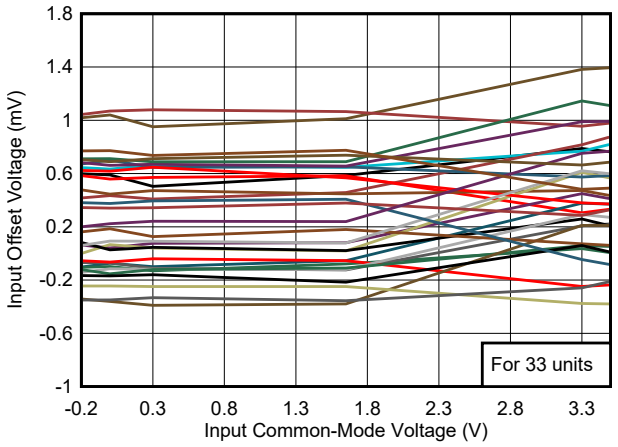


图 6-15. TLV3603 Offset vs. Common-Mode, 3.3 V

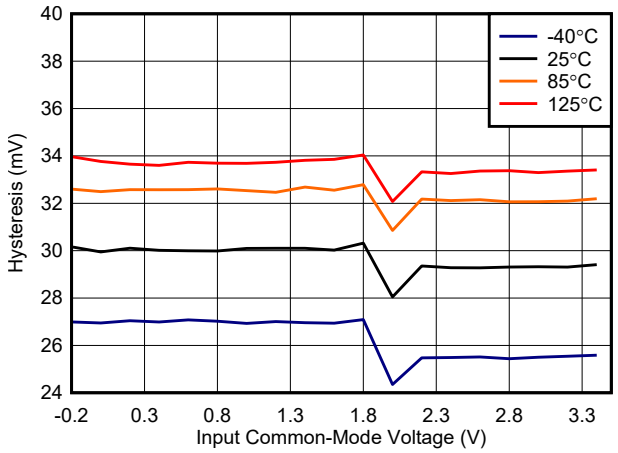


图 6-16. TLV3603 Hysteresis vs. Common-Mode, 3.3 V

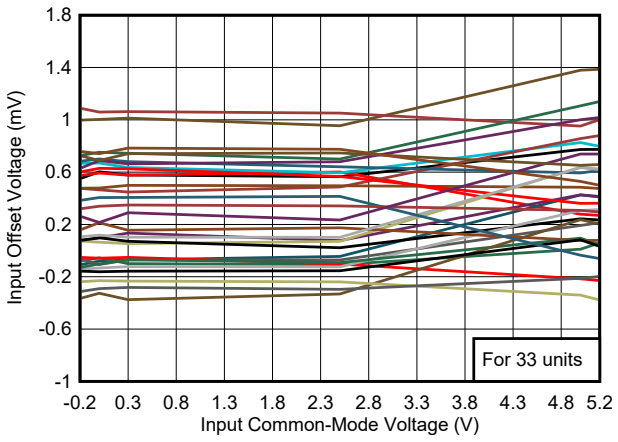


图 6-17. TLV3603 Offset vs. Common-Mode, 5 V

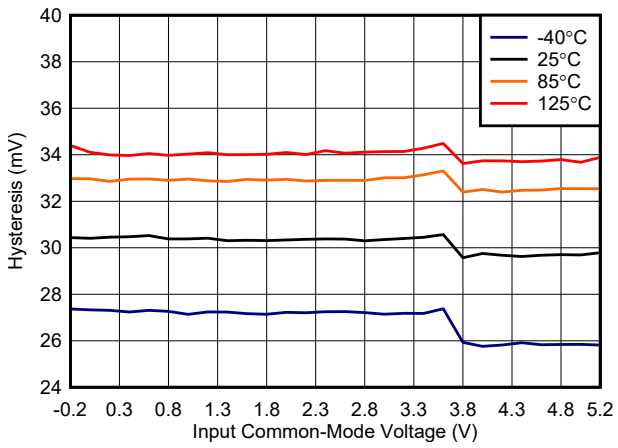


图 6-18. TLV3603 Hysteresis vs. Common-Mode, 5 V

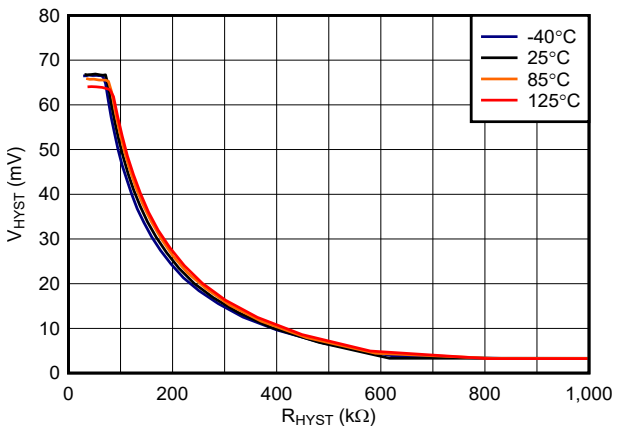


图 6-19. TLV3603 Hysteresis vs. Resistance, 2.5 V

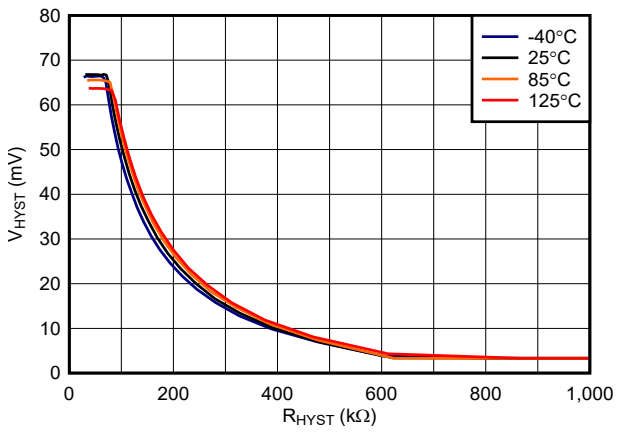


图 6-20. TLV3603 Hysteresis vs. Resistance, 3.3 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

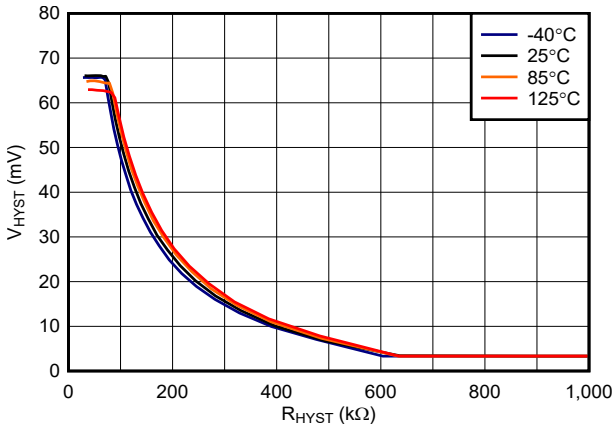


图 6-21. TLV3603 Hysteresis vs. Resistance, 5 V

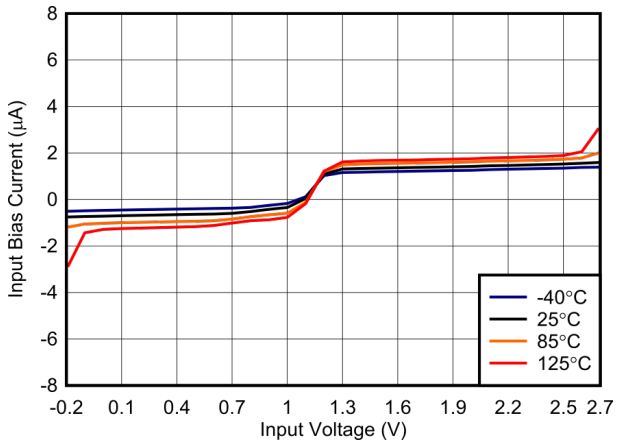


图 6-22. Bias Current vs. Input Voltage, 2.5 V

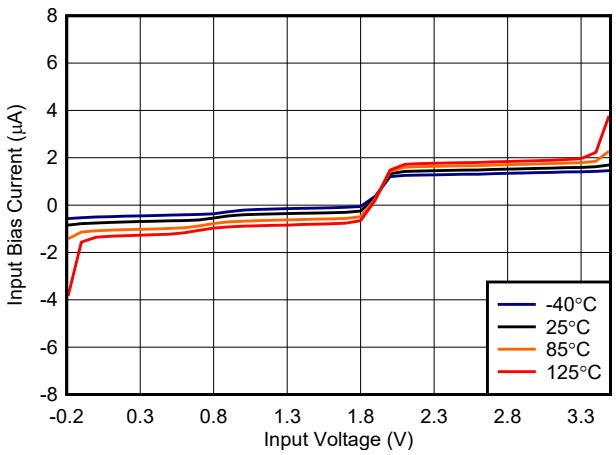


图 6-23. Bias Current vs. Input Voltage, 3.3 V

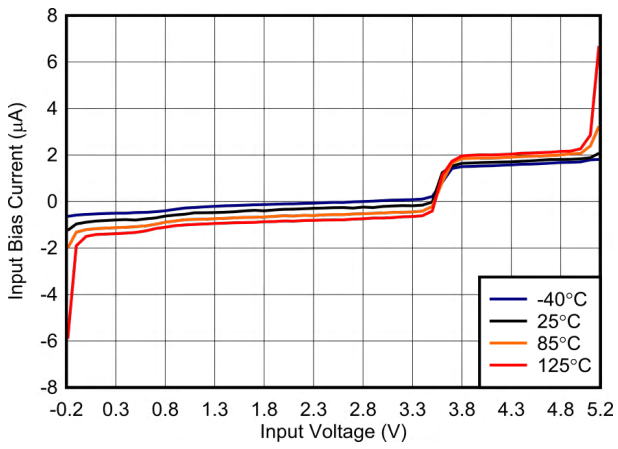


图 6-24. Bias Current vs. Input Voltage, 5 V

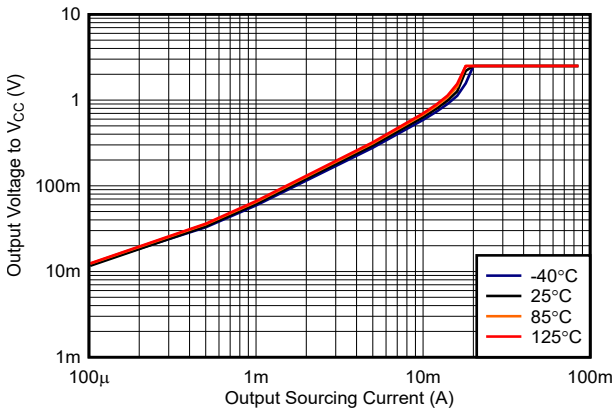


图 6-25. Output Voltage vs. Output Sourcing Current, 2.5 V

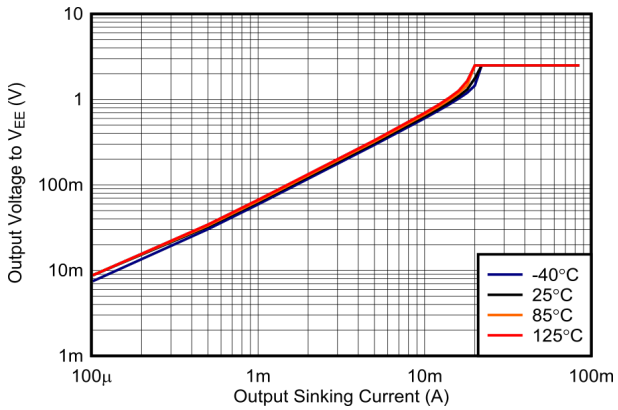


图 6-26. Output Voltage vs. Output Sinking Current, 2.5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

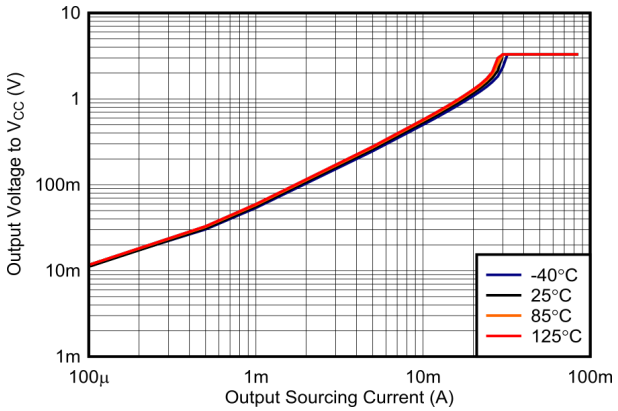


图 6-27. Output Voltage vs. Output Sourcing Current, 3.3 V

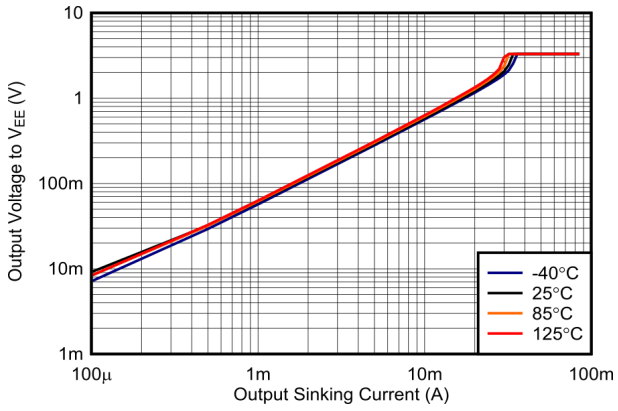


图 6-28. Output Voltage vs. Output Sinking Current, 3.3 V

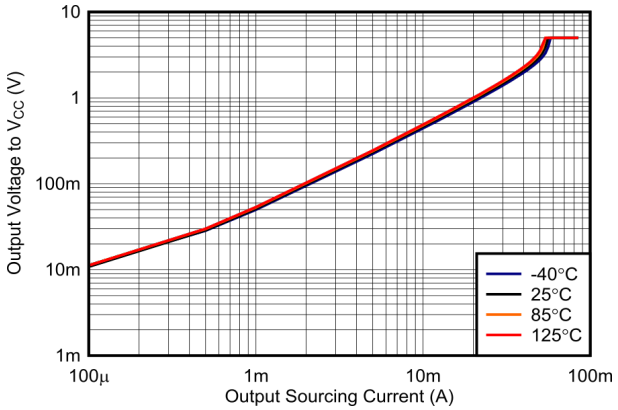


图 6-29. Output Voltage vs. Output Sourcing Current, 5 V

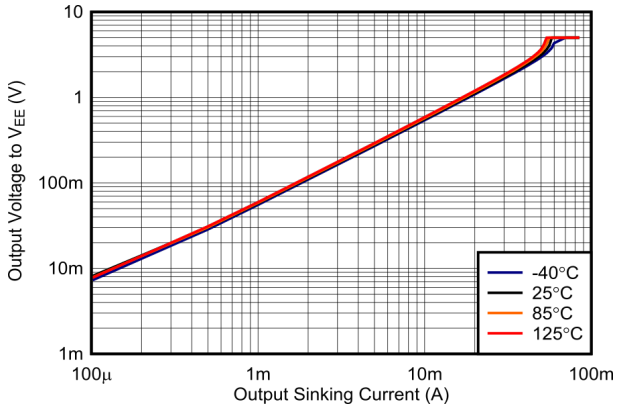


图 6-30. Output Voltage vs. Output Sinking Current, 5 V

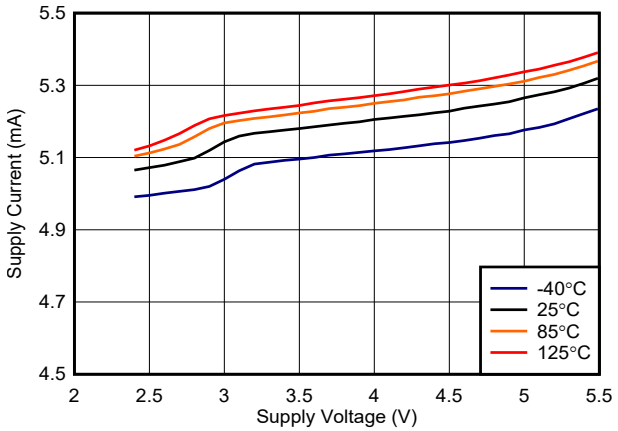


图 6-31. TLV3601 Supply Current vs. Voltage (Output Low)

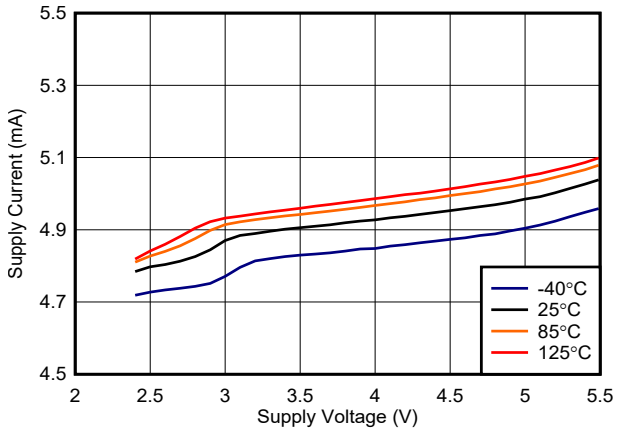


图 6-32. TLV3601 Supply Current vs. Voltage (Output High)

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

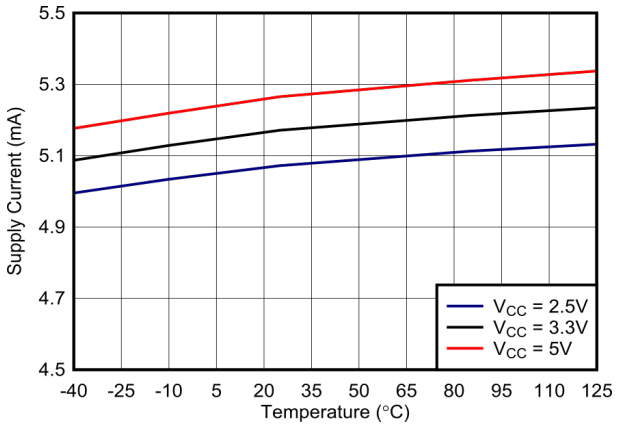


图 6-33. TLV3601 Supply Current vs. Temp (Output Low)

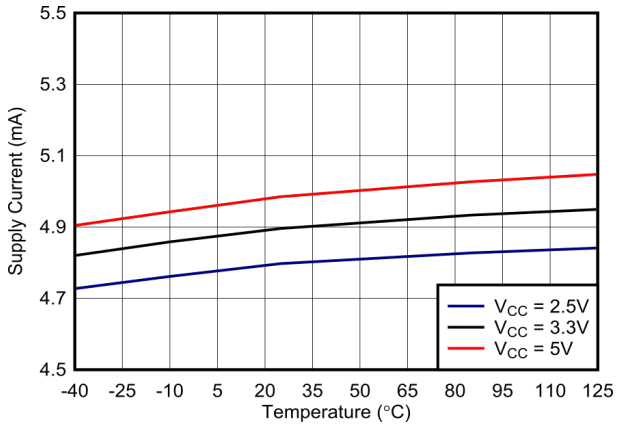


图 6-34. TLV3601 Supply Current vs. Temp (Output High)

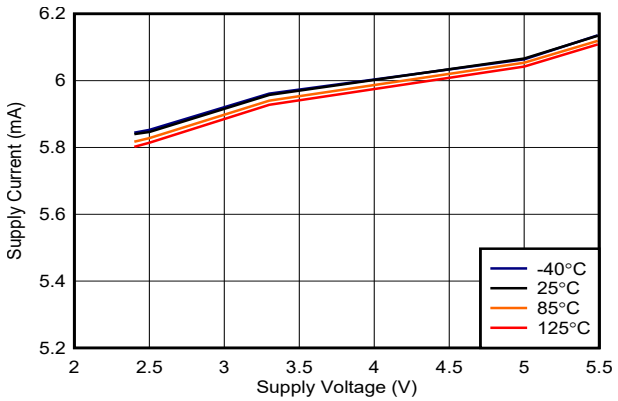


图 6-35. TLV3603 Supply Current vs. Voltage (Output Low)

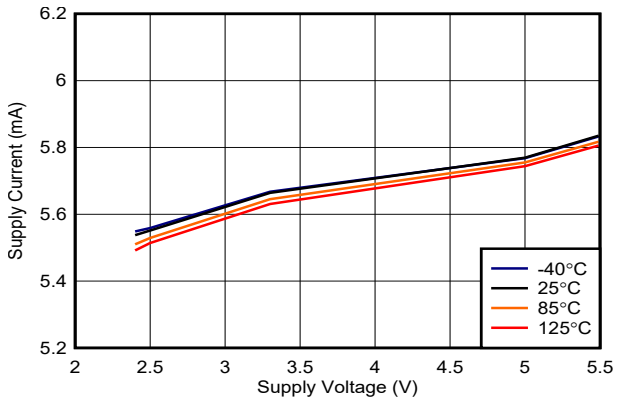


图 6-36. TLV3603 Supply Current vs. Voltage (Output High)

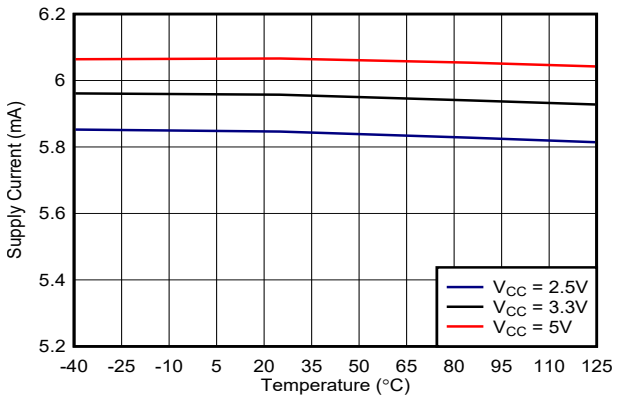


图 6-37. TLV3603 Supply Current vs. Temp (Output Low)

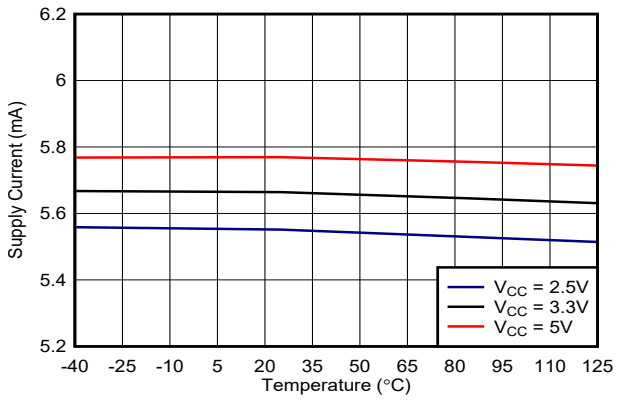


图 6-38. TLV3603 Supply Current vs. Temp (Output High)

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

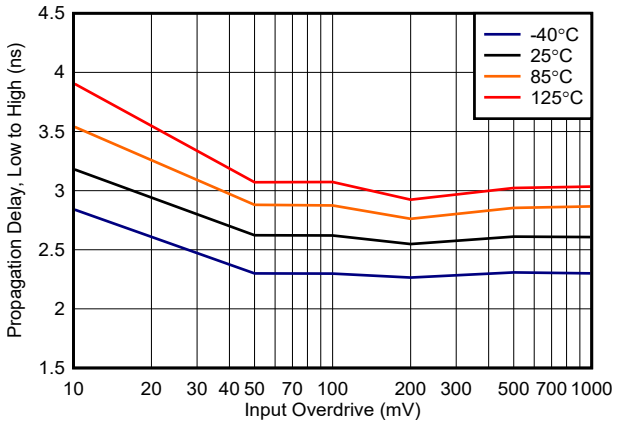


图 6-39. Propagation Delay, Low to High, 2.5 V

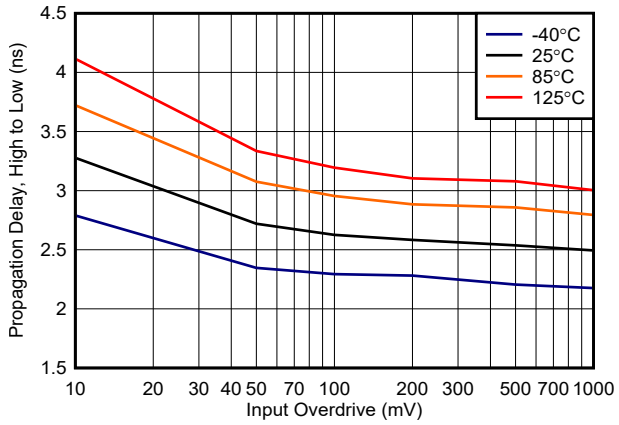


图 6-40. Propagation Delay, High to Low, 2.5 V

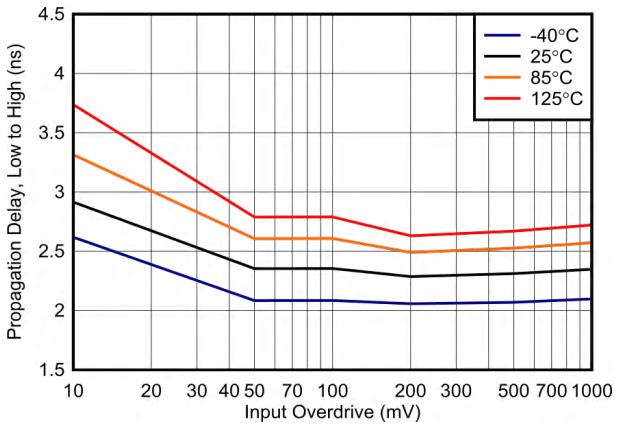


图 6-41. Propagation Delay, Low to High, 3.3 V

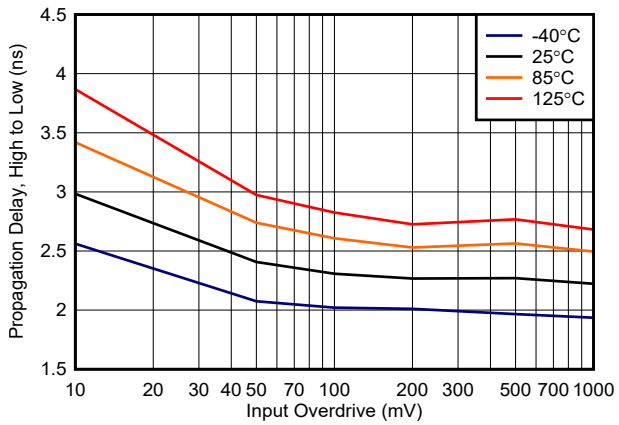


图 6-42. Propagation Delay, High to Low, 3.3 V

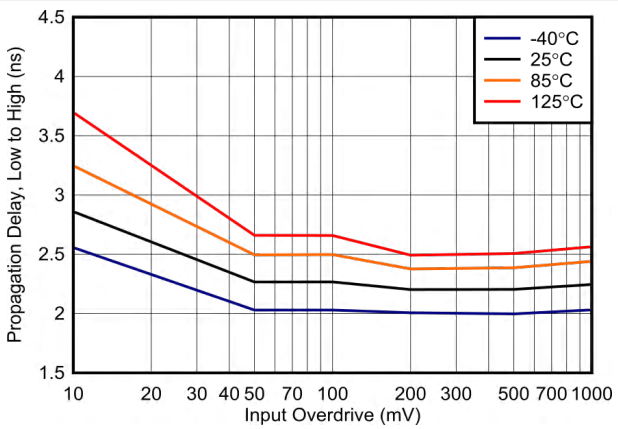


图 6-43. Propagation Delay, Low to High, 5 V

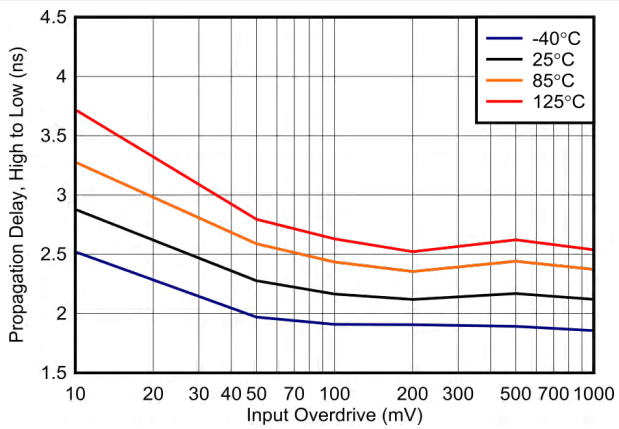


图 6-44. Propagation Delay, High to Low, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5 V to 5 V, V_{CM} = 300 mV, R_{HYST} = 150 kΩ (TLV3603-Q1 only), and input overdrive = 50 mV, unless otherwise noted.

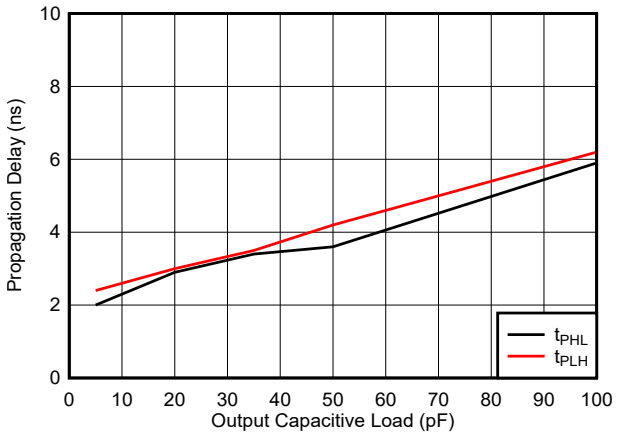


图 6-45. Propagation Delay vs. Load Capacitance, 3.3 V

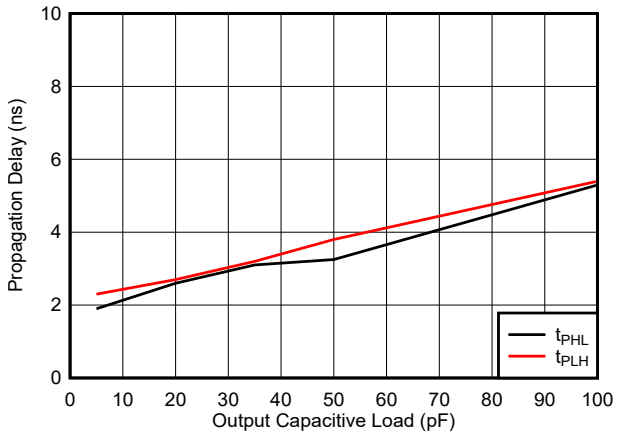


图 6-46. Propagation Delay vs. Load Capacitance, 5 V

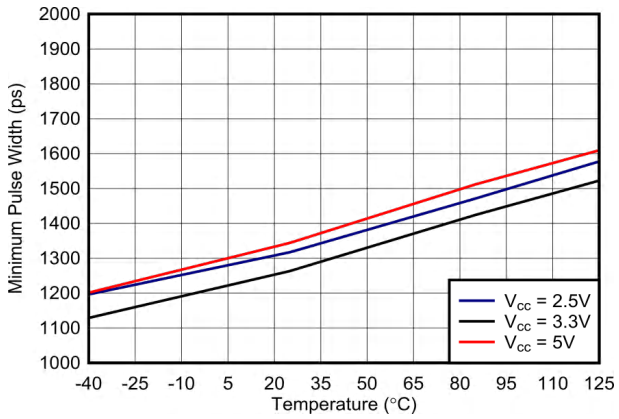


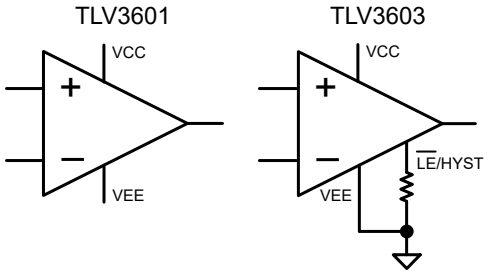
图 6-47. Minimum Pulse Width vs. Temperature

7 Detailed Description

7.1 Overview

TheTLV360x family are high-speed comparators with single-ended (push-pull) output stages. The fast response time of these comparators make them well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV3601-Q1 is available in a 5-pin SC70 and SOT23 package, while the TLV3603-Q1 is packaged in a 6-pin SC70. The TLV3602-Q1 is a dual channel version of the TLV3601-Q1 and is packaged in an 8-pin VSSOP and WSON package.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV3601-Q1,TLV3603-Q1, and TLV3602-Q1 are single and dual channel, high speed comparators with a typical propagation delay of 2.5 ns and push-pull outputs. The minimum pulse width detection capability is 1.25 ns and the typical toggle rate is 325 MHz. These comparators are well-suited for distance measurement applications that utilize a time-of-flight arechitecture as well as systems that suffer from capacitive loading and require data and clock recovery. In addition to their high speed, the TLV360x family offers rail-to-rail input stages capable of operating up to 200 mV beyond each power supply rail combined with a maximum 5 mV input offset. The TLV3603-Q1 also provides adjustable hysteresis via an external resistor for noise suppression or a latching mode to hold the output of the comparators.

7.4 Device Functional Modes

The TLV3601-Q1 has a single functional mode and is active when the power supply voltage is greater than 2.4V. The TLV3603-Q1 has two modes of operation. The first is an active mode where the output reflects the condition at the inputs when an external resistor is connected to ground on the $\overline{LE}$/HYS pin. The second is a latch mode where the output is held at its last active state when the $\overline{LE}$/HYS pin is pulled low. The TLV3603-Q1 returns to active mode after a short delay when the pin is pulled high.

7.4.1 Inputs

The TLV360x family features input stages capable of operating 200 mV below negative power supply (ground) and 200 mV beyond the positive supply voltage, allowing for zero cross detection and maximizing input dynamic range given a certain power supply. The input stages are protected from conditions where the voltage on either pin exceeds this level by internal ESD protection diodes to VCC and VEE. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor should be used to limit the current.

7.4.2 Push-Pull (Single-Ended) Output

The TLV360x outputs have excellent drive capability and are designed to connect directly to CMOS logic input devices. Likewise, the comparator output stages can drive capacitive loads. Transient performance parameters in the Electrical Characteristics Tables and Typical Characteristics section are for a load of 5pF, corresponding to a standard CMOS load. Device performance for larger capacitive loads can be found in the typical performance curves titled Propagation Delay vs Capacitive Load. For optimal speed and performance, output load capacitance should be reduced as much as possible.

7.4.3 Known Startup Condition

The TLV360x have a Power-on-Reset (POR) circuit which provides system designers a known start-up condition for the output of the comparators. When the power supply (VCC) is ramping up or ramping down, the POR circuit will be active when VCC is below V_{POR}. When active, the POR circuit holds the output low at VEE. When VCC is greater than or equal to V_{POR} as stated in 节 6.5 , the comparator output reflects the state of the input pins.

图 7-1 shows how the TLV360x outputs respond for VCC rising. The input is configured with a logic high input to highlight the transition from the POR circuit control (logic low output) to a standard comparator operation where the output reflects the input condition. Note how the output goes high when VCC reaches 2.1V.

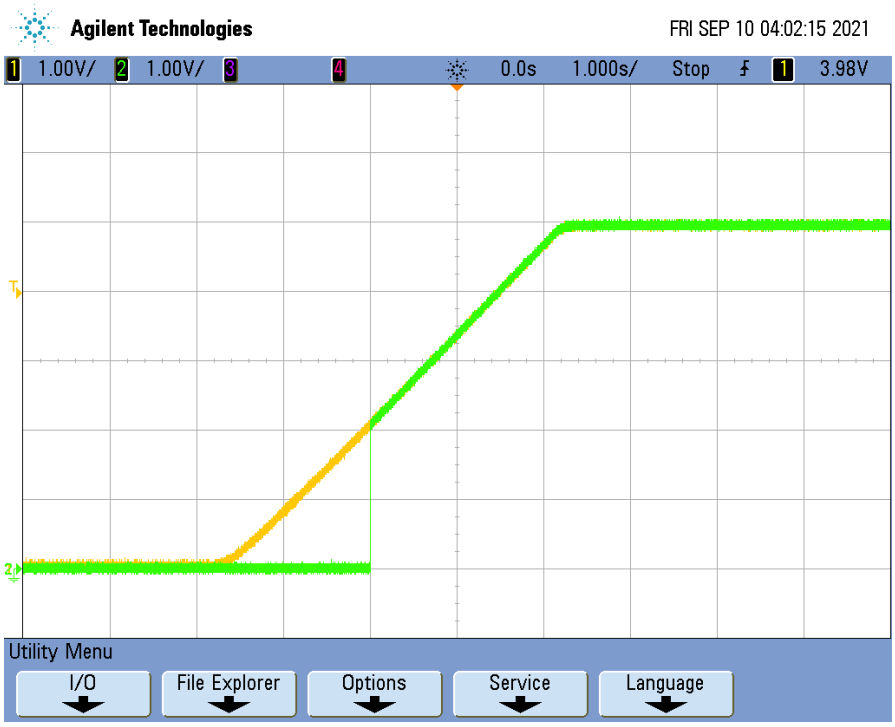


图 7-1. TLV3601/TLV3603 Output for VCC Rising

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Hysteresis

As a result of a comparator’s high open loop gain, there is a small band of input differential voltage where the output can toggle back and forth between “logic high” and “logic low” states. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be overcome by adding hysteresis to the comparator.

Since the TLV3601-Q1 and TLV3602-Q1 only has a minimal amount of internal hysteresis, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. See the Implementing Hysteresis section for more details.

The TLV3603-Q1 on the other hand has a $\overline{LE}$/HYS pin that can be used to increase or eliminate the internal hysteresis of the comparator. In order to increase the internal hysteresis of the TLV3603-Q1, connect a single resistor as shown in the adjusting hysteresis figure between the $\overline{LE}$/HYS pin and VEE. A curve of hysteresis versus resistance is provided below to provide guidance in setting the desired amount of hysteresis. Likewise, for applications where no hysteresis is desired, the $\overline{LE}$/HYS pin can be connected to VCC.

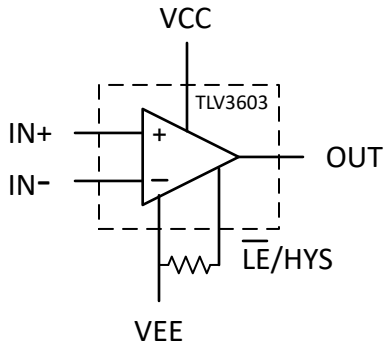


图 8-1. Adjustable Hysteresis with an External Resistor

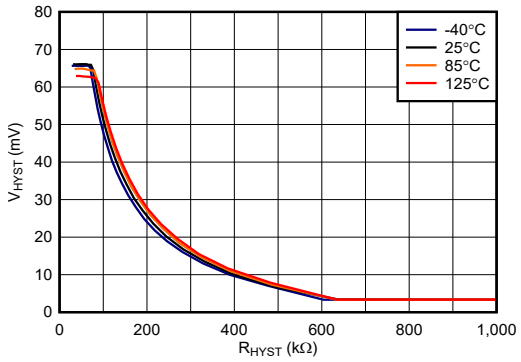


图 8-2. V_{HYST} (mV) vs R_{HYST} (kΩ), V_{CC} = 5 V

8.1.2 Capacitive Loads

For capacitive loads under 100 pF, the propagation delay has minimum change (see Propagation Delay vs. Capacitive Load). However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.1.3 Latch Functionality

The latch pin for the TLV3603-Q1 holds the output state of the device when the voltage at the $\overline{LE}$/HYS pin is a logic low. This is particularly useful when the output state is intended to remain unchanged. An important consideration of the latch functionality is the latch hold and setup times. Latch hold time is the minimum time required (after the latch pin is asserted) for properly latching the comparator output. Likewise, latch setup time is defined as the time that the input must be stable before the latch pin is asserted low. The figure below illustrates when the input can transition for a valid latch. Note that the typical setup time in the EC table is negative; this is due to the internal trace delays of the $\overline{LE}$/HYS pin relative to the input pin trace delays. A small delay (t_{PL}) in the output response is shown below when the TLV3603-Q1 exits a latched output stage.

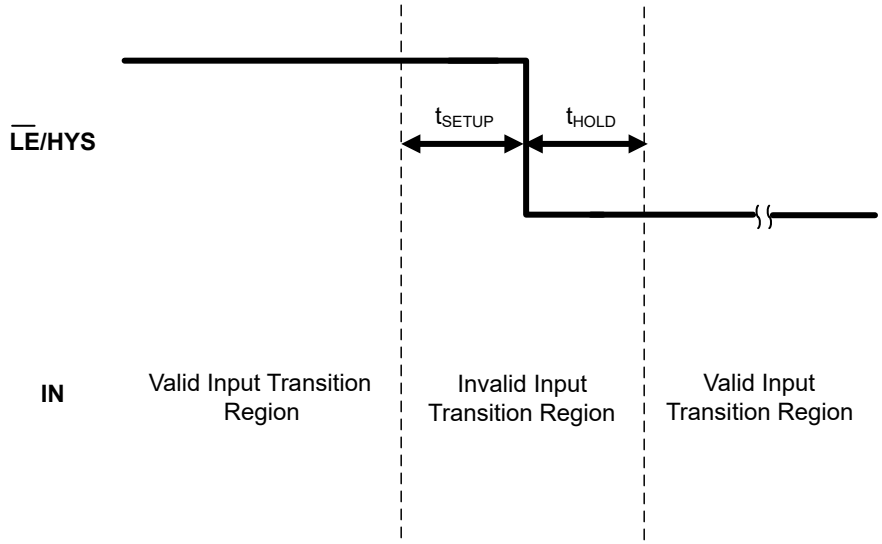


图 8-3. Input Change Properly Latched

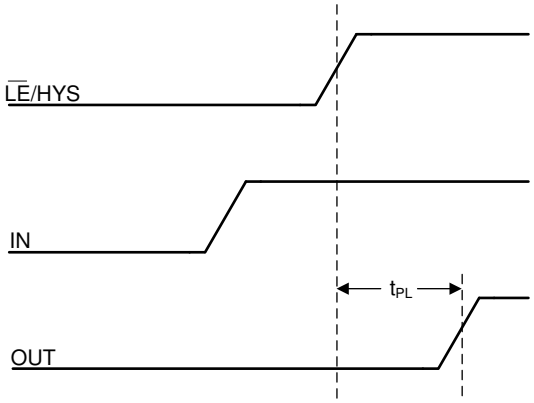


图 8-4. Latch Disable with Input Change

8.2 Typical Application

8.2.1 Implementing Hysteresis

A comparator may produce “chatter” (multiple transitions) at the output when there are noise or signal variations around the reference threshold; this causes the output to change states in rapid random successions

as the comparator input goes above and below the threshold of the reference. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by using the internal hysteresis feature of the comparator or by the addition of external hysteresis.

The TLV3603-Q1 has a $\overline{LE}$/HYS pin that allows for variable internal hysteresis depending on the resistor value connected between the pin and VEE, where increasing the resistance decreases the hysteresis to a minimum level.

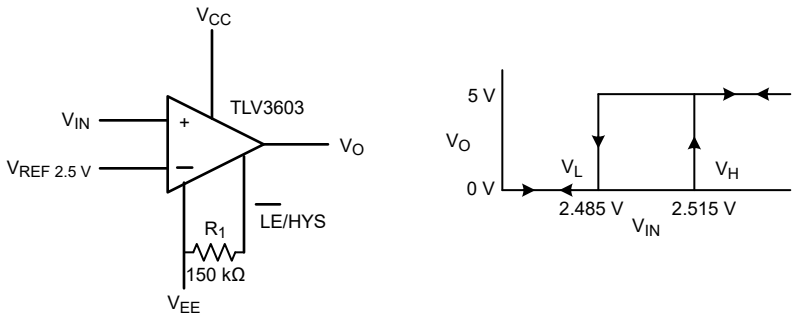


图 8-5. Adjustable Hysteresis with a 150kΩ Resistor using TLV3603

Since the TLV3601-Q1 and TLV3602-Q1 only have a minimal amount of internal hysteresis, external hysteresis can be added in the form of a positive feedback loop. A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 8-6.

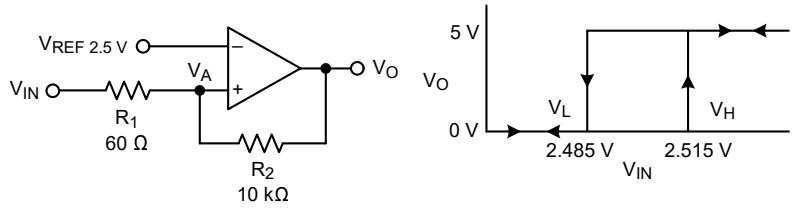


图 8-6. Non-Inverting Configuration for Hysteresis using TLV3601

8.2.1.1 Design Requirements

For this design, follow these design requirements.

表 8-1. Design Parameters

PARAMETER	VALUE
Supply Voltage (V_{CC})	5 V
V_{REF}	2.5 V
V_{HYS}	30 mV
Lower Threshold (V_L)	2.485 V
Upper Threshold (V_H)	2.515 V

8.2.1.2 Detailed Design Procedure

For the TLV3603-Q1, the hysteresis vs. resistance curve (Figure 8-2) can be used as a guidance to set the desired amount of hysteresis. Figure 8-2 shows that for a 30-mV hysteresis, a 150 kΩ resistor must be placed from the $\overline{LE}$/HYS pin to VEE.

For the TLV3601-Q1 and TLV3602-Q1, the following procedure can be used to add external hysteresis for a non-inverting configuration. Note that $V_{HYST} << V_{REF}$, so V_{HYST} can be ignored and is not included in the following equations for simpler calculation.

The equivalent resistor networks when the output is high and low are shown in Figure 8-7.

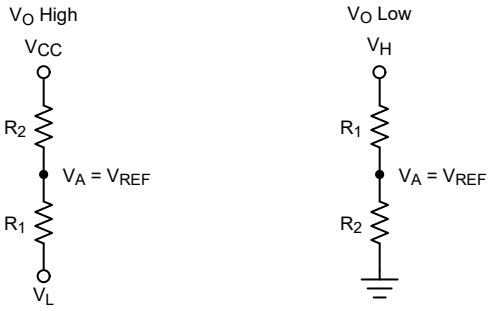


图 8-7. Equivalent Resistor Networks for Non-Inverting Configuration with Hysteresis

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_H threshold. Use Equation 1 to calculate V_H.

$$V_H = (R1 \times V_{REF}/R2) + V_{REF} \quad (1)$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below the V_L threshold. Use Equation 2 to calculate V_L.

$$V_L = [V_{REF} (R1 + R2) - V_{CC} \times R1] / R2 \quad (2)$$

The hysteresis of this circuit is the difference between V_H and V_L, as shown in Equation 3.

$$\Delta V_{IN} = V_{HYS} = (V_{CC} \times R1/R2) \quad (3)$$

Select a value for R2. Plug in given values for V_{CC}, V_{REF}, V_H, and V_L . For the given example, R2 = 10 kΩ, and R1 is solved as 60 Ω.

For more information, please see Application Notes SNOA997 "Inverting Comparator with Hysteresis Circuit", SBOA313 "Non-Inverting Comparator With Hysteresis Circuit", SBOA219 "Comparator with and without hysteresis circuit".

8.2.1.3 Application Curve

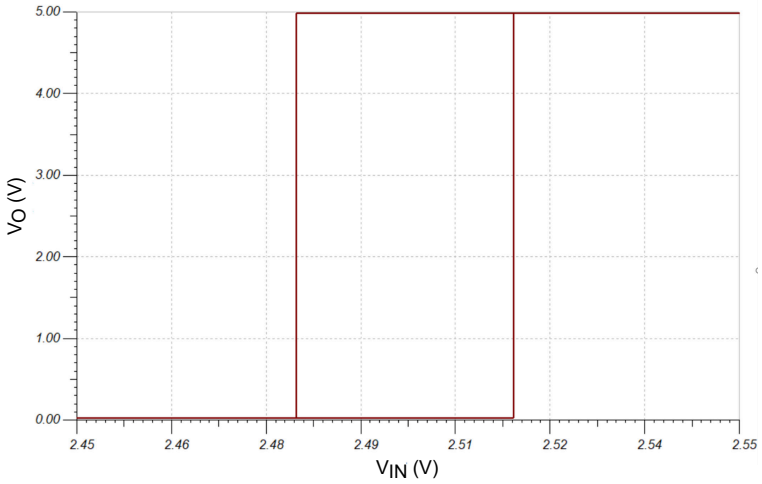


图 8-8. Hysteresis Transfer Curve using TLV3601/TLV3603

8.2.2 Optical Receiver

The TLV360x can be used in conjunction with a high speed amplifier such as the OPA858 to create an optical receiver as shown in the figure below. The photodiode is connected to a bias voltage and is being driven with a pulsed laser. The OPA858 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The comparators will then output the proper output signal according to the threshold set (V_{REF}).

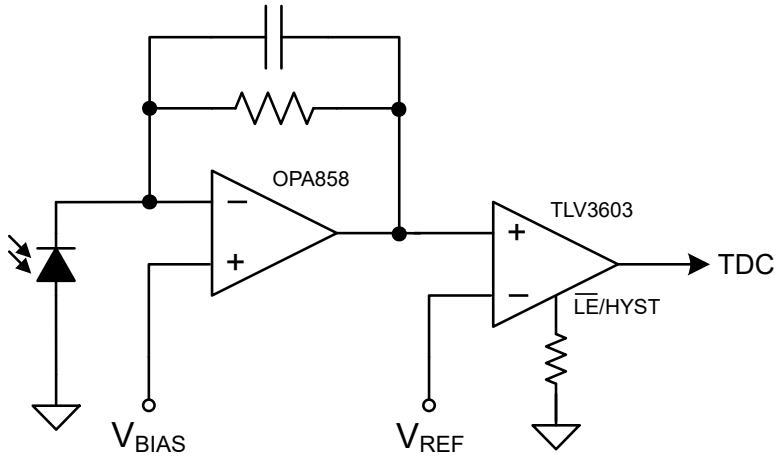


图 8-9. Optical Receiver

8.2.3 Over-Current Latch Condition

When it is important for a system to detect a brief over-current condition, it is advisable to utilize the latching feature of the TLV3603-Q1. By latching the comparator output, the MCU is reassured not to miss the over-current occurrence. The circuit below shows one way to implement the latching function.

When an over-current condition is detected by the TLV3603-Q1, the output will go high. The occurrence of the output going high coupled with a logic high from the $\overline{\text{RESET}}$ signal from the MCU will create a logic low signal at the output of the 2-channel NAND gate. This will cause the output of the TLV3603-Q1 to be held in a logic high state (latched), thus allowing the MCU to detect the fault condition regardless of how narrow the over-current condition persists. The addition of the NAND gate also provides a means of clearing the latch state of the comparator once the MCU is done processing the event. This is accomplished by the MCU passing a logic low state to the NAND input causing the $\overline{\text{LE}}$/HYS pin of the comparator to be returned to a logic high state. The TLV3603-Q1 latched status is cleared and the TLV3603-Q1 output can continue to track the status of the input pins.

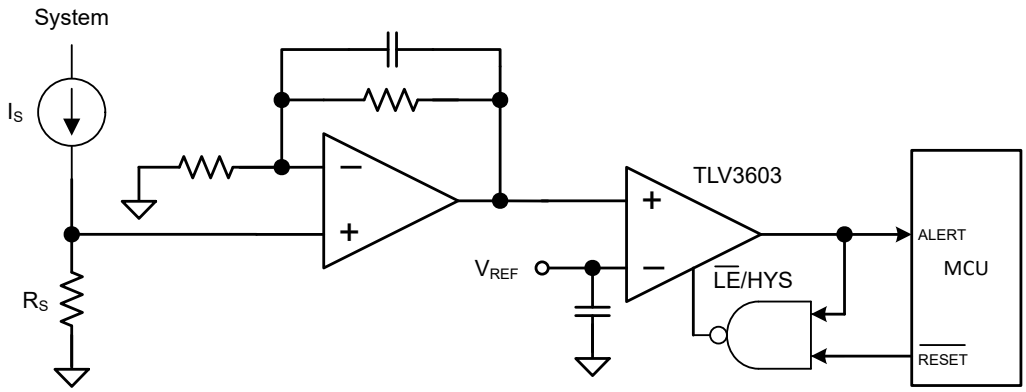


图 8-10. Over-Current Latched Output Circuit

8.2.4 External Trigger Function for Oscilloscopes

Below is a typical configuration for creating an external trigger on oscilliscopes. The user adjusts the trigger level by programming a DAC that the TLV360x can use as a reference. The input from an oscilloscope channel is then compared to the trigger reference voltage, and the comparator sends a signal to a downstream FPGA to begin a capture.

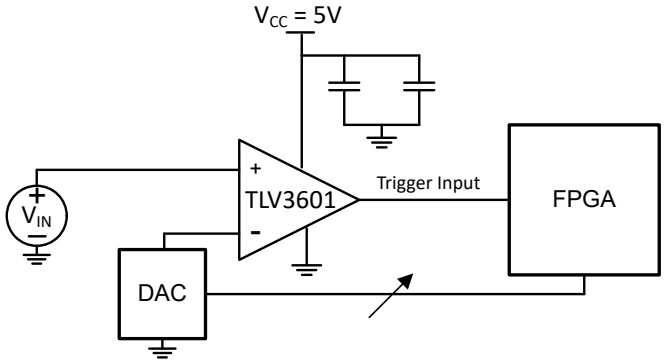


图 8-11. External Trigger Function

9 Power Supply Recommendations

The TLV360x are specified for operation from 2.4 V to 5.5 V. While most applications will require single supply operation where VEE is connected to the ground plane and VCC is connected to the intended power supply level, the comparators can also be operated with split supplies. One caution when using split supplies is that the output logic levels are determined by the VCC and VEE levels. For example, if split supplies of +/- 2.5V are used, the output levels will be 2.5V and -2.5V accordingly. In addition, the logic level of the $\overline{\text{LE}}$/HYS pin will also be referenced to VEE. This means that the external hysteresis resistor on the TLV3603-Q1 needs to be connected between the $\overline{\text{LE}}$/HYS pin and VEE (not to ground) for proper operation.

Regardless of single supply or split supply operation, proper decoupling capacitors are required. It is recommended to use a scheme of multiple, low-ESR ceramic capacitors from the supply pins to the ground plane for optimum performance. A good combination would be 100 pF, 10 nF, and 1 uF with the lowest value capacitor closest to the comparator.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.

   Likewise, high performance board materials such as Rogers or high speed FR4 is also recommended.
2. Place a decoupling capacitor (100-pF ceramic, surface-mount capacitor) between V_{CC} and

   V_{EE} as close to the device as possible. Using multiple bypass capacitors in different decade ranges such as 100-pF, 100-nF, and 1-µF provides the best noise reduction across frequency ranges.
3. On the inputs and the output, keep lead lengths as short and minimize capacitive coupling to the traces by having a keepout area around the traces that is 3x the width of the traces. It is also recommended to keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.

10.2 Layout Example

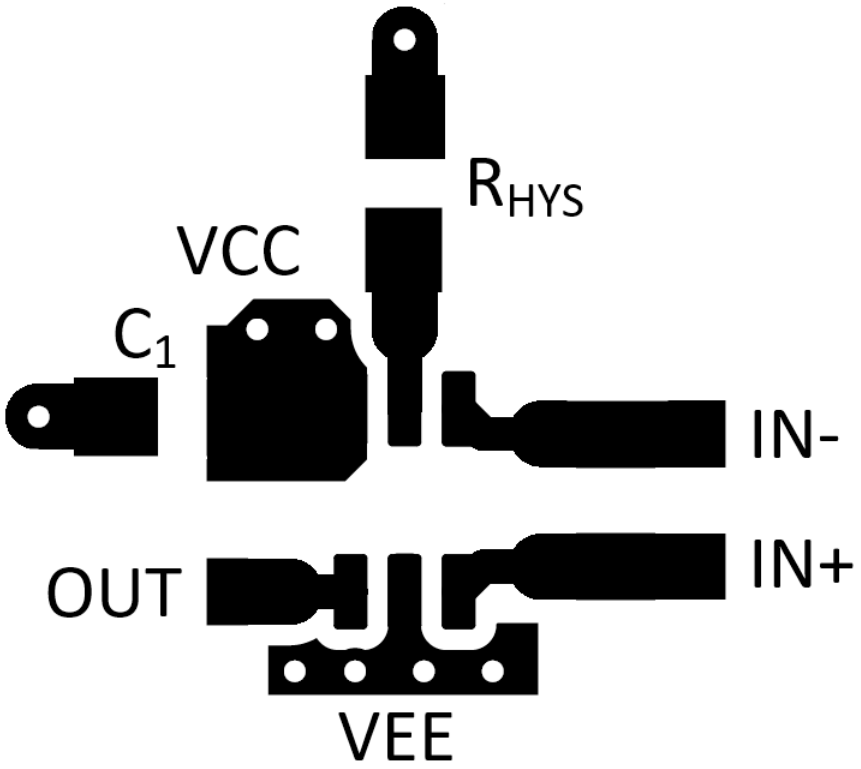


图 10-1. TLV3603 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3601QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	601Q
TLV3601QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	601Q
TLV3601QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1JG
TLV3601QDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1JG
TLV3602QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	602Q
TLV3602QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	602Q
TLV3603QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1JH
TLV3603QDCKRQ1.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1JH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3601-Q1, TLV3602-Q1, TLV3603-Q1 :

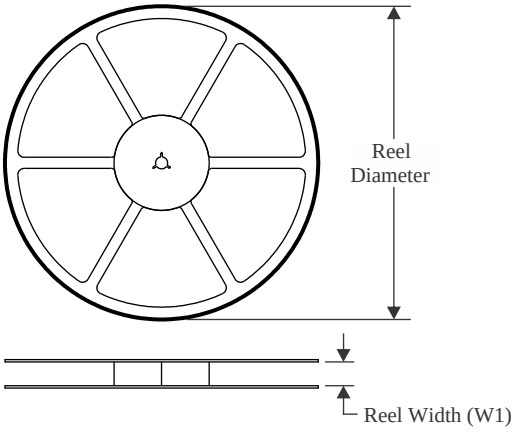
- Catalog : TLV3601, TLV3602, TLV3603
- Enhanced Product : TLV3603-EP

NOTE: Qualified Version Definitions:

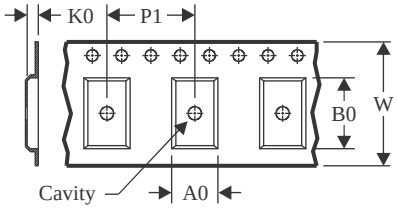
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

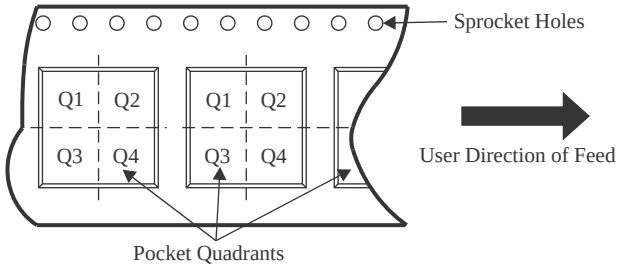


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

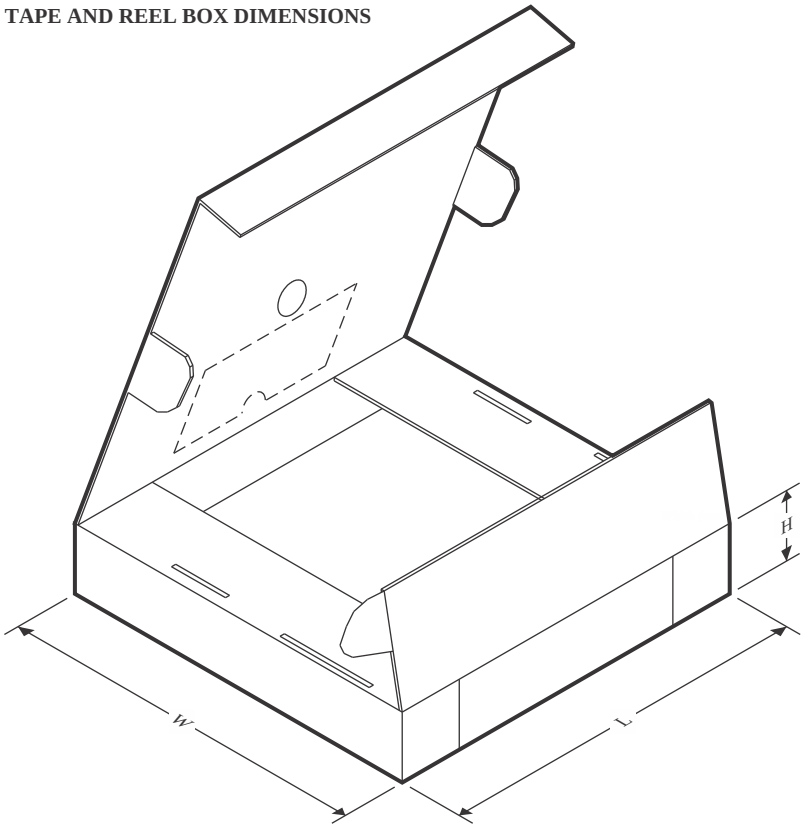
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3601QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3601QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TLV3602QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV3603QDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

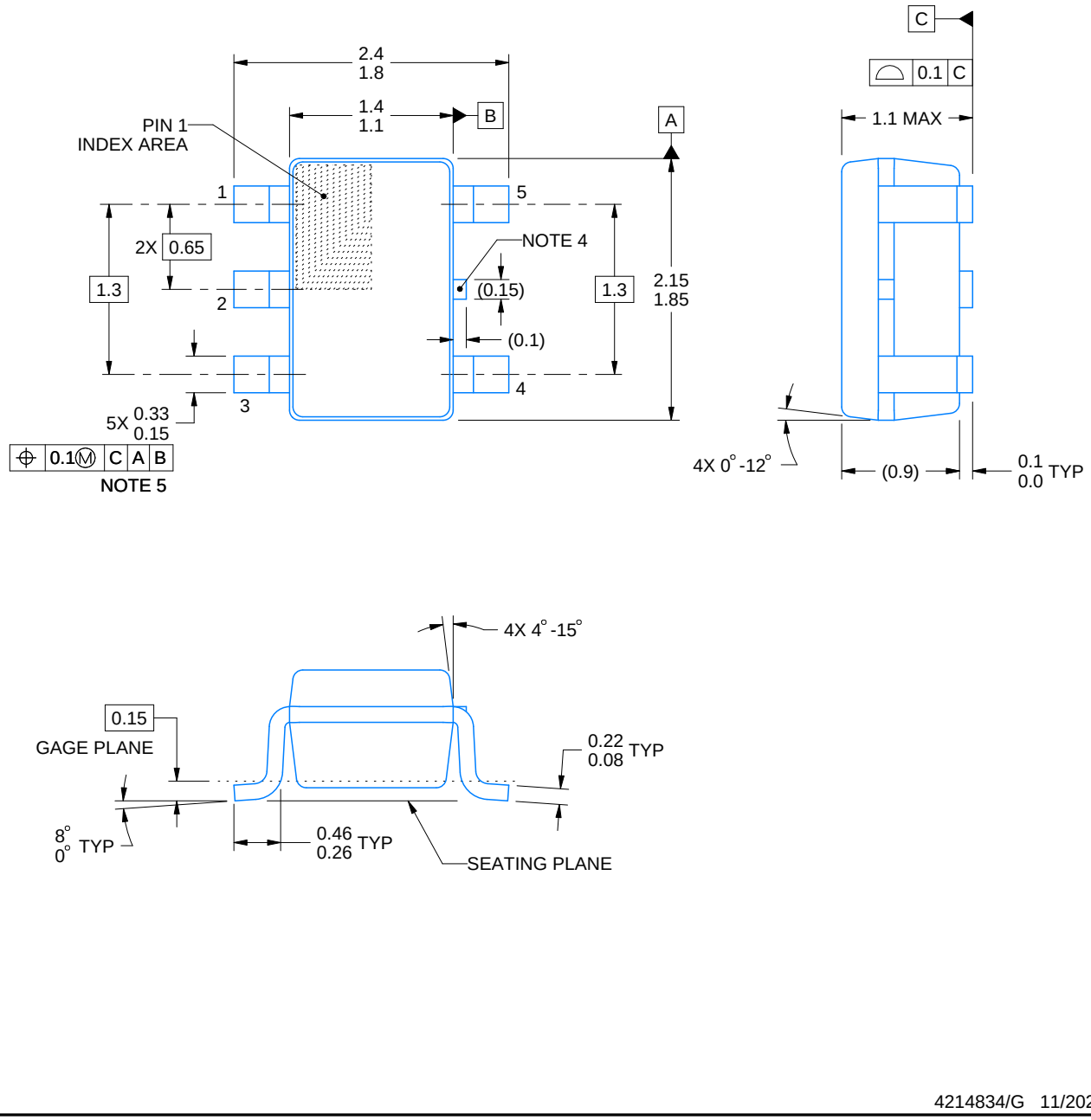
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3601QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV3601QDCKRQ1	SC70	DCK	5	3000	183.0	183.0	20.0
TLV3602QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV3603QDCKRQ1	SC70	DCK	6	3000	183.0	183.0	20.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

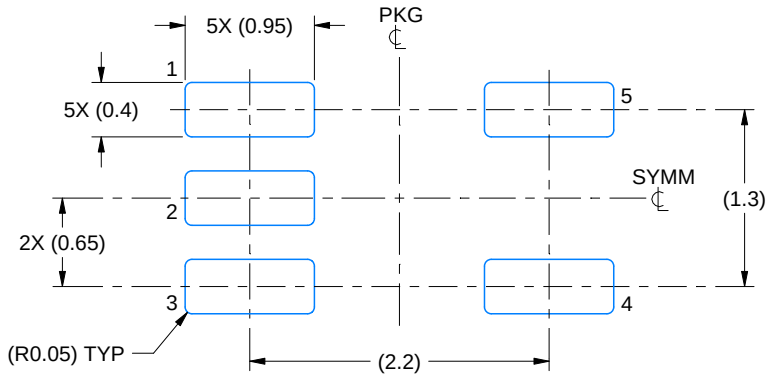
SMALL OUTLINE TRANSISTOR



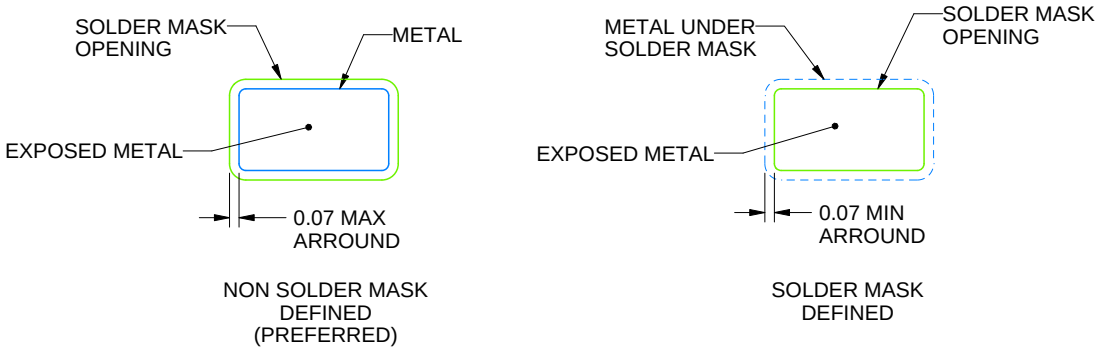
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

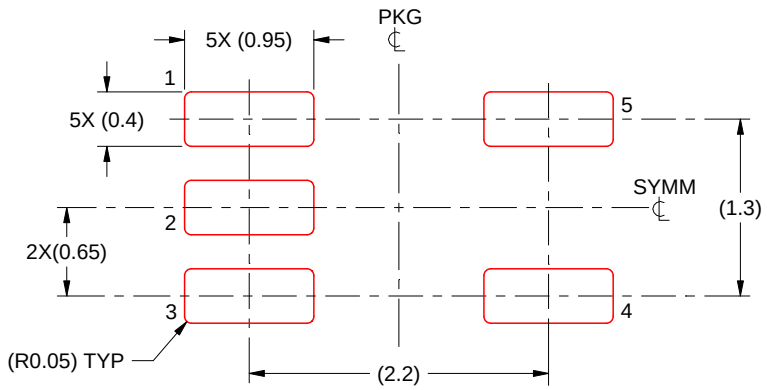


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

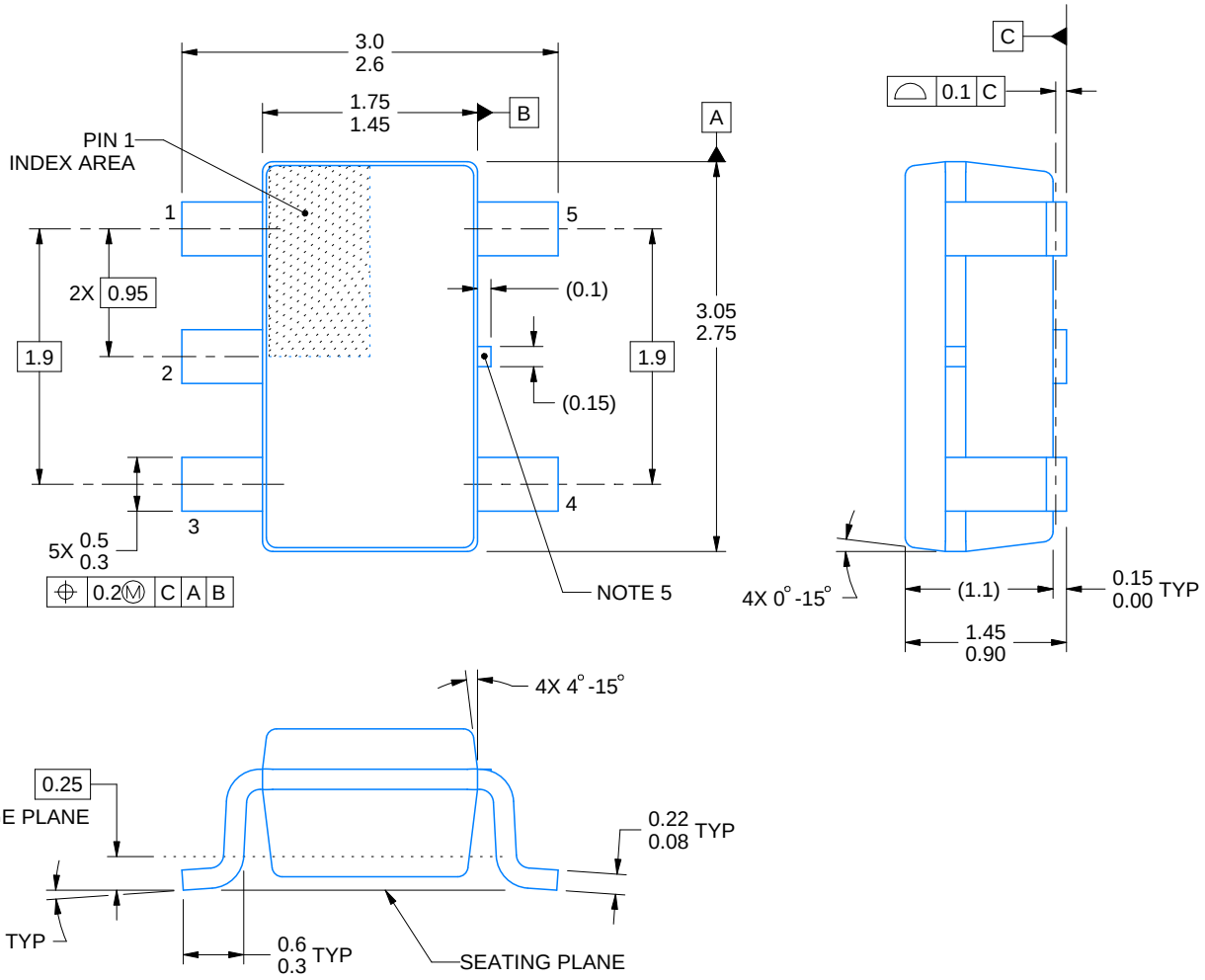
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

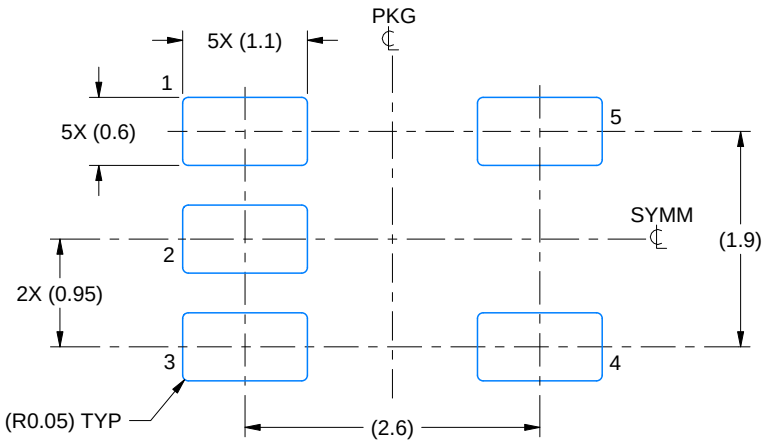
SMALL OUTLINE TRANSISTOR



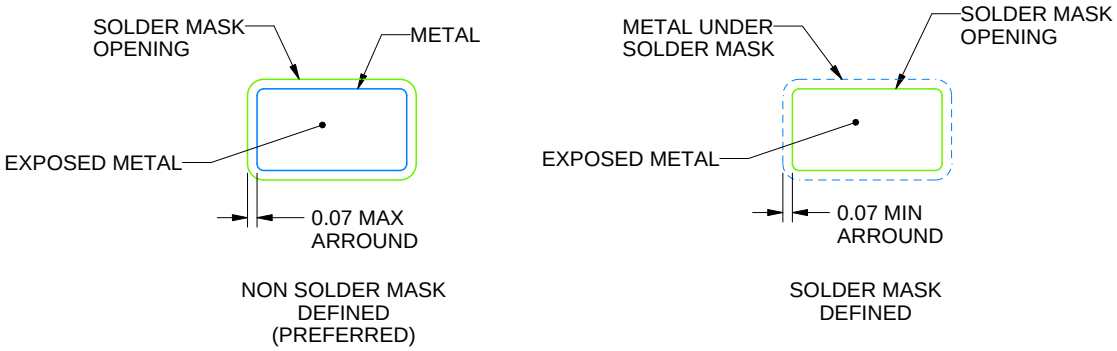
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

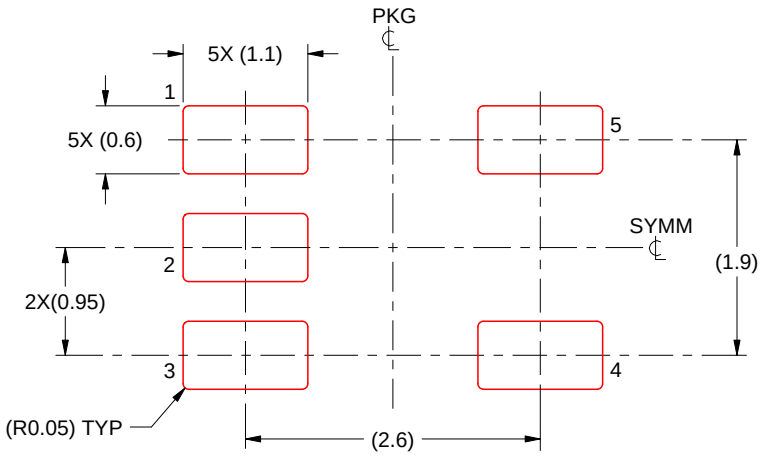


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

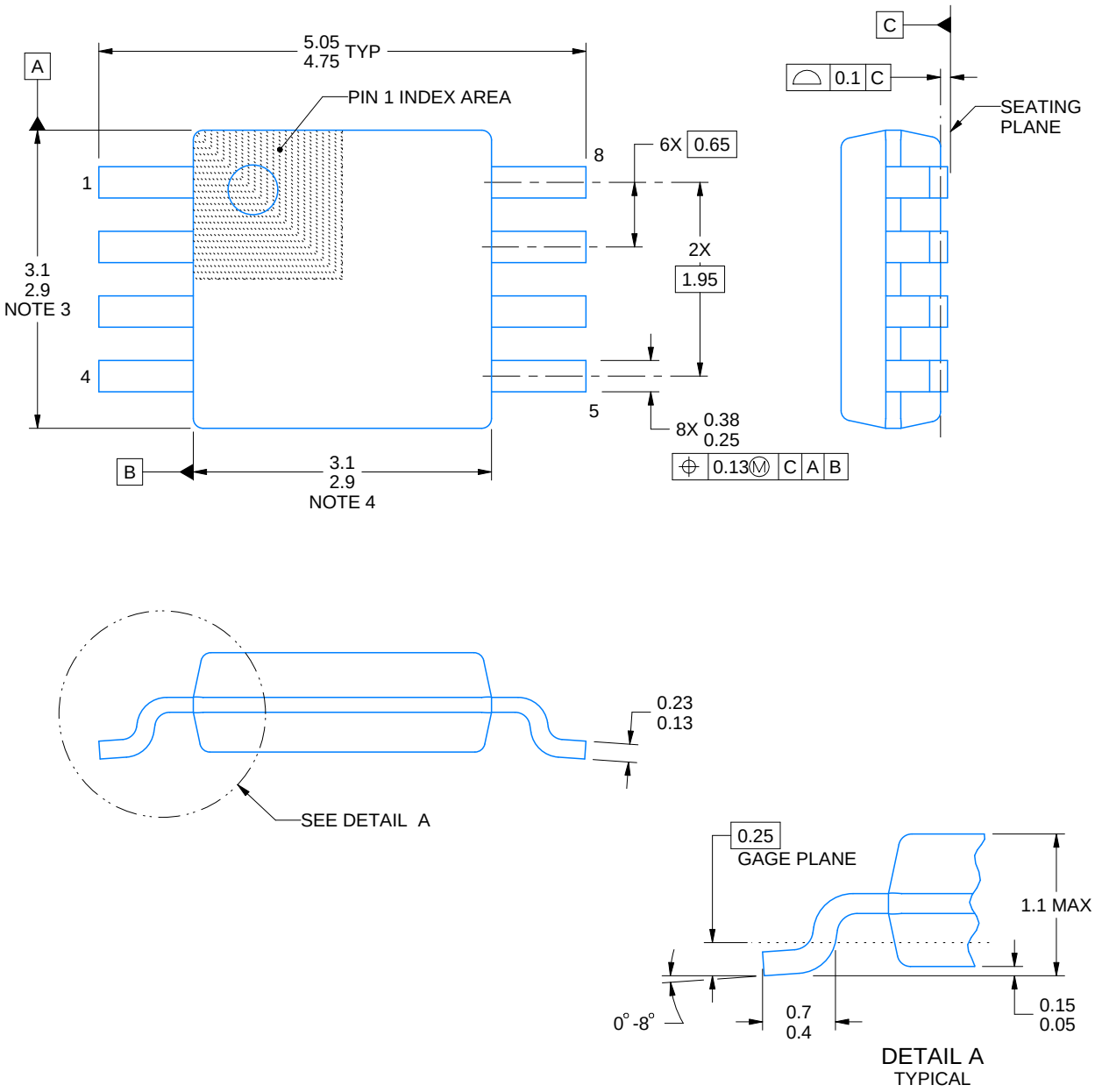
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

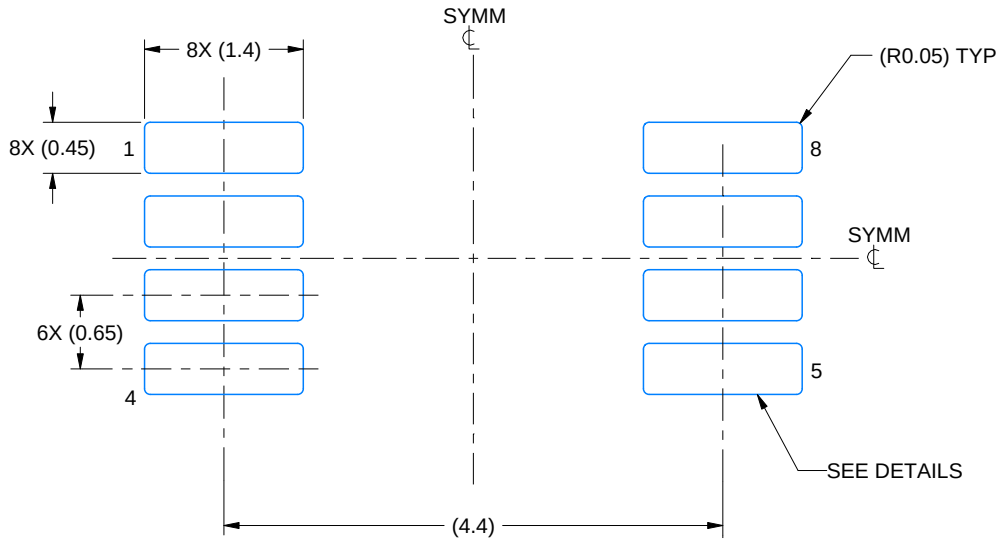
SMALL OUTLINE PACKAGE



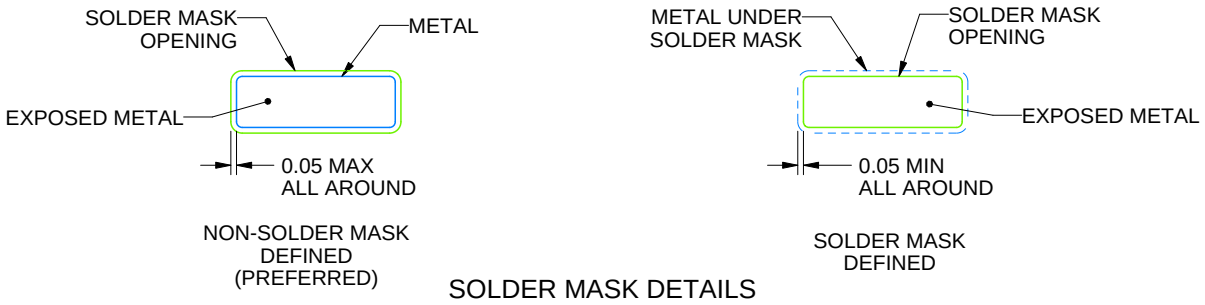
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

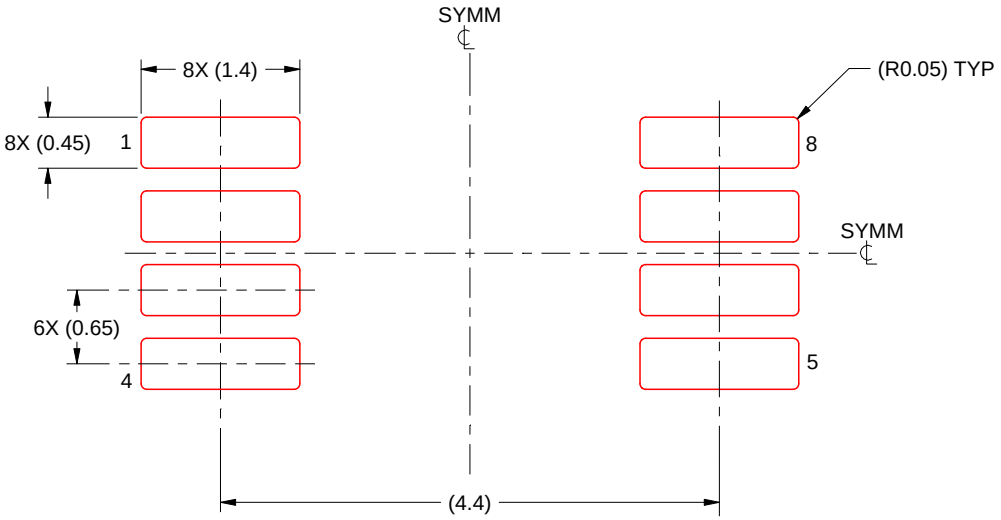


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

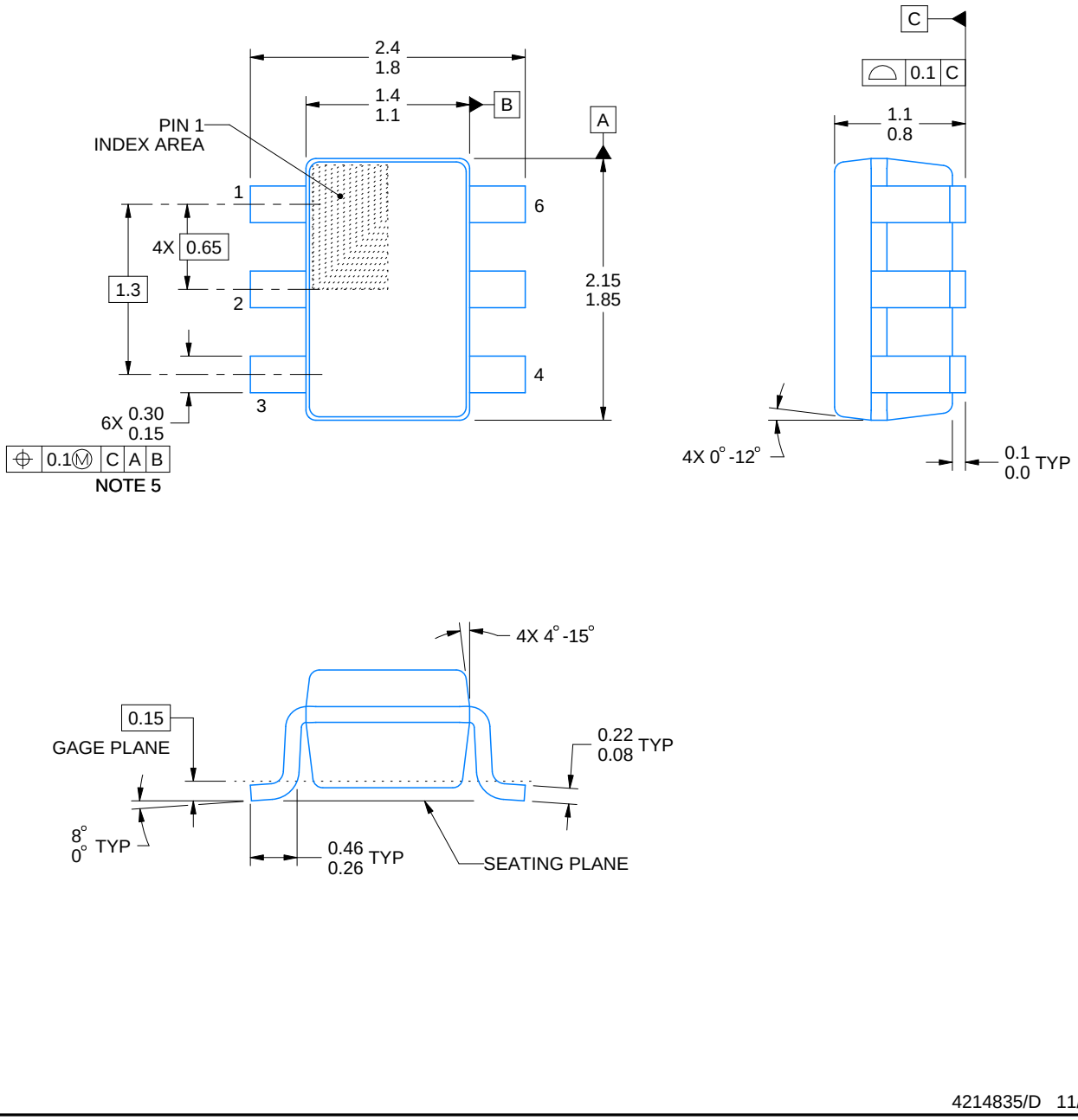
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

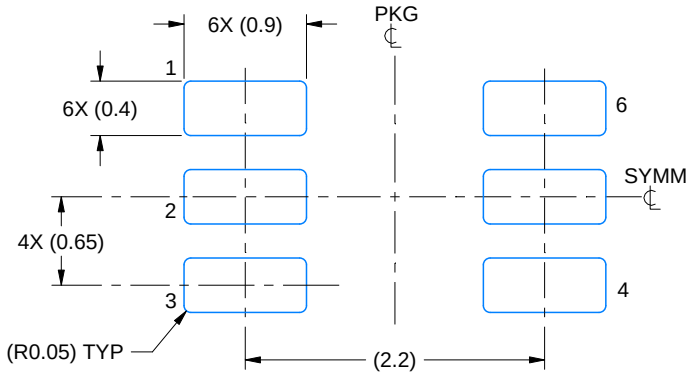
SMALL OUTLINE TRANSISTOR



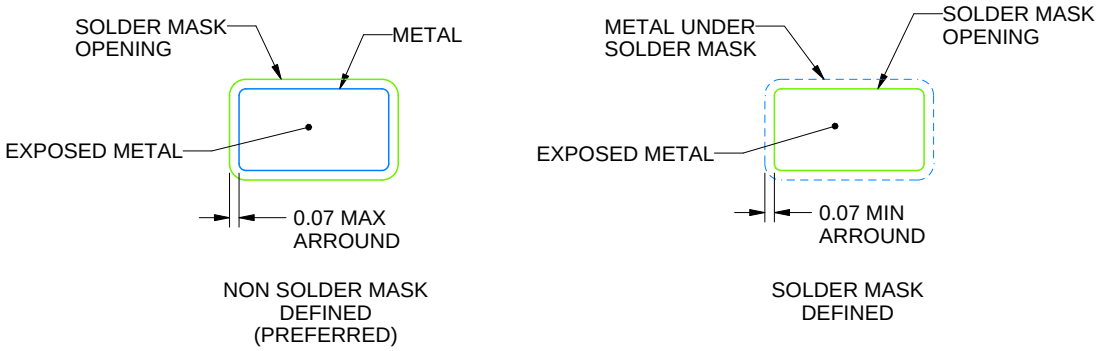
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

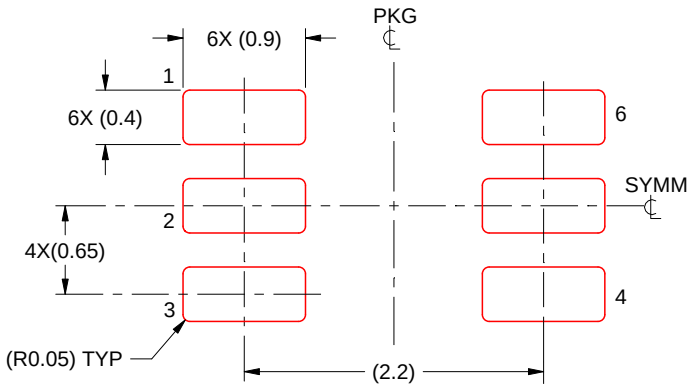


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月