

适用于成本敏感型系统的 TLV600x-Q1 低功耗、轨至轨输入/输出、1MHz 运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
 - 器件温度等级 1: -40°C 至 $+125^{\circ}\text{C}$, T_A
 - 器件 HBM ESD 分类等级 3A
 - 器件 CDM ESD 分类等级 C6
- 适用于成本敏感型系统的通用型放大器
- 电源电压范围: 1.8V 至 5.5V
- 增益带宽: 1MHz
- 低静态电流: $75\mu\text{A}/\text{通道}$
- 轨至轨输入和输出
- 低失调电压: 0.75mV
- 单位增益稳定
- 输入电压噪声密度: 1kHz 时为 $28\text{nV}/\sqrt{\text{Hz}}$
- 内部射频和电磁干扰滤波器
- 扩展温度范围: -40°C 至 125°C

2 应用

- 针对 AEC-Q100 等级 1 应用进行了优化
- 电动汽车逆变器
- 信息娱乐系统
- 被动安全
- 车身电子装置和照明

3 说明

TLV600x-Q1 系列单通道和双通道运算放大器专为通用汽车应用而设计。该系列具有轨至轨输入和输出 (RRIO) 摆幅、低静态电流 (典型值为 $75\mu\text{A}$)、高带宽 (1MHz) 以及超低噪声 (1kHz 时为 $28\text{nV}/\sqrt{\text{Hz}}$) 等特性, 因此对于需要在成本与性能之间实现良好平衡的各种汽车应用 (如信息娱乐系统、发动机控制单元和汽车照明) 而言很具有吸引力。低输入偏置电流 (典型值为 $\pm 1\text{pA}$) 使 TLV600x-Q1 适合用于具有兆欧级源阻抗的应用。

TLV600x-Q1 采用稳健耐用的设计, 方便电路设计人员使用: 该器件在容性负载高达 150pF 的条件下具有单位增益稳定性, 集成了射频/EMI 抑制滤波器, 在过驱条件下无相位反转, 并具有高静电放电 (ESD) 保护 (4kV HBM)。

这些器件经过优化, 适合在低至 1.8V ($\pm 0.9\text{V}$) 和高达 5.5V ($\pm 2.75\text{V}$) 的电压下工作, 并且具有 -40°C 至 $+125^{\circ}\text{C}$ 的额定扩展工作温度范围。

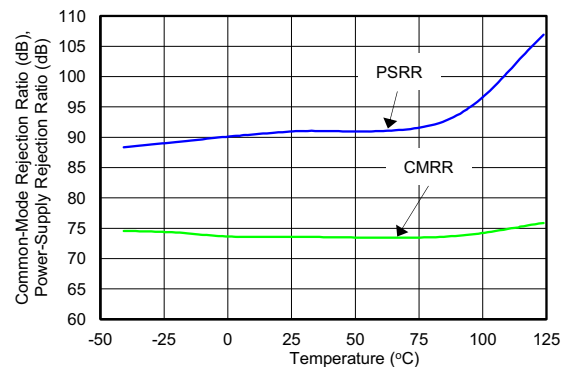
单通道 TLV6001-Q1 采用 SC70-5 封装, 双通道 TLV6002-Q1 采用 SOIC 和 VSSOP 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TLV6001-Q1	SC70 (5)	2.00mm × 1.25mm
TLV6002-Q1	SOIC (8)	3.91mm × 4.90mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

CMRR 和 PSRR 与温度间的关系



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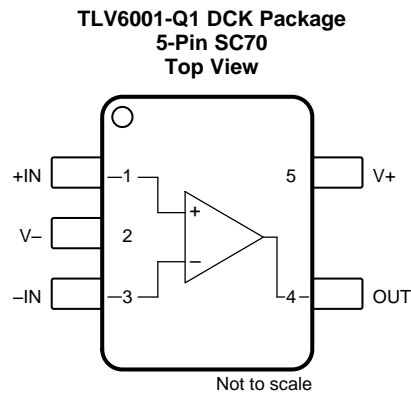
4 修订历史记录

Changes from Original (August 2018) to Revision A

Page

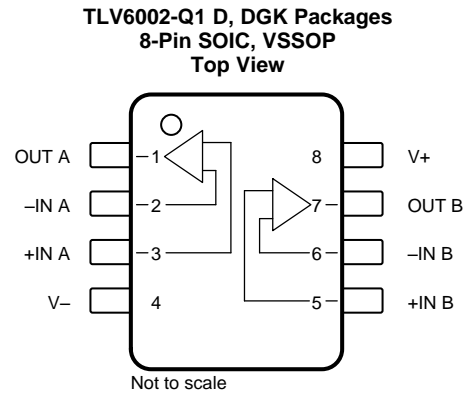
• 已添加 在数据表中添加了 TLV6002-Q1 器件	1
• 已添加 在整个数据表中添加 TLV6002-Q1 器件的双通道信息	1
• 已添加 添加了 TLV600x-Q1 系列的 ESD 分类级别	1

5 Pin Configuration and Functions



Pin Functions: TLV6001-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN	3	I	Inverting input
+IN	1	I	Noninverting input
OUT	4	O	Output
V-	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply


Pin Functions: TLV6002-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply voltage (V+) – (V–)	7		V
	Signal input pins, voltage ⁽²⁾	(V–) – 0.5	(V+) + 0.5	
Current	Signal input pins, current ⁽²⁾	–10	10	mA
	Output short-circuit ⁽³⁾	Continuous		
Temperature	Operating, T _A	–40	150	°C
	Junction, T _J	150		
	Storage, T _{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _S	Supply voltage	1.8	5.5	V
T _A	Specified temperature	–40	125	°C

6.4 Thermal Information: TLV6001-Q1

THERMAL METRIC ⁽¹⁾		TLV6001-Q1	
		DCK (SC70)	
		5 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	281.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	91.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.8	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

6.5 Thermal Information: TLV6002-Q1

THERMAL METRIC ⁽¹⁾		TLV6002-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.6	186.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	73.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.4	107.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.7	14.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	74.6	105.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics: $V_S = 1.8\text{ V to }5\text{ V }(\pm 0.9\text{ V to } \pm 2.75\text{ V})^{(1)}$

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			0.75	4.5	mV
dV_{OS}/dT	V_{OS} vs temperature	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		2		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio			86		dB
INPUT BIAS CURRENT						
I_B	Input bias current	$T_A = 25^\circ\text{C}$		± 1		μA
I_{OS}	Input offset current			± 1		μA
INPUT IMPEDANCE						
Z_{ID}	Differential			100 1		$\text{M}\Omega \text{pF}$
Z_{IC}	Common-mode			1 5		$10^{13}\Omega \text{pF}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	$(V-) - 0.2$		$(V+) + 0.2$	V
CMRR	Common-mode rejection ratio	$V_{CM} = -0.2\text{ V to } 5.7\text{ V}$	60	76		dB
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$0.3\text{ V} < V_O < (V+) - 0.3\text{ V}$, $R_L = 2\text{ k}\Omega$	90	110		
	Phase margin	$V_S = 5\text{ V}$, $G = 1$		65		$^\circ$
OUTPUT						
V_O	Voltage output swing from supply rails	$R_L = 100\text{ k}\Omega$		5		mV
		$R_L = 2\text{ k}\Omega$		75	100	
I_{SC}	Short-circuit current			± 15		mA
R_O	Open-loop output impedance			2300		Ω
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1		MHz
SR	Slew rate			0.5		$\text{V}/\mu\text{s}$
t_s	Settling time	To 0.1%, $V_S = 5\text{ V}$, 2-V step, $G = +1$		5		μs
NOISE						
	Input voltage noise (peak-to-peak)	$f = 0.1\text{ Hz to } 10\text{ Hz}$		6		μV_{PP}
e_n	Input voltage noise density	$f = 1\text{ kHz}$		28		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input current noise density	$f = 1\text{ kHz}$		5		$\text{fA}/\sqrt{\text{Hz}}$
POWER SUPPLY						
V_S	Specified voltage range		1.8 (± 0.9)		5.5 (± 2.75)	V
I_Q	Quiescent current per amplifier	$I_O = 0\text{ mA}$, $V_S = 5\text{ V}$		75	100	μA
	Power-on time	$V_S = 0\text{ V to } 5\text{ V}$, to 90% I_Q level		10		μs

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25°C , unless otherwise noted. Overtemperature limits are based on characterization and statistical analysis.

6.7 Typical Characteristics: Table of Graphs

表 1. Table of Graphs

TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	图 1
Quiescent Current vs Supply Voltage	图 2
Offset Voltage Production Distribution	图 3
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	图 4
CMRR and PSRR vs Frequency (RTI)	图 5
0.1-Hz to 10-Hz Input Voltage Noise (5.5 V)	图 6
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	图 7
Input Bias and Offset Current vs Temperature	图 8
Open-Loop Output Impedance vs Frequency	图 9
Maximum Output Voltage vs Frequency and Supply Voltage	图 10
Output Voltage Swing vs Output Current	图 11
Closed-Loop Gain vs Frequency, $G = 1, -1, 10$ (1.8 V)	图 12
Small-Signal Step Response, Noninverting (1.8 V)	图 13
Small-Signal Step Response, Noninverting (5.5 V)	图 14
Large-Signal Step Response, Noninverting (1.8 V)	图 15
Large-Signal Step Response, Noninverting (5.5 V)	图 16
No Phase Reversal	图 17
EMIRR IN+ vs Frequency	图 18

6.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

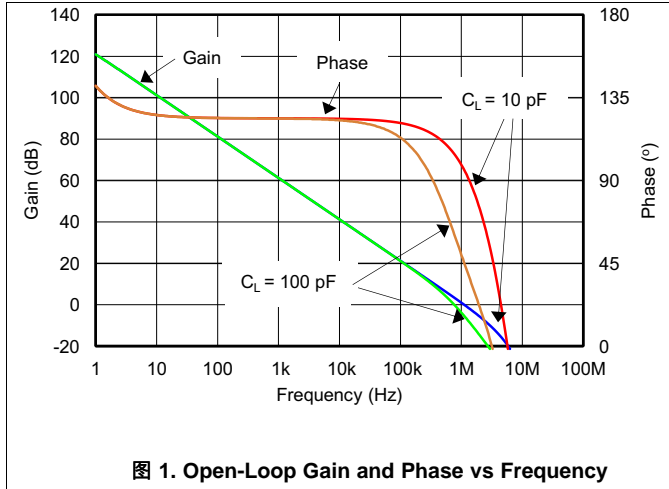


图 1. Open-Loop Gain and Phase vs Frequency

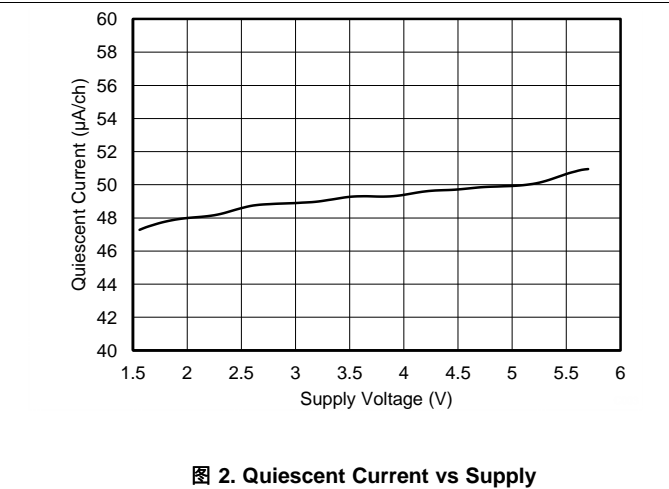


图 2. Quiescent Current vs Supply

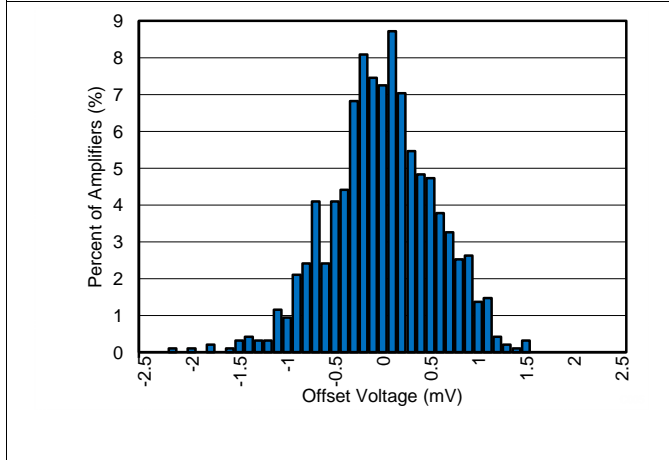


图 3. Offset Voltage Production Distribution

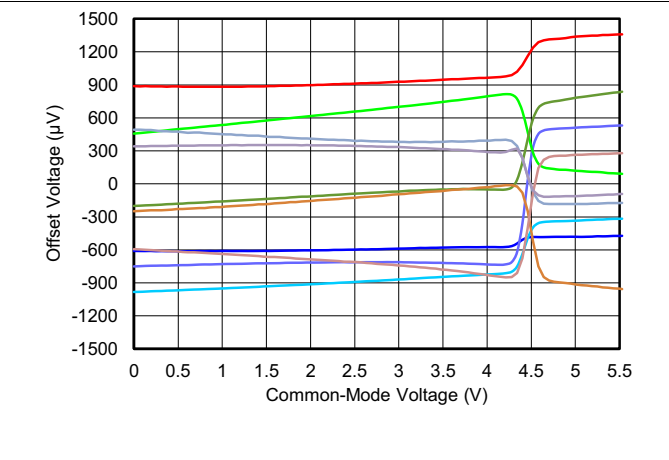


图 4. Offset Voltage vs Common-Mode Voltage

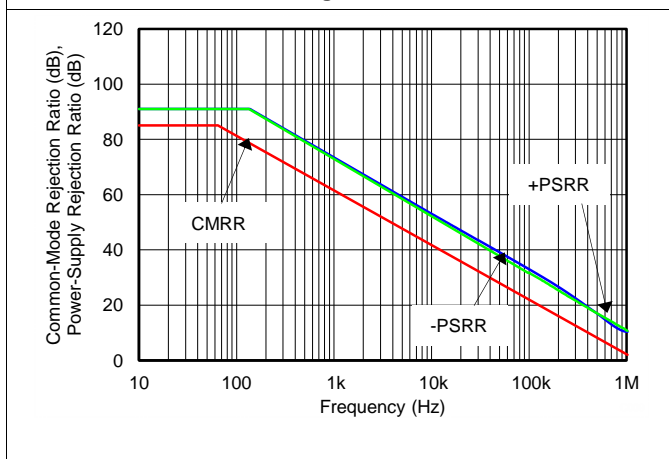


图 5. CMRR and PSRR vs Frequency (Referred-to-Input)

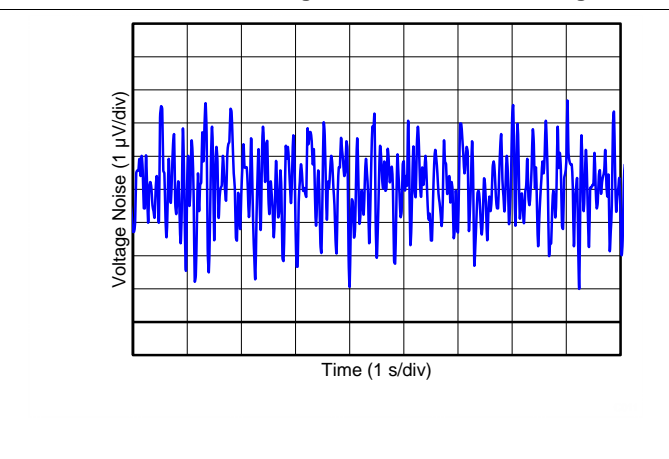


图 6. 0.1-Hz to 10-Hz Input Voltage Noise

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

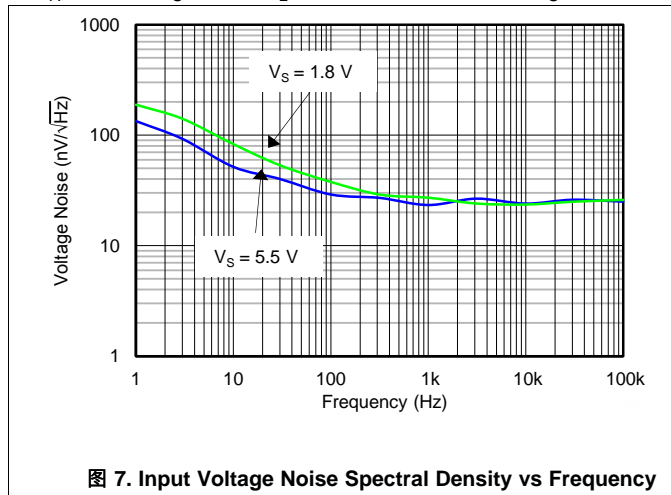


图 7. Input Voltage Noise Spectral Density vs Frequency

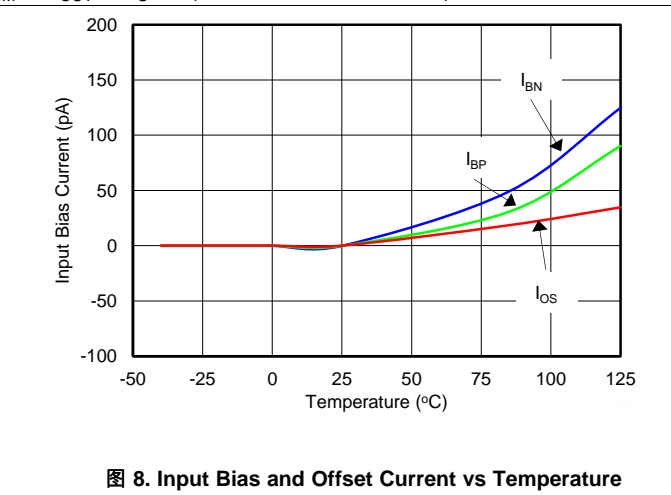


图 8. Input Bias and Offset Current vs Temperature

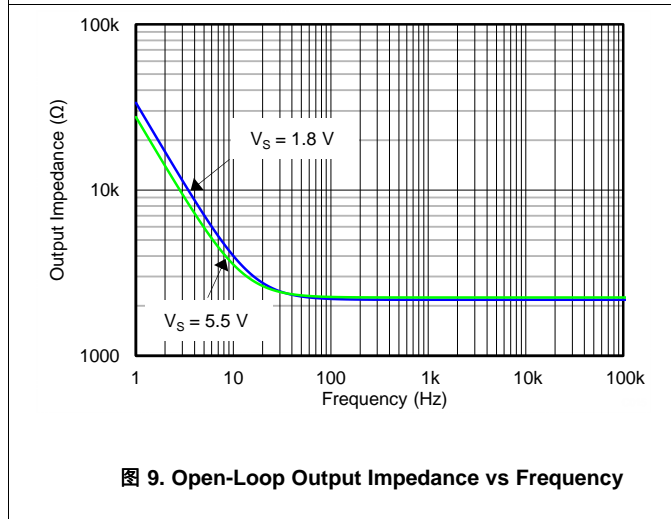


图 9. Open-Loop Output Impedance vs Frequency

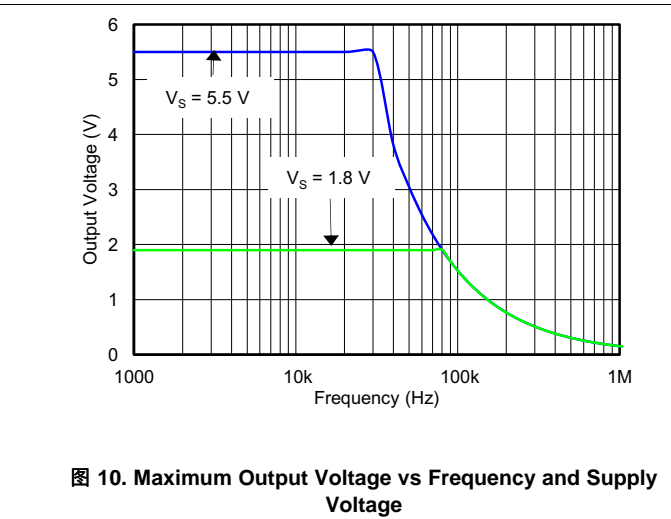


图 10. Maximum Output Voltage vs Frequency and Supply Voltage

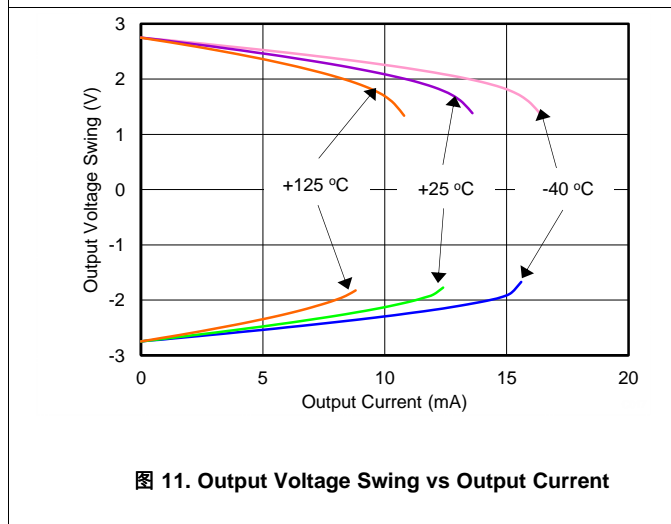


图 11. Output Voltage Swing vs Output Current

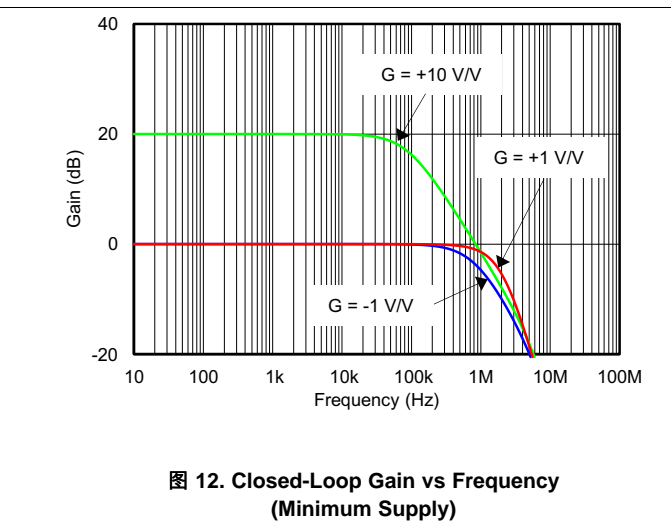


图 12. Closed-Loop Gain vs Frequency (Minimum Supply)

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

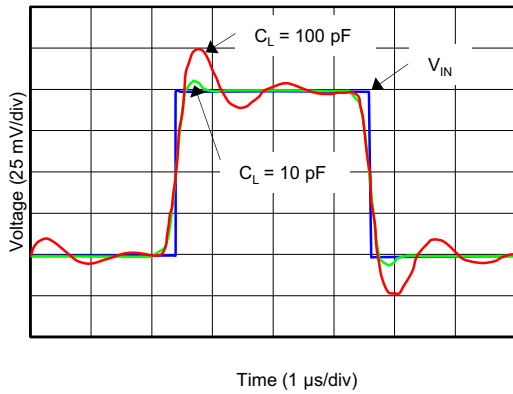


图 13. Small-Signal Pulse Response (Minimum Supply)

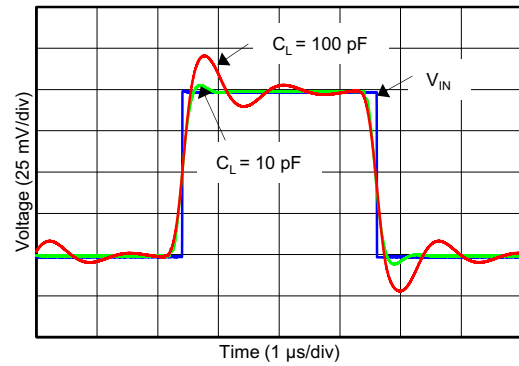


图 14. Small-Signal Pulse Response (Maximum Supply)

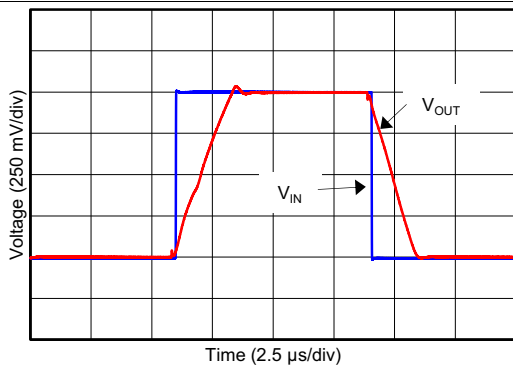


图 15. Large-Signal Pulse Response (Minimum Supply)

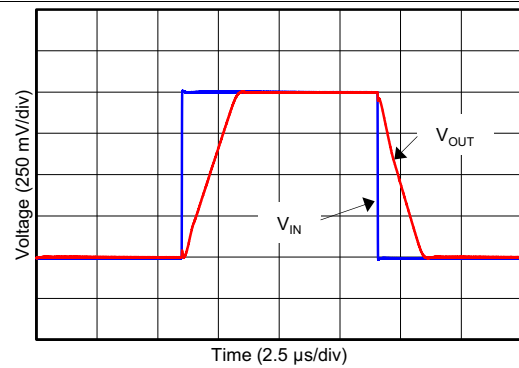


图 16. Large-Signal Pulse Response (Maximum Supply)

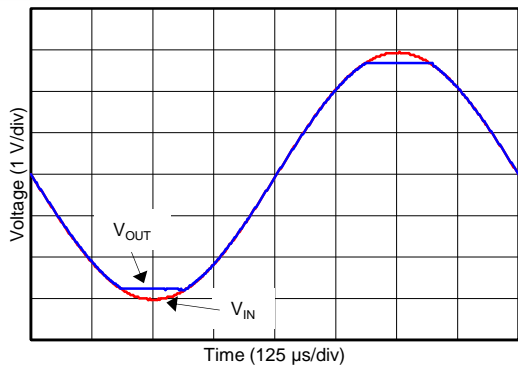


图 17. No Phase Reversal

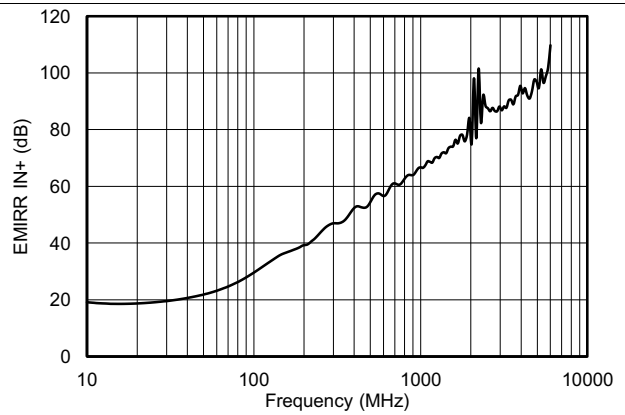


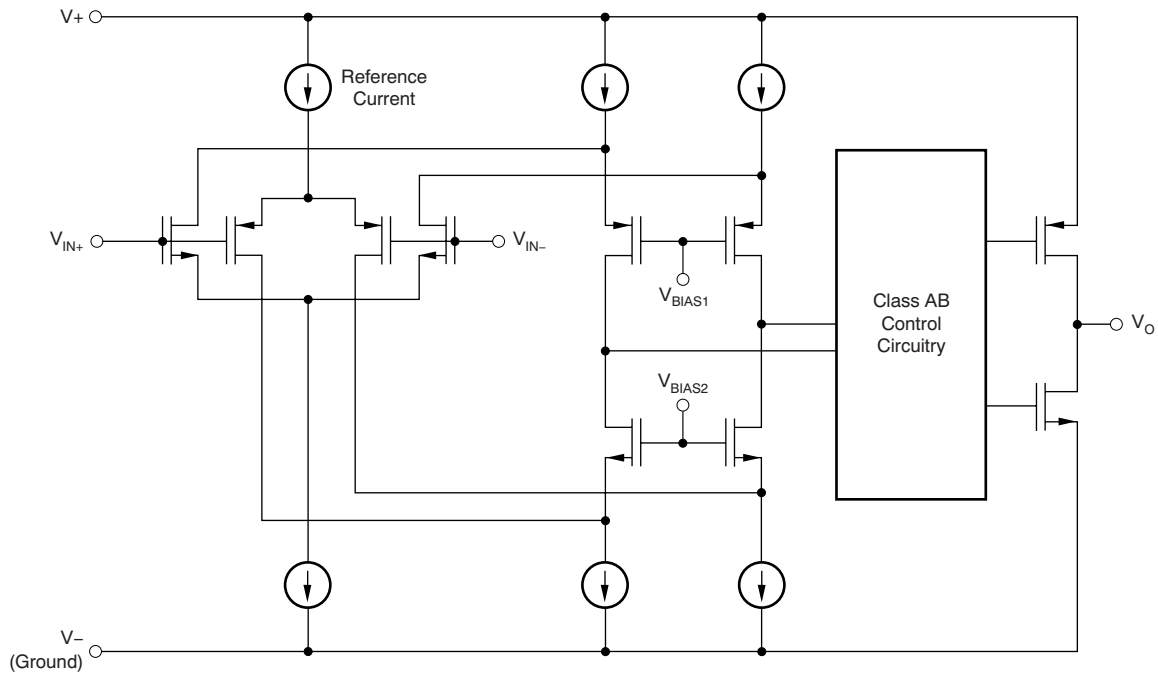
图 18. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The TLV600x-Q1 family of operational amplifiers is a general-purpose, low-cost family that is designed for a wide range of portable applications. Rail-to-rail input and output swings, low quiescent current, and wide dynamic range make the operational amplifier designed to drive sampling analog-to-digital converters (ADCs) and other single-supply applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLV600x-Q1 family is fully specified and tested from 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V). The [Typical Characteristics](#) section shows parameters that vary with supply voltage.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV600x-Q1 family extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as the [Functional Block Diagram](#) section shows. The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.3$ V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately $(V+) - 1.3$ V. There is a small transition region, typically $(V+) - 1.4$ V to $(V+) - 1.2$ V, in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. As a result, the transition region (both stages on) can range from $(V+) - 1.7$ V to $(V+) - 1.5$ V on the low end, and up to $(V+) - 1.1$ V to $(V+) - 0.9$ V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

7.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLV600x-Q1 family delivers a robust output drive capability. A class AB output stage with common source transistors achieve full rail-to-rail output swing capability. For resistive loads up to 100 k Ω , the output swings typically to within 5 mV of either supply rail regardless of the power supply voltage that is applied. [Figure 11](#) shows that different load conditions change the ability of the amplifier to swing close to the rails.

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the TLV600x-Q1 family is specified in several ways so the best match for a given application can be used; see the [Electrical Characteristics](#). First, the CMRR of the device in the common-mode range below the transition region ($V_{CM} < (V+) - 1.3$ V) is shown. This specification is the best indicator of the capability of the device when the application requires the use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at ($V_{CM} = -0.2$ V to 5.7 V). This last value includes the variations seen through the transition region, as [Figure 4](#) shows.

7.3.5 Capacitive Load and Stability

The TLV600x-Q1 family is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the TLV600x-Q1 family can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing if an amplifier is stable in operation. An operational amplifier in the unity-gain (1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency for instability than an amplifier that is operated at a higher noise gain. The capacitive load in conjunction with the op amp output resistance creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the TLV600x-Q1 family remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some capacitors (C_L greater than 1 μ F) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains.

Feature Description (接下页)

One technique for increasing the capacitive load drive capability of the amplifier when the device operates in a unity-gain configuration is to insert a small resistor, typically $10\ \Omega$ to $20\ \Omega$, in series with the output, as 图 19 shows. This resistor reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

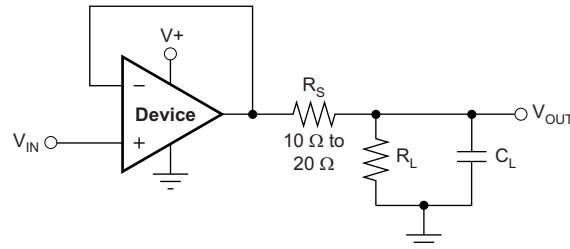


图 19. Improving Capacitive Load Drive

7.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output can shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The TLV600x-Q1 family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. This filter provides common-mode and differential mode filtering. The filter is designed for a cutoff frequency of approximately 35 MHz ($-3\ \text{dB}$) with a rolloff of 20 dB per decade.

Texas Instruments developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. 图 18 shows the results of this testing on the TLV600x-Q1 family. [EMI Rejection Ratio of Operational Amplifiers](#) shows detailed information, and is available for download from www.ti.com.

7.4 Device Functional Modes

The TLV600x-Q1 family has a single functional mode. The device is powered on if the power-supply voltage is between $1.8\ \text{V}$ ($\pm 0.9\ \text{V}$) and $5.5\ \text{V}$ ($\pm 2.75\ \text{V}$).

7.5 Input and ESD Protection

The TLV600x-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power supply pins. The ESD protection diodes provide in-circuit, input overdrive protection if the current is limited to 10 mA, as the [Absolute Maximum Ratings](#) lists. 图 20 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

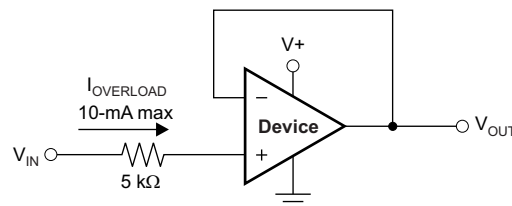


图 20. Input Current Protection

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV600x-Q1 is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is designed for a wide range of general-purpose applications. The class AB output stage can drive $\leq 10\text{-k}\Omega$ loads connected to any point between $V+$ and ground. The input common-mode voltage range includes both rails and allows the TLV600x-Q1 family to be used in any single-supply application.

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as 图 21 shows. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier makes negative input voltages positive on the output. To add amplification, select an input resistor (R_I) and a feedback resistor (R_F .)

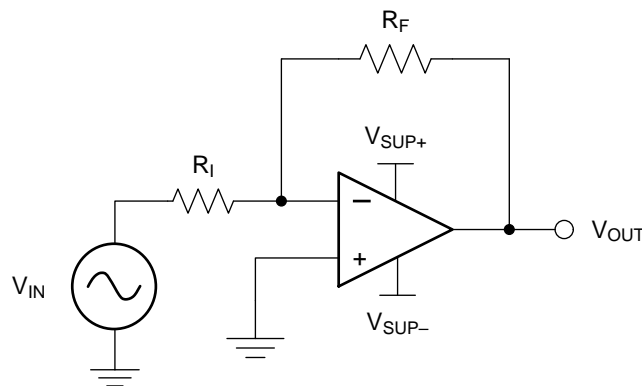


图 21. Application Schematic

8.2.1 Design Requirements

Select a supply voltage value that is larger than the input voltage range and the desired output range. Users must consider the limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O). For example, this application scales a signal of $\pm 0.5\text{ V}$ (1 V) to $\pm 1.8\text{ V}$ (3.6 V). Setting the supply at $\pm 2.5\text{ V}$ is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Use 公式 1 and 公式 2 to calculate the required gain for the inverting amplifier:

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Typical Application (接下页)

When the desired gain is determined, select a value for R_I or R_F . Selecting a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that large resistors (hundreds of kilohms) draw the smallest current but generate the highest noise. Small resistors (hundreds of ohms) generate low noise but draw high current. In this example, R_I equals 10 k Ω , and R_F equals 36 V. 公式 3 determines these values:

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

8.2.3 Application Curve

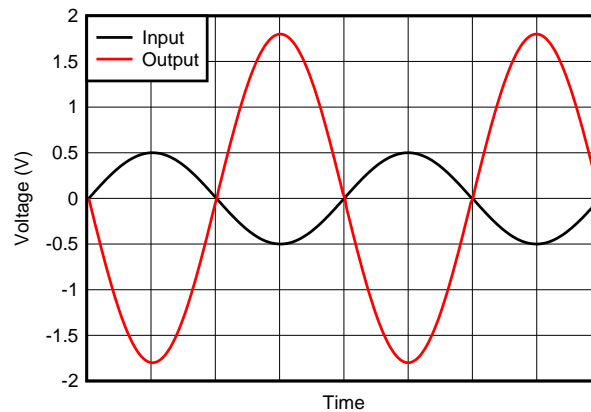
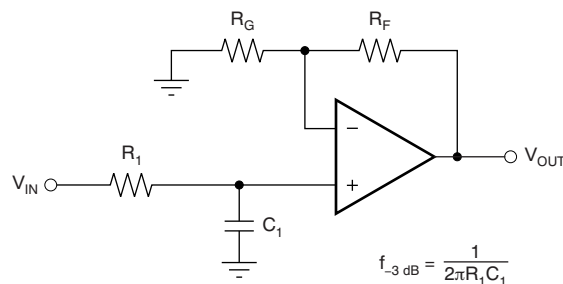


图 22. Inverting Amplifier Input and Output

8.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. To establish this minimum bandwidth, place an RC filter at the noninverting pin of the amplifier, as 图 23 shows.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

图 23. Single-Pole Low-Pass Filter

System Examples (接下页)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as 图 24 shows. For best results, the amplifier must have a bandwidth that is 8 to 10 times larger than the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

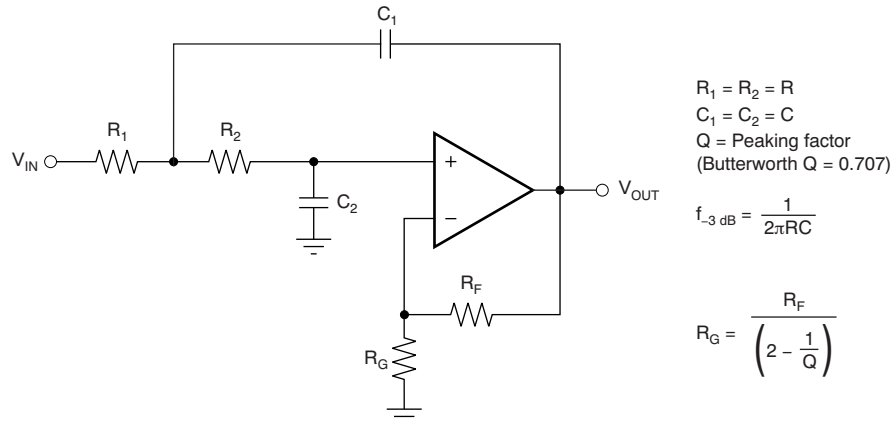


图 24. Two-Pole, Low-Pass, Sallen-Key Filter

9 Power Supply Recommendations

The TLV600x-Q1 family is specified for operation from 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V). The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V may permanently damage the device. (See the [Absolute Maximum Ratings](#)).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout Guidelines](#) section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#) (available for download from www.ti.com).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If the traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input in order to minimize parasitic capacitance, as shown in [图 25](#).
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example: Single Channel

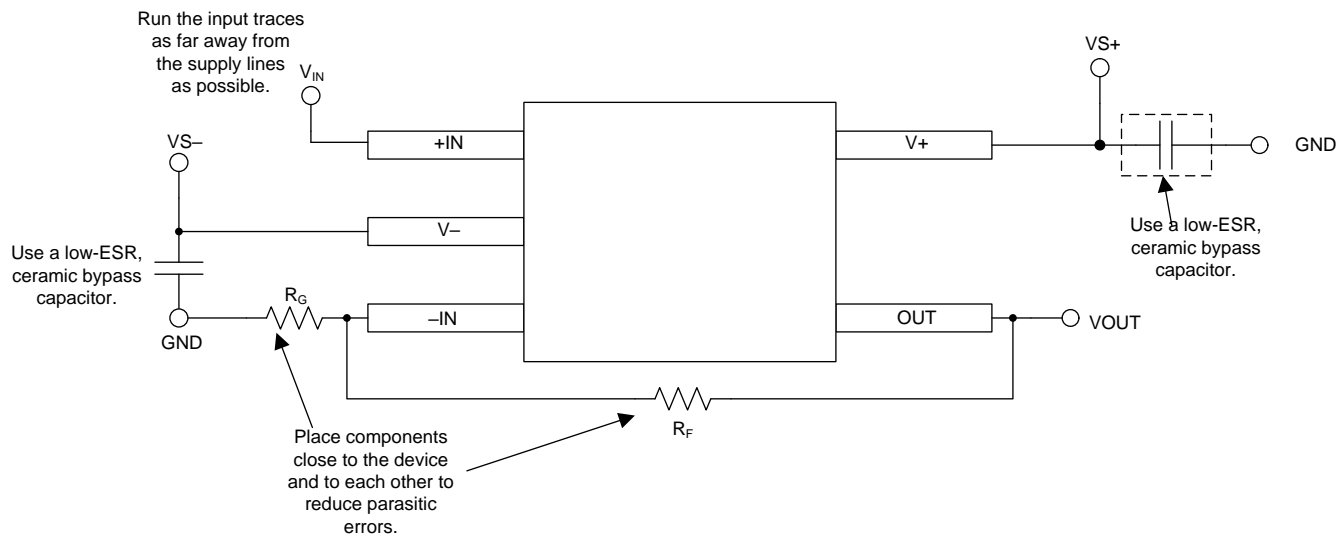


图 25. Operational Amplifier Board Layout for Noninverting Configuration

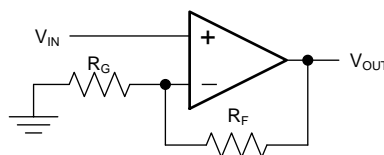


图 26. Schematic Representation of 图 25

10.3 Layout Example: Dual Channel

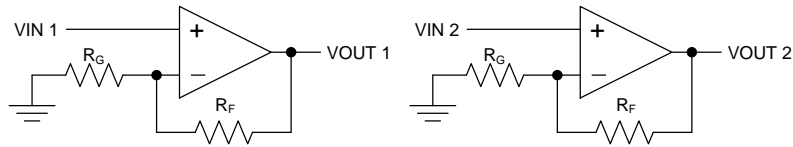


图 27. Schematic Representation for 图 25

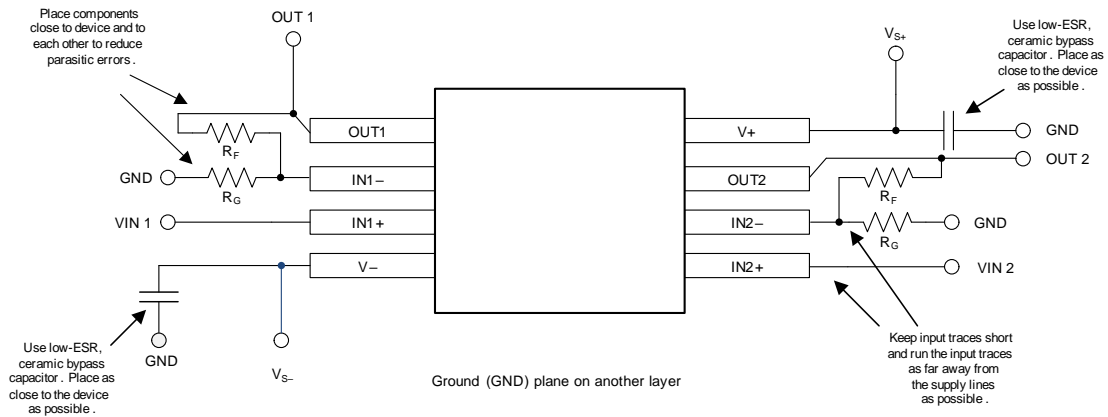


图 28. Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI), 《运算放大器的 EMI 抑制比》
- 德州仪器 (TI), 《电路板布局技巧》

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV6001-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV6002-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

E2E is a trademark of Texas Instruments.
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11.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — [TI 术语表](#)。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV6001QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1B1	Samples
TLV6002QDQGRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1NX6	Samples
TLV6002QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V6002Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV6001-Q1, TLV6002-Q1 :

- Catalog : [TLV6001](#), [TLV6002](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6001QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TLV6002QDGRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV6002QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6001QDCKRQ1	SC70	DCK	5	3000	183.0	183.0	20.0
TLV6002QDQKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV6002QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

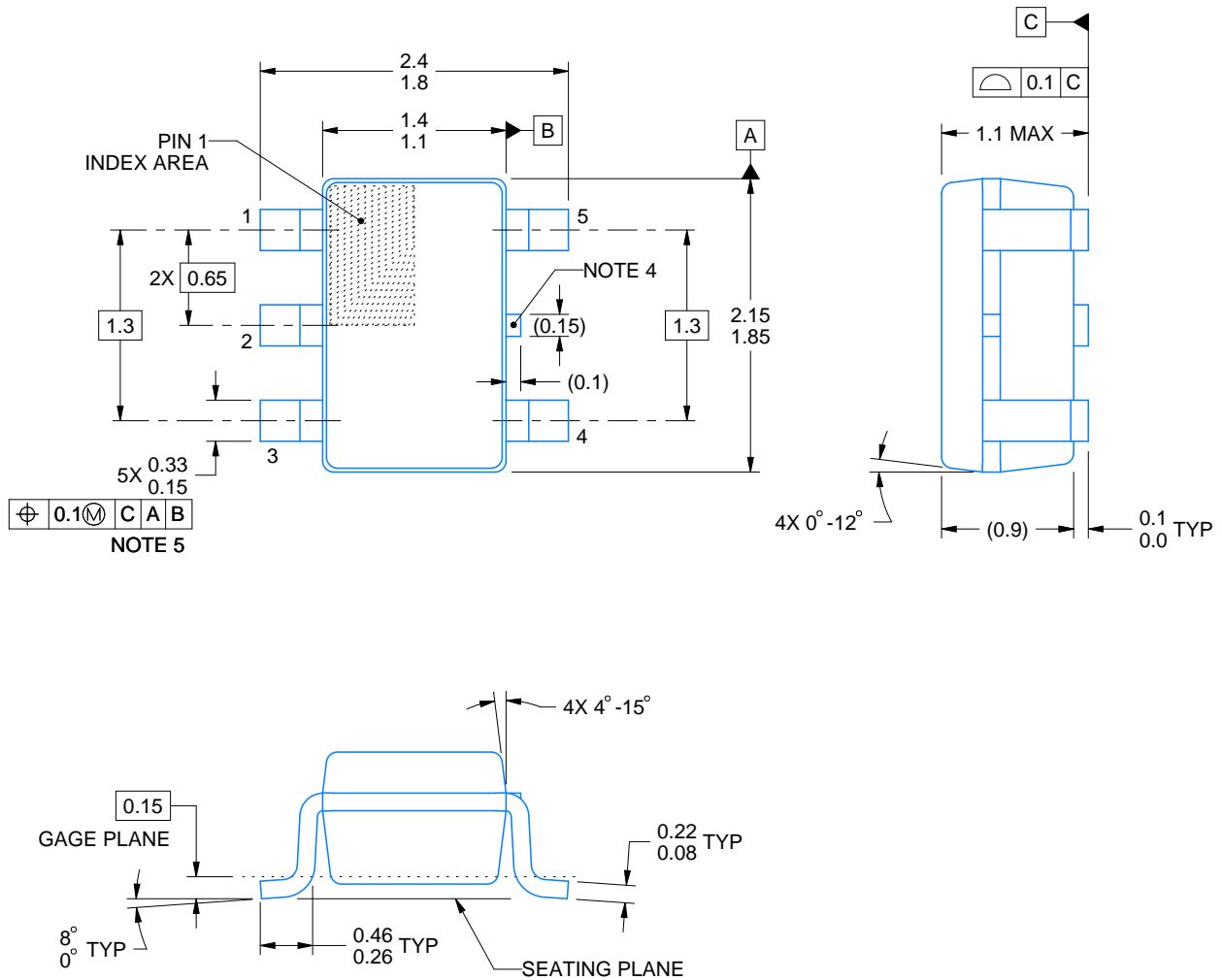
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

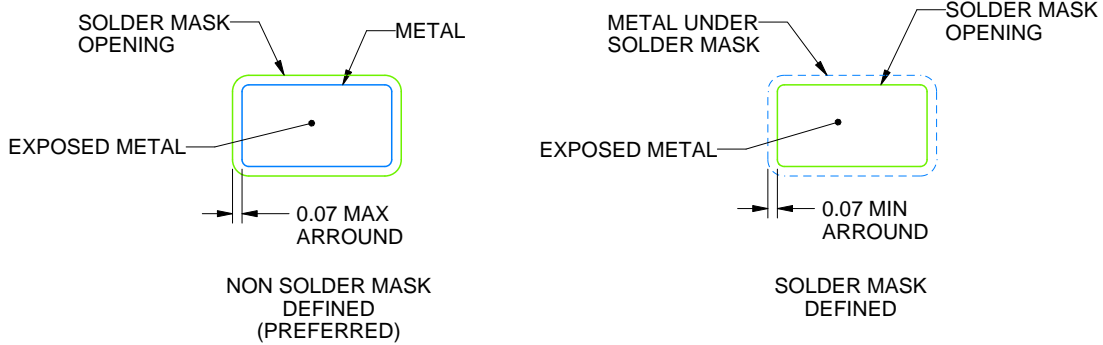
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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