具有折返式电流限制的 TLV741P 150mA 低压差稳压器

1 特性

- 输入电压范围：1.4V 至 5.5V
- 使用 1μF 陶瓷电容器实现稳定工作
- 折返过流保护
- 封装：
  - 5 引脚 SOT-23
  - 4 引脚 X2SON
- 超低压降：150mA 时为 230mV
- 准确度：1%
- 低 I_Q：50μA
- 可提供固定输出电压：1V 至 3.3V
- 高 PSRR：1kHz 时为 65dB
- 有源输出放电（仅限 P 版本）

2 应用

- 掌上电脑 (PDA) 和电池供电便携式设备
- MP3 播放器和其它手持产品
- 无线局域网 (WLAN) 及其他 PC 附加卡

3 说明

TLV741P 低压降线性稳压器 (LDO) 是一款低静态电流器件，具有出色的线路和负载瞬态性能，适用于功耗敏感型 应用。此器件提供了 1% 的典型精度。

TLV741P 旨在使用小型的 1μF 输出电容器实现稳定工作。

TLV741P 可在器件加电和使能期间提供浪涌电流控制。TLV741P 将输入电流限制为定义的电流限值，从而防止从输入电源流出的电流过大。该功能对于电池供电型器件尤为重要。

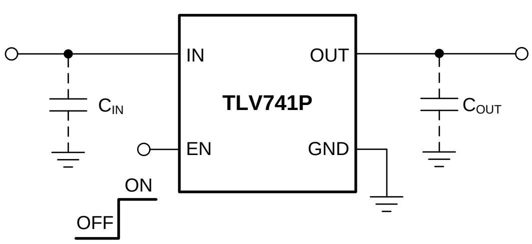
TLV741P 采用标准 DBV (SOT-23) 和 DQN (X2SON) 封装。TLV741P 提供了有源下拉电路，用于对输出负载进行快速放电。

器件信息[(1)]

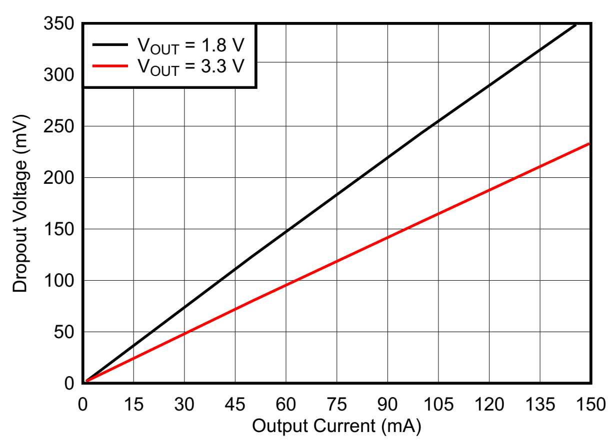
器件名称	封装	封装尺寸
TLV741P	SOT-23 (5)	2.90mm × 1.60mm
	X2SON (4)	1.00mm x 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

典型应用电路



压降电压与输出电流间的关系



目录

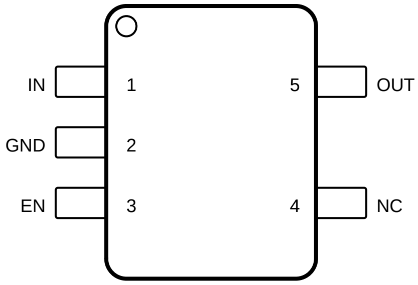
4 修订历史记录

Changes from Original (July 2017) to Revision A **Page**

- 已添加 在数据表中添加 DQN (X2SON) 封装 1

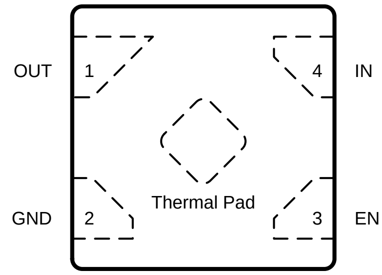
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

DQN Package
4-Pin X2SON With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. SOT-23	NO. X2SON		
EN	3	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	2	—	Ground pin
IN	1	4	I	Input pin. Use a small capacitor from this pin to ground. See the *Input and Output Capacitor Considerations* section for more details.
NC	4	—	—	No internal connection
OUT	5	1	O	Regulated output voltage pin. For best transient response, use a small 1-µF ceramic capacitor from this pin to ground. See the *Input and Output Capacitor Considerations* section for more details.
Thermal pad	—	—	—	The thermal pad is electrically connected to the GND node. Connect the thermal pad to the ground plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted). All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	V_{IN} + 0.3	
	Output, V_{OUT}	–0.3	3.6	
Current	Maximum output, $I_{OUT(max)}$	Internally limited		
Output short-circuit duration		Indefinite		
Total power dissipation	Continuous, $P_{D(tot)}$	See *Thermal Information*		
Temperature	Junction, T_J	–55	125	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.4		5.5	V
V_{EN}	Enable range	0		V_{IN}	V
I_{OUT}	Output current	0		150	mA
C_{IN}	Input capacitor	0	1		µF
C_{OUT}	Output capacitor	1		100	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV741P		UNIT
		DQN (X2SON)	DBV (SOT-23)	
		4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	249	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	210.4	172.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	174.7	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.2	49.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	174.5	75.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	140.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report

6.5 Electrical Characteristics

over operating temperature range T_J = –40°C to +125°C, $V_{IN(nom)} = V_{OUT(nom)}$ + 0.5 V or $V_{IN(nom)}$ = 2 V (whichever is greater), I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, and C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage range			1		3.3	V
	DC output accuracy	V_{OUT} ≥ 1.8 V T_J = 25°C		–1%		1%	
		V_{OUT} < 1.8 V T_J = 25°C		–20		20	mV
		V_{OUT} ≥ 1.2 V –40°C ≤ T_J ≤ 125°C		–1.5%		1.5%	
		V_{OUT} < 1.2 V –40°C ≤ T_J ≤ 125°C		–50		50	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	Maximum {$V_{OUT(nom)}$ + 0.5 V V_{IN} = 2 V} ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	30	mV
V_{DO}	Dropout voltage	V_{OUT} = 0.98 × $V_{OUT(nom)}$, T_J = –40°C to 85°C	1 V ≤ V_{OUT} < 1.8 V I_{OUT} = 150 mA		600	900	mV
			V_{OUT} = 1.1 V I_{OUT} = 100 mA		470	600	
			1.8 V ≤ V_{OUT} < 2.1 V I_{OUT} = 30 mA		70		
			1.8 V ≤ V_{OUT} < 2.1 V I_{OUT} = 150 mA		350	575	
			2.1 V ≤ V_{OUT} < 2.5 V I_{OUT} = 30 mA		90		
			2.1 V ≤ V_{OUT} < 2.5 V I_{OUT} = 150 mA		290	481	
			2.5 V ≤ V_{OUT} < 3 V I_{OUT} = 30 mA		50		
			2.5 V ≤ V_{OUT} < 3 V I_{OUT} = 150 mA		246	445	
			3 V ≤ V_{OUT} < 3.6 V I_{OUT} = 30 mA		46		
			3 V ≤ V_{OUT} < 3.6 V I_{OUT} = 150 mA		230	420	
		V_{OUT} = 0.98 × $V_{OUT(nom)}$ T_J = –40°C to 125°C	1 V ≤ V_{OUT} < 1.8 V I_{OUT} = 150 mA		600	1020	
			V_{OUT} = 1.1 V I_{OUT} = 100 mA		470	720	
			1.8 V ≤ V_{OUT} < 2.1 V I_{OUT} = 150 mA		350	695	
			2.1 V ≤ V_{OUT} < 2.5 V I_{OUT} = 150 mA		290	601	
			2.5 V ≤ V_{OUT} < 3 V I_{OUT} = 150 mA		246	565	
			3 V ≤ V_{OUT} < 3.6 V I_{OUT} = 150 mA		230	540	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			50	75	µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 5.5 V T_J = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V V_{OUT} = 2.8 V I_{OUT} = 30 mA	f = 100 Hz		70		dB
			f = 10 kHz		55		
			f = 1 MHz		55		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz V_{IN} = 2.3 V V_{OUT} = 1.8 V I_{OUT} = 10 mA			73		μV_{RMS}
t_{STR}	Start-up time(1)	C_{OUT} = 1 µF I_{OUT} = 150 mA			100		µs

(1) Start-up time is the time from EN assertion to (0.98 × $V_{OUT(nom)}$).

Electrical Characteristics (continued)

over operating temperature range T_J = –40°C to +125°C, $V_{IN(nom)}$ = $V_{OUT(nom)}$ + 0.5 V or $V_{IN(nom)}$ = 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HI}	Enable high (enabled)		0.9		V_{IN}	V
V_{LO}	Enable low (disabled)		0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V		0.01		µA
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 4 V		120		Ω
I_{LIM}	Output current limit	V_{IN} = 3.8 V V_{OUT} = 3.3 V T_J = –40 to 85°C	180			mA
		V_{IN} = 2.25 V V_{OUT} = 1.8 V T_J = –40 to 85°C	180			
		V_{IN} = 2 V V_{OUT} = 1.2 V T_J = –40 to 85°C	180			
I_{SC}	Short-circuit current	V_{OUT} = 0 V		40		mA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		158		°C
		Reset, temperature decreasing		140		

6.6 Typical Characteristics

over operating temperature range T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

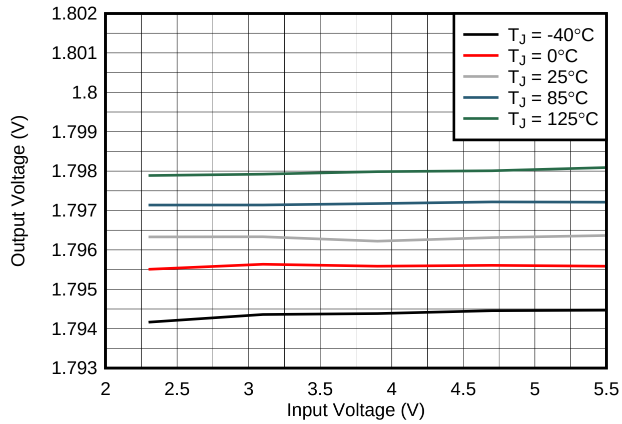


图 1. 1.8-V Line Regulation vs V_{IN} and Temperature

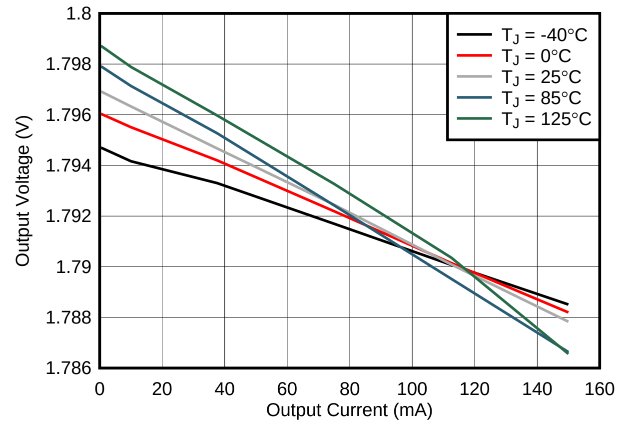


图 2. 1.8-V Load Regulation vs I_{OUT} and Temperature

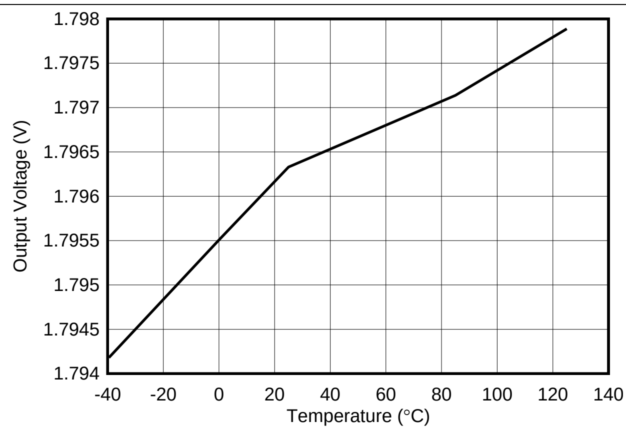


图 3. 1.8-V Output Voltage Over Temperature

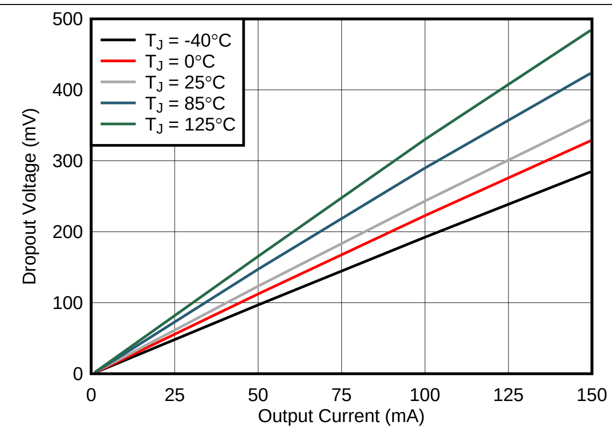


图 4. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

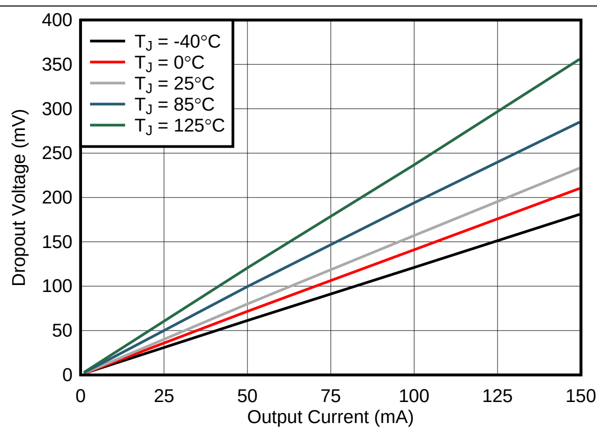


图 5. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

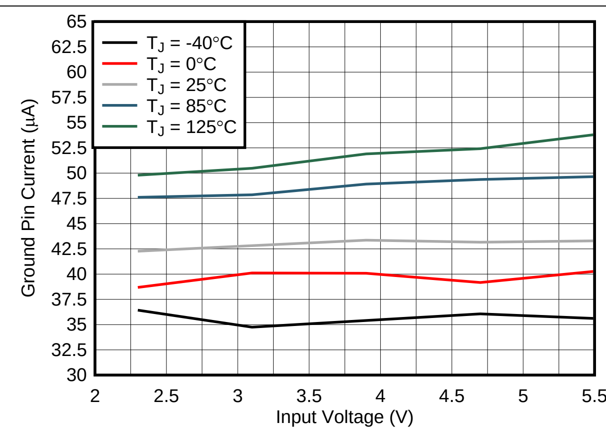


图 6. Ground Pin Current vs V_{IN} and Temperature

Typical Characteristics (接下页)

over operating temperature range T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

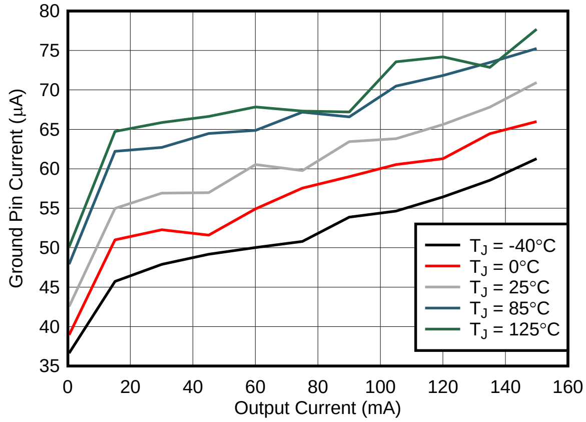


图 7. Ground Pin Current vs I_{OUT} and Temperature

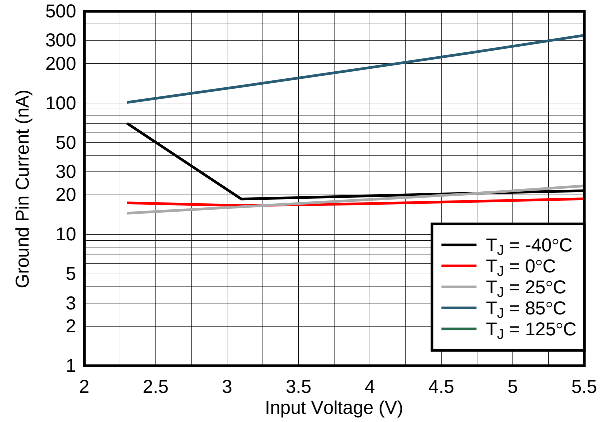


图 8. Shutdown Current vs V_{IN} and Temperature

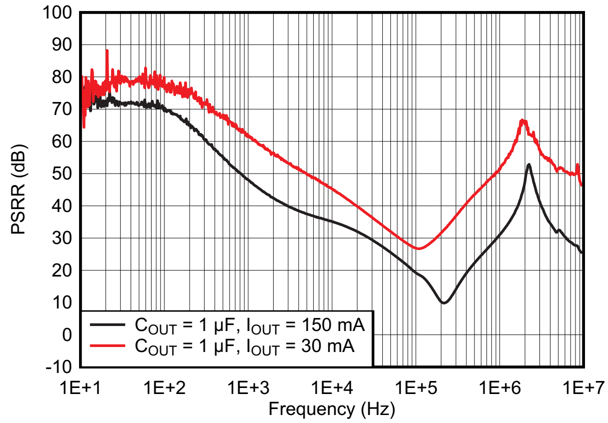


图 9. Power-Supply Rejection Ratio Over C_{OUT}

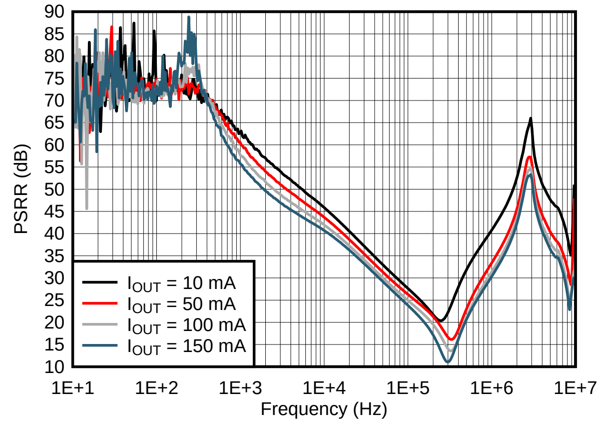
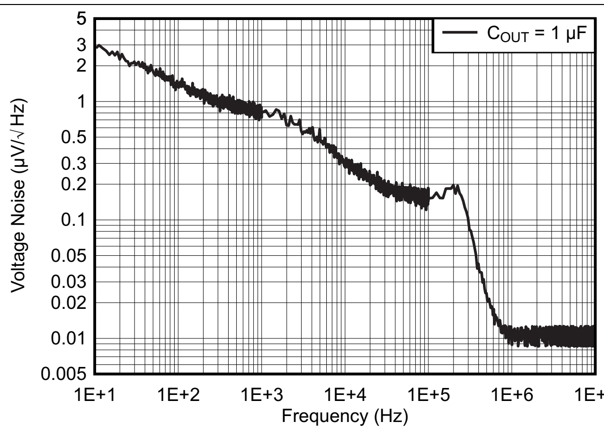
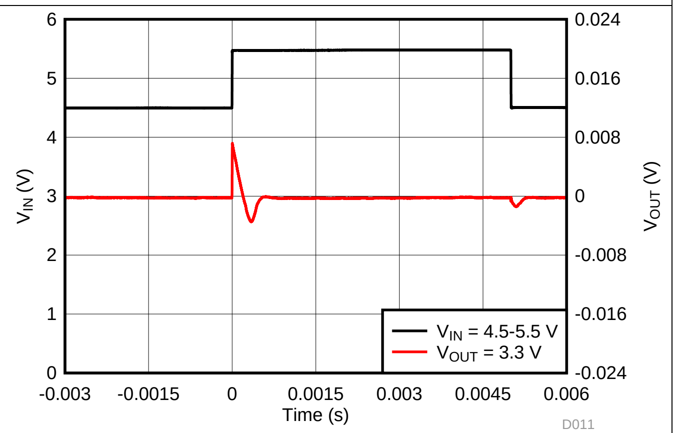


图 10. Power-Supply Rejection Ratio Over I_{OUT}



C_{OUT} = 1 µF

图 11. Output Spectral Noise Density

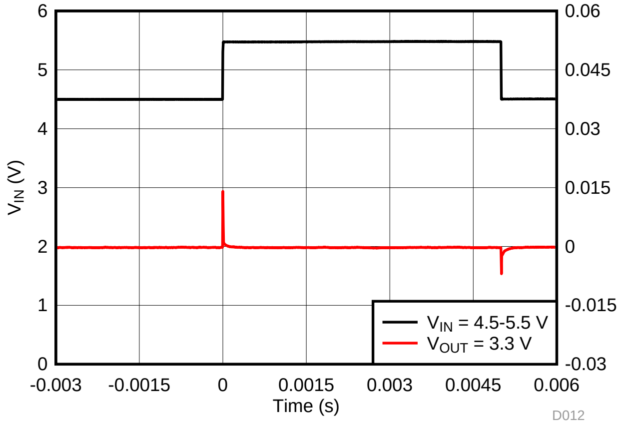


I_{OUT} = 0 mA

图 12. Line Transient

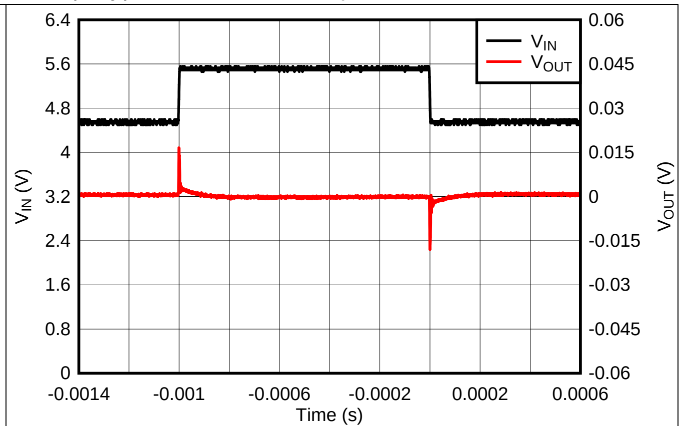
Typical Characteristics (接下页)

over operating temperature range T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V (unless otherwise noted). Typical values are at T_J = 25°C.



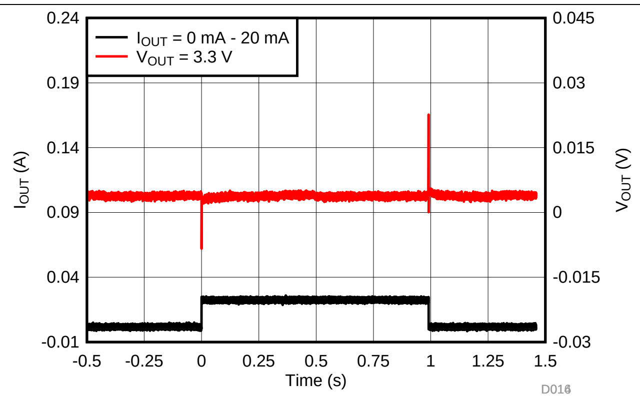
I_{OUT} = 1 mA

图 13. Line Transient



I_{OUT} = 150 mA

图 14. Line Transient



I_{OUT} = 0 mA - 20 mA V_{OUT} = 3.3 V

图 15. Load Transient

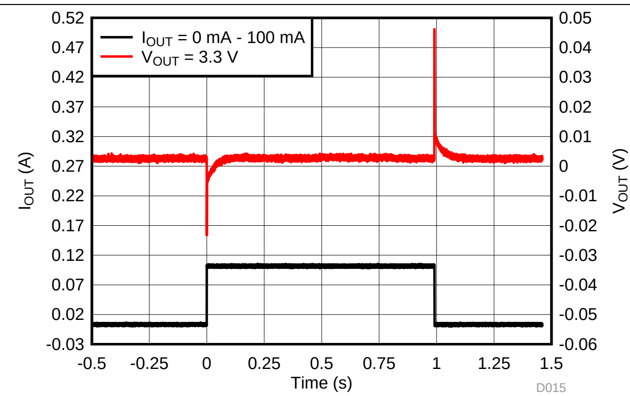
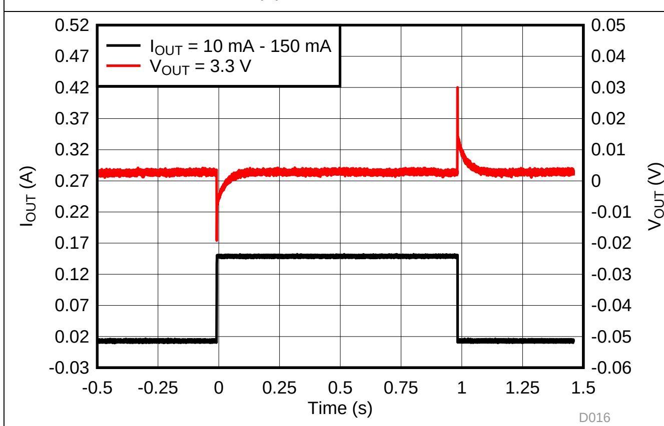
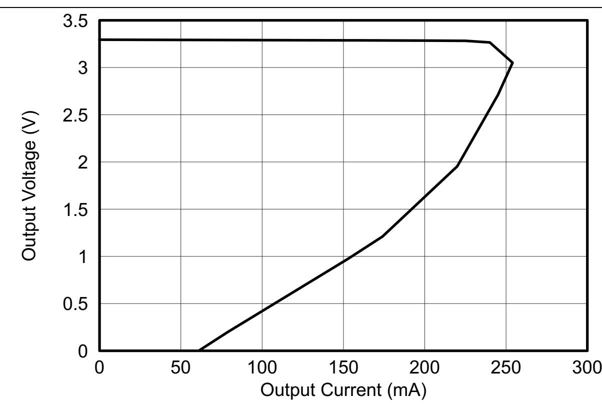


图 16. Load Transient



I_{OUT} = 10 mA - 150 mA V_{OUT} = 3.3 V

图 17. Load Transient

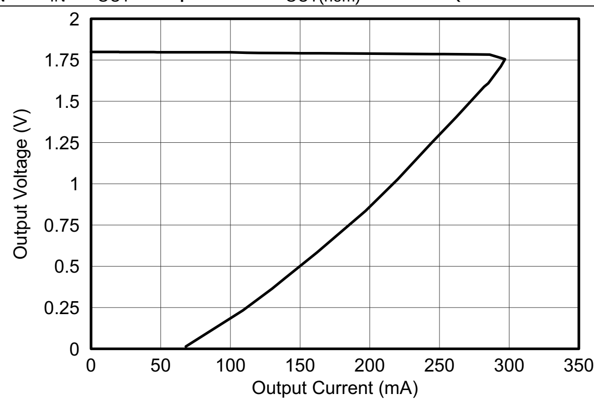


TLV74133P

图 18. 3.3-V Output Voltage vs Output Current (Foldback Current Limit)

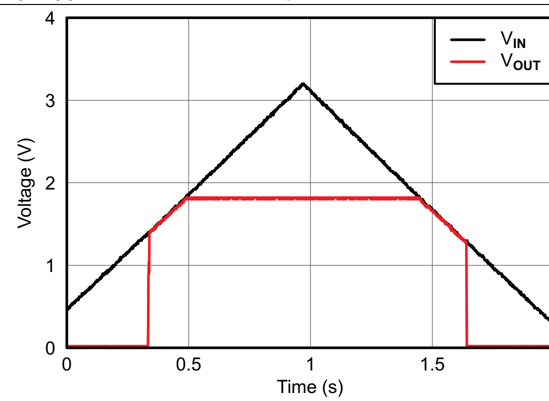
Typical Characteristics (接下页)

over operating temperature range T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V (unless otherwise noted). Typical values are at T_J = 25°C.



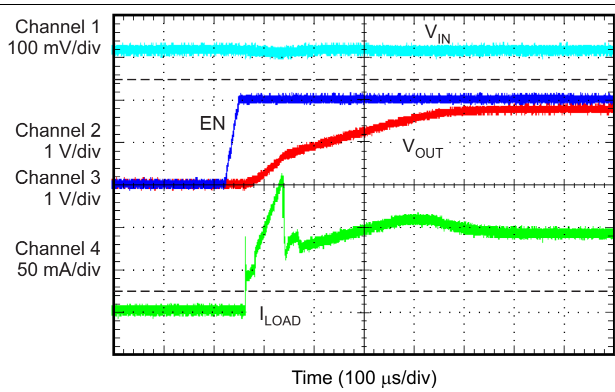
TLV74118P

图 19. 1.8-V Output Voltage vs Output Current (Foldback Current Limit)



TLV74118P I_{OUT} = 150 mA

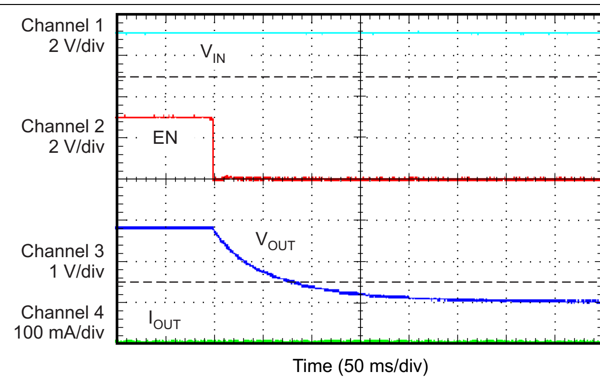
图 20. V_{IN} Power-Up and Power-Down



V_{IN} = 2.3 V V_{OUT} = 1.8 V C_{IN} = 1 µF

C_{OUT} = 10 µF I_{OUT} = 90 mA TLV74118P from design

图 21. Start-Up With EN



V_{IN} = 3 V V_{OUT} = 1.8 V C_{IN} = C_{OUT} = 1 µF

TPS74118P No load

图 22. Shutdown Response With Enable

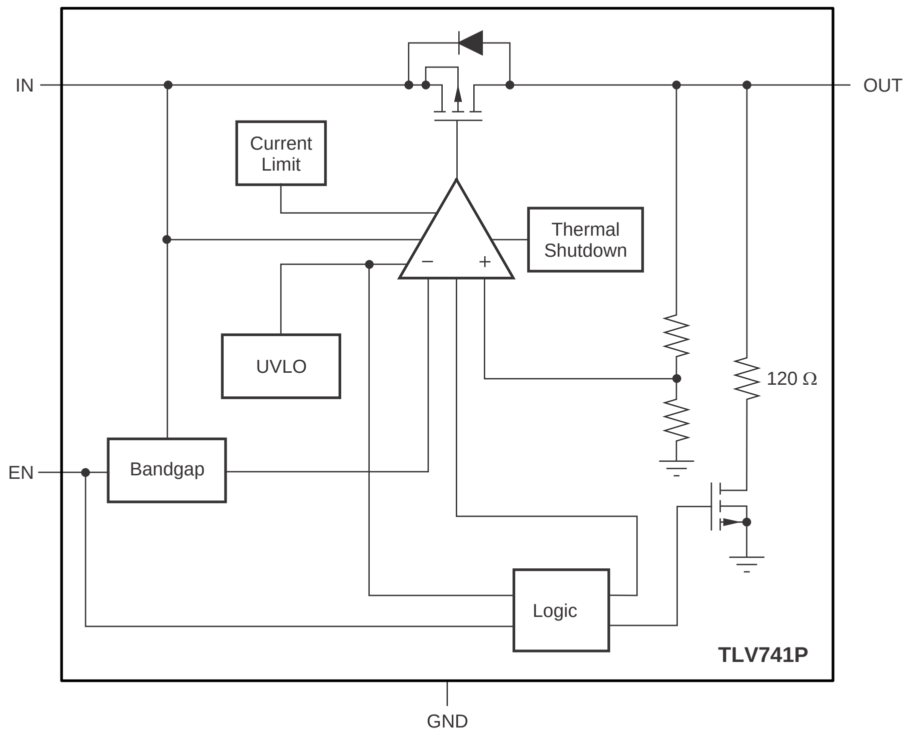
7 Detailed Description

7.1 Overview

The TLV741P belongs to a new family of next-generation value low-dropout (LDO) regulators. The TLV741P consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom makes the device suitable for RF portable applications.

This regulator offers current limit and thermal protection. Device operating junction temperature is –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV741P uses a UVLO circuit that disables the output until the input voltage is greater than the rising UVLO voltage. The circuit makes sure that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$. During UVLO disable, the output of the TLV741P version is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V. If shutdown capability is not required, connect EN to IN.

The TLV741P has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in 公式 1.

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \tag{1}$$

7.3.3 Foldback Current Limit

The TLV741P has an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device is gradually reduced while the output voltage decreases. When the output shorts, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is calculated by 公式 2:

$$V_{OUT} = I_{LIMIT} \times R_{LOAD} \tag{2}$$

The PMOS pass transistor dissipates [(V_{IN} – V_{OUT}) × I_{LIMIT}] until thermal shutdown is triggered and the device turns off. The internal thermal shutdown circuit turns on the device during cool down. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Protection* for more details.

The TLV741P PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, TI recommends externally limiting the rated output current to 5%.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, which protects the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV741P internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TLV741P into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

表 1 lists conditions that result in different operating modes.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158°C$

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Considerations

The TLV741P uses an advanced internal control loop to obtain stable operation by using an input or output capacitor. An output capacitance of 1 µF or larger generally provides good dynamic response. TI recommends using X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. TI recommends using an input capacitor if the source impedance is more than 0.5 Ω. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

The TLV741P uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

8.1.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2 Typical Application

Several versions of the TLV741P are suitable for powering the MSP430 microcontroller.

图 23 shows a diagram of the TLV741P powering an MSP430 microcontroller. 表 2 lists potential applications of some voltage versions.

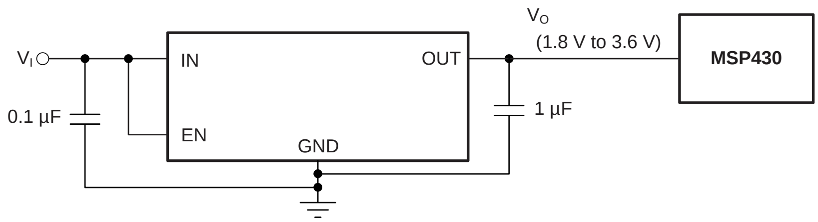


图 23. TLV741P Powering a Microcontroller

表 2. Typical MSP430 Applications

DEVICE	V_{OUT} (TYPICAL)	APPLICATION
TLV741P18P	1.8 V	Allows for lowest power consumption with many MSP430s
TLV741P25P	2.5 V	2.2-V supply required by many MSP430s for flash programming and erasing

8.2.1 Design Requirements

表 3 lists the design requirements.

表 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, ±1%
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

An input capacitor is not required for this design because of the low impedance connection directly to the battery.

A small output capacitor allows for the minimal possible inrush current during start-up, and makes sure that the 180-mA maximum input current limit is not exceeded.

See 图 29 to verify that the maximum junction temperature is not exceeded.

8.2.3 Application Curves

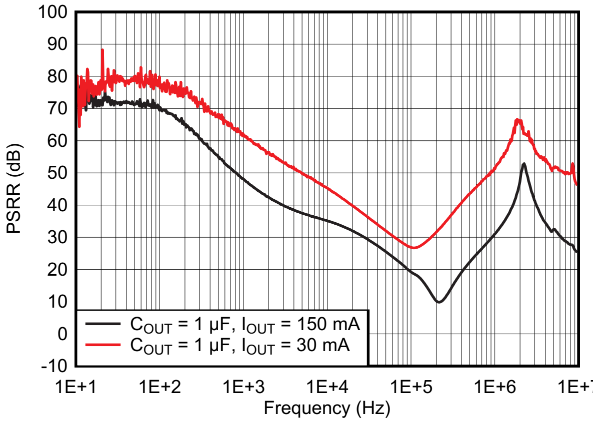
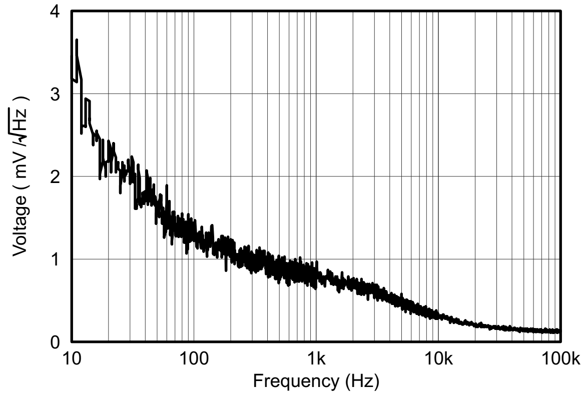
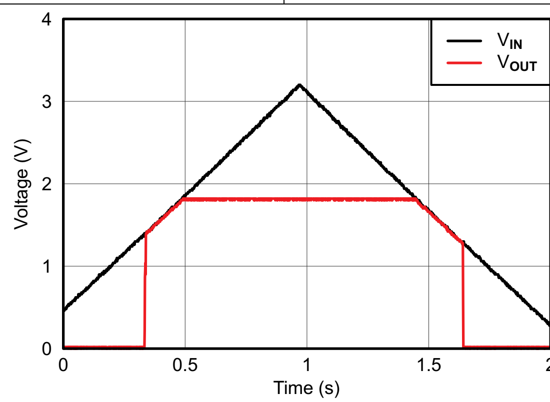


图 24. Power-Supply Rejection Ratio vs Frequency



V_{OUT} = 1.8 V I_{OUT} = 10 mA

图 25. Output Spectral Noise Density



I_{OUT} = 150 mA

图 26. V_{IN}Power Up and Power Down

8.3 What to Do and What Not to Do

Place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator for best transient performance.

Place at least one 1-µF capacitor as close as possible to the IN pin for best transient performance.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not continuously operate the device in current limit or near thermal shutdown.

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range from 1.4 V to 5.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

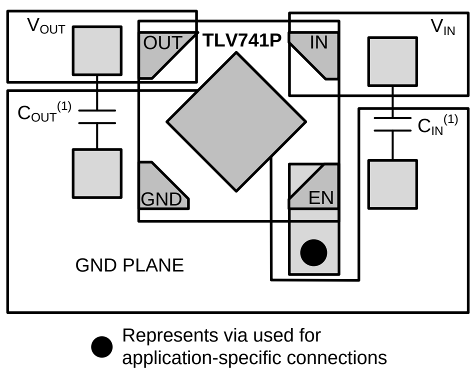
10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve AC performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High-ESR capacitors may degrade PSRR performance.

10.2 Layout Examples



(1) Not required.

图 27. X2SON Layout Example

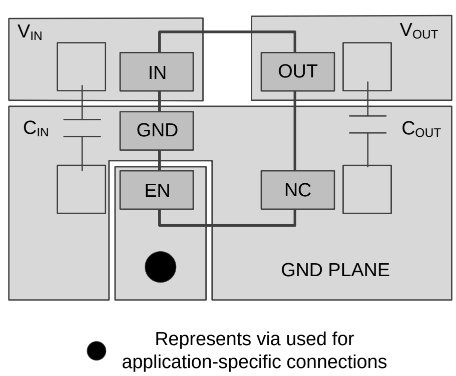


图 28. SOT-23 Layout Example

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in **Thermal Information**. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in 公式 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{3}$$

图 29 shows the maximum ambient temperature versus the power dissipation of the TLV741P. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to make sure the TLV741P does not operate above a junction temperature of 125°C.

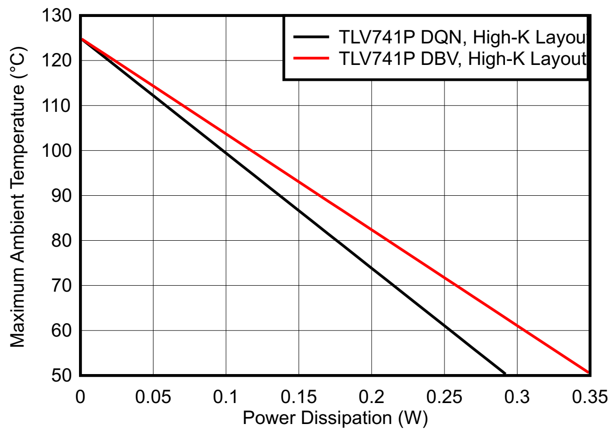


图 29. Maximum Ambient Temperature vs Device Power Dissipation

Estimate junction temperature by using the Ψ_{JT} and Ψ_{JB} thermal metrics, shown in*Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with 公式 4:

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

- P_D is the power dissipation shown by 公式 3,
- T_T is the temperature at the center-top of the device package,
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface. (4)

注

Both T_T and T_B can be measured on actual application boards using a thermogun (an infrared thermometer).

For more information about measuring T_T and T_B, see *Using New Thermal Metrics* , available for download at www.ti.com.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

通用低压降 (LDO) 线性稳压器 EVM 用户指南

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV741105PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1NFT
TLV741105PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NFT
TLV74110PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1C9T
TLV74110PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C9T
TLV74110PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8T
TLV74110PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8T
TLV74111PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1DHT
TLV74111PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1DHT
TLV74111PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8R
TLV74111PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8R
TLV74112PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1DIT
TLV74112PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1DIT
TLV74112PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8Q
TLV74112PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8Q
TLV74115PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	1DJT
TLV74115PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1DJT
TLV74115PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8P
TLV74115PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8P
TLV74118PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	1DKT
TLV74118PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DKT
TLV74118PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8O
TLV74118PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8O
TLV74125PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	1DLT
TLV74125PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DLT
TLV74125PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8N
TLV74125PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8N
TLV741285PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	1DMT
TLV741285PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DMT
TLV741285PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV741285PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8M
TLV74128PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	1DNT
TLV74128PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DNT
TLV74128PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8L
TLV74128PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8L
TLV74130PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	1DOT
TLV74130PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DOT
TLV74130PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8K
TLV74130PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8K
TLV74133PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	1CAT
TLV74133PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1CAT
TLV74133PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8J
TLV74133PDQNR.B	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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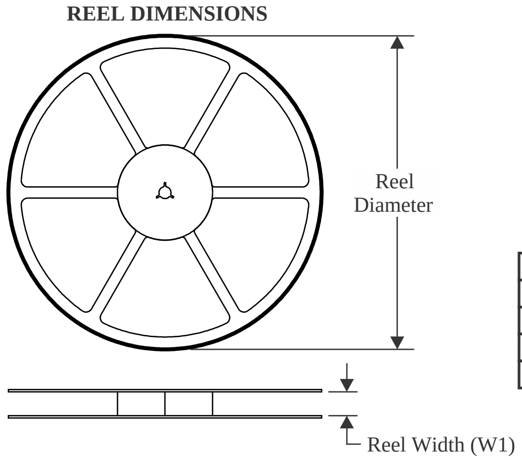
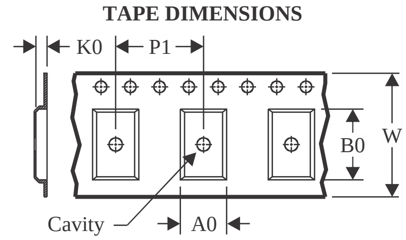
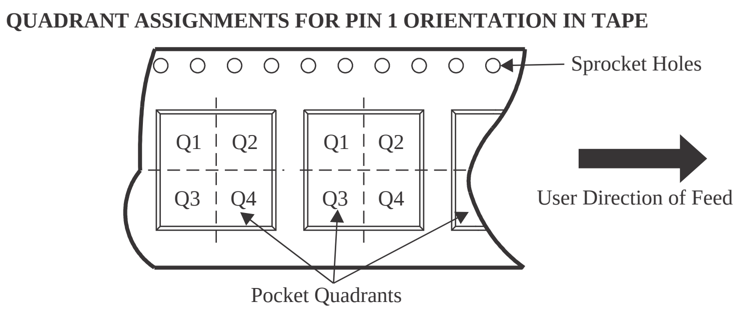
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

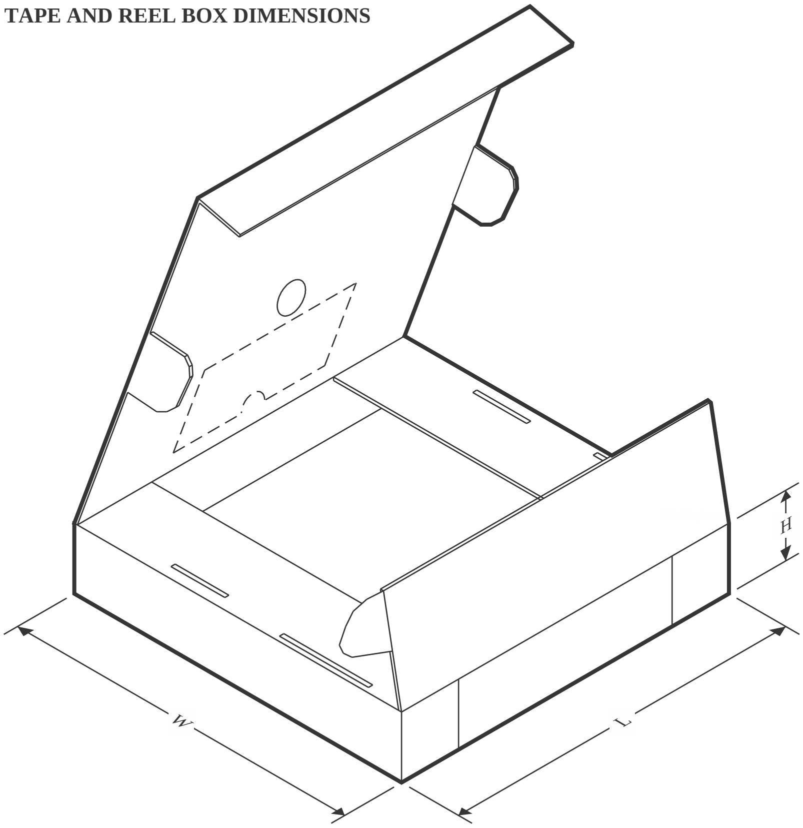


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV741105PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74110PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74110PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74111PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74111PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74112PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74112PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74115PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74115PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74118PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74118PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74125PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74125PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV741285PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV741285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74128PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74128PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74130PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74130PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74133PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74133PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV74133PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

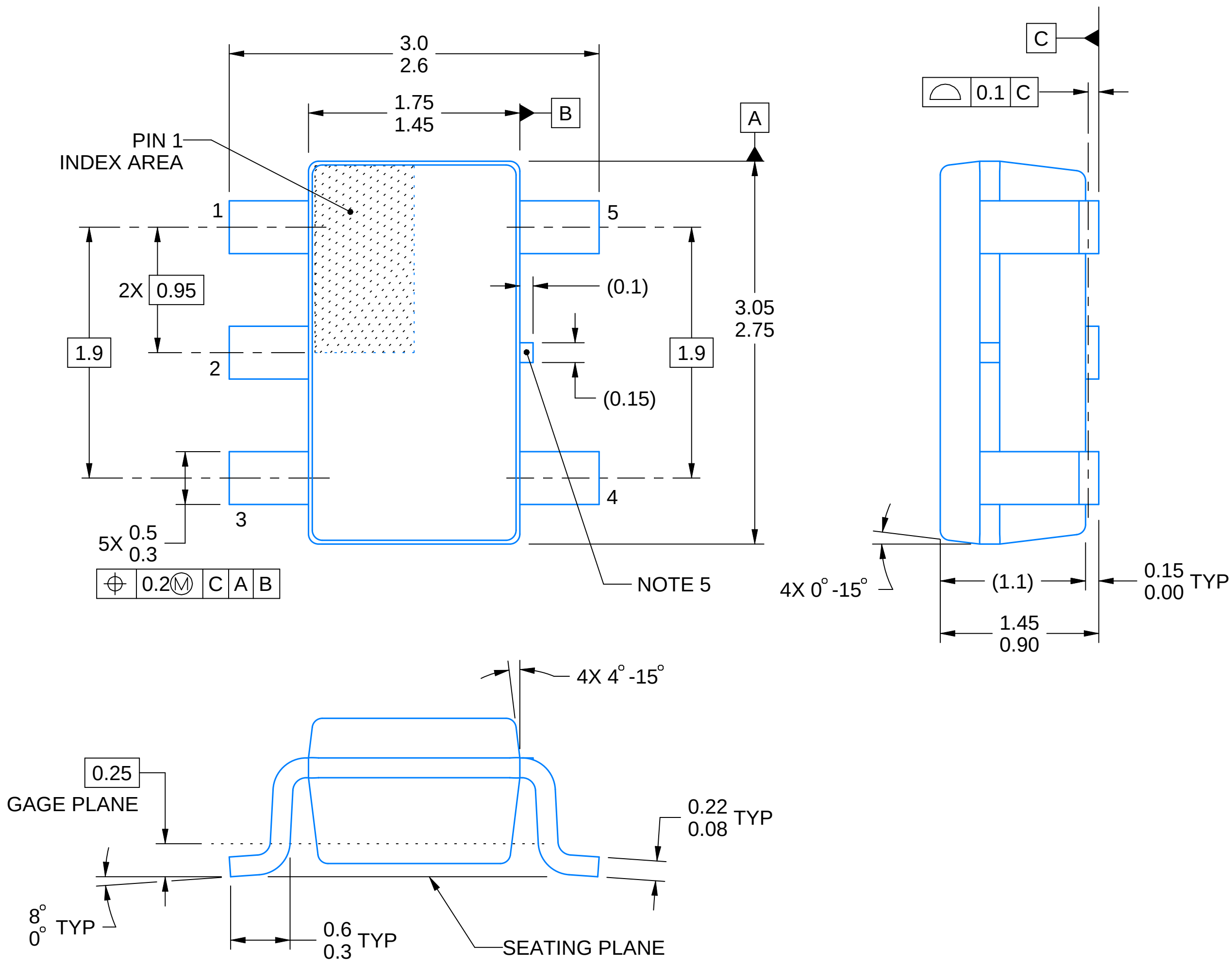
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV741105PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74110PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74110PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74111PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74111PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74112PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74112PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74115PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74115PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74118PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV74118PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74125PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV74125PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV741285PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV741285PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74128PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74128PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74130PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

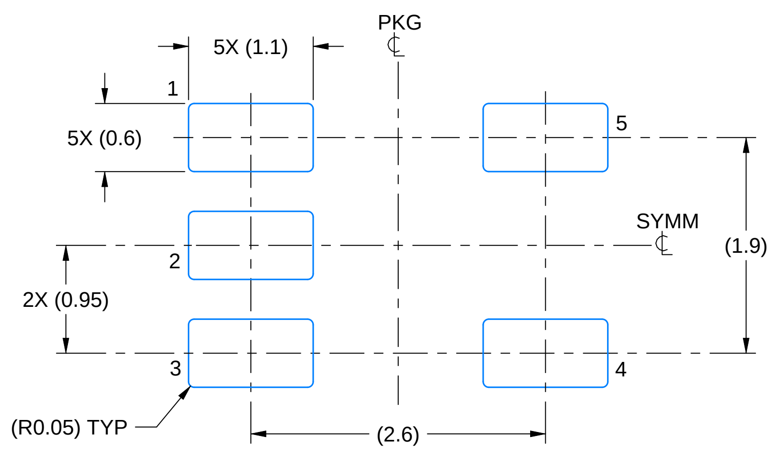
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74130PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74133PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV74133PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV74133PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0



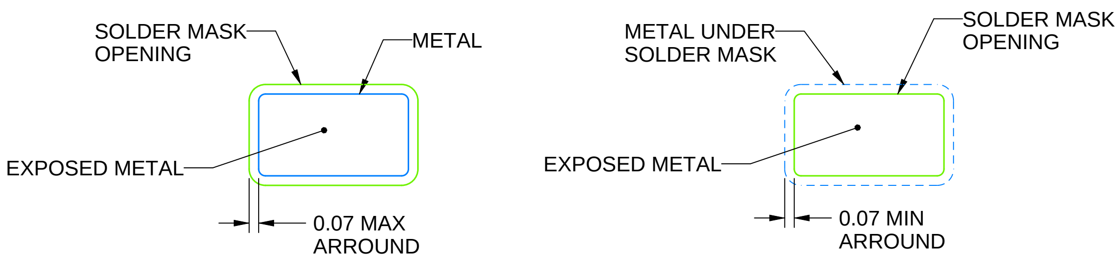
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

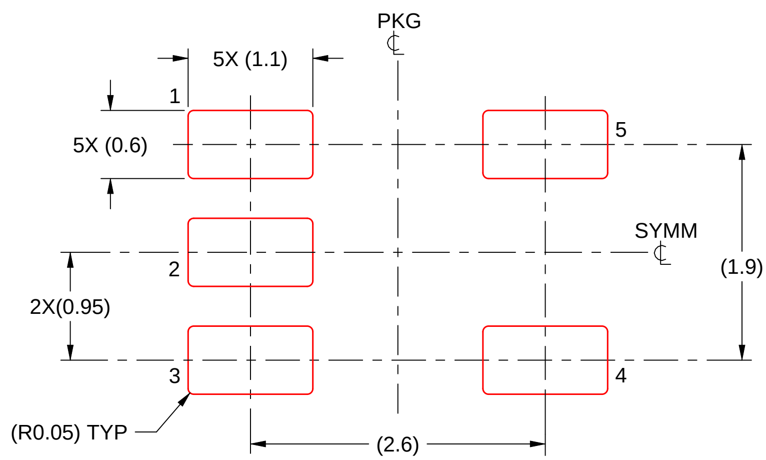
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

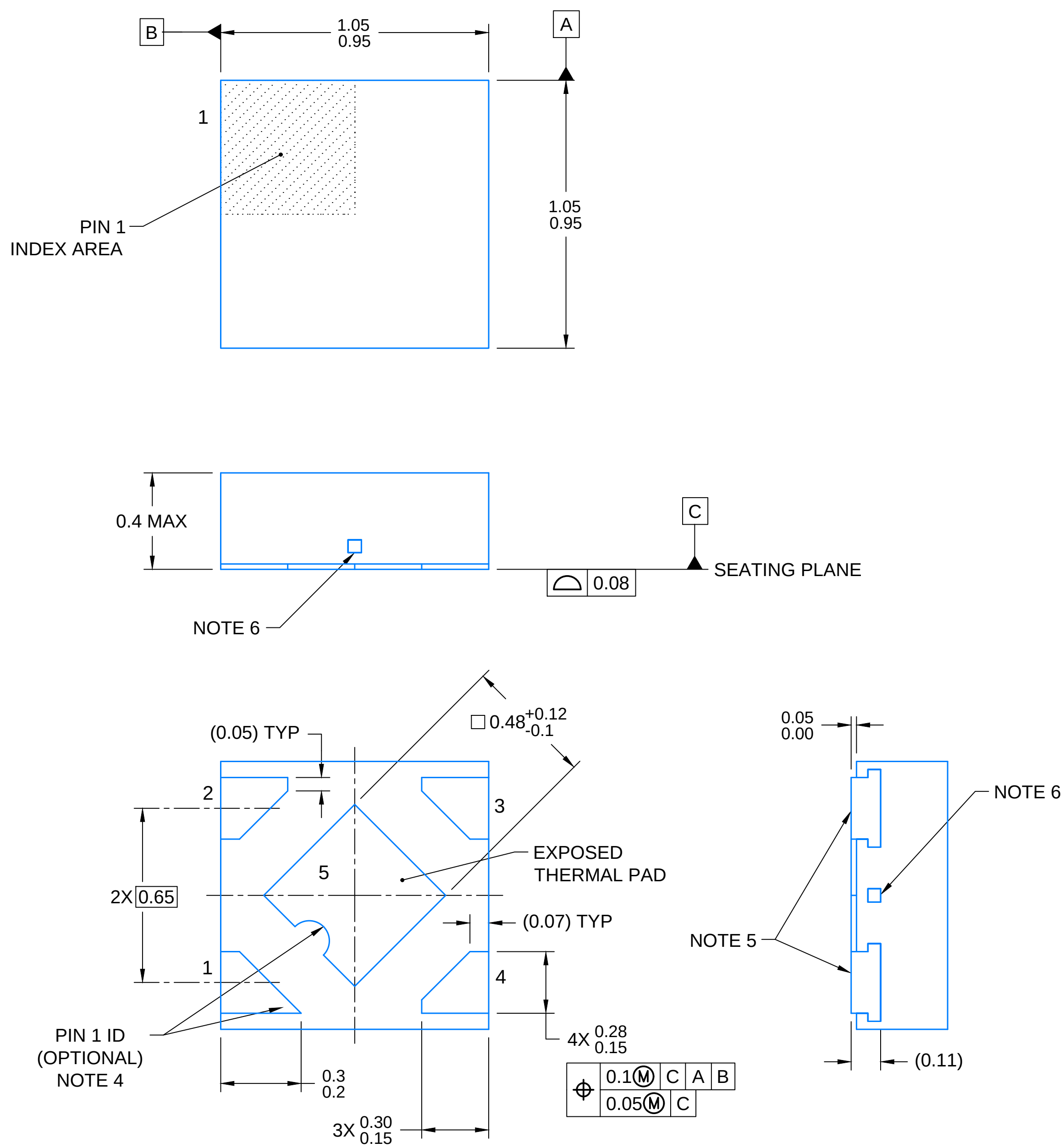
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

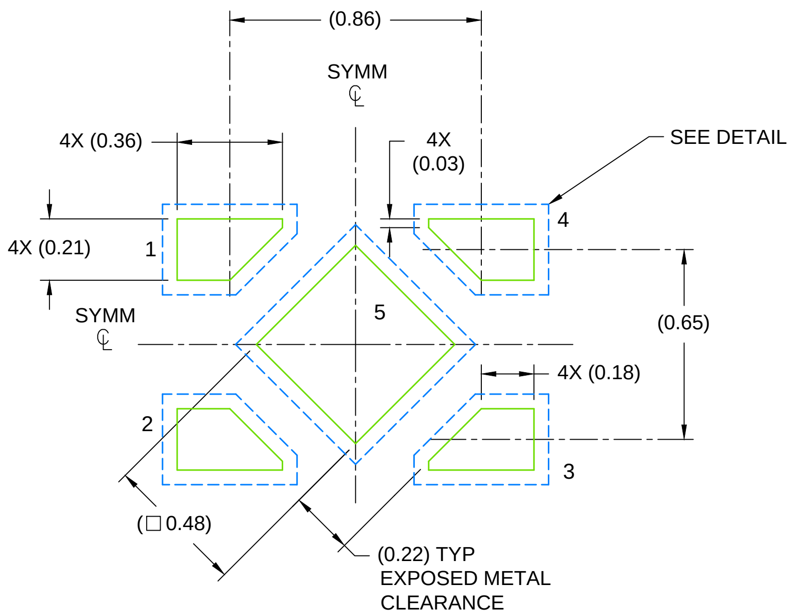
4210367/F



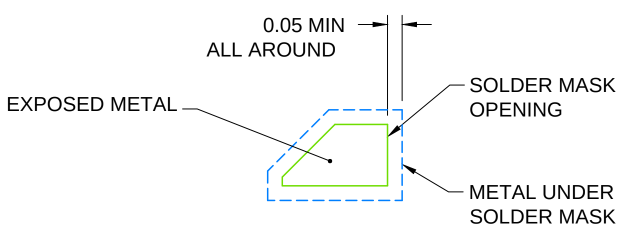
4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X



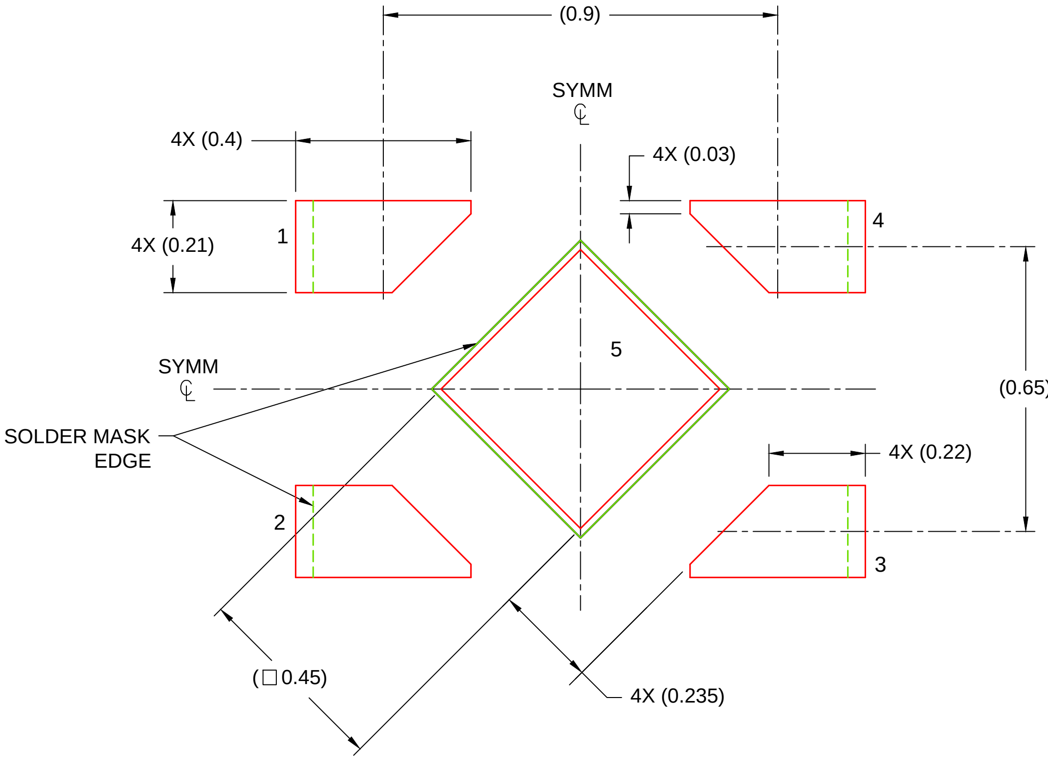
SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明