

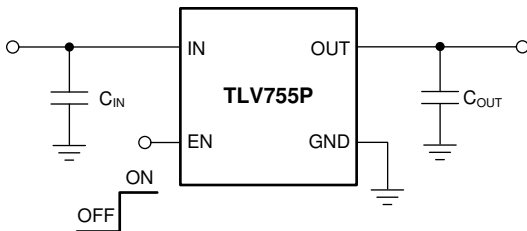
## TLV755P 500mA、低 $I_Q$ 、小型、低压降稳压器

### 1 特性

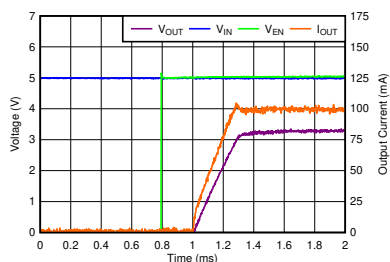
- 采用 SOT-23-5 封装，具有  $60.3^{\circ}\text{C}/\text{W}$   $R_{\theta JA}$
- 输入电压范围：1.45V 至 5.5V
- 低  $I_Q$ ：25  $\mu\text{A}$  (典型值)
- 低压降：
  - 在 500mA 下为 238mV (最大值) ( $V_{OUT}$  为 3.3V)
- 输出精度：1% (85°C 时为最大值)
- 内置软启动功能，具有单调  $V_{OUT}$  上升
- 折返电流限制
- 有源输出放电
- 高 PSRR：100kHz 时为 46dB
- 与 1 $\mu\text{F}$  的陶瓷输出电容器搭配使用时可保持稳定
- 封装：
  - 2.9mm  $\times$  2.8mm SOT-23-5 (DBV)
  - 带有散热焊盘的 2.9mm  $\times$  2.8mm SOT-23-5 (DYD)
  - 1mm  $\times$  1mm X2SON-4 (DQN)
  - 2mm  $\times$  2mm WSON-6 (DRV)

### 2 应用

- 机顶盒、电视和游戏机
- 便携式和电池供电类设备
- 台式机、笔记本电脑和超极本
- 平板电脑和遥控器
- 白色家电和电器
- 电网基础设施和保护继电器
- 摄像头模块和图像传感器



典型应用



启动波形

### 3 说明

TLV755P 是一款超小型低静态电流、低压差稳压器 (LDO)，可提供 500mA 拉电流，具有良好的线路和负载瞬态性能。TLV755P 经过优化，可支持 1.45V 至 5.5V 的输入电压范围，可适用于各种应用。为更大限度地缩减成本和解决方案尺寸，该器件可在 0.6V 至 5V 范围内提供固定输出电压，以支持现代微控制器 (MCU) 更低的内核电压。此外，TLV755P 具备带有使能功能的低  $I_Q$ ，从而可将待机功耗降至最低。此器件具有内部软启动功能，旨在降低浪涌电流，因此可为负载提供受控电压并在启动过程中最大限度地降低输入电压压降。关断时，该器件可主动下拉输出以使输出快速放电并实现已知的启动状态。

TLV755P 在与支持小尺寸总体解决方案的小型陶瓷输出电容器搭配使用时，可保持稳定。高精度带隙与误差放大器支持 1% 的典型精度。所有器件版本均具有集成的热关断保护、电流限制和低压锁定 (UVLO) 功能。TLV755P 具有内部折返电流限制，有助于在发生短路时减少热耗散。

TLV755 采用常见的 WSON、X2SON 和 SOT23-5 (DRV、DQN 和 DBV) 封装。该器件还提供带有散热焊盘的热增强型 SOT23-5 (DYD) 封装，与标准 SOT23-5 封装相比，热阻显著降低。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
TLV755P	DQN (X2SON, 4)	1mm $\times$ 1mm
	DBV (SOT-23, 5)	2.9mm $\times$ 2.8mm
	DYD (SOT-23, 5)	2.9mm $\times$ 2.8mm
	DRV (WSON, 6)	2mm $\times$ 2mm

- (1) 如需更多信息，请参阅 [机械、封装和可订购信息](#)。
- (2) 封装尺寸 (长  $\times$  宽) 为标称值，并包括引脚 (如适用)。



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## 4 Pin Configuration and Functions

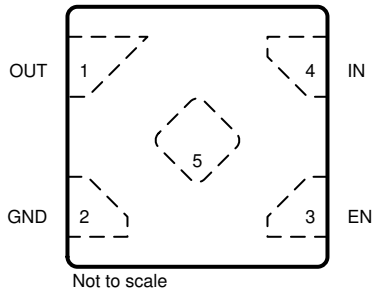


图 4-1. DQN Package, 4-Pin X2SON (Top View)

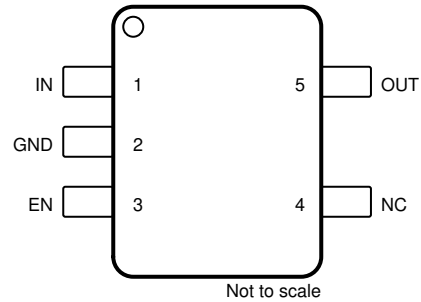


图 4-2. DBV Package, 5-Pin SOT-23 (Top View)

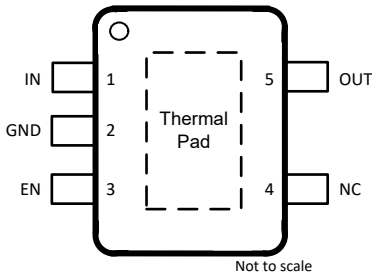


图 4-3. DYD Package, 5-Pin SOT-23 With Exposed Thermal Pad (Top View)

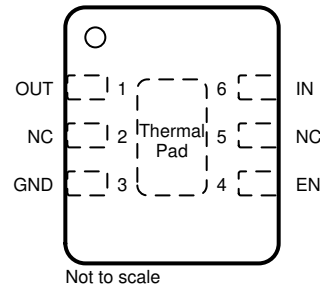


图 4-4. DRV Package, 6-Pin WSON With Exposed Thermal Pad (Top View)  
NC = no internal connection.

表 4-1. Pin Functions

NAME	PIN				TYPE <sup>(2)</sup>	DESCRIPTION
	DQN	DBV	DYD	DRV		
EN	3	3	3	4	I	Enable pin. Drive EN greater than $V_{HI}$ to turn on the regulator. Drive EN less than $V_{LO}$ to place the low-dropout regulator (LDO) into shutdown mode.
GND	2	2	2	3	—	Ground pin.
IN	4	1	1	6	I	Input pin. A capacitor with a value of $1\mu F$ or larger is required from this pin to ground. <sup>(1)</sup> See the <a href="#">Input and Output Capacitor Selection</a> section for more information.
NC	—	4	4	2, 5	—	No internal connection.
OUT	1	5	5	1	O	Regulated output voltage pin. A capacitor with a value of $1\mu F$ or larger is required from this pin to ground. <sup>(1)</sup> See the <a href="#">Input and Output Capacitor Selection</a> section for more information.
Thermal pad	Pad	—	Pad	Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

(1) Make sure the nominal input and output capacitance is greater than  $0.47\mu F$ . Throughout this document the nominal derating on these capacitors is 50%. Make sure the effective capacitance at the pin is greater than  $0.47\mu F$ .

(2) I = Input; O = Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{IN}$	-0.3	6.0	V
Enable voltage, $V_{EN}$	-0.3	6.0	V
Output voltage, $V_{OUT}$	-0.3	$V_{IN} + 0.3$ <sup>(2)</sup>	V
Operating junction temperature $T_J$	-40	150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The absolute maximum rating is  $V_{IN} + 0.3$  V or 6.0 V, whichever is smaller.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	1.45		5.5	V
$V_{OUT}$	Output voltage	0.6		5.0	V
$V_{EN}$	Enable voltage	0		5.5	V
$I_{OUT}$	Output current	0		500	mA
$C_{IN}$	Input capacitor	1			μF
$C_{OUT}$	Output capacitor	1		200	μF
$f_{EN}$	Enable toggle frequency			10	kHz
$T_J$	Junction temperature	-40		125	°C

## 5.4 Thermal Information

PCB	THERMAL METRIC <sup>(1) (2)</sup>		TLV755				UNIT
			DYD (SOT-23-5)	DQN (X2SON)	DBV (SOT-23-5)	DRV (WSON)	
			5 PINS	4 PINS	5 PINS	6 PINS	
EVM	$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.3	N/A	100.8	N/A	°C/W
	$\psi_{JT}$	Junction-to-top characterization parameter	14.2	N/A	23.3	N/A	
	$\psi_{JB}$	Junction-to-board characterization parameter	35.9	N/A	67.8	N/A	
JEDEC	$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	168.4	231.1	100.2	°C/W
	$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.8	139.1	118.4	108.5	
	$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	101.4	64.4	64.3	
	$\psi_{JT}$	Junction-to-top characterization parameter	16.7	5.6	28.4	10.4	
	$\psi_{JB}$	Junction-to-board characterization parameter	44.9	101.7	63.8	64.8	
	$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	34.3	88.4	N/A	34.7	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) JEDEC thermal metrics apply to JEDEC standard PCB (2s2p, no vias to internal plane and bottom layer). EVM metrics apply to the LP087A EVM with an exposed pad SOT-23-5 (DYD) layout.

## 5.5 Electrical Characteristics

at operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$  or  $2.0\text{V}$  (whichever is greater),  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted); all typical values at  $T_J = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$V_{IN}$	Input voltage	1.45		5.5	V		
$V_{OUT}$	Output voltage	0.6		5.0	V		
Output accuracy	$-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$ , DBV and DRV package	-1		1	%		
	$V_{OUT} \geq 1.0\text{V}$ , DQN package	-1.2		1.2	%		
	$-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$ ; $0.6\text{V} \leq V_{OUT} < 1.0\text{V}$	-10		10	mV		
	$V_{OUT} \geq 1\text{V}$	-1.5		1.5	%		
	$0.6\text{V} \leq V_{OUT} < 1\text{V}$	-15		15	mV		
$(\Delta V_{OUT}) / \Delta V_{IN}$	Line regulation	$V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $V_{OUT} > 1.5\text{V}$		2	mV		
$\Delta V_{OUT} / \Delta I_{OUT}$	Load regulation	$0.1\text{mA} \leq I_{OUT} \leq 500\text{mA}$	DQN package	0.036	V/A		
			DBV and DYD packages	0.060			
			DRV package	0.044			
$I_{GND}$	Ground current	$T_J = 25^{\circ}\text{C}$ , $I_{OUT} = 0\text{mA}$		14	25	31	$\mu\text{A}$
		$-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$ , $I_{OUT} = 0\text{mA}$				33	
		$-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$ , $I_{OUT} = 0\text{mA}$				40	
$I_{SHDN}$	Shutdown current	$V_{EN} \leq 0.4\text{V}$ , $1.4\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$		0.1	1	$\mu\text{A}$	
$I_{CL}$	Output current limit	$V_{IN} = V_{OUT} + V_{DO(MAX)} + 0.25\text{V}$	$V_{OUT} = V_{OUT} - 0.2\text{V}$ , $V_{OUT} \leq 1.5\text{V}$	560	720	865	mA
			$V_{OUT} = 0.9 \times V_{OUT}$ , $1.5\text{V} < V_{OUT} \leq 4.5\text{V}$	560	720	865	
$I_{SC}$	Short-circuit current limit	$V_{OUT} = 0\text{V}$		355		mA	

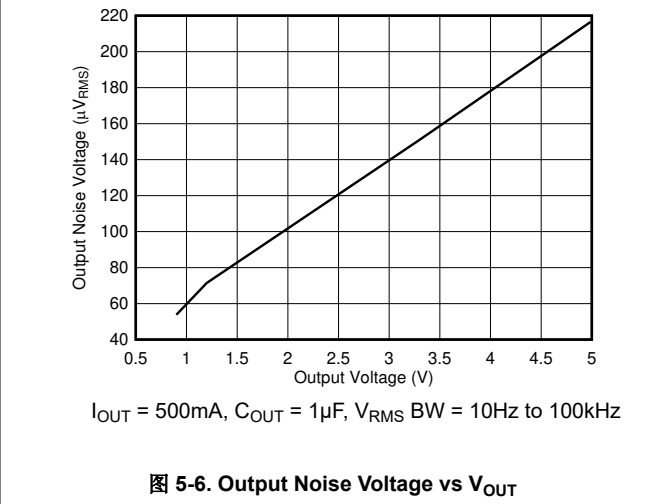
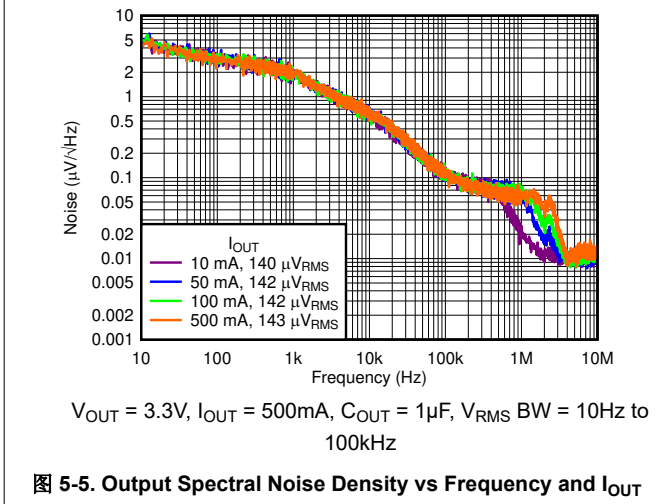
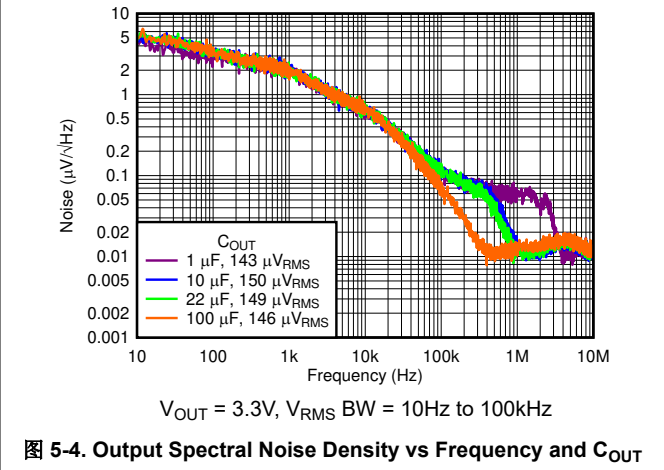
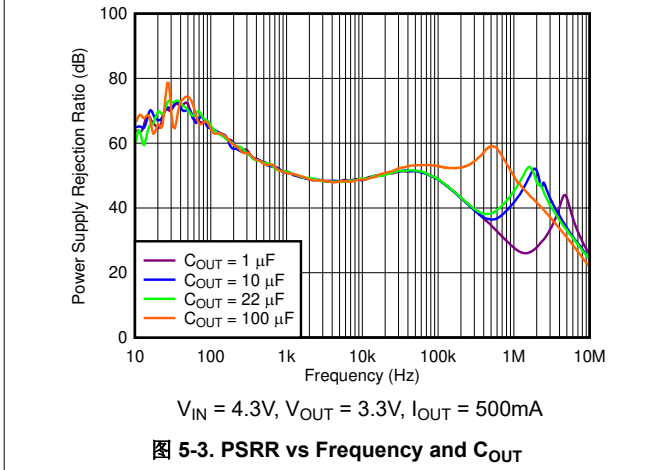
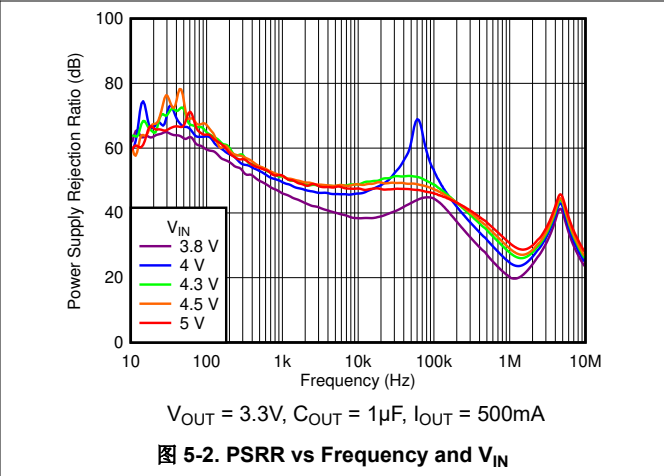
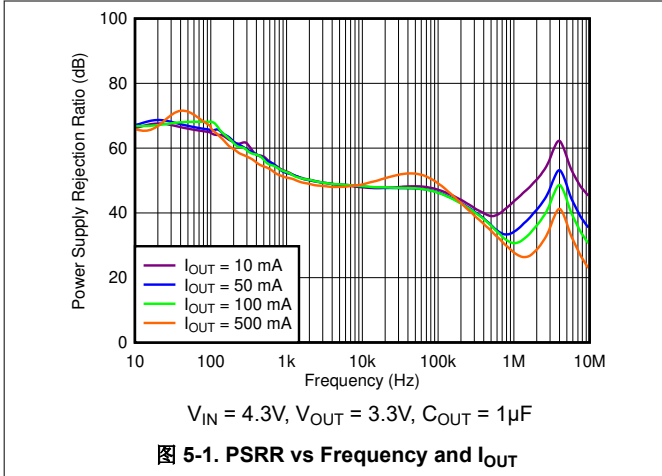
### 5.5 Electrical Characteristics (续)

at operating temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$  or  $2.0\text{V}$  (whichever is greater),  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted); all typical values at  $T_J = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$V_{DO}$	Dropout voltage	$I_{OUT} = 500\text{mA}$ , $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$	$0.6\text{V} \leq V_{OUT} < 0.8\text{V}$	675	1080	mV	
			$0.8\text{V} \leq V_{OUT} < 1.0\text{V}$	600	930		
			$0.8\text{V} \leq V_{OUT} < 1.0\text{V}$ , DYD package	600	950		
			$1.0\text{V} \leq V_{OUT} < 1.2\text{V}$	550	780		
			$1.0\text{V} \leq V_{OUT} < 1.2\text{V}$ , DYD package	550	800		
			$1.2\text{V} \leq V_{OUT} < 1.5\text{V}$	500	630		
			$1.2\text{V} \leq V_{OUT} < 1.5\text{V}$ , DYD package	500	650		
			$1.5\text{V} \leq V_{OUT} < 1.8\text{V}$	350	400		
			$1.5\text{V} \leq V_{OUT} < 1.8\text{V}$ , DYD package	350	420		
			$1.8\text{V} \leq V_{OUT} < 2.5\text{V}$	325	380		
			$1.8\text{V} \leq V_{OUT} < 2.5\text{V}$ , DYD package	325	400		
			$2.5\text{V} \leq V_{OUT} < 3.3\text{V}$	250	300		
		$2.5\text{V} \leq V_{OUT} < 3.3\text{V}$ , DYD package	250	320			
		$3.3\text{V} \leq V_{OUT} < 5.0\text{V}$	150	215			
		$3.3\text{V} \leq V_{OUT} < 5.0\text{V}$ , DYD package	150	238			
		$I_{OUT} = 500\text{mA}$ , $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	$0.6\text{V} \leq V_{OUT} < 0.8\text{V}$				1140
			$0.8\text{V} \leq V_{OUT} < 1.0\text{V}$				985
			$0.8\text{V} \leq V_{OUT} < 1.0\text{V}$ , DYD package				1005
			$1.0\text{V} \leq V_{OUT} < 1.2\text{V}$				825
			$1.0\text{V} \leq V_{OUT} < 1.2\text{V}$ , DYD package				845
			$1.2\text{V} \leq V_{OUT} < 1.5\text{V}$				665
			$1.2\text{V} \leq V_{OUT} < 1.5\text{V}$ , DYD package				685
			$1.5\text{V} \leq V_{OUT} < 1.8\text{V}$				425
			$1.5\text{V} \leq V_{OUT} < 1.8\text{V}$ , DYD package				445
$1.8\text{V} \leq V_{OUT} < 2.5\text{V}$				400			
$1.8\text{V} \leq V_{OUT} < 2.5\text{V}$ , DYD package				420			
$2.5\text{V} \leq V_{OUT} < 3.3\text{V}$				325			
$2.5\text{V} \leq V_{OUT} < 3.3\text{V}$ , DYD package			345				
$3.3\text{V} \leq V_{OUT} < 5.0\text{V}$			238				
$3.3\text{V} \leq V_{OUT} < 5.0\text{V}$ , DYD package			258				
PSRR	Power-supply rejection ratio	$f = 1\text{kHz}$ , $V_{IN} = V_{OUT} + 1\text{V}$ , $I_{OUT} = 50\text{mA}$		52	dB		
		$f = 100\text{kHz}$ , $V_{IN} = V_{OUT} + 1\text{V}$ , $I_{OUT} = 50\text{mA}$		46			
		$f = 1\text{MHz}$ , $V_{IN} = V_{OUT} + 1\text{V}$ , $I_{OUT} = 50\text{mA}$		52			
$V_N$	Output noise voltage	$\text{BW} = 10\text{Hz to } 100\text{kHz}$ ; $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 50\text{mA}$		71.5	$\mu\text{V}_{\text{RMS}}$		
$V_{UVLO}$	Undervoltage lockout	$V_{IN}$ rising	1.21	1.3	1.44	V	
$V_{UVLO,HYST}$	Undervoltage lockout hysteresis	$V_{IN}$ falling		40		mV	
$t_{STR}$	Startup time			550		$\mu\text{s}$	
$V_{HI}$	EN pin high voltage (enabled)		1			V	
$V_{LO}$	EN pin low voltage (enabled)				0.3	V	
$I_{EN}$	Enable pin current	$\text{EN} = 5.5\text{V}$		10		nA	
$T_{SD}$	Thermal shutdown	Shutdown, temperature increasing		165		$^\circ\text{C}$	
		Reset, temperature decreasing		155			
$R_{PULLDOWN}$	Pulldown resistance	$V_{IN} = 5.5\text{V}$		120		$\Omega$	

### 5.6 Typical Characteristics

at operating temperature  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$  or  $1.45\text{V}$  (whichever is greater),  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\mu\text{F}$  (unless otherwise noted)



### 5.6 Typical Characteristics (continued)

at operating temperature  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$  or  $1.45\text{V}$  (whichever is greater),  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\mu\text{F}$  (unless otherwise noted)

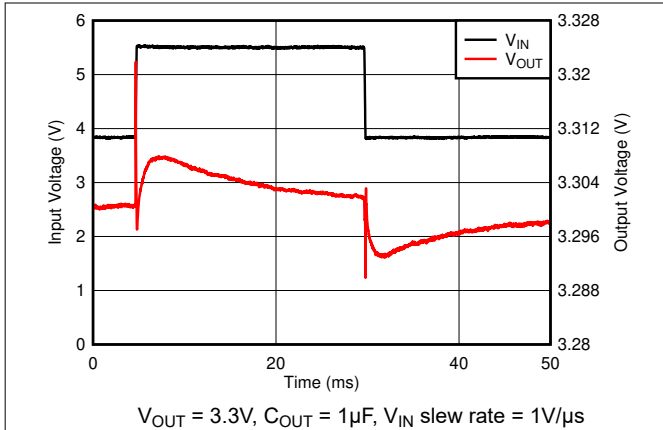


图 5-7. Line Transient

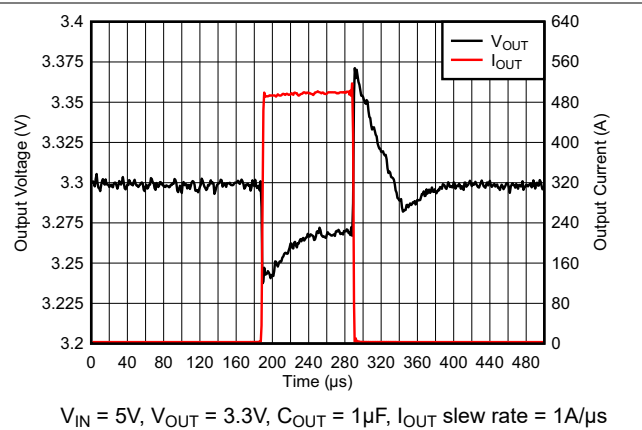


图 5-8. 3.3V, 1mA to 500mA Load Transient

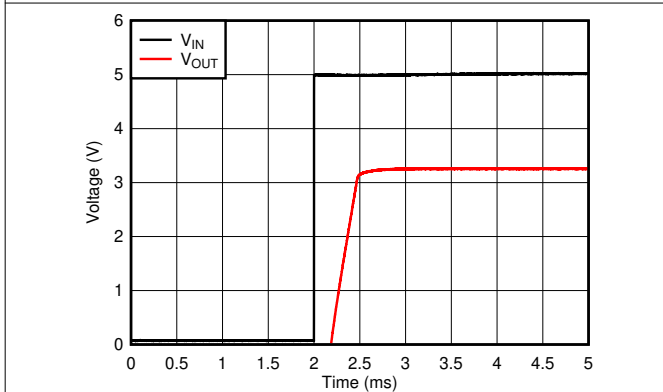


图 5-9.  $V_{IN} = V_{EN}$  Power-Up

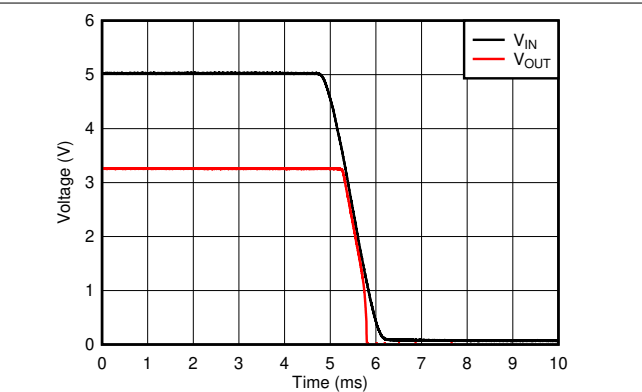


图 5-10.  $V_{IN} = V_{EN}$  Shutdown

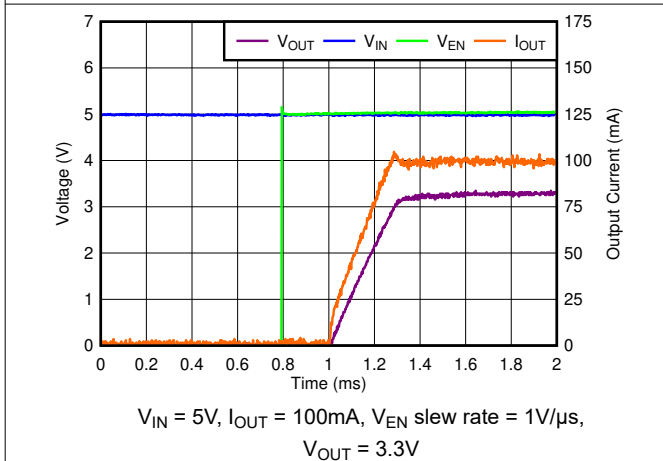


图 5-11. EN Start-Up

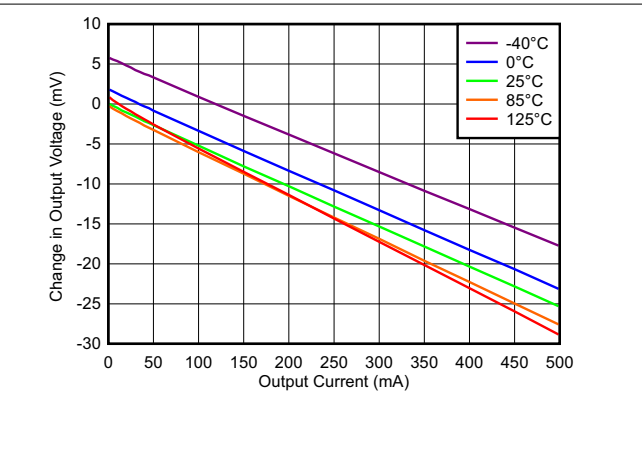


图 5-12. Load Regulation vs  $I_{OUT}$



### 5.6 Typical Characteristics (continued)

at operating temperature  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$  or  $1.45\text{V}$  (whichever is greater),  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\mu\text{F}$  (unless otherwise noted)

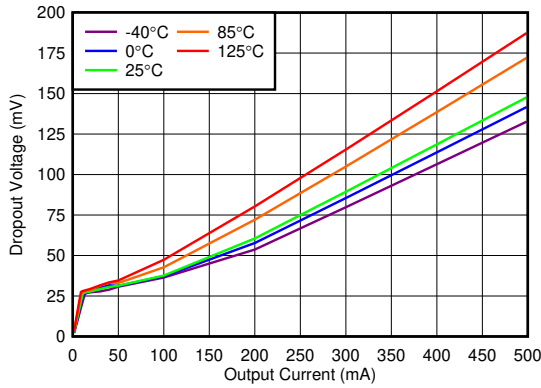


图 5-13. 3.3V Dropout Voltage vs  $I_{OUT}$

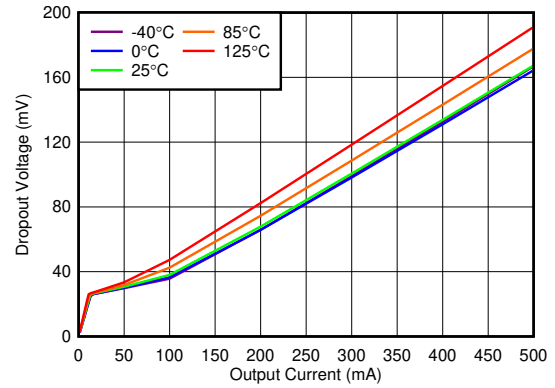


图 5-14. 5.0V Dropout Voltage vs  $I_{OUT}$

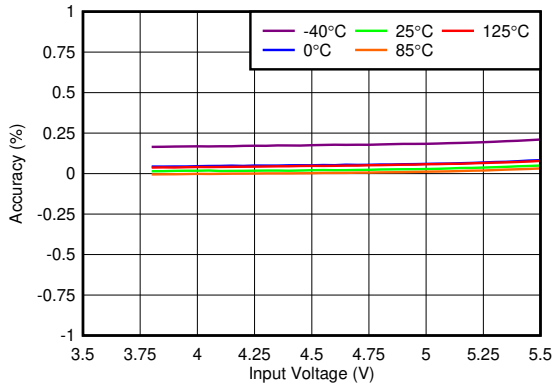


图 5-15. 3.3V Regulation vs  $V_{IN}$  (Line Regulation)

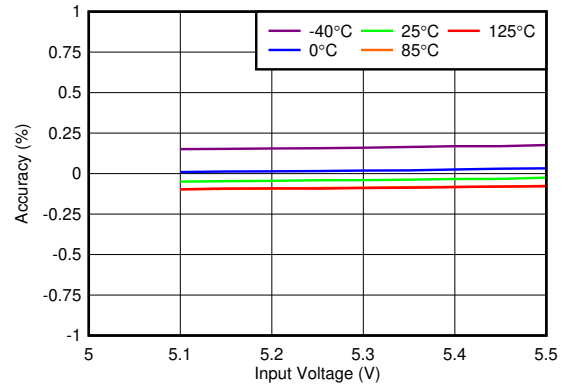


图 5-16. 5.0V Accuracy vs  $V_{IN}$  (Line Regulation)

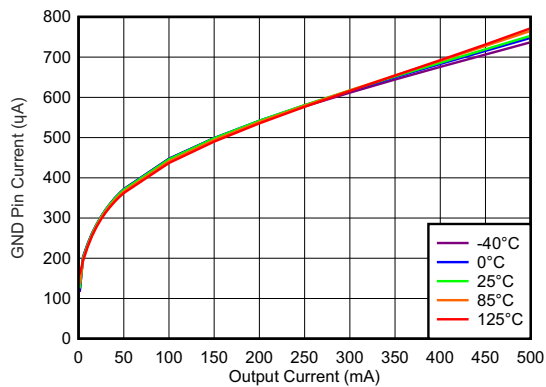
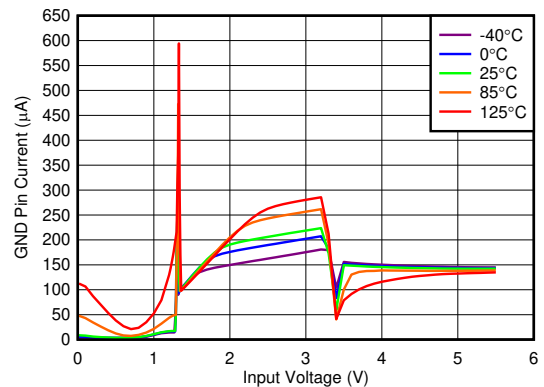


图 5-17.  $I_{GND}$  vs  $I_{OUT}$

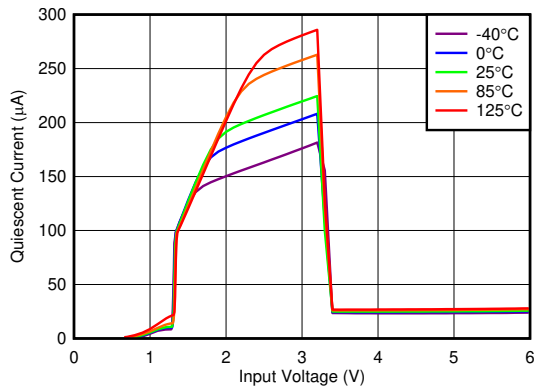


$V_{OUT} = 3.3\text{V}$ ,  $I_{OUT} = 1\text{mA}$

图 5-18.  $I_{GND}$  vs  $V_{IN}$

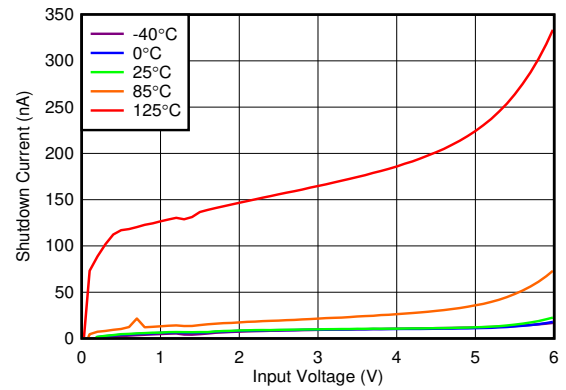
### 5.6 Typical Characteristics (continued)

at operating temperature  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$  or  $1.45\text{V}$  (whichever is greater),  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\mu\text{F}$  (unless otherwise noted)



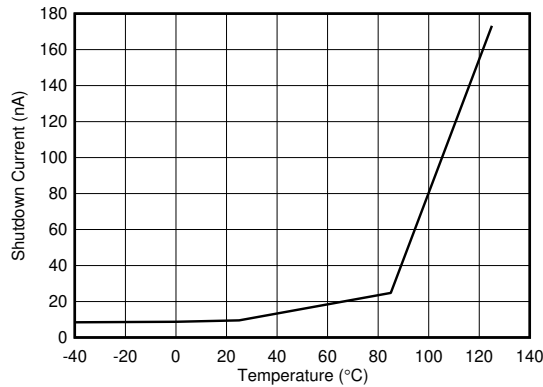
$V_{OUT} = 3.3\text{V}$ ,  $I_{OUT} = 0\text{mA}$

图 5-19.  $I_Q$  vs  $V_{IN}$



$V_{EN} = 0\text{V}$

图 5-20.  $I_{SHDN}$  vs  $V_{IN}$



$V_{EN} = 0\text{V}$

图 5-21.  $I_{SHDN}$  vs Temperature

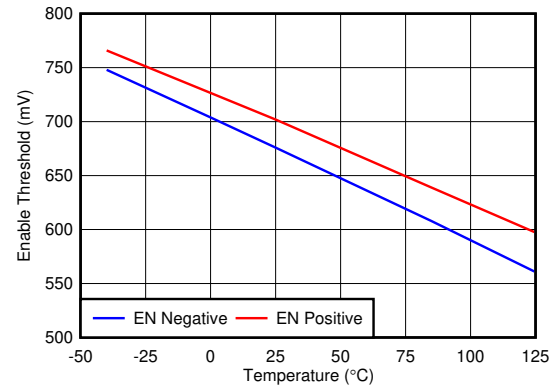
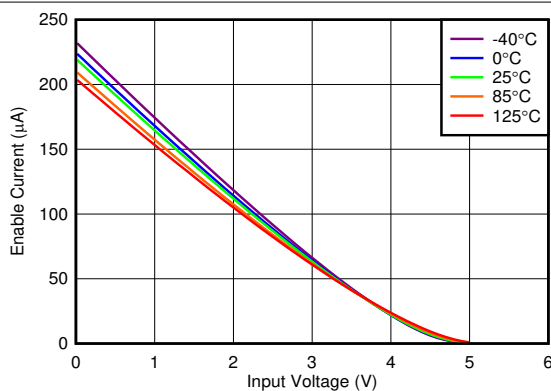


图 5-22. Enable Threshold vs Temperature



$V_{EN} = 5.5\text{V}$

图 5-23.  $I_{EN}$  vs  $V_{IN}$

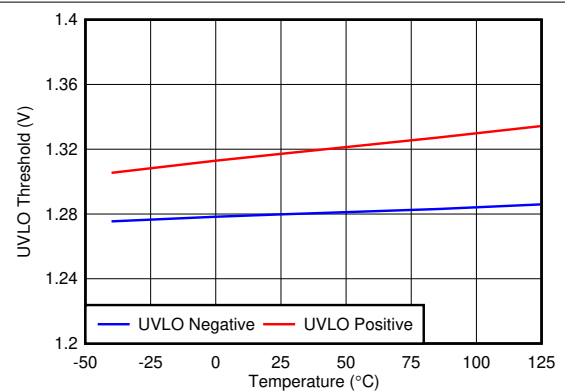
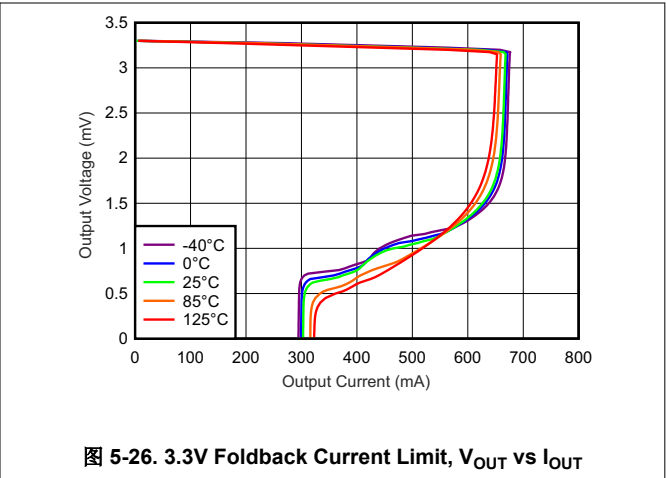
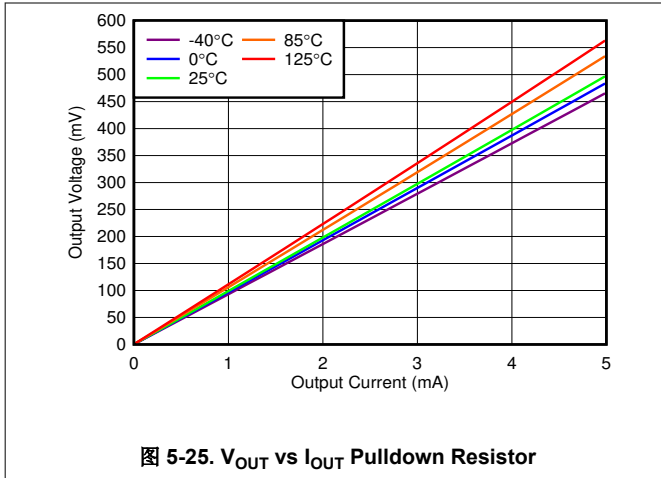


图 5-24. UVLO Threshold vs Temperature

### 5.6 Typical Characteristics (continued)

at operating temperature  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$  or  $1.45\text{V}$  (whichever is greater),  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\mu\text{F}$  (unless otherwise noted)



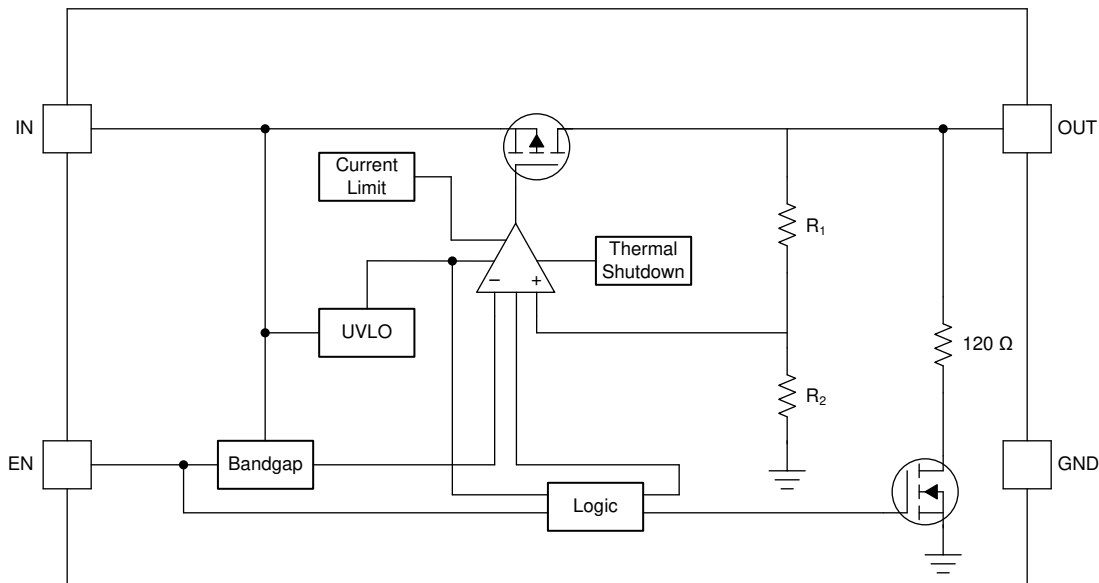
## 6 Detailed Description

### 6.1 Overview

The TLV755P low-dropout regulator (LDO) consumes low quiescent current and delivers excellent line and load transient performance. The TLV755P is optimized for a wide variety of applications by supporting an input voltage range from 1.45V to 5.5V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 0.6V to 5V to support the lower core voltages of modern microcontrollers (MCUs).

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### 6.2 Functional Block Diagram



$R_2 = 550\text{k}\Omega$ ,  $R_1 = \text{adjustable}$ .

### 6.3 Feature Description

#### 6.3.1 Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit disables the output until the input voltage is greater than the rising UVLO voltage ( $V_{UVLO}$ ). This circuit makes sure the device does not exhibit unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When  $V_{IN}$  is less than  $V_{UVLO}$ , the output is connected to ground with a  $120\Omega$  pulldown resistor.

#### 6.3.2 Enable (EN)

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed  $V_{HI}$ . Turn off the device by forcing the EN pin below  $V_{LO}$ . If shutdown capability is not required, connect EN to IN.

The device has an internal pulldown that connects a  $120\Omega$  resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance ( $C_{OUT}$ ) and the load resistance ( $R_L$ ) in parallel with the  $120\Omega$  pulldown resistor. 方程式 1 calculates the time constant  $\tau$ :

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

The EN pin is independent of the input pin (IN), but if the EN pin is driven to a higher voltage than  $V_{IN}$ , the current into the EN pin increases. This effect is illustrated in [图 5-23](#). When the EN voltage is higher than the input voltage there is an increased current flow into the EN pin. If this increased flow causes problems in the application, sequence the EN pin after  $V_{IN}$  is high, or to tie EN to  $V_{IN}$  to prevent this flow increase from happening. If EN is driven to a higher voltage than  $V_{IN}$ , limit the frequency on EN to below 10kHz.

### 6.3.3 Internal Foldback Current Limit

The TLV755P has an internal current limit that protects the regulator during fault conditions. The current limit is a hybrid scheme with brick wall until the output voltage is less than  $0.4V \times V_{OUT(NOM)}$ . When the voltage drops below  $0.4V \times V_{OUT(NOM)}$ , a foldback current limit is implemented that scales back the current as the output voltage approaches GND. When the output shorts, the LDO supplies a typical current of  $I_{SC}$ . The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output shorts, the PMOS pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{SC}]$  until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown.

The foldback current-limit circuit limits the current that is allowed through the device to current levels lower than the minimum current limit at nominal  $V_{OUT}$  current limit ( $I_{CL}$ ) during start-up. See [图 5-26](#) for typical current limit values. If the output is loaded by a constant-current load during start-up, or if the output voltage is negative when the device is enabled, then the load current demanded by the load potentially exceeds the foldback current limit and the device does not rise to the full output voltage. For constant-current loads, disable the output load until the output rises to the nominal voltage.

Excess inductance causes the current limit to oscillate. Minimize the inductance to keep the current limit from oscillating during a fault condition.

### 6.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 165°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits regulator dissipation that protects the circuit from damage as a result of overheating.

Activating the thermal shutdown feature typically indicates excessive power dissipation as a result of the product of the  $(V_{IN} - V_{OUT})$  voltage and the load current. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the device into thermal shutdown degrades device reliability.

## 6.4 Device Functional Modes

表 6-1 lists a comparison between the normal, dropout, and disabled modes of operation.

表 6-1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	$V_{IN}$	EN	$I_{OUT}$	$T_J$
Normal <sup>(1)</sup>	$V_{IN} > V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout <sup>(1)</sup>	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	—	$T_J < T_{SD}$
Disabled <sup>(2)</sup>	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{LO}$	—	$T_J > T_{SD}$

(1) Make sure all table conditions are met.

(2) The device is disabled when any condition is met.

### 6.4.1 Normal Operation

The device regulates to the nominal output voltage when all of the following conditions are met.

- The input voltage is greater than the nominal output voltage plus the dropout voltage ( $V_{OUT(NOM)} + V_{DO}$ )
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit ( $I_{OUT} < I_{CL}$ )
- The device junction temperature is less than the thermal shutdown temperature ( $T_J < T_{SD}$ )

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device degrades because the pass transistor is in a triode state and no longer controls the output voltage of the LDO. Line or load transients in dropout result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout,  $V_{IN} < V_{OUT(NOM)} + V_{DO}$ , right after being in a normal regulation state, but not during start-up), the pass transistor is driven as hard as possible when the control loop is out of balance. During the normal time required for the device to regain regulation,  $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$ ,  $V_{OUT}$  overshoots  $V_{OUT(NOM)}$  during fast transients.

### 6.4.3 Disabled

The output is shut down by forcing the enable pin below  $V_{LO}$ . When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal switch from the output to ground. The active pulldown is on when sufficient input voltage is provided.

## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Application Information

#### 7.1.1 Input and Output Capacitor Selection

The TLV755P requires an output capacitance of 0.47 $\mu$ F or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in capacitance value and equivalent series resistance (ESR) over temperature. When selecting a capacitor for a specific application, consider the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. Generally, derate ceramic capacitors by 50%. For best performance, use a maximum output capacitance value of 200 $\mu$ F.

Place a 1 $\mu$ F or greater capacitor on the input pin of the LDO. Some input supplies have a high impedance. Placing a capacitor on the input supply reduces the input impedance. The input capacitor counteracts reactive input sources and improves transient response and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors are used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

#### 7.1.2 Dropout Voltage

The TLV755P uses a PMOS pass transistor to achieve low dropout. When ( $V_{IN} - V_{OUT}$ ) is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass transistor.  $V_{DO}$  scales linearly with the output current because the PMOS transistor functions like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ( $V_{IN} - V_{OUT}$ ) approaches dropout operation. See [图 5-13](#) and [图 5-14](#) for typical dropout values.

#### 7.1.3 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on  $V_{IN}$  during start-up. As with other LDOs, the output overshoots on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up when the slew rate and voltage levels are in the correct range; see [图 7-1](#). Use an enable signal to avoid this condition.

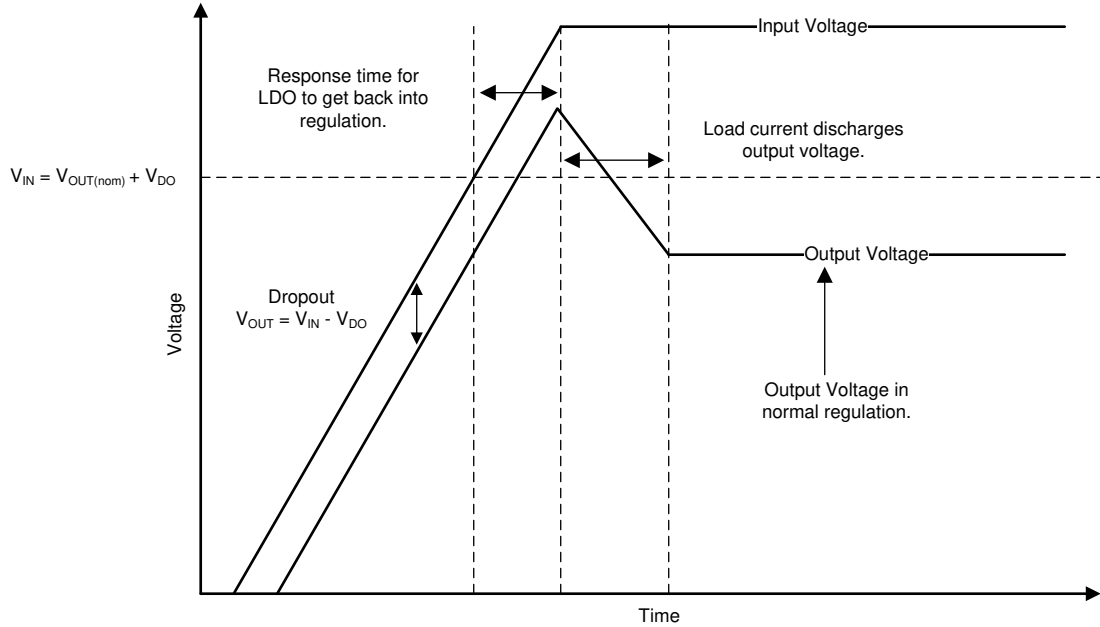


图 7-1. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass transistor and bring the gate back to the correct voltage for proper regulation. 图 7-2 illustrates what is happening internally with the gate voltage and how overshoot is caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass transistor the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and causes the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.



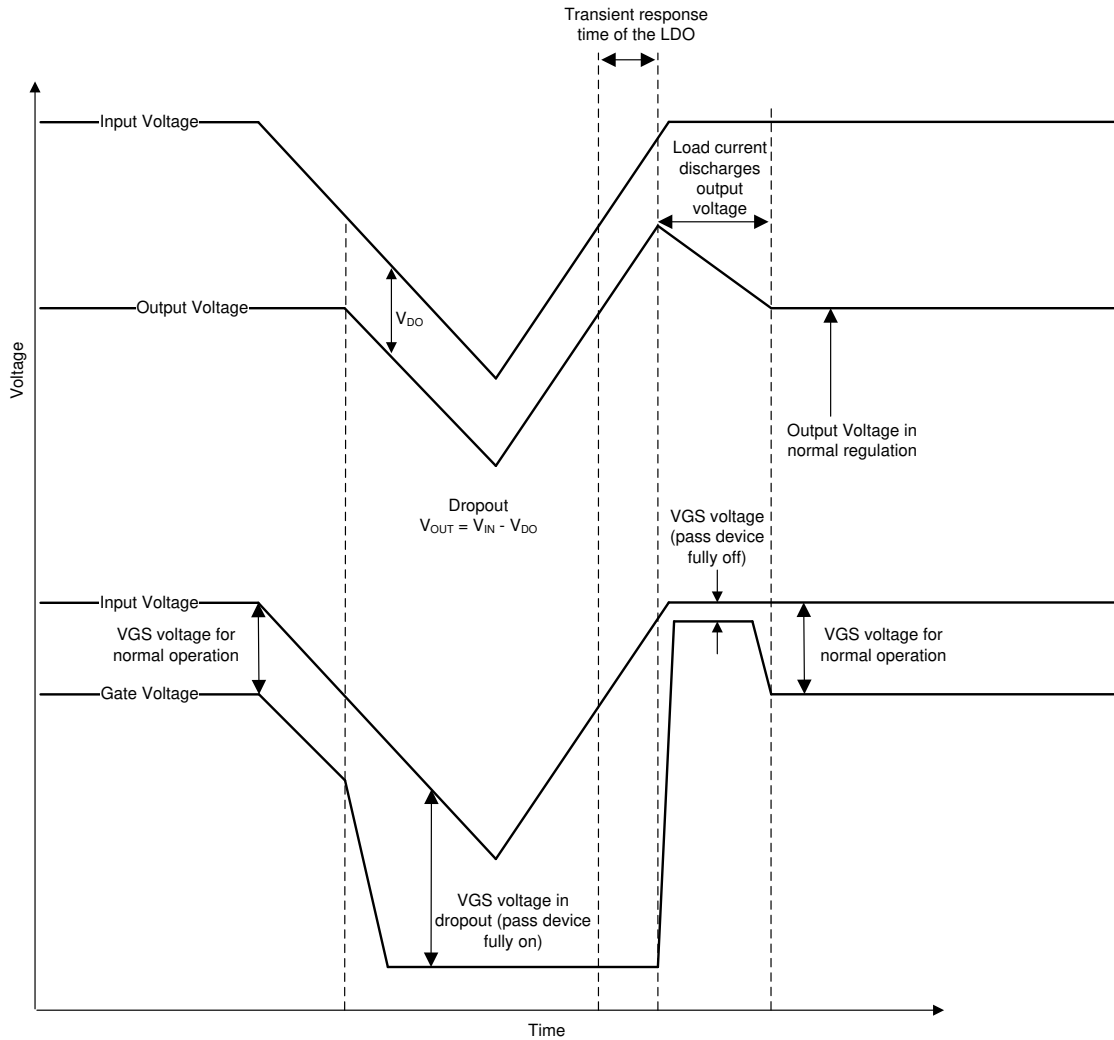


图 7-2. Line Transients From Dropout

### 7.1.4 Reverse Current

As with most LDOs, excessive reverse current potentially damages this device.

Reverse current flows through the body diode on the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current occur are outlined in this section, all of which exceed the absolute maximum rating of  $V_{OUT} > V_{IN} + 0.3V$ :

- If the device has a large  $C_{OUT}$  and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. 图 7-3 shows one approach of protecting the device.

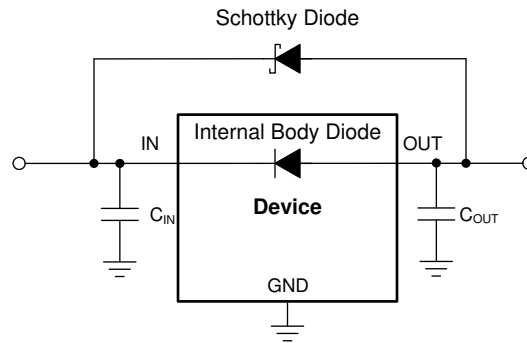


图 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

### 7.1.5 Power Dissipation ( $P_D$ )

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator is as free of other heat-generating devices as possible that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 方程式 2 to approximate  $P_D$ :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Minimize power dissipation to achieve greater efficiency. This minimizing process is achieved by selecting the correct system voltage rails. Proper selection helps obtain the minimum input-to-output voltage differential. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat-conduction path for the device is through the thermal pad on the package. As such, solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to inner plane areas or to a bottom-side copper plane.

The maximum allowable junction temperature ( $T_J$ ) determines the maximum power dissipation for the device. According to 方程式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB, device package, and the temperature of the ambient air ( $T_A$ ).

$$T_J = T_A + R_{\theta JA} \times P_D \quad (3)$$

Unfortunately, this thermal resistance ( $R_{\theta JA}$ ) is dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The  $R_{\theta JA}$  value is only used as a relative measure of package thermal performance.  $R_{\theta JA}$  is the sum of the package junction-to-case (bottom) thermal resistance ( $R_{\theta JCbott}$ ) plus the thermal resistance contribution by the PCB copper.

### 7.1.5.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi ( $\Psi$ ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not thermal resistances, but offer practical and relative means of estimating junction temperatures. These psi metrics are independent of the copper-spreading area. The key thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) are used in accordance with [方程式 4](#) and are described in the *Thermal Information* table.

$$\begin{aligned} \Psi_{JT}: T_J &= T_T + \Psi_{JT} \times P_D \\ \Psi_{JB}: T_J &= T_B + \Psi_{JB} \times P_D \end{aligned} \quad (4)$$

where:

- $P_D$  is the power dissipated as shown in [方程式 2](#)
- $T_T$  is the temperature at the center-top of the device package
- $T_B$  is the PCB surface temperature measured 1mm from the device package and centered on the package edge

## 7.2 Typical Application

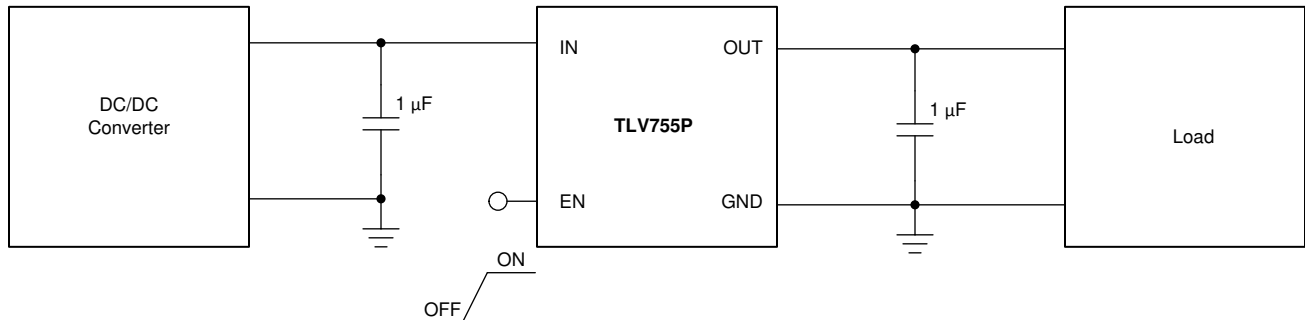


图 7-4. TLV755P Typical Application

### 7.2.1 Design Requirements

[表 7-1](#) lists the design requirements for this application.

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.3V
Output voltage	3.3V
Input current	500mA (maximum)
Output load	250mA DC
Maximum ambient temperature	70°C

## 7.2.2 Detailed Design Procedure

### 7.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During start-up, the input current is higher as a result of the inrush current charging the output capacitor. Use [方程式 5](#) to calculate the current through the input.

$$I_{OUT(t)} = \left[ \frac{C_{OUT} \times dV_{OUT}(t)}{dt} \right] + \left[ \frac{V_{OUT}(t)}{R_{LOAD}} \right] \quad (5)$$

where:

- $V_{OUT}(t)$  is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$  is the slope of the  $V_{OUT}$  ramp
- $R_{LOAD}$  is the resistive load impedance

### 7.2.2.2 Thermal Dissipation

Junction temperature is determined using the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) and the total power dissipation ( $P_D$ ). Use [方程式 6](#) to calculate the power dissipation. Multiply  $P_D$  by  $R_{\theta JA}$  as [方程式 7](#) shows and add the ambient temperature ( $T_A$ ) to calculate the junction temperature ( $T_J$ ).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (6)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (7)$$

Calculate the maximum ambient temperature as [方程式 8](#) shows if the ( $T_{J(MAX)}$ ) value does not exceed 125°C. [方程式 9](#) calculates the maximum ambient temperature with a value of 99.95°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (8)$$

$$T_{A(MAX)} = 125^\circ\text{C} - 100.2^\circ\text{C/W} \times (4.3\text{V} - 3.3\text{V}) \times (0.25\text{A}) = 99.95^\circ\text{C} \quad (9)$$

## 7.2.3 Application Curve

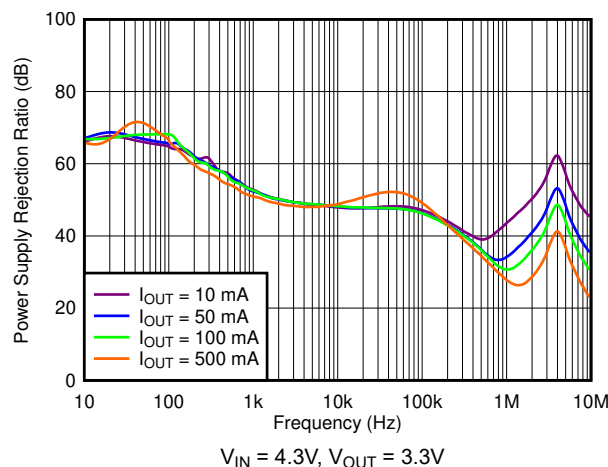


图 7-5. PSRR vs Frequency (4.3V to 3.3V)

### 7.3 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV755P. If the input source is reactive, consider using multiple input capacitors in parallel with the 1µF input capacitor to lower the input supply impedance over frequency.

### 7.4 Layout

#### 7.4.1 Layout Guidelines

- Place input and output capacitors as close as possible to the device.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- For packages with thermal pads, solder the thermal pad to copper to achieve best thermal resistance. Thermal resistance increases significantly when the thermal pad is not soldered.

#### 7.4.2 Layout Examples

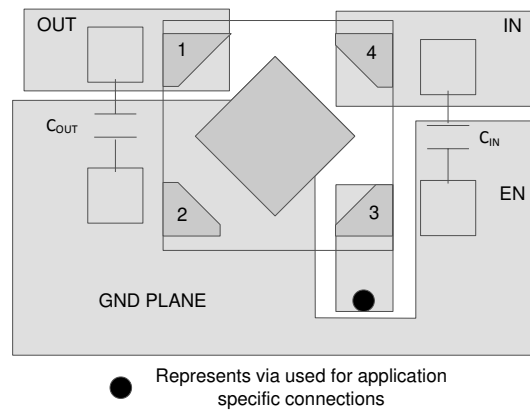


图 7-6. Layout Example for the DQN Package

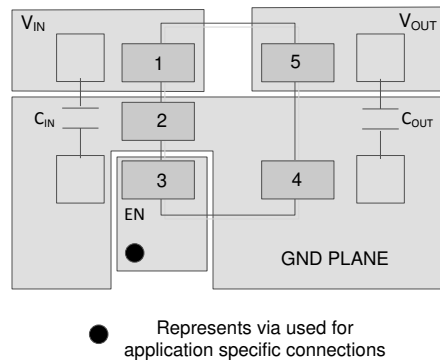
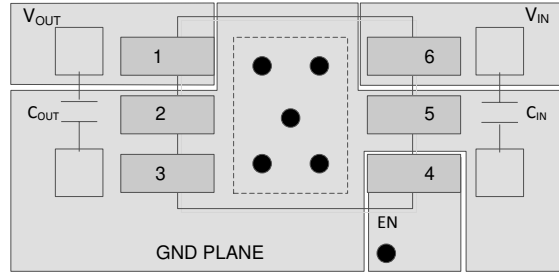
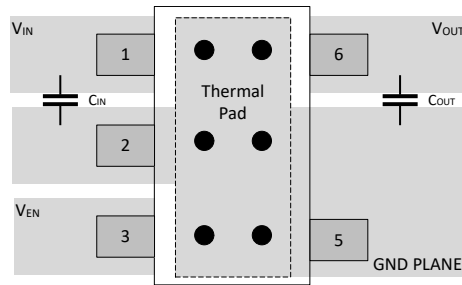


图 7-7. Layout Example for the DBV Package



● Represents via used for application specific connections

图 7-8. Layout Example for the DRV Package



● Represents via used for application specific connections

图 7-9. Layout Example for the DYD Package

## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Device Nomenclature

**表 8-1. Device Nomenclature**

PRODUCT <sup>(1) (2)</sup>	DESCRIPTION
TLV755xx(x)Pyyyz(M3)	<p><b>xx(x)</b> is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V).</p> <p><b>P</b> indicates an active output discharge feature. All members of the TLV755P family actively discharge the output when the device is disabled.</p> <p><b>yyy</b> is the package designator.</p> <p><b>z</b> is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).</p> <p><b>M3</b> is a suffix designator for devices that only use the latest manufacturing flow.</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).
- (2) Output voltages from 0.6V to 5V in 50mV increments are available. Contact the factory for details and availability.

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (March 2024) to Revision D (September 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Changed 3.3V, 1mA to 500mA Load Transient and Load Regulation vs $I_{OUT}$ curves.....	7
• Added M3 information to <i>Device Nomenclature</i> table.....	23

Changes from Revision B (November 2023) to Revision C (March 2024)	Page
• 将 SOT-23 (DYD) 从 预告信息 更改为 量产数据 .....	1
• 添加了 SOT-23 (DYD) 特性 封装要点.....	1
• Added last bullet item to <i>Layout Guidelines</i> .....	21
• Added <i>Layout Example for the DYD Package</i> figure.....	21

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV755075PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	DJ	<a href="#">Samples</a>
TLV75507PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KD	<a href="#">Samples</a>
TLV75507PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KD	<a href="#">Samples</a>
TLV75509PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1HAF	<a href="#">Samples</a>
TLV75509PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AX	<a href="#">Samples</a>
TLV75509PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AX	<a href="#">Samples</a>
TLV75509PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HDH	<a href="#">Samples</a>
TLV75509PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DPH	<a href="#">Samples</a>
TLV75510PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FPF	<a href="#">Samples</a>
TLV75510PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KE	<a href="#">Samples</a>
TLV75510PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KE	<a href="#">Samples</a>
TLV75510PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KE	<a href="#">Samples</a>
TLV75510PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GUH	<a href="#">Samples</a>
TLV75511PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E8	<a href="#">Samples</a>
TLV75512PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FQF	<a href="#">Samples</a>
TLV75512PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AG	<a href="#">Samples</a>
TLV75512PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AG	<a href="#">Samples</a>
TLV75512PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AG	<a href="#">Samples</a>
TLV75512PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GVH	<a href="#">Samples</a>
TLV75512PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DQH	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV75515PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FRF	<a href="#">Samples</a>
TLV75515PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KF	<a href="#">Samples</a>
TLV75515PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KF	<a href="#">Samples</a>
TLV75515PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GWH	<a href="#">Samples</a>
TLV755185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EZ	<a href="#">Samples</a>
TLV755185PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EZ	<a href="#">Samples</a>
TLV75518PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FSF	<a href="#">Samples</a>
TLV75518PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AI	<a href="#">Samples</a>
TLV75518PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AI	<a href="#">Samples</a>
TLV75518PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GXH	<a href="#">Samples</a>
TLV75518PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DRH	<a href="#">Samples</a>
TLV75519PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1HBF	<a href="#">Samples</a>
TLV75519PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B5	<a href="#">Samples</a>
TLV75519PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B5	<a href="#">Samples</a>
TLV75519PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HEH	<a href="#">Samples</a>
TLV75525PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FTF	<a href="#">Samples</a>
TLV75525PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AJ	<a href="#">Samples</a>
TLV75525PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AJ	<a href="#">Samples</a>
TLV75525PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GZH	<a href="#">Samples</a>
TLV75525PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DSH	<a href="#">Samples</a>
TLV75528PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FUF	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV75528PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KG	<a href="#">Samples</a>
TLV75528PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KG	<a href="#">Samples</a>
TLV75528PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H1H	<a href="#">Samples</a>
TLV75528PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DTH	<a href="#">Samples</a>
TLV75529PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1HCF	<a href="#">Samples</a>
TLV75529PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HFH	<a href="#">Samples</a>
TLV75530PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FVF	<a href="#">Samples</a>
TLV75530PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KI	<a href="#">Samples</a>
TLV75530PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KI	<a href="#">Samples</a>
TLV75530PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H2H	<a href="#">Samples</a>
TLV75533PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1FWF	<a href="#">Samples</a>
TLV75533PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AN	<a href="#">Samples</a>
TLV75533PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AN	<a href="#">Samples</a>
TLV75533PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AN	<a href="#">Samples</a>
TLV75533PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H3H	<a href="#">Samples</a>
TLV75533PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DUH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV755075PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75507PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75507PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75507PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75507PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75509PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75509PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75509PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75509PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75509PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75509PDRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75509PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75510PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75510PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75510PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75510PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75510PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75510PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75510PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75510PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75511PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75512PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75512PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75512PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75512PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75512PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75512PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75512PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75512PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75515PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75515PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75515PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75515PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75515PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75515PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75515PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV755185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV755185PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75518PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75518PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75518PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75518PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75518PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75518PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75518PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75519PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75519PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75519PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75519PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75519PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75519PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75519PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75525PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75525PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75525PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75525PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75525PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75525PDRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75525PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75528PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75528PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75528PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75528PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75528PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75528PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75528PDRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75528PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75529PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75529PDRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75530PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75530PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75530PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75530PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75530PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75530PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75530PDRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75533PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75533PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75533PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV75533PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV75533PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV75533PDRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75533PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV755075PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75507PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75507PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75507PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75507PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75509PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75509PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75509PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75509PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75509PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75509PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75509PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75510PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75510PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75510PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75510PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV75510PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75510PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75510PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75510PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75511PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75512PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75512PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75512PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75512PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75512PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75512PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75512PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75512PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75515PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75515PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75515PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75515PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75515PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75515PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75515PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV755185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV755185PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75518PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75518PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75518PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75518PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75518PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75518PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75518PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75519PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75519PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75519PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75519PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75519PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75519PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75519PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75525PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75525PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75525PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75525PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75525PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75525PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75525PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75528PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75528PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75528PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75528PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75528PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75528PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75528PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75528PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75529PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75529PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75530PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75530PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75530PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75530PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75530PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV75530PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75530PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75533PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75533PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV75533PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV75533PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV75533PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV75533PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75533PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0

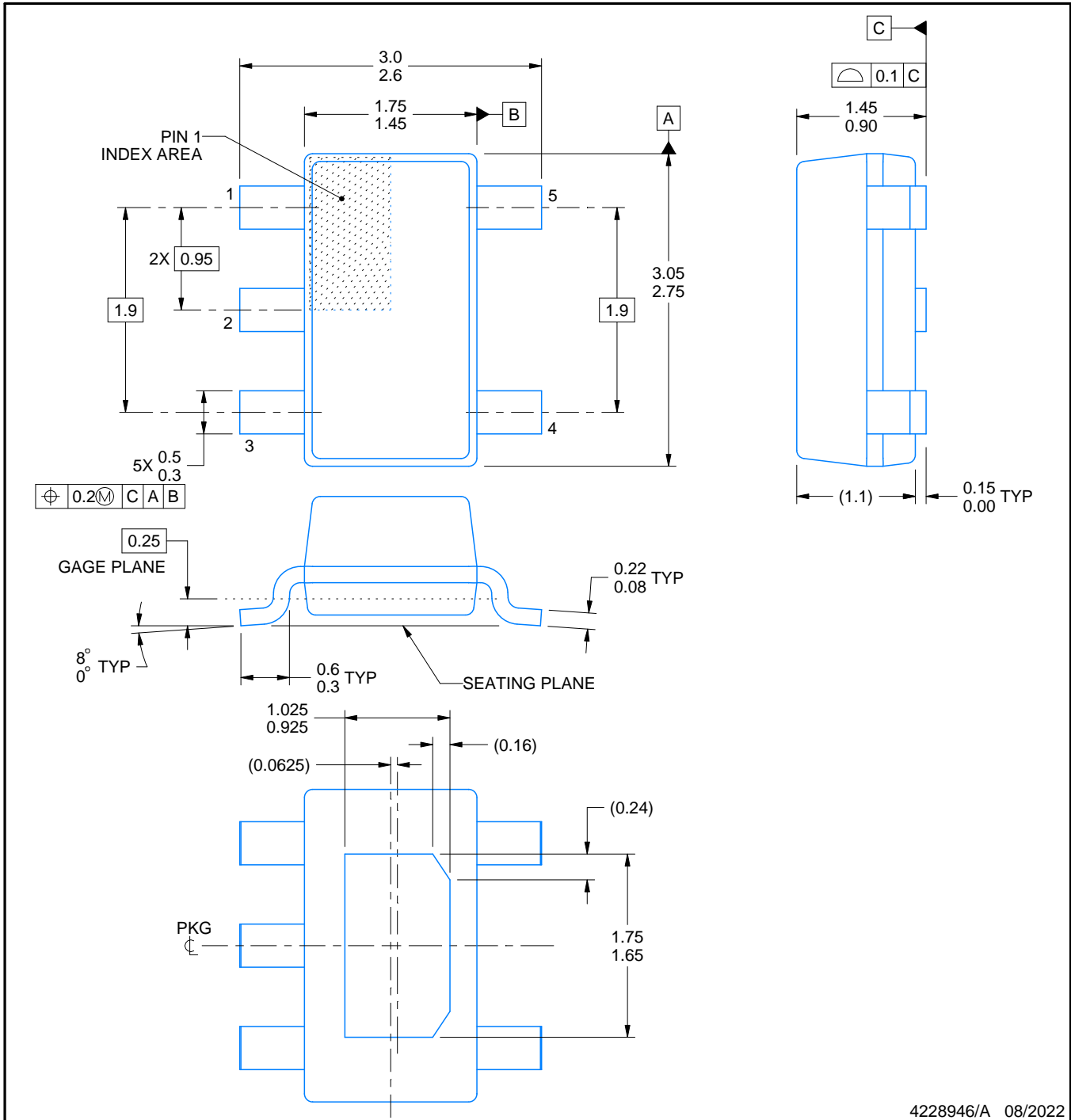
# DYD0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4228946/A 08/2022

## NOTES:

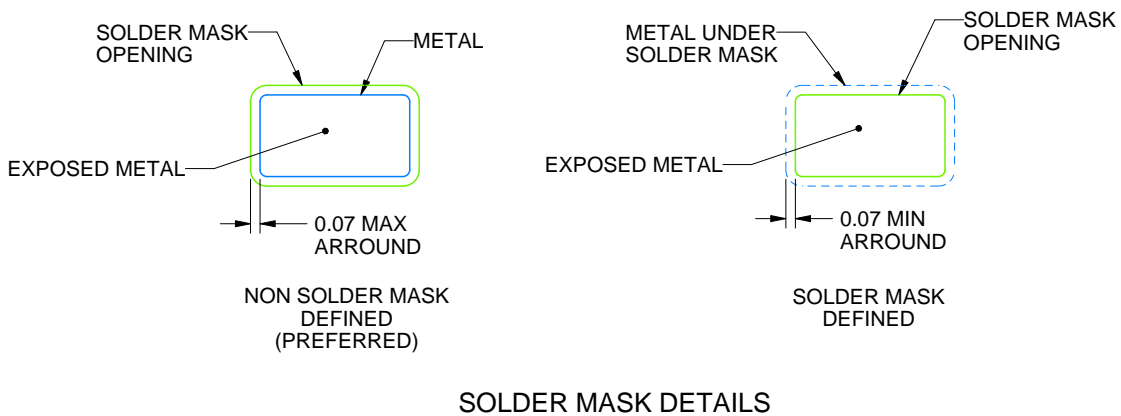
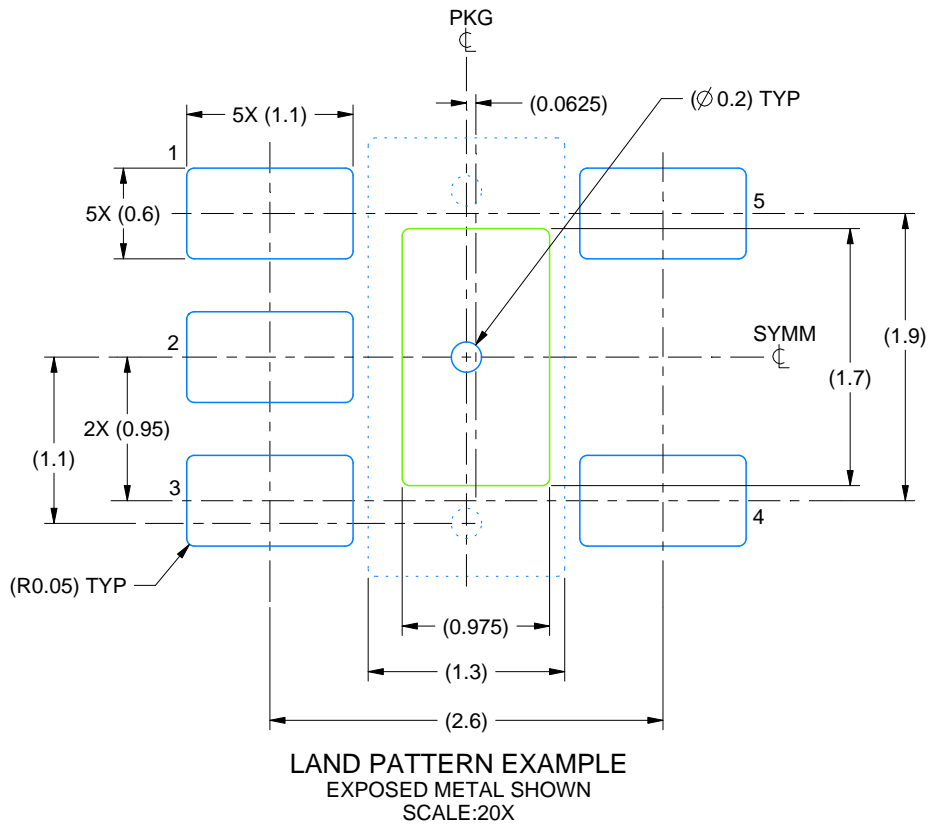
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

DYD0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4228946/A 08/2022

NOTES: (continued)

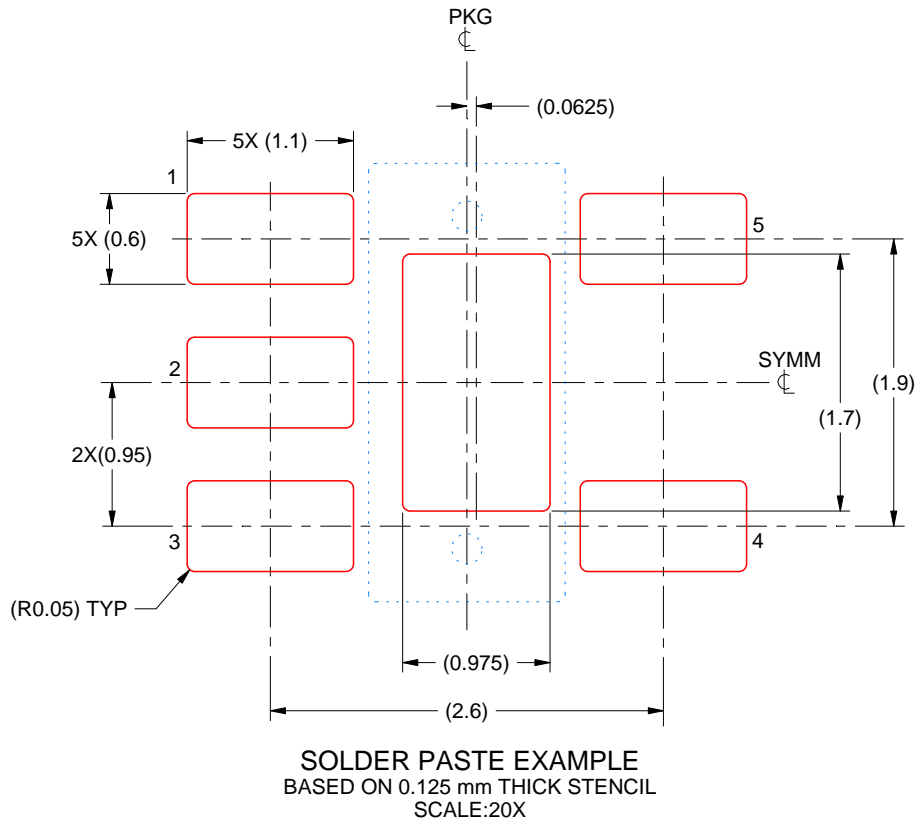
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DYD0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.100	1.09 X 1.90
0.125	0.975 X 1.700 (SHOWN)
0.150	0.89 X 1.55
0.175	0.82 X 1.44

4228946/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

DQN 4

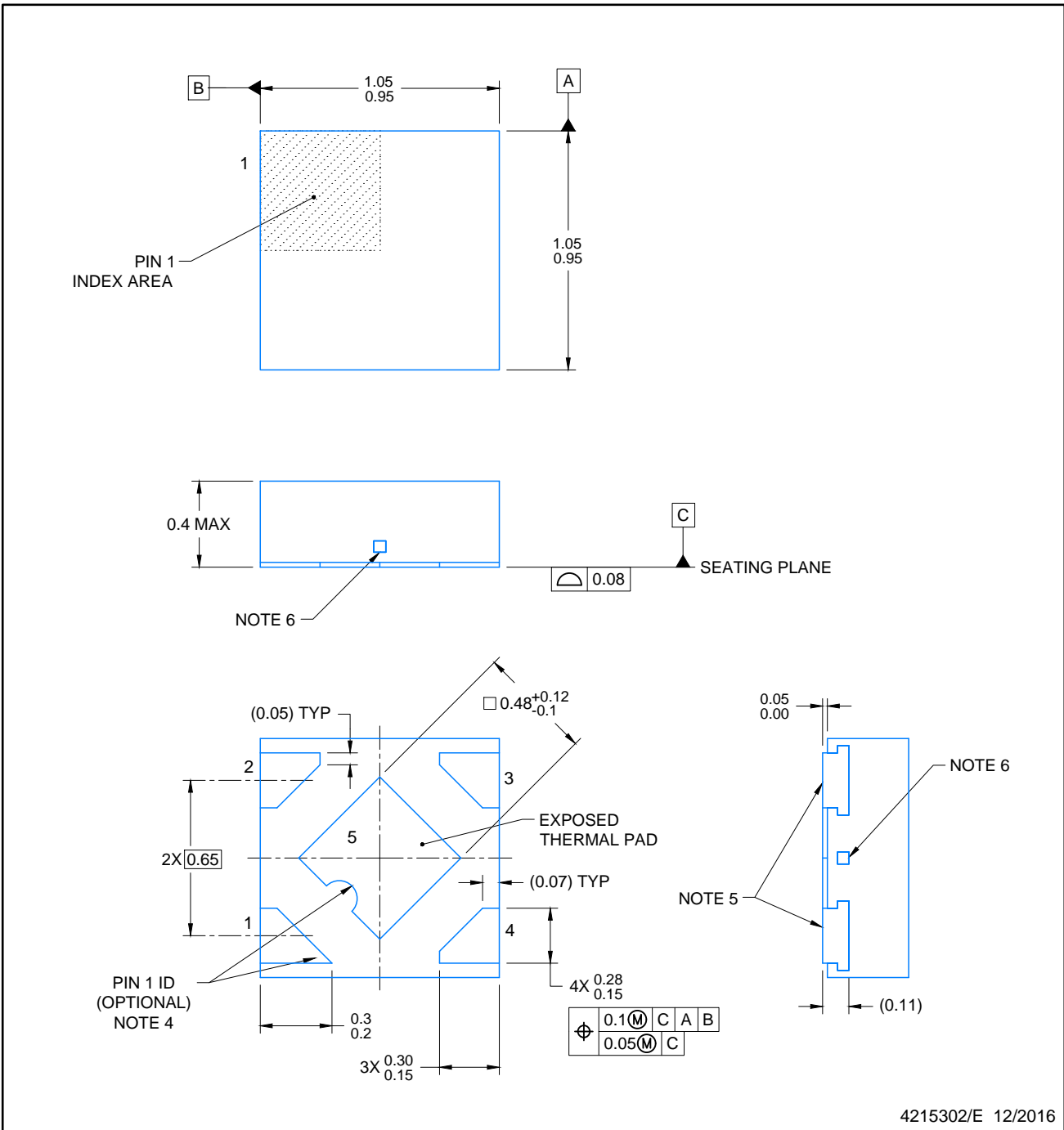
**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

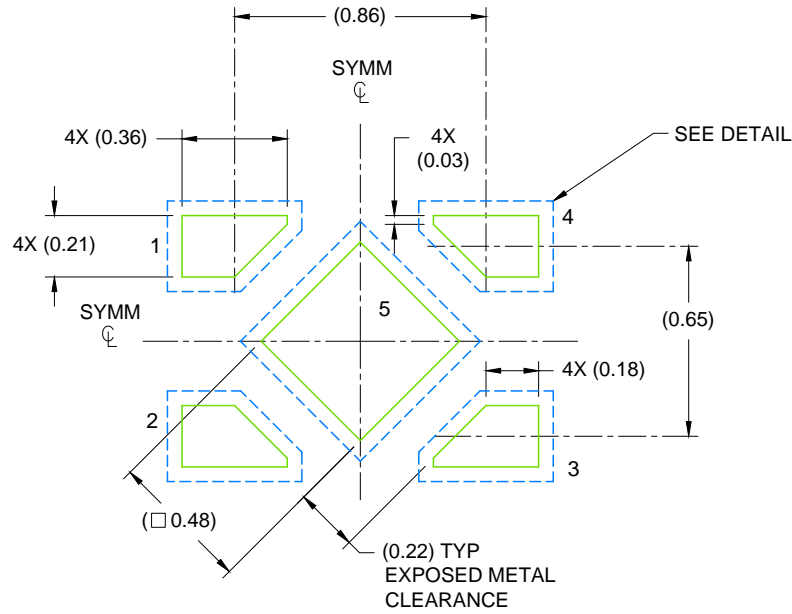
4210367/F



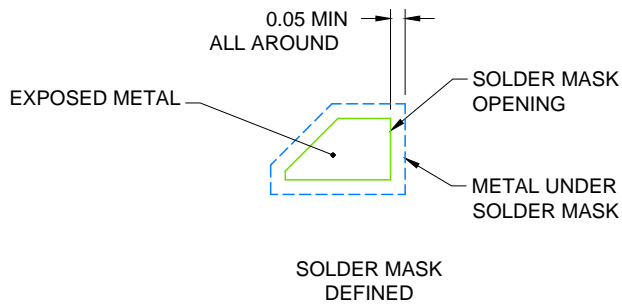
4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE  
SCALE: 40X



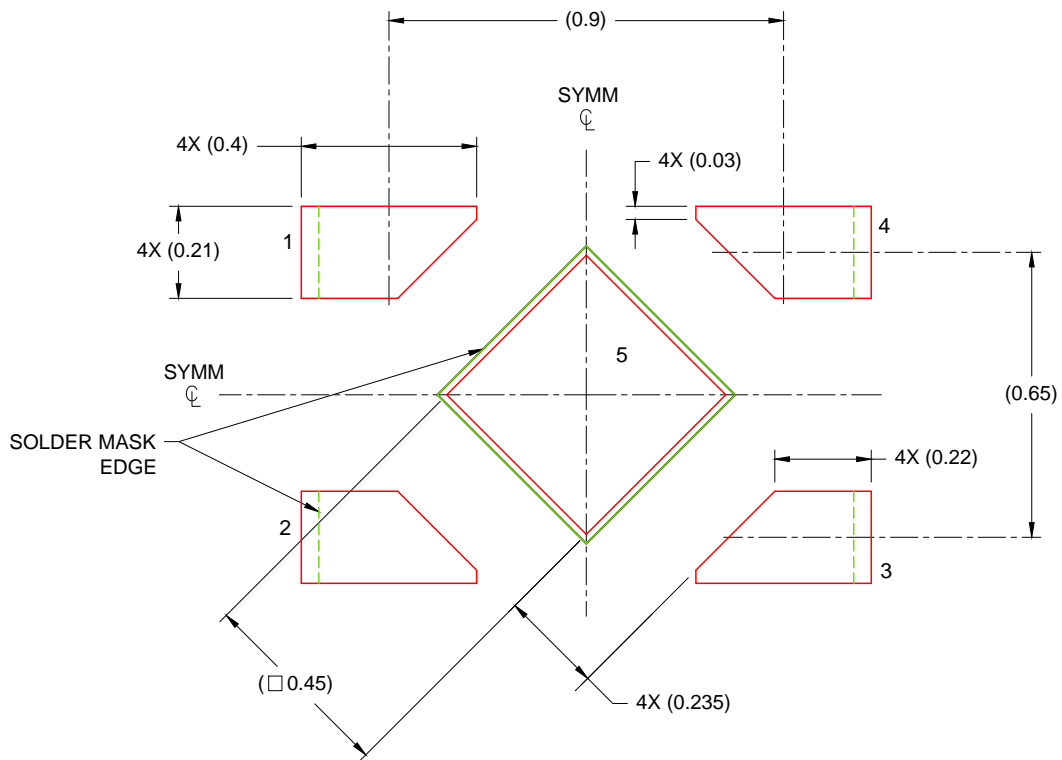
SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.





SOLDER PASTE EXAMPLE  
 BASED ON 0.075 - 0.1mm THICK STENCIL  
 EXPOSED PAD  
 88% PRINTED SOLDER COVERAGE BY AREA  
 SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

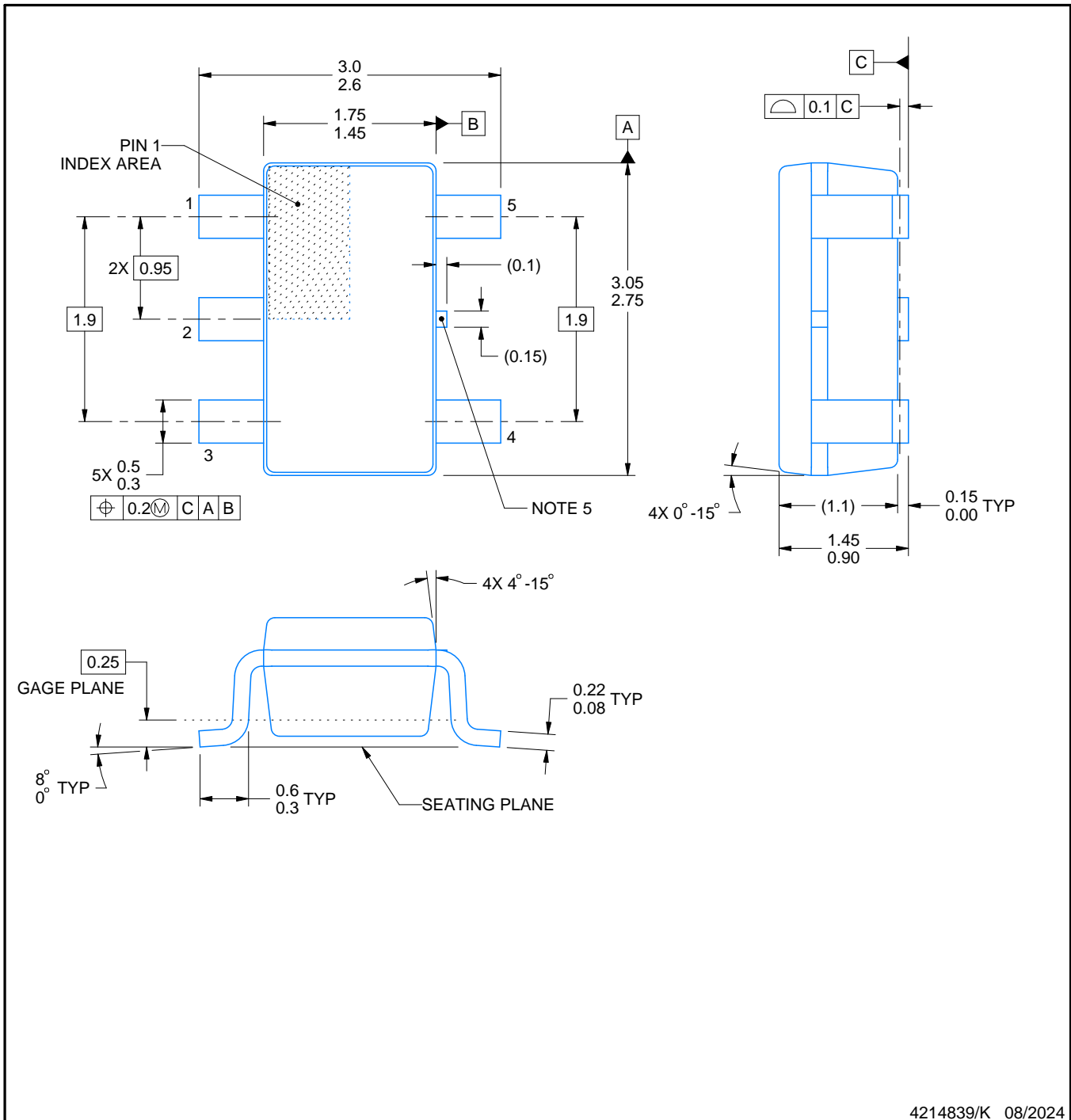
# DBV0005A



## PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

DRV 6

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## 重要声明和免责声明

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