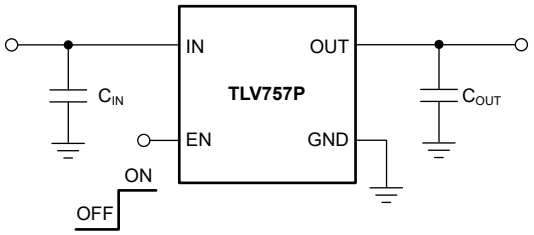
TLV757P 1A、低 I_Q、小型、低压降稳压器

1 特性

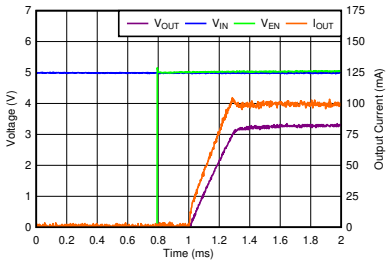
- 采用 SOT-23 (DYD) 封装，具有 60.3°C/W $R_{\theta JA}$
- 输入电压范围：1.45V 至 5.5V
- 可提供固定输出电压：
  - 0.6V 至 5V（阶跃为 50mV）
- 低 I_Q：25 μA（典型值）
- 低压降：
  - 在 1A 下为 425mV（最大值）（V_{OUT} 为 3.3V）
- 输出精度：1%（最大值）
- 内置软启动功能，具有单调 V_{OUT} 上升
- 折返电流限制
- 有源输出放电
- 高 PSRR：100kHz 时为 45dB
- 与 1μF 的陶瓷输出电容器搭配使用时可保持稳定
- 封装：
  - 2.9mm × 2.8mm SOT-23-5 (DBV)
  - 带有散热焊盘的 2.9mm × 2.8mm SOT-23-5 (DYD)
  - 2mm × 2mm WSON-6 (DRV)

2 应用

- 机顶盒、电视和游戏机
- 便携式和电池供电类设备
- 台式机、笔记本电脑和超极本
- 平板电脑和遥控器
- 白色家电和电器
- 电网基础设施和保护继电器
- 摄像头模块和图像传感器



典型应用



启动波形

3 说明

TLV757P 低压降稳压器 (LDO) 是一款超小型低静态电流 LDO，可提供 1A 拉电流，具有良好的线路和负载瞬态性能。TLV757P 经过优化，可支持 1.45V 至 5.5V 的输入电压范围，可适用于各种应用。为更大限度地缩减成本和解决方案尺寸，该器件可在 0.6V 至 5V 范围内提供固定输出电压。此范围支持现代微控制器 (MCU) 更低的内核电压。此外，TLV757P 具备带有使能功能的低 I_Q，从而可将待机功耗降至最低。该器件具有内部软启动功能，可降低浪涌电流。该功能可为负载提供受控电压并在启动过程中更大程度地降低输入电压压降。关断时，该器件可主动下拉输出以使输出快速放电并实现已知的启动状态。

TLV757P 在与支持小尺寸总体解决方案的小型陶瓷输出电容器搭配使用时，可保持稳定。高精度带隙与误差放大器支持 1% 的典型精度。所有器件版本均具有集成的热关断保护、电流限制和低压锁定 (UVLO) 功能。TLV757P 具有内部折返电流限制，有助于在发生短路时减少热耗散。

TLV757 采用流行的 SON 和 SOT23-5 封装。此器件还采用带有散热焊盘的热增强型 SOT23-5 封装 (DYD)。与标准 SOT23-5 封装相比，此封装可显著降低热阻。

封装信息

器件型号	封装(1)	封装尺寸(2)
TLV757P	DRV（WSON，6）	2mm × 2mm
	DBV（SOT-23，5）	2.9mm × 2.8mm
	DYD（SOT-23，5）	2.9mm × 1.6mm

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

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4 Pin Configuration and Functions

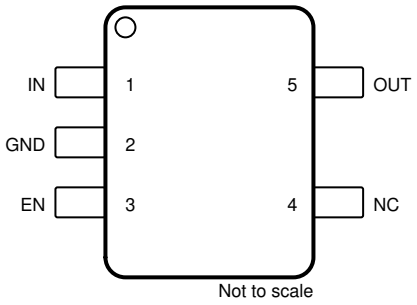


图 4-1. DBV Package, 5-Pin SOT-23 (Top View)

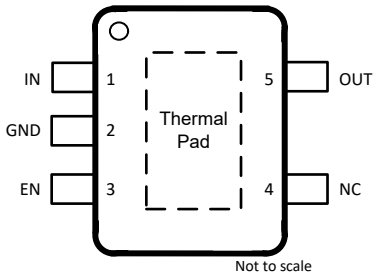


图 4-2. DYD Package, 5-Pin SOT-23 With Exposed Thermal Pad (Top View)

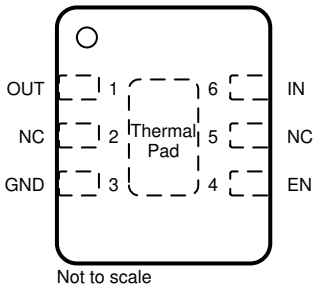


图 4-3. DRV Package, 6-Pin WSON With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DBV	DYD	DRV		
EN	3	3	4	I	Enable pin. Drive EN greater than V_{HI} to turn on the regulator. Drive EN less than V_{LO} to place the LDO into shutdown mode.
GND	2	2	3	—	Ground pin.
IN	1	1	6	I	Input pin. A capacitor with a value of 1µF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Selection* section for more information.
NC	4	4	2, 5	—	No internal connection.
OUT	5	5	1	O	Regulated output voltage pin. A capacitor with a value of 1µF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Selection* section for more information.
Thermal pad	—	Pad	Pad	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

(1) Make sure the nominal input and output capacitance are greater than 0.47µF. Throughout this document the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 0.47µF.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage,V_{IN}	–0.3	6.0	V
Enable voltage, V_{EN}	–0.3	6.0	V
Output voltage, V_{OUT}	–0.3	V_{IN} + 0.3(2)	V
Operating junction temperature range, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3V or 6.0V, whichever is smaller

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.45		5.5	V
V_{OUT}	Output voltage	0.6		5.0	V
V_{EN}	Enable voltage	0		5.5	V
I_{OUT}	Output current	0		1	A
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor	1		200	µF
f_{EN}	Enable toggle frequency			10	kHz
T_J	Junction temperature	–40		125	°C

5.4 Thermal Information

PCB	THERMAL METRIC(1) (2)		TLV757			UNIT
			DYD (SOT-23)	DBV (SOT-23)	DRV (SON)	
			5 PINS	5 PINS	6 PINS	
EVM	$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.3	100.8	N/A	°C/W
	ψ_{JT}	Junction-to-top characterization parameter	14.2	23.3	N/A	°C/W
	ψ_{JB}	Junction-to-board characterization parameter	35.9	67.8	N/A	°C/W
JEDEC	$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	231.1	100.2	°C/W
	$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.8	118.4	108.5	°C/W
	$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	64.4	64.3	°C/W
	ψ_{JT}	Junction-to-top characterization parameter	16.7	28.4	10.4	°C/W
	ψ_{JB}	Junction-to-board characterization parameter	44.9	63.8	64.8	°C/W
	$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	34.3	N/A	34.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) JEDEC thermal metrics apply to JEDEC standard PCB (2s2p, no vias to internal plane and bottom layer). EVM metrics apply to the LP087A EVM with an exposed pad SOT-23-5 (DYD) layout.

5.5 Electrical Characteristics

over operating free-air temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT} + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.45		5.5	V
V_{OUT}	Output voltage			0.6		5.0	V
	Output accuracy	–40°C ≤ T_J ≤ 85°C, V_{OUT} ≥ 1V		–1		1	%
		–40°C ≤ T_J ≤ 85°C, 0.6V ≤ V_{OUT} < 1V		–10		10	mV
		V_{OUT} ≥ 1V		–1.5		1.5	%
		0.6V ≤ V_{OUT} < 1V		–15		15	mV
$(\Delta V_{OUT})/\Delta V_{IN}$	Line regulation	V_{OUT} + 0.5V(1) ≤ V_{IN} ≤ 5.5V			2		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0.1mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 2.4V	DRV package		0.044		V/A
			DBV package		0.060		
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	0.1 mA ≤ I_{OUT} ≤ 1A, V_{IN} ≥ 2.4V	DYD package		0.069		V/A
I_{GND}	Ground current	T_J = 25°C			25	31	µA
		–40°C ≤ T_J ≤ +85°C				33	
		–40°C ≤ T_J ≤ +125°C				40	
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4V, 1.45V ≤ V_{IN} ≤ 5.5V			0.1	1	µA
I_{CL}	Output current limit	V_{IN} = V_{OUT} + $V_{DO(MAX)}$ + 0.25V	V_{OUT} = V_{OUT} - 0.2V, V_{OUT} ≤ 1.5V	1.2	1.55	1.78	A
			V_{OUT} = 0.9 x V_{OUT}, 1.5V < V_{OUT} ≤ 4.5V				
I_{SC}	Short circuit current limit	V_{OUT} = 0V, V_{IN} = V_{OUT} + $V_{DO(MAX)}$ + 0.25V			755		mA

5.5 Electrical Characteristics（续）

over operating free-air temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT} + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	I_{OUT} = 1A, –40°C ≤ T_J ≤ +85°C	0.6V ≤ V_{OUT} < 0.8V		1350	1400	mV
			0.8V ≤ V_{OUT} < 1V		1200	1300	
			0.8V ≤ V_{OUT} < 1V, DYD package		1225	1325	
			1V ≤ V_{OUT} < 1.2V		1100	1150	
			1V ≤ V_{OUT} < 1.2V, DYD package		1125	1175	
			1.2V ≤ V_{OUT} < 1.5V		1000	1050	
			1.2V ≤ V_{OUT} < 1.5V, DYD package		1025	1075	
			1.5V ≤ V_{OUT} < 1.8V		700	800	
			1.5V ≤ V_{OUT} < 1.8V, DYD package		725	825	
			1.8V ≤ V_{OUT} < 2.5V		650	750	
			1.8V ≤ V_{OUT} < 2.5V, DYD package		650	775	
			2.5V ≤ V_{OUT} < 3.3V		500	600	
			2.5V ≤ V_{OUT} < 3.3V, DYD package		525	625	
			3.3V ≤ V_{OUT} < 5.0V		300	425	
			3.3V ≤ V_{OUT} < 5.0V, DYD package		300	450	
		I_{OUT} = 1A, –40°C ≤ T_J ≤ +125°C	0.6V ≤ V_{OUT} < 0.8V			1450	
			0.8V ≤ V_{OUT} < 1V			1350	
			0.8V ≤ V_{OUT} < 1V, DYD package			1375	
			1V ≤ V_{OUT} < 1.2V			1200	
			1V ≤ V_{OUT} < 1.2V, DYD package			1225	
			1.2V ≤ V_{OUT} < 1.5V			1100	
			1.2V ≤ V_{OUT} < 1.5V, DYD package			1125	
			1.5V ≤ V_{OUT} < 1.8V			850	
			1.5V ≤ V_{OUT} < 1.8V, DYD package			875	
			1.8V ≤ V_{OUT} < 2.5V			800	
			1.8V ≤ V_{OUT} < 2.5V, DYD package			825	
			2.5V ≤ V_{OUT} < 3.3V			650	
			2.5V ≤ V_{OUT} < 3.3V, DYD package			675	
			3.3V ≤ V_{OUT} < 5.0V			475	
			3.3V ≤ V_{OUT} < 5.0V, DYD package			500	
PSRR	Power supply rejection ratio	f = 1kHz, V_{IN} = V_{OUT} + 1V, I_{OUT} = 50mA			52		dB
		f = 100kHz, , V_{IN} = V_{OUT} + 1 V, I_{OUT} = 50mA			46		
		f = 1MHz, , V_{IN} = V_{OUT} + 1V, I_{OUT} = 50mA			52		
V_n	Output noise voltage	BW = 10Hz to 100kHz, V_{OUT} = 1.2V, I_{OUT} = 1A			71.5		μV_{RMS}
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.21	1.3	1.44	V
$V_{UVLO, HYST}$	Undervoltage lockout hysteresis	V_{IN} falling			40		mV
t_{STR}	Startup time				550		µs
V_{HI}	EN pin high voltage (enabled)			1			V
V_{LO}	EN pin low voltage (enabled)					0.3	V
I_{EN}	Enable pin current	V_{IN} = 5.5V, EN = 5.5V			10		nA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 3.3V (P version only)			95		Ω

5.5 Electrical Characteristics（续）

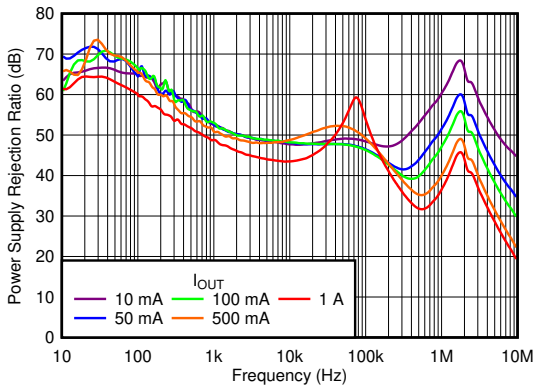
over operating free-air temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT} + 0.5 V or 1.45 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		155		°C

(1) V_{IN} = 1.45V for V_{OUT} < 0.9V

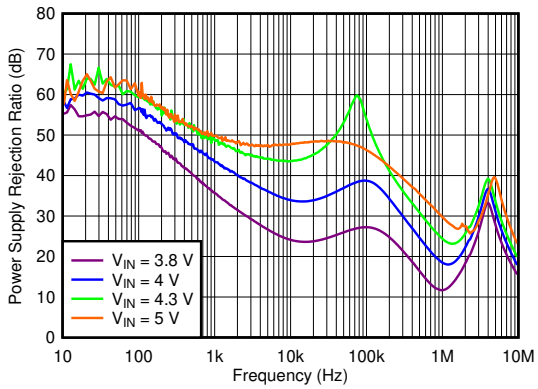
5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



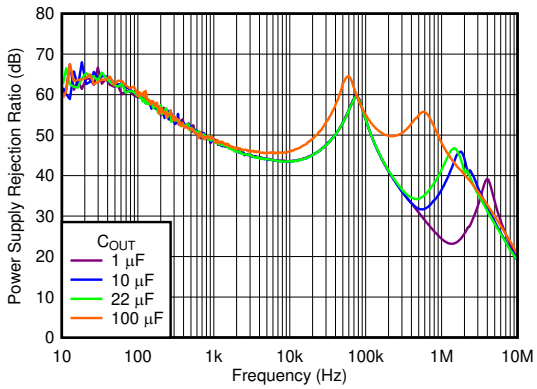
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 1µF

图 5-1. PSRR vs I_{OUT}



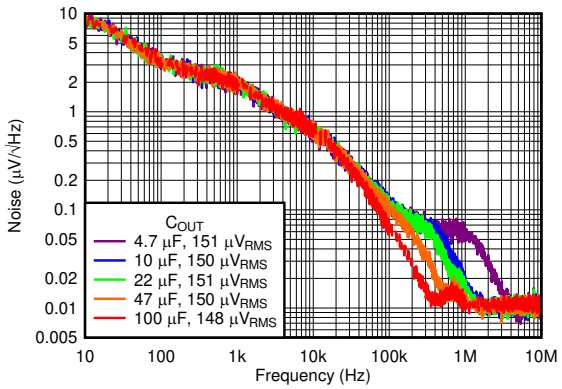
V_{OUT} = 3.3V, C_{OUT} = 1µF, I_{OUT} = 1A

图 5-2. PSRR vs V_{IN}



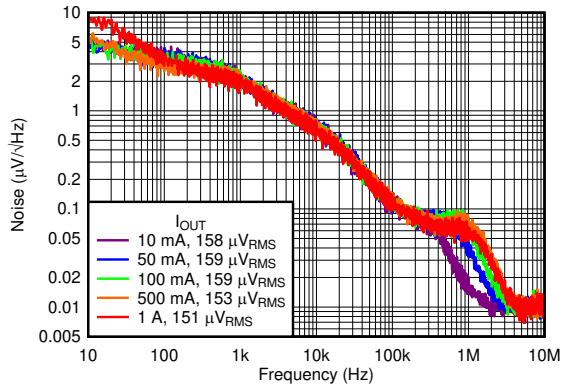
V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 1µF

图 5-3. PSRR vs C_{OUT}



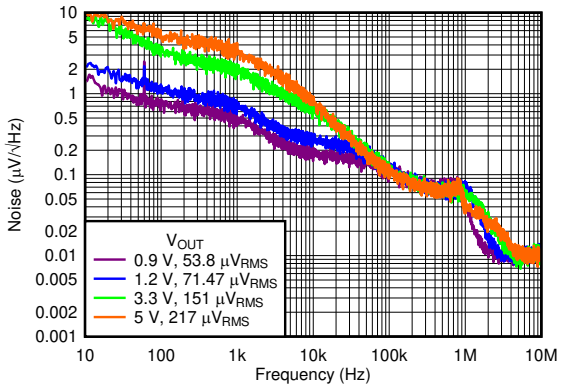
V_{OUT} = 3.3V, I_{OUT} = 1A, V_{RMS} BW = 10Hz to 100kHz

图 5-4. Output Spectral Noise Density



V_{OUT} = 3.3V, C_{OUT} = 1µF, V_{RMS} BW = 10Hz to 100kHz

图 5-5. Output Spectral Noise Density

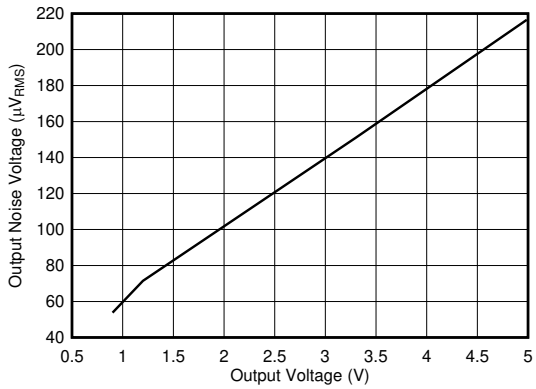


I_{OUT} = 1A, C_{OUT} = 1µF, V_{RMS} BW = 10Hz to 100kHz

图 5-6. Output Noise vs Frequency and V_{OUT}

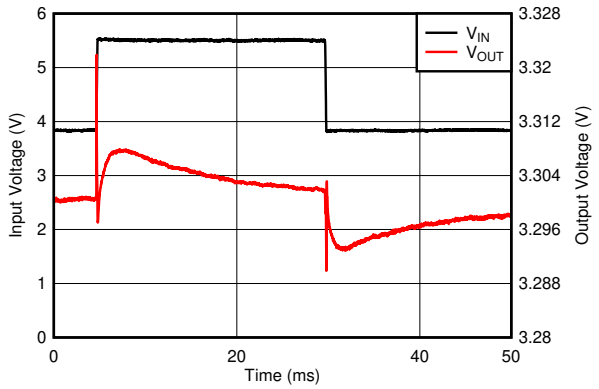
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



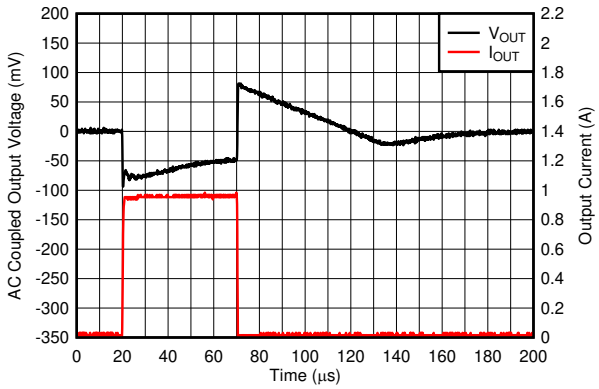
I_{OUT} = 1A, C_{OUT} = 1µF, V_{RMS} BW = 10Hz to 100kHz

图 5-7. Output Noise Voltage vs V_{OUT}



V_{OUT} = 3.3V, C_{OUT} = 1µF, V_{IN} slew rate = 1V/µs

图 5-8. Line Transient



V_{IN} = 5V, V_{OUT} = 3.3V, C_{OUT} = 1µF, I_{OUT} slew rate = 1A/µs

图 5-9. 3.3V, 1mA to 1A Load Transient

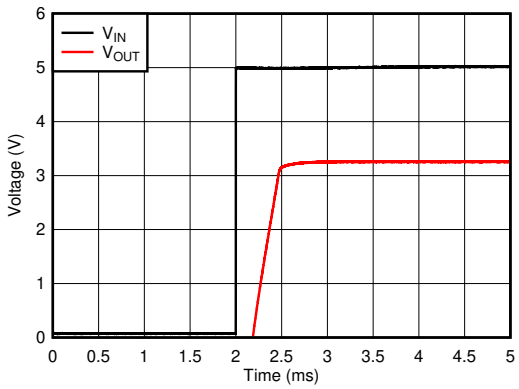


图 5-10. V_{IN} = V_{EN} Power-Up

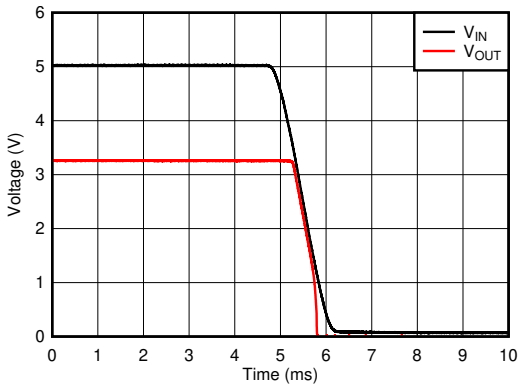
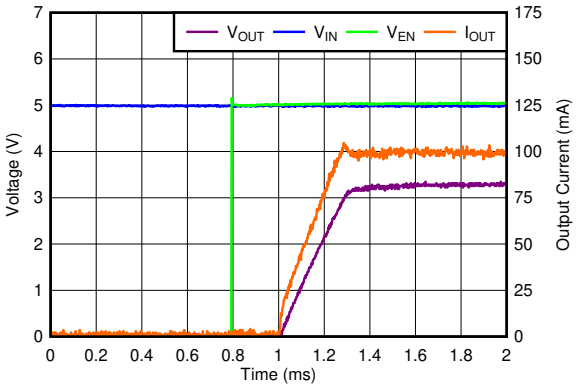


图 5-11. V_{IN} = V_{EN} Shutdown



V_{IN} = 5V, I_{OUT} = 100mA, V_{EN} slew rate = 1V/µs, V_{OUT} = 3.3V

图 5-12. EN Start-Up

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)

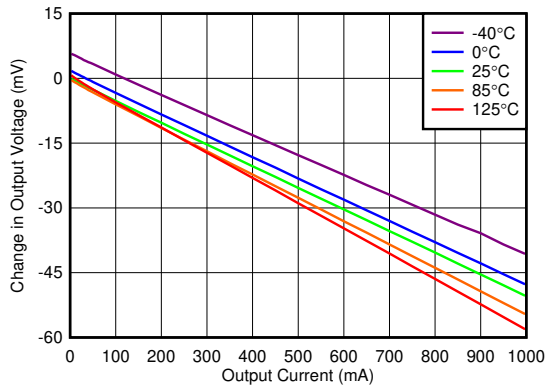


图 5-13. Load Regulation vs I_{OUT}

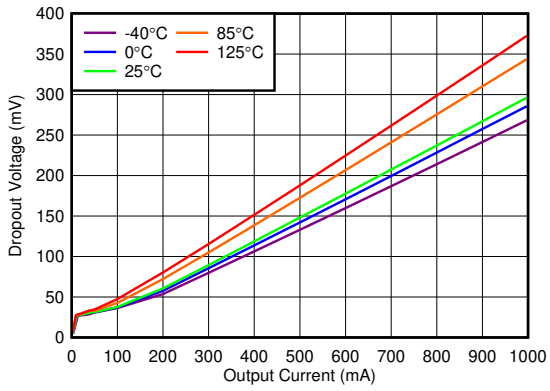


图 5-14. 3.3V Dropout Voltage vs I_{OUT}

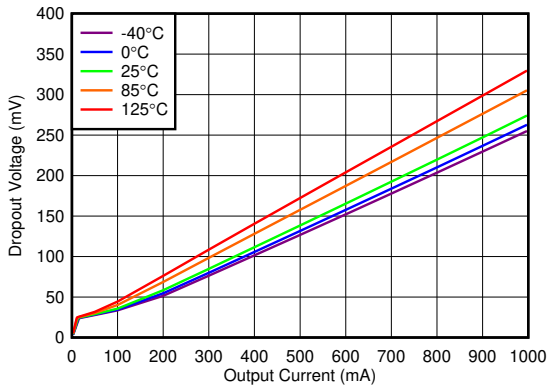
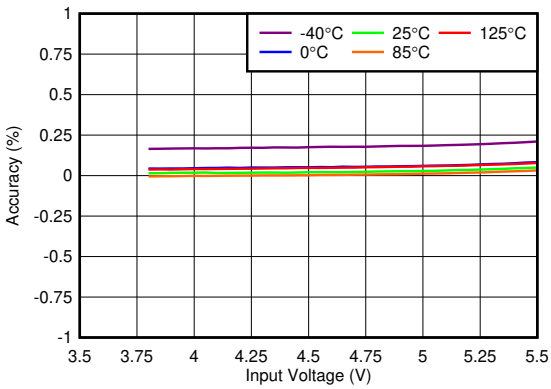
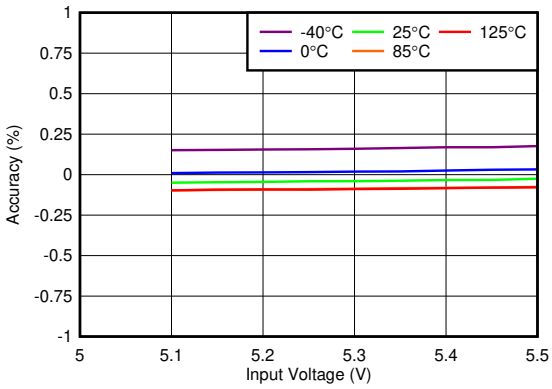


图 5-15. 5.0V Dropout Voltage vs I_{OUT}



V_{OUT} = 3.3V, I_{OUT} = 1mA

图 5-16. 3.3V Regulation vs V_{IN} (Line Regulation)



I_{OUT} = 1mA, V_{OUT} = 5V

图 5-17. 5.0V Accuracy vs V_{IN} (Line Regulation)

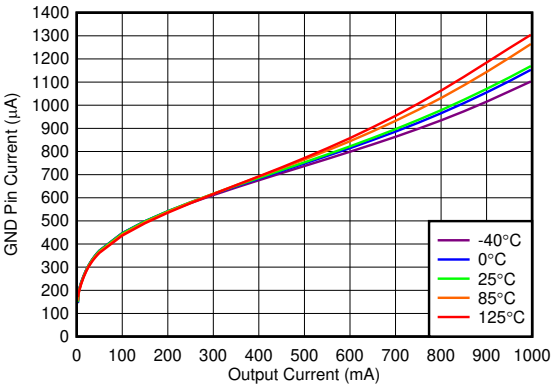
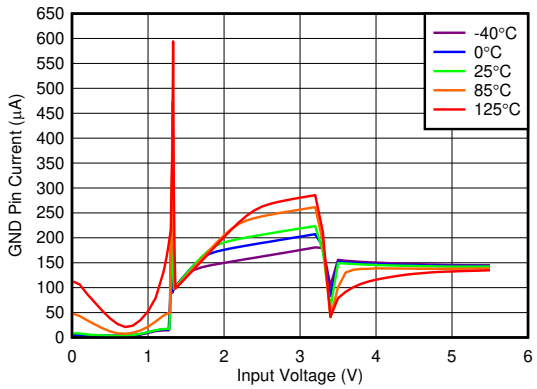


图 5-18. I_{GND} vs I_{OUT}

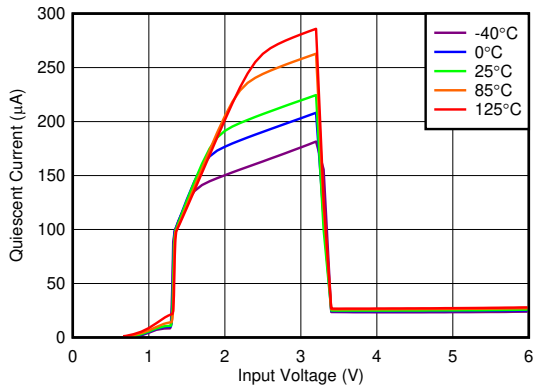
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



V_{OUT} = 3.3V, I_{OUT} = 1mA

图 5-19. I_{GND} vs V_{IN}



V_{OUT} = 3.3V, I_{OUT} = 0mA

图 5-20. I_{GND} vs V_{IN}

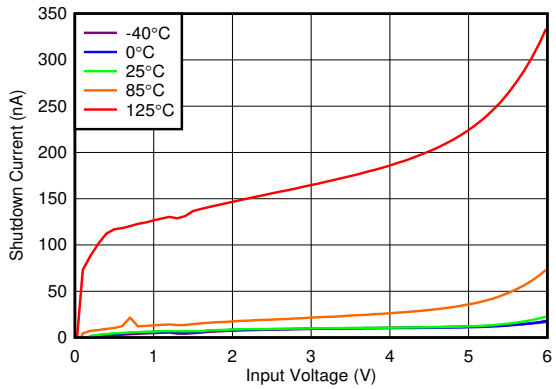


图 5-21. I_{SHDN} vs V_{IN}

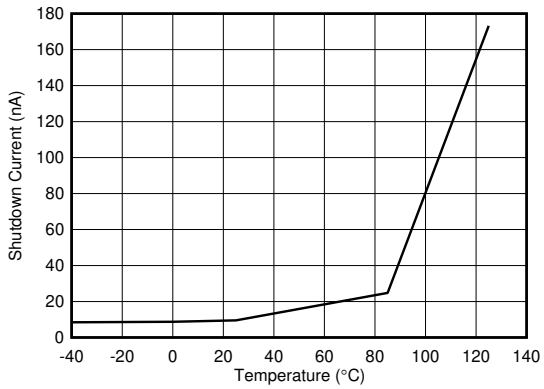


图 5-22. I_{SHDN} vs Temperature

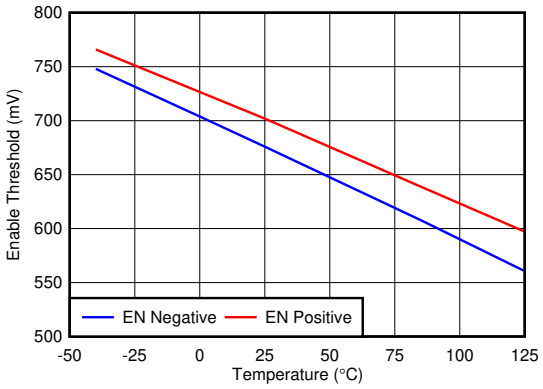
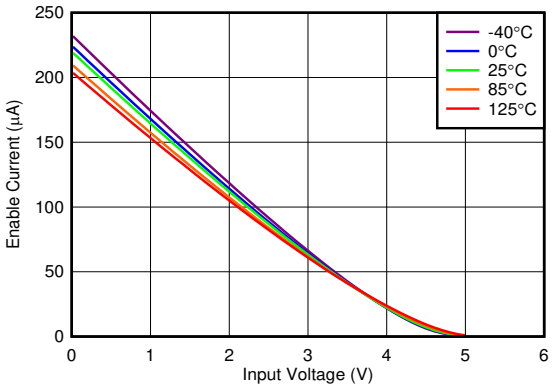


图 5-23. Enable Threshold vs Temperature



V_{EN} = 5.5V

图 5-24. I_{EN} vs V_{IN}

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 1.45V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)

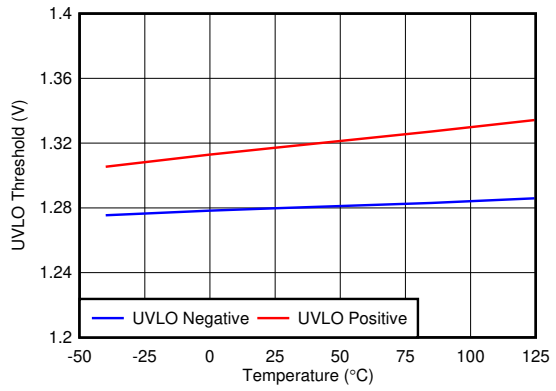


图 5-25. UVLO Threshold vs Temperature

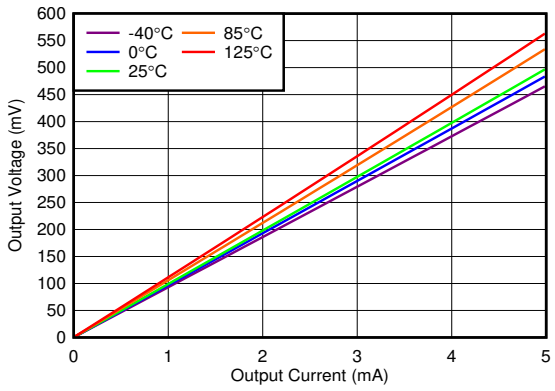


图 5-26. I_{OUT} vs V_{OUT} Pulldown Resistor

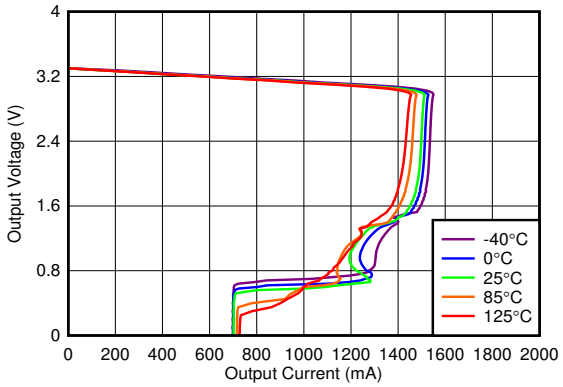


图 5-27. 3.3V Foldback Current Limit vs I_{OUT}

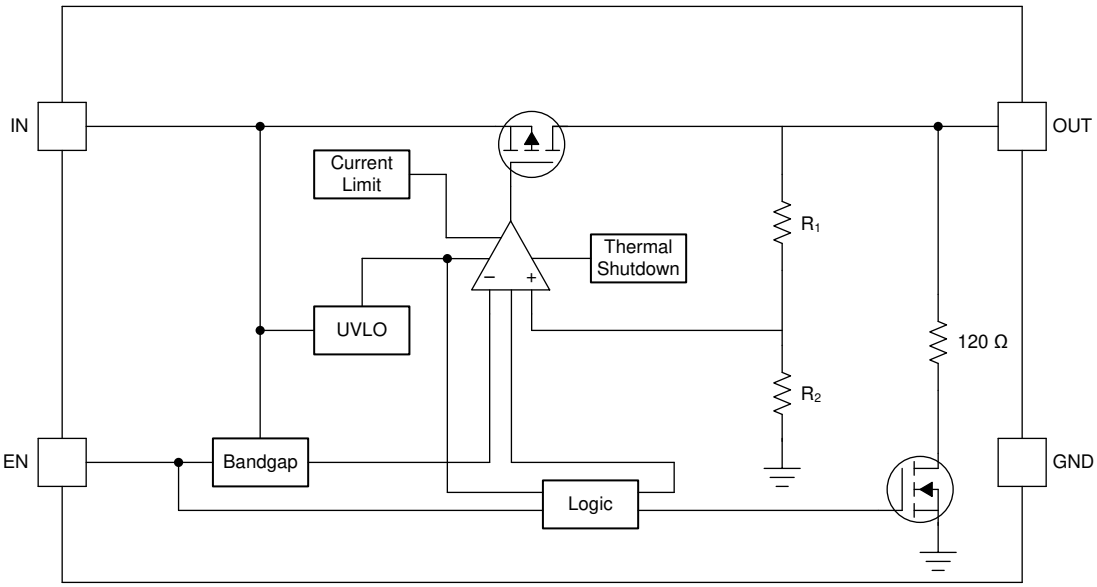
6 Detailed Description

6.1 Overview

The TLV757P is a next-generation, low-dropout regulator (LDO). This device consumes low quiescent current and delivers excellent line and load transient performance. The TLV757P is optimized for a wide variety of applications by supporting an input voltage range from 1.4V to 5.5V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 0.6V to 5V. This range supports the lower core voltages of modern microcontrollers (MCUs).

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature is –40°C to +125°C.

6.2 Functional Block Diagram



A. R_2 = 550kΩ, R_1 = adjustable.

6.3 Feature Description

6.3.1 Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit disables the output until the input voltage is greater than the rising UVLO voltage (V_{UVLO}). This circuit makes sure the device does not exhibit unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_{IN} is less than V_{UVLO}, the output is connected to ground with a 120Ω pulldown resistor.

6.3.2 Enable (EN)

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed V_{HI}. Turn off the device by forcing the EN pin below V_{LO}. If shutdown capability is not required, connect EN to IN.

The device has an internal pull-down that connects a 120Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120Ω pulldown resistor. 方程式 1 calculates the time constant τ:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

The EN pin is independent of the input pin. However, if the EN pin is driven to a higher voltage than V_{IN}, the current into the EN pin increases. This effect is illustrated in 图 5-24. When the EN voltage is higher than the input voltage there is an increased current flow into the EN pin. If this increased flow causes problems in the application, sequence the EN pin after V_{IN} is high, or tie EN to V_{IN}. If EN is driven to a higher voltage than V_{IN}, limit the frequency on EN to below 10kHz.

6.3.3 Internal Foldback Current Limit

The TLV757P has an internal current limit that protects the regulator during fault conditions. The current limit is a hybrid scheme with brick wall until the output voltage is less than 0.4 × $V_{OUT(NOM)}$. When the voltage drops below 0.4 × $V_{OUT(NOM)}$, a foldback current limit is implemented that scales back the current as the output voltage approaches GND. When the output shorts, the LDO supplies a typical current of I_{SC}. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output is shorts, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown.

The foldback current-limit circuit limits the current that is allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{CL}) during start up. See 图 5-27 for typical current limit values. If the output is loaded by a constant-current load during start up, or if the output voltage is negative when the device is enabled, then the load current demanded by the load potentially exceeds the foldback current limit. Thus, causing the device to possibly not rise to the full output voltage. For constant-current loads, disable the output load until the output rises to the nominal voltage.

Excess inductance causes the current limit to oscillate. Minimize the inductance to keep the current limit from oscillating during a fault condition.

6.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 165°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit cycles on and off. This cycling limits regulator dissipation, which protects the circuit from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the device into thermal shutdown degrades device reliability.

6.4 Device Functional Modes

表 6-1 lists a comparison between the normal, dropout, and disabled modes of operation.

表 6-1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal(1)	$V_{IN} > V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout(1)	$V_{IN} < V_{OUT(NOM)} + V_{DO}$	$V_{EN} > V_{HI}$	—	$T_J < T_{SD}$
Disabled(2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{LO}$	—	$T_J > T_{SD}$

(1) Make sure all table conditions are met.
(2) The device is disabled when any condition is met.

6.4.1 Normal Operation

The device regulates to the nominal output voltage when all of the following conditions are met.

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device degrades because the pass transistor is in a triode state and no longer controls the output voltage of the LDO. Line or load transients in dropout result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but not during start-up), the pass transistor is driven as hard as possible when the control loop is out of balance. During the normal time required for the device to regain regulation, $V_{IN} \geqslant V_{OUT(NOM)} + V_{DO}$, V_{OUT} overshoots $V_{OUT(NOM)}$ during fast transients.

6.4.3 Disabled

The output is shut down by forcing the enable pin below V_{LO}. When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal switch from the output to ground. The active pulldown is on when sufficient input voltage is provided.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

7.1.1 Input and Output Capacitor Selection

The TLV757P requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in capacitance value and equivalent series resistance (ESR) over temperature. When selecting a capacitor for a specific application, consider the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. As a general rule, make sure ceramic capacitors are derated by 50%. For best performance, use an output capacitance value no greater than 200µF.

Place a 1µF or greater capacitor on the input pin of the LDO. Some input supplies have a high impedance. Placing a capacitor on the input supply reduces the input impedance. The input capacitor counteracts reactive input sources and improves transient response and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

7.1.2 Dropout Voltage

The TLV757P uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass transistor. V_{DO} scales linearly with the output current because the PMOS transistor functions like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See 图 5-14 and 图 5-15 for typical dropout values.

7.1.3 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output overshoots on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up when the slew rate and voltage levels are in the correct range; see 图 7-1. Use an enable signal to avoid this condition.

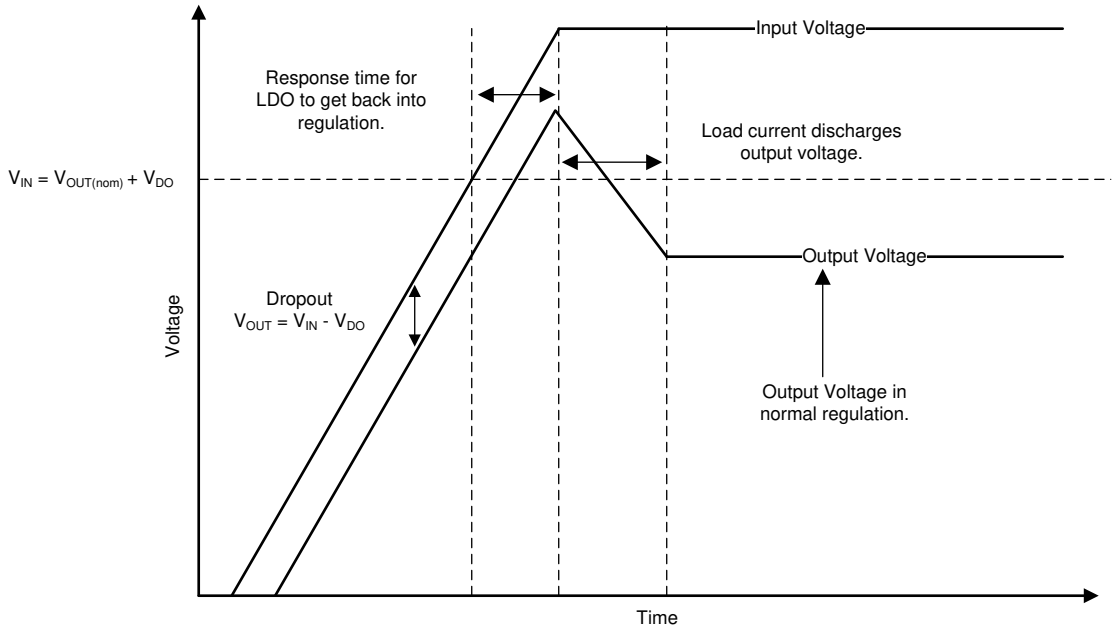


图 7-1. Start-Up Into Dropout

Line transients out of dropout also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass transistor and bring the gate back to the correct voltage for proper regulation. 图 7-2 illustrates what is happening internally with the gate voltage and how overshoot is caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to give the pass transistor the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation, which causes the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

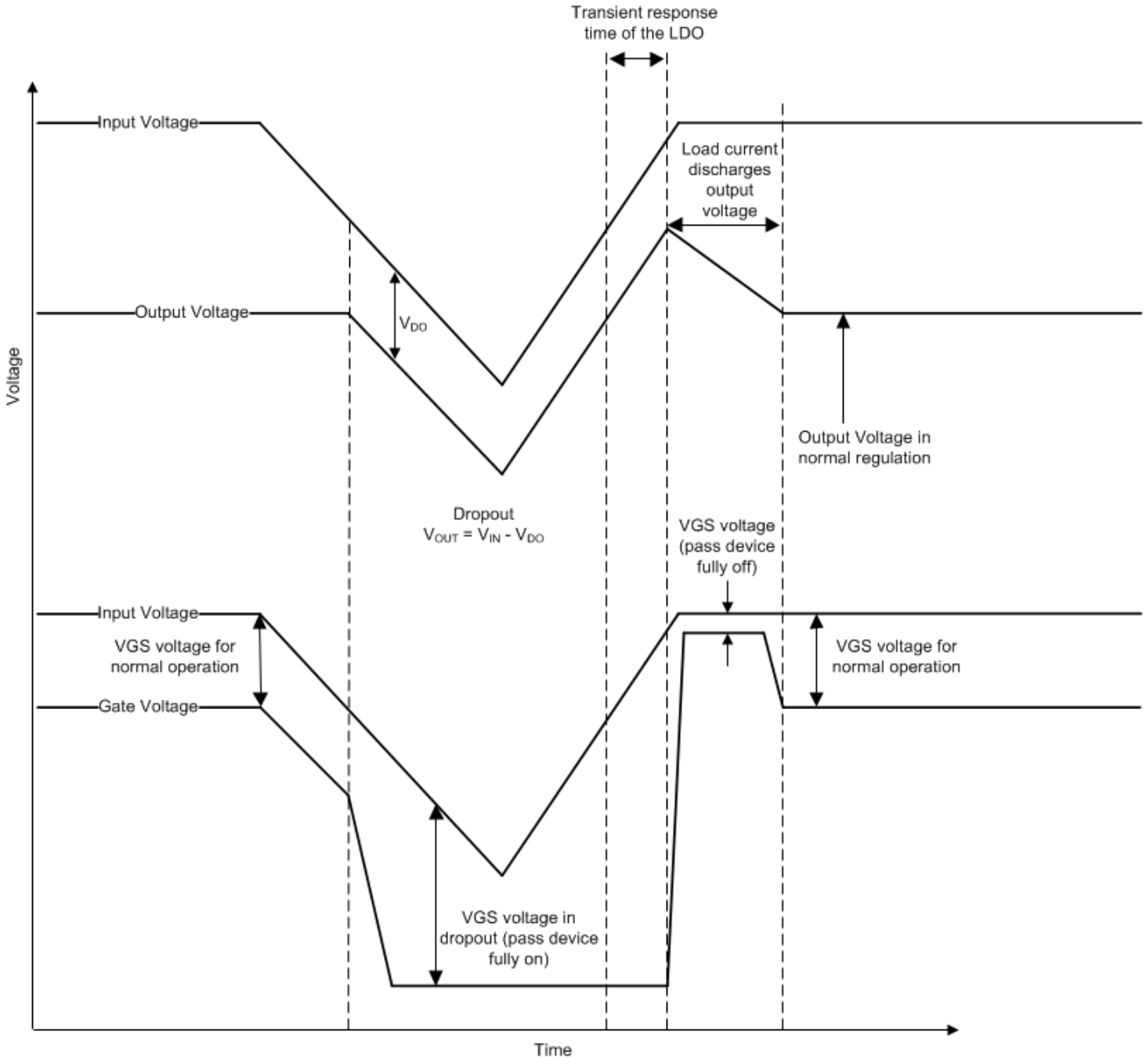


图 7-2. Line Transients From Dropout

7.1.4 Reverse Current

As with most LDOs, excessive reverse current potentially damages this device.

Reverse current flows through the body diode on the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current occurs are outlined in this section, all of which exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3V$:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. 图 7-3 shows one approach of protecting the device.

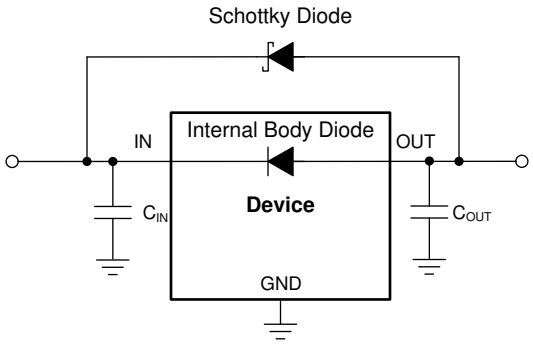


图 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator is as free of other heat-generating devices as possible that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 方程式 2 to approximate P_D:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Minimize power dissipation to achieve greater efficiency. This minimizing process is achieved by selecting the correct system voltage rails. Proper selection helps obtain the minimum input-to-output voltage differential. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, solder the thermal pad to a copper pad area under the device. Make sure this pad area contains an array of plated vias that conduct heat to inner plane areas or to a bottom-side copper plane.

The maximum allowable junction temperature (T_J) determines the maximum power dissipation for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air (T_A), according to 方程式 3.

$$T_J = T_A + R_{\theta JA} \times P_D \quad (3)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ value is only used as a relative measure of package thermal performance. $R_{\theta JA}$ is the sum of the WSON package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

7.1.5.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not thermal resistances, but offer practical and relative means of estimating junction temperatures. These psi metrics are independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are shown in the *Thermal Information* table and are used in accordance with 方程式 4.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (4)$$

where:

- P_D is the power dissipated as shown in 方程式 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.2 Typical Application

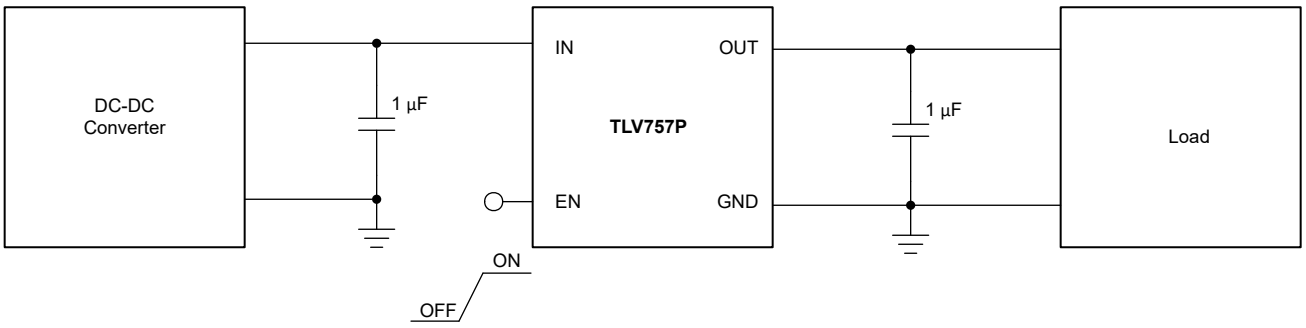


图 7-4. TLV757P Typical Application

7.2.1 Design Requirements

表 7-1 lists the design requirements for this application.

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.5V
Output voltage	1.8V
Input current	700mA (maximum)
Output load	600mA DC
Maximum ambient temperature	70°C

7.2.2 Detailed Design Procedure

7.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During start-up, the input current is higher as a result of the inrush current charging the output capacitor. Use 方程式 5 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (5)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

7.2.2.2 Thermal Dissipation

Junction temperature is determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 方程式 6 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A) to calculate the junction temperature (T_J) as 方程式 7 shows.

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (6)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (7)$$

If the ($T_{J(MAX)}$) value does not exceed 125°C, calculate the maximum ambient temperature as 方程式 8 shows. 方程式 9 calculates the maximum ambient temperature with a value of 82.916°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (8)$$

$$T_{A(MAX)} = 125°C - 100.2 \times (2.5V - 1.8V) \times (0.6A) = 82.916°C \quad (9)$$

7.2.3 Application Curves

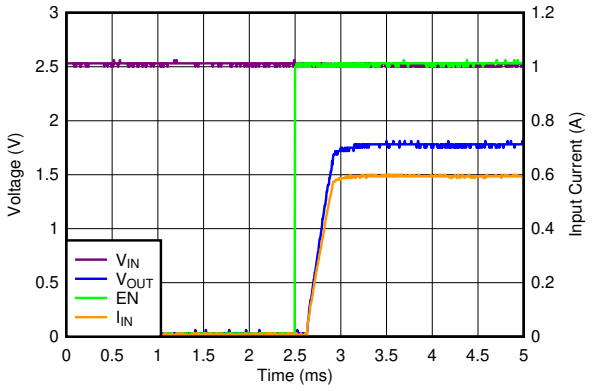
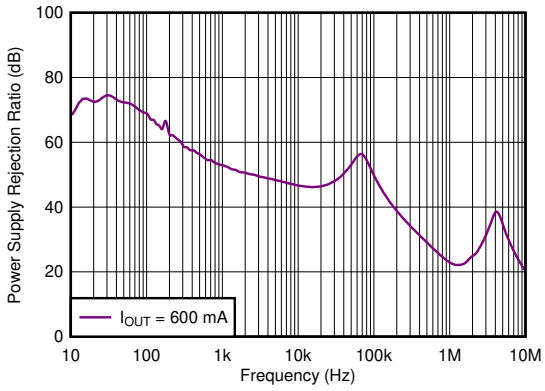


图 7-5. Start-Up With a 600mA Load



V_{IN} = 2.5V, V_{OUT} = 1.8V, I_{OUT} = 600mA

图 7-6. PSRR (2.5V to 1.8V at 600mA)

7.3 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV757P. If the input source is reactive, use multiple input capacitors in parallel with the 1µF input capacitor to lower the input supply impedance over frequency.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close as possible to the device.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- For packages with thermal pads, solder the thermal pad to copper to achieve best thermal resistance. Thermal resistance increases significantly when the thermal pad is not soldered.

7.4.2 Layout Examples

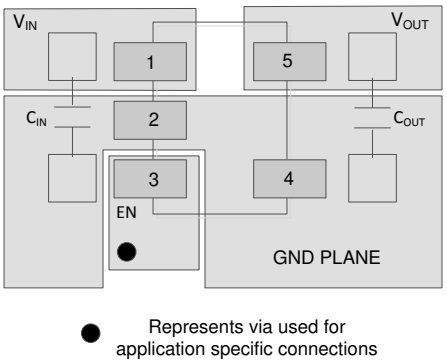


图 7-7. Layout Example: DBV Package

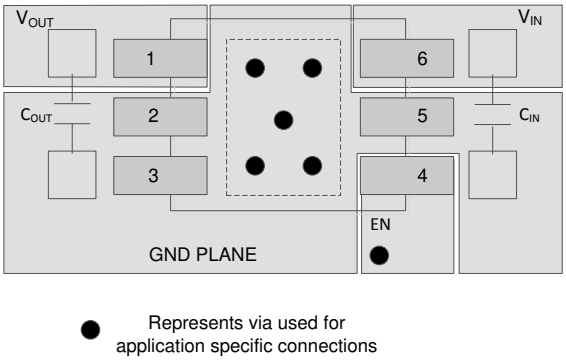


图 7-8. Layout Example: DRV Package

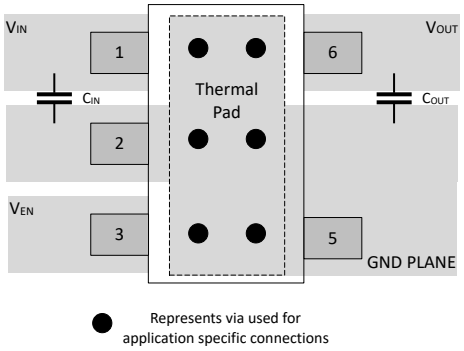


图 7-9. Layout Example: DYD Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TLV757**xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 50mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V). **P** indicates an active output discharge feature. All members of the TLV757P family actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.6V to 5V in 50mV increments are available. Contact the factory for details and availability.

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (December 2023) to Revision C (March 2024)	Page
• 将 DYD 封装从*预发布* 更改为*量产数据*	1
• 向*特性* 部分添加了 SOT-23 (DYD) 封装要点	1
• Added last bullet item to *Layout Guidelines* section	22
• Added *Layout Example: DYD Package* figure	22

Changes from Revision A (December 2017) to Revision B (December 2023) **Page**

- 将 DBV 封装从*预发布*更改为*量产数据*（正在供货）.....1
- 添加了 DYD 封装为预发布状态.....1
- 添加了指向*应用*部分的链接.....1
- 向*说明*部分添加了封装说明.....1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV75709PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1H8F	Samples
TLV75709PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HGH	Samples
TLV75710PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FEF	Samples
TLV75710PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HHH	Samples
TLV75712PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FFF	Samples
TLV75712PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HIH	Samples
TLV75712PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DVH	Samples
TLV75715PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FGF	Samples
TLV75715PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HJH	Samples
TLV75718PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FHF	Samples
TLV75718PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HKH	Samples
TLV75718PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DWH	Samples
TLV75719PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1H7F	Samples
TLV75719PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HLH	Samples
TLV75725PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FIF	Samples
TLV75725PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HMH	Samples
TLV75725PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DXH	Samples
TLV75728PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FJF	Samples
TLV75728PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HNH	Samples
TLV75728PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3DZH	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV75729PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1H9F	Samples
TLV75730PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1GHF	Samples
TLV75730PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HOH	Samples
TLV75730PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3E1H	Samples
TLV75733PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1FKF	Samples
TLV75733PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HPH	Samples
TLV75733PDYDR	ACTIVE	SOT-23	DYD	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3E2H	Samples
TLV75740PDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HQH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

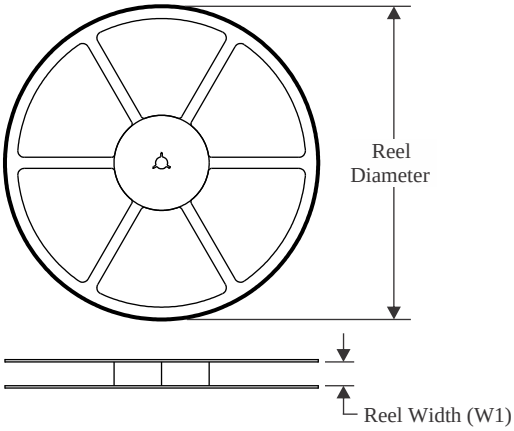
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

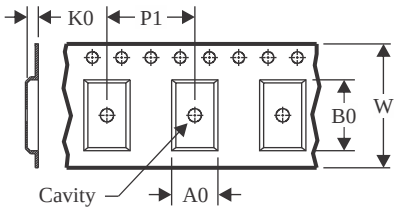
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

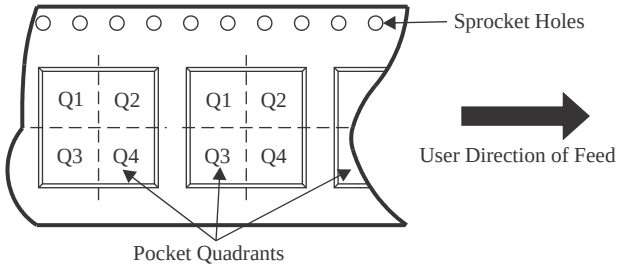


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

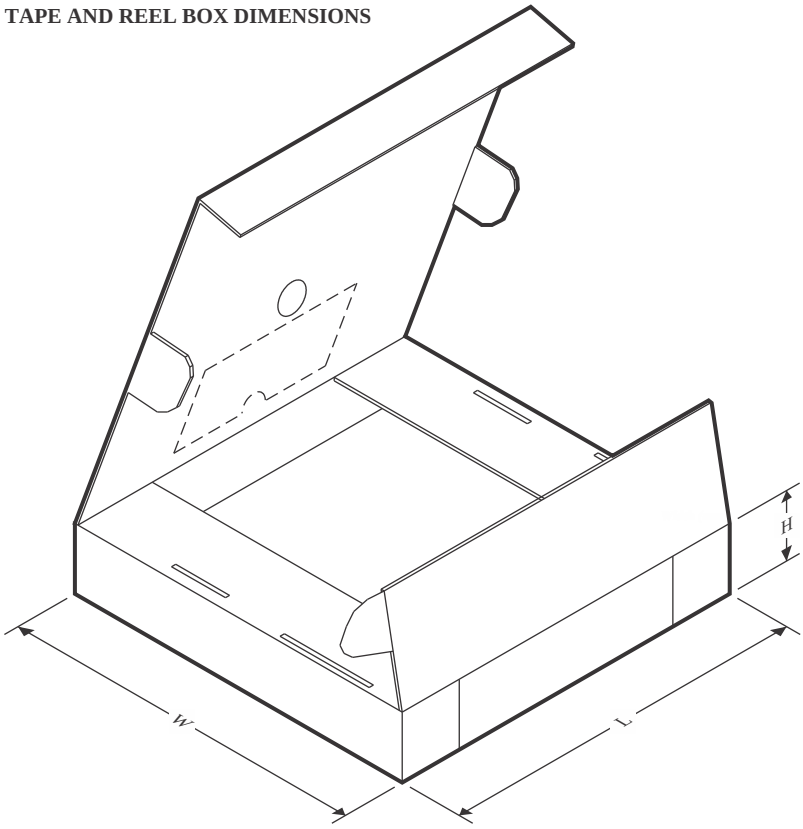


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75709PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75709PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75710PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75710PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75710PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75712PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75712PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75712PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75715PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75715PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75715PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75718PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75718PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75718PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75719PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75719PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75719PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75725PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75725PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75725PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75725PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75728PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75728PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75728PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75728PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75729PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75729PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75730PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75730PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75730PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75730PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75733PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75733PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75733PDYDR	SOT-23	DYD	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75740PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75709PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75709PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75710PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75710PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75710PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75712PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75712PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75712PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75715PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75715PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75715PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75718PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75718PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75718PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75719PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75719PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75719PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75725PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

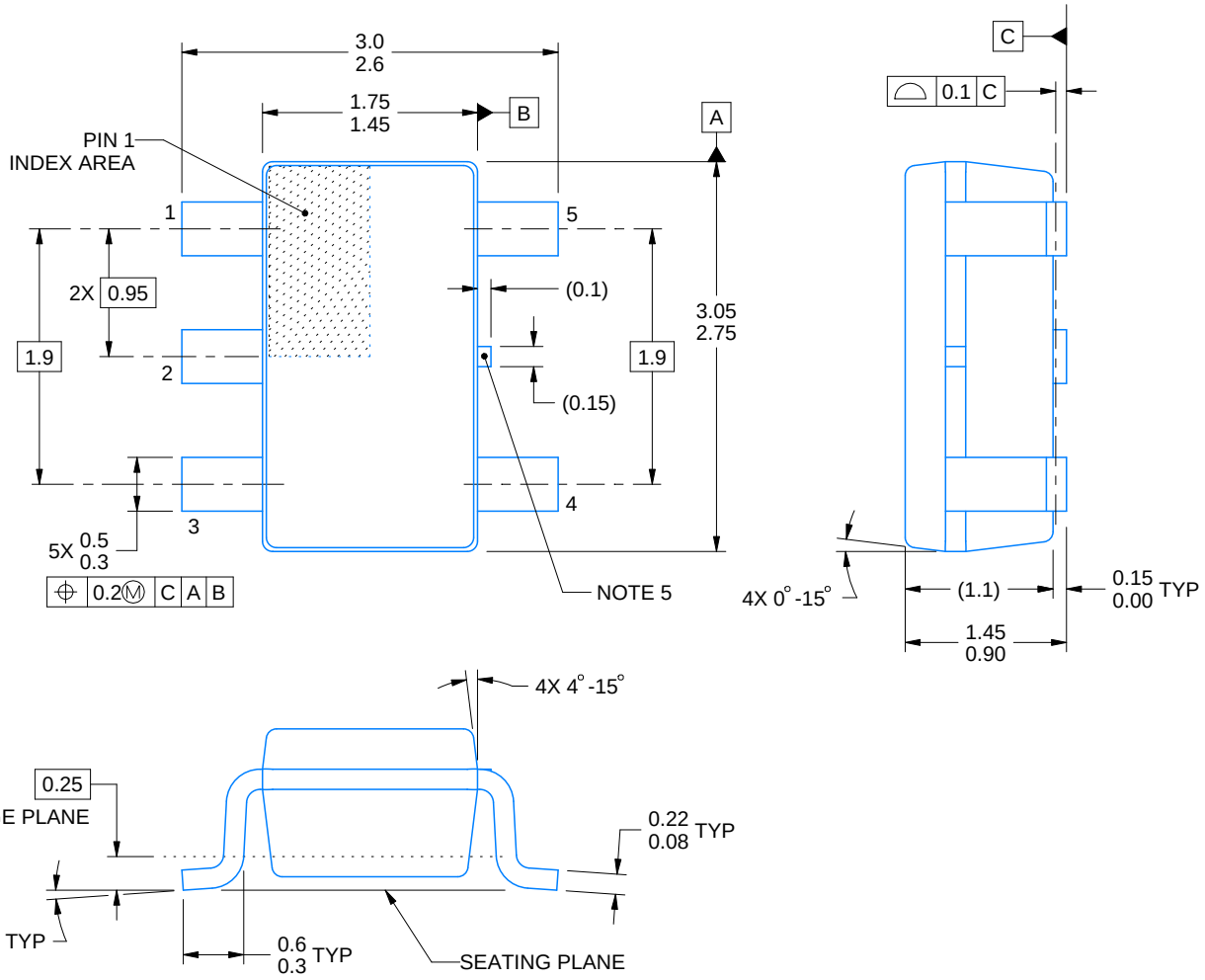
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75725PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75725PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75725PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75728PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75728PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75728PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75728PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75729PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75729PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75730PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75730PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75730PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75730PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75733PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV75733PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75733PDYDR	SOT-23	DYD	5	3000	210.0	185.0	35.0
TLV75740PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

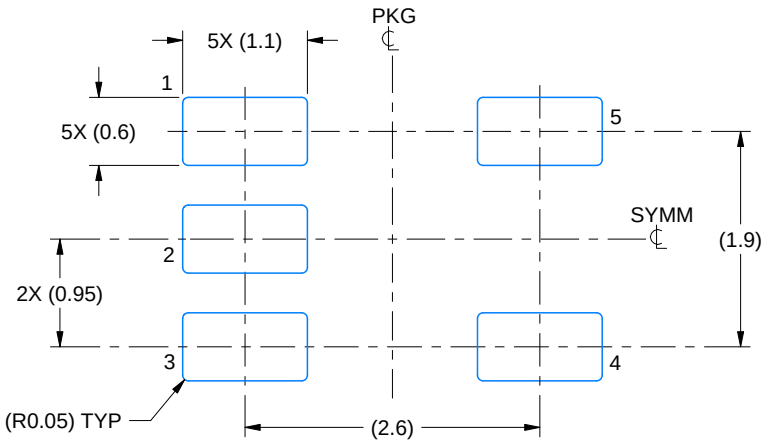
SMALL OUTLINE TRANSISTOR



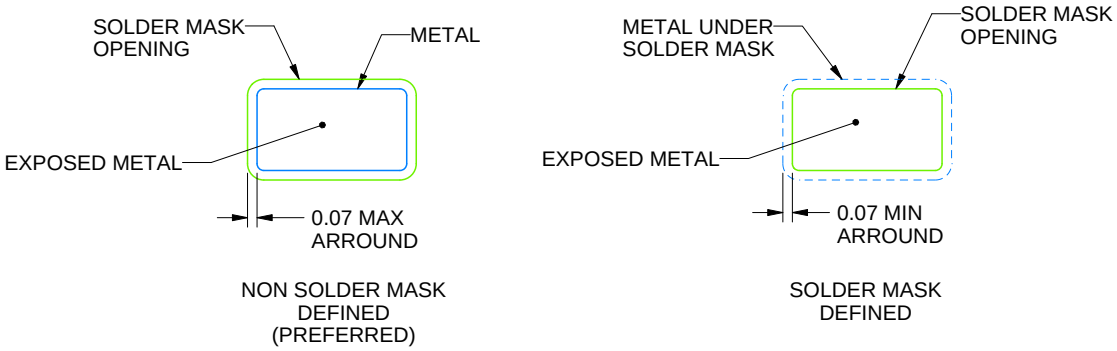
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

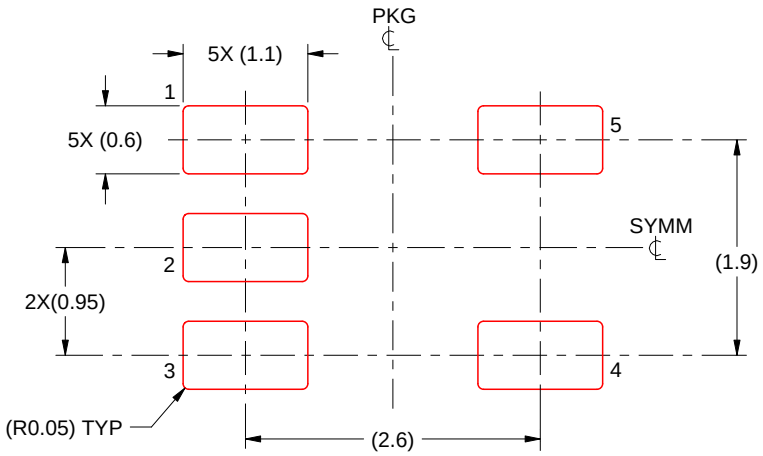


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

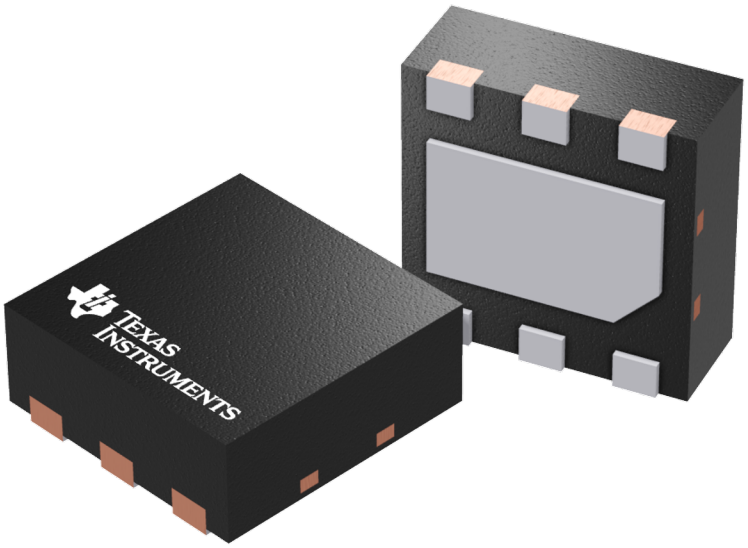
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



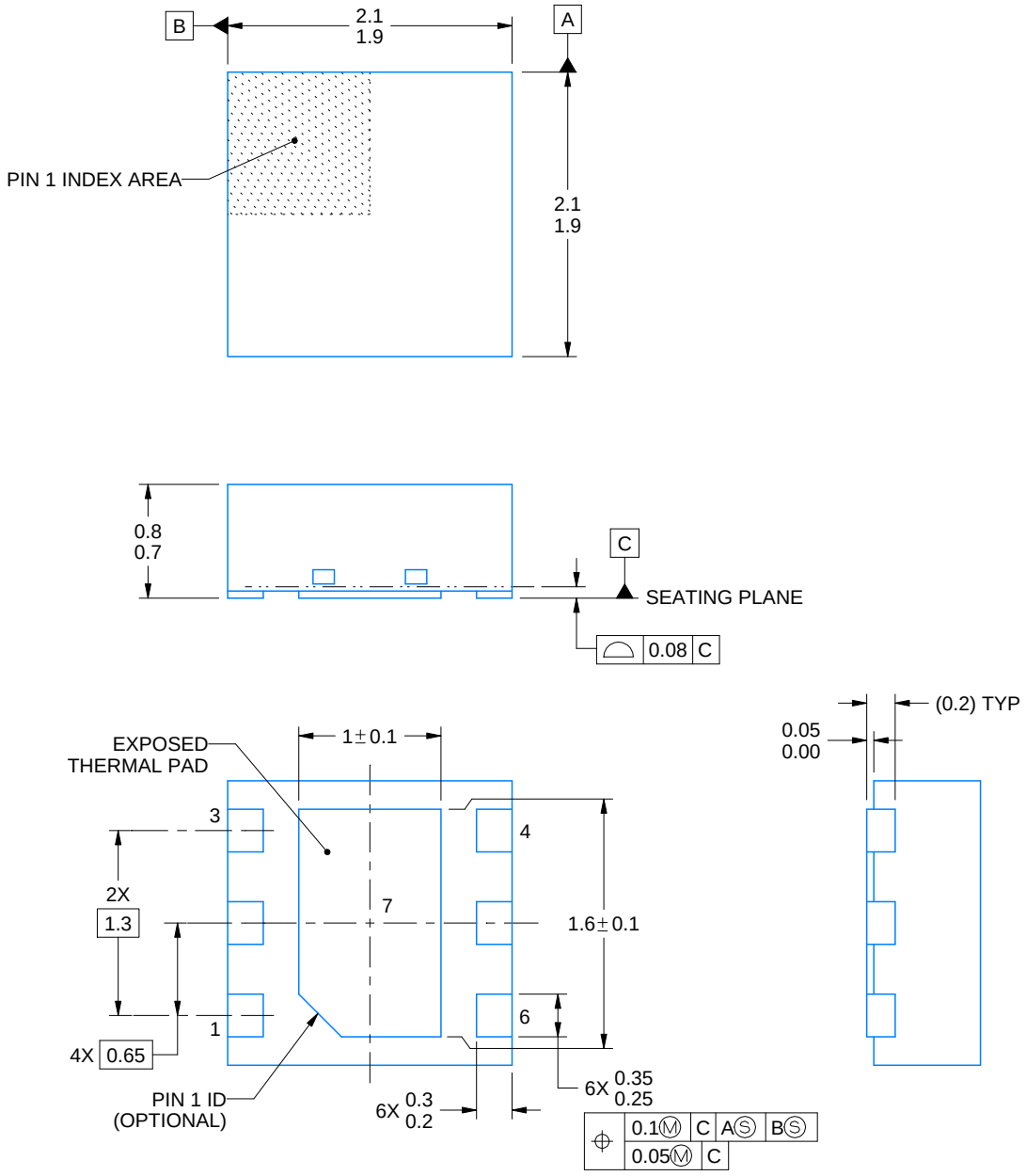
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

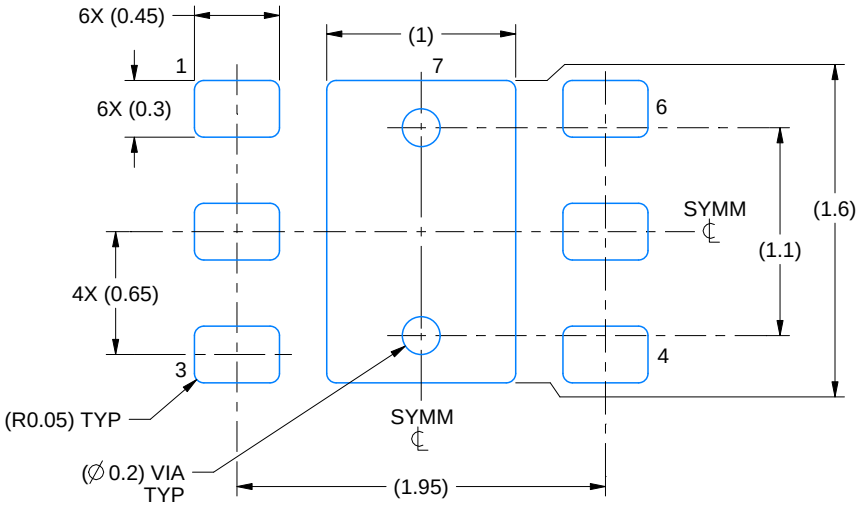
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

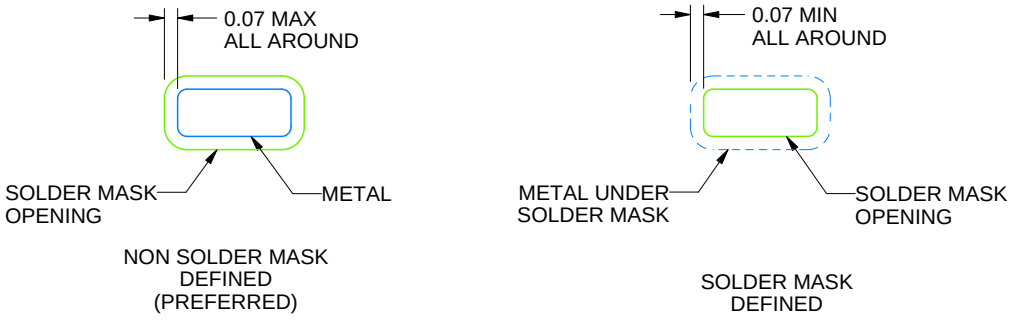


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

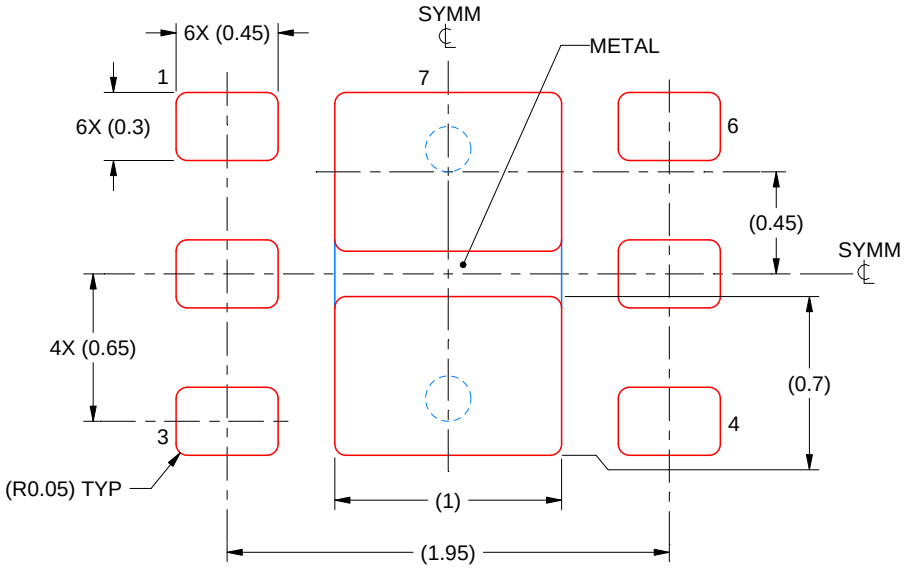
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

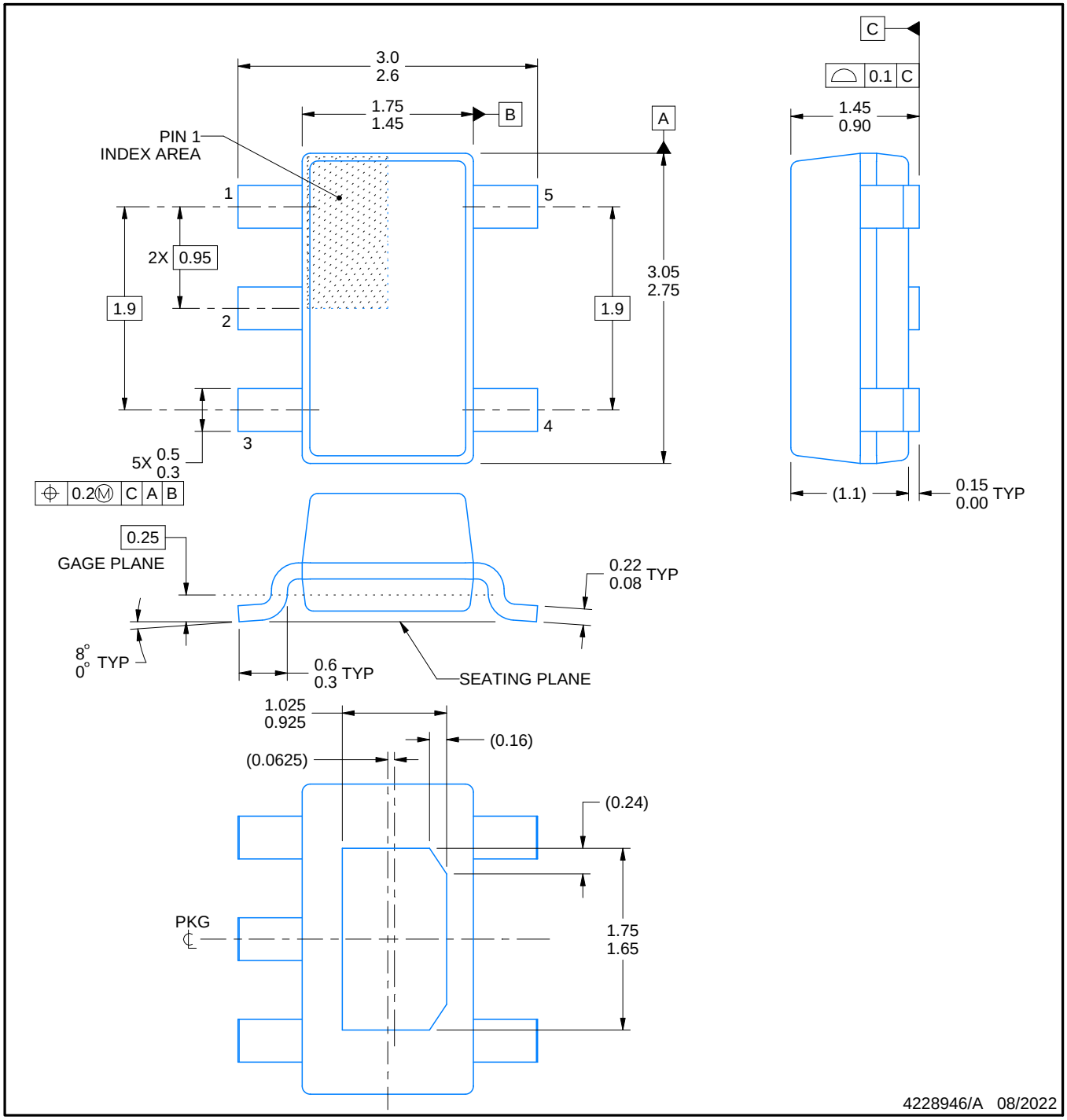
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYD0005A

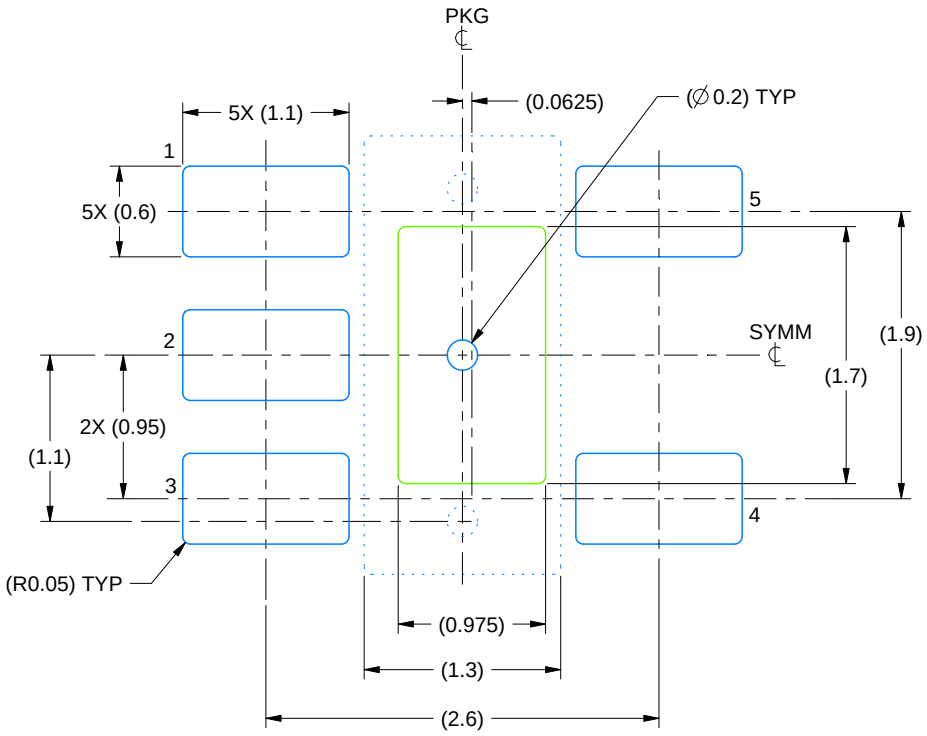
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

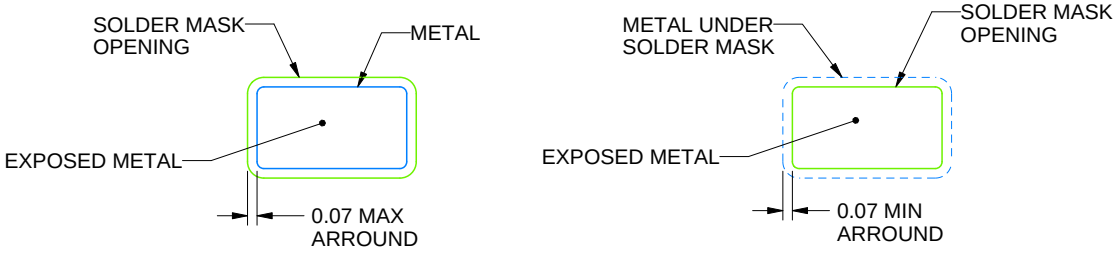


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK DEFINED (PREFERRED)

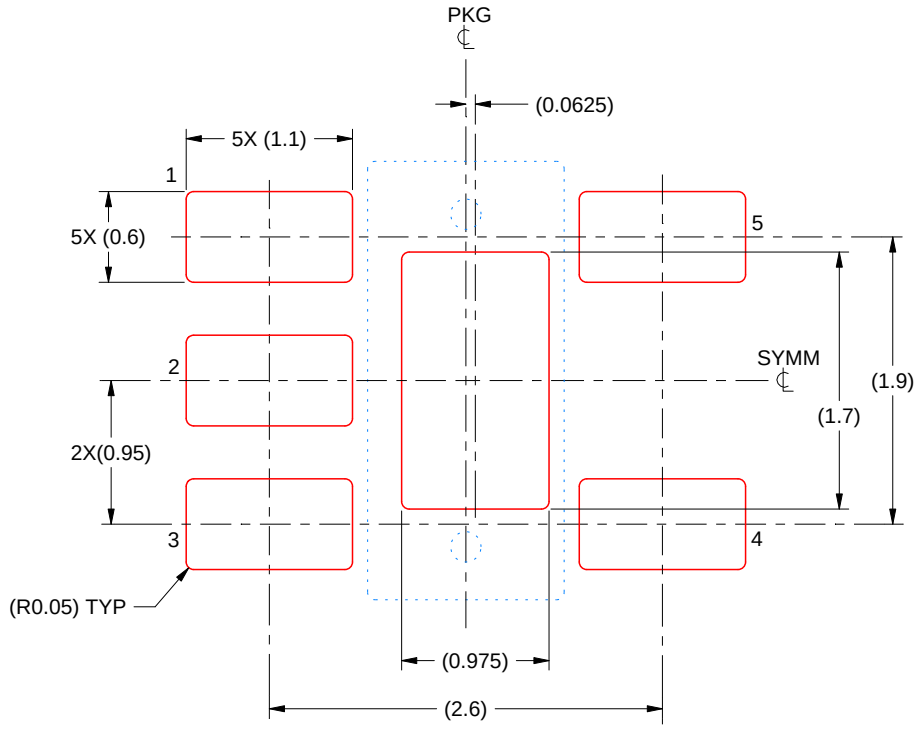
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4228946/A 08/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:20X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.100	1.09 X 1.90
0.125	0.975 X 1.700 (SHOWN)
0.150	0.89 X 1.55
0.175	0.82 X 1.44

4228946/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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