TMS320F28035-EP Piccolo™ 微控制器

1 器件概述

1.1 特性

- 高效 32 位 CPU (TMS320C28x)
  - 60MHz（16.67ns 周期时间）
  - 16 × 16 和 32 × 32 MAC 操作
  - 16 × 16 双 MAC
  - 哈佛 (Harvard) 总线架构
  - 连动运算
  - 快速中断响应和处理
  - 统一存储器编程模型
  - 高效代码（使用 C/C++ 和汇编语言）
- 可编程控制律加速器 (CLA)
  - 32 位浮点算术加速器
  - 独立于主 CPU 之外的代码执行
- 尾数法：小尾数法
- 支持 JTAG 边界扫描
  - IEEE 标准 1149.1-1990 标准测试访问端口和边界扫面架构
- 器件和系统均可实现低成本：
  - 3.3V 单电源
  - 无需电源排序
  - 集成型加电复位和欠压复位
  - 低功率
  - 无模拟支持引脚
- 计时:
  - 两个内部零引脚振荡器
  - 片载晶体振荡器及外部时钟输入
  - 看门狗定时器模块
  - 丢失时钟检测电路
- 多达 45 个具有输入滤波功能可单独编程的多路复用通用输入输出 (GPIO) 引脚
- 可支持所有外设中断的外设中断扩展 (PIE) 模块
- 三个 32 位 CPU 定时器
- 每个增强型脉宽调制器 (ePWM) 中均有一个独立的 16 位计时器
- 片载存储器
  - 闪存，SRAM，OTP，引导 ROM 可用
- 代码安全模块
- 128 位安全密钥和锁
  - 保护安全内存块
  - 防止固件逆向工程
- 串行端口外设
  - 一个串行通信接口 (SCI) 通用异步接收器/发送器 (UART) 模块
  - 两个串行外设接口 (SPI) 模块
  - 一个内部集成电路 (I2C) 模块
  - 一个本地互联网络 (LIN) 模块
  - 一个增强型控制器局域网 (eCAN) 模块
- 增强型控制外设
  - ePWM
  - 高分辨率 PWM (HRPWM)
  - 增强型捕捉 (eCAP)模块
  - 高分辨率输入捕捉 (HRCAP) 模块
  - 增强型正交编码器脉冲 (eQEP) 模块
  - 模数转换器 (ADC)
  - 片载温度传感器
  - 比较器
- 高级仿真 特性
  - 分析和断点功能
  - 通过硬件进行实时调试
- 80 引脚 PN 薄型四方扁平 (LQFP) 封装
- 支持国防、航天和医疗 应用：
  - 受控基线
  - 一个组装/测试场所
  - 一个制造场所
  - 在扩展温度范围（-55°C 至 125°C）内可用
  - 延长的产品生命周期
  - 延长的产品变更通知
  - 产品可追溯性

1.2 应用范围

- 电器
- 楼宇自动化
- 电动汽车/混合动力电动汽车 (EV/HEV) 动力传动
- 工厂自动化
- 电网基础设施
- 医疗、保健与健身
- 电机驱动器
- 电力输送
- 电信基础设施
- 测试和测量

1.3 说明

F28035 Piccolo™系列微控制器将 C28x 内核和控制律加速器 (CLA) 的性能与高度集成的控制外设整合到低引脚数的器件中。该系列器件的代码与基于 C28x 的旧版代码兼容，同时具有较高的模拟集成度。

一个内部稳压器实现了单电源轨运行。HRPWM 模块经过强化，可实现双边沿控制（调频）。增设了具有 10 位内部基准的模拟比较器，可直接进行路由以控制 PWM 输出。ADC 可在 0V 至 3.3V 的固定满量程范围内实施转换，支持 V_{REFHI}/V_{REFLO} 基准的比例运算。ADC 接口已针对低开销和延迟进行了优化。

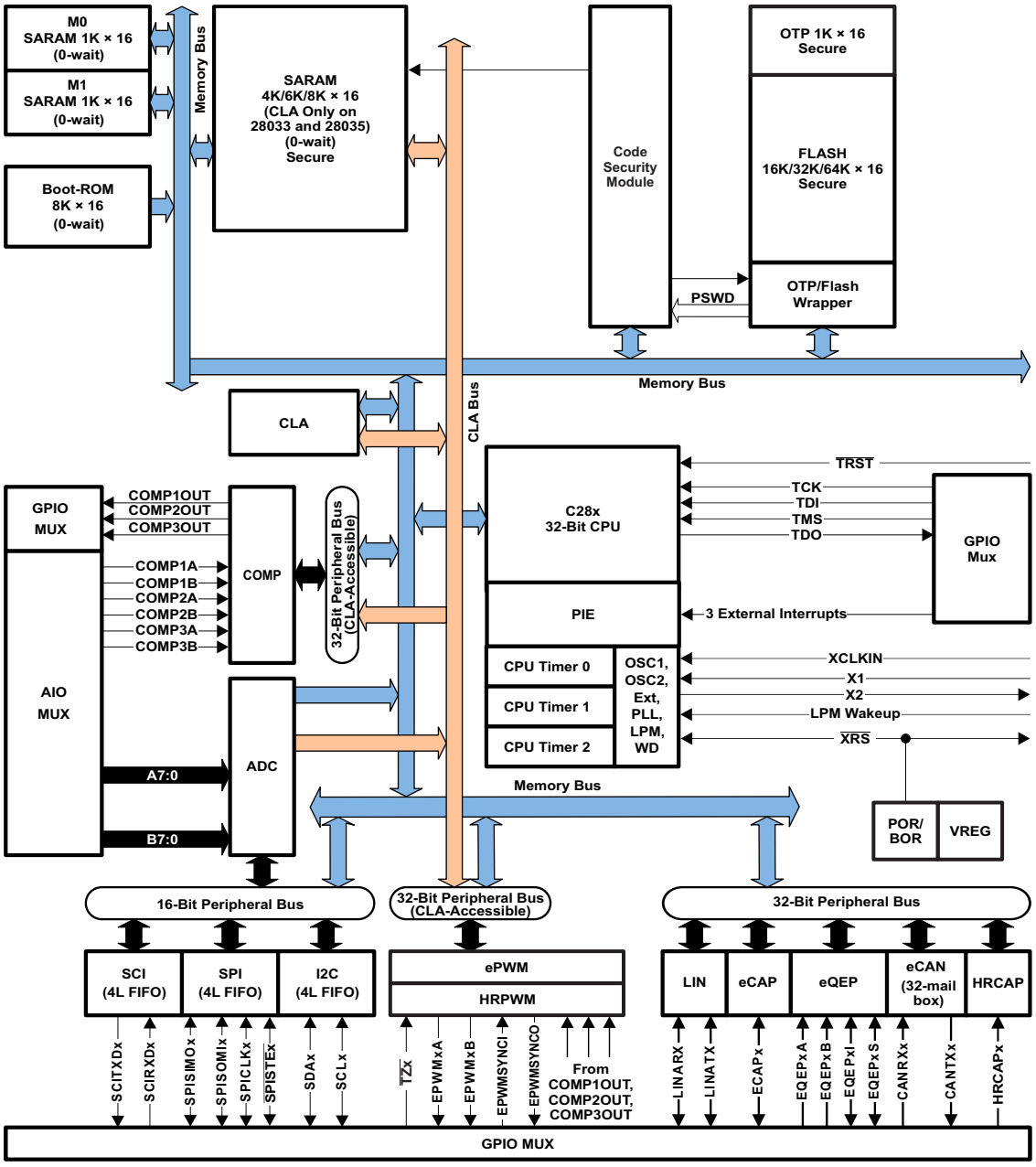
器件信息(1)

器件型号	封装	封装尺寸
TMS320F28035MPNTEP	LQFP (80)	12.0mm x 12.0mm

(1) 有关这些器件的更多信息，请参阅机械、封装和可订购信息。

1.4 功能方框图

图 1-1 展示了器件的功能方框图。



A. 由于引脚复用，所有外设引脚不能同时使用。

图 1-1. 功能方框图

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2018) to Revision A	Page
• Added Operating Life Derating Chart to the *Power-On Hours (POH) Limits* section	16

3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows the 80-pin PN Low-Profile Quad Flatpack (LQFP) pin assignments.

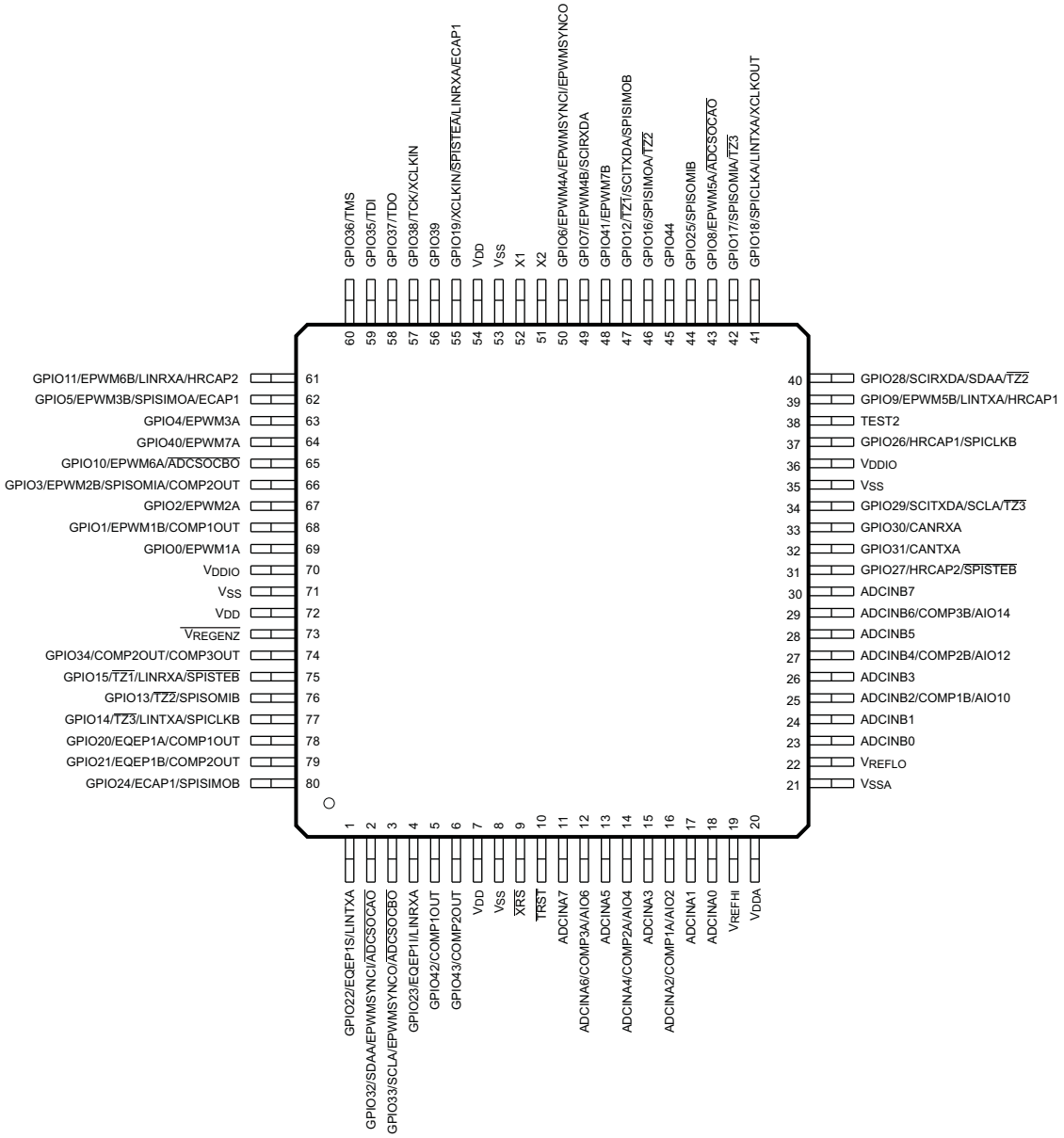


Figure 3-1. 28035 80-Pin PN LQFP (Top View)

3.2 Signal Descriptions

Table 3-1 describes the signals. With the exception of the JTAG pins, the GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. Inputs are not 5-V tolerant. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled/disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups on the PWM pins are not enabled at reset. The pullups on other GPIO pins are enabled upon reset. The AIO pins do not have an internal pullup.

NOTE

When the on-chip VREG is used, the GPIO19, GPIO34, GPIO35, GPIO36, GPIO37, and GPIO38 pins could glitch during power up. This potential glitch will finish before the boot mode pins are read and will not affect boot behavior. If glitching is unacceptable in an application, 1.8 V could be supplied externally. Alternatively, adding a current-limiting resistor (for example, 470 Ω) in series with these pins and any external driver could be considered to limit the potential for degradation to the pin and/or external circuitry. There is no power-sequencing requirement when using an external 1.8-V supply. However, if the 3.3-V transistors in the level-shifting output buffers of the I/O pins are powered before the 1.8-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins before or with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7 V.

Table 3-1. Signal Descriptions(1)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
JTAG			
$\overline{\text{TRST}}$	10	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. **NOTE:** $\overline{\text{TRST}}$ is an active high test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Because this is application-specific, TI recommends validating each target board for proper operation of the debugger and the application. (↓)
TCK	See GPIO38	I	See GPIO38. JTAG test clock with internal pullup. (↑)
TMS	See GPIO36	I	See GPIO36. JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (↑)
TDI	See GPIO35	I	See GPIO35. JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑)
TDO	See GPIO37	O/Z	See GPIO37. JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (8 mA drive)
FLASH			
TEST2	38	I/O	Test Pin. Reserved for TI. Must be left unconnected.

(1) I = Input, O = Output, Z = High Impedance, OD = Open Drain, ↑ = Pullup, ↓ = Pulldown

Table 3-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
CLOCK			
XCLKOUT	See GPIO18	O/Z	See GPIO18. Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
XCLKIN	See GPIO19 and GPIO38	I	See GPIO19 and GPIO38. External oscillator input. Pin source for the clock is controlled by the XCLKINSEL bit in the XCLK register, GPIO38 is the default selection. This pin feeds a clock from an external 3.3-V oscillator. In this case, the X1 pin, if available, must be tied to GND and the on-chip crystal oscillator must be disabled through bit 14 in the CLKCTL register. If a crystal/resonator is used, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. **NOTE:** Designs that use the GPIO38/TCK/XCLKIN pin to supply an external clock for normal device operation may need to incorporate some hooks to disable this path during debug using the JTAG connector. This is to prevent contention with the TCK signal, which is active during JTAG debug sessions. The zero-pin internal oscillators may be used during this time to clock the device.
X1	52	I	On-chip 1.8-V crystal-oscillator input. To use this oscillator, a quartz crystal or a ceramic resonator must be connected across X1 and X2. In this case, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. If this pin is not used, it must be tied to GND. (I)
X2	51	O	On-chip crystal-oscillator output. A quartz crystal or a ceramic resonator must be connected across X1 and X2. If X2 is not used, it must be left unconnected. (O)
RESET			
$\overline{\text{XRS}}$	9	I/O	Device Reset (in) and Watchdog Reset (out). Piccolo devices have a built-in power-on reset (POR) and brown-out reset (BOR) circuitry. During a power-on or brown-out condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between $\overline{\text{XRS}}$ and V_{DDIO}. If a capacitor is placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3F FFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain device with an internal pullup. (↑) If this pin is driven by an external device, TI recommends using an open-drain device.
ADC, COMPARATOR, ANALOG I/O			
ADCINA7	11	I	ADC Group A, Channel 7 input
ADCINA6	12	I	ADC Group A, Channel 6 input
COMP3A		I	Comparator Input 3A
AIO6		I/O	Digital AIO 6
ADCINA5	13	I	ADC Group A, Channel 5 input
ADCINA4	14	I	ADC Group A, Channel 4 input
COMP2A		I	Comparator Input 2A
AIO4		I/O	Digital AIO 4
ADCINA3	15	I	ADC Group A, Channel 3 input
ADCINA2	16	I	ADC Group A, Channel 2 input
COMP1A		I	Comparator Input 1A
AIO2		I/O	Digital AIO 2

Table 3-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
ADCINA1	17	I	ADC Group A, Channel 1 input
ADCINA0	18	I	ADC Group A, Channel 0 input. **NOTE:** V_{REFHI} and ADCINA0 share the same pin on the 64-pin PAG device and their use is mutually exclusive to one another. **NOTE:** V_{REFHI} and ADCINA0 share the same pin on the 56-pin RSH device and their use is mutually exclusive to one another.
V_{REFHI}	19	I	ADC External Reference High – only used when in ADC external reference mode. See Section 5.9.2.1, ADC. **NOTE:** V_{REFHI} and ADCINA0 share the same pin on the 64-pin PAG device and their use is mutually exclusive to one another. **NOTE:** V_{REFHI} and ADCINA0 share the same pin on the 56-pin RSH device and their use is mutually exclusive to one another.
ADCINB7	30	I	ADC Group B, Channel 7 input
ADCINB6	29	I	ADC Group B, Channel 6 input
COMP3B		I	Comparator Input 3B
AIO14		I/O	Digital AIO 14
ADCINB5	28	I	ADC Group B, Channel 5 input
ADCINB4	27	I	ADC Group B, Channel 4 input
COMP2B		I	Comparator Input 2B
AIO12		I/O	Digital AIO12
ADCINB3	26	I	ADC Group B, Channel 3 input
ADCINB2	25	I	ADC Group B, Channel 2 input
COMP1B		I	Comparator Input 1B
AIO10		I/O	Digital AIO 10
ADCINB1	24	I	ADC Group B, Channel 1 input
ADCINB0	23	I	ADC Group B, Channel 0 input
V_{REFLO}	22	I	ADC External Reference Low. **NOTE:** V_{REFLO} is always connected to V_{SSA} on the 64-pin PAG device and on the 56-pin RSH device.
CPU AND I/O POWER			
V_{DDA}	20		Analog Power Pin. Tie with a 2.2-µF capacitor (typical) close to the pin.
V_{SSA}	21		Analog Ground Pin. **NOTE:** V_{REFLO} is always connected to V_{SSA} on the 64-pin PAG device and on the 56-pin RSH device.
V_{DD}	7		CPU and Logic Digital Power Pins. When using internal VREG, place one 1.2-µF capacitor between each V_{DD} pin and ground. Higher value capacitors may be used.
	54		
	72		
V_{DDIO}	36		Digital I/O Buffers and Flash Memory Power Pin. Single supply source when VREG is enabled. Place a decoupling capacitor on each pin. The exact value should be determined by the system voltage regulation solution.
	70		
V_{SS}	8		Digital Ground Pins
	35		
	53		
	71		

Table 3-1. Signal Descriptions[1] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
VOLTAGE REGULATOR CONTROL SIGNAL			
$\overline{\text{VREGENZ}}$	73	I	Internal VREG Enable/Disable – pull low to enable VREG, pull high to disable VREG
GPIO AND PERIPHERAL SIGNALS [2]			
GPIO0	69	I/O/Z	General-purpose input/output 0
EPWM1A		O	Enhanced PWM1 Output A and HRPWM channel
–		–	–
–		–	–
GPIO1	68	I/O/Z	General-purpose input/output 1
EPWM1B		O	Enhanced PWM1 Output B
–			–
COMP1OUT		O	Direct output of Comparator 1
GPIO2	67	I/O/Z	General-purpose input/output 2
EPWM2A		O	Enhanced PWM2 Output A and HRPWM channel
–			–
–			–
GPIO3	66	I/O/Z	General-purpose input/output 3
EPWM2B		O	Enhanced PWM2 Output B
SPISOMIA		I/O	SPI-A slave out, master in
COMP2OUT		O	Direct output of Comparator 2
GPIO4	63	I/O/Z	General-purpose input/output 4
EPWM3A		O	Enhanced PWM3 output A and HRPWM channel
–			–
–			–
GPIO5	62	I/O/Z	General-purpose input/output 5
EPWM3B		O	Enhanced PWM3 output B
SPISIMOA		I/O	SPI-A slave in, master out
ECAP1		I/O	Enhanced Capture input/output 1
GPIO6	50	I/O/Z	General-purpose input/output 6
EPWM4A		O	Enhanced PWM4 output A and HRPWM channel
EPWMSYNCI		I	External ePWM sync pulse input
EPWMSYNCO		O	External ePWM sync pulse output
GPIO7	49	I/O/Z	General-purpose input/output 7
EPWM4B		O	Enhanced PWM4 output B
SCIRXDA		I	SCI-A receive data
–			–
GPIO8	43	I/O/Z	General-purpose input/output 8
EPWM5A		O	Enhanced PWM5 output A and HRPWM channel
–			–
$\overline{\text{ADCSOCAO}}$		O	ADC start-of-conversion A

(2) The GPIO function (shown in bold italics) is the default at reset. The peripheral signals that are listed under them are alternate functions. For JTAG pins that have the GPIO functionality multiplexed, the input path to the GPIO block is always valid. The output path from the GPIO block and the path to the JTAG block from a pin is enabled/disabled based on the condition of the $\overline{\text{TRST}}$ signal. See the *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* for details.

Table 3-1. Signal Descriptions(1) (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
GPIO9	39	I/O/Z	General-purpose input/output 9
EPWM5B		O	Enhanced PWM5 output B
LINTXA		O	LIN transmit A
HRCAP1		I	High-resolution input capture 1
GPIO10	65	I/O/Z	General-purpose input/output 10
EPWM6A		O	Enhanced PWM6 output A and HRPWM channel
–			–
$\overline{\text{ADCSOCBO}}$		O	ADC start-of-conversion B
GPIO11	61	I/O/Z	General-purpose input/output 11
EPWM6B		O	Enhanced PWM6 output B
LINRXA		I	LIN receive A
HRCAP2		I	High-resolution input capture 2
GPIO12	47	I/O/Z	General-purpose input/output 12
$\overline{\text{TZ1}}$		I	Trip Zone input 1
SCITXDA		O	SCI-A transmit data
SPISIMOB		I/O	SPI-B slave in, master out. **NOTE:** SPI-B is available only in the PN package.
GPIO13	76	I/O/Z	General-purpose input/output 13
$\overline{\text{TZ2}}$		I	Trip Zone input 2
–			–
SPISOMIB		I/O	SPI-B slave out, master in
GPIO14	77	I/O/Z	General-purpose input/output 14
$\overline{\text{TZ3}}$		I	Trip zone input 3
LINTXA		O	LIN transmit
SPICLKB		I/O	SPI-B clock input/output
GPIO15	75	I/O/Z	General-purpose input/output 15
$\overline{\text{TZ1}}$		I	Trip zone input 1
LINRXA		I	LIN receive
$\overline{\text{SPISTEB}}$		I/O	SPI-B slave transmit enable input/output
GPIO16	46	I/O/Z	General-purpose input/output 16
SPISIMOA		I/O	SPI-A slave in, master out
–			–
$\overline{\text{TZ2}}$		I	Trip Zone input 2
GPIO17	42	I/O/Z	General-purpose input/output 17
SPISOMIA		I/O	SPI-A slave out, master in
–			–
$\overline{\text{TZ3}}$		I	Trip zone input 3

Table 3-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
GPIO18	41	I/O/Z	General-purpose input/output 18
SPICLKA		I/O	SPI-A clock input/output
LINTXA		O	LIN transmit
XCLKOUT		O/Z	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
GPIO19	55	I/O/Z	General-purpose input/output 19
XCLKIN			External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken not to enable this path for clocking if it is being used for the other peripherhal functions
$\overline{\text{SPISTEA}}$		I/O	SPI-A slave transmit enable input/output
LINRXA		I	LIN receive
ECAP1		I/O	Enhanced Capture input/output 1
GPIO20	78	I/O/Z	General-purpose input/output 20
EQEP1A		I	Enhanced QEP1 input A
–			–
COMP1OUT		O	Direct output of Comparator 1
GPIO21	79	I/O/Z	General-purpose input/output 21
EQEP1B		I	Enhanced QEP1 input B
–			–
COMP2OUT		O	Direct output of Comparator 2
GPIO22	1	I/O/Z	General-purpose input/output 22
EQEP1S		I/O	Enhanced QEP1 strobe
–			–
LINTXA		O	LIN transmit
GPIO23	4	I/O/Z	General-purpose input/output 23
EQEP1I		I/O	Enhanced QEP1 index
–			–
LINRXA		I	LIN receive
GPIO24	80	I/O/Z	General-purpose input/output 24
ECAP1		I/O	Enhanced Capture input/output 1
–			–
SPISIMOB		I/O	SPI-B slave in, master out. **NOTE:** SPI-B is available only in the PN and RSH packages.
GPIO25	44	I/O/Z	General-purpose input/output 25
–			–
–			–
SPISOMIB		I/O	SPI-B slave out, master in

Table 3-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
GPIO26	37	I/O/Z	General-purpose input/output 26
HRCAP1		I	High-resolution input capture 1
–			–
SPICLKB		I/O	SPI-B clock input/output
GPIO27	31	I/O/Z	General-purpose input/output 27
HRCAP2		I	High-resolution input capture 2
–			–
$\overline{\text{SPISTEB}}$		I/O	SPI-B slave transmit enable input/output
GPIO28	40	I/O/Z	General-purpose input/output 28
SCIRXDA		I	SCI receive data
SDAA		I/OD	I2C data open-drain bidirectional port
$\overline{\text{TZ2}}$		I	Trip zone input 2
GPIO29	34	I/O/Z	General-purpose input/output 29
SCITXDA		O	SCI transmit data
SCLA		I/OD	I2C clock open-drain bidirectional port
$\overline{\text{TZ3}}$		I	Trip zone input 3
GPIO30	33	I/O/Z	General-purpose input/output 30
CANRXA		I	CAN receive
–			–
–			–
GPIO31	32	I/O/Z	General-purpose input/output 31
CANTXA		O	CAN transmit
–			–
–			–
GPIO32	2	I/O/Z	General-purpose input/output 32
SDAA		I/OD	I2C data open-drain bidirectional port
EPWMSYNCI		I	Enhanced PWM external sync pulse input
$\overline{\text{ADCSOCAO}}$		O	ADC start-of-conversion A
GPIO33	3	I/O/Z	General-Purpose Input/Output 33
SCLA		I/OD	I2C clock open-drain bidirectional port
EPWMSYNCO		O	Enhanced PWM external synch pulse output
$\overline{\text{ADCSOCBO}}$		O	ADC start-of-conversion B
GPIO34	74	I/O/Z	General-Purpose Input/Output 34
COMP2OUT		O	Direct output of Comparator 2
–			–
COMP3OUT		O	Direct output of Comparator 3
GPIO35	59	I/O/Z	General-Purpose Input/Output 35
TDI		I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK
GPIO36	60	I/O/Z	General-Purpose Input/Output 36
TMS		I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.

Table 3-1. Signal Descriptions[(1)] (continued)

TERMINAL		I/O/Z	DESCRIPTION
NAME	PN PIN NO.		
GPIO37	58	I/O/Z	General-Purpose Input/Output 37
TDO		O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK (8 mA drive)
GPIO38	57	I/O/Z	General-Purpose Input/Output 38
TCK		I	JTAG test clock with internal pullup
XCLKIN		I	External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken to not enable this path for clocking if it is being used for the other functions.
–			–
GPIO39	56	I/O/Z	General-Purpose Input/Output 39
–			–
–			–
–			–
GPIO40	64	I/O/Z	General-Purpose Input/Output 40
EPWM7A		O	Enhanced PWM7 output A and HRPWM channel
–			–
–			–
GPIO41	48	I/O/Z	General-Purpose Input/Output 41
EPWM7B		O	Enhanced PWM7 output B
–			–
–			–
GPIO42	5	I/O/Z	General-Purpose Input/Output 42
–			–
–			–
COMP1OUT		O	Direct output of Comparator 1
GPIO43	6	I/O/Z	General-Purpose Input/Output 43
–			–
–			–
COMP2OUT		O	Direct output of Comparator 2
GPIO44	45	I/O/Z	General-Purpose Input/Output 44
–			–
–			–
–			–

4 Specifications

4.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{DDIO} (I/O and Flash) with respect to V_{SS}	–0.3	4.6	V
	V_{DD} with respect to V_{SS}	–0.3	2.5	
Analog voltage	V_{DDA} with respect to V_{SSA}	–0.3	4.6	V
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
	V_{IN} (X1)	–0.3	2.5	
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital input (per pin), I_{IK} ($V_{IN} < V_{SS}$ or $V_{IN} > V_{DDIO}$)(3)	–20	20	mA
	Analog input (per pin), $I_{IKANALOG}$ ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$)	–20	20	
	Total for all inputs, $I_{IKTOTAL}$ ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$)	–20	20	
Output clamp current	I_{OK} ($V_O < 0$ or $V_O > V_{DDIO}$)	–20	20	mA
Junction temperature(4)	T_J	–55	150	°C
Storage temperature(4)	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 4.4 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ±2 mA.
(4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *Semiconductor and IC Package Thermal Metrics*.

4.2 ESD Ratings

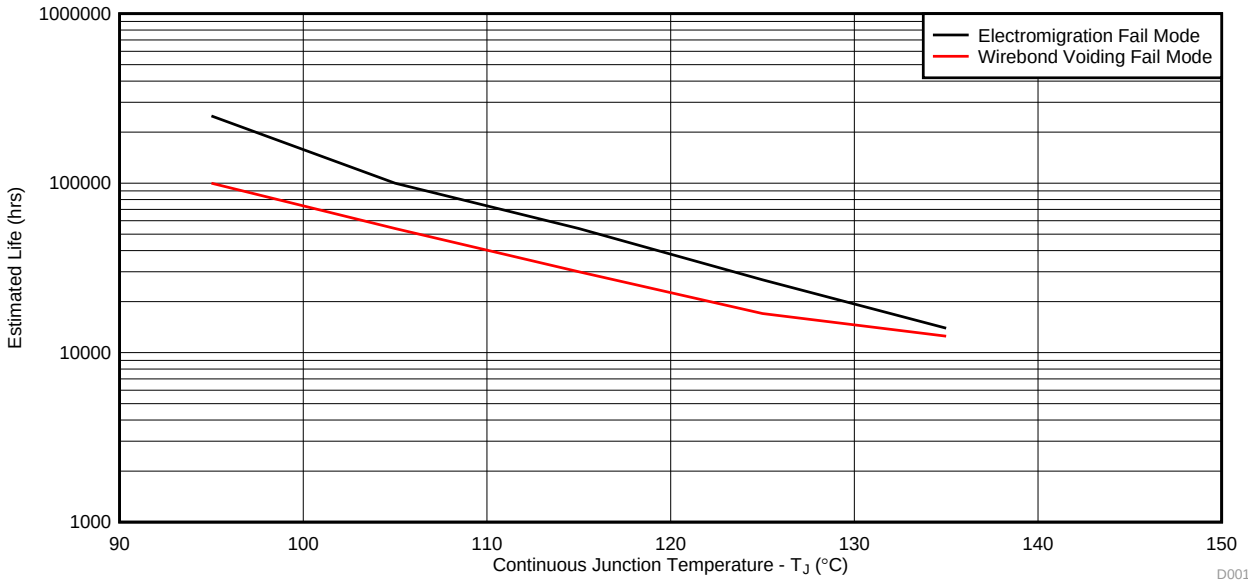
			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Power-On Hours (POH) Limits(1)

NOMINAL VCC VOLTAGE (V)	JUNCTION TEMPERATURE (T_J)	LIFETIME POH(2)
1.2	105°C	100k
	125°C	25k

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) POH represents device operation under the specified nominal conditions continuously for the duration of the calculated lifetime.



(1) Silicon operating life design goal is 100000 power-on hours (POH) at 105°C junction temperature (does not include package interconnect life).
(2) The predicted operating lifetime versus junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wear out for the specific device process and design characteristics.

Figure 4-1. TMS320F28035-EP Operating Life Derating Chart

4.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		2.97	3.3	3.63	V
Device supply voltage CPU, V_{DD} (when internal VREG is disabled and 1.8 V is supplied externally)		1.71	1.8	1.995	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA}		2.97	3.3	3.63	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)		2		60	MHz
High-level input voltage, V_{IH} (3.3 V)		2		V_{DDIO} + 0.3	V
Low-level input voltage, V_{IL} (3.3 V)		V_{SS} – 0.3		0.8	V
High-level output source current, $V_{OH} = V_{OH(MIN)}$, I_{OH}	All GPIO/AIO pins			–4	mA
	Group 2 (1)			–8	mA
Low-level output sink current, $V_{OL} = V_{OL(MAX)}$, I_{OL}	All GPIO/AIO pins			4	mA
	Group 2 (1)			8	mA
Ambient temperature, T_A		–40		125	°C

(1) Group 2 pins are as follows: GPIO16, GPIO17, GPIO18, GPIO19, GPIO28, GPIO29, GPIO36, GPIO37.

4.5 Power Consumption Summary

Table 4-1. TMS320F2803x Current Consumption at 60-MHz SYSCLKOUT

MODE	TEST CONDITIONS	VREG ENABLED				VREG DISABLED					
		I_{DDIO} (1)		I_{DDA} (2)		I_{DD}		I_{DDIO} (1)		I_{DDA} (2)	
		TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3/4/5/6/7 • eCAP1 • eQEP1 • eCAN • LIN • CLA • HRPWM • SCI-A • SPI-A/B • ADC • I2C • COMP1/2/3 • CPU-TIMER0/1/2 All PWM pins are toggled at 60 kHz. All I/O pins are left unconnected. (4) (5) Code is running out of flash with 2 wait states. XCLKOUT is turned off.	114 mA (6)	140 mA (6)	14 mA	18 mA	101 mA (6)	120 mA (6)	14 mA	23 mA	14 mA	23 mA
IDLE	Flash is powered down. XCLKOUT is turned off. All peripheral clocks are turned off.	13 mA	23 mA	10 µA	20 µA	13 mA	24 mA	120 µA	400 µA	10 µA	20µA
STANDBY	Flash is powered down. Peripheral clocks are off.	4 mA	9 mA	10 µA	20µA	4 mA	7 mA	120 µA	450 µA	10 µA	20 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled. (7)	46 µA		10 µA	20 µA	30 µA		24 µA		10 µA	20 µA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) To realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(3) The TYP numbers are applicable over room temperature and nominal voltage.
(4) The following is done in a loop:
- Data is continuously transmitted out of SPI-A/B, SCI-A, eCAN, LIN, and I2C ports.
- The hardware multiplier is exercised.
- Watchdog is reset.
- ADC is performing continuous conversion.
- COMP1/2 are continuously switching voltages.
- GPIO17 is toggled.

(5) CLA is continuously performing polynomial calculations.
(6) For F2803x devices that do not have CLA, subtract the I_{DD} current number for CLA (see Table 4-2) from the I_{DD} (VREG disabled)/I_{DDIO} (VREG enabled) current numbers shown in Table 4-1 for operational mode.
(7) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.

NOTE

The peripheral - I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

4.5.1 Reducing Current Consumption

The 28035 devices incorporate a method to reduce the device current consumption. Because each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. Table 4-2 indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 4-2. Typical Current Consumption by Various Peripherals (at 60 MHz)(1)

PERIPHERAL MODULE(2)	I_{DD} CURRENT REDUCTION (mA)
ADC	2(3)
I2C	3
ePWM	2
eCAP	2
eQEP	2
SCI	2
SPI	2
COMP/DAC	1
HRPWM	3
HRCAP	3
CPU-TIMER	1
Internal zero-pin oscillator	0.5
CAN	2.5
LIN	1.5
CLA	20

(1) All peripheral clocks (except CPU Timer clock) are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.
(3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well.

NOTE

I_{DDIO} current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

NOTE

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 40 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

Following are other methods to reduce power consumption further:

- The flash module may be powered down if code is run off SARAM. This results in a current reduction of 18 mA (typical) in the V_{DD} rail and 13 mA (typical) in the V_{DDIO} rail.
- Savings in I_{DDIO} may be realized by disabling the pullups on pins that assume an output function.

4.5.2 Current Consumption Graphs (VREG Enabled)

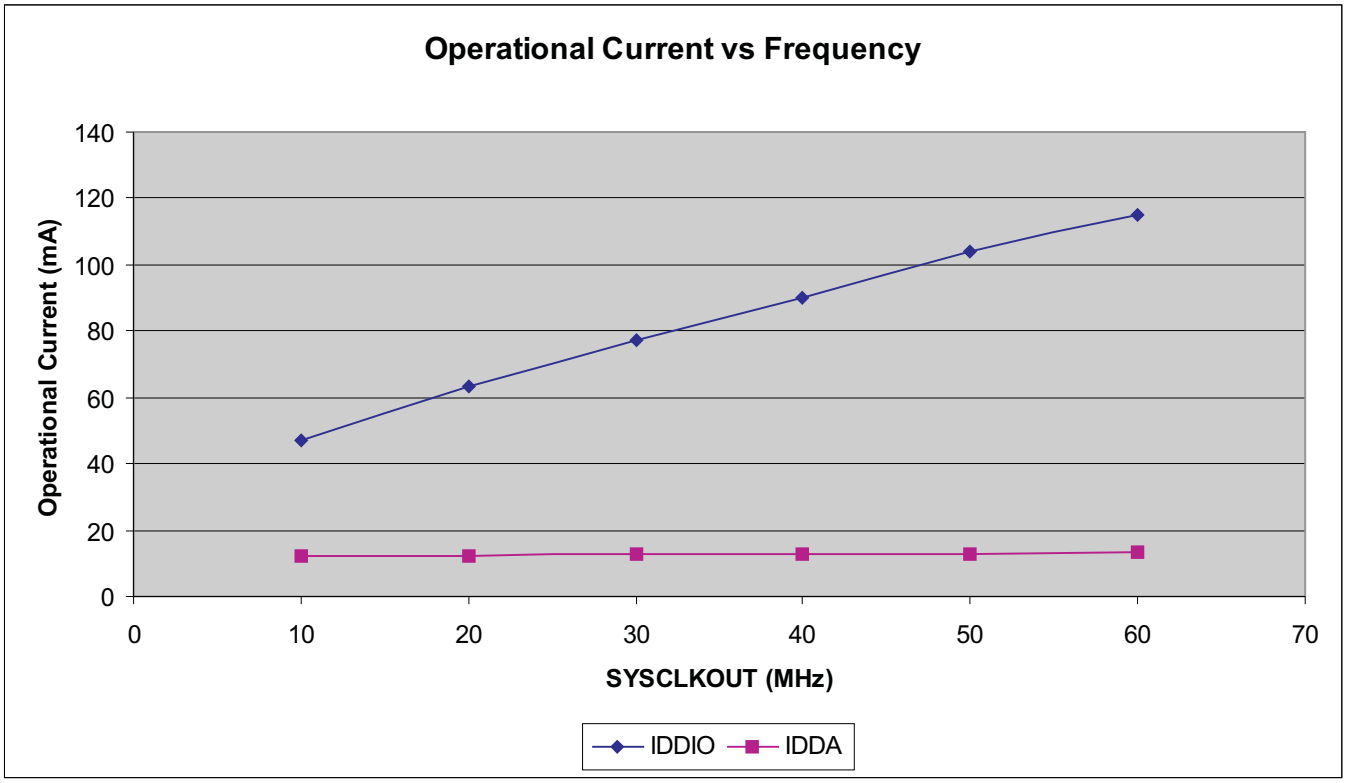


Figure 4-2. Typical Operational Current Versus Frequency (F2803x)

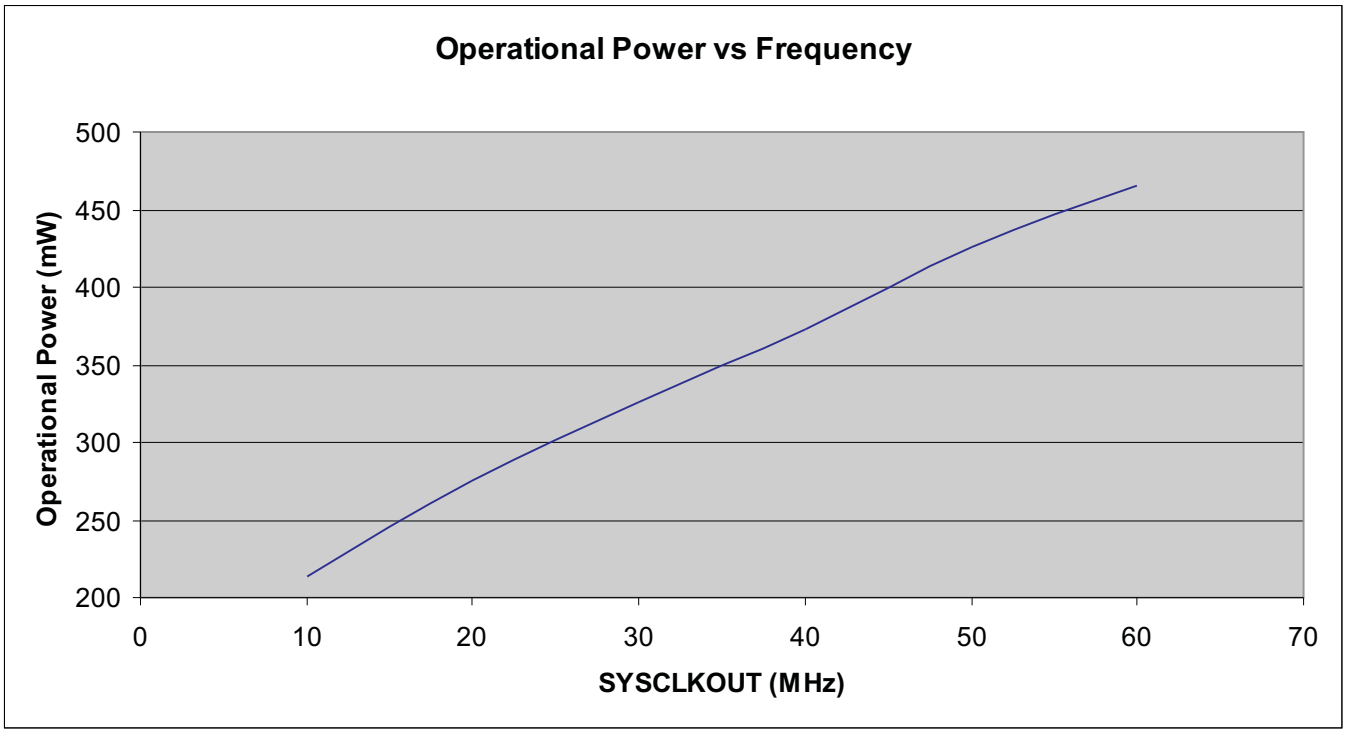


Figure 4-3. Typical Operational Power Versus Frequency (F2803x)

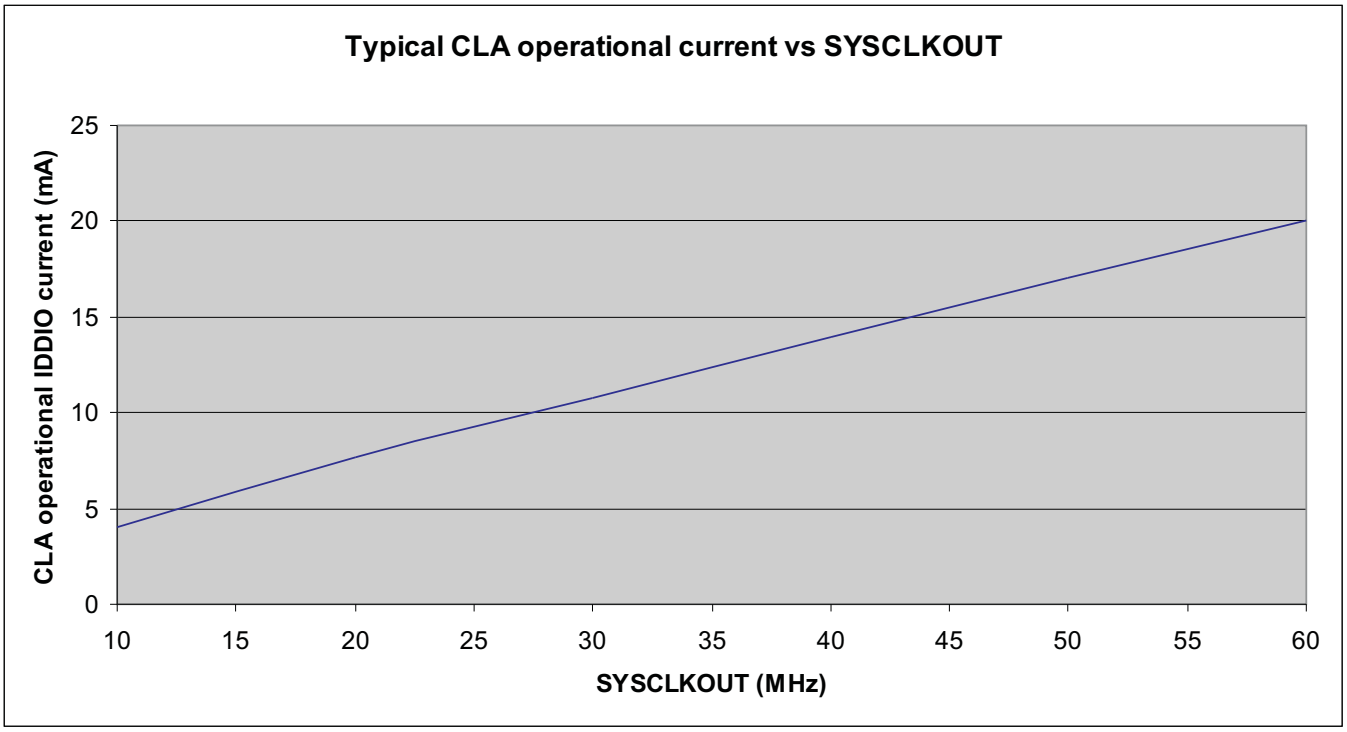


Figure 4-4. Typical CLA Operational Current Versus SYSCLKOUT

4.6 Electrical Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MAX		2.4			V
			I_{OH} = 50 μA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All GPIO	–80	–140	–205	μA
				$\overline{XRS}$ pin	–230	–300	–375	
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}				±2	μA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}		28	50	80	
I_{OZ}	Output current, pullup or pulldown disabled		V_O = V_{DDIO} or 0 V				±2	μA
C_I	Input capacitance					2		pF
	V_{DDIO} BOR trip point		Falling V_{DDIO}		2.50	2.78	2.96	V
	V_{DDIO} BOR hysteresis					35		mV
	Supervisor reset release delay time		Time after BOR/POR/OVR event is removed to $\overline{XRS}$ release		400		800	μs
	VREG V_{DD} output		Internal VREG on			1.9		V

(1) When the on-chip VREG is used, its output is monitored by the POR/BOR circuit, which will reset the device should the core voltage (V_{DD}) go out of range.

4.7 Thermal Resistance Characteristics

Table 4-3. PN Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	14.2	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	21.9	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	49.9	0
		38.3	150
		36.7	250
		34.4	500
Psi_{JT}	Junction-to-package top	0.8	0
		1.18	150
		1.34	250
		1.62	500
Psi_{JB}	Junction-to-board	21.6	0
		20.7	150
		20.5	250
		20.1	500

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

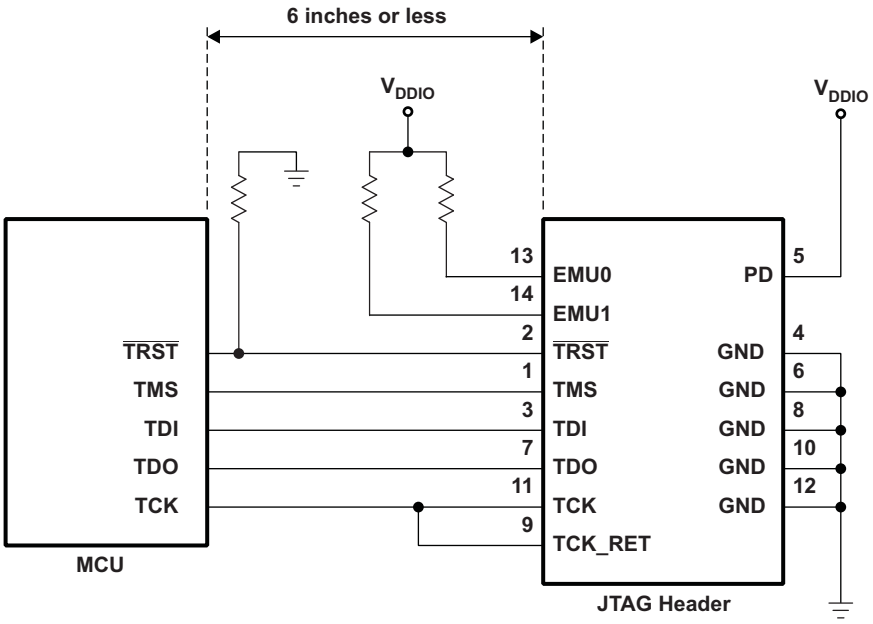
(2) lfm = linear feet per minute

4.8 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

4.9 Emulator Connection Without Signal Buffering for the MCU

Figure 4-5 shows the connection between the MCU and JTAG header for a single-processor configuration. If the distance between the JTAG header and the MCU is greater than 6 inches, the emulation signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 4-5 shows the simpler, no-buffering situation. For the pullup/pulldown resistor values, see Section 3.2, Signal Descriptions.



A. See Figure 5-41 for JTAG/GPIO multiplexing.

Figure 4-5. Emulator Connection Without Signal Buffering for the MCU

NOTE

The 28035 device does not have EMU0/EMU1 pins. For designs that have a JTAG Header onboard, the EMU0/EMU1 pins on the header must be tied to V_{DDIO} through a 4.7-kΩ (typical) resistor.

4.10 Parameter Information

4.10.1 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

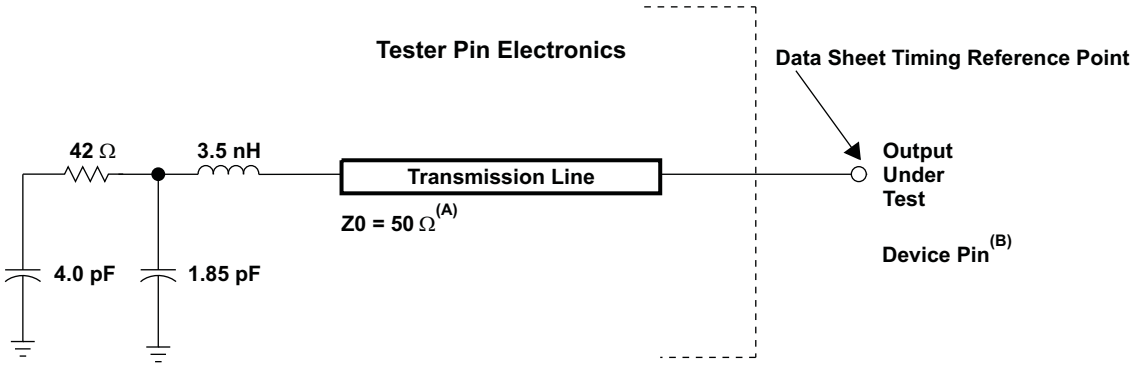
4.10.2 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

4.11 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



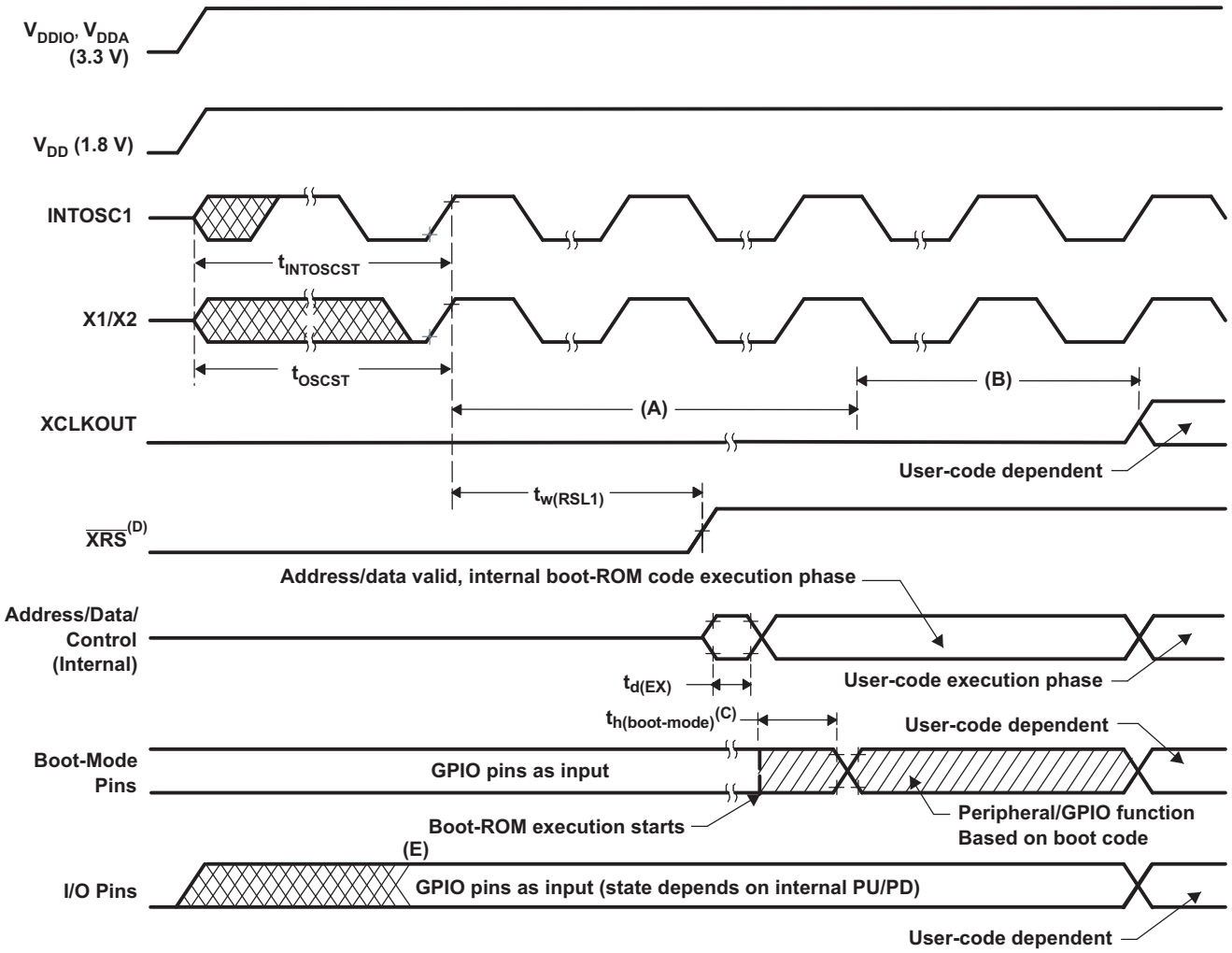
A. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

B. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 4-6. 3.3-V Test Load Circuit

4.12 Power Sequencing

There is no power sequencing requirement needed to ensure the device is in the proper state after reset or to prevent the I/Os from glitching during power up/down (GPIO19, GPIO34–38 do not have glitch-free I/Os). No voltage larger than a diode drop (0.7 V) above V_{DDIO} should be applied to any digital pin (for analog pins, this value is 0.7 V above V_{DDA}) before powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.



A. Upon power up, SYSCLKOUT is OSCCLK/4. Because the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. XCLKOUT = OSCCLK/16 during this phase.

B. Boot ROM configures the DIVSEL bits for /1 operation. XCLKOUT = OSCCLK/4 during this phase. XCLKOUT will not be visible at the pin until explicitly configured by user code.

C. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

D. Using the $\overline{\text{XRS}}$ pin is optional due to the on-chip power-on reset (POR) circuitry.

E. The internal pullup/pulldown will take effect when BOR is driven high.

Figure 4-7. Power-On Reset

Table 4-4. Reset ($\overline{XRS}$) Timing Requirements

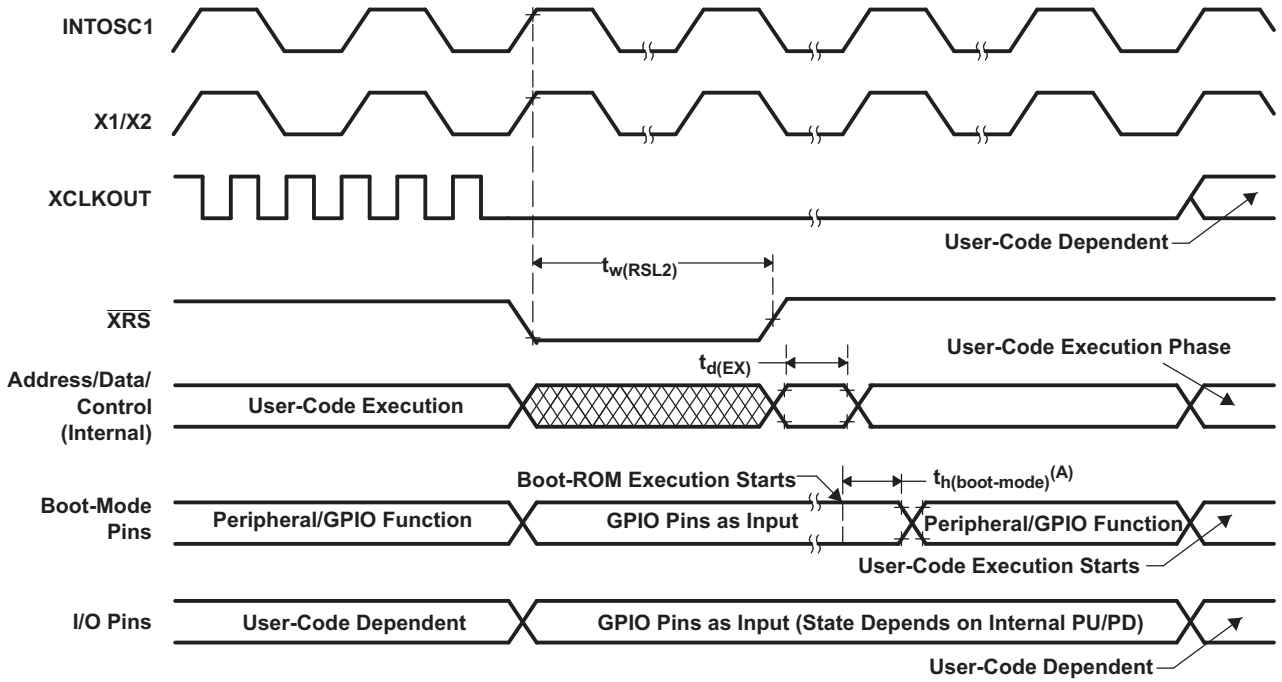
		MIN	MAX	UNIT
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins	$1000t_{c(SCO)}$		cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low on warm reset	$32t_{c(OSCCLK)}$		cycles

Table 4-5. Reset ($\overline{XRS}$) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{XRS}$ driven by device			600		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog			$512t_{c(OSCCLK)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high			$32t_{c(OSCCLK)}$		cycles
$t_{INTOSCST}$	Start-up time, internal zero-pin oscillator			3		µs
t_{OSCST} (1)	On-chip crystal-oscillator start-up time		1	10		ms

(1) Dependent on crystal/resonator and board design.



A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 4-8. Warm Reset

Figure 4-9 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and SYSCLKOUT = OSCCLK x 2. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, SYSCLKOUT = OSCCLK/2. After the PLL lock-up is complete, SYSCLKOUT reflects the new operating frequency, OSCCLK x 4.

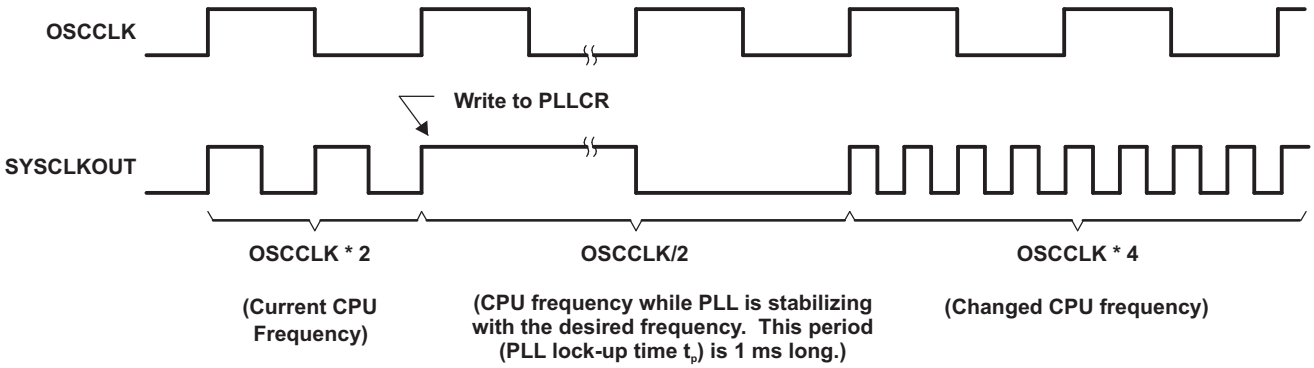


Figure 4-9. Example of Effect of Writing Into PLLCR Register

4.13 Clock Specifications

4.13.1 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the 2803x MCUs. Table 4-6 lists the cycle times of various clocks.

Table 4-6. 2803x Clock Table and Nomenclature (60-MHz Devices)

		MIN	NOM	MAX	UNIT
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	16.67		500	ns
	Frequency	2		60	MHz
LSPCLK(1)	$t_{c(LCO)}$, Cycle time	16.67	66.67(2)		ns
	Frequency		15(2)	60	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	16.67			ns
	Frequency			60	MHz

(1) Lower LSPCLK will reduce device power consumption.
(2) This is the default reset value if SYSCLKOUT = 60 MHz.

Table 4-7. Device Clocking Requirements/Characteristics

		MIN	NOM	MAX	UNIT
On-chip oscillator (X1/X2 pins) (Crystal/Resonator)	$t_{c(OSC)}$, Cycle time	50		200	ns
	Frequency	5		20	MHz
External oscillator/clock source (XCLKIN pin) — PLL Enabled	$t_{c(CI)}$, Cycle time (C8)	33.3		200	ns
	Frequency	5		30	MHz
External oscillator/clock source (XCLKIN pin) — PLL Disabled	$t_{c(CI)}$, Cycle time (C8)	33.33		250	ns
	Frequency	4		30	MHz
Limp mode SYSCLKOUT (with /2 enabled)	Frequency range		1 to 5		MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time (C1)	66.67		2000	ns
	Frequency	0.5		15	MHz
PLL lock time(1)	t_p			1	ms

(1) The PLLLOCKPRD register must be updated based on the number of OSCCLK cycles. If the zero-pin internal oscillators (10 MHz) are used as the clock source, then the PLLLOCKPRD register must be written with a value of 10,000 (minimum).

Table 4-8. Internal Zero-Pin Oscillator (INTOSC1/INTOSC2) Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
Internal zero-pin oscillator 1 (INTOSC1) at 30°C(1)(2)	Frequency		10.000		MHz
Internal zero-pin oscillator 2 (INTOSC2) at 30°C(1)(2)	Frequency		10.000		MHz
Step size (coarse trim)			55		kHz
Step size (fine trim)			14		kHz
Temperature drift(3)			3.03	4.85	kHz/°C
Voltage (V_{DD}) drift(3)			175		Hz/mV

(1) Oscillator frequency will vary over temperature, see Figure 4-10. To compensate for oscillator temperature drift, see the *Oscillator Compensation Guide* and the controlSUITE™ example, Example_2803xOscComp.c.
(2) Frequency range ensured only when VREG is enabled, $\overline{\text{VREGENZ}}$ = V_{SS}.
(3) Output frequency of the internal oscillators follows the direction of both the temperature gradient and voltage (V_{DD}) gradient. For example:
- Increase in temperature will cause the output frequency to increase per the temperature coefficient.
- Decrease in voltage (V_{DD}) will cause the output frequency to decrease per the voltage coefficient.

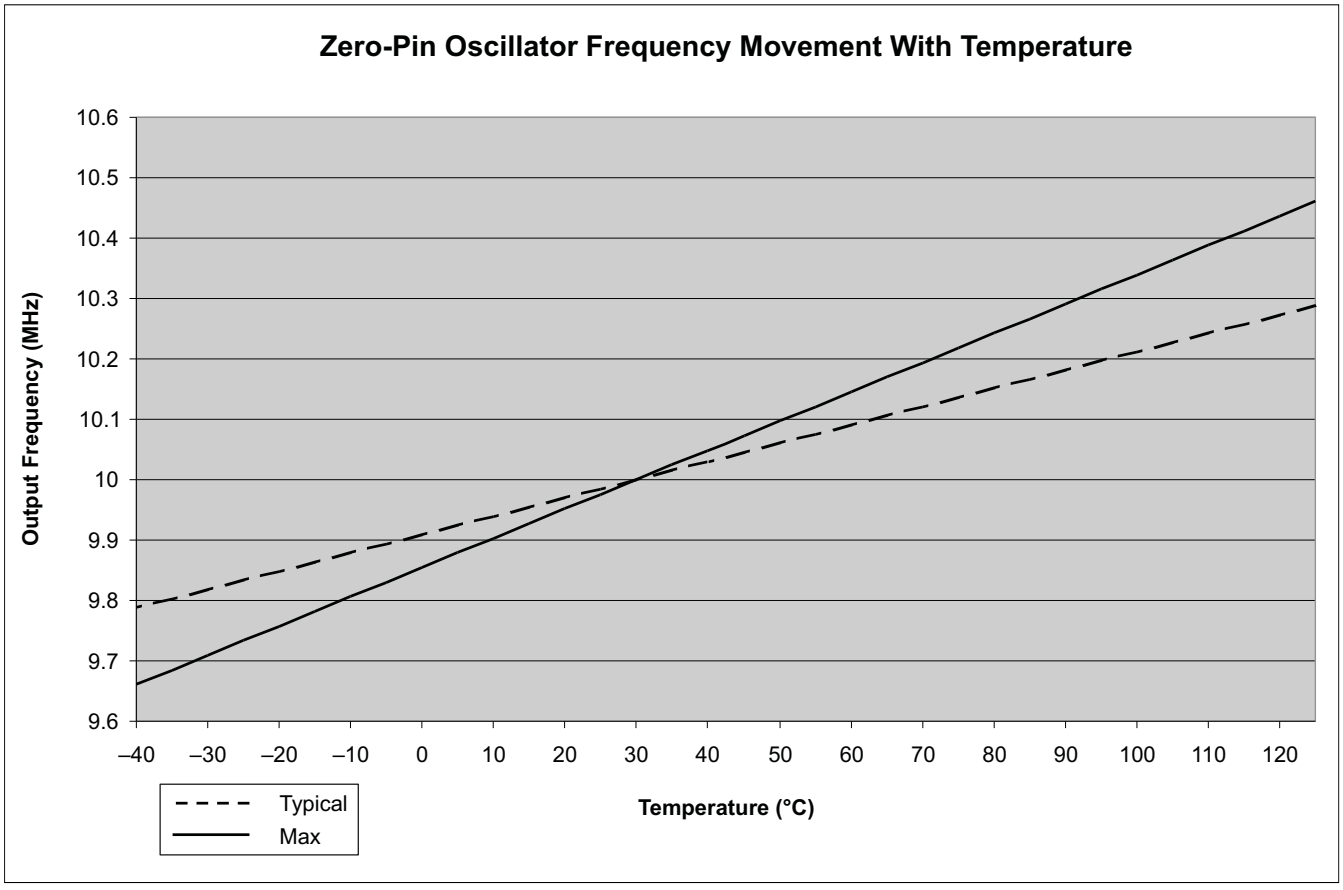


Figure 4-10. Zero-Pin Oscillator Frequency Movement With Temperature

4.13.2 Clock Requirements and Characteristics

Table 4-9. XCLKIN Timing Requirements – PLL Enabled

NO.			MIN	MAX	UNIT
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45%	55%	
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45%	55%	

Table 4-10. XCLKIN Timing Requirements – PLL Disabled

NO.				MIN	MAX	UNIT
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 30 MHz		2	
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 30 MHz		2	
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$		45%	55%	
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$		45%	55%	

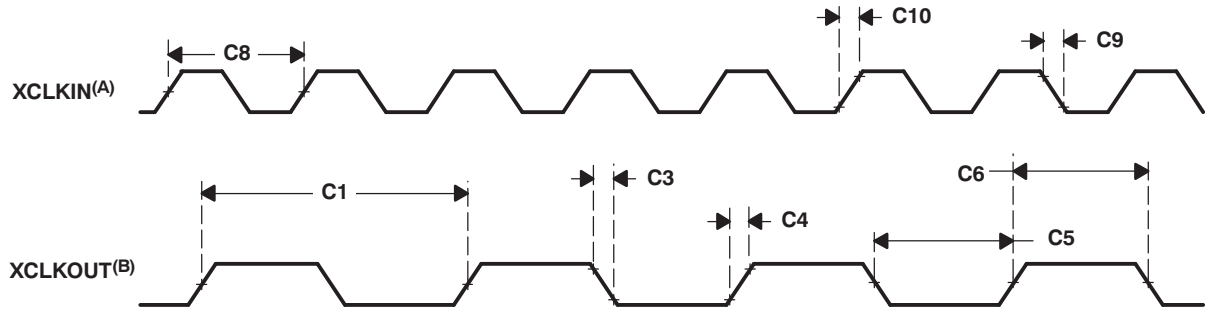
The possible configuration modes are shown in Table 5-15.

Table 4-11. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)(1) (2)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2	H + 2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$



A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.
B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 4-11. Clock Timing

4.14 Flash Timing

Table 4-12. Flash/OTP Endurance(1)

		ERASE/PROGRAM TEMPERATURE	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	–40°C to 125°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	–40°C to 30°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.

Table 4-13. Flash Parameters at 60-MHz SYSCLKOUT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Time(1)	8K Sector			250	2000(2)	ms
	4K Sector			125	2000(2)	ms
	16-Bit Word			50		µs
Erase Time(3)	8K Sector			2	12(2)	s
	4K Sector			2	12(2)	s
I_{DDP}(4)	V_{DD} current consumption during Erase/Program cycle	VREG disabled		80		mA
I_{DDIOP}(4)	V_{DDIO} current consumption during Erase/Program cycle			60		mA
I_{DDIOP}(4)	V_{DDIO} current consumption during Erase/Program cycle	VREG enabled		120		mA

(1) Program time is at the maximum device frequency. The programming time indicated in this table is applicable only when all the required code/data is available in the device RAM, ready for programming. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- the code that uses flash API to program the flash
- the Flash API itself
- Flash data to be programmed

(2) Maximum flash parameter mentioned are for the first 100 program and erase cycles.

(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

(4) Typical parameters as seen at room temperature including function call overhead, with all peripherals off. It is important to maintain a stable power supply during the entire flash programming process. It is conceivable that device current consumption during flash programming could be higher than normal operating conditions. The power supply used should ensure V_{MIN} on the supply rails at all times, as specified in the *Recommended Operating Conditions* of the data sheet. Any brown-out or interruption to power during erasing/programming could potentially corrupt the password locations and lock the device permanently. Powering a target board (during flash programming) through the USB port is not recommended, as the port may be unable to respond to the power demands placed during the programming process.

Table 4-14. Flash/OTP Access Timing

PARAMETER		MIN	MAX	UNIT
$t_{a(fp)}$	Paged Flash access time	40		ns
$t_{a(fr)}$	Random Flash access time	40		ns
$t_{a(OTP)}$	OTP access time	60		ns

Table 4-15. Flash Data Retention Duration

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{retention}$	Data retention duration	T_J = 55°C	15		years

Table 4-16. Minimum Required Flash/OTP Wait States at Different Frequencies

SYSCLKOUT (MHz)	SYSCLKOUT (ns)	PAGE WAIT STATE(1)	RANDOM WAIT STATE(1)	OTP WAIT STATE
60	16.67	2	2	3
55	18.18	2	2	3
50	20	1	1	2
45	22.22	1	1	2
40	25	1	1	2
35	28.57	1	1	2
30	33.33	1	1	1
25	40	0	1	1

(1) Random wait state must be ≥ 1.

The equations to compute the Flash page wait state and random wait state in Table 4-16 are as follows:

$$\text{Flash Page Wait State} = \left[\left(\frac{t_{a(f\bullet p)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer}$$

$$\text{Flash Random Wait State} = \left[\left(\frac{t_{a(f\cdot r)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer, or 1, whichever is larger}$$

The equation to compute the OTP wait state in Table 4-16 is as follows:

$$\text{OTP Wait State} = \left[\left(\frac{t_{a(OTP)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer, or 1, whichever is larger}$$

5 Detailed Description

5.1 Overview

5.1.1 CPU

The 28035 (C28x) is a member of the TMS320C2000™ microcontroller (MCU) platform. The C28x-based controllers have the same 32-bit fixed-point architecture as existing C28x MCUs. It is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enabling development of math algorithms using C/C++. The device is as efficient at MCU math tasks as it is at system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 × 32-bit MAC 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables it to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

5.1.2 Control Law Accelerator (CLA)

The C28x control law accelerator is a single-precision (32-bit) floating-point unit that extends the capabilities of the C28x CPU by adding parallel processing. The CLA is an independent processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks, or routines, can be specified. Each task is started by software or a peripheral such as the ADC, an ePWM, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers and the ePWM+HRPWM registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

5.1.3 Memory Bus (Harvard Bus Architecture)

As with many MCU-type devices, multiple buses are used to move data between the memories and peripherals and the CPU. The memory bus architecture contains a program read bus, data read bus, and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write buses consist of 32 address lines and 32 data lines each. The 32-bit-wide data buses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

5.1.4 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) MCU family of devices, the devices adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various buses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Three versions of the peripheral bus are supported. One version supports only 16-bit accesses (called peripheral frame 2). Another version supports both 16- and 32-bit accesses (called peripheral frame 1). The third version supports CLA access and both 16- and 32-bit accesses (called peripheral frame 3).

5.1.5 Real-Time JTAG and Analysis

The devices implement the standard IEEE 1149.1 JTAG (1) interface for in-circuit based debug. Additionally, the devices support real-time mode of operation allowing modification of the contents of memory, peripheral, and register locations while the processor is running and executing code and servicing interrupts. The user can also single step through non-time-critical code while enabling time-critical interrupts to be serviced without interference. The device implements the real-time mode in hardware within the CPU. This is a feature unique to the 28x family of devices, requiring no software monitor. Additionally, special analysis hardware is provided that allows setting of hardware breakpoint or data/address watch-points and generating various user-selectable break events when a match occurs.

5.1.6 Flash

The F28035 device contains 64K × 16 of embedded flash memory, segregated into eight 8K × 16 sectors. This device also contains a single 1K × 16 of OTP memory at address range 0x3D 7800 to 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Addresses 0x3F 7FF0 to 0x3F 7FF5 are reserved for data variables and should not contain program code.

NOTE

The Flash and OTP wait states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait state, and OTP wait-state registers, see the *TMS320F2803x Piccolo System Control and Interrupts Reference Guide*.

5.1.7 M0, M1 SARAMs

This device contains two blocks of single access memory, each 1K × 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

5.1.8 L0 SARAM, and L1, L2, and L3 DPSARAMs

The device contains up to 8K × 16 of single-access RAM. To ascertain the exact size for a given device, see the device-specific memory map figures in Section 5.2. This block is mapped to both program and data space. Block L0 is 2K in size and is dual mapped to both program and data space. Blocks L1 and L2 are both 1K in size and are shared with the CLA which can ultilize these blocks for its data space. Block L3 is 4K (2K on the 28031 device) in size and is shared with the CLA which can ultilize this block for its program space. DPSARAM refers to the dual-port configuration of these blocks.

5.1.9 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms.

Table 5-1. Boot Mode Selection

MODE	GPIO37/TDO	GPIO34/COMP2OUT/ COMP3OUT	$\overline{\text{TRST}}$	MODE
3	1	1	0	GetMode
2	1	0	0	Wait (see Section 5.1.10 for description)
1	0	1	0	SCI
0	0	0	0	Parallel IO
EMU	x	x	1	Emulation Boot

5.1.9.1 Emulation Boot

When the emulator is connected, the GPIO37/TDO pin cannot be used for boot mode selection. In this case, the boot ROM detects that an emulator is connected and uses the contents of two reserved SARAM locations in the PIE vector table to determine the boot mode. If the content of either location is invalid, then the *Wait* boot option is used. All boot mode options can be accessed in emulation boot.

5.1.9.2 GetMode

The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. If the content of either OTP location is invalid, then boot to flash is used. One of the following loaders can be specified: SCI, SPI, I2C, CAN, or OTP.

5.1.9.3 Peripheral Pins Used by the Bootloader

Table 5-2 shows which GPIO pins are used by each peripheral bootloader. Refer to the GPIO mux table to see if these conflict with any of the peripherals you would like to use in your application.

Table 5-2. Peripheral Bootload Pins

BOOTLOADER	PERIPHERAL LOADER PINS
SCI	SCIRXDA (GPIO28) SCITXDA (GPIO29)
Parallel Boot	Data (GPIO31,30,5:0) 28x Control (AIO6) Host Control (AIO12)
SPI	SPISIMOA (GPIO16) SPISOMIA (GPIO17) SPICLKA (GPIO18) SPISTEA (GPIO19)
I2C	SDAA (GPIO32) SCLA (GPIO33)
CAN	CANRXA (GPIO30) CANTXA (GPIO31)

5.1.10 Security

The devices support high levels of security to protect the user firmware from being reverse engineered. The security features a 128-bit password (hardcoded for 16 wait states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents through the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit KEY value that matches the value stored in the password locations within the Flash.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to CSM secure memory while the emulator is connected will trip the ECSL and break the emulation connection. To allow emulation of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct value into the lower 64 bits of the KEY register, which matches the value stored in the lower 64 bits of the password locations within the flash. Dummy reads of all 128 bits of the password in the flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match.

When initially debugging a device with the password locations in flash programmed (that is, secured), the CPU will start running and may execute an instruction that performs an access to a protected ECSL area. If this happens, the ECSL will trip and cause the emulator connection to be cut.

The solution is to use the *Wait* boot option. This will sit in a loop around a software breakpoint to allow an emulator to be connected without tripping security. Piccolo devices do not support a hardware wait-in-reset mode.

NOTE

- When the code-security passwords are programmed, all addresses from 0x3F7F80 to 0x3F7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F7F80 to 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 to 0x3F7FF5 are reserved for data and should not contain program code.

The 128-bit password (at 0x3F 7FF8 to 0x3F 7FFF) must not be programmed to zeros. Doing so would permanently lock the device.

Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

5.1.11 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F2803x, 56 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

5.1.12 External Interrupts (XINT1–XINT3)

The devices support three masked external interrupts (XINT1–XINT3). Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled/disabled. These interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. There are no dedicated pins for the external interrupts. XINT1, XINT2, and XINT3 interrupts can accept inputs from GPIO0–GPIO31 pins.

5.1.13 Internal Zero Pin Oscillators, Oscillator, and PLL

The device can be clocked by either of the two internal zero-pin oscillators, an external oscillator, or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 12 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to Section 4, Electrical Specifications, for timing details. The PLL block can be set in bypass mode.

5.1.14 Watchdog

Each device contains two watchdogs: CPU-Watchdog that monitors the core and NMI-Watchdog that is a missing clock-detect circuit. The user software must regularly reset the CPU-watchdog counter within a certain time frame; otherwise, the CPU-watchdog generates a reset to the processor. The CPU-watchdog can be disabled if necessary. The NMI-Watchdog engages only in case of a clock failure and can either generate an interrupt or a device reset.

5.1.15 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I2C) can be scaled relative to the CPU clock.

5.1.16 Low-power Modes

The devices are full static CMOS devices. Three low-power modes are provided:

- IDLE: Place CPU in low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that must function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
- STANDBY: Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
- HALT: This mode basically shuts down the device and places it in the lowest possible power consumption mode. If the internal zero-pin oscillators are used as the clock source, the HALT mode turns them off, by default. To keep these oscillators from shutting down, the INTOSCnHALTI bits in CLKCTL register may be used. The zero-pin oscillators may thus be used to clock the CPU-watchdog in this mode. If the on-chip crystal oscillator is used as the clock source, it is shut down in this mode. A reset or an external signal (through a GPIO pin) or the CPU-watchdog can wake the device from this mode.

The CPU clock (OSCCLK) and WDCLK should be from the same clock source before attempting to put the device into HALT or STANDBY.

5.1.17 Peripheral Frames 0, 1, 2, 3 (PFn)

The device segregates peripherals into four sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Waitstate Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result Registers
	CLA	Control Law Accelrator Registers and Message RAMs
PF1:	GPIO:	GPIO MUX Configuration and Control Registers
	eCAN:	Enhanced Control Area Network Configuration and Control Registers
	LIN:	Local Interconnect Network Configuration and Control Registers
	eCAP:	Enhanced Capture Module and Registers
	eQEP:	Enhanced Quadrature Encoder Pulse Module and Registers
	HRCAP:	High-Resolution Capture Module and Registers
PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Configuration Registers
	I2C:	Inter-Integrated Circuit Module and Registers
	XINT:	External Interrupt Registers
PF3:	ePWM:	Enhanced Pulse Width Modulator Module and Registers
	HRPWM:	High-Resolution Pulse-Width Modulator Registers
	Comparators:	Comparator Modules

5.1.18 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

5.1.19 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and can be connected to INT13 of the CPU. CPU-Timer 2 is reserved for DSP/BIOS. It is connected to INT14 of the CPU. If DSP/BIOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLKOUT (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- External clock source

5.1.20 Control Peripherals

The devices support the following peripherals that are used for embedded control and communication:

ePWM:	The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support the HRPWM high resolution duty and period features. The type 1 module found on 2803x devices also supports increased dead-band resolution, enhanced SOC and interrupt generation, and advanced triggering including trip functions based on comparator outputs.
eCAP:	The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes. This peripheral can also be configured to generate an auxiliary PWM signal.
eQEP:	The enhanced QEP peripheral uses a 32-bit position counter, supports low-speed measurement using capture unit and high-speed measurement using a 32-bit unit timer. This peripheral has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals.
ADC:	The ADC block is a 12-bit converter. It has up to 16 single-ended channels pinned out, depending on the device. It contains two sample-and-hold units for simultaneous sampling.
Comparator:	Each comparator block consists of one analog comparator along with an internal 10-bit reference for supplying one input of the comparator.
HRCAP:	The high-resolution capture peripheral operates in normal capture mode through a 16-bit counter clocked off of the HCCAPCLK or in high-resolution capture mode by utilizing built-in calibration logic in conjunction with a TI-supplied calibration library.

5.1.21 Serial Port Peripherals

The devices support the following serial communication peripherals:

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI. The SPI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. The SCI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

I2C: The inter-integrated circuit (I2C) module provides an interface between an MCU and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus®) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the MCU through the I2C module. The I2C contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

eCAN: This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is compliant with ISO11898-1 (CAN 2.0B).

LIN: LIN 1.3 or 2.0 compatible peripheral. Can also be configured as additional SCI port

5.2 Memory Maps

In Figure 5-1, the following apply:

- Memory blocks are not to scale.
- Peripheral Frame 0, Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.
- *Protected* means the order of Write-followed-by-Read operations is preserved rather than the pipeline order.
- Certain memory ranges are EALLOW protected against spurious writes after configuration.
- Locations 0x3D7C80 to 0x3D7CC0 contain the internal oscillator and ADC calibration routines. These locations are not programmable by the user.

	Data Space	Prog Space
0x00 0000	*M0 Vector RAM (Enabled if VMAP = 0)*	
0x00 0040	M0 SARAM (1K × 16, 0-Wait)	
0x00 0400	M1 SARAM (1K × 16, 0-Wait)	
0x00 0800	Peripheral Frame 0	Reserved
0x00 0D00	PIE Vector - RAM (256 × 16) (Enabled if VMAP = 1, ENPIE = 1)	
0x00 0E00	Peripheral Frame 0	
0x00 1400	CLA Registers	
0x00 1480	CLA-to-CPU Message RAM	
0x00 1500	CPU-to-CLA Message RAM	
0x00 1580	Peripheral Frame 0	
0x00 2000	Reserved	
0x00 6000	Peripheral Frame 1 (1K × 16, Protected)	Reserved
0x00 6400	Peripheral Frame 3 (1.5K × 16, Protected)	
0x00 6A00	Peripheral Frame 1 (1.5K × 16, Protected)	
0x00 7000	Peripheral Frame 2 (4K × 16, Protected)	
0x00 8000	L0 SARAM (2K × 16) (0-Wait, Secure Zone + ECSL, Dual-Mapped)	
0x00 8800	L1 DPSARAM (1K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 0)	
0x00 8C00	L2 DPSARAM (1K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 1)	
0x00 9000	L3 DPSARAM (4K × 16) (0-Wait, Secure Zone + ECSL, CLA Prog RAM)	
0x00 A000	Reserved	
0x3D 7800	User OTP (1K × 16, Secure Zone + ECSL)	
0x3D 7C00	Reserved	
0x3D 7C80	Calibration Data	
0x3D 7CC0	Get_mode function	
0x3D 7CE0	Reserved	
0x3D 7E80	PARTID	
	Calibration Data	
0x3D 7EB0	Reserved	
0x3E 8000	FLASH (64K × 16, 8 Sectors, Secure Zone + ECSL)	
0x3F 7FF8	128-Bit Password	
0x3F 8000	L0 SARAM (2K × 16) (0-Wait, Secure Zone + ECSL, Dual-Mapped)	
0x3F 8800	Reserved	
0x3F E000	Boot ROM (8K × 16, 0-Wait)	
0x3F FFC0	*Vector (32 Vectors, Enabled if VMAP = 1)*	

A. CLA-specific registers and RAM apply to the 28035 device only.
B. Memory locations 0x3D7E80-0x3D7EAF are reserved in TMX silicon.

Figure 5-1. 28035 Memory Map

Table 5-3. Addresses of Flash Sectors in 28035

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 to 0x3E 9FFF	Sector H (8K × 16)
0x3E A000 to 0x3E BFFF	Sector G (8K × 16)
0x3E C000 to 0x3E DFFF	Sector F (8K × 16)
0x3E E000 to 0x3E FFFF	Sector E (8K × 16)
0x3F 0000 to 0x3F 1FFF	Sector D (8K × 16)
0x3F 2000 to 0x3F 3FFF	Sector C (8K × 16)
0x3F 4000 to 0x3F 5FFF	Sector B (8K × 16)
0x3F 6000 to 0x3F 7F7F	Sector A (8K × 16)
0x3F 7F80 to 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 to 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 to 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

NOTE

- When the code-security passwords are programmed, all addresses from 0x3F 7F80 to 0x3F 7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F 7F80 to 0x3F 7FEF may be used for code or data. Addresses 0x3F 7FF0 to 0x3F 7FF5 are reserved for data and should not contain program code.

Table 5-4 shows how to handle these memory locations.

Table 5-4. Impact of Using the Code Security Module

ADDRESS	FLASH	
	CODE SECURITY ENABLED	CODE SECURITY DISABLED
0x3F 7F80 to 0x3F 7FEF	Fill with 0x0000	Application code and data
0x3F 7FF0 to 0x3F 7FF5		Reserved for data only

Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode makes sure that all accesses to these blocks happen as written. Because of the pipeline, a write immediately followed by a read to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The CPU supports a block protection mode where a region of memory can be protected so that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it protects the selected zones.

The wait states for the various spaces in the memory map area are listed in Table 5-5.

Table 5-5. Wait States

AREA	WAIT STATES (CPU)	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Cycles can be extended by peripheral generated ready. Back-to-back write operations to Peripheral Frame 1 registers will incur a 1-cycle stall (1-cycle delay).

Table 5-5. Wait States (continued)

AREA	WAIT STATES (CPU)	COMMENTS
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed. Cycles cannot be extended by the peripheral.
Peripheral Frame 3	0-wait (writes) 2-wait (reads)	Assumes no conflict between CPU and CLA. Cycles can be extended by peripheral-generated ready.
L0 SARAM	0-wait data and program	Assumes no CPU conflicts
L1 SARAM	0-wait data and program	Assumes no CPU conflicts
L2 SARAM	0-wait data and program	Assumes no CPU conflicts
L3 SARAM	0-wait data and program	Assumes no CPU conflicts
OTP	Programmable 1-wait minimum	Programmed through the Flash registers. 1-wait is minimum number of wait states allowed.
FLASH	Programmable 0-wait Paged min 1-wait Random min Random ≥ Paged	Programmed through the Flash registers.
FLASH Password	16-wait fixed	Wait states of password locations are fixed.
Boot-ROM	0-wait	

5.3 Register Maps

The devices contain four peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 5-6.

Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 5-7.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 5-8.

Peripheral Frame 3: These are peripherals that are mapped to the 32-bit peripheral bus and are accessible by the CLA. See Table 5-9.

Table 5-6. Peripheral Frame 0 Registers(1)

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED(2)
Device Emulation Registers	0x00 0880 to 0x00 0984	261	Yes
System Power Control Registers	0x00 0985 to 0x00 0987	3	Yes
FLASH Registers(3)	0x00 0A80 to 0x00 0ADF	96	Yes
Code Security Module Registers	0x00 0AE0 to 0x00 0AEF	16	Yes
ADC registers (0 wait read only)	0x00 0B00 to 0x00 0B0F	16	No
CPU–TIMER0/1/2 Registers	0x00 0C00 to 0x00 0C3F	64	No
PIE Registers	0x00 0CE0 to 0x00 0CFF	32	No
PIE Vector Table	0x00 0D00 to 0x00 0DFF	256	No
CLA Registers	0x00 1400 to 0x00 147F	128	Yes
CLA to CPU Message RAM (CPU writes ignored)	0x00 1480 to 0x00 14FF	128	NA
CPU to CLA Message RAM (CLA writes ignored)	0x00 1500 to 0x00 157F	128	NA

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Code Security Module (CSM).

Table 5-7. Peripheral Frame 1 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
eCAN-A registers	0x00 6000 to 0x00 61FF	512	(1)
eCAP1 registers	0x00 6A00 to 0x00 6A1F	32	No
HRCAP1 registers	0x00 6AC0 to 0x00 6ADF	32	(1)
HRCAP2 registers	0x00 6AE0 to 0x00 6AFF	32	(1)
eQEP1 registers	0x00 6B00 to 0x00 6B3F	64	(1)
LIN-A registers	0x00 6C00 to 0x00 6C7F	128	(1)
GPIO registers	0x00 6F80 to 0x00 6FFF	128	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 5-8. Peripheral Frame 2 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
System Control Registers	0x00 7010 to 0x00 702F	32	Yes
SPI-A Registers	0x00 7040 to 0x00 704F	16	No
SCI-A Registers	0x00 7050 to 0x00 705F	16	No
NMI Watchdog Interrupt Registers	0x00 7060 to 0x00 706F	16	Yes
External Interrupt Registers	0x00 7070 to 0x00 707F	16	Yes
ADC Registers	0x00 7100 to 0x00 717F	128	(1)
I2C-A Registers	0x00 7900 to 0x00 793F	64	(1)
SPI-B Registers	0x00 7740 to 0x00 774F	16	No

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 5-9. Peripheral Frame 3 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
Comparator 1 registers	0x00 6400 to 0x00 641F	32	
(1)Comparator 2 registers	0x00 6420 to 0x00 643F	32	(1)
Comparator 3 registers	0x00 6440 to 0x00 645F	32	(1)
ePWM1 + HRPWM1 registers	0x00 6800 to 0x00 683F	64	(1)
ePWM2 + HRPWM2 registers	0x00 6840 to 0x00 687F	64	(1)
ePWM3 + HRPWM3 registers	0x00 6880 to 0x00 68BF	64	(1)
ePWM4 + HRPWM4 registers	0x00 68C0 to 0x00 68FF	64	(1)
ePWM5 + HRPWM5 registers	0x00 6900 to 0x00 693F	64	(1)
ePWM6 + HRPWM6 registers	0x00 6940 to 0x00 697F	64	(1)
ePWM7 + HRPWM7 registers	0x00 6980 to 0x00 69BF	64	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

5.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 5-10 .

Table 5-10. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION			EALLOW PROTECTED
DEVICECNF	0x0880 0x0881	2	Device Configuration Register			Yes
PARTID	0x3D 7E80	1	Part ID Register	TMS320F28035MPNTEP	0x00BF	No
CLASSID	0x0882	1	Class ID Register	TMS320F28035	0x00BF	No
REVID	0x0883	1	Revision ID Register	0x0001 - Silicon Rev. A - TMS		No

5.5 VREG/BOR/POR

Although the core and I/O circuitry operate on two different voltages, these devices have an on-chip voltage regulator (VREG) to generate the V_{DD} voltage from the V_{DDIO} supply. This eliminates the cost and space of a second external regulator on an application board. Additionally, internal power-on reset (POR) and brown-out reset (BOR) circuits monitor both the V_{DD} and V_{DDIO} rails during power-up and run mode.

5.5.1 On-chip Voltage Regulator (VREG)

A linear regulator generates the core voltage (V_{DD}) from the V_{DDIO} supply. Therefore, although capacitors are required on each V_{DD} pin to stabilize the generated voltage, power need not be supplied to these pins to operate the device. Conversely, the VREG can be disabled, should power or redundancy be the primary concern of the application.

5.5.1.1 Using the On-chip VREG

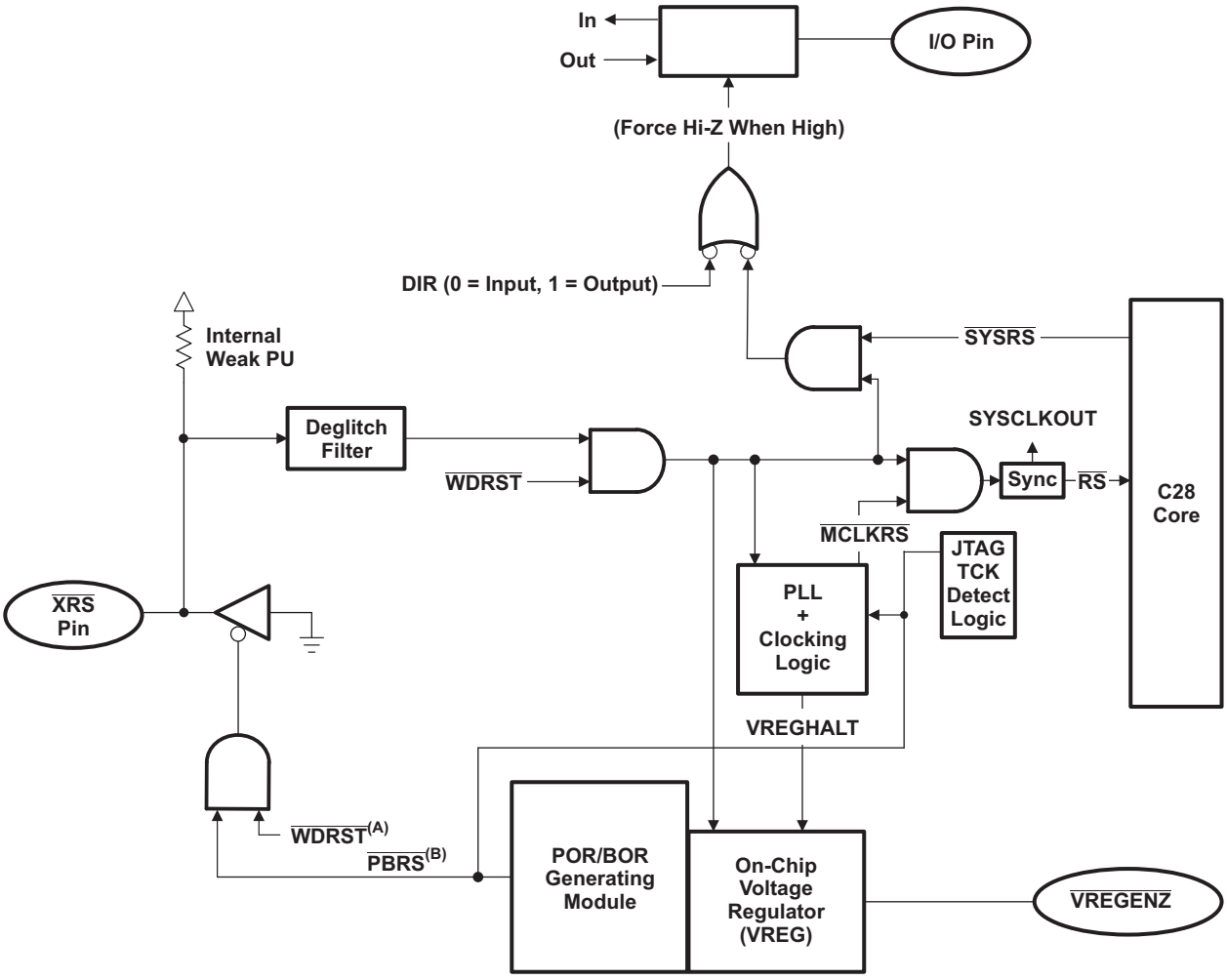
To use the on-chip VREG, the $\overline{\text{VREGENZ}}$ pin should be tied low and the appropriate recommended operating voltage should be supplied to the V_{DDIO} and V_{DDA} pins. In this case, the V_{DD} voltage needed by the core logic will be generated by the VREG. Each V_{DD} pin requires on the order of 1.2 μF (minimum) capacitance for proper regulation of the VREG. These capacitors should be located as close as possible to the V_{DD} pins. Driving an external load with the internal VREG is not supported.

5.5.1.2 Disabling the On-chip VREG

To conserve power, it is also possible to disable the on-chip VREG and supply the core logic voltage to the V_{DD} pins with a more efficient external regulator. To enable this option, the $\overline{\text{VREGENZ}}$ pin must be tied high.

5.5.2 On-chip Power-On Reset (POR) and Brown-Out Reset (BOR) Circuit

Two on-chip supervisory circuits, the power-on reset (POR) and the brown-out reset (BOR) remove the burden of monitoring the V_{DD} and V_{DDIO} supply rails from the application board. The purpose of the POR is to create a clean reset throughout the device during the entire power-up procedure. The trip point is a looser, lower trip point than the BOR, which watches for dips in the V_{DD} or V_{DDIO} rail during device operation. The POR function is present on both V_{DD} and V_{DDIO} rails at all times. After initial device power-up, the BOR function is present on V_{DDIO} at all times, and on V_{DD} when the internal VREG is enabled ($\overline{\text{VREGENZ}}$ pin is tied low). Both functions tie the $\overline{\text{XRS}}$ pin low when one of the voltages is below their respective trip point. V_{DD} BOR and overvoltage trip points are outside of the recommended operating voltages. Proper device operation cannot be ensured. If overvoltage or undervoltage conditions affecting the system is a concern for an application, an external voltage supervisor should be added. Figure 5-2 shows the VREG, POR, and BOR. To disable both the V_{DD} and V_{DDIO} BOR functions, a bit is provided in the BORCFG register. For details, see the *TMS320F2803x Piccolo System Control and Interrupts Reference Guide*.



A. $\overline{\text{WDRST}}$ is the reset signal from the CPU-watchdog.
B. $\overline{\text{PBRS}}$ is the reset signal from the POR/BOR module.

Figure 5-2. VREG + POR + BOR + Reset Signal Connectivity

5.6 System Control

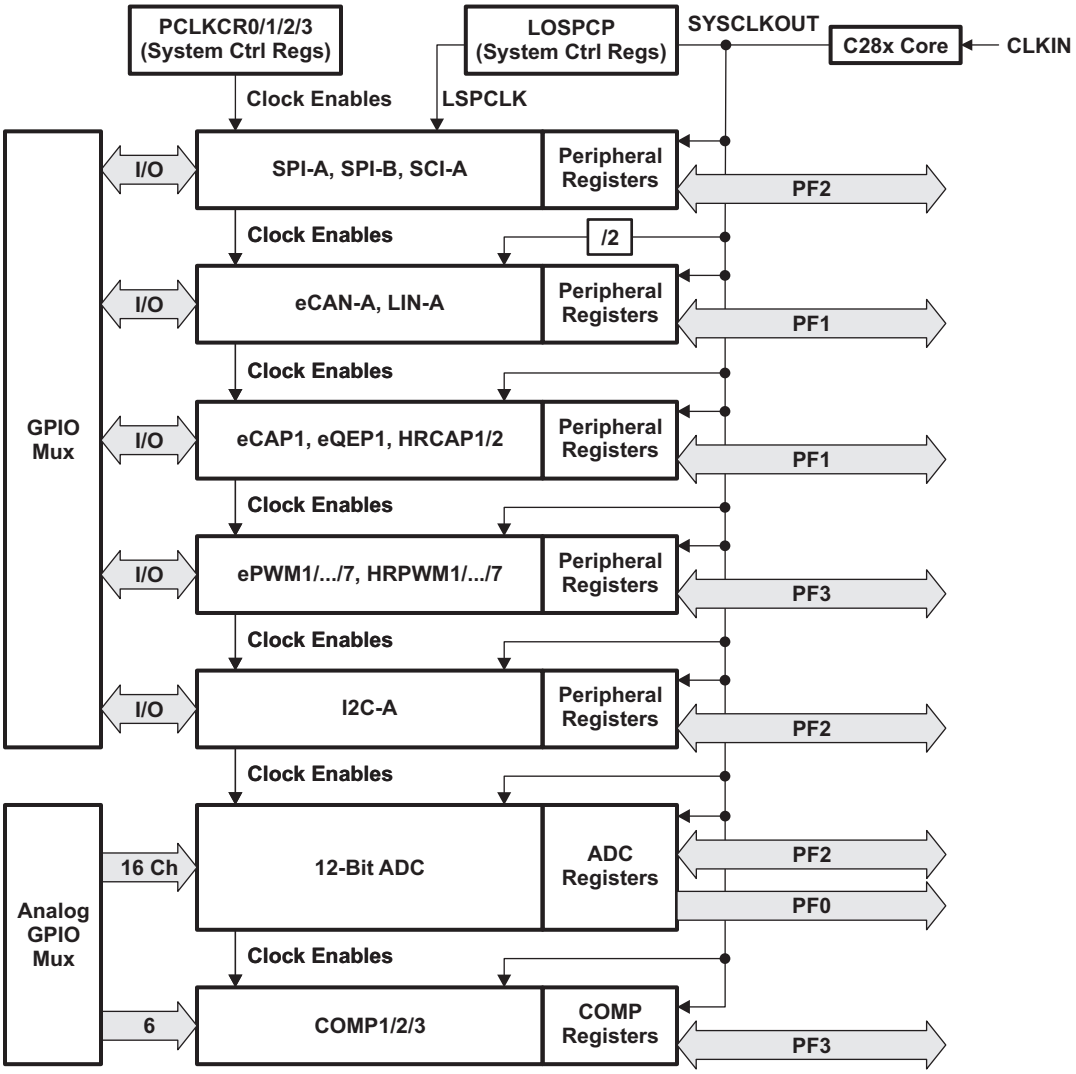
This section describes the oscillator and clocking mechanisms, the watchdog function and the low-power modes.

Table 5-11. PLL, Clocking, Watchdog, and Low-Power Mode Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
BORCFG	0x00 0985	1	BOR Configuration Register
XCLK	0x00 7010	1	XCLKOUT Control
PLLSTS	0x00 7011	1	PLL Status Register
CLKCTL	0x00 7012	1	Clock Control Register
PLLLOCKPRD	0x00 7013	1	PLL Lock Period
INTOSC1TRIM	0x00 7014	1	Internal Oscillator 1 Trim Register
INTOSC2TRIM	0x00 7016	1	Internal Oscillator 2 Trim Register
PCLKCR2	0x00 7019	1	Peripheral Clock Control Register 2
LOSPCP	0x00 701B	1	Low-Speed Peripheral Clock Prescaler Register
PCLKCR0	0x00 701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x00 701D	1	Peripheral Clock Control Register 1
LPMCR0	0x00 701E	1	Low-Power Mode Control Register 0
PCLKCR3	0x00 7020	1	Peripheral Clock Control Register 3
PLLCR	0x00 7021	1	PLL Control Register
SCSR	0x00 7022	1	System Control and Status Register
WDCNTR	0x00 7023	1	Watchdog Counter Register
WDKEY	0x00 7025	1	Watchdog Reset Key Register
WDCR	0x00 7029	1	Watchdog Control Register

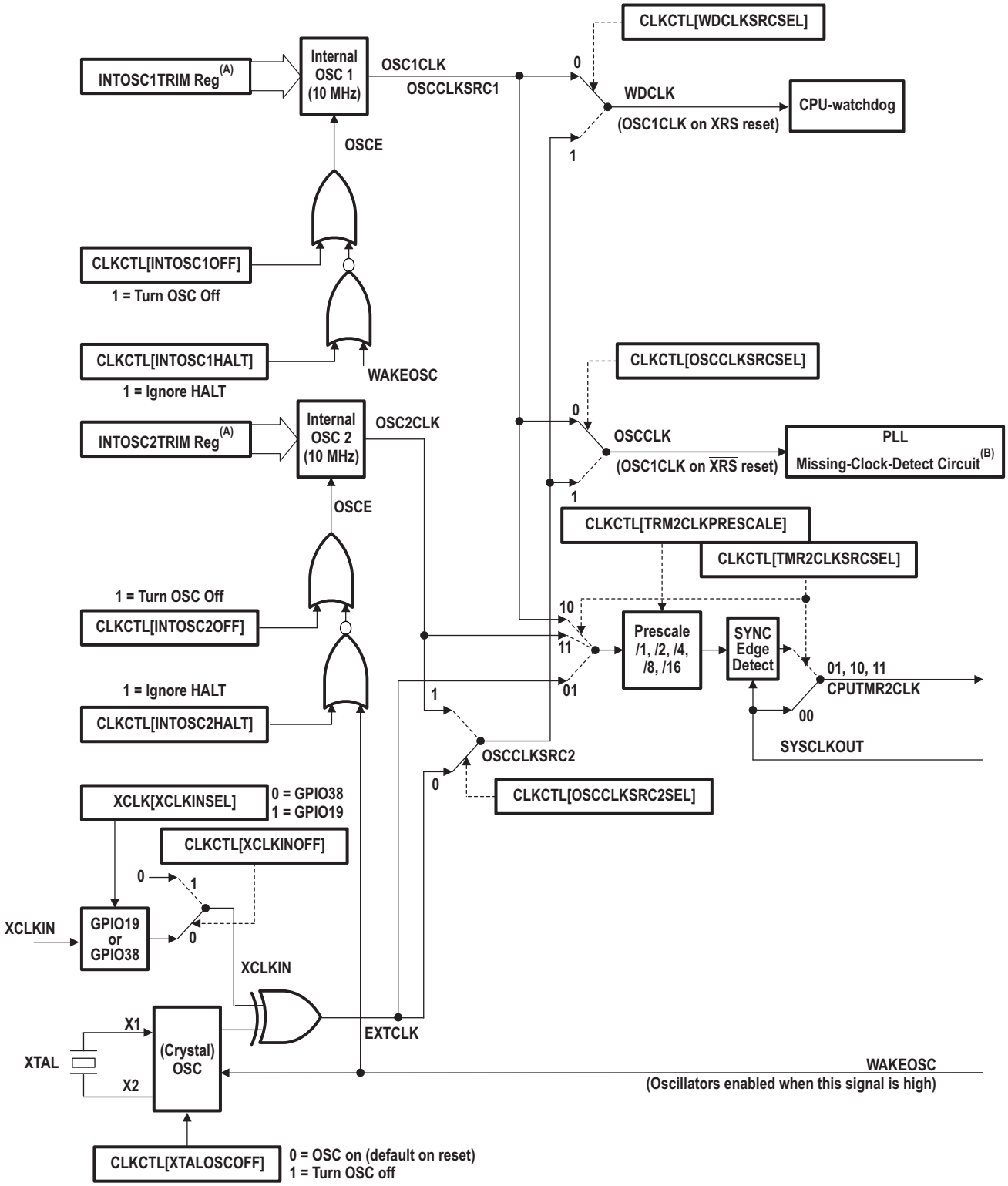
(1) All registers in this table are EALLOW protected.

Figure 5-3 shows the various clock domains that are discussed. Figure 5-4 shows the various clock sources (both internal and external) that can provide a clock for device operation.



A. CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 5-3. Clock and Reset Domains



A. Register loaded from TI OTP-based calibration function.
B. See Section 5.6.4 for details on missing clock detection.

Figure 5-4. Clock Tree

5.6.1 Internal Zero Pin Oscillators

The F2803x devices contain two independent internal zero pin oscillators. By default both oscillators are turned on at power up, and internal oscillator 1 is the default clock source at this time. For power savings, unused oscillators may be powered down by the user. The center frequency of these oscillators is determined by their respective oscillator trim registers, written to in the calibration routine as part of the boot ROM execution. See Section 4, Electrical Specifications, for more information on these oscillators.

5.6.2 Crystal Oscillator Option

The on-chip crystal oscillator X1 and X2 pins are 1.8-V level signals and must never have 3.3-V level signals applied to them. If a system 3.3-V external oscillator is to be used as a clock source, it should be connected to the XCLKIN pin only. The X1 pin is not intended to be used as a single-ended clock input, it should be used with X2 and a crystal.

The typical specifications for the external quartz crystal (fundamental mode, parallel resonant) are listed in Table 5-12. Furthermore, ESR range = 30 to 150 Ω.

Table 5-12. Typical Specifications for External Quartz Crystal(1)

FREQUENCY (MHz)	R_d (Ω)	C_{L1} (pF)	C_{L2} (pF)
5	2200	18	18
10	470	15	15
15	0	15	15
20	0	12	12

(1) C_{shunt} should be less than or equal to 5 pF.

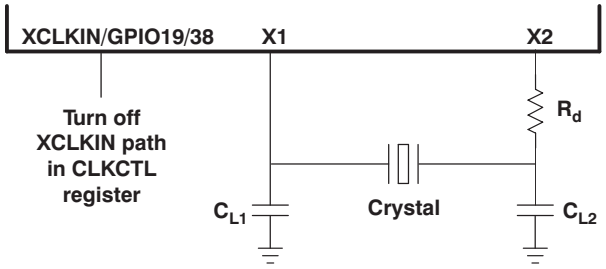


Figure 5-5. Using the On-chip Crystal Oscillator

NOTE

1. C_{L1} and C_{L2} are the total capacitance of the circuit board and components excluding the IC and crystal. The value is usually approximately twice the value of the crystal's load capacitance.
2. The load capacitance of the crystal is described in the crystal specifications of the manufacturers.
3. TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the MCU chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start-up and stability over the entire operating range.

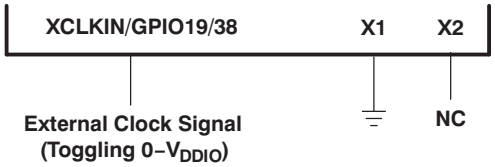


Figure 5-6. Using a 3.3-V External Oscillator

5.6.3 PLL-Based Clock Module

The devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 1 ms. The input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) is at least 50 MHz.

Table 5-13. PLL Settings

PLLCR[DIV] VALUE(1) (2)	SYSCLKOUT (CLKIN)		
	PLLSTS[DIVSEL] = 0 or 1(3)	PLLSTS[DIVSEL] = 2	PLLSTS[DIVSEL] = 3
0000 (PLL bypass)	OSCCLK/4 (Default)(1)	OSCCLK/2	OSCCLK
0001	(OSCCLK * 1)/4	(OSCCLK * 1)/2	(OSCCLK * 1)/1
0010	(OSCCLK * 2)/4	(OSCCLK * 2)/2	(OSCCLK * 2)/1
0011	(OSCCLK * 3)/4	(OSCCLK * 3)/2	(OSCCLK * 3)/1
0100	(OSCCLK * 4)/4	(OSCCLK * 4)/2	(OSCCLK * 4)/1
0101	(OSCCLK * 5)/4	(OSCCLK * 5)/2	(OSCCLK * 5)/1
0110	(OSCCLK * 6)/4	(OSCCLK * 6)/2	(OSCCLK * 6)/1
0111	(OSCCLK * 7)/4	(OSCCLK * 7)/2	(OSCCLK * 7)/1
1000	(OSCCLK * 8)/4	(OSCCLK * 8)/2	(OSCCLK * 8)/1
1001	(OSCCLK * 9)/4	(OSCCLK * 9)/2	(OSCCLK * 9)/1
1010	(OSCCLK * 10)/4	(OSCCLK * 10)/2	(OSCCLK * 10)/1
1011	(OSCCLK * 11)/4	(OSCCLK * 11)/2	(OSCCLK * 11)/1
1100	(OSCCLK * 12)/4	(OSCCLK * 12)/2	(OSCCLK * 12)/1

(1) The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to their default state by the $\overline{\text{XRS}}$ signal or a watchdog reset only. A reset issued by the debugger or the missing clock detect logic has no effect.
(2) This register is EALLOW protected. See the *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* for more information.
(3) By default, PLLSTS[DIVSEL] is configured for /4. (The boot ROM changes this to /1.) PLLSTS[DIVSEL] must be 0 before writing to the PLLCR and should be changed only after PLLSTS[PLLLOCKS] = 1.

Table 5-14. CLKIN Divide Options

PLLSTS [DIVSEL]	CLKIN DIVIDE
0	/4
1	/4
2	/2
3	/1

The PLL-based clock module provides four modes of operation:

- **INTOSC1 (Internal Zero-pin Oscillator 1):** This is the on-chip internal oscillator 1. This can provide the clock for the Watchdog block, core and CPU-Timer 2
- **INTOSC2 (Internal Zero-pin Oscillator 2):** This is the on-chip internal oscillator 2. This can provide the clock for the Watchdog block, core and CPU-Timer 2. Both INTOSC1 and INTOSC2 can be independently chosen for the Watchdog block, core and CPU-Timer 2.
- **Crystal/Resonator Operation:** The on-chip (crystal) oscillator enables the use of an external crystal/resonator attached to the device to provide the time base. The crystal/resonator is connected to the X1/X2 pins. Some devices may not have the X1/X2 pins. See Table 3-1 for details.
- **External Clock Source Operation:** If the on-chip (crystal) oscillator is not used, this mode allows it to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. The XCLKIN is multiplexed with GPIO19 or GPIO38 pin. The XCLKIN input can be selected as GPIO19 or GPIO38 through the XCLKINSEL bit in XCLK register. The CLKCTL[XCLKINOFF] bit disables this clock input (forced low). If the clock source is not used or the respective pins are used as GPIOs, the user should disable at boot time.

Before changing clock sources, ensure that the target clock is present. If a clock is not present, then that clock source must be disabled (using the CLKCTL register) before switching clocks.

Table 5-15. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[DIVSEL]	CLKIN AND SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low-power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{XRS}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL is bypassed but the PLL is not turned off.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Enable	Achieved by writing a nonzero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0, 1 2 3	OSCCLK * n/4 OSCCLK * n/2 OSCCLK * n/1

5.6.4 Loss of Input Clock (NMI Watchdog Function)

The 28035 device may be clocked from either one of the internal zero-pin oscillators (INTOSC1/INTOSC2), the on-chip crystal oscillator, or from an external clock input. Regardless of the clock source, in PLL-enabled and PLL-bypass mode, if the input clock to the PLL vanishes, the PLL will issue a limp-mode clock at its output. This limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1–5 MHz.

When the limp mode is activated, a $\overline{CLOCKFAIL}$ signal is generated that is latched as an NMI interrupt. Depending on how the NMIRESETSEL bit has been configured, a reset to the device can be fired immediately or the NMI watchdog counter can issue a reset when it overflows. In addition to this, the Missing Clock Status (MCLKSTS) bit is set. The NMI interrupt could be used by the application to detect the input clock failure and initiate necessary corrective action such as switching over to an alternative clock source (if available) or initiate a shut-down procedure for the system.

If the software does not respond to the clock-fail condition, the NMI watchdog triggers a reset after a preprogrammed time interval. Figure 5-7 shows the interrupt mechanisms involved.

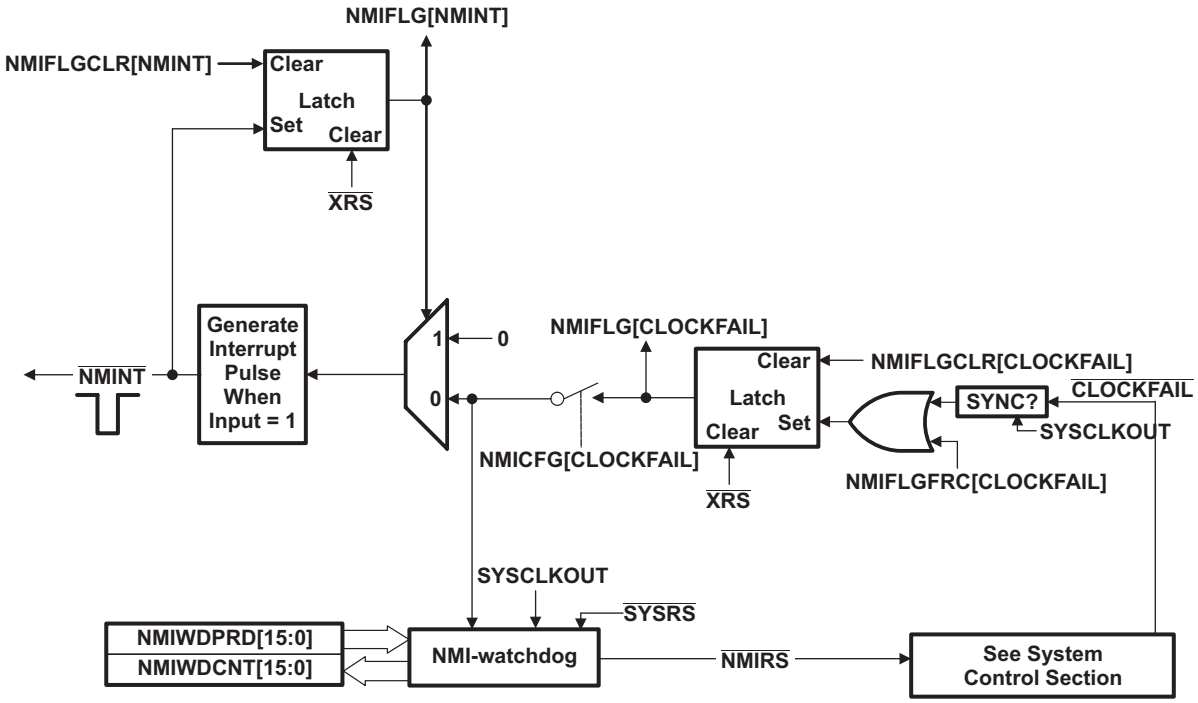


Figure 5-7. NMI-watchdog

5.6.5 CPU-Watchdog Module

The CPU-watchdog module on the 28035 device is similar to the one used on the 281x/280x/283xx devices. This module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user must disable the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register that resets the watchdog counter. Figure 5-8 shows the various functional blocks within the watchdog module.

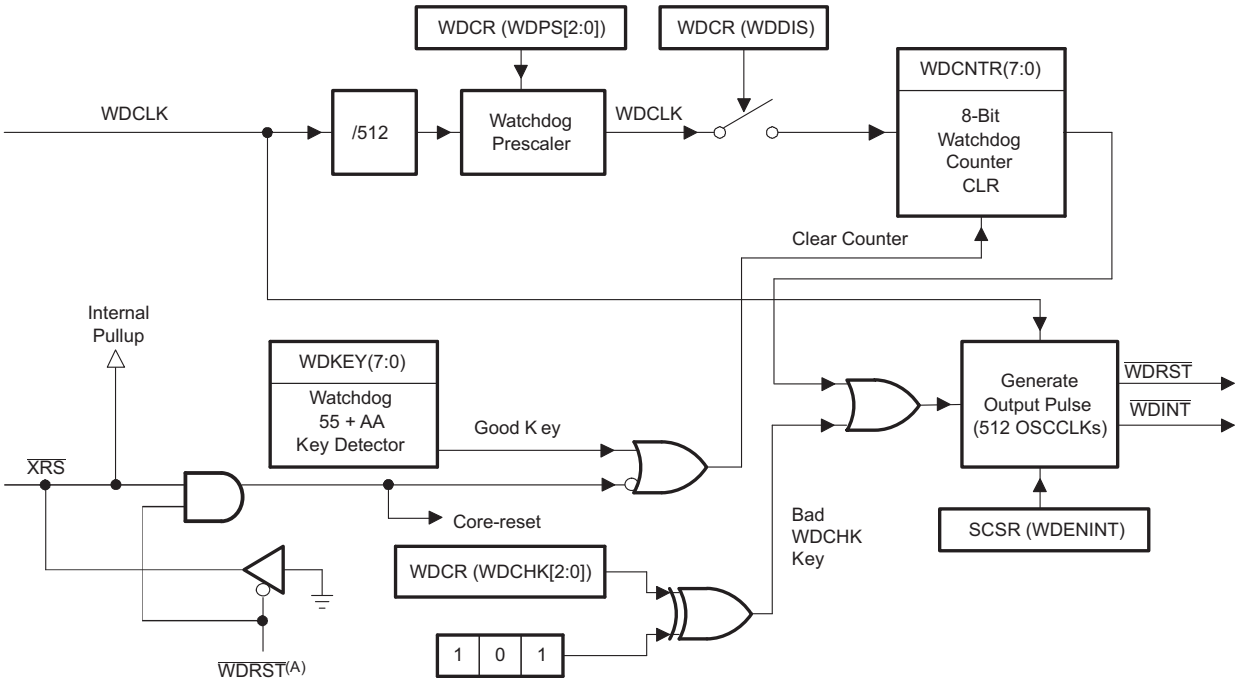
Normally, when the input clocks are present, the CPU-watchdog counter decrements to initiate a CPU-watchdog reset or WDINT interrupt. However, when the external input clock fails, the CPU-watchdog counter stops decrementing (that is, the watchdog counter does not change with the limp-mode clock).

NOTE

The CPU-watchdog is different from the NMI watchdog. It is the legacy watchdog that is present in all 28x devices.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the MCU will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the MCU, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the flash memory.



A. The WDRST signal is driven low for 512 OSCCLK cycles.

Figure 5-8. CPU-watchdog Module

The WDINT signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the CPU-watchdog. This module will run off OSCCLK. The WDINT signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section 5.7, Low-power Modes Block, for more details.

In IDLE mode, the WDINT signal can generate an interrupt to the CPU, through the PIE, to take the CPU out of IDLE mode.

In HALT mode, the CPU-watchdog can be used to wake up the device through a device reset.

5.7 Low-Power Modes Block

Table 5-16 summarizes the various modes.

Table 5-16. Low-power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On	$\overline{XRS}$, CPU-watchdog interrupt, any enabled interrupt
STANDBY	01	On (CPU-watchdog still running)	Off	Off	$\overline{XRS}$, CPU-watchdog interrupt, GPIO Port A signal, debugger(2)
HALT(3)	1X	Off (on-chip crystal oscillator and PLL turned off, zero-pin oscillator and CPU-watchdog state dependent on user code.)	Off	Off	$\overline{XRS}$, GPIO Port A signal, debugger(2), CPU-watchdog

(1) The EXIT column lists which signals or under what conditions the low-power mode is exited. A low signal, on any of the signals, exits the low-power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the low-power mode will not be exited and the device will go back into the indicated low-power mode.
(2) The JTAG port can still function even if the CPU clock (CLKIN) is turned off.
(3) The WDCLK must be active for the device to go into HALT mode.

The various low-power modes operate as follows:

IDLE Mode: This mode is exited by any enabled interrupt that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode: Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode: CPU-watchdog, $\overline{XRS}$, and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* for more details.

5.8 Interrupts

Figure 5-9 shows how the various interrupt sources are multiplexed.

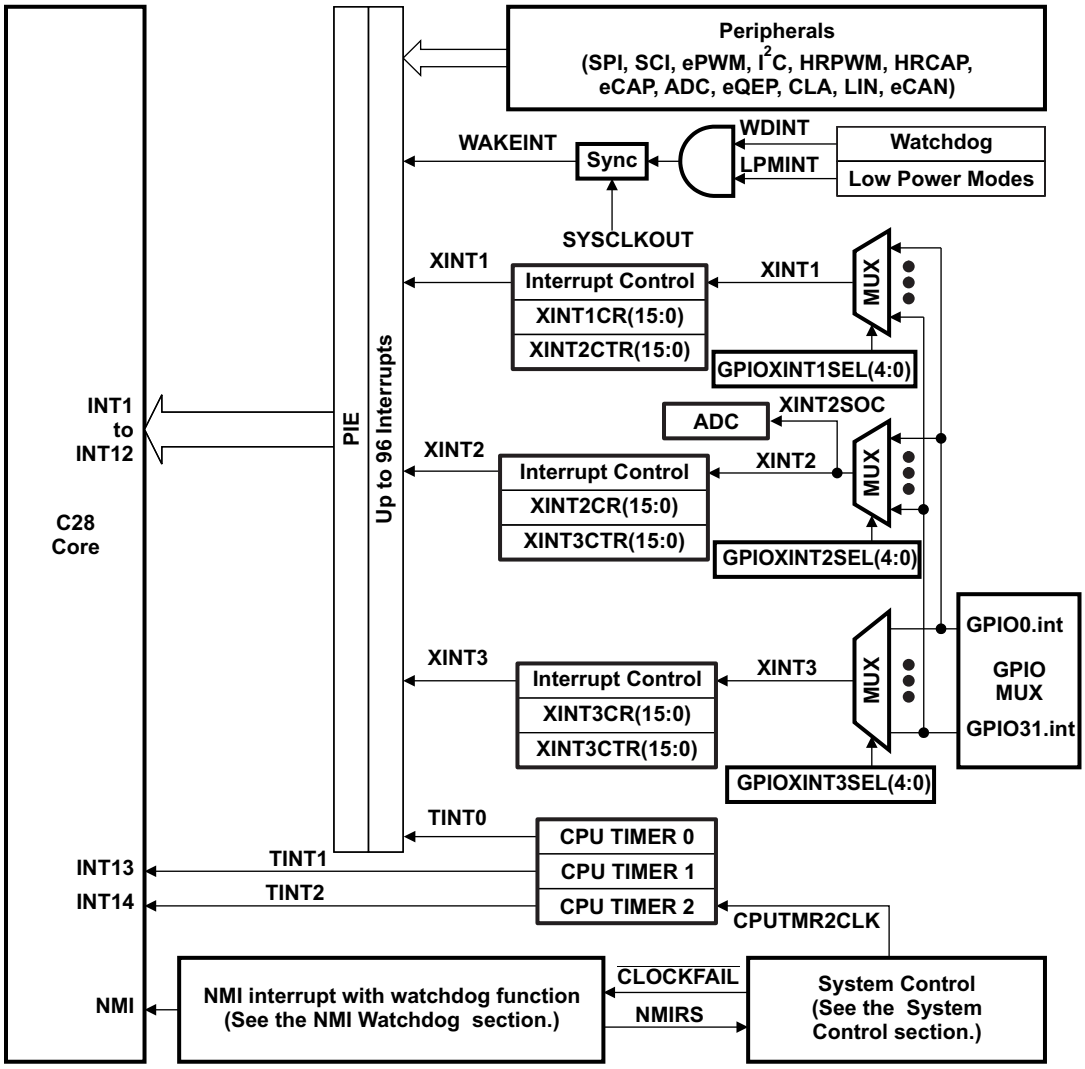


Figure 5-9. External and PIE Interrupt Sources

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. Table 5-17 shows the interrupts used by 2803x devices.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. The TRAP #0 instruction attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, the TRAP #0 instruction should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, the TRAP #1 to TRAP #12 instructions will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: the TRAP #1 instruction fetches the vector from INT1.1, the TRAP #2 instruction fetches the vector from INT2.1, and so forth.

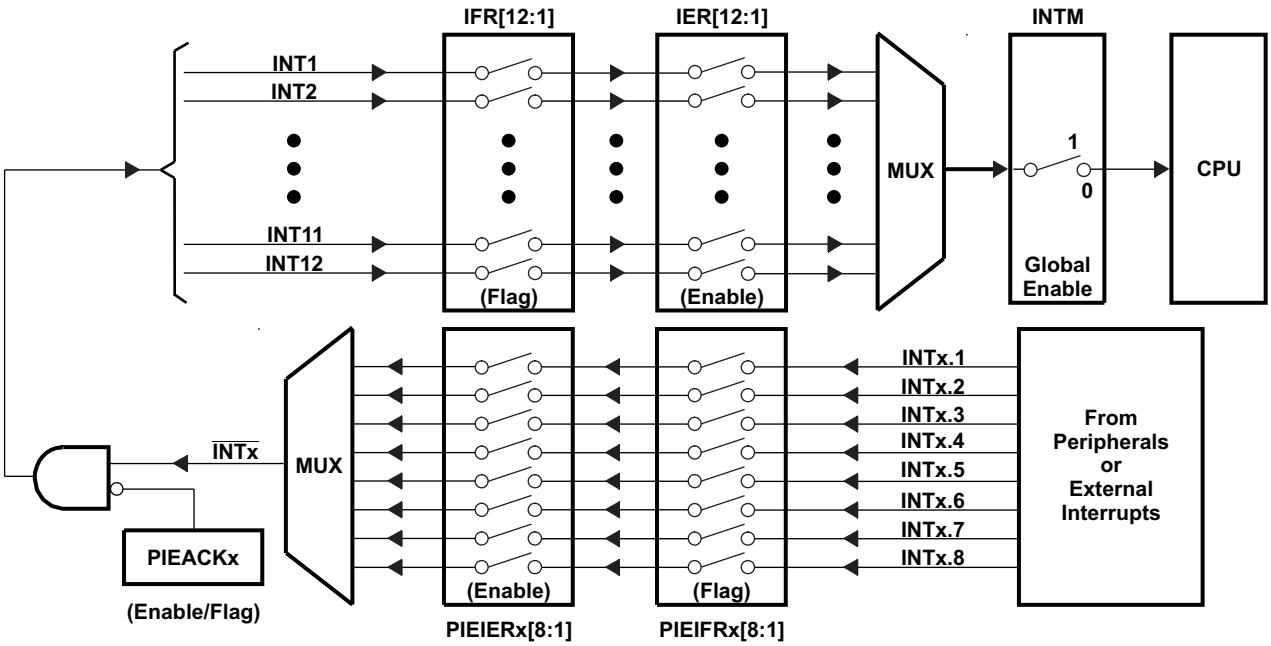


Figure 5-10. Multiplexing of Interrupts Using the PIE Block

Table 5-17. PIE MUXed Peripheral Interrupt Vector Table(1)

	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1.y	WAKEINT	TINT0	ADCINT9	XINT2	XINT1	Reserved	ADCINT2	ADCINT1
	(LPM/WD)	(TIMER 0)	(ADC)	Ext. int. 2	Ext. int. 1	–	(ADC)	(ADC)
	0xD4E	0xD4C	0xD4A	0xD48	0xD46	0xD44	0xD42	0xD40
INT2.y	Reserved	EPWM7_TZINT	EPWM6_TZINT	EPWM5_TZINT	EPWM4_TZINT	EPWM3_TZINT	EPWM2_TZINT	EPWM1_TZINT
	–	(ePWM7)	(ePWM6)	(ePWM5)	(ePWM4)	(ePWM3)	(ePWM2)	(ePWM1)
	0xD5E	0xD5C	0xD5A	0xD58	0xD56	0xD54	0xD52	0xD50
INT3.y	Reserved	EPWM7_INT	EPWM6_INT	EPWM5_INT	EPWM4_INT	EPWM3_INT	EPWM2_INT	EPWM1_INT
	–	(ePWM7)	(ePWM6)	(ePWM5)	(ePWM4)	(ePWM3)	(ePWM2)	(ePWM1)
	0xD6E	0xD6C	0xD6A	0xD68	0xD66	0xD64	0xD62	0xD60
INT4.y	HRCAP2_INT	HRCAP1_INT	Reserved	Reserved	Reserved	Reserved	Reserved	ECAP1_INT
	(HRCAP2)	(HRCAP1)	–	–	–	–	–	(eCAP1)
	0xD7E	0xD7C	0xD7A	0xD78	0xD76	0xD74	0xD72	0xD70
INT5.y	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EQEP1_INT
	–	–	–	–	–	–	–	(eQEP1)
	0xD8E	0xD8C	0xD8A	0xD88	0xD86	0xD84	0xD82	0xD80
INT6.y	Reserved	Reserved	Reserved	Reserved	SPITXINTB	SPIRXINTB	SPITXINTA	SPIRXINTA
	–	–	–	–	(SPI-B)	(SPI-B)	(SPI-A)	(SPI-A)
	0xD9E	0xD9C	0xD9A	0xD98	0xD96	0xD94	0xD92	0xD90
INT7.y	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	–	–	–	–	–	–	–	–
	0xDAE	0xDAC	0xDAA	0xDA8	0xDA6	0xDA4	0xDA2	0xDA0
INT8.y	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	I2CINT2A	I2CINT1A
	–	–	–	–	–	–	(I2C-A)	(I2C-A)
	0xDBE	0xDBC	0xDBA	0xDB8	0xDB6	0xDB4	0xDB2	0xDB0
INT9.y	Reserved	Reserved	ECAN1_INTA	ECAN0_INTA	LIN1_INTA	LIN0_INTA	SCITXINTA	SCIRXINTA
	–	–	(CAN-A)	(CAN-A)	(LIN-A)	(LIN-A)	(SCI-A)	(SCI-A)
	0xDCE	0xDCC	0xDCA	0xDC8	0xDC6	0xDC4	0xDC2	0xDC0
INT10.y	ADCINT8	ADCINT7	ADCINT6	ADCINT5	ADCINT4	ADCINT3	ADCINT2	ADCINT1
	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)	(ADC)
	0xDDE	0xDDC	0xDDA	0xDD8	0xDD6	0xDD4	0xDD2	0xDD0
INT11.y	CLA1_INT8	CLA1_INT7	CLA1_INT6	CLA1_INT5	CLA1_INT4	CLA1_INT3	CLA1_INT2	CLA1_INT1
	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)	(CLA)
	0xDEE	0xDEC	0xDEA	0xDE8	0xDE6	0xDE4	0xDE2	0xDE0
INT12.y	LUF	LVF	Reserved	Reserved	Reserved	Reserved	Reserved	XINT3
	(CLA)	(CLA)	–	–	–	–	–	Ext. Int. 3
	0xDFE	0xDFC	0xDFA	0xDF8	0xDF6	0xDF4	0xDF2	0xDF0

(1) Out of 96 possible interrupts, some interrupts are not used. These interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:
- No peripheral within the group is asserting interrupts.
- No peripheral interrupts are assigned to the group (for example, PIE group 7).

Table 5-18. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA – 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

5.8.1 External Interrupts

Table 5-19. External Interrupt Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x00 7070	1	XINT1 configuration register
XINT2CR	0x00 7071	1	XINT2 configuration register
XINT3CR	0x00 7072	1	XINT3 configuration register
XINT1CTR	0x00 7078	1	XINT1 counter register
XINT2CTR	0x00 7079	1	XINT2 counter register
XINT3CTR	0x00 707A	1	XINT3 counter register

Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the *TMS320F2803x Piccolo System Control and Interrupts Reference Guide*.

5.8.1.1 External Interrupt Electrical Data/Timing

Table 5-20. External Interrupt Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(INT)}$ (2)	Pulse duration, INT input low/high	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-64.
(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

Table 5-21. External Interrupt Switching Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{w(IQSW)} + 12t_{c(SCO)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 5-64.

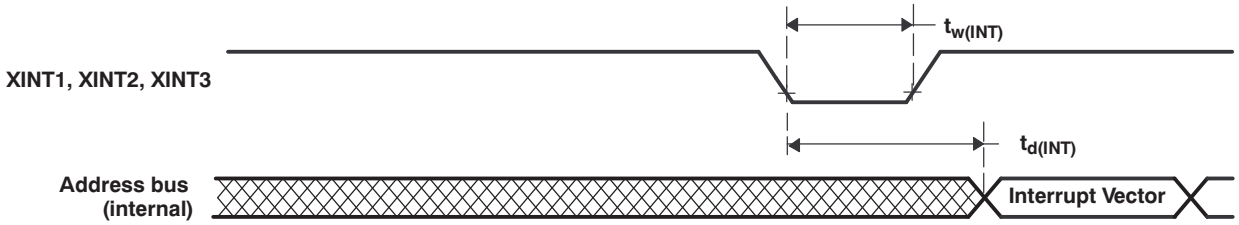


Figure 5-11. External Interrupt Timing

5.9 Peripherals

5.9.1 Control Law Accelerator (CLA) Overview

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Utilizing the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurently. The following is a list of major features of the CLA.

- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
  - Complete bus architecture:
    - Program address bus and program data bus
    - Data address bus, data read bus, and data write bus
  - Independent eight-stage pipeline.
  - 12-bit program counter (MPC)
  - Four 32-bit result registers (MR0–MR3)
  - Two 16-bit auxillary registers (MAR0, MAR1)
  - Status register (MSTF)
- Instruction set includes:
  - IEEE single-precision (32-bit) floating-point math operations
  - Floating-point math with parallel load or store
  - Floating-point multiply with parallel add or subtract
  - 1/X and 1/sqrt(X) estimations
  - Data type conversions.
  - Conditional branch and call
  - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines.
  - The start address of each task is specified by the MVECT registers.
  - No limit on task size as long as the tasks fit within the CLA program memory space.
  - One task is serviced at a time through to completion. There is no nesting of tasks.
  - Upon task completion, a task-specific interrupt is flagged within the PIE.
  - When a task finishes, the next highest-priority pending task is automatically started.
- Task trigger mechanisms:
  - C28x CPU through the IACK instruction
  - Task1 to Task7: the corresponding ADC or ePWM module interrupt. For example:
    - Task1: ADCINT1 or EPWM1_INT
    - Task2: ADCINT2 or EPWM2_INT
    - Task7: ADCINT7 or EPWM7_INT
  - Task8: ADCINT8 or by CPU Timer 0.
- Memory and Shared Peripherals:
  - Two dedicated message RAMs for communication between the CLA and the main CPU.
  - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
  - The CLA has direct access to the ADC Result registers, comparator registers, and the ePWM+HRPWM registers.

For more information on the CLA, see the *TMS320x2803x Piccolo Control Law Accelerator (CLA) Reference Guide*.

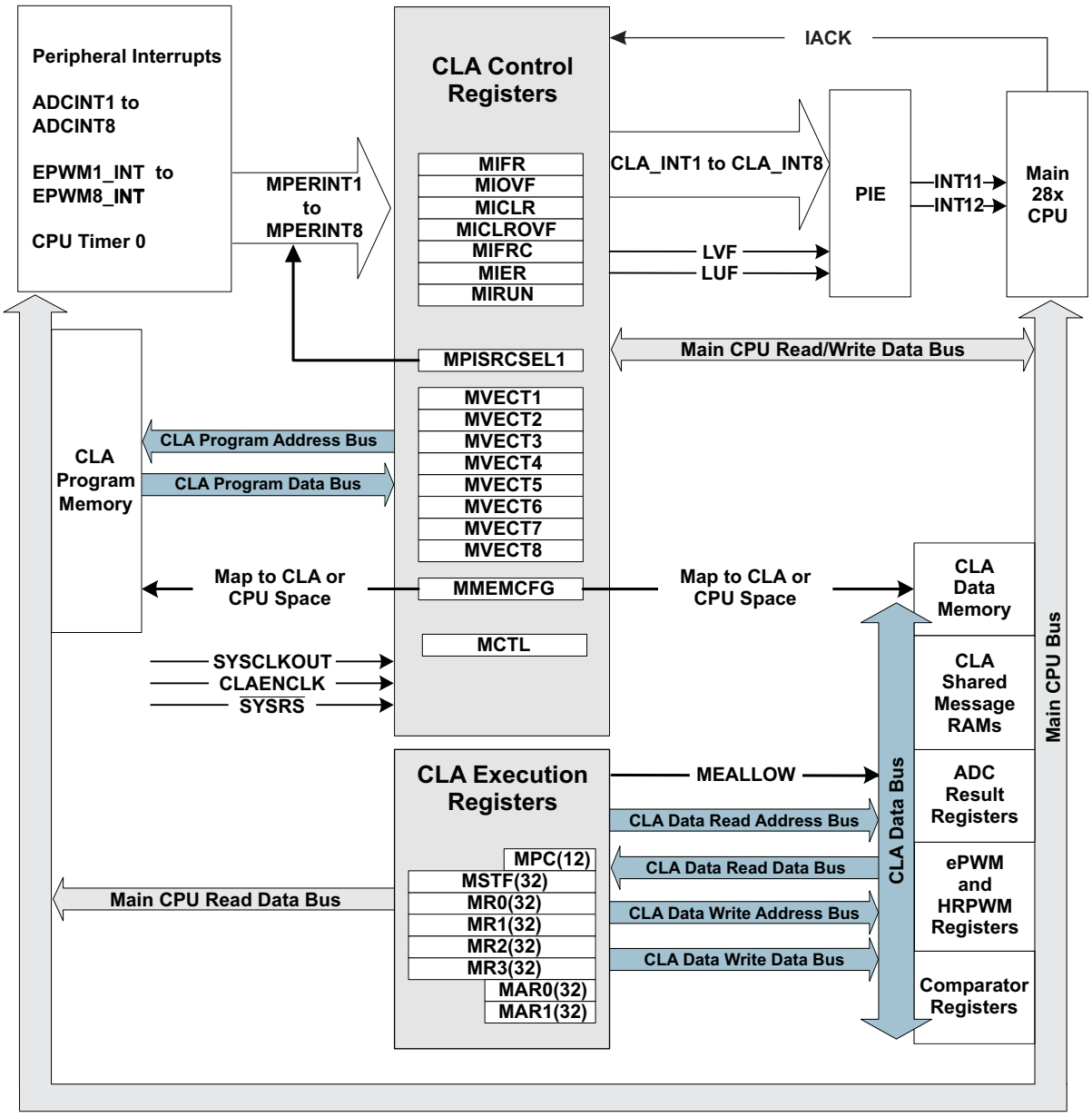


Figure 5-12. CLA Block Diagram

Table 5-22. CLA Control Registers

REGISTER NAME	CLA1 ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION(1)
MVECT1	0x1400	1	Yes	CLA Interrupt/Task 1 Start Address
MVECT2	0x1401	1	Yes	CLA Interrupt/Task 2 Start Address
MVECT3	0x1402	1	Yes	CLA Interrupt/Task 3 Start Address
MVECT4	0x1403	1	Yes	CLA Interrupt/Task 4 Start Address
MVECT5	0x1404	1	Yes	CLA Interrupt/Task 5 Start Address
MVECT6	0x1405	1	Yes	CLA Interrupt/Task 6 Start Address
MVECT7	0x1406	1	Yes	CLA Interrupt/Task 7 Start Address
MVECT8	0x1407	1	Yes	CLA Interrupt/Task 8 Start Address
MCTL	0x1410	1	Yes	CLA Control Register
MMEMCFG	0x1411	1	Yes	CLA Memory Configure Register
MPISRCSEL1	0x1414	2	Yes	Peripheral Interrupt Source Select Register 1
MIFR	0x1420	1	Yes	Interrupt Flag Register
MIOVF	0x1421	1	Yes	Interrupt Overflow Register
MIFRC	0x1422	1	Yes	Interrupt Force Register
MICLR	0x1423	1	Yes	Interrupt Clear Register
MICLROVF	0x1424	1	Yes	Interrupt Overflow Clear Register
MIER	0x1425	1	Yes	Interrupt Enable Register
MIRUN	0x1426	1	Yes	Interrupt RUN Register
MIPCTL	0x1427	1	Yes	Interrupt Priority Control Register
MPC(2)	0x1428	1	–	CLA Program Counter
MAR0(2)	0x142A	1	–	CLA Aux Register 0
MAR1(2)	0x142B	1	–	CLA Aux Register 1
MSTF(2)	0x142E	2	–	CLA STF Register
MR0(2)	0x1430	2	–	CLA R0H Register
MR1(2)	0x1434	2	–	CLA R1H Register
MR2(2)	0x1438	2	–	CLA R2H Register
MR3(2)	0x143C	2	–	CLA R3H Register

(1) All registers in this table are CSM protected
(2) The main C28x CPU has read only access to this register for debug purposes. The main CPU cannot perform CPU or debugger writes to this register.

Table 5-23. CLA Message RAM

ADDRESS RANGE	SIZE (x16)	DESCRIPTION
0x1480 – 0x14FF	128	CLA to CPU Message RAM
0x1500 – 0x157F	128	CPU to CLA Message RAM

5.9.2 Analog Block

A 12-bit ADC core is implemented that has different timings than the 12-bit ADC used on F280x/F2833x. The ADC wrapper is modified to incorporate the new timings and also other enhancements to improve the timing control of start of conversions. Figure 5-13 shows the interaction of the analog module with the rest of the F2803x system.

For more information on the ADC, see the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide*.

56-Pin 64-Pin	80-Pin
VDDA	VDDA
VREFLO Tied To VSSA	VSSA
	VREFLO
VREFHI Tied To A0	VREFHI
	A0
A1	A1
A2	A2
A3	A3
A4	A4
	A5
A6	A6
A7	A7
B0	B0
B1	B1
B2	B2
B3	B3
B4	B4
	B5
B6	B6
B7	B7

Signal Pinout

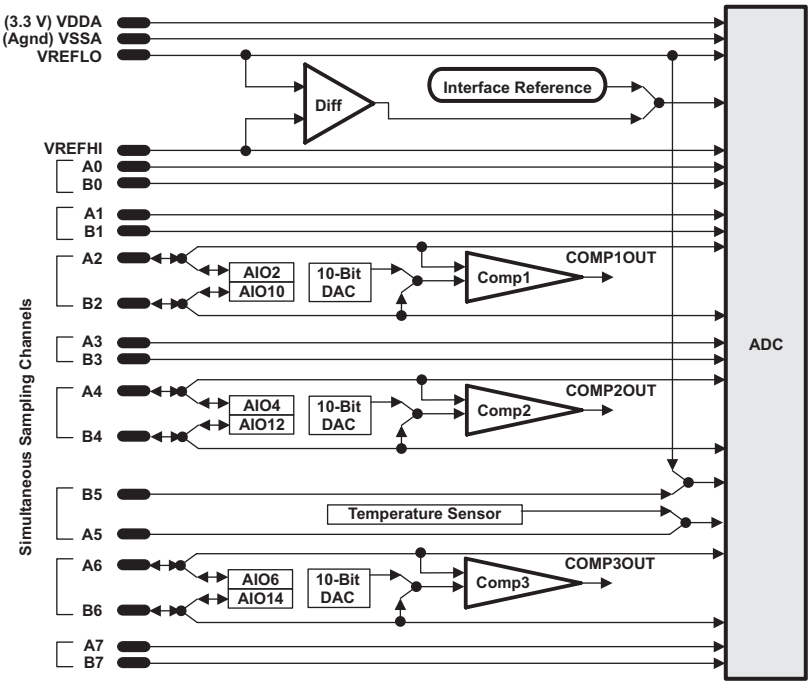


Figure 5-13. Analog Pin Configurations

5.9.2.1 Analog-to-Digital Converter (ADC)

5.9.2.1.1 Features

The core of the ADC contains a single 12-bit converter fed by two sample-and-hold circuits. The sample-and-hold circuits can be sampled simultaneously or sequentially. These, in turn, are fed by a total of up to 16 analog input channels. The converter can be configured to run with an internal band-gap reference to create true-voltage based conversions or with a pair of external voltage references (V_{REFHI}/V_{REFLO}) to create ratiometric-based conversions.

Contrary to previous ADC types, this ADC is not sequencer-based. It is easy for the user to create a series of conversions from a single trigger. However, the basic principle of operation is centered around the configurations of individual conversions, called SOCs, or Start-Of-Conversions.

Functions of the ADC module include:

- 12-bit ADC core with built-in dual sample-and-hold (S/H)
- Simultaneous sampling or sequential sampling modes
- Full range analog input: 0-V to 3.3-V fixed, or V_{REFHI}/V_{REFLO} ratiometric. The digital value of the input analog voltage is derived by:
  - Internal Reference (V_{REFLO} = V_{SSA}. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{3.3}, \quad \text{when } 0\ \text{V} < \text{input} < 3.3\ \text{V}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge 3.3\ \text{V}$$

  - External Reference (V_{REFHI}/V_{REFLO} connected to external references. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{V_{REFHI} - V_{REFLO}}, \quad \text{when } 0\ \text{V} < \text{input} < V_{REFHI}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge V_{REFHI}$$

- Up to 16-channel, multiplexed inputs
- 16 SOCs, configurable for trigger, sample window, and channel
- 16 result registers (individually addressable) to store conversion values
- Multiple trigger sources
  - S/W – software immediate start
  - ePWM 1–7
  - GPIO XINT2
  - CPU Timers 0/1/2
  - ADCINT1/2
- 9 flexible PIE interrupts, can configure interrupt request after any conversion

Table 5-24. ADC Configuration and Control Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCCTL1	0x7100	1	Yes	Control 1 Register
ADCCTL2	0x7101	1	Yes	Control 2 Register
ADCINTFLG	0x7104	1	No	Interrupt Flag Register
ADCINTFLGCLR	0x7105	1	No	Interrupt Flag Clear Register
ADCINTOVF	0x7106	1	No	Interrupt Overflow Register
ADCINTOVFCLR	0x7107	1	No	Interrupt Overflow Clear Register
INTSEL1N2	0x7108	1	Yes	Interrupt 1 and 2 Selection Register
INTSEL3N4	0x7109	1	Yes	Interrupt 3 and 4 Selection Register
INTSEL5N6	0x710A	1	Yes	Interrupt 5 and 6 Selection Register
INTSEL7N8	0x710B	1	Yes	Interrupt 7 and 8 Selection Register
INTSEL9N10	0x710C	1	Yes	Interrupt 9 Selection Register (reserved Interrupt 10 Selection)
SOCPRICTL	0x7110	1	Yes	SOC Priority Control Register
ADCSAMPLEMODE	0x7112	1	Yes	Sampling Mode Register
ADCINTSOCSEL1	0x7114	1	Yes	Interrupt SOC Selection 1 Register (for 8 channels)
ADCINTSOCSEL2	0x7115	1	Yes	Interrupt SOC Selection 2 Register (for 8 channels)
ADCSOCFLG1	0x7118	1	No	SOC Flag 1 Register (for 16 channels)
ADCSOCFRC1	0x711A	1	No	SOC Force 1 Register (for 16 channels)
ADCSOCOVF1	0x711C	1	No	SOC Overflow 1 Register (for 16 channels)
ADCSOCOVFCLR1	0x711E	1	No	SOC Overflow Clear 1 Register (for 16 channels)
ADCSOC0CTL to ADCSOC15CTL	0x7120 – 0x712F	1	Yes	SOC0 Control Register to SOC15 Control Register
ADCREFTRIM	0x7140	1	Yes	Reference Trim Register
ADCOFFTRIM	0x7141	1	Yes	Offset Trim Register
COMPHYSTCTL	0x714C	1	Yes	Comparator Hysteresis Control Register
ADCREV	0x714F	1	No	Revision Register

Table 5-25. ADC Result Registers (Mapped to PF0)

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCRESULT0 to ADCRESULT15	0xB00 to 0xB0F	1	No	ADC Result 0 Register to ADC Result 15 Register

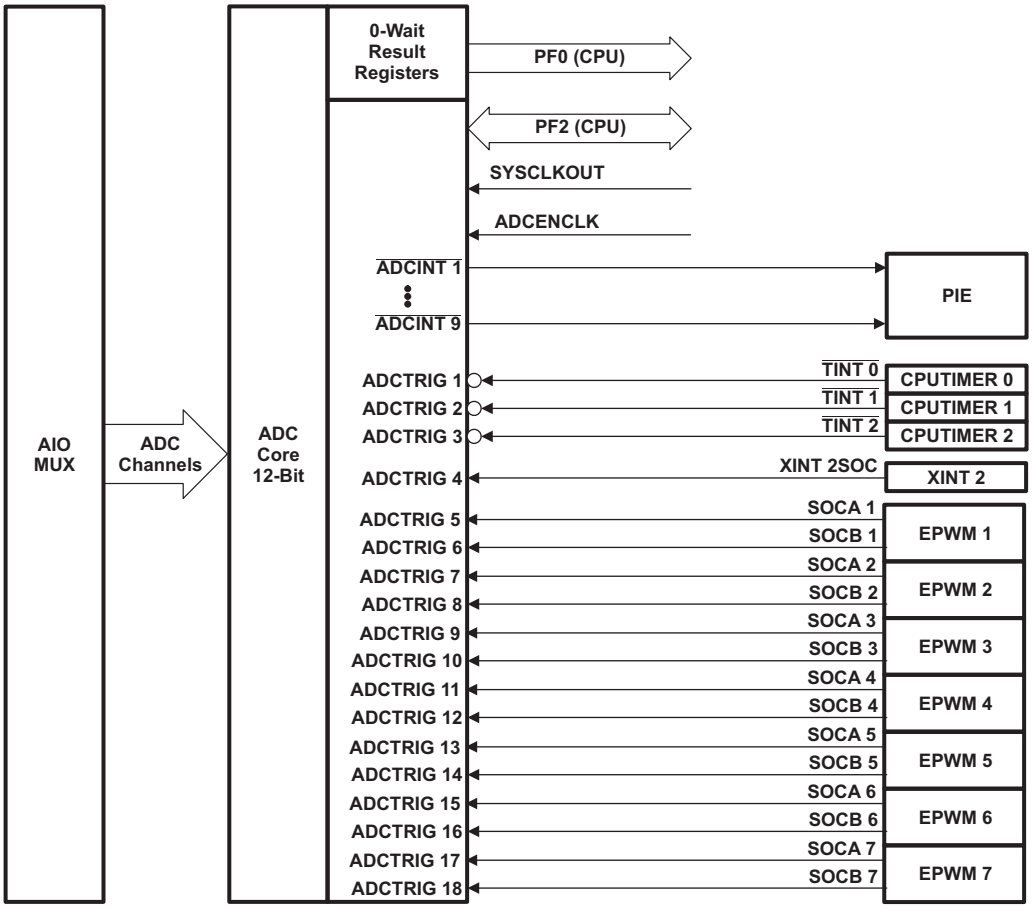


Figure 5-14. ADC Connections

ADC Connections if the ADC is Not Used

TI recommends keeping the connections for the analog power pins, even if the ADC is not used. Following is a summary of how the ADC pins should be connected, if the ADC is not used in an application:

- V_{DDA} – Connect to V_{DDIO}
- V_{SSA} – Connect to V_{SS}
- V_{REFLO} – Connect to V_{SS}
- ADCINAn, ADCINBn, V_{REFHI} – Connect to V_{SSA}

When the ADC module is used in an application, unused ADC input pins should be connected to analog ground (V_{SSA}).

NOTE

Unused ADCIN pins that are multiplexed with AIO function should not be directly connected to analog ground. They should be grounded through a 1-kΩ resistor. This is to prevent an errant code from configuring these pins as AIO outputs and driving grounded pins to a logic-high state.

When the ADC is not used, be sure that the clock to the ADC module is not turned on to realize power savings.

5.9.2.1.2 ADC Start-of-Conversion Electrical Data/Timing

Table 5-26. External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(HCO)}$		cycles

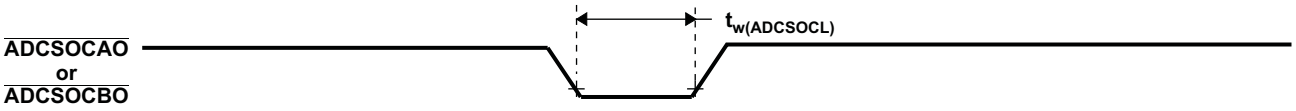


Figure 5-15. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

5.9.2.1.3 On-Chip Analog-to-Digital Converter (ADC) Electrical Data/Timing

Table 5-27. ADC Electrical Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution		12			Bits
ADC clock	60-MHz device	0.001		60	MHz
Sample Window	28035/34/33/32	7		64	ADC Clocks
	28031/30	24		64	
ACCURACY					
INL (Integral nonlinearity) at ADC Clock ≤ 30 MHz(1)		–4		4	LSB
DNL (Differential nonlinearity) at ADC Clock ≤ 30 MHz, no missing codes		–1		1	LSB
Offset error(2)	Executing a single self-recalibration(3)	–20	0	20	LSB
	Executing periodic self-recalibration(4)	–4	0	4	
Overall gain error with internal reference		–60		60	LSB
Overall gain error with external reference		–40		40	LSB
Channel-to-channel offset variation		–4		4	LSB
Channel-to-channel gain variation		–4		4	LSB
ADC temperature coefficient with internal reference			–50		ppm/°C
ADC temperature coefficient with external reference			–20		ppm/°C
V_{REFLO}			–100		µA
V_{REFHI}			100		µA
ANALOG INPUT					
Analog input voltage with internal reference		0		3.3	V
Analog input voltage with external reference		V_{REFLO}		V_{REFHI}	V
V_{REFLO} input voltage(5)		V_{SSA}		0.66	V
V_{REFHI} input voltage(6)		2.64		V_{DDA}	V
	with $V_{REFLO} = V_{SSA}$	1.98		V_{DDA}	
Input capacitance			5		pF
Input leakage current			±2		µA

(1) INL will degrade when the ADC input voltage goes above V_{DDA}.
(2) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and V_{REFHI} - V_{REFLO} for external reference.
(3) For more details, see the *TMS320F2803x Piccolo™ MCUs Silicon Errata*.
(4) Periodic self-recalibration will remove system-level and temperature dependencies on the ADC zero offset error. This can be performed as needed in the application without sacrificing an ADC channel by using the procedure listed in the "ADC Zero Offset Calibration" section of the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide*.
(5) V_{REFLO} is always connected to V_{SSA} on the 64-pin PAG device.
(6) V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes. Because V_{REFHI} is tied to ADCINA0 on the 64-pin PAG device, the input signal on ADCINA0 must not exceed V_{DDA}.

Table 5-28. ADC Power Modes

ADC OPERATING MODE	CONDITIONS	I_{DDA}	UNITS
Mode A – Operating Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 1)	13	mA
Mode B – Quick Wake Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 0)	4	mA
Mode C – Comparator-Only Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0)	1.5	mA
Mode D – Off Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 0) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0)	0.075	mA

5.9.2.1.3.1 Internal Temperature Sensor

Table 5-29. Temperature Sensor Coefficient

PARAMETER(1)		MIN	TYP	MAX	UNIT
T_{SLOPE}	Degrees C of temperature movement per measured ADC LSB change of the temperature sensor		0.18(2)(3)		°C/LSB
T_{OFFSET}	ADC output at 0°C of the temperature sensor		1750		LSB

(1) The temperature sensor slope and offset are given in terms of ADC LSBs using the internal reference of the ADC. Values must be adjusted accordingly in external reference mode to the external reference voltage.
(2) ADC temperature coeffieicient is accounted for in this specification
(3) Output of the temperature sensor (in terms of LSBs) is sign-consistent with the direction of the temperature movement. Increasing temperatures will give increasing ADC values relative to an initial value; decreasing temperatures will give decreasing ADC values relative to an initial value.

5.9.2.1.3.2 ADC Power-Up Control Bit Timing

Table 5-30. ADC Power-Up Delays

PARAMETER(1)		MIN	MAX	UNIT
$t_{d(PWD)}$	Delay time for the ADC to be stable after power up		1	ms

(1) Timings maintain compatibility to the ADC module. The 2803x ADC supports driving all 3 bits at the same time $t_{d(PWD)}$ ms before first conversion.

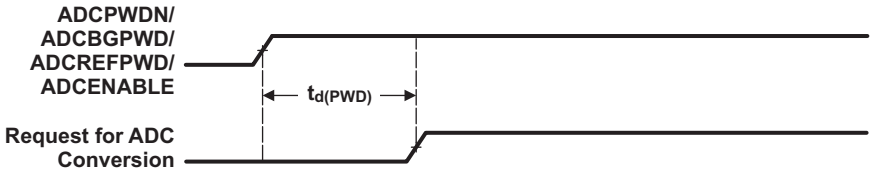
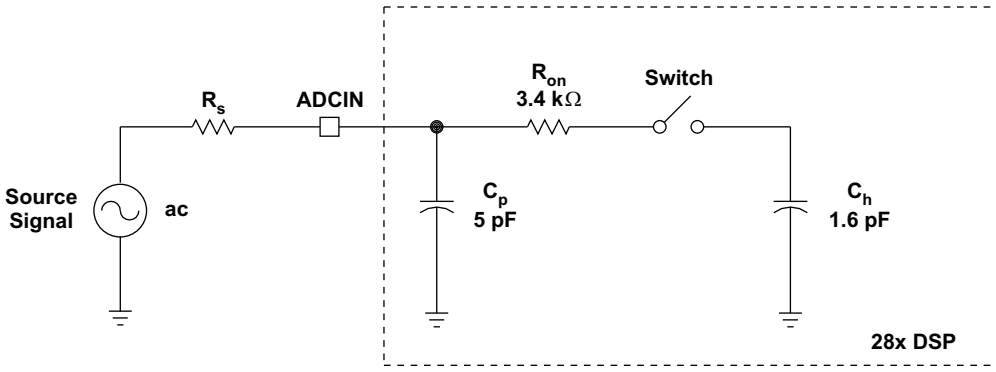


Figure 5-16. ADC Conversion Timing



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}): 3.4 kΩ
Sampling Capacitor (C_h): 1.6 pF
Parasitic Capacitance (C_p): 5 pF
Source Resistance (R_s): 50 Ω

Figure 5-17. ADC Input Impedance Model

5.9.2.1.3.3 ADC Sequential and Simultaneous Timings

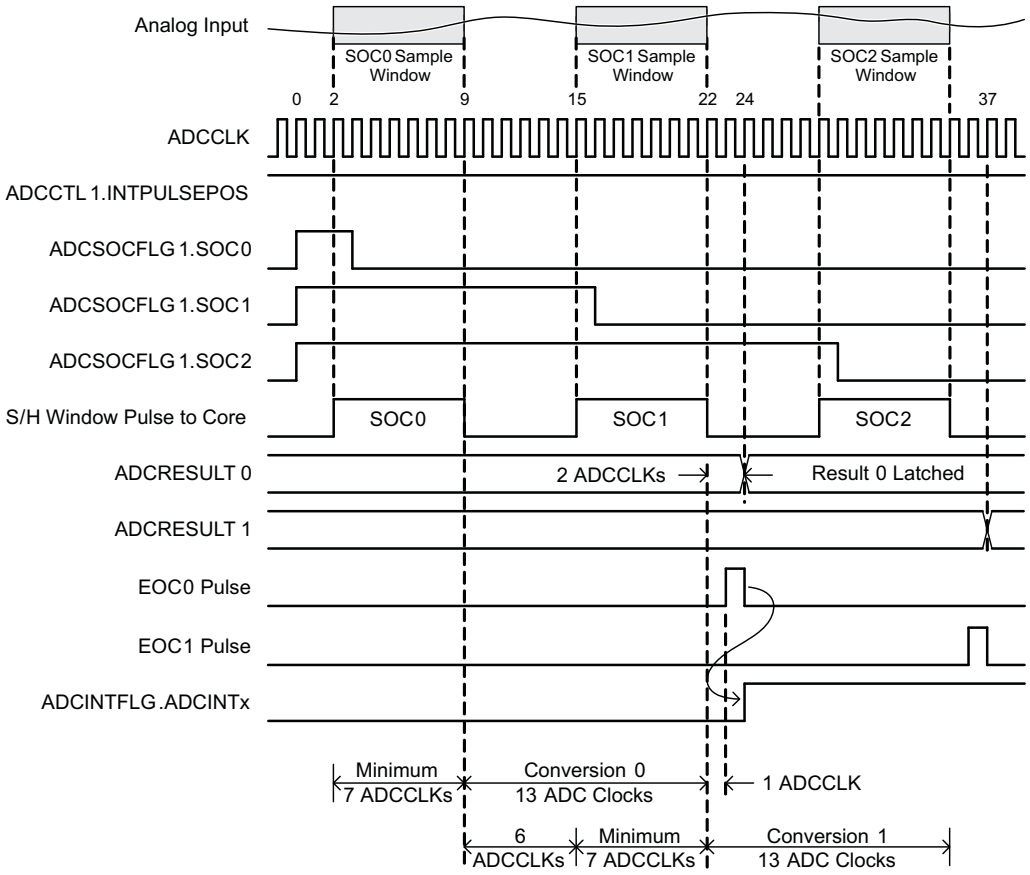


Figure 5-18. Timing Example for Sequential Mode / Late Interrupt Pulse

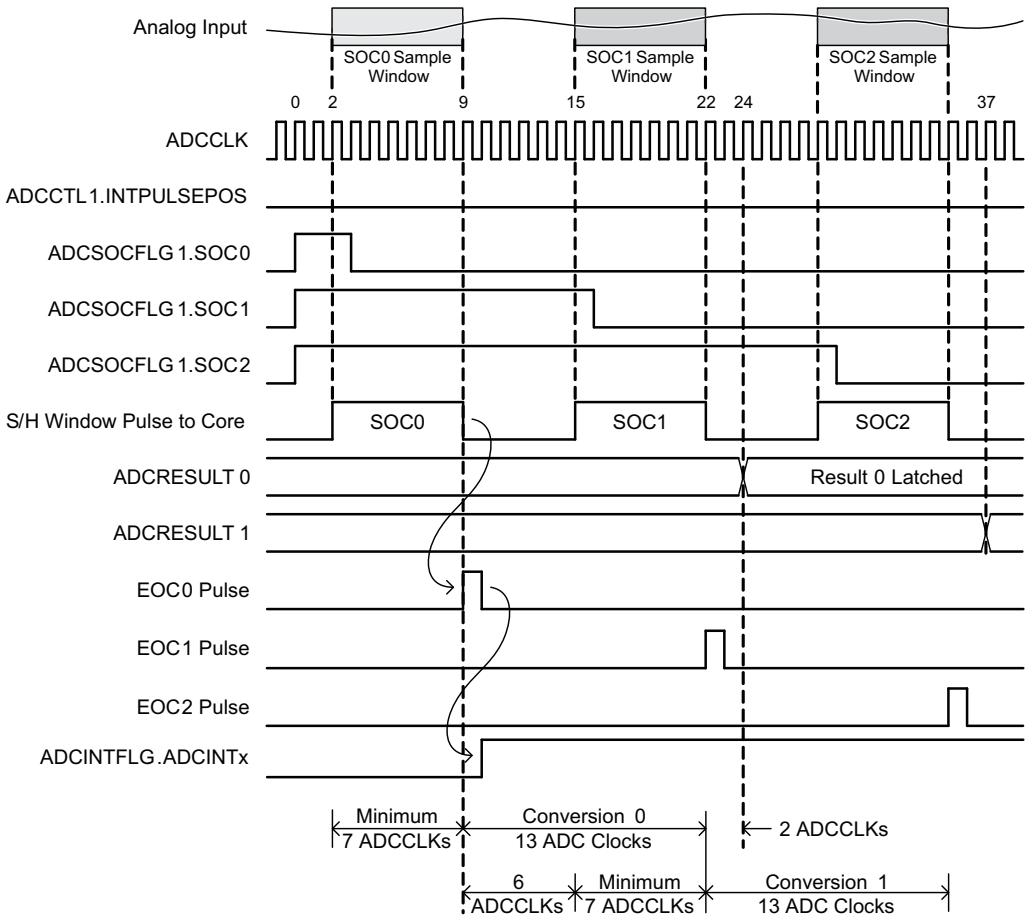


Figure 5-19. Timing Example for Sequential Mode / Early Interrupt Pulse

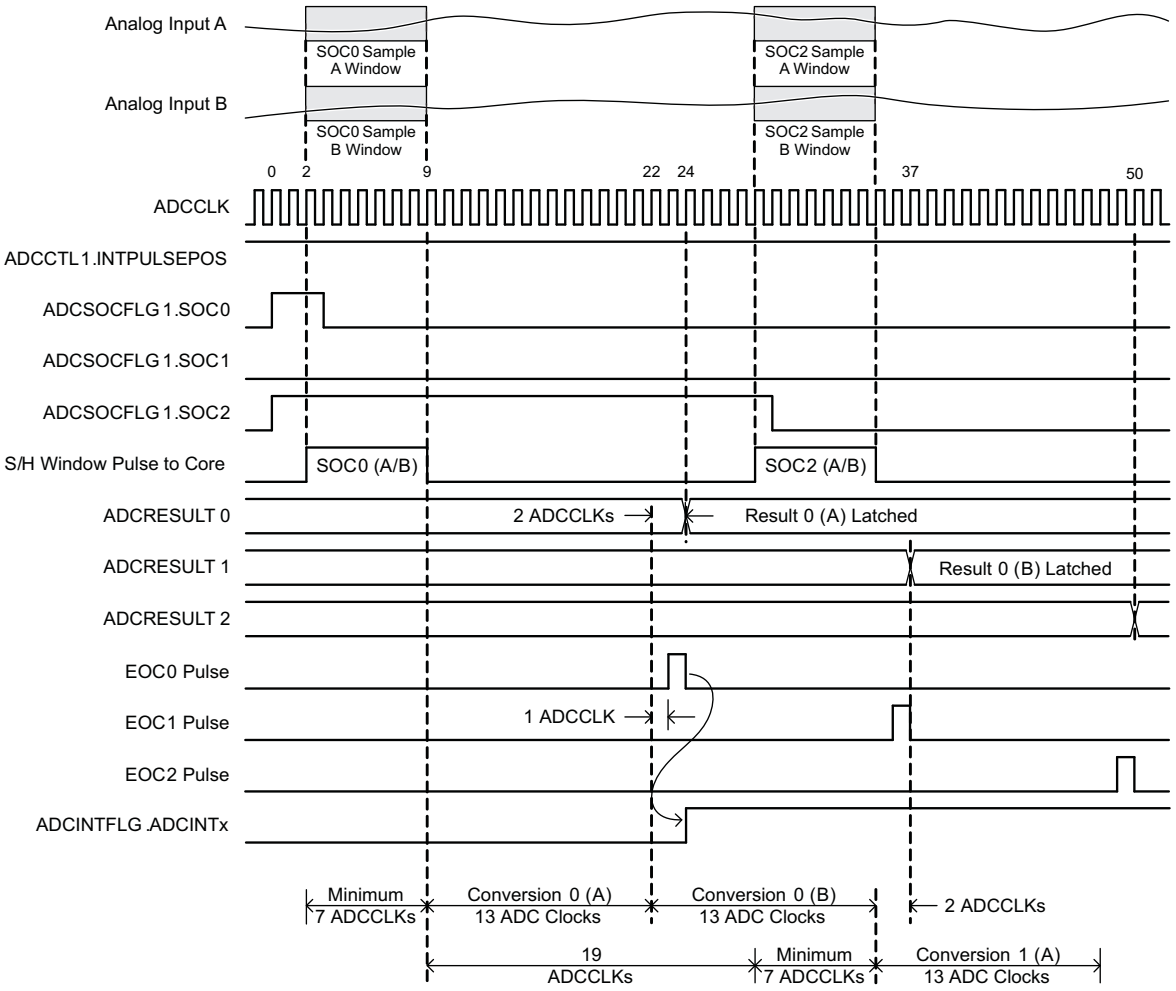


Figure 5-20. Timing Example for Simultaneous Mode / Late Interrupt Pulse

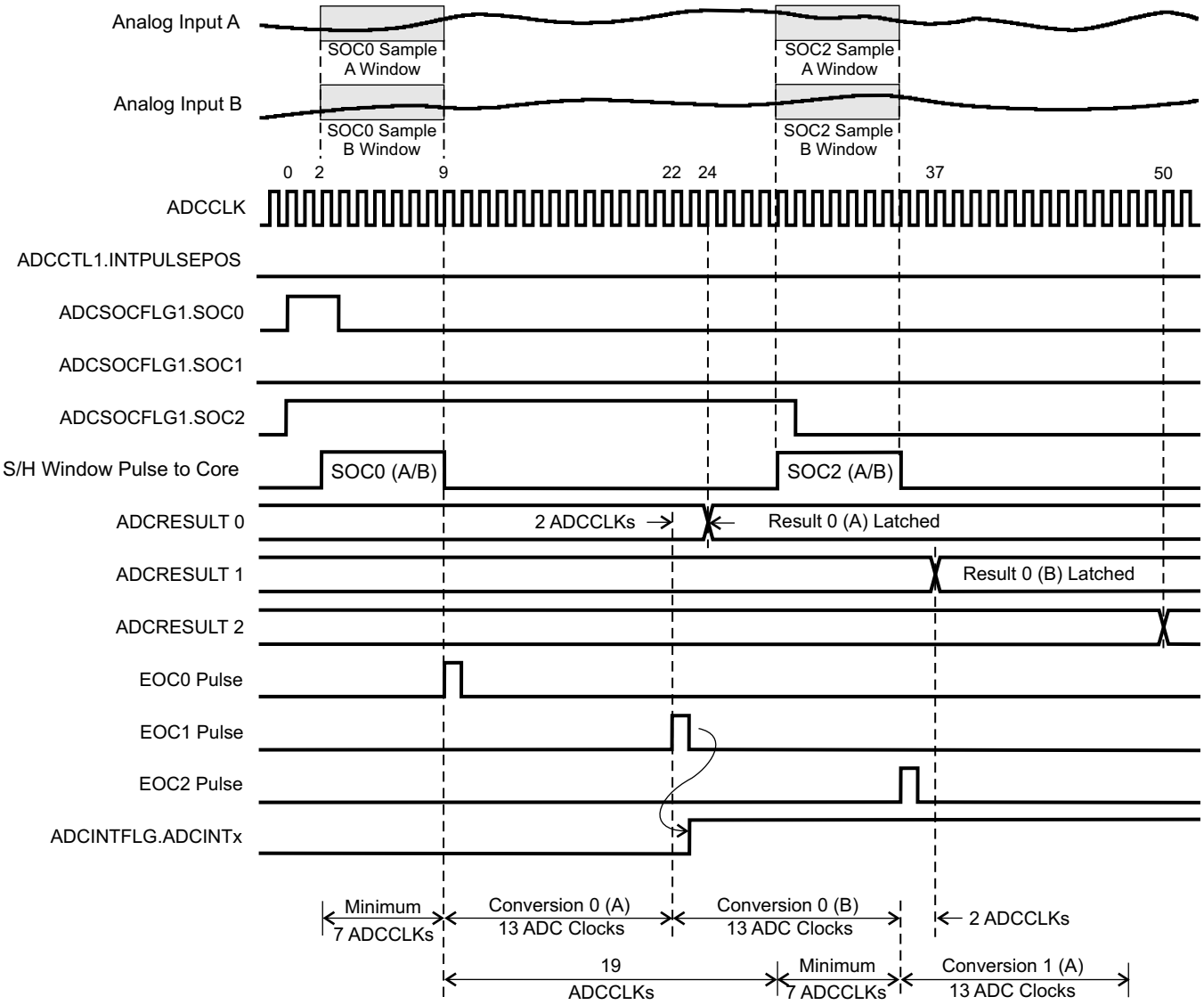


Figure 5-21. Timing Example for Simultaneous Mode / Early Interrupt Pulse

5.9.2.2 ADC MUX

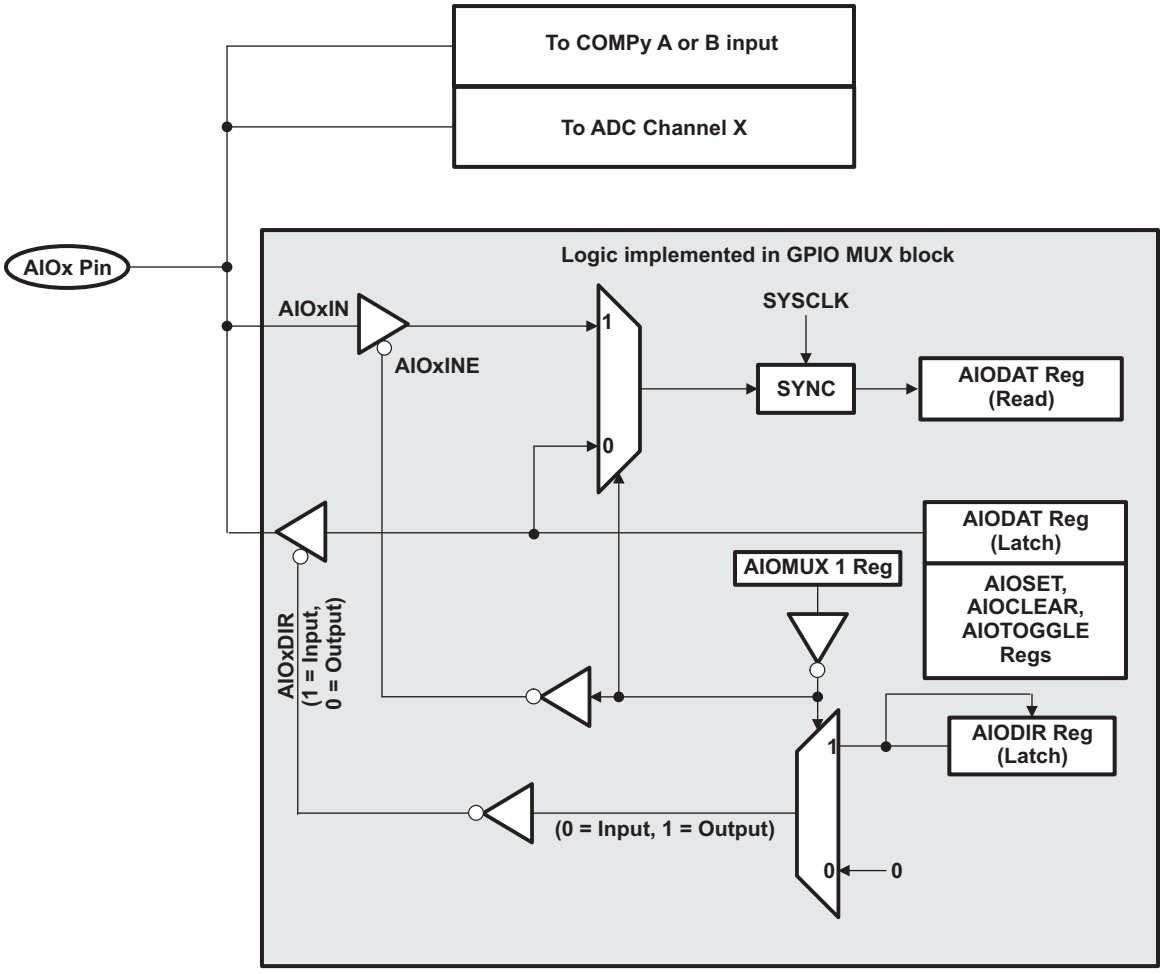


Figure 5-22. AIOx Pin Multiplexing

The ADC channel and Comparator functions are always available. The digital I/O function is available only when the respective bit in the AIOMUX1 register is 0. In this mode, reading the AIODAT register reflects the actual pin state.

The digital I/O function is disabled when the respective bit in the AIOMUX1 register is 1. In this mode, reading the AIODAT register reflects the output latch of the AIODAT register and the input digital I/O buffer is disabled to prevent analog signals from generating noise.

On reset, the digital function is disabled. If the pin is used as an analog input, users should keep the AIO function disabled for that pin.

5.9.2.3 Comparator Block

Figure 5-23 shows the interaction of the Comparator modules with the rest of the system.

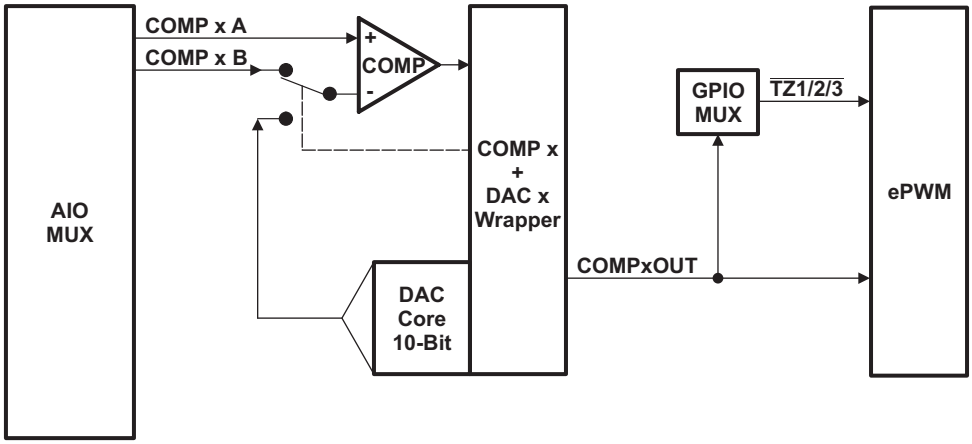


Figure 5-23. Comparator Block Diagram

Table 5-31. Comparator Control Registers

REGISTER NAME	COMP1 ADDRESS	COMP2 ADDRESS	COMP3 ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
COMPCTL	0x6400	0x6420	0x6440	1	Yes	Comparator Control Register
COMPSTS	0x6402	0x6422	0x6442	1	No	Comparator Status Register
DACCTL	0x6404	0x6424	0x6444	1	Yes	DAC Control Register
DACVAL	0x6406	0x6426	0x6446	1	No	DAC Value Register
RAMPMAXREF_ ACTIVE	0x6408	0x6428	0x6448	1	No	Ramp Generator Maximum Reference (Active) Register
RAMPMAXREF_ SHDW	0x640A	0x642A	0x644A	1	No	Ramp Generator Maximum Reference (Shadow) Register
RAMPDECVAL_ ACTIVE	0x640C	0x642C	0x644C	1	No	Ramp Generator Decrement Value (Active) Register
RAMPDECVAL_ SHDW	0x640E	0x642E	0x644E	1	No	Ramp Generator Decrement Value (Shadow) Register
RAMPSTS	0x6410	0x6430	0x6450	1	No	Ramp Generator Status Register

5.9.2.3.1 On-Chip Comparator/DAC Electrical Data/Timing

Table 5-32. Electrical Characteristics of the Comparator/DAC

PARAMETER	MIN	TYP	MAX	UNITS
Comparator				
Comparator Input Range		$V_{SSA} – V_{DDA}$		V
Comparator response time to PWM Trip Zone (Async)		30		ns
Input Offset		±5		mV
Input Hysteresis(1)		35		mV
DAC				
DAC Output Range		$V_{SSA} – V_{DDA}$		V
DAC resolution		10		bits
DAC settling time		See Figure 5-24		
DAC Gain		–1.5%		
DAC Offset		10		mV
Monotonic		Yes		
INL		±3		LSB

(1) Hysteresis on the comparator inputs is achieved with a Schmidt trigger configuration. This results in an effective 100-kΩ feedback resistance between the output of the comparator and the noninverting input of the comparator. There is an option to disable the hysteresis and, with it, the feedback resistance; see the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* for more information on this option if needed in your system.

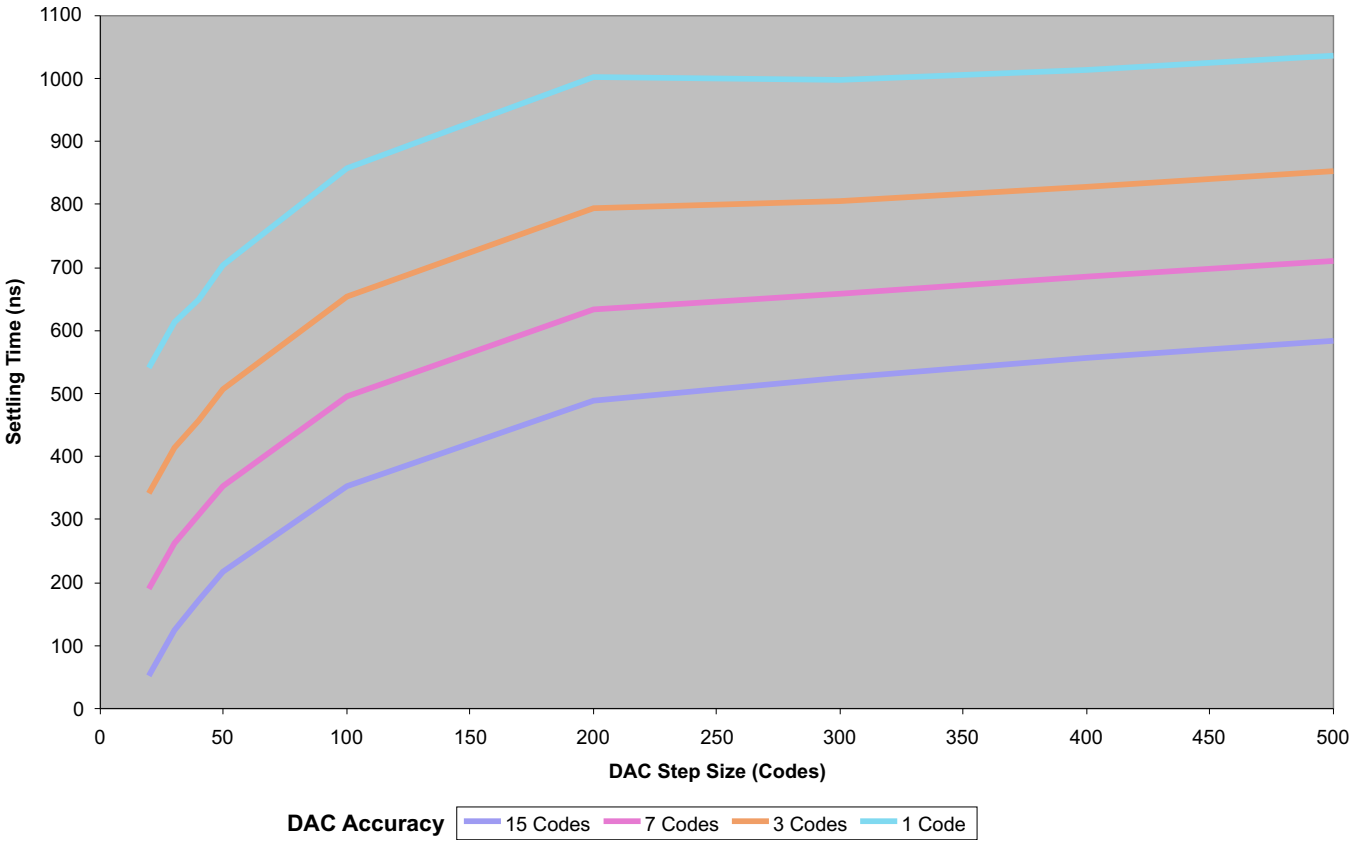


Figure 5-24. DAC Settling Time

5.9.3 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, $N = \frac{(SINAD - 1.76)}{6.02}$ it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

5.9.4 Serial Peripheral Interface (SPI) Module

The device includes the four-pin serial peripheral interface (SPI) module. Up to two SPI modules are available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE

All four pins can be used as GPIO if the SPI module is not used.

- Two operational modes: master and slave
  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \qquad \text{when SPIBRR} = 3 \text{ to } 127$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \qquad \text{when SPIBRR} = 0, 1, 2$$

- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: In control register frame beginning at address 7040h.

NOTE

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 4-level transmit/receive FIFO
- Delayed transmit control
- Bidirectional 3 wire SPI mode support
- Audio data receive support through $\overline{\text{SPISTE}}$ inversion

The SPI port operation is configured and controlled by the registers listed in Table 5-33 and Table 5-34.

Table 5-33. SPI-A Registers

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION(1)
SPICCR	0x7040	1	No	SPI-A Configuration Control Register
SPICTL	0x7041	1	No	SPI-A Operation Control Register
SPISTS	0x7042	1	No	SPI-A Status Register
SPIBRR	0x7044	1	No	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	No	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	No	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	No	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	No	SPI-A Serial Data Register
SPIFFTX	0x704A	1	No	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	No	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	No	SPI-A FIFO Control Register
SPIPRI	0x704F	1	No	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

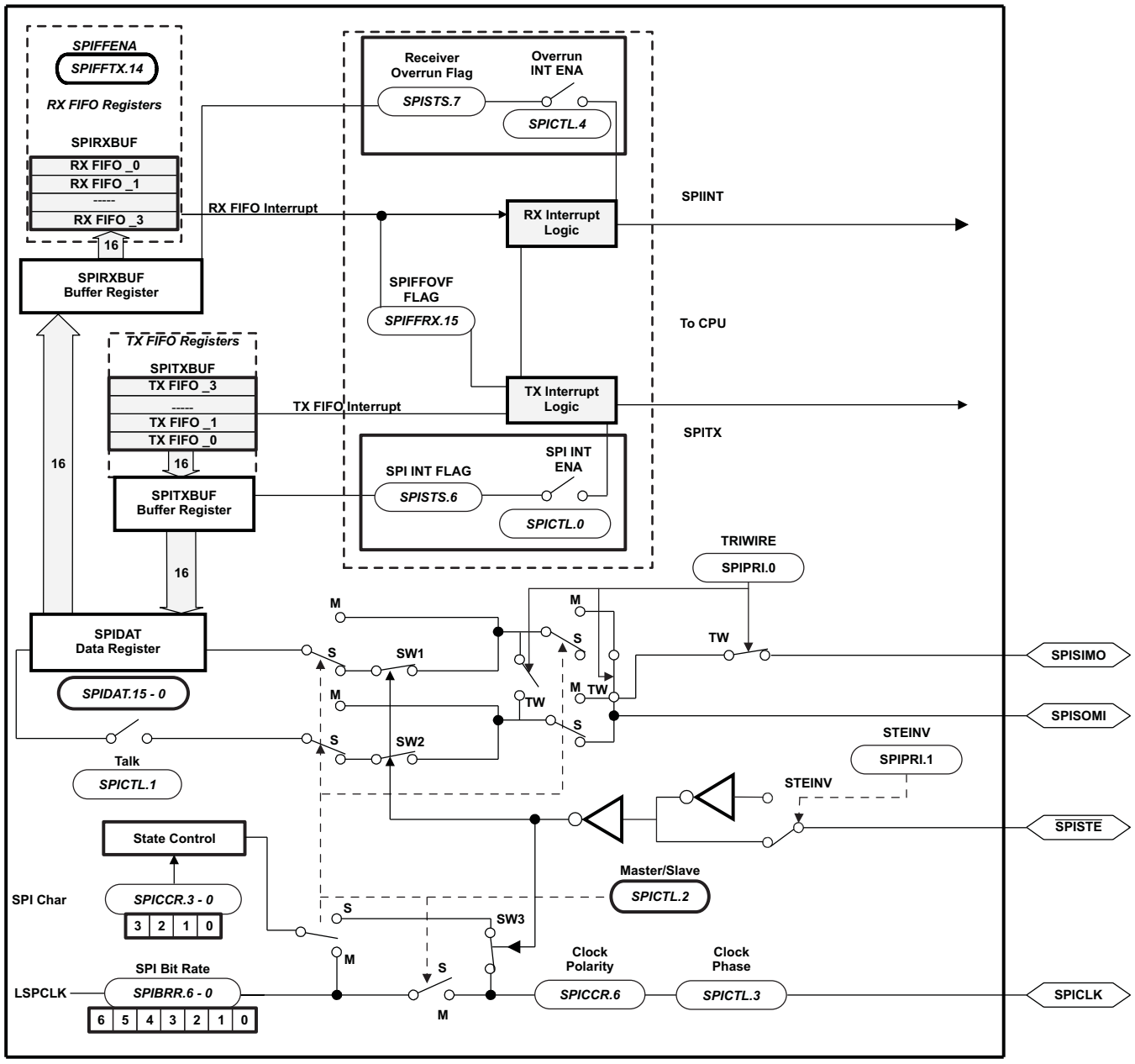
Table 5-34. SPI-B Registers

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION(1)
SPICCR	0x7740	1	No	SPI-B Configuration Control Register
SPICTL	0x7741	1	No	SPI-B Operation Control Register
SPISTS	0x7742	1	No	SPI-B Status Register
SPIBRR	0x7744	1	No	SPI-B Baud Rate Register
SPIRXEMU	0x7746	1	No	SPI-B Receive Emulation Buffer Register
SPIRXBUF	0x7747	1	No	SPI-B Serial Input Buffer Register
SPITXBUF	0x7748	1	No	SPI-B Serial Output Buffer Register
SPIDAT	0x7749	1	No	SPI-B Serial Data Register
SPIFFTX	0x774A	1	No	SPI-B FIFO Transmit Register
SPIFFRX	0x774B	1	No	SPI-B FIFO Receive Register
SPIFFCT	0x774C	1	No	SPI-B FIFO Control Register
SPIPRI	0x774F	1	No	SPI-B Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

For more information on the SPI, see the *TMS320x2802x, 2803x Piccolo Serial Peripheral Interface (SPI) Reference Guide*.

Figure 5-25 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

Figure 5-25. SPI Module Block Diagram (Slave Mode)

5.9.4.1 SPI Master Mode Electrical Data/Timing

Table 5-35 lists the master mode timing (clock phase = 0) and Table 5-36 lists the master mode timing (clock phase = 1). Figure 5-26 and Figure 5-27 show the timing waveforms.

Table 5-35. SPI Master Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.	PARAMETER		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid		10		10	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
8	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	26		26		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MAX, slave mode receive 12.5-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).

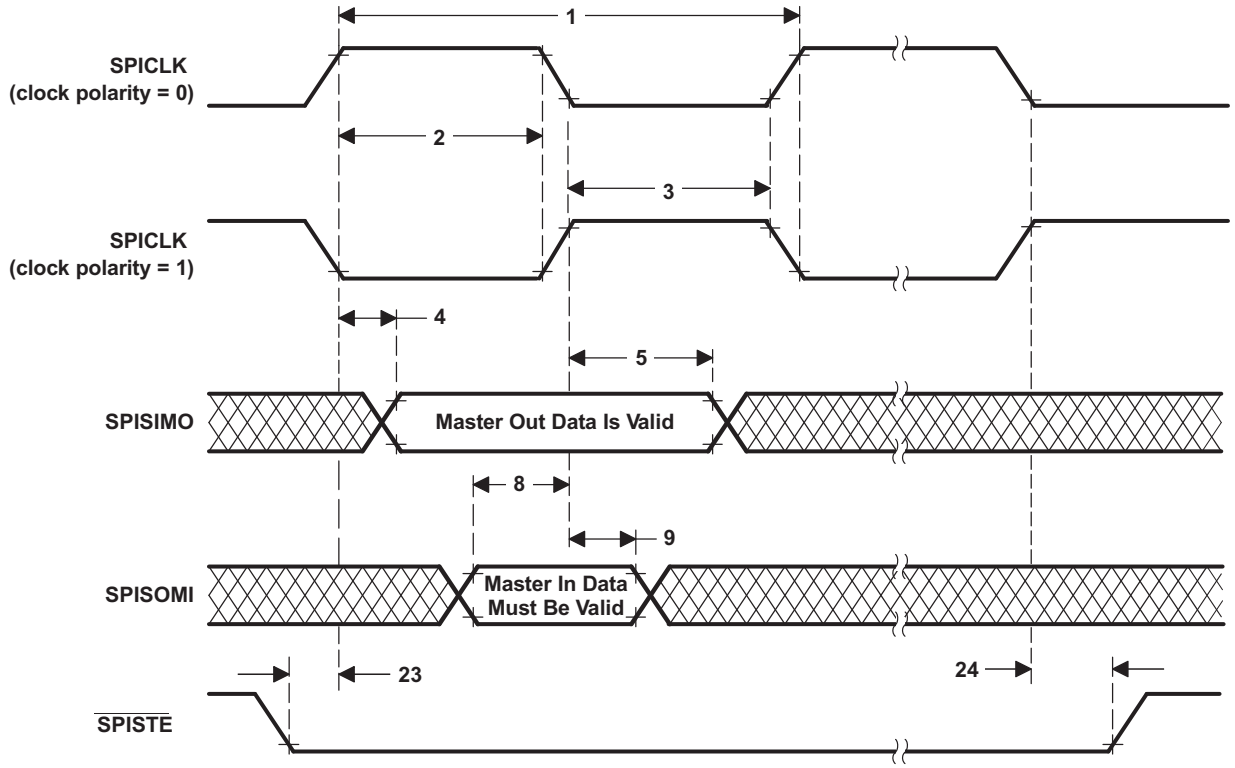


Figure 5-26. SPI Master Mode External Timing (Clock Phase = 0)

Table 5-36. SPI Master Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)(5)

NO.	PARAMETER		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
6	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$		ns
7	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
10	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	26		26		ns
11	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$t_{c(SPC)} - 10$		$t_{c(SPC)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)} - 10$		$0.5t_{c(SPC)} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1).
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

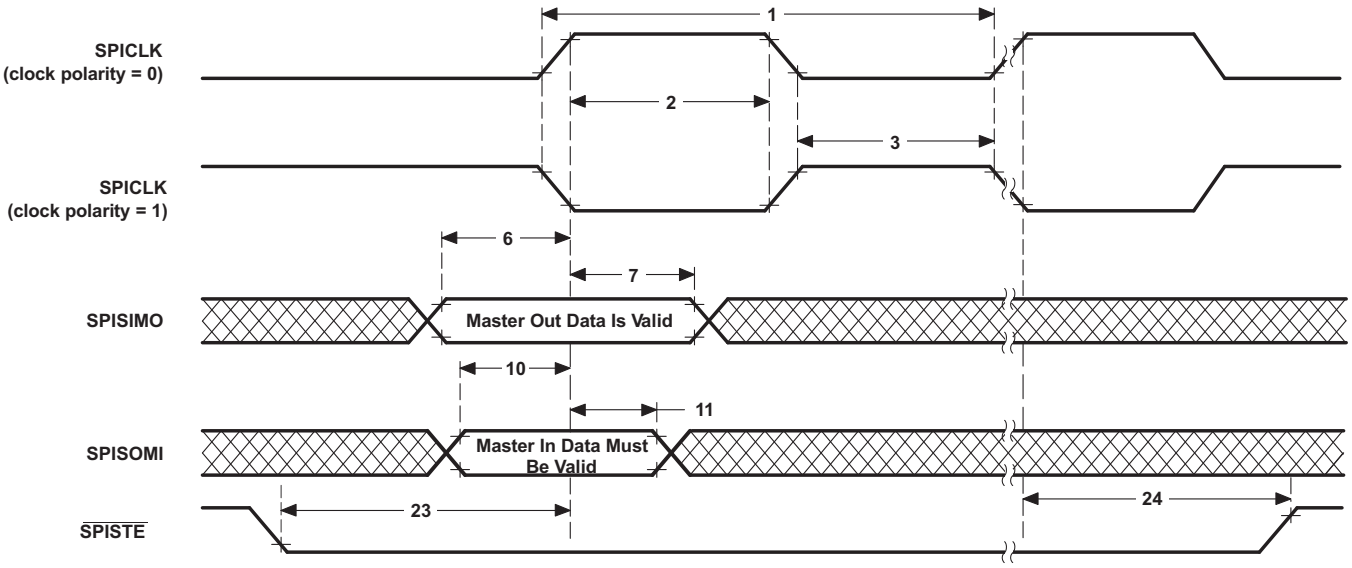


Figure 5-27. SPI Master Mode External Timing (Clock Phase = 1)

5.9.4.2 SPI Slave Mode Electrical Data/Timing

Table 5-37 lists the slave mode timing (clock phase = 0) and Table 5-38 lists the slave mode timing (clock phase = 1). Figure 5-28 and Figure 5-29 show the timing waveforms.

Table 5-37. SPI Slave Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.	PARAMETER		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		21	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1).
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

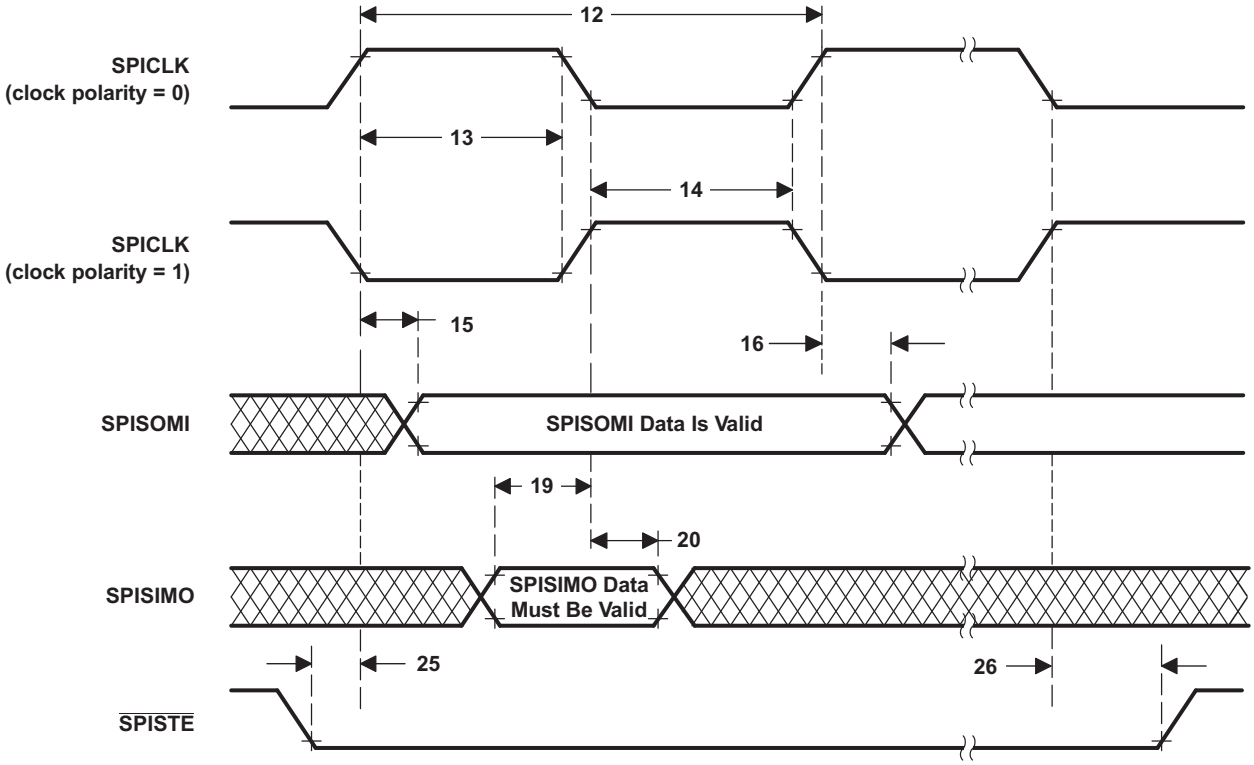


Figure 5-28. SPI Slave Mode External Timing (Clock Phase = 0)

Table 5-38. SPI Slave Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)

NO.	PARAMETER		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
17	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		21	ns
18	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
21	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
22	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1).
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

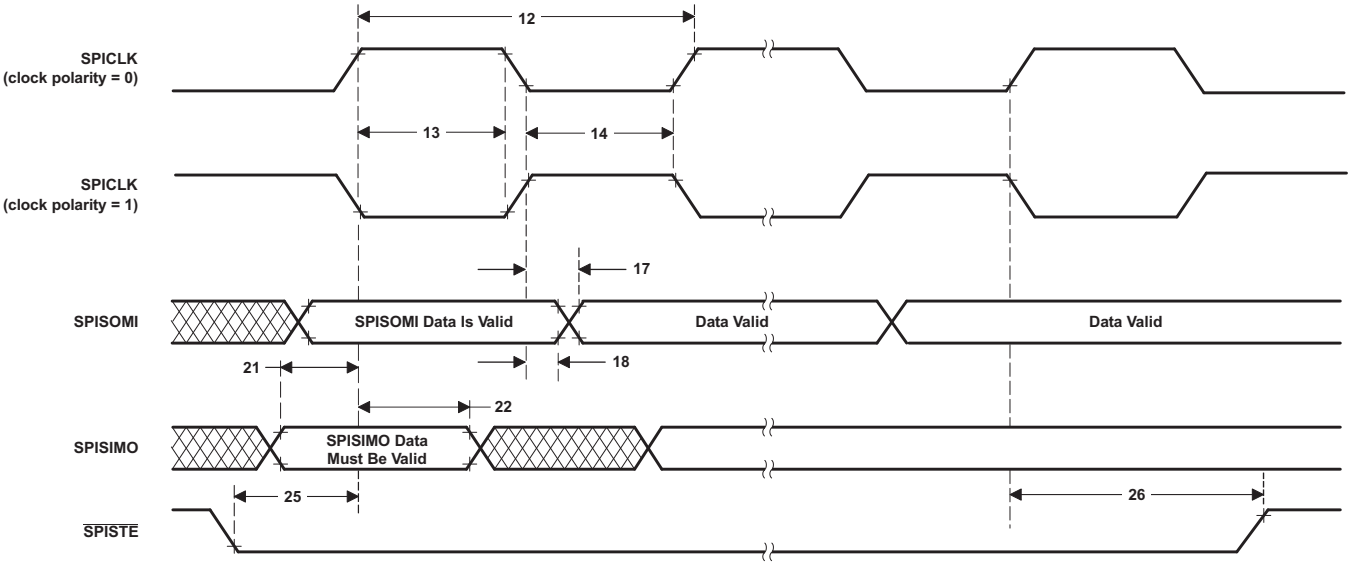


Figure 5-29. SPI Slave Mode External Timing (Clock Phase = 1)

5.9.5 Serial Communications Interface (SCI) Module

The devices include one serial communications interface (SCI) module (SCI-A). The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard nonreturn-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

NOTE

Both pins can be used as GPIO if not used for SCI.

  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \qquad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \qquad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - One or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (nonreturn-to-zero) format

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 4-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 5-39.

Table 5-39. SCI-A Registers(1)

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
SCICCRA	0x7050	1	No	SCI-A Communications Control Register
SCICTL1A	0x7051	1	No	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	No	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	No	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	No	SCI-A Control Register 2
SCIRXSTA	0x7055	1	No	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	No	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	No	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	No	SCI-A Transmit Data Buffer Register
SCIFFTXA(2)	0x705A	1	No	SCI-A FIFO Transmit Register
SCIFFRXA(2)	0x705B	1	No	SCI-A FIFO Receive Register
SCIFFCTA(2)	0x705C	1	No	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	No	SCI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

For more information on the SCI, see the *TMS320x2802x, 2803x Piccolo Serial Communications Interface (SCI) Reference Guide*.

Figure 5-30 shows the SCI module block diagram.

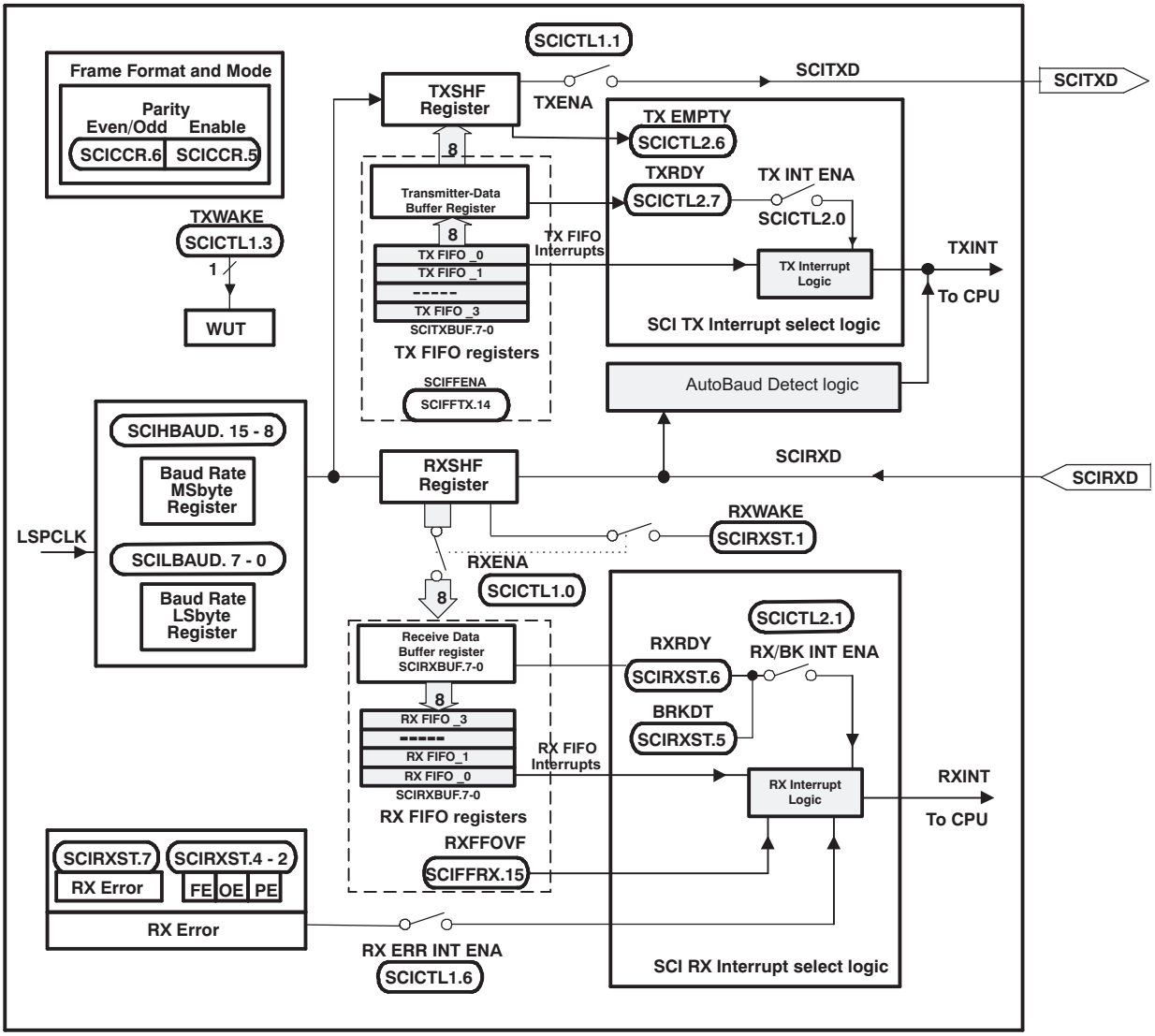


Figure 5-30. Serial Communications Interface (SCI) Module Block Diagram

5.9.6 Local Interconnect Network (LIN)

The device contains one LIN controller. The LIN standard is based on the SCI (UART) serial data link format. The LIN module can be configured to work as a SCI as well.

The LIN module has the following features:

- Compatible to LIN 1.3 or 2.0 protocols
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic master header generation
  - Programmable sync break field
  - Sync field
  - Identifier field
- Slave automatic synchronization
  - Sync break detection
  - Optional baudrate update
  - Synchronization validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wakeup support
  - Wakeup signal generation
  - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
  - Bit error
  - Bus error
  - No-response error
  - Checksum error
  - Sync field error
  - Parity error
- 2 Interrupt lines with priority encoding for:
  - Receive
  - Transmit
  - ID, error and status

NOTE

The 2803x devices have passed LIN 2.0 conformance tests (master and slave). Contact TI for details.

For more information on the LIN, see the *TMS320F2803x Piccolo Local Interconnect Network (LIN) Module User's Guide*.

The registers in Table 5-40 configure and control the operation of the LIN module.

Table 5-40. LIN-A Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCIGCR0	0x6C00	2	Global Control Register 0
SCIGCR1	0x6C02	2	Global Control Register 1
SCIGCR2	0x6C04	2	Global Control Register 2
SCISETINT	0x6C06	2	Interrupt Enable Register
SCICLEARINT	0x6C08	2	Interrupt Disable Register
SCISETINTLVL	0x6C0A	2	Set Interrupt Level Register
SCICLEARINTLVL	0x6C0C	2	Clear Interrupt Level Register
SCIFLR	0x6C0E	2	Flag Register
SCIINTVECT0	0x6C10	2	Interrupt Vector Offset Register 0
SCIINTVECT1	0x6C12	2	Interrupt Vector Offset Register 1
SCIFORMAT	0x6C14	2	Length Control register
BRSR	0x6C16	2	Baud Rate Selection Register
SCIED	0x6C18	2	Emulation buffer register
SCIRD	0x6C1A	2	Receiver data buffer register
SCITD	0x6C1C	2	Transmit data buffer register
Reserved	0x6C1E	4	RSVD
SIPIO2	0x6C22	2	Pin control register 2
Reserved	0x6C24	10	RSVD
LINCOMP	0x6C30	2	Compare register
LINRD0	0x6C32	2	Receive data register 0
LINRD1	0x6C34	2	Receive data register 1
LINMASK	0x6C36	2	Acceptance mask register
LINID	0x6C38	2	Register containing ID- byte, ID-SlaveTask byte, and ID received fields.
LINTD0	0x6C3A	2	Transmit Data Register 0
LINTD1	0x6C3C	2	Transmit Data Register 1
MBRSR	0x6C3E	2	Baud Rate Selection Register
Reserved	0x6C40	8	RSVD
IODFTCTRL	0x6C48	2	IODFT for BLIN

(1) Some registers and some bits in other registers are EALLOW-protected. See the *TMS320F2803x Piccolo Local Interconnect Network (LIN) Module User's Guide* for more details.

Figure 5-31 shows the LIN module block diagram.

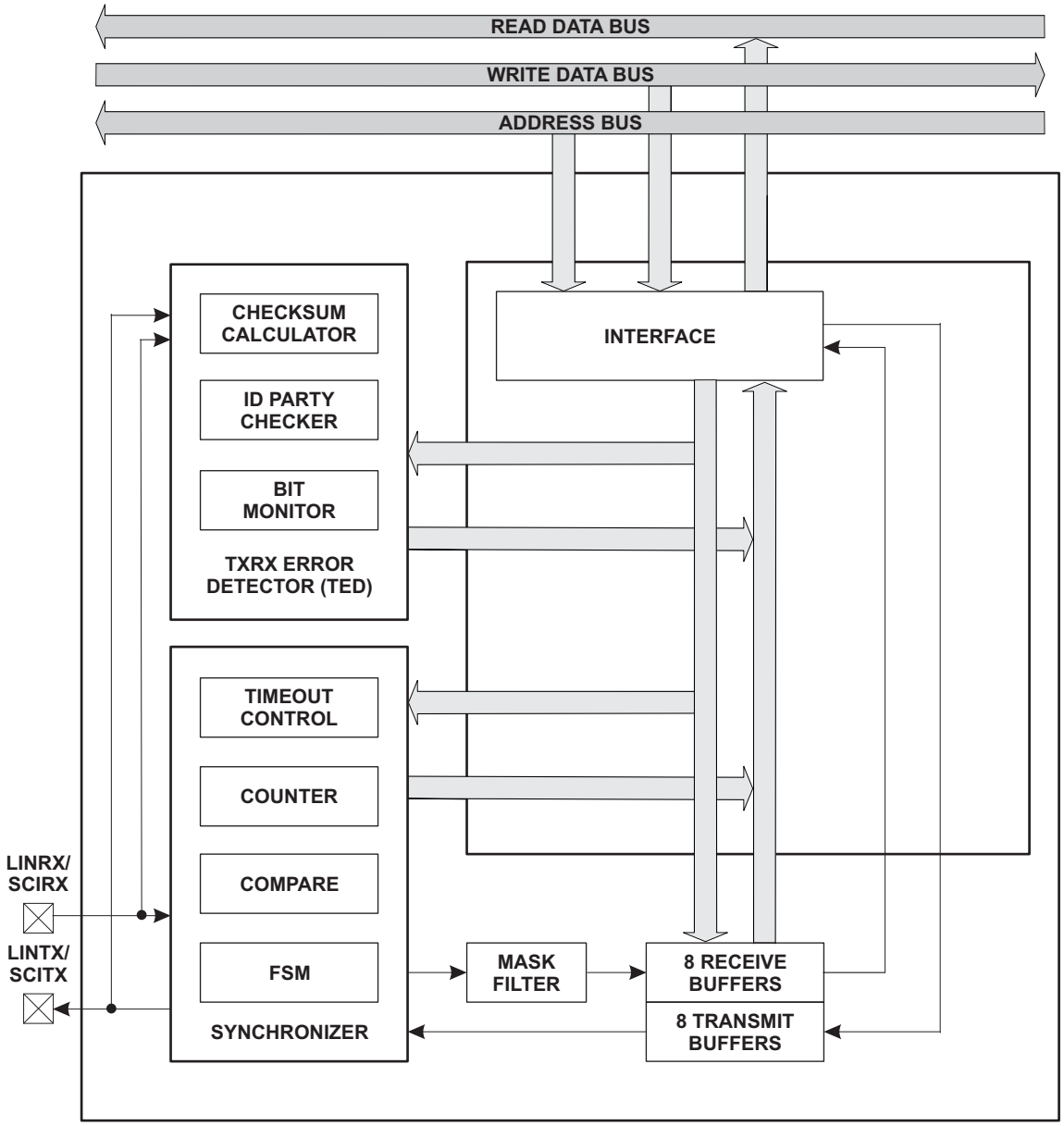


Figure 5-31. LIN Block Diagram

5.9.7 Enhanced Controller Area Network (eCAN) Module

The CAN module (eCAN-A) has the following features:

- Fully compliant with ISO11898-1 (CAN 2.0B)
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE

For a SYSCLKOUT of 60 MHz, the smallest bit rate possible is 4.6875 kbps.

The F2803x CAN has passed the conformance test per ISO/DIS 16845. Contact TI for test report and exceptions.

For information on using the CAN module with the on-chip zero-pin oscillators, see *Piccolo MCU CAN Module Operation Using the On-Chip Zero-Pin Oscillator*.

For more information on the CAN, see the *TMS320x2803x Piccolo Enhanced Controller Area Network (eCAN) Reference Guide*.

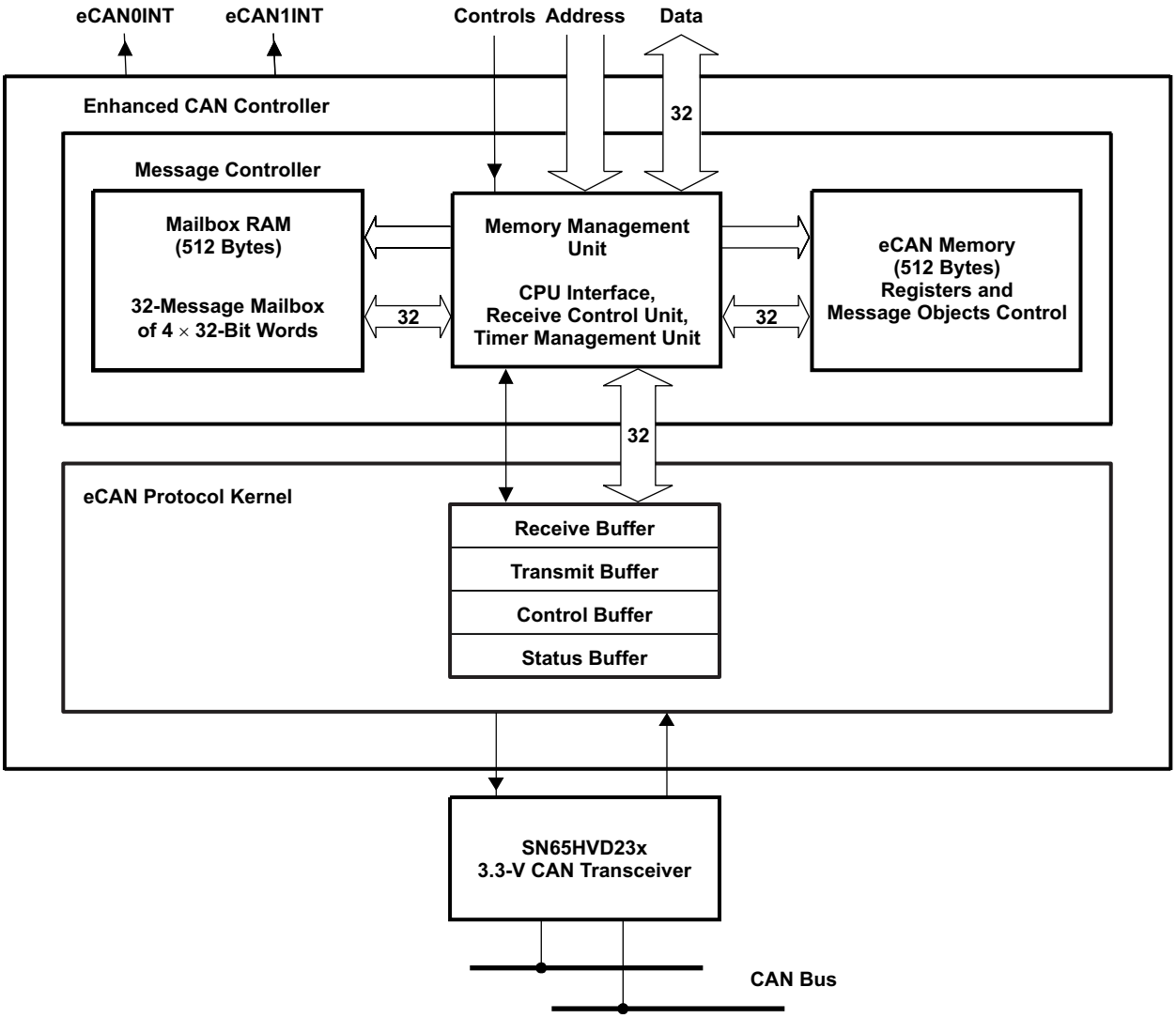


Figure 5-32. eCAN Block Diagram and Interface Circuit

Table 5-41. 3.3-V eCAN Transceivers

PART NUMBER	SUPPLY VOLTAGE	LOW-POWER MODE	SLOPE CONTROL	VREF	OTHER	T_A
SN65HVD230	3.3 V	Standby	Adjustable	Yes	–	–40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	–	–40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 125°C
SN65HVD232	3.3 V	None	None	None	–	–40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	–	–40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	–40°C to 125°C
SN65HVD234	3.3 V	Standby and Sleep	Adjustable	None	–	–40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	–40°C to 125°C
ISO1050	3–5.5 V	None	None	None	Built-in Isolation Low Prop Delay Thermal Shutdown Failsafe Operation Dominant Time-Out	–55°C to 105°C

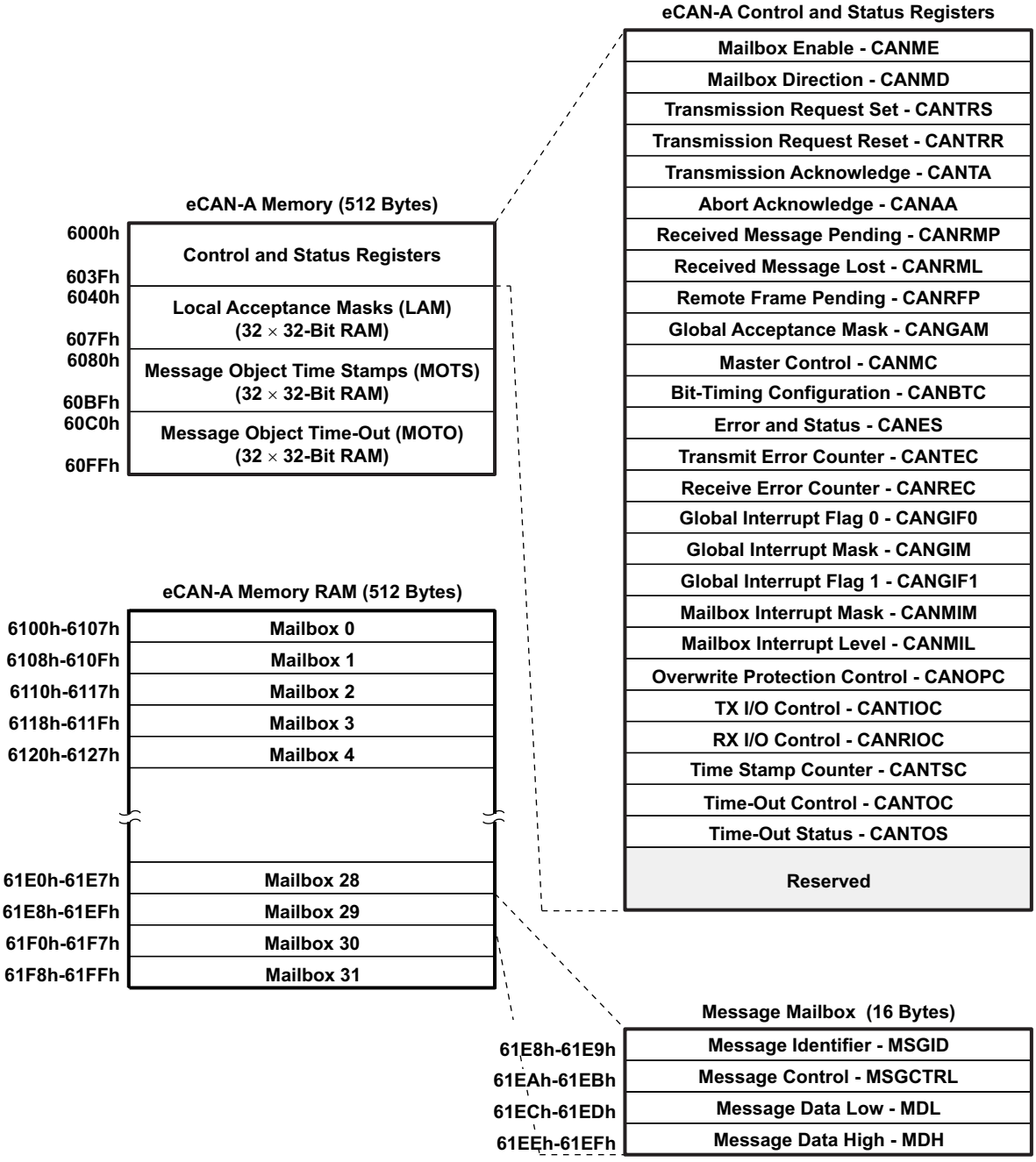


Figure 5-33. eCAN-A Memory Map

NOTE

If the eCAN module is not used in an application, the RAM available (LAM, MOTS, MOTO, and mailbox RAM) can be used as general-purpose RAM. The CAN module clock should be enabled for this.

The CAN registers listed in Table 5-42 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 5-42. CAN Register Map(1)

REGISTER NAME	eCAN-A ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x6000	1	Mailbox enable
CANMD	0x6002	1	Mailbox direction
CANTRS	0x6004	1	Transmit request set
CANTRR	0x6006	1	Transmit request reset
CANTA	0x6008	1	Transmission acknowledge
CANAA	0x600A	1	Abort acknowledge
CANRMP	0x600C	1	Receive message pending
CANRML	0x600E	1	Receive message lost
CANRFP	0x6010	1	Remote frame pending
CANGAM	0x6012	1	Global acceptance mask
CANMC	0x6014	1	Master control
CANBTC	0x6016	1	Bit-timing configuration
CANES	0x6018	1	Error and status
CANTEC	0x601A	1	Transmit error counter
CANREC	0x601C	1	Receive error counter
CANGIF0	0x601E	1	Global interrupt flag 0
CANGIM	0x6020	1	Global interrupt mask
CANGIF1	0x6022	1	Global interrupt flag 1
CANMIM	0x6024	1	Mailbox interrupt mask
CANMIL	0x6026	1	Mailbox interrupt level
CANOPC	0x6028	1	Overwrite protection control
CANTIOC	0x602A	1	TX I/O control
CANRIOC	0x602C	1	RX I/O control
CANTSC	0x602E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x6030	1	Time-out control (Reserved in SCC mode)
CANTOS	0x6032	1	Time-out status (Reserved in SCC mode)

(1) These registers are mapped to Peripheral Frame 1.

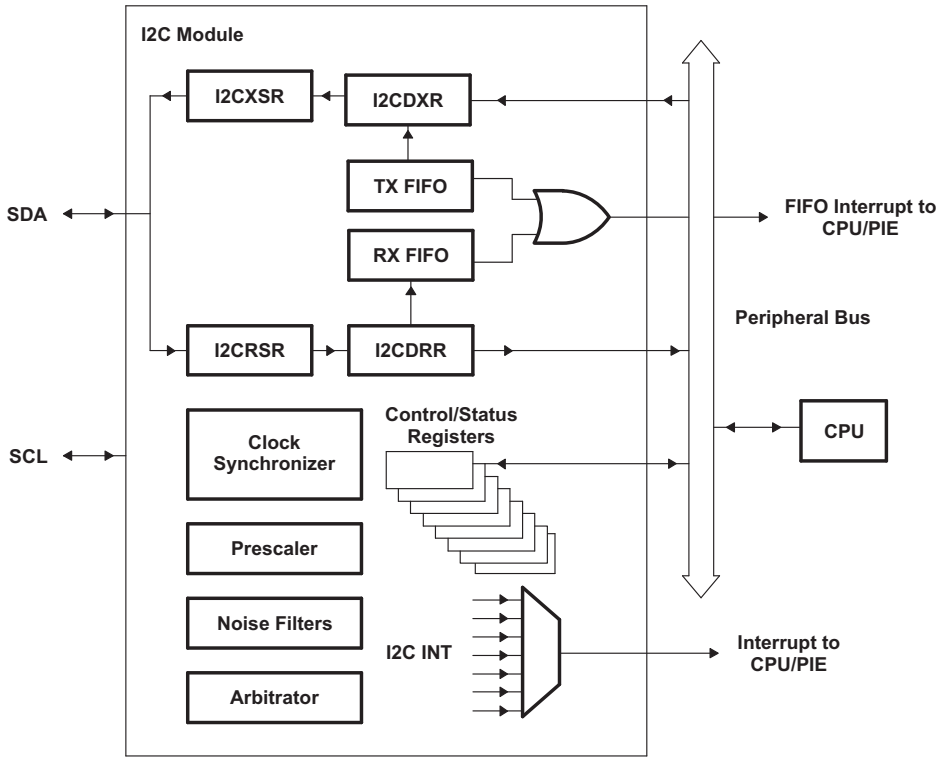
5.9.8 Inter-Integrated Circuit (I2C)

The device contains one I2C Serial Port. Figure 5-34 shows how the I2C peripheral module interfaces within the device.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

For more information on the I2C, see the *TMS320x2802x, 2803x Piccolo Inter-Integrated Circuit (I2C) Module Reference Guide*.



A. The I2C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I2C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low-power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 5-34. I2C Peripheral Module Interfaces

The registers in Table 5-43 configure and control the I2C port operation.

Table 5-43. I2C-A Registers

NAME	ADDRESS	EALLOW PROTECTED	DESCRIPTION
I2COAR	0x7900	No	I2C own address register
I2CIER	0x7901	No	I2C interrupt enable register
I2CSTR	0x7902	No	I2C status register
I2CCLKL	0x7903	No	I2C clock low-time divider register
I2CCLKH	0x7904	No	I2C clock high-time divider register
I2CCNT	0x7905	No	I2C data count register
I2CDRR	0x7906	No	I2C data receive register
I2CSAR	0x7907	No	I2C slave address register
I2CDXR	0x7908	No	I2C data transmit register
I2CMDR	0x7909	No	I2C mode register
I2CISRC	0x790A	No	I2C interrupt source register
I2CPSC	0x790C	No	I2C prescaler register
I2CFFTX	0x7920	No	I2C FIFO transmit register
I2CFFRX	0x7921	No	I2C FIFO receive register
I2CRSR	–	No	I2C receive shift register (not accessible to the CPU)
I2CXSR	–	No	I2C transmit shift register (not accessible to the CPU)

5.9.8.1 I2C Electrical Data/Timing

Table 5-44 shows the I2C timing requirements. Table 5-45 shows the I2C switching characteristics.

Table 5-44. I2C Timing Requirements

			MIN	MAX	UNIT
$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall		0.6		µs
$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay		0.6		µs
$t_{h(SCL-DAT)}$	Hold time, data after SCL fall		0		µs
$t_{su(DAT-SCL)}$	Setup time, data before SCL rise		100		ns
$t_{r(SDA)}$	Rise time, SDA	Input tolerance	20	300	ns
$t_{r(SCL)}$	Rise time, SCL	Input tolerance	20	300	ns
$t_{f(SDA)}$	Fall time, SDA	Input tolerance	11.4	300	ns
$t_{f(SCL)}$	Fall time, SCL	Input tolerance	11.4	300	ns
$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay		0.6		µs

Table 5-45. I2C Switching Characteristics

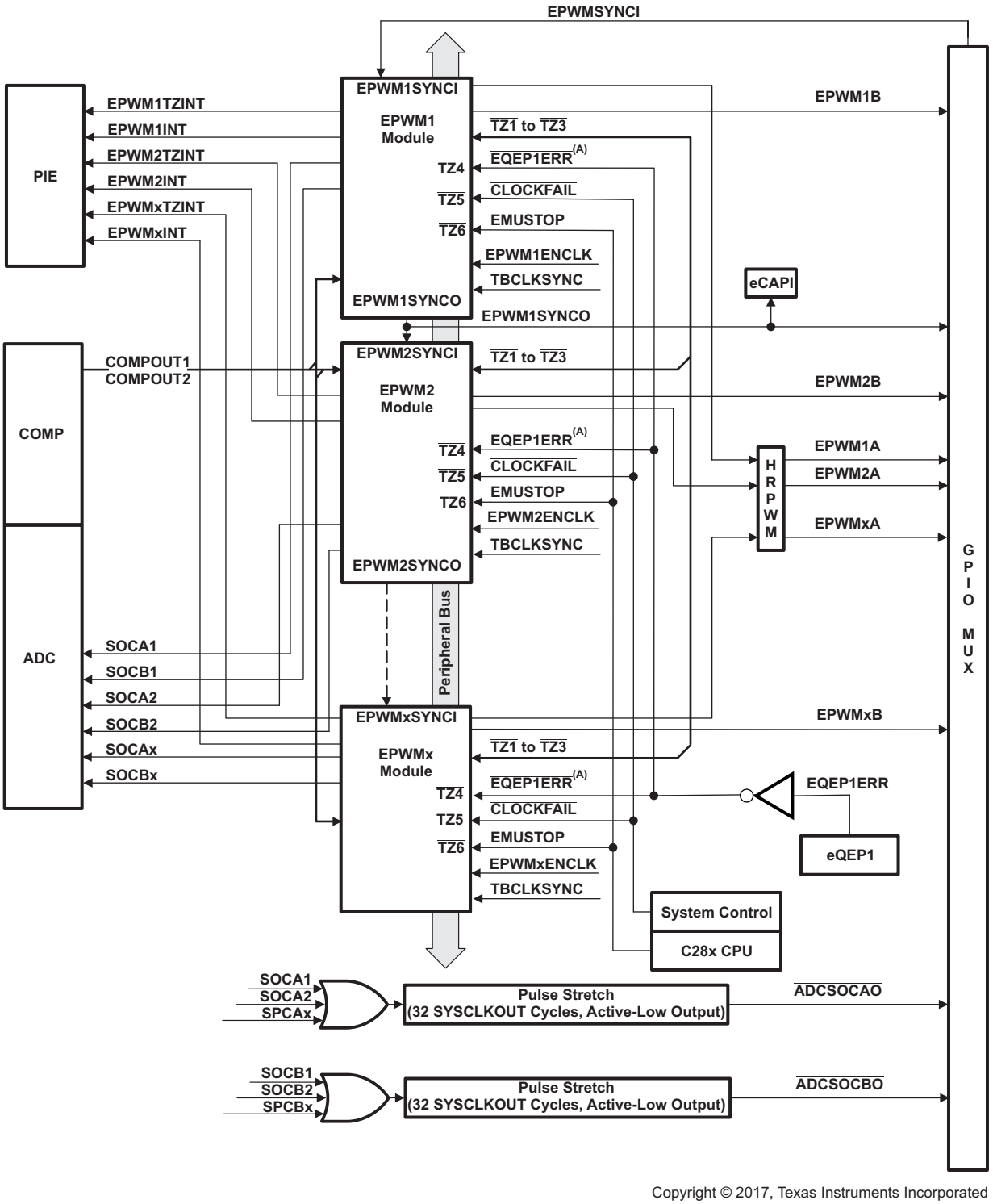
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	I2C clock module frequency is from 7 MHz to 12 MHz and I2C prescaler and clock divider registers are configured appropriately.		400	kHz
V_{il}	Low level input voltage			0.3 V_{DDIO}	V
V_{ih}	High level input voltage		0.7 V_{DDIO}		V
V_{hys}	Input hysteresis		0.05 V_{DDIO}		V
V_{ol}	Low level output voltage	3-mA sink current	0	0.4	V
t_{LOW}	Low period of SCL clock	I2C clock module frequency is from 7 MHz to 12 MHz and I2C prescaler and clock divider registers are configured appropriately.	1.3		µs
t_{HIGH}	High period of SCL clock	I2C clock module frequency is from 7 MHz to 12 MHz and I2C prescaler and clock divider registers are configured appropriately.	0.6		µs
I_I	Input current with an input voltage from 0.1 V_{DDIO} to 0.9 V_{DDIO} MAX		–10	10	µA

5.9.9 Enhanced PWM Modules (ePWM1/2/3/4/5/6/7)

The devices contain up to seven enhanced PWM Modules (ePWM). Figure 5-35 shows a block diagram of multiple ePWM modules. Figure 5-36 shows the signal interconnections with the ePWM. See the *TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* for more details.

Table 5-46 and Table 5-47 show the complete ePWM register set per module.



A. This signal exists only on devices with an eQEP1 module.

Figure 5-35. ePWM

Table 5-46. ePWM1–ePWM4 Control and Status Registers

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	1 / 0	Time Base Status Register
TBPHSHR	0x6802	0x6842	0x6882	0x68C2	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	1 / 0	Time Base Phase Register
TBCTR	0x6804	0x6844	0x6884	0x68C4	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	1 / 1	Time Base Period Register Set
TBPRDHR	0x6806	0x6846	0x6886	0x68C6	1 / 1	Time Base Period High Resolution Register(1)
CMPCTL	0x6807	0x6847	0x6887	0x68C7	1 / 0	Counter Compare Control Register
CMPAHR	0x6808	0x6848	0x6888	0x68C8	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6809	0x6849	0x6889	0x68C9	1 / 1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	1 / 0	Trip Zone Select Register(1)
TZDCSEL	0x6813	0x6853	0x6893	0x98D3	1 / 0	Trip Zone Digital Compare Register
TZCTL	0x6814	0x6854	0x6894	0x68D4	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6815	0x6855	0x6895	0x68D5	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6816	0x6856	0x6896	0x68D6	1 / 0	Trip Zone Flag Register (1)
TZCLR	0x6817	0x6857	0x6897	0x68D7	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6818	0x6858	0x6898	0x68D8	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6819	0x6859	0x6899	0x68D9	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	1 / 0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	1 / 0	PWM Chopper Control Register
HRCNFG	0x6820	0x6860	0x68A0	0x68E0	1 / 0	HRPWM Configuration Register(1)

(1) Registers that are EALLOW protected.

Table 5-46. ePWM1–ePWM4 Control and Status Registers (continued)

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (x16) / #SHADOW	DESCRIPTION
HRPWR	0x6821	-	-	-	1 / 0	HRPWM Power Register
HRMSTEP	0x6826	-	-	-	1 / 0	HRPWM MEP Step Register
HRPCTL	0x6828	0x6868	0x68A8	0x68E8	1 / 0	High resolution Period Control Register(1)
TBPRDHRM	0x682A	0x686A	0x68AA	0x68EA	1 / W(2)	Time Base Period HRPWM Register Mirror
TBPRDM	0x682B	0x686B	0x68AB	0x68EB	1 / W(2)	Time Base Period Register Mirror
CMPAHRM	0x682C	0x686C	0x68AC	0x68EC	1 / W(2)	Compare A HRPWM Register Mirror
CMPAM	0x682D	0x686D	0x68AD	0x68ED	1 / W(2)	Compare A Register Mirror
DCTRIPSEL	0x6830	0x6870	0x68B0	0x68F0	1 / 0	Digital Compare Trip Select Register (1)
DCACTL	0x6831	0x6871	0x68B1	0x68F1	1 / 0	Digital Compare A Control Register(1)
DCBCTL	0x6832	0x6872	0x68B2	0x68F2	1 / 0	Digital Compare B Control Register(1)
DCFCTL	0x6833	0x6873	0x68B3	0x68F3	1 / 0	Digital Compare Filter Control Register(1)
DCCAPCT	0x6834	0x6874	0x68B4	0x68F4	1 / 0	Digital Compare Capture Control Register(1)
DCFOFFSET	0x6835	0x6875	0x68B5	0x68F5	1 / 1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6836	0x6876	0x68B6	0x68F6	1 / 0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6837	0x6877	0x68B7	0x68F7	1 / 0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6838	0x6878	0x68B8	0x68F8	1 / 0	Digital Compare Filter Window Counter Register
DCCAP	0x6839	0x6879	0x68B9	0x68F9	1 / 1	Digital Compare Counter Capture Register

(2) W = Write to shadow register

Table 5-47. ePWM5–ePWM7 Control and Status Registers

NAME	ePWM5	ePWM6	ePWM7	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6900	0x6940	0x6980	1 / 0	Time Base Control Register
TBSTS	0x6901	0x6941	0x6981	1 / 0	Time Base Status Register
TBPHSHR	0x6902	0x6942	0x6982	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6903	0x6943	0x6983	1 / 0	Time Base Phase Register
TBCTR	0x6904	0x6944	0x6984	1 / 0	Time Base Counter Register
TBPRD	0x6905	0x6945	0x6985	1 / 1	Time Base Period Register Set
TBPRDHR	0x6906	0x6946	0x6986	1 / 1	Time Base Period High Resolution Register(1)
CMPCTL	0x6907	0x6947	0x6987	1 / 0	Counter Compare Control Register
CMPAHR	0x6908	0x6948	0x6988	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6909	0x6949	0x6989	1 / 1	Counter Compare A Register Set

(1) Registers that are EALLOW protected.

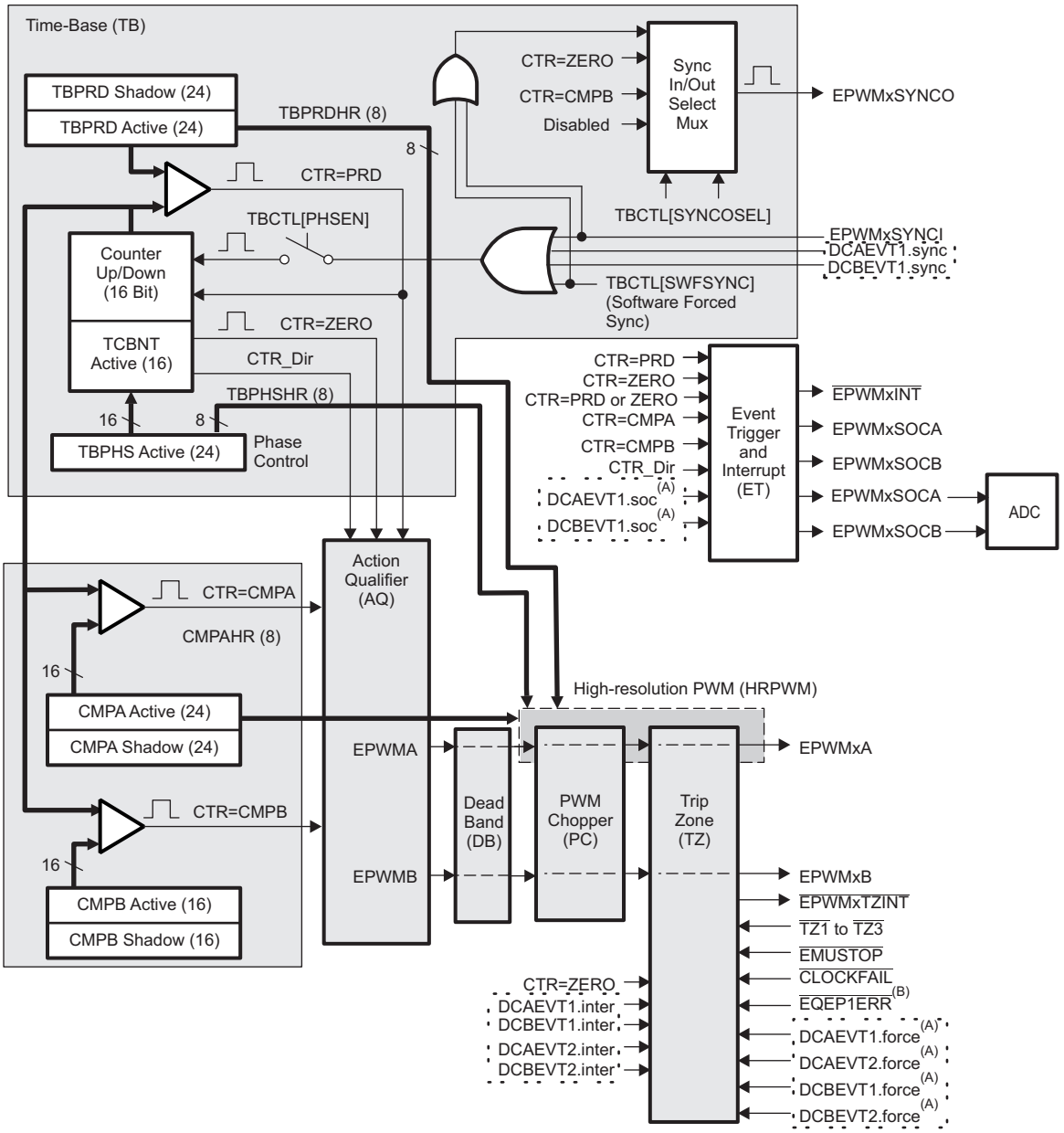
Table 5-47. ePWM5–ePWM7 Control and Status Registers (continued)

NAME	ePWM5	ePWM6	ePWM7	SIZE (x16) / #SHADOW	DESCRIPTION
CMPB	0x690A	0x694A	0x698A	1 / 1	Counter Compare B Register Set
AQCTLA	0x690B	0x694B	0x698B	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x690C	0x694C	0x698C	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x690D	0x694D	0x698D	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x690E	0x694E	0x698E	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x690F	0x694F	0x698F	1 / 1	Dead-Band Generator Control Register
DBRED	0x6910	0x6950	0x6990	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6911	0x6951	0x6991	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6912	0x6952	0x6992	1 / 0	Trip Zone Select Register(1)
TZDCSEL	0x6913	0x6953	0x6993	1 / 0	Trip Zone Digital Compare Register
TZCTL	0x6914	0x6954	0x6994	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6915	0x6955	0x6995	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6916	0x6956	0x6996	1 / 0	Trip Zone Flag Register (1)
TZCLR	0x6917	0x6957	0x6997	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6918	0x6958	0x6998	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6919	0x6959	0x6999	1 / 0	Event Trigger Selection Register
ETPS	0x691A	0x695A	0x699A	1 / 0	Event Trigger Prescale Register
ETFLG	0x691B	0x695B	0x699B	1 / 0	Event Trigger Flag Register
ETCLR	0x691C	0x695C	0x699C	1 / 0	Event Trigger Clear Register
ETFRC	0x691D	0x695D	0x699D	1 / 0	Event Trigger Force Register
PCCTL	0x691E	0x695E	0x699E	1 / 0	PWM Chopper Control Register
HRCNFG	0x6920	0x6960	0x69A0	1 / 0	HRPWM Configuration Register(1)
HRPWR	-	-	-	1 / 0	HRPWM Power Register
HRMSTEP	-	-	-	1 / 0	HRPWM MEP Step Register
HRPCTL	0x6928	0x6968	0x69A8	1 / 0	High resolution Period Control Register(1)
TBPRDHRM	0x692A	0x696A	0x69AA	1 / W(2)	Time Base Period HRPWM Register Mirror
TBPRDM	0x692B	0x696B	0x69AB	1 / W(2)	Time Base Period Register Mirror
CMPAHRM	0x692C	0x696C	0x69AC	1 / W(2)	Compare A HRPWM Register Mirror
CMPAM	0x692D	0x696D	0x69AD	1 / W(2)	Compare A Register Mirror
DCTRIPSEL	0x6930	0x6970	0x69B0	1 / 0	Digital Compare Trip Select Register (1)
DCACTL	0x6931	0x6971	0x69B1	1 / 0	Digital Compare A Control Register(1)
DCBCTL	0x6932	0x6972	0x69B2	1 / 0	Digital Compare B Control Register(1)

(2) W = Write to shadow register

Table 5-47. ePWM5–ePWM7 Control and Status Registers (continued)

NAME	ePWM5	ePWM6	ePWM7	SIZE (x16) / #SHADOW	DESCRIPTION
DCFCTL	0x6933	0x6973	0x69B3	1 / 0	Digital Compare Filter Control Register(1)
DCCAPCT	0x6934	0x6974	0x69B4	1 / 0	Digital Compare Capture Control Register(1)
DCFOFFSET	0x6935	0x6975	0x69B5	1 / 1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6936	0x6976	0x69B6	1 / 0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6937	0x6977	0x69B7	1 / 0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6938	0x6978	0x69B8	1 / 0	Digital Compare Filter Window Counter Register
DCCAP	0x6939	0x6979	0x69B9	1 / 1	Digital Compare Counter Capture Register



A. These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and $\overline{TZ}$ signals.

B. This signal exists only on devices with an eQEP1 module.

Figure 5-36. ePWM Submodules Showing Critical Internal Signal Interconnections

5.9.9.1 ePWM Electrical Data/Timing

PWM refers to PWM outputs on ePWM1–7. Table 5-48 shows the PWM timing requirements and Table 5-49, switching characteristics.

Table 5-48. ePWM Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(SYCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-64.

Table 5-49. ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

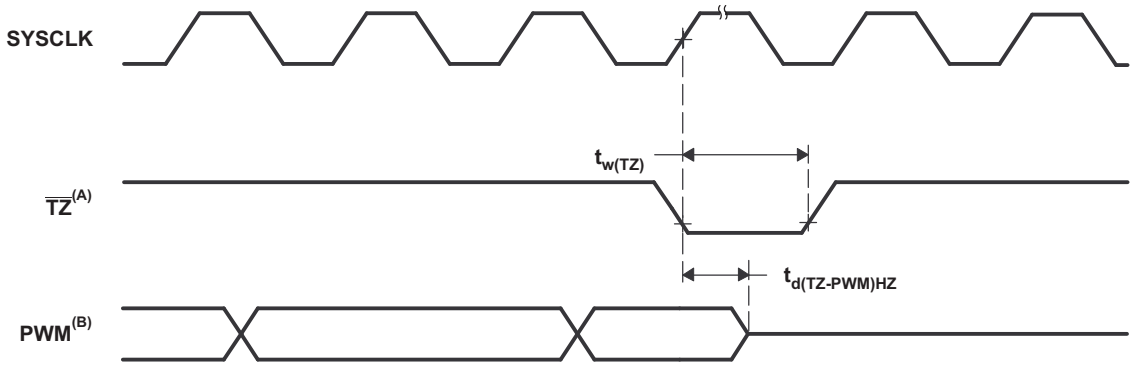
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		33.33		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

5.9.9.2 Trip-Zone Input Timing

Table 5-50. Trip-Zone Input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$2t_{c(TBCLK)}$		cycles
		Synchronous	$2t_{c(TBCLK)}$		cycles
		With input qualifier	$2t_{c(TBCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-64.



A. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, $\overline{TZ4}$, $\overline{TZ5}$, $\overline{TZ6}$

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 5-37. PWM Hi-Z Characteristics

5.9.10 High-Resolution PWM (HRPWM)

This module combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities, when available on a particular device, are offered only on the A signal path of an ePWM module (that is, on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

NOTE

The minimum SYSCLKOUT frequency allowed for HRPWM is 60 MHz.

NOTE

When dual-edge high-resolution is enabled (high-resolution period mode), the PWMxB output is not available for use.

For more information on the HRPWM, see the *TMS320x2802x, 2803x Piccolo High Resolution Pulse Width Modulator (HRPWM) Reference Guide*.

5.9.10.1 HRPWM Electrical Data/Timing

Table 5-51 shows the high-resolution PWM switching characteristics.

Table 5-51. High-Resolution PWM Characteristics(1)

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(2)		150	310	ps

(1) The HRPWM operates at a minimum SYSCLKOUT frequency of 60 MHz.
(2) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.

5.9.11 Enhanced Capture Module (eCAP1)

The device contains an enhanced capture (eCAP) module. Figure 5-38 shows a functional block diagram of a module.

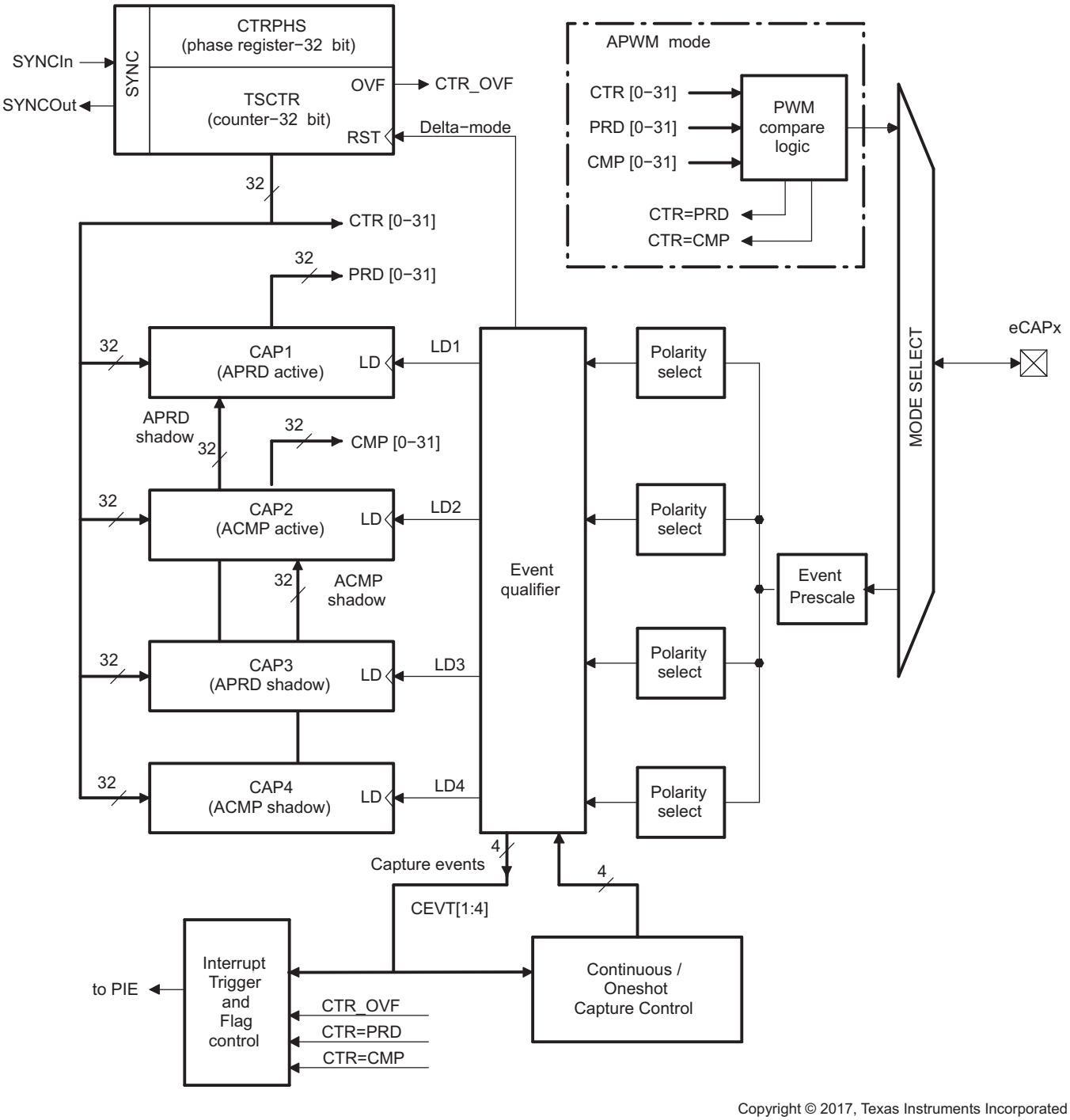


Figure 5-38. eCAP Functional Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

Table 5-52. eCAP Control and Status Registers

NAME	eCAP1	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
TSCTR	0x6A00	2		Time-Stamp Counter
CTRPHS	0x6A02	2		Counter Phase Offset Value Register
CAP1	0x6A04	2		Capture 1 Register
CAP2	0x6A06	2		Capture 2 Register
CAP3	0x6A08	2		Capture 3 Register
CAP4	0x6A0A	2		Capture 4 Register
Reserved	0x6A0C to 0x6A12	8		Reserved
ECCTL1	0x6A14	1		Capture Control Register 1
ECCTL2	0x6A15	1		Capture Control Register 2
ECEINT	0x6A16	1		Capture Interrupt Enable Register
ECFLG	0x6A17	1		Capture Interrupt Flag Register
ECCLR	0x6A18	1		Capture Interrupt Clear Register
ECFRC	0x6A19	1		Capture Interrupt Force Register
Reserved	0x6A1A to 0x6A1F	6		Reserved

For more information on the eCAP, see the *TMS320F2802x, 2803x Piccolo Enhanced Capture (eCAP) Module Reference Guide*.

5.9.11.1 eCAP Electrical Data/Timing

Table 5-53 shows the eCAP timing requirement and Table 5-54 shows the eCAP switching characteristics.

Table 5-53. Enhanced Capture (eCAP) Timing Requirement(1)

			MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-64.

Table 5-54. eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low		20		ns

5.9.12 High-Resolution Capture (HRCAP) Module

The High-Resolution Capture (HRCAP) module measures the difference between external pulses with a typical resolution of 300 ps.

Uses for the HRCAP include:

- Capactive touch applications
- High-resolution period and duty cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance/sonar measurement and scanning

The HRCAP module features include:

- Pulse width capture in either non-high-resolution or high-resolution modes
- Difference (Delta) mode pulse width capture
- Typical high-resolution capture on the order of 300 ps resolution on each edge
- Interrupt on either falling or rising edge
- Continuous mode capture of pulse widths in 2-deep buffer
- Calibration logic for precision high-resolution capture
- All of the above resources are dedicated to a single input pin
- HRCAP calibration software library supplied by TI is used for both calibration and calculating fractional pulse widths

The HRCAP module includes one capture channel in addition to a high-resolution calibration block, which connects internally to the last available ePWMxA HRPWM channel when calibrating (that is, if there are eight ePWMs with HRPWM capability, it will be HRPWM8A).

Each HRCAP channel has the following independent key resources:

- Dedicated input capture pin
- 16-bit HRCAP clock which is either equal to the PLL output frequency (asynchronous to SYSCLK) or equal to the SYSCLK frequency (synchronous to SYSCLK)
- High-resolution pulse width capture in a 2-deep buffer

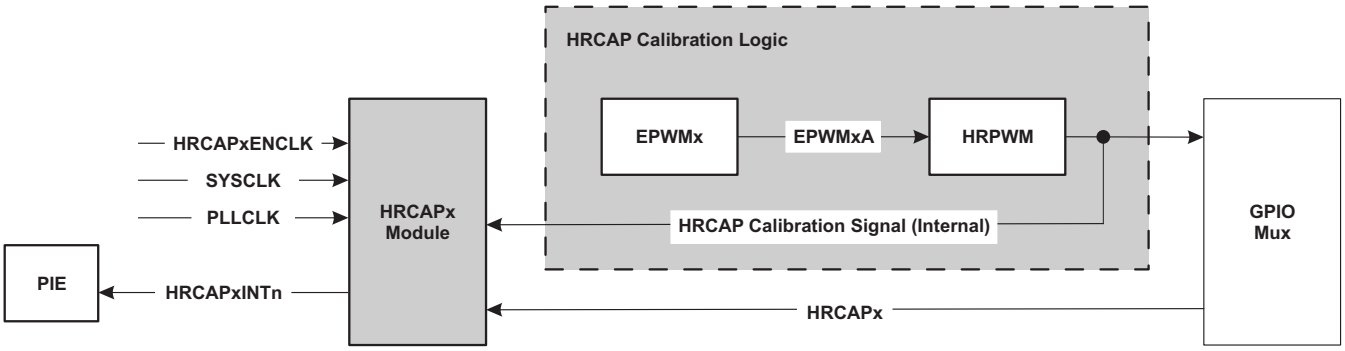


Figure 5-39. HRCAP Functional Block Diagram

Table 5-55. HRCAP Registers

NAME	HRCAP1	HRCAP2	SIZE (x16)	DESCRIPTION
HCCTL	0x6AC0	0x6AE0	1	HRCAP Control Register(1)
HCIFR	0x6AC1	0x6AE1	1	HRCAP Interrupt Flag Register
HCICLR	0x6AC2	0x6AE2	1	HRCAP Interrupt Clear Register
HCIFRC	0x6AC3	0x6AE3	1	HRCAP Interrupt Force Register
HCCOUNTER	0x6AC4	0x6AE4	1	HRCAP 16-bit Counter Register
HCCAPCNTRISE0	0x6AD0	0x6AF0	1	HRCAP Capture Counter on Rising Edge 0 Register
HCCAPCNTFALL0	0x6AD2	0x6AF2	1	HRCAP Capture Counter on Falling Edge 0 Register
HCCAPCNTRISE1	0x6AD8	0x6AF8	1	HRCAP Capture Counter on Rising Edge 1 Register
HCCAPCNTFALL1	0x6ADA	0x6AFA	1	HRCAP Capture Counter on Falling Edge 1 Register

(1) Registers that are EALLOW-protected.

For more information on the HRCAP, see the *TMS320x2803x Piccolo High Resolution Capture (HRCAP) Reference Guide*.

5.9.12.1 HRCAP Electrical Data/Timing

Table 5-56. High-Resolution Capture (HRCAP) Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{c(HCCAPCLK)}$	Cycle time, HRCAP capture clock	8.333		10.204	ns
$t_{w(HRCAP)}$	Pulse width, HRCAP capture	$7t_{c(HCCAPCLK)}$(1)			ns
	HRCAP step size(2)		300		ps

(1) The listed minimum pulse width does not take into account the limitation that all relevant HCCAP registers must be read and RISE/FALL event flags cleared within the pulse width to ensure valid capture data.
(2) HRCAP step size will increase with low voltage and high temperature and decrease with high voltage and low temperature. Applications that use the HRCAP in high-resolution mode should use the HRCAP calibration functions to dynamically calibrate for varying operating conditions.

5.9.13 Enhanced Quadrature Encoder Pulse (eQEP)

The device contains one enhanced quadrature encoder pulse (eQEP) module.

Table 5-57. eQEP Control and Status Registers

NAME	eQEP1 ADDRESS	eQEP1 SIZE(x16)/ #SHADOW	REGISTER DESCRIPTION
QPOSCNT	0x6B00	2/0	eQEP Position Counter
QPOSINIT	0x6B02	2/0	eQEP Initialization Position Count
QPOSMAX	0x6B04	2/0	eQEP Maximum Position Count
QPOSCMP	0x6B06	2/1	eQEP Position-compare
QPOSILAT	0x6B08	2/0	eQEP Index Position Latch
QPOSSLAT	0x6B0A	2/0	eQEP Strobe Position Latch
QPOSLAT	0x6B0C	2/0	eQEP Position Latch
QUTMR	0x6B0E	2/0	eQEP Unit Timer
QUPRD	0x6B10	2/0	eQEP Unit Period Register
QWDTMR	0x6B12	1/0	eQEP Watchdog Timer
QWDPRD	0x6B13	1/0	eQEP Watchdog Period Register
QDECCTL	0x6B14	1/0	eQEP Decoder Control Register
QEPCTL	0x6B15	1/0	eQEP Control Register
QCAPCTL	0x6B16	1/0	eQEP Capture Control Register
QPOSCTL	0x6B17	1/0	eQEP Position-compare Control Register
QEINT	0x6B18	1/0	eQEP Interrupt Enable Register
QFLG	0x6B19	1/0	eQEP Interrupt Flag Register
QCLR	0x6B1A	1/0	eQEP Interrupt Clear Register
QFRC	0x6B1B	1/0	eQEP Interrupt Force Register
QEPSTS	0x6B1C	1/0	eQEP Status Register
QCTMR	0x6B1D	1/0	eQEP Capture Timer
QCPRD	0x6B1E	1/0	eQEP Capture Period Register
QCTMRLAT	0x6B1F	1/0	eQEP Capture Timer Latch
QCPRDLAT	0x6B20	1/0	eQEP Capture Period Latch
Reserved	0x6B21 – 0x6B3F	31/0	

For more information on the eQEP, see the *TMS320x2803x Piccolo Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide*.

Figure 5-40 shows the eQEP functional block diagram.

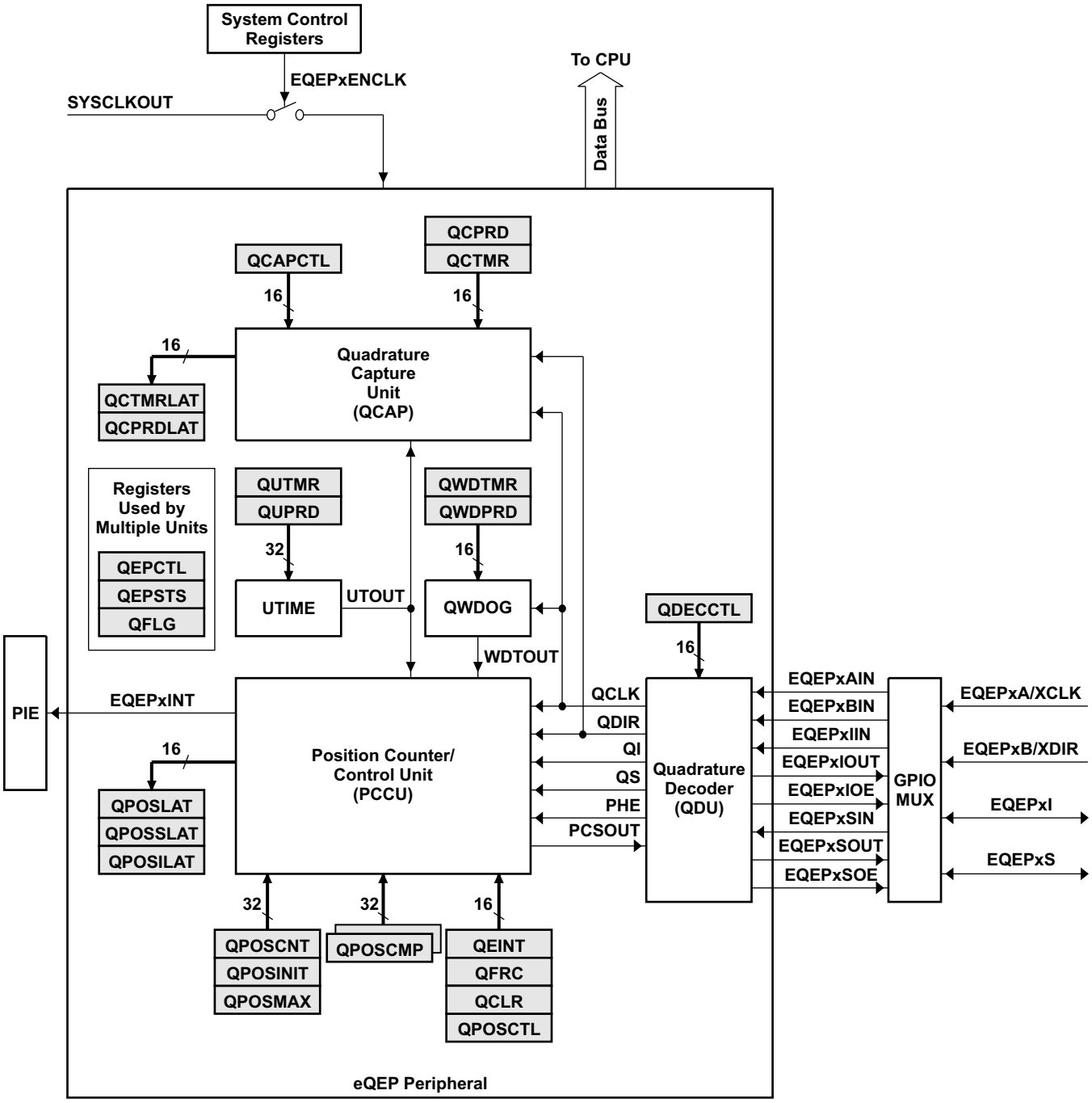


Figure 5-40. eQEP Functional Block Diagram

5.9.13.1 eQEP Electrical Data/Timing

Table 5-58 shows the eQEP timing requirement and Table 5-59 shows the eQEP switching characteristics.

Table 5-58. Enhanced Quadrature Encoder Pulse (eQEP) Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Asynchronous(2)/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2[1t_{c(SCO)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Asynchronous(2)/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Asynchronous(2)/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Asynchronous(2)/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Asynchronous(2)/synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-64.
(2) Refer to the *TMS320F2803x Piccolo™ MCUs Silicon Errata* for limitations in the asynchronous mode.

Table 5-59. eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment			$4t_{c(SCO)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output			$6t_{c(SCO)}$	cycles

5.9.14 JTAG Port

On the 2803x device, the JTAG port is reduced to 5 pins ($\overline{\text{TRST}}$, TCK, TDI, TMS, TDO). TCK, TDI, TMS and TDO pins are also GPIO pins. The $\overline{\text{TRST}}$ signal selects either JTAG or GPIO operating mode for the pins in Figure 5-41. During emulation/debug, the GPIO function of these pins are not available. If the GPIO38/TCK/XCLKIN pin is used to provide an external clock, an alternate clock source should be used to clock the device during emulation/debug because this pin will be needed for the TCK function.

NOTE

In 2803x devices, the JTAG pins may also be used as GPIO pins. Care should be taken in the board design to ensure that the circuitry connected to these pins do not affect the emulation capabilities of the JTAG pin function. Any circuitry connected to these pins should not prevent the emulator from driving (or being driven by) the JTAG pins for successful debug.

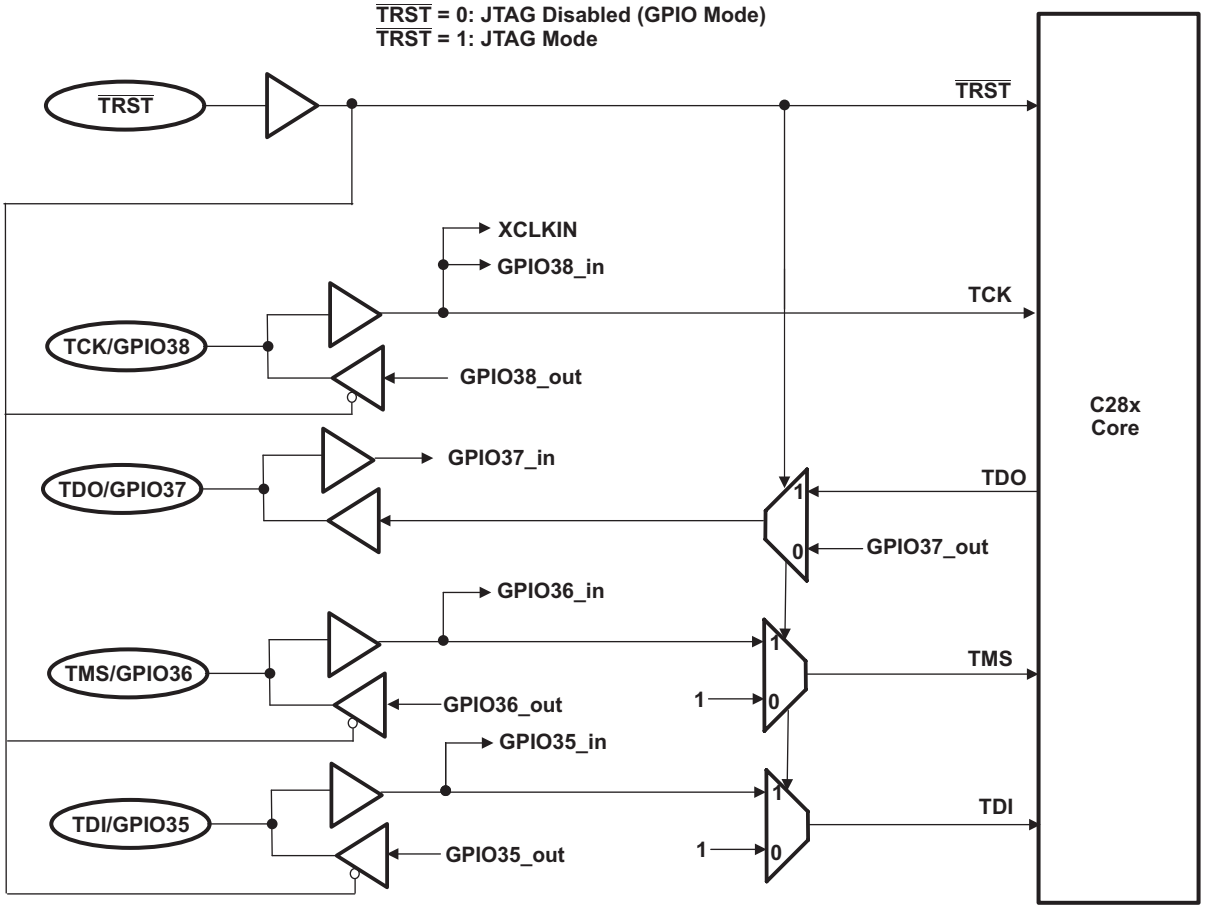


Figure 5-41. JTAG/GPIO Multiplexing

5.9.15 General-Purpose Input/Output (GPIO) MUX

The GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging I/O capability.

The device supports 45 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 5-60 shows the GPIO register mapping.

Table 5-60. GPIO Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pullup Disable Register (GPIO0 to 31)
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 44)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 44)
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 44)
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 44)
GPBPUD	0x6F9C	2	GPIO B Pullup Disable Register (GPIO32 to 44)
AIOMUX1	0x6FB6	2	Analog, I/O mux 1 register (AIO0 to AIO15)
AIODIR	0x6FBA	2	Analog, I/O Direction Register (AIO0 to AIO15)
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO A Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO A Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO A Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO A Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO B Data Register (GPIO32 to 44)
GPBSET	0x6FCA	2	GPIO B Data Set Register (GPIO32 to 44)
GPBCLEAR	0x6FCC	2	GPIO B Data Clear Register (GPIO32 to 44)
GPBTOGGLE	0x6FCE	2	GPIO B Data Toggle Register (GPIO32 to 44)
AIODAT	0x6FD8	2	Analog I/O Data Register (AIO0 to AIO15)
AIOSET	0x6FDA	2	Analog I/O Data Set Register (AIO0 to AIO15)
AIOCLEAR	0x6FDC	2	Analog I/O Data Clear Register (AIO0 to AIO15)
AIOTOGGLE	0x6FDE	2	Analog I/O Data Toggle Register (AIO0 to AIO15)
GPIO INTERRUPT AND LOW-POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT3SEL	0x6FE2	1	XINT3 GPIO Input Select Register (GPIO0 to 31)
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)

NOTE

There is a two-SYSCLKOUT cycle delay from when the write to the GPxMUXn/AIOMUXn and GPxQSELn registers occurs to when the action is valid.

Table 5-61. GPIOA MUX(1)(2)

	DEFAULT AT RESET PRIMARY I/O FUNCTION	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPAMUX1 REGISTER BITS	**(GPAMUX1 BITS = 00)**	**(GPAMUX1 BITS = 01)**	**(GPAMUX1 BITS = 10)**	**(GPAMUX1 BITS = 11)**
1-0	GPIO0	EPWM1A (O)	Reserved	Reserved
3-2	GPIO1	EPWM1B (O)	Reserved	COMP1OUT (O)
5-4	GPIO2	EPWM2A (O)	Reserved	Reserved
7-6	GPIO3	EPWM2B (O)	SPISOMIA (I/O)	COMP2OUT (O)
9-8	GPIO4	EPWM3A (O)	Reserved	Reserved
11-10	GPIO5	EPWM3B (O)	SPISIMOA (I/O)	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPIO7	EPWM4B (O)	SCIRXDA (I)	Reserved
17-16	GPIO8	EPWM5A (O)	Reserved	$\overline{\text{ADCSOCAO}}$ (O)
19-18	GPIO9	EPWM5B (O)	LINTXA (O)	HRCAP1 (I)
21-20	GPIO10	EPWM6A (O)	Reserved	$\overline{\text{ADCSOCBO}}$ (O)
23-22	GPIO11	EPWM6B (O)	LINRXA (I)	HRCAP2 (I)
25-24	GPIO12	$\overline{\text{TZ1}}$ (I)	SCITXDA (O)	SPISIMOB (I/O)
27-26	GPIO13(3)	$\overline{\text{TZ2}}$ (I)	Reserved	SPISOMIB (I/O)
29-28	GPIO14(3)	$\overline{\text{TZ3}}$ (I)	LINTXA (O)	SPICLKB (I/O)
31-30	GPIO15(3)	$\overline{\text{TZ1}}$ (I)	LINRXA (I)	$\overline{\text{SPISTEB}}$ (I/O)
GPAMUX2 REGISTER BITS	**(GPAMUX2 BITS = 00)**	**(GPAMUX2 BITS = 01)**	**(GPAMUX2 BITS = 10)**	**(GPAMUX2 BITS = 11)**
1-0	GPIO16	SPISIMOA (I/O)	Reserved	$\overline{\text{TZ2}}$ (I)
3-2	GPIO17	SPISOMIA (I/O)	Reserved	$\overline{\text{TZ3}}$ (I)
5-4	GPIO18	SPICLKA (I/O)	LINTXA (O)	XCLKOUT (O)
7-6	GPIO19/XCLKIN	$\overline{\text{SPISTEA}}$ (I/O)	LINRXA (I)	ECAP1 (I/O)
9-8	GPIO20	EQEP1A (I)	Reserved	COMP1OUT (O)
11-10	GPIO21	EQEP1B (I)	Reserved	COMP2OUT (O)
13-12	GPIO22	EQEP1S (I/O)	Reserved	LINTXA (O)
15-14	GPIO23	EQEP1I (I/O)	Reserved	LINRXA (I)
17-16	GPIO24	ECAP1 (I/O)	Reserved	SPISIMOB (I/O)
19-18	GPIO25(3)	Reserved	Reserved	SPISOMIB (I/O)
21-20	GPIO26(3)	HRCAP1 (I)	Reserved	SPICLKB (I/O)
23-22	GPIO27(3)	HRCAP2 (I)	Reserved	$\overline{\text{SPISTEB}}$ (I/O)
25-24	GPIO28	SCIRXDA (I)	SDAA (I/OD)	$\overline{\text{TZ2}}$ (I)
27-26	GPIO29	SCITXDA (O)	SCLA (I/OD)	$\overline{\text{TZ3}}$ (I)
29-28	GPIO30	CANRXA (I)	Reserved	Reserved
31-30	GPIO31	CANTXA (O)	Reserved	Reserved

(1) The word reserved means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.
(2) I = Input, O = Output, OD = Open Drain
(3) These pins are not available in the 64-pin package.

Table 5-62. GPIOB MUX(1)

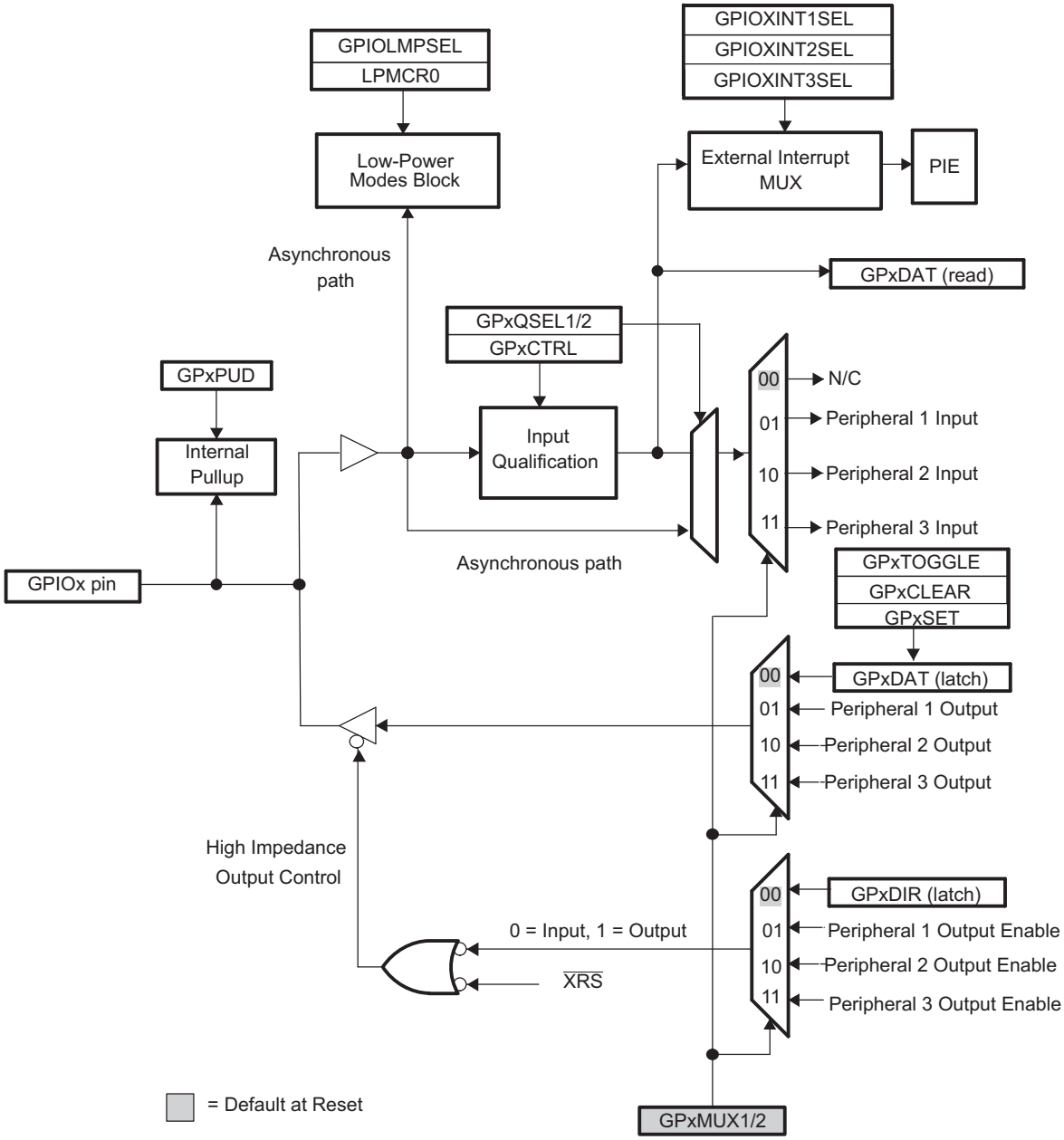
GPBMUX1 REGISTER BITS	DEFAULT AT RESET PRIMARY I/O FUNCTION (GPBMUX1 BITS = 00)	PERIPHERAL SELECTION 1 (GPBMUX1 BITS = 01)	PERIPHERAL SELECTION 2 (GPBMUX1 BITS = 10)	PERIPHERAL SELECTION 3 (GPBMUX1 BITS = 11)
1-0	GPIO32	SDAA (I/OD)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3-2	GPIO33	SCLA (I/OD)	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5-4	GPIO34	COMP2OUT (O)	Reserved	COMP3OUT (O)
7-6	GPIO35 (TDI)	Reserved	Reserved	Reserved
9-8	GPIO36 (TMS)	Reserved	Reserved	Reserved
11-10	GPIO37 (TDO)	Reserved	Reserved	Reserved
13-12	GPIO38/XCLKIN (TCK)	Reserved	Reserved	Reserved
15-14	GPIO39(2)	Reserved	Reserved	Reserved
17-16	GPIO40(2)	EPWM7A (O)	Reserved	Reserved
19-18	GPIO41(2)	EPWM7B (O)	Reserved	Reserved
21-20	GPIO42(2)	Reserved	Reserved	COMP1OUT (O)
23-22	GPIO43(2)	Reserved	Reserved	COMP2OUT (O)
25-24	GPIO44(2)	Reserved	Reserved	Reserved
27-26	Reserved	Reserved	Reserved	Reserved
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved

(1) I = Input, O = Output, OD = Open Drain
(2) These pins are not available in the 64-pin package.

The user can select the type of input qualification for each GPIO pin through the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2 = 0, 0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2 = 0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.
- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 4-18 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2 = 1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multilevel multiplexing that is required on the device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.



A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.

B. GPxDAT latch/read are accessed at the same memory location.

C. This is a generic GPIO MUX block diagram. Not all options may be applicable for all GPIO pins. See the *TMS320F2803x Piccolo System Control and Interrupts Reference Guide* for pin-specific variations.

Figure 5-42. GPIO Multiplexing

5.9.15.1 GPIO Electrical Data/Timing

5.9.15.1.1 GPIO - Output Timing

Table 5-63. General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		13(1)	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		13(1)	ns
t_{fGPO}	Toggling frequency			15	MHz

(1) Rise time and fall time vary with electrical loading on I/O pins. Values given in Table 5-63 are applicable for a 40-pF load on I/O pins.

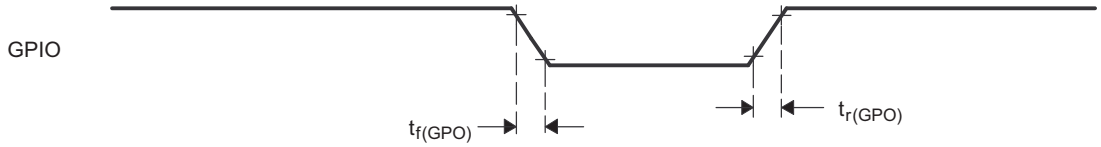


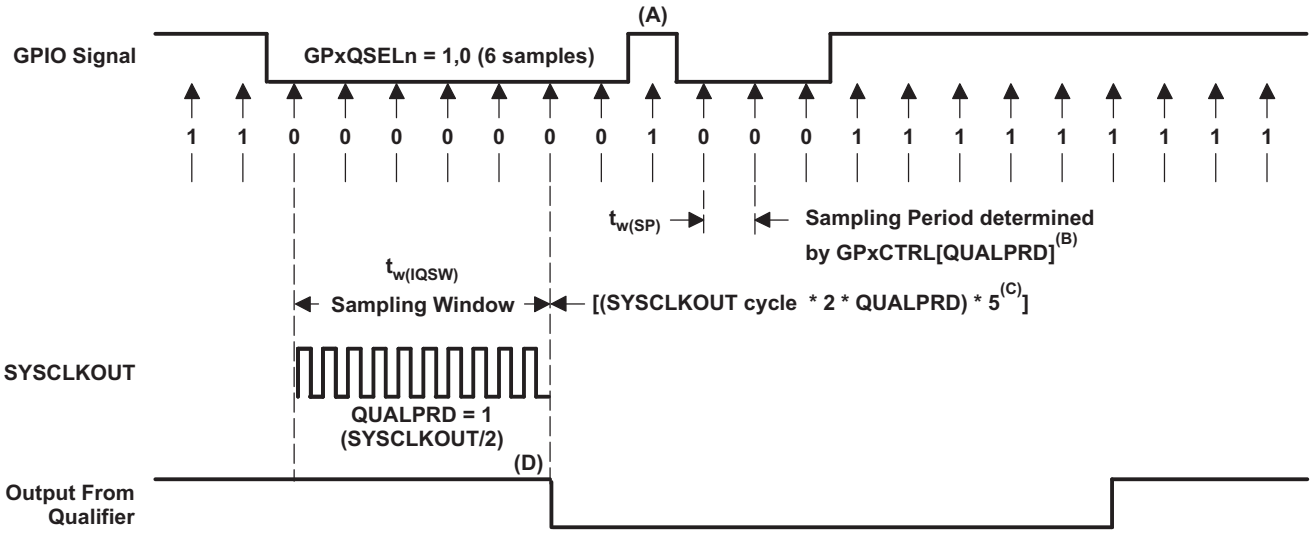
Figure 5-43. General-Purpose Output Timing

5.9.15.1.2 GPIO - Input Timing

Table 5-64. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SCO)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SCO)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SCO)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SCO)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (that is, at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).

B. The qualification period selected through the GPxCTRL register applies to groups of 8 GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLKOUT cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 5-44. Sampling Mode

5.9.15.1.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = SYSCLKOUT/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLKOUT, if QUALPRD = 0

Sampling period = SYSCLKOUT cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the above equations, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLKOUT cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLKOUT cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) × 5, if QUALPRD = 0

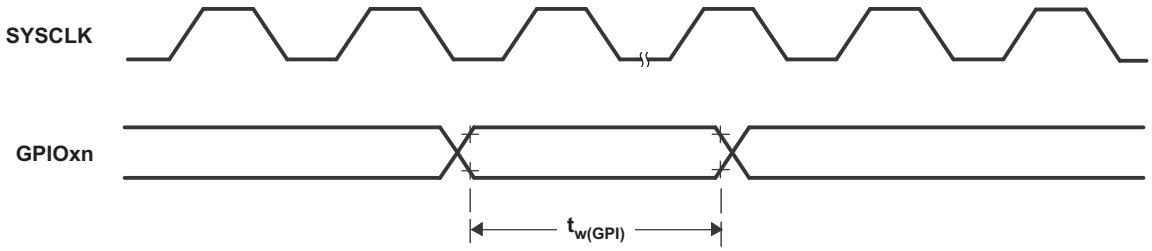


Figure 5-45. General-Purpose Input Timing

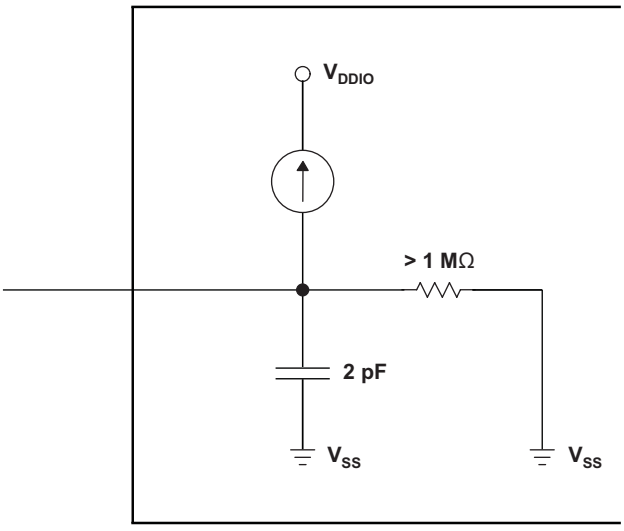


Figure 5-46. Input Resistance Model for a GPIO Pin With an Internal Pullup

5.9.15.1.4 Low-Power Mode Wakeup Timing

Table 5-65 shows the timing requirements, Table 5-66 shows the switching characteristics, and Figure 5-47 shows the timing diagram for IDLE mode.

Table 5-65. IDLE Mode Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SCO)}$		cycles
		With input qualifier	$5t_{c(SCO)} + t_{w(IQSW)}$		

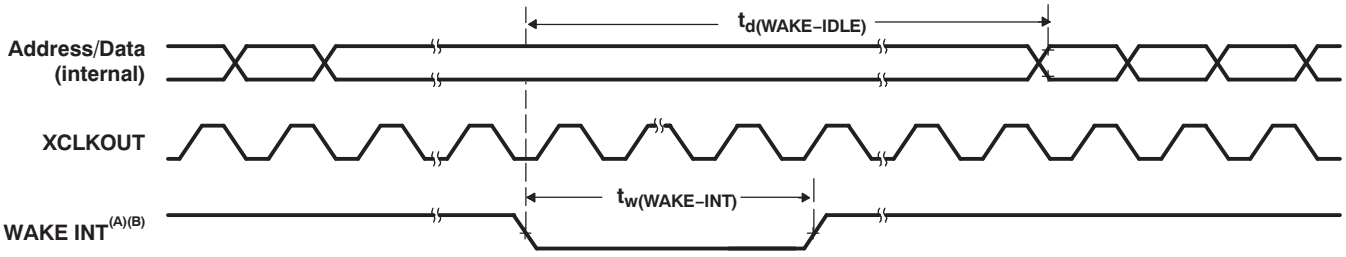
(1) For an explanation of the input qualifier parameters, see Table 5-64.

Table 5-66. IDLE Mode Switching Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)				cycles
	• Wake up from Flash – Flash module in active state	Without input qualifier		$20t_{c(SCO)}$	cycles
		With input qualifier		$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake up from Flash – Flash module in sleep state	Without input qualifier		$1050t_{c(SCO)}$	cycles
		With input qualifier		$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake up from SARAM	Without input qualifier		$20t_{c(SCO)}$	cycles
		With input qualifier		$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Table 5-64.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.



A. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$ or $\overline{\text{XRS}}$. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
B. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-47. IDLE Entry and Exit Timing

Table 5-67. STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification	$3t_{c(OSCCLK)}$		cycles
		With input qualification(1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

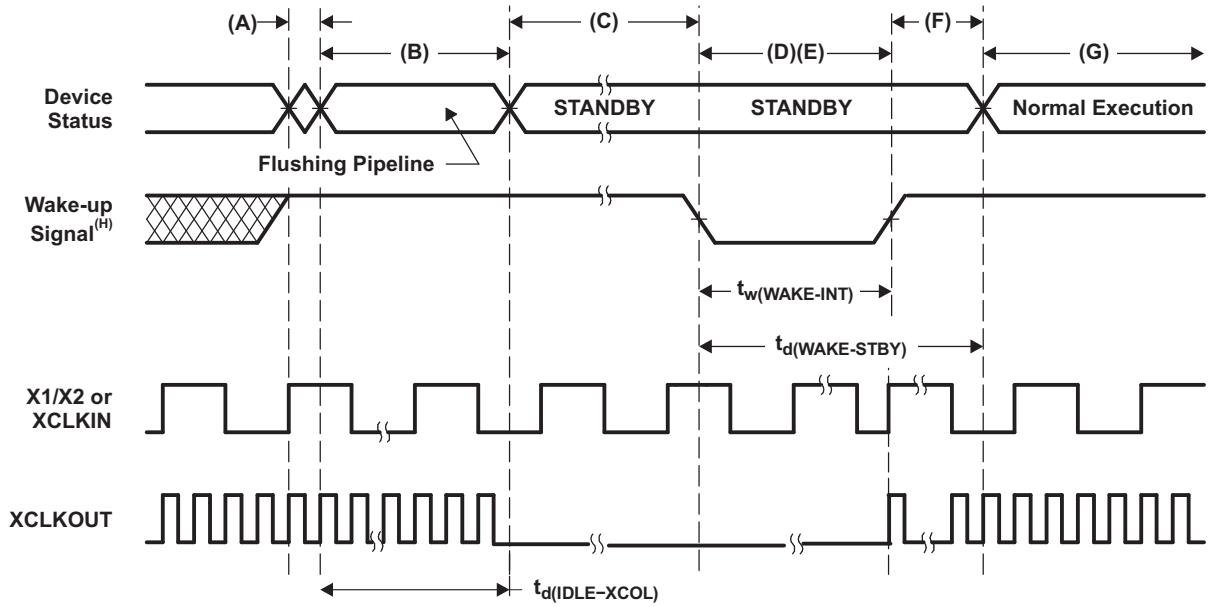
(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

Table 5-68. STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low		$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)				cycles
	• Wake up from flash – Flash module in active state	Without input qualifier		$100t_{c(SCO)}$	cycles
		With input qualifier		$100t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier		$1125t_{c(SCO)}$	cycles
		With input qualifier		$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from SARAM	Without input qualifier		$100t_{c(SCO)}$	cycles
		With input qualifier		$100t_{c(SCO)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for the number of cycles indicated below before being turned off:
   - 16 cycles, when DIVSEL = 00 or 01
   - 32 cycles, when DIVSEL = 10
   - 64 cycles, when DIVSEL = 11

   This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).
H. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-48. STANDBY Entry and Exit Timing Diagram

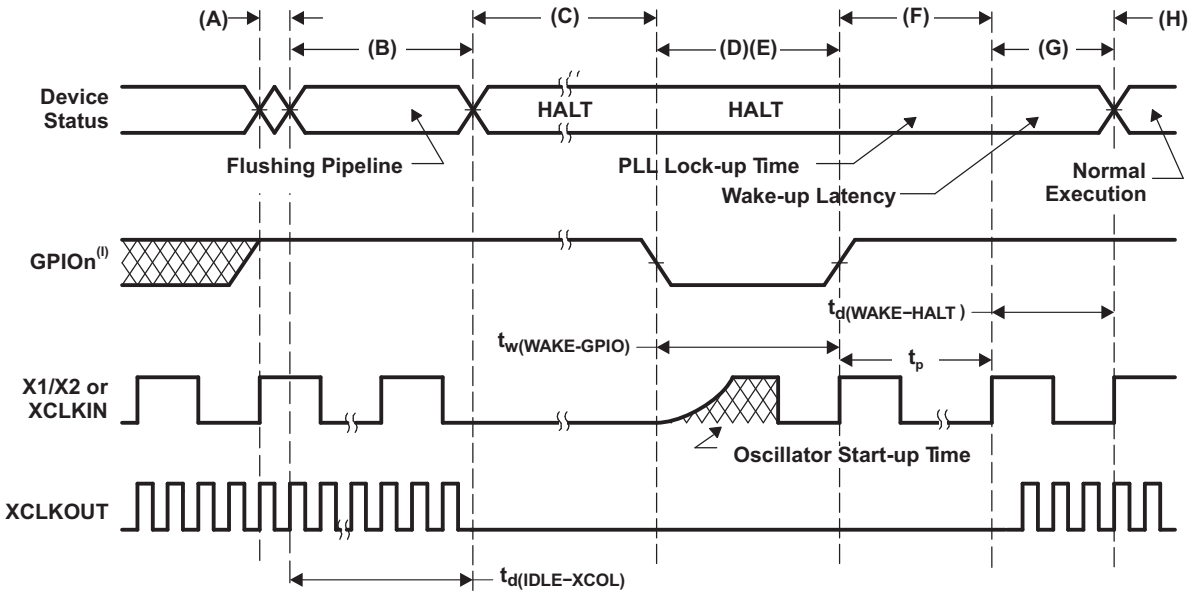
Table 5-69. HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

Table 5-70. HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low	$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
t_p	PLL lock-up time		1	ms
$t_{d(WAKE-HALT)}$	Delay time, PLL lock to program execution resume • Wake up from flash – Flash module in sleep state		$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM		$35t_{c(SCO)}$	cycles



A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for the number of cycles indicated below before oscillator is turned off and the CLKIN to the core is stopped:
   - 16 cycles, when DIVSEL = 00 or 01
   - 32 cycles, when DIVSEL = 10
   - 64 cycles, when DIVSEL = 11

   This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT mode. This is done by writing to the appropriate bits in the CLKCTL register. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.

F. Once the oscillator has stabilized, the PLL lock sequence is initiated, which takes 1 ms.

G. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.

H. Normal operation resumes.

I. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-49. HALT Mode Wakeup Using GPIOn

6 Applications, Implementation, and Layout

NOTE

Information in the following sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 TI Design or Reference Design

The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

DC Power Line Communication (PLC) Reference Design

The DC (24 V, nominal) Power-Line Communication (PLC) reference design is intended as an evaluation module that customers can use to develop end-products for industrial applications leveraging the capability to deliver both power and communications over the same DC power line. The reference design provides a complete design guide for the hardware and firmware design of a master (PLC) node, or a slave (PLC) node in an extremely small (approximately 1-inch diameter) industrial form factor.

Multiple Channels of High Density LED Control for Automotive Headlight Applications

This design, featuring the TMS320F2803x Piccolo microcontroller, implements a high-efficiency, multichannel DC-DC LED control system for typically automotive lighting systems. The design support up to six channels of LED controls, each with a maximum of 1.2-A current driving capabilities. With a 2-stage power topology of boost and buck, the system can be operated with a wide input DC voltage from 8 V to 20 V, which fits perfectly in automotive applications.

Automotive Digitally Controlled Boost Power Supply

This TI reference design is an automotive voltage boost converter module. The purpose of this module is to supply a steady voltage to vehicle electronics by boosting during voltage droop events such as engine crank. The design is based on the C2000 Real-Time Microcontroller, and will provide up to 400 W of power from a 12-V automotive battery system. This solution supports continuous operational input voltage of 6 V to 16 V with protection against 36-V load dump to provide a stable 12-V output supply with reverse battery protection.

7 器件和文档支持

7.1 使用入门

重要链接包括：

1. C2000 实时控制 MCU 使用入门
2. 电机驱动与控制
3. 数字电源
4. 用于高性能 MCU 的工具和软件

7.2 器件和开发支持工具命名规则

为了标明产品开发周期的阶段，TI 为所有 TMS320™MCU 器件和支持工具的部件号指定前缀。每个 TMS320 MCU 商用系列产品成员均具有以下三个前缀中的一个：TMX、TMP 或者 TMS（例如，**TMS**320F28032）。德州仪器 (TI) 建议为其支持的工具使用三个可能前缀指示符中的两个：TMDX 和 TMDS。这些前缀代表了产品开发的发展阶段，即从工程原型 (TMX/TMDX) 直到完全合格的生产器件/工具 (TMS/TMDS)。

器件开发进化流程：

TMX 试验器件不一定代表最终器件的电气规范标准。

TMP 最终的芯片模型符合器件的电气规范标准，但是未经完整的质量和可靠性验证。

TMS 完全合格的生产器件

支持工具开发发展流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品

TMDS 完全合格的开发支持产品

TMX 和 TMP 器件和 TMDX 开发支持工具出货时带有如下的免责声明：
“开发产品用于内部评估用途。”

TMS 器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（TMX 或者 TMP）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器建议不要将这些器件用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。这个后缀包括封装类型（例如，PN）和温度范围（如，T）。图 7-1 提供了解读任一系列产品成员完整器件名称的图例。

要获取器件部件号以及更多订购信息，请访问 TI 网站 (www.ti.com) 或者联系您的 TI 销售代表。

有关裸片器件命名规则标记的其他 说明 ，请参阅*《TMS320F2803x Piccolo™ MCU 器件勘误表》*。

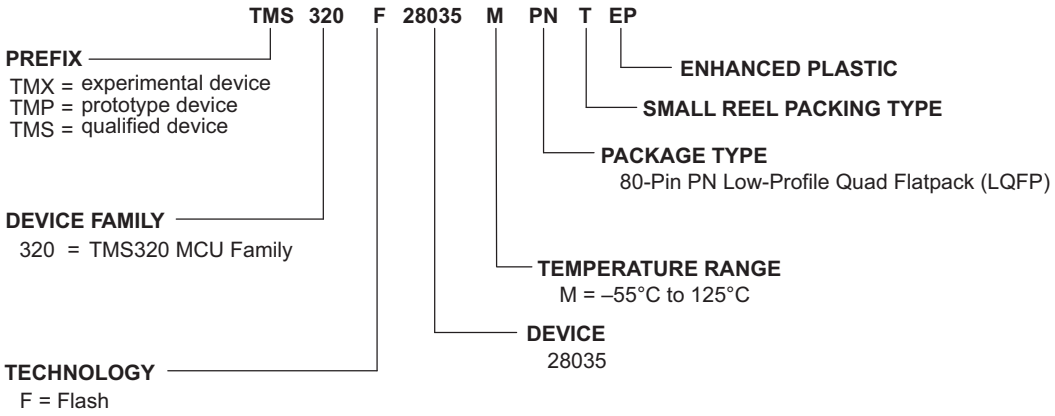


图 **7-1.** 器件命名规则

7.3 工具和软件

TI 提供大量的开发工具。下面列出了部分用于评估器件性能、生成代码和开发解决方案的工具和软件。要查看 C2000™ 实时控制 MCU 的所有可用工具和软件，请访问 C2000™ 实时控制 MCU 的工具和软件页面。

开发工具

用于 C2000 微控制器的 Code Composer Studio (CCS) 集成开发环境 (IDE)
Code Composer Studio 是支持 TI 的微控制器和嵌入式处理器产品系列的集成开发环境 (IDE)。CCS 包含一整套用于开发和调试嵌入式 应用的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种 功能。直观的 IDE 提供了单个用户界面，有助于完成应用程序开发流程的每个步骤。熟悉的工具和界面使用户能够比以前更快地入手。CCS 将 Eclipse 软件框架的优点和 TI 先进的嵌入式调试功能相结合，为嵌入式开发人员提供了一种功能丰富的优异开发环境。

软件工具

powerSUITE - 用于 C2000™ MCU 的数字电源设计软件工具
powerSUITE 是一套用于德州仪器 (TI) C2000 实时微控制器 (MCU) 系列的数字电源软件设计软件工具。电源工程师在设计基于 C2000 实时控制 MCU 的数控电源时，powerSUITE 可帮助他们大幅缩短开发时间。

模型

您可以从产品的“工具与软件”页面下载各种模型。这些模型包括 I/O 缓冲器信息规范 (IBIS) 模型和边界扫描描述 语言 (BSDL) 模型。要查看所有可用的模型，请访问“工具与软件”页面的“模型”部分，具体链接见本文档第一页的顶部。

培训

C2000™ 架构和外设
C2000 系列微控制器包含独特的新型先进外设组合以及非常强大的 C28x 内核。此视频介绍了 C2000 器件上的核心架构和每个外设。

Piccolo 控制律加速器 (CLA) 技术概述
此 C2000 Piccolo TMS320F2803x 控制律加速器 (CLA) 技术概述介绍了独立 32 位浮点数学加速器如何与 C28x 内核并行运行。

7.4 文档支持

如需接收文档更新通知，请访问 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

下面列出了介绍处理器、相关外设以及其他配套技术资料的最新文档。

勘误表

《TMS320F2803x Piccolo™ MCU 器件勘误表》介绍了器件的已知问题并提供了补救办法。

CPU 用户指南

《TMS320C28x CPU 和指令集参考指南》 介绍了 TMS320C28x 定点数字信号处理器 (DSP) 的中央处理器 (CPU) 和汇编语言指令。它还介绍了这些 DSP 上 提供 的仿真特性。

外设指南

《TMS320F2803x Piccolo 系统控制和中断参考指南》介绍了 2803x 微控制器 (MCU) 的各种中断和系统控制 特性 。

《C2000 实时控制外设参考指南》介绍了 28x 数字信号处理器 (DSP) 的外设参考指南。

《TMS320x2803x Piccolo 引导 ROM 参考指南》介绍了引导加载程序（工厂编程的引导加载软件）的作用和 特性 并提供了代码示例。它还介绍了器件的片上引导 ROM 的其它内容，并标识了所有信息在该存储器内的位置。

《TMS320x2802x、2803x Piccolo 模数转换器 (ADC) 和比较器参考指南》介绍了如何配置和使用片上 ADC 模块，此模块是一种 12 位管线型 ADC。

《TMS320x2802x、2803x Piccolo 增强型脉宽调制器 (ePWM) 模块参考指南》介绍了增强型脉宽调制器的主要应用领域，包括数字电机控制、开关模式电源控制、UPS（不间断电源）和其它形式的电力转换。

《TMS320x2802x、2803x Piccolo 高分辨率脉宽调制器 (HRPWM) 参考指南》介绍了脉宽调制器 (HRPWM) 的高分辨率扩展件的操作。

《TMS320x2802x、2803x Piccolo 串行通信接口 (SCI) 参考指南》介绍了如何使用 SCI。

《TMS320F2802x、2803x Piccolo 增强型捕捉 (eCAP) 模块参考指南》介绍了增强型捕捉模块。它包含模块 说明 和寄存器。

《TMS320x2802x、2803x Piccolo 串行外设接口 (SPI) 参考指南》介绍了 SPI，这是一种高速同步串行输入/输出 (I/O) 端口，允许按照已编程的位传输速率将具有编程长度（1 到 16 位）的串行比特流移入或移出器件。

《TMS320x2802x、2803x Piccolo 内部集成电路 (I2C) 模块参考指南》介绍了内部集成电路 (I2C) 模块的特性 与操作。

《TMS320x2803x Piccolo 控制律加速器 (CLA) 参考指南》介绍了控制律加速器 (CLA) 的操作。

《TMS320F2803x Piccolo 本地互联网络 (LIN) 模块用户指南》介绍了本地互联网络 (LIN) 模块的操作。

《TMS320x2803x Piccolo 增强型正交编码器脉冲 (eQEP) 参考指南》介绍了增强型正交编码器脉冲 (eQEP) 的操作。

《TMS320x2803x Piccolo 增强型控制器局域网 (eCAN) 参考指南》介绍了增强型控制器局域网 (eCAN) 的操作。

《TMS320x2803x Piccolo 高分辨率捕捉 (HRCAP) 用户指南》介绍了高分辨率捕捉 (HRCAP) 模块的操作。

工具指南

《TMS320C28x 汇编语言工具 v17.9.0.STS 用户指南》介绍了用于 TMS320C28x 器件的汇编语言工具（用于开发汇编语言代码的汇编器和其他工具）、汇编器指令、宏、通用目标文件格式和符号调试指令。

《TMS320C28x 优化 C/C++ 编译器 v17.9.0.STS 用户指南》介绍了 TMS320C28x C/C++ 编译器。此编译器接受 ANSI 标准 C/C++ 源代码，并为 TMS320C28x 器件生成 TMS320 DSP 汇编语言源代码。

《TMS320C28x 指令集仿真器技术概述》 介绍了用于 TMS320C2000 IDE 的 Code Composer Studio 内提供的仿真器，该仿真器可以对 C28x 内核的指令集进行仿真。

应用报告

《半导体封装方法》 介绍了准备向最终用户运输半导体器件时所用的封装方法。

《计算嵌入式处理器的有效使用寿命》 介绍了如何计算 TI 嵌入式处理器 (EP) 在电子系统中运行时的有效使用寿命。本文档的目标读者为希望确定 TI EP 的可靠性是否符合终端系统可靠性要求的总工程师。

《半导体和 IC 封装热指标》介绍了传统和全新的热指标，并将它们应用于系统级结温估算方面。

《振荡器补偿指南》介绍了一种为 Piccolo 内部振荡器补偿温度引起的频率漂移的工厂方法。

《使用片上零引脚振荡器的 Piccolo MCU CAN 模块操作》。
TMS320C2803x/TMS320F2806x 系列微控制器配有需要外部补偿的片上零引脚振荡器。此应用报告介绍了如何使用具有此振荡器的 CAN 模块，才能使其在最大位速率和总线长度下运行，且无需承担因使用外部时钟源而增加的成本。

《IBIS（I/O 缓冲器信息规范）建模简介》讨论了 IBIS 的各个方面，包括其历史、优势、兼容性、模型生成流程、输入/输出结构建模中的数据要求以及未来趋势。

7.5 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 为了促进工程师之间的合作，我们创建了 TI 工程师对工程师 (E2E) 社区。在 e2e.ti.com 中，您可以提问、分享知识、拓展思路并与同行工程师一道帮助解决问题。

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.6 商标

Piccolo, controlSUITE, TMS320C2000, TMS320, E2E are trademarks of Texas Instruments.
I^2C-bus is a registered trademark of NXP B.V. Corporation.
All other trademarks are the property of their respective owners.

7.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.8 术语表

TI 术语表 这份术语表列出并解释术语、缩写和定义。

8 机械、封装和可订购信息

8.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

对于具有散热焊盘的封装，“机械数据”图显示了通用散热焊盘（无尺寸）。有关适用于该器件的实际散热焊盘尺寸，请参阅“散热焊盘机械数据”图。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28035MPNTEP	ACTIVE	LQFP	PN	80	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	F28035PNMEP TMS320	Samples
V62/18605-01XE	ACTIVE	LQFP	PN	80	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	F28035PNMEP TMS320	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

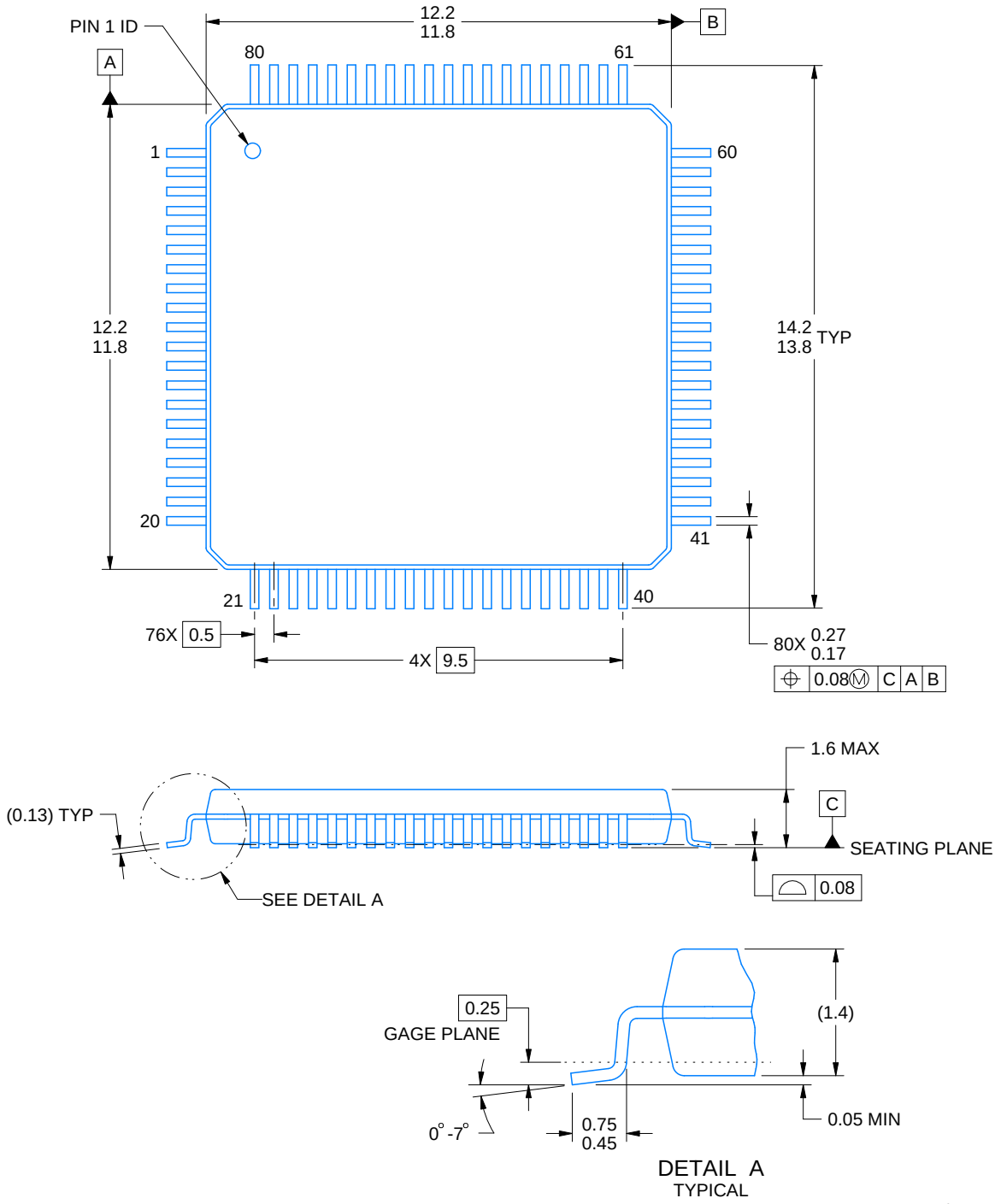
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PN0080A

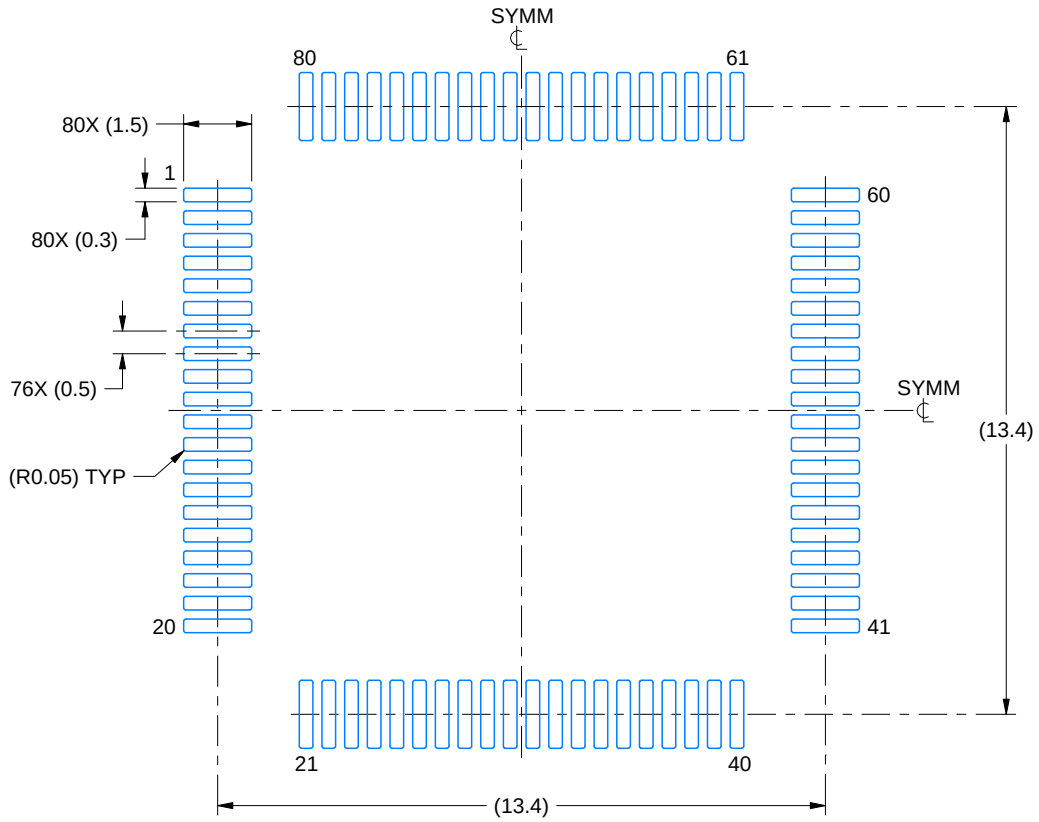
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

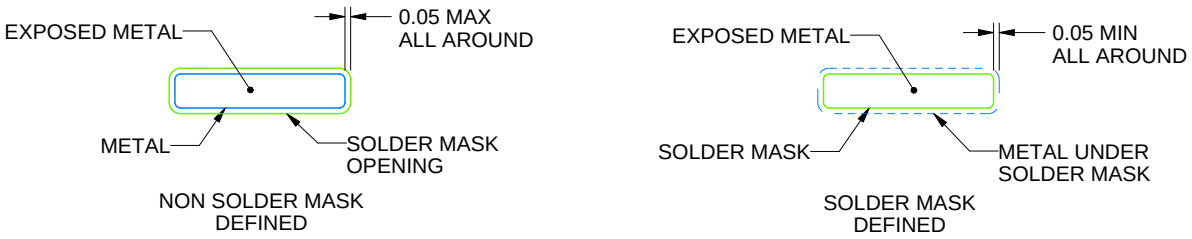


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

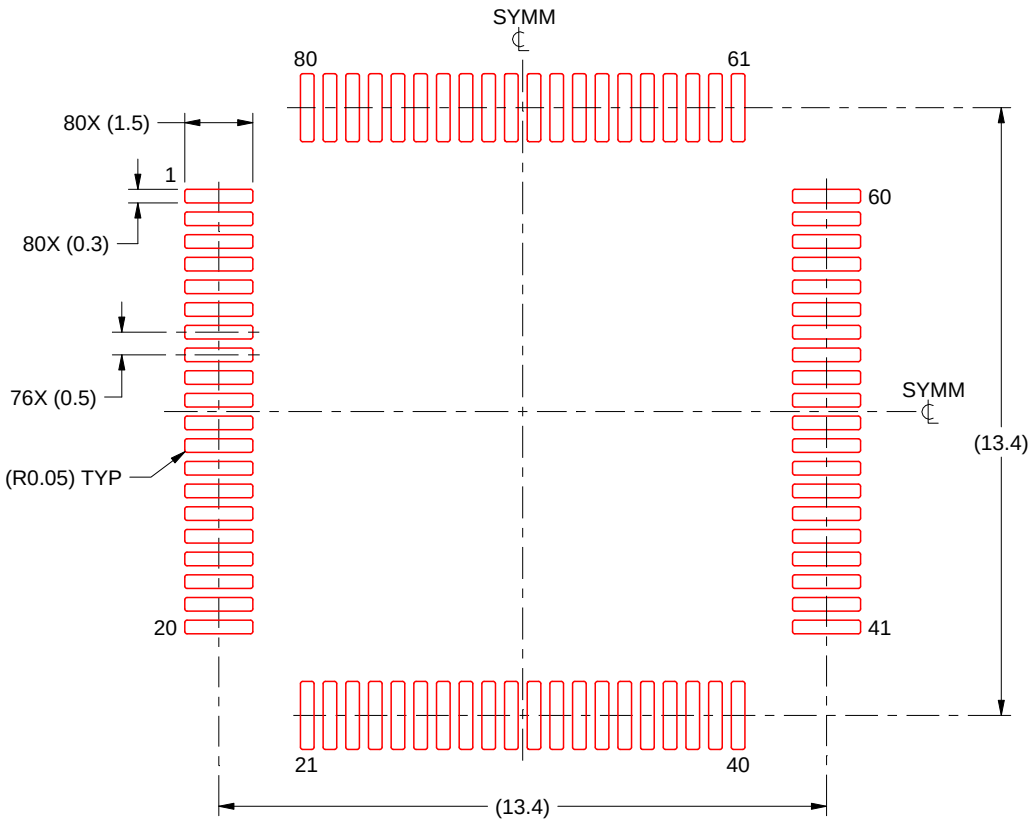


SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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