TMS320F28044 Digital Signal Processor

1 Device Overview

1.1 Features

- High-performance 100-MHz (10-ns cycle time) processor
- TMS320C28x 32-bit CPU
  - Single-cycle 16 × 16 and 32 × 32 multiply-accumulate (MAC) operations
  - Dual 16 × 16 MAC
  - Fast interrupt response
  - Unified memory programming model
- On-chip memory
  - 64K × 16 flash
  - 10K × 16 SARAM
  - 1K × 16 OTP
  - 4K × 16 Boot ROM
  - Code Security Module protects against unauthorized memory access
- Clocking
  - On-chip oscillator
  - Clock-Fail-Detect mode
- Interrupts
  - Support for up to three external core interrupts
  - Peripheral Interrupt Expansion (PIE) block that supports all peripheral interrupts
- High-speed, 12-bit ADC
  - 80-ns (12.5-MSPS) conversion rate
  - 16 channels
  - Two sample-and-hold
  - Single/simultaneous conversions
  - Internal or external reference
- High-resolution PWM
  - 16 outputs with 150-ps resolution
  - 14.8 bits at 200-kHz switching
  - 13.4 bits at 500-kHz switching
  - 12.4 bits at 1-MHz switching
- Endianness: Little endian
- Communications port peripherals
  - Serial Peripheral Interface (SPI) module
  - Serial Communications Interface (SCI)
  - Inter-Integrated Circuit (I2C) bus
- Timers
  - Three 32-bit CPU timers
  - Up to 16 16-bit timers
  - Watchdog Timer module
- Up to 35 General-Purpose Input/Output (GPIO) pins with input filtering
- On-chip JTAG emulation with real-time debug via hardware
- JTAG boundary scan support
  - IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- Low-power IDLE, STANDBY, and HALT modes
- Development tools
  - Code Composer Studio™ IDE with flash programming plug-in
  - C28x-optimized ANSI C/C++ compiler/assembler/linker
  - SYS/BIOS real-time operating system
  - USB-based JTAG debug probes
    - IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- Available Software
  - C2000™ Digital Power Supply Software Library
  - C28x IQ Math Library
  - C28x header files with example programs for all peripherals
  - C28x DSP Library
  - C28x Digital Motor Control Software Library
- Package options
  - 100-pin Low-Profile Quad Flatpack (PZ)
  - 100-pin MicroStar BGA™ (GGM, ZGM)
  - RoHS-compliant, Green packaging
- Temperature range:
  A: –40°C to 85°C (PZ, GGM, ZGM)

1.2 Applications

- String inverter
- Industrial AC-DC
- Three phase UPS

1.3 Description

The TMS320F28044 device, member of the TMS320C28x DSP generation, is a highly integrated, high-performance solution for demanding control applications.

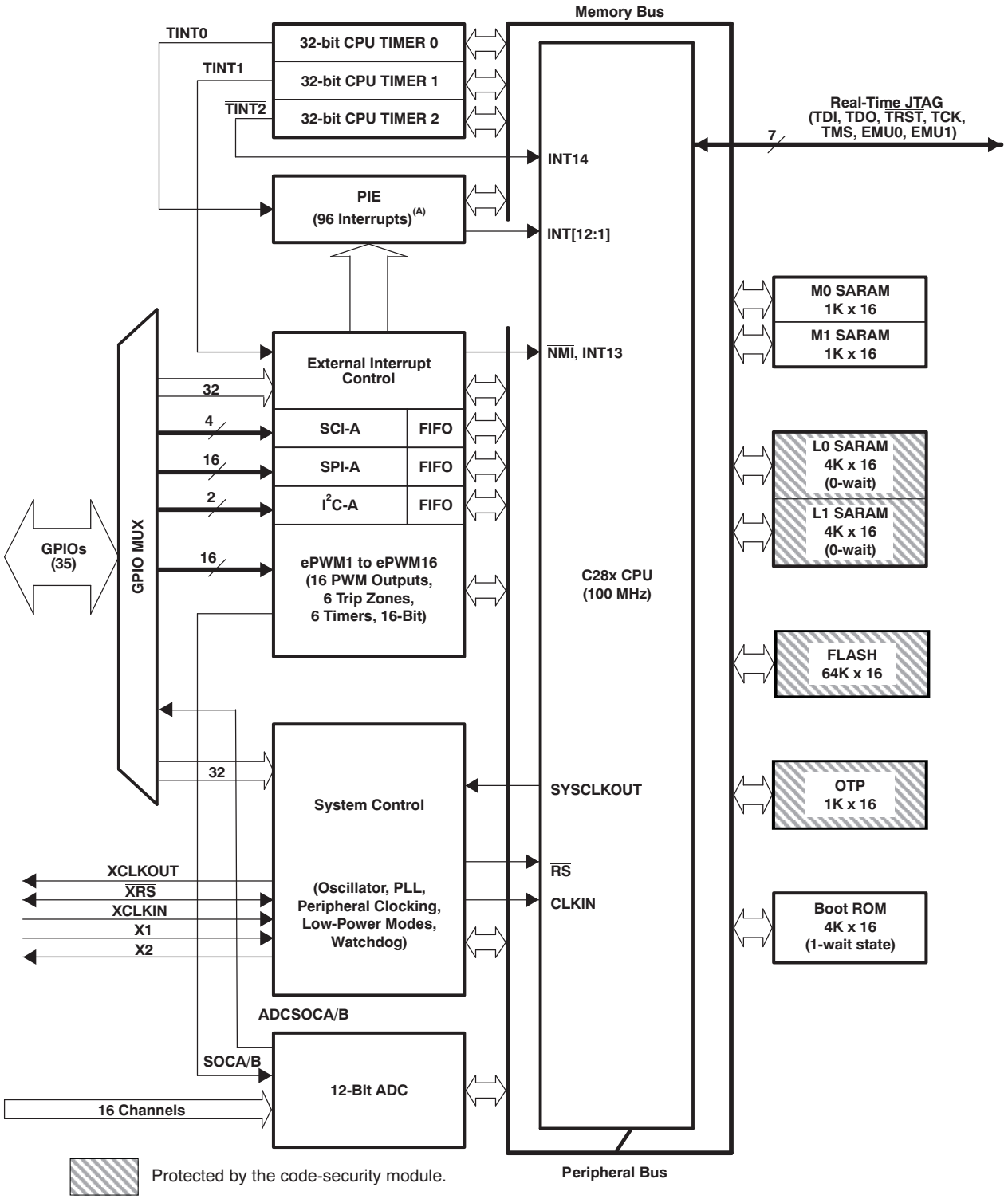
Throughout this document, TMS320F28044 is abbreviated as F28044.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TMS320F28044ZGM	BGA MicroStar (100)	10.0 mm × 10.0 mm
TMS320F28044GGM	BGA MicroStar (100)	10.0 mm × 10.0 mm
TMS320F28044PZ	LQFP (100)	14.0 mm × 14.0 mm

(1) For more information on these devices, see Mechanical, Packaging, and Orderable Information.

1.4 Functional Block Diagram



A. 43 of the possible 96 interrupts are used on the devices.

Figure 1-1. Functional Block Diagram

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2 Revision History

Changes from January 18, 2010 to June 4, 2020 (from C Revision (January 2010) to D Revision) **Page**

- **Global:** Restructured document. 1
- **Global:** Replaced "DSP/BIOS" with "SYS/BIOS". 1
- **Global:** Replaced "emulator" with "JTAG debug probe". 1
- Section 1 (Device Overview): Changed section title from "F28044 Digital Signal Processor" to "Device Overview". 1
- Section 1.1 (Features): Removed "Dynamic PLL Ratio Changes Supported" feature. 1
- Section 1.1: Added "Endianness: Little Endian" feature. 1
- Section 1.1: Removed "F28044 eZdsp Starter Kit" feature. 1
- Section 1.2 (Applications): Added section. 1
- Section 1.3 (Description): Added section. 2
- Section 1.4 (Functional Block Diagram): Added section. 3
- Section 3 (Device Comparison): Changed section title from "Introduction" to "Device Comparison". 7
- Table 3-1 (Device Comparison): Changed table title from "Hardware Features" to "Device Comparison". 7
- Table 3-1: Removed "Product status" row. 7
- Table 3-1: Changed "PWM outputs" to "PWM channels". 7
- Section 3.1 (Related Products): Added section. 7
- Section 4 (Terminal Configuration and Functions): Added section. 8
- Table 4-1 (Signal Descriptions): Updated DESCRIPTION of $\overline{\text{XRS}}$. 10
- Section 5 (Specifications): Changed section title from "Electrical Specifications" to "Specifications". 16
- Section 5.1 (Absolute Maximum Ratings): Updated "Long-term high-temperature storage ..." footnote. 16
- Section 5.2 (ESD Ratings – Commercial): Added section. 16
- Section 5.4 (Power Consumption Summary): Changed section title from "Current Consumption" to "Power Consumption Summary". 18
- Section 5.6 (Thermal Resistance Characteristics for F28044 100-Ball GGM Package): Added section. 21
- Section 5.7 (Thermal Resistance Characteristics for F28044 100-Pin PZ Package): Added section. 21
- Section 5.8 (Thermal Design Considerations): Added section. 21
- Section 5.9 (Timing and Switching Characteristics): Added section. 22
- Section 5.9.2 (Power Sequencing): Updated section.. 24
- Figure 5-8 (General-Purpose Input Timing): Changed XCLKOUT to SYSCLK. 32
- Figure 5-12 (PWM Hi-Z Characteristics): Changed XCLKOUT to SYSCLK. 37
- Section 5.9.4.2.3 (High-Resolution PWM Timing): Added section title. 38
- Table 5-21 (High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)): Updated footnote. 38
- Section 5.9.4.2.4 (ADC Start-of-Conversion Timing): Added section title. 38
- Section 5.9.4.5 (Serial Peripheral Interface (SPI) Master Mode Timing): Updated section. 40
- Section 5.9.4.6 (SPI Slave Mode Timing): Updated section. 42
- Table 5-31 (Flash Parameters at 100-MHz SYSCLKOUT): Added footnote about the on-chip flash memory being in an erase state when the device is shipped from TI. 45
- Table 5-31: Updated footnote about typical parameters. 45
- Table 5-33 (Flash Data Retention Duration): Added table. 45
- Section 6 (Detailed Description): Changed the section title from "Functional Overview" to "Detailed Description". 53
- Section 6.2.4 (Enhanced Analog-to-Digital Converter (ADC) Module): Updated equations by which the digital value of the input analog voltage is derived. 68
- Section 6.2.4.2 (ADC Registers): Added section title. 72
- Figure 6-8 (Serial Communications Interface (SCI) Module Block Diagram): Updated figure. 75
- Section 6.2.6 (Serial Peripheral Interface (SPI) Module (SPI-A)): Updated "Rising edge with phase delay" clocking scheme. 76
- Section 6.3 (Memory Map): Added NOTE about security. 85
- Table 6-14 (Impact of Using the Code Security Module): Added table. 86
- Figure 6-21 (Watchdog Module): Updated figure. 101
- Section 7 (Applications, Implementation, and Layout): Added section. 103
- Section 8 (Device and Documentation Support): Changed section title from "Device Support" to "Device and Documentation Support". Restructured and updated section. 104
- Section 8.1 (Getting Started): Updated section. 104
- Figure 8-1 (Device Nomenclature): Changed title from "Example of TMS320x280x Device Nomenclature" to "Device Nomenclature". Updated TEMPERATURE RANGE. 106
- Section 8.3 (Tools and Software): Added section. 107

- Section 8.4 (Documentation Support): Updated section. 109
- Section 9 (Mechanical, Packaging, and Orderable Information): Changed section title from "Mechanical Data" to "Mechanical, Packaging, and Orderable Information". 112
- Section 9.1 (Packaging Information): Added section. 112

3 Device Comparison

Table 3-1 provides a summary of the device's features.

Table 3-1. Device Comparison

FEATURE		TYPE(1)	F28044
Instruction cycle (at 100 MHz)		–	10 ns
Single-access RAM (SARAM) (16-bit word)		–	10K (L0, L1, M0, M1)
3.3-V on-chip flash (16-bit word)		–	64K
On-chip ROM (16-bit word)		–	–
Code security for on-chip flash/SARAM/OTP blocks		–	Yes
Boot ROM (4K × 16)		–	Yes
One-time programmable (OTP) ROM (16-bit word)		–	1K
PWM channels (one 16-bit timer/module)		0	ePWM1–16
HRPWM channels		0	ePWM1–16
Watchdog timer		–	Yes
12-Bit ADC	No. of channels	1	16
	MSPS	1	12.5
	Conversion time	1	80 ns
32-Bit CPU timers		–	3
Serial Peripheral Interface (SPI)		0	SPI-A
Serial Communications Interface (SCI)		0	SCI-A
Inter-Integrated Circuit (I^2C)		0	I^2C-A
Digital I/O pins (shared)		–	35
External interrupts		–	3
Supply voltage	1.8-V Core, 3.3-V I/O	–	Yes
Packaging	100-Pin PZ	–	Yes
	100-ball GGM, ZGM	–	Yes
Temperature options	A: –40°C to 85°C	–	(PZ, GGM, ZGM)

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the *C2000 Real-Time Control Peripherals Reference Guide* and in the peripheral reference guides.

3.1 Related Products

TMS320F2833x Microcontrollers

The F2833x series is the first C2000™ MCU that is offered with a floating-point unit (FPU). It has the first-generation ePWM timers. The 12.5-MSPS, 12-bit ADC is still class-leading for an integrated analog-to-digital converter. The F2833x has a 150-MHz CPU and up to 512KB of on-chip Flash. It is available in a 176-pin QFP or 179-ball BGA package.

TMS320F2837xD Dual-Core Microcontrollers

The F2837xD series sets a new standard for performance with dual subsystems. Each subsystem consists of a C28x CPU and a parallel control law accelerator (CLA), each running at 200 MHz. Enhancing performance are TMU and VCU accelerators. New capabilities include multiple 16-bit/12-bit mode ADCs, DAC, Sigma-Delta filters, USB, configurable logic block (CLB), on-chip oscillators, and enhanced versions of all peripherals. The F2837xD is available with up to 1MB of Flash. It is available in a 176-pin QFP or 337-pin BGA package.

TMS320F2837xS Microcontrollers

The F2837xS series is a pin-to-pin compatible version of F2837xD but with only one C28x-CPU-and-CLA subsystem enabled. It is also available in a 100-pin QFP to enable compatibility with the TMS320F2807x series.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

The TMS320F28044 100-pin PZ low-profile quad flatpack (LQFP) pin assignments are shown in Figure 4-1. The 100-ball GGM and ZGM ball grid array (BGA) terminal assignments are shown in Figure 4-2. Table 4-1 describes the function(s) of each pin.

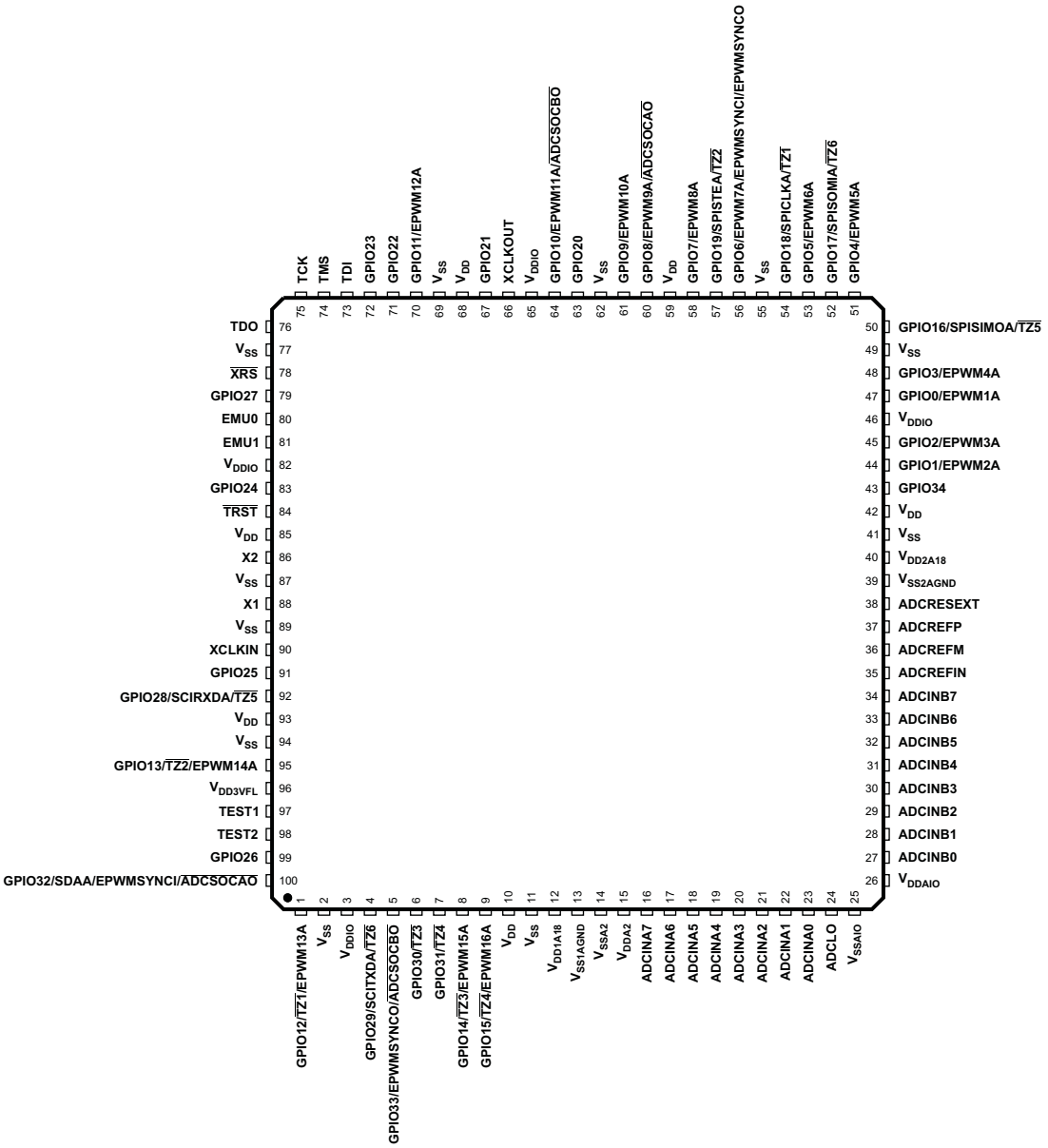

Figure 4-1. 100-Pin PZ LQFP (Top View)

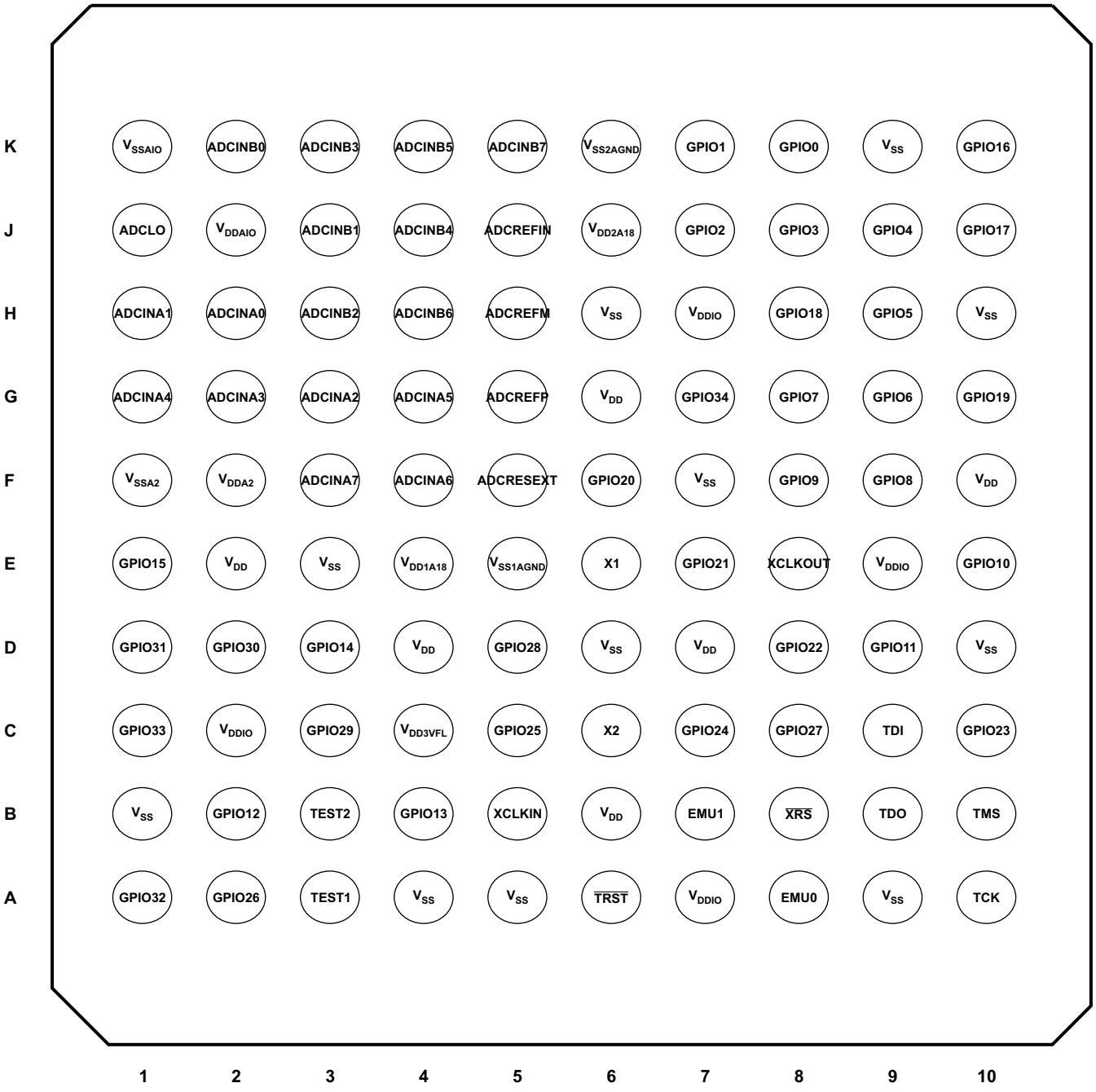

Figure 4-2. 100-Ball GGM and ZGM MicroStar BGA™ (Bottom View)

4.2 Signal Descriptions

Table 4-1 describes the signals on the F28044 device. All digital inputs are TTL-compatible. All outputs are 3.3 V with CMOS levels. Inputs are not 5-V tolerant.

Table 4-1. Signal Descriptions

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM/ ZGM BALL #	
JTAG			
$\overline{\text{TRST}}$	84	A6	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. **NOTE:** Do not use pullup resistors on $\overline{\text{TRST}}$; it has an internal pull-down device. $\overline{\text{TRST}}$ is an active high test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. (I, ↓)
TCK	75	A10	JTAG test clock with internal pullup (I, ↑)
TMS	74	B10	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (I, ↑)
TDI	73	C9	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (I, ↑)
TDO	76	B9	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (O/Z 8 mA drive)
EMU0	80	A8	Emulator pin 0. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the JTAG debug probe system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{\text{TRST}}$ pin would latch the device into boundary-scan mode. (I/O/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
EMU1	81	B7	Emulator pin 1. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the JTAG debug probe system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{\text{TRST}}$ pin would latch the device into boundary-scan mode. (I/O/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
FLASH			
V_{DD3VFL}	96	C4	3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times. On the ROM parts (C280x), this pin should be connected to V_{DDIO}.
TEST1	97	A3	Test Pin. Reserved for TI. Must be left unconnected. (I/O)
TEST2	98	B3	Test Pin. Reserved for TI. Must be left unconnected. (I/O)
CLOCK			
XCLKOUT	66	E8	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by the bits 1, 0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. Unlike other GPIO pins, the XCLKOUT pin is not placed in high-impedance state during a reset. (O/Z, 8 mA drive).
XCLKIN	90	B5	External Oscillator Input. This pin is to feed a clock from an external 3.3-V oscillator. In this case, the X1 pin must be tied to GND. If a crystal/resonator is used (or if an external 1.8-V oscillator is used to feed clock to X1 pin), this pin must be tied to GND. (I)

(1) I = Input, O = Output, Z = High impedance, OD = Open drain, ↑ = Pullup, ↓ = Pulldown

Table 4-1. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM/ ZGM BALL #	
X1	88	E6	Internal/External Oscillator Input. To use the internal oscillator, a quartz crystal or a ceramic resonator may be connected across X1 and X2. The X1 pin is referenced to the 1.8-V core digital power supply. A 1.8-V external oscillator may be connected to the X1 pin. In this case, the XCLKIN pin must be connected to ground. If a 3.3-V external oscillator is used with the XCLKIN pin, X1 must be tied to GND. (I)
X2	86	C6	Internal Oscillator Output. A quartz crystal or a ceramic resonator may be connected across X1 and X2. If X2 is not used it must be left unconnected. (O)
RESET			
$\overline{\text{XRS}}$	78	B8	Device Reset (in) and Watchdog Reset (out). Device reset. $\overline{\text{XRS}}$ causes the device to terminate execution. The PC will point to the address contained at the location 0x3FFFC0. When $\overline{\text{XRS}}$ is brought to a high level, execution begins at the location pointed to by the PC. This pin is driven low by the DSP when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. (I/OD, ↑) The output buffer of this pin is an open-drain with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.
ADC SIGNALS			
ADCINA7	16	F3	ADC Group A, Channel 7 input (I)
ADCINA6	17	F4	ADC Group A, Channel 6 input (I)
ADCINA5	18	G4	ADC Group A, Channel 5 input (I)
ADCINA4	19	G1	ADC Group A, Channel 4 input (I)
ADCINA3	20	G2	ADC Group A, Channel 3 input (I)
ADCINA2	21	G3	ADC Group A, Channel 2 input (I)
ADCINA1	22	H1	ADC Group A, Channel 1 input (I)
ADCINA0	23	H2	ADC Group A, Channel 0 input (I)
ADCINB7	34	K5	ADC Group B, Channel 7 input (I)
ADCINB6	33	H4	ADC Group B, Channel 6 input (I)
ADCINB5	32	K4	ADC Group B, Channel 5 input (I)
ADCINB4	31	J4	ADC Group B, Channel 4 input (I)
ADCINB3	30	K3	ADC Group B, Channel 3 input (I)
ADCINB2	29	H3	ADC Group B, Channel 2 input (I)
ADCINB1	28	J3	ADC Group B, Channel 1 input (I)
ADCINB0	27	K2	ADC Group B, Channel 0 input (I)
ADCLO	24	J1	Low Reference (connect to analog ground) (I)
ADCRESEXT	38	F5	ADC External Current Bias Resistor. Connect a 22-kΩ resistor to analog ground.
ADCREFIN	35	J5	External reference input (I)
ADCREFP	37	G5	Internal Reference Positive Output. Requires a low ESR (50 mΩ – 1.5 Ω) ceramic bypass capacitor of 2.2 μF to analog ground. (O)
ADCREFM	36	H5	Internal Reference Medium Output. Requires a low ESR (50 mΩ – 1.5 Ω) ceramic bypass capacitor of 2.2 μF to analog ground. (O)
CPU AND I/O POWER PINS			
V_{DDA2}	15	F2	ADC Analog Power Pin (3.3 V)
V_{SSA2}	14	F1	ADC Analog Ground Pin
V_{DDAIO}	26	J2	ADC Analog I/O Power Pin (3.3 V)
V_{SSAIO}	25	K1	ADC Analog I/O Ground Pin
V_{DD1A18}	12	E4	ADC Analog Power Pin (1.8 V)
$V_{SS1AGND}$	13	E5	ADC Analog Ground Pin
V_{DD2A18}	40	J6	ADC Analog Power Pin (1.8 V)
$V_{SS2AGND}$	39	K6	ADC Analog Ground Pin

Table 4-1. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM/ ZGM BALL #	
V_{DD}	10	E2	CPU and Logic Digital Power Pins (1.8 V)
V_{DD}	42	G6	
V_{DD}	59	F10	
V_{DD}	68	D7	
V_{DD}	85	B6	
V_{DD}	93	D4	
V_{DDIO}	3	C2	Digital I/O Power Pin (3.3 V)
V_{DDIO}	46	H7	
V_{DDIO}	65	E9	
V_{DDIO}	82	A7	
V_{SS}	2	B1	Digital Ground Pins
V_{SS}	11	E3	
V_{SS}	41	H6	
V_{SS}	49	K9	
V_{SS}	55	H10	
V_{SS}	62	F7	
V_{SS}	69	D10	
V_{SS}	77	A9	
V_{SS}	87	D6	
V_{SS}	89	A5	
V_{SS}	94	A4	
GPIOA AND PERIPHERAL SIGNALS (2)			
GPIO0 EPWM1A - -	47	K8	General purpose input/output 0 (I/O/Z) (3) Enhanced PWM1 Output and HRPWM channel (O) - -
GPIO1 EPWM2A - -	44	K7	General purpose input/output 1 (I/O/Z) (3) Enhanced PWM2 Output A and HRPWM channel (O) - -
GPIO2 EPWM3A - -	45	J7	General purpose input/output 2 (I/O/Z) (3) Enhanced PWM3 Output A and HRPWM channel (O) - -
GPIO3 EPWM4A - -	48	J8	General purpose input/output 3 (I/O/Z) (3) Enhanced PWM4 Output A and HRPWM channel (O) - -
GPIO4 EPWM5A - -	51	J9	General purpose input/output 4 (I/O/Z) (3) Enhanced PWM5 output A and HRPWM channel (O) - -
GPIO5 EPWM6A - -	53	H9	General purpose input/output 5 (I/O/Z) (3) Enhanced PWM6 Output A and HRPWM channel (O) - -

(2) All GPIO pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup, which can be selectively enabled/disabled on a per-pin basis. This feature only applies to the GPIO pins. The GPIO function (shown in Italics) is the default at reset. The peripheral signals that are listed under them are alternate functions.
(3) The pullups on GPIO0–GPIO15 pins are not enabled at reset.

Table 4-1. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM/ ZGM BALL #	
GPIO6 EPWM7A EPWMSYNCI EPWMSYNCO	56	G9	General purpose input/output 6 (I/O/Z)(3) Enhanced PWM7 output A and HRPWM channel (O) External ePWM sync pulse input (I) External ePWM sync pulse output (O)
GPIO7 EPWM8A -	58	G8	General purpose input/output 7 (I/O/Z)(3) Enhanced PWM8 Output A and HRPWM channel (O) -
GPIO8 EPWM9A - $\overline{\text{ADCSOCAO}}$	60	F9	General purpose input/output 8 (I/O/Z)(3) Enhanced PWM9 output A(O) - ADC start-of-conversion A (O)
GPIO9 EPWM10A -	61	F8	General purpose input/output 9 (I/O/Z)(3) Enhanced PWM10 Output A and HRPWM channel (O) -
GPIO10 EPWM11A - $\overline{\text{ADCSOCBO}}$	64	E10	General purpose input/output 10 (I/O/Z)(3) Enhanced PWM11 Output A and HRPWM channel (O) - ADC start-of-conversion B (O)
GPIO11 EPWM12A -	70	D9	General purpose input/output 11 (I/O/Z)(3) Enhanced PWM12 Output A and HRPWM channel (O) -
GPIO12 $\overline{\text{TZ1}}$ EPWM13A -	1	B2	General purpose input/output 12 (I/O/Z)(4) Trip Zone input 1 (I) Enhanced PWM13 Output A and HRPWM channel (O) -
GPIO13 $\overline{\text{TZ2}}$ EPWM14A -	95	B4	General purpose input/output 13 (I/O/Z)(4) Trip zone input 2 (I) Enhanced PWM14 Output A and HRPWM channel (O) -
GPIO14 $\overline{\text{TZ3}}$ EPWM15A -	8	D3	General purpose input/output 14 (I/O/Z)(4) Trip zone input 3 (I) Enhanced PWM15 Output A and HRPWM channel (O) -
GPIO15 $\overline{\text{TZ4}}$ EPWM16A -	9	E1	General purpose input/output 15 (I/O/Z)(4) Trip zone input 4 (I) Enhanced PWM16 Output A and HRPWM channel (O) -
GPIO16 SPISIMOA - $\overline{\text{TZ5}}$	50	K10	General purpose input/output 16 (I/O/Z)(4) SPI-A slave in, master out (I/O) - Trip zone input 5 (I)
GPIO17 SPISOMIA - $\overline{\text{TZ6}}$	52	J10	General purpose input/output 17 (I/O/Z)(4) SPI-A slave out, master in (I/O) - Trip zone input 6(I)
GPIO18 SPICLKA - $\overline{\text{TZ1}}$	54	H8	General purpose input/output 18 (I/O/Z)(4) SPI-A clock input/output (I/O) - Trip zone input 1 (I)
GPIO19 SPISTEA - $\overline{\text{TZ2}}$	57	G10	General purpose input/output 19 (I/O/Z)(4) SPI-A slave transmit enable input/output (I/O) - Trip zone input 2 (I)
GPIO20 - - -	63	F6	General purpose input/output 20 (I/O/Z)(4) - - -

(4) The pullups on GPIO16–GPIO34 are enabled upon reset.

Table 4-1. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM/ ZGM BALL #	
GPIO21 - - -	67	E7	General purpose input/output 21 (I/O/Z)(4) - - -
GPIO22 - - -	71	D8	General purpose input/output 22 (I/O/Z)(4) - - -
GPIO23 - - -	72	C10	General purpose input/output 23 (I/O/Z)(4) - - -
GPIO24 - - -	83	C7	General purpose input/output 24 (I/O/Z)(4) - - -
GPIO25 - - -	91	C5	General purpose input/output 25 (I/O/Z)(4) - - -
GPIO26 - - -	99	A2	General purpose input/output 26 (I/O/Z)(4) - - -
GPIO27 - - -	79	C8	General purpose input/output 27 (I/O/Z)(4) - - -
GPIO28 SCIRXDA - $\overline{TZ5}$	92	D5	General purpose input/output 28. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) SCI receive data (I) - Trip zone 5 (I)
GPIO29 SCITXDA - $\overline{TZ6}$	4	C3	General purpose input/output 29. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) SCI transmit data (O) - Trip zone 6 (I)
GPIO30 - - $\overline{TZ3}$	6	D2	General purpose input/output 30. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) - - Trip zone input 3 (I)
GPIO31 - - $\overline{TZ4}$	7	D1	General purpose input/output 31. This pin has an 8-mA (typical) output buffer. (I/O/Z)(4) - - Trip zone input 4 (I)
GPIO32 SDAA EPWMSYNCI $\overline{ADCSOCAO}$	100	A1	General purpose input/output 32 (I/O/Z)(4) I2C data open-drain bidirectional port (I/OD) Enhanced PWM external sync pulse input (I) ADC start-of-conversion (O)

Table 4-1. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PZ PIN #	GGM/ ZGM BALL #	
GPIO33 SCLA EPWMSYNCO ADCSOCBO	5	C1	General-Purpose Input/Output 33 (I/O/Z)(4) I2C clock open-drain bidirectional port (I/OD) Enhanced PWM external synch pulse output (O) ADC start-of-conversion (O)
GPIO34 - - -	43	G7	General-Purpose Input/Output 34 (I/O/Z)(4) - - -

5 Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320F28044 DSP.

5.1 Absolute Maximum Ratings(1)(2)

Unless otherwise noted, the list of absolute maximum ratings are specified over operating temperature ranges.

		MIN	MAX	UNIT
Supply voltage	V_{DDIO}, V_{DD3VFL} with respect to V_{SS}	–0.3	4.6	V
	V_{DDA2}, V_{DDAIO} with respect to V_{SSA}	–0.3	4.6	
	V_{DD} with respect to V_{SS}	–0.3	2.5	
	V_{DD1A18}, V_{DD2A18} with respect to V_{SSA}	–0.3	2.5	
	V_{SSA2}, V_{SSAIO}, $V_{SS1AGND}$, $V_{SS2AGND}$ with respect to V_{SS}	–0.3	0.3	
Input voltage	V_{IN}	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})(3)	–20	20	mA
Output clamp current	I_{OK} (V_O < 0 or V_O > V_{DDIO})	–20	20	mA
Operating ambient temperature, T_A	A version (GGM, PZ)(4)	–40	85	°C
Junction temperature	T_J(4)	–40	150	°C
Storage temperature	T_{stg}(4)	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ±2 mA. This includes the analog inputs which have an internal clamping circuit that clamps the voltage to a diode drop above V_{DDA2} or below V_{SSA2}.
(4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *Semiconductor and IC Package Thermal Metrics*; *Calculating Useful Lifetimes of Embedded Processors*; and *Calculating FIT for a Mission Profile*.

5.2 ESD Ratings – Commercial

			VALUE	UNIT
100-ball ZGM package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	
100-ball GGM package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	
100-pin PZ package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		3.14	3.3	3.47	V
Device supply voltage CPU, V_{DD}		1.71	1.8	1.89	V
Supply ground, V_{SS}, V_{SSIO}			0		V
ADC supply voltage (3.3 V), V_{DDA2}, V_{DDAIO}		3.14	3.3	3.47	V
ADC supply voltage (1.8 V), V_{DD1A18}, V_{DD2A18}		1.71	1.8	1.89	V
Flash supply voltage, V_{DD3VFL}		3.14	3.3	3.47	V
Device clock frequency (system clock), $f_{SYSCLKOUT}$		2		100	MHz
High-level input voltage, V_{IH}	All inputs except X1	2		V_{DDIO} + 0.3	V
	X1	0.7 * V_{DD} – 0.05		V_{DD}	
Low-level input voltage, V_{IL}	All inputs except X1	V_{SS} – 0.3		0.8	V
	X1			0.3 * V_{DD} + 0.05	
High-level output source current, V_{OH} = 2.4 V, I_{OH}	All I/Os except Group 2			–4	mA
	Group 2 (1)			–8	
Low-level output sink current, V_{OL} = V_{OL} MAX, I_{OL}	All I/Os except Group 2			4	mA
	Group 2 (1)			8	
Ambient temperature, T_A	A version	–40		85	°C

(1) Group 2 pins are as follows: GPIO28, GPIO29, GPIO30, GPIO31, TDO, XCLKOUT, EMU0, and EMU1

5.4 Power Consumption Summary

Table 5-1. TMS320F28044 Current Consumption by Power-Supply Pins at 100-MHz SYSCLKOUT

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} (1)		I_{DD3VFL} (2)		I_{DDA18} (3)		I_{DDA33} (4)	
		TYP(5)	MAX(6)	TYP(5)	MAX(6)	TYP	MAX(6)	TYP(5)	MAX(6)	TYP(5)	MAX(6)
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1-16 • SCI-A • SPI-A • ADC • I^2C All PWM pins are toggled at 100 kHz. All I/O pins are left unconnected. Data is continuously transmitted out of the SCI-A port. The hardware multiplier is exercised. Code is running out of flash with 3 wait-states. XCLKOUT is turned off.	205 mA	230 mA	10 mA	15 mA	35 mA	40 mA	30 mA	38 mA	1.5 mA	2 mA
IDLE	Flash is powered down. XCLKOUT is turned off. The following peripheral clocks are enabled: • SCI-A • SPI-A • I^2C	75 mA	90 mA	500 µA	2 mA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
STANDBY	Flash is powered down. Peripheral clocks are off.	6 mA	12 mA	100 µA	500 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled.	70 µA		60 µA	120 µA	2 µA	10 µA	5 µA	50 µA	15 µA	30 µA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) The I_{DD3VFL} current indicated in this table is the flash read-current and does not include additional current for erase/write operations. During flash programming, extra current is drawn from the V_{DD} and V_{DD3VFL} rails, as indicated in Table 5-31. If the user application involves on-board flash programming, this extra current must be taken into account while architecting the power-supply stage.
(3) I_{DDA18} includes current into V_{DD1A18} and V_{DD2A18} pins. In order to realize the I_{DDA18} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(4) I_{DDA33} includes current into V_{DDA2} and V_{DDAIO} pins.
(5) The TYP numbers are applicable over room temperature and nominal voltage.
(6) MAX numbers are at 85°C and MAX voltage.

NOTE

The peripheral - I/O multiplexing implemented in the F28044 device prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

5.4.1 Reducing Current Consumption

Since each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. Table 5-2 indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 5-2. Typical Current Consumption by Various Peripherals (at 100 MHz)(1)

PERIPHERAL MODULE	I_{DD} CURRENT REDUCTION (mA)(2)
ADC	8(3)
I^2C	5
ePWM	5
SCI	4
SPI	5

(1) All peripheral clocks are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) For peripherals with multiple instances, the current quoted is per module. For example, the 5 mA number quoted for ePWM is for one ePWM module.
(3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA18}) as well.

NOTE

I_{DDIO} current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

NOTE

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 110 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

5.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}$ MAX		2.4			V
			I_{OH} = 50 µA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}$ MAX				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os (including $\overline{XRS}$)	–80	–140	–190	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DDIO}$				±2	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DDIO}$ (F280x)		28	50	80	
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DDIO}$ (C280x)		80	140	190	
I_{OZ}	Output current, pullup or pulldown disabled		$V_O = V_{DDIO}$ or 0 V				±2	µA
C_I	Input capacitance					2		pF

5.6 Thermal Resistance Characteristics for F28044 100-Ball GGM Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	10.36	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	13.3	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	28.15	0
		26.89	150
		25.68	250
		24.22	500
Psi_{JT}	Junction-to-package top	0.38	0
		0.35	150
		0.33	250
		0.44	500

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

5.7 Thermal Resistance Characteristics for F28044 100-Pin PZ Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	7.06	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	28.76	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	44.02	0
		28.34	150
		36.28	250
		33.68	500
Psi_{JT}	Junction-to-package top	0.2	0
		0.56	150
		0.7	250
		0.95	500

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
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- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

5.8 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems with more than 1 Watt power dissipation may require a product level thermal design. Care should be taken to keep T_j within specified limits. In the end applications, T_{case} should be measured to estimate the operating junction temperature T_j. T_{case} is normally measured at the center of the package top side surface. The thermal application note *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

5.9 Timing and Switching Characteristics

5.9.1 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

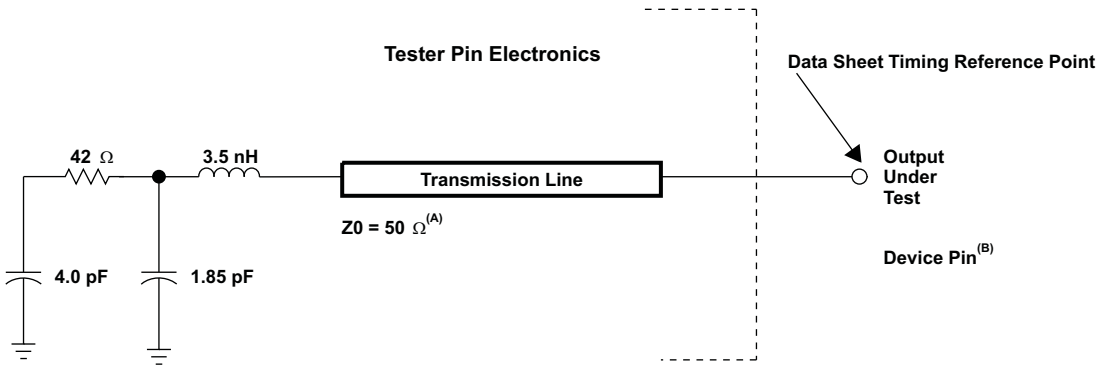
5.9.1.1 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

5.9.1.2 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



A. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

B. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 5-1. 3.3-V Test Load Circuit

5.9.1.3 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the F28044 DSP. Table 5-3 lists the cycle times of various clocks.

Table 5-3. TMS320x280x Clock Table and Nomenclature

		MIN	NOM	MAX	UNIT
On-chip oscillator clock	$t_{c(OSC)}$, Cycle time	28.6		50	ns
	Frequency	20		35	MHz
XCLKIN(1)	$t_{c(CI)}$, Cycle time	10		250	ns
	Frequency	4		100	MHz
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	10		500	ns
	Frequency	2		100	MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time	10		2000	ns
	Frequency	0.5		100	MHz
HSPCLK(2)	$t_{c(HCO)}$, Cycle time	10	20(3)		ns
	Frequency		50(3)	100	MHz
LSPCLK(2)	$t_{c(LCO)}$, Cycle time	10	40(3)		ns
	Frequency		25(3)	100	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	80			ns
	Frequency			12.5	MHz

(1) This also applies to the X1 pin if a 1.8-V oscillator is used.
(2) Lower LSPCLK and HSPCLK will reduce device power consumption.
(3) This is the default reset value if SYSCLKOUT = 100 MHz.

5.9.2 Power Sequencing

No requirements are placed on the power up/down sequence of the various power pins to ensure the correct reset state for all the modules. However, if the 3.3-V transistors in the level shifting output buffers of the I/O pins are powered prior to the 1.8-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} (core voltage) pins prior to or simultaneously with the V_{DDIO} (input/output voltage) pins, ensuring that the V_{DD} pins have reached 0.7 V before or at the same time as the V_{DDIO} pins reach 0.7 V.

There are some requirements on the $\overline{XRS}$ pin:

1. During power up, the $\overline{XRS}$ pin must be held low for $t_{w(RSL1)}$ after the input clock is stable (see Table 5-5). This is to enable the entire device to start from a known condition.
2. During power down, the $\overline{XRS}$ pin must be pulled low at least 8 µs prior to V_{DD} reaching 1.5 V. This is to enhance flash reliability.

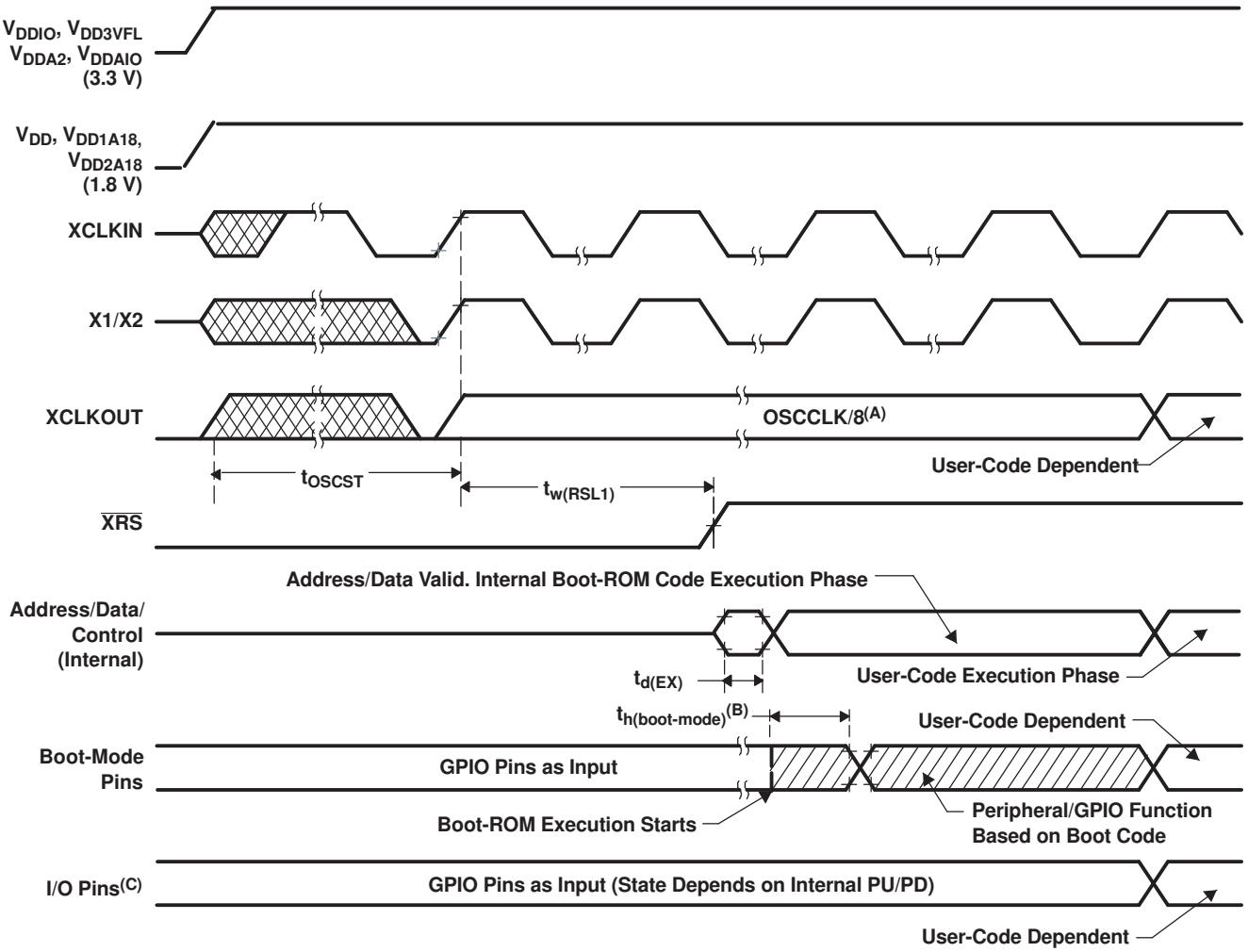
No voltage larger than a diode drop (0.7 V) above V_{DDIO} should be applied to any digital pin (for analog pins, it is 0.7 V above V_{DDA}) prior to powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.

5.9.2.1 Power Management and Supervisory Circuit Solutions

Table 5-4 lists the power management and supervisory circuit solutions for F28044 DSP. LDO selection depends on the total power consumed in the end application. Go to www.power.ti.com for a complete list of TI power ICs or select the **Reference Designs** link for specific power reference designs.

Table 5-4. Power Management and Supervisory Circuit Solutions

SUPPLIER	TYPE	PART	DESCRIPTION
Texas Instruments	LDO	TPS767D301	Dual 1-A low-dropout regulator (LDO) with supply voltage supervisor (SVS)
Texas Instruments	LDO	TPS70202	Dual 500/250-mA LDO with SVS
Texas Instruments	LDO	TPS766xx	250-mA LDO with PG
Texas Instruments	SVS	TPS3808	Open Drain SVS with programmable delay
Texas Instruments	SVS	TPS3803	Low-cost Open-drain SVS with 5-µS delay
Texas Instruments	LDO	TPS799xx	200-mA LDO in WCSP package
Texas Instruments	LDO	TPS736xx	400-mA LDO with 40 mV of V_{DO}
Texas Instruments	DC/DC	TPS62110	High V_{in} 1.2-A dc/dc converter in 4 x 4 QFN package
Texas Instruments	DC/DC	TPS6230x	500-mA converter in WCSP package



A. Upon power up, SYSCLKOUT is OSCCLK/2. Since the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = OSCCLK/8 during this phase.

B. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

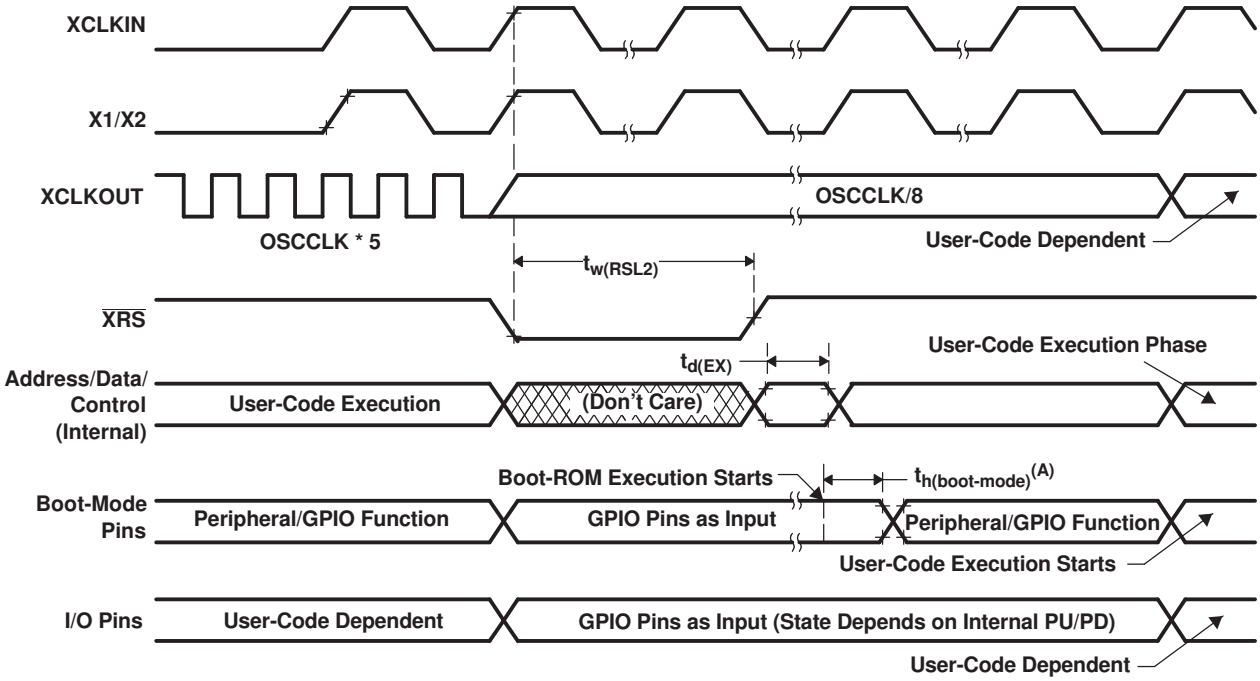
C. See Section 5.9.2 for requirements to ensure a high-impedance state for GPIO pins during power-up.

Figure 5-2. Power-on Reset

Table 5-5. Reset ($\overline{XRS}$) Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(RSL1)}$ (1)	Pulse duration, stable XCLKIN to $\overline{XRS}$ high		$8t_{c(OSCCLK)}$			cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low	Warm reset	$8t_{c(OSCCLK)}$			cycles
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog			$512t_{c(OSCCLK)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high			$32t_{c(OSCCLK)}$		cycles
t_{OSCST} (2)	Oscillator start-up time		1	10		ms
$t_{h(boot-mode)}$	Hold time for boot-mode pins		$200t_{c(OSCCLK)}$			cycles

(1) In addition to the $t_{w(RSL1)}$ requirement, $\overline{XRS}$ has to be low at least for 1 ms after V_{DD} reaches 1.5 V.
(2) Dependent on crystal/resonator and board design.



A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 5-3. Warm Reset

Figure 5-4 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and SYSCLKOUT = OSCCLK x 2. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, SYSCLKOUT = OSCCLK/2. After the PLL lock-up is complete (which takes 131072 OSCCLK cycles), SYSCLKOUT reflects the new operating frequency, OSCCLK x 4.

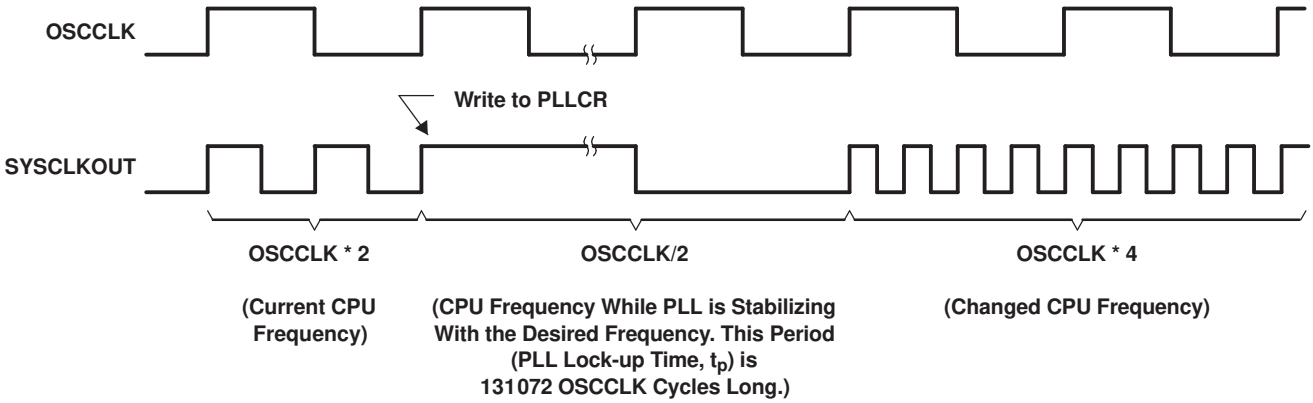


Figure 5-4. Example of Effect of Writing Into PLLCR Register

5.9.3 Clock Requirements and Characteristics

Table 5-6. Input Clock Frequency

PARAMETER			MIN	TYP	MAX	UNIT
f_x	Input clock frequency	Resonator (X1/X2)	20		35	MHz
		Crystal (X1/X2)	20		35	
		External oscillator/clock source (XCLKIN or X1 pin)	4		100	
f_l	Limp mode SYSCLKOUT frequency range (with /2 enabled)			1–5		MHz

Table 5-7. XCLKIN(1) Timing Requirements - PLL Enabled

NO.			MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN	33.3	200	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45	55	%

(1) This applies to the X1 pin also.

Table 5-8. XCLKIN(1) Timing Requirements - PLL Disabled

NO.				MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN		10	250	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 100 MHz		2	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 100 MHz		2	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$		45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$		45	55	%

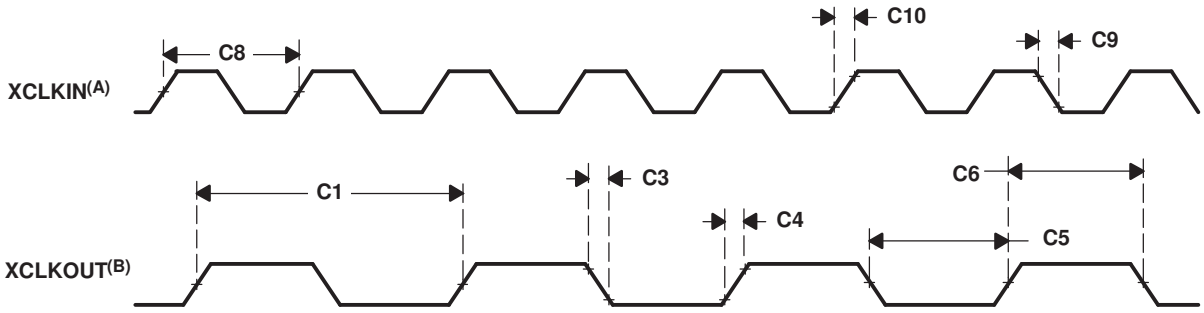
(1) This applies to the X1 pin also.

The possible configuration modes are shown in Table 6-25.

Table 5-9. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)(1) (2)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
C1	$t_{c(XCO)}$	Cycle time, XCLKOUT	10			ns
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		2		ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		2		ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2		H + 2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2		H + 2	ns
	t_p	PLL lock time			$131072t_{c(OSCCLK)}$ (3)	cycles

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$
(3) OSCCLK is either the output of the on-chip oscillator or the output from an external oscillator.



A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.

B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 5-5. Clock Timing

5.9.4 Peripherals

5.9.4.1 General-Purpose Input/Output (GPIO)

5.9.4.1.1 GPIO - Output Timing

Table 5-10. General-Purpose Output Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8	ns
t_{fGPO}	Toggling frequency, GPO pins			25	MHz

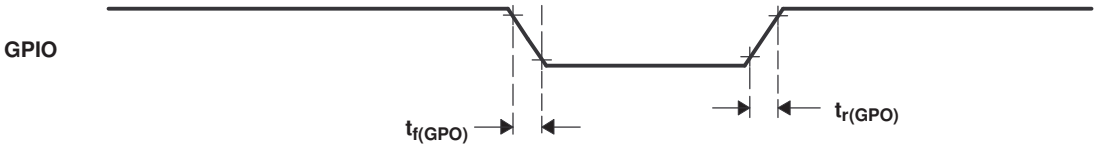


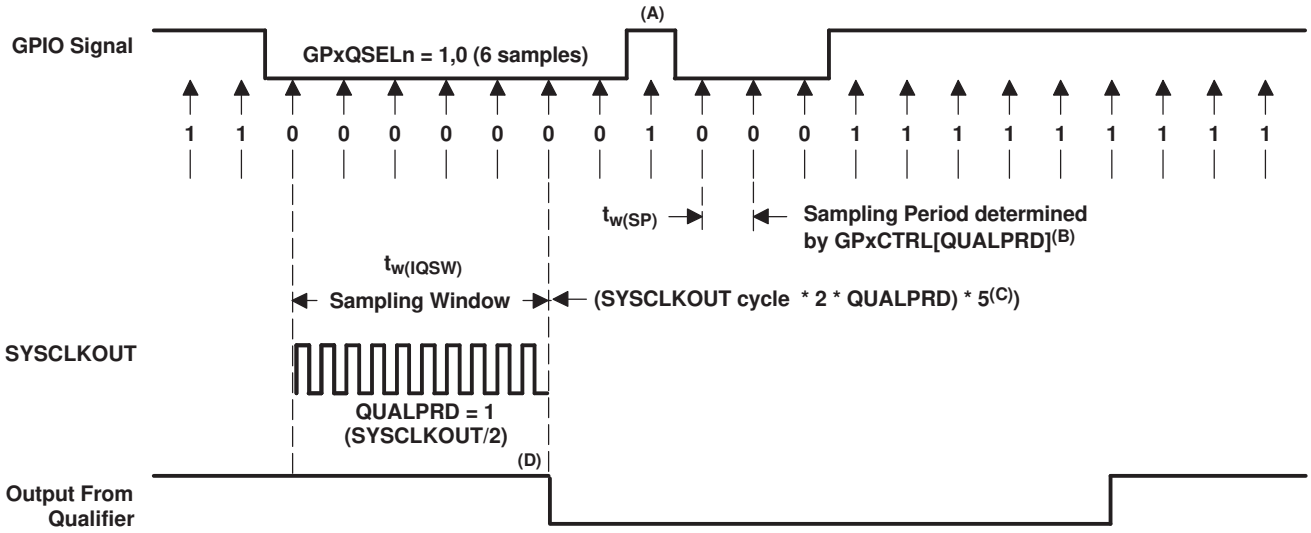
Figure 5-6. General-Purpose Output Timing

5.9.4.1.2 GPIO - Input Timing

Table 5-11. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SCO)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SCO)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * [n(1) – 1]		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SCO)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SCO)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (that is, at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).

B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLKOUT cycles. This would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 5-7. Sampling Mode

5.9.4.1.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = SYSCLKOUT/(2 * QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLKOUT, if QUALPRD = 0

Sampling period = SYSCLKOUT cycle x 2 x QUALPRD, if QUALPRD ≠ 0

In the above equations, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 5, if QUALPRD = 0

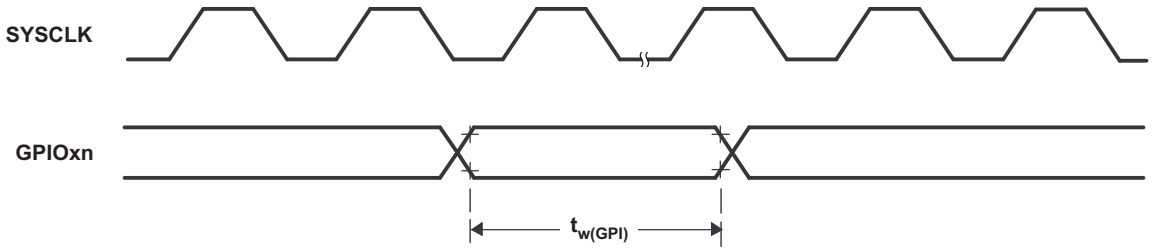


Figure 5-8. General-Purpose Input Timing

NOTE

The pulse-width requirement for general-purpose input is applicable for the XINT2_ADCSOC signal as well.

5.9.4.1.4 Low-Power Mode Wakeup Timing

Table 5-12 shows the timing requirements, Table 5-13 shows the switching characteristics, and Figure 5-9 shows the timing diagram for IDLE mode.

Table 5-12. IDLE Mode Timing Requirements(1)

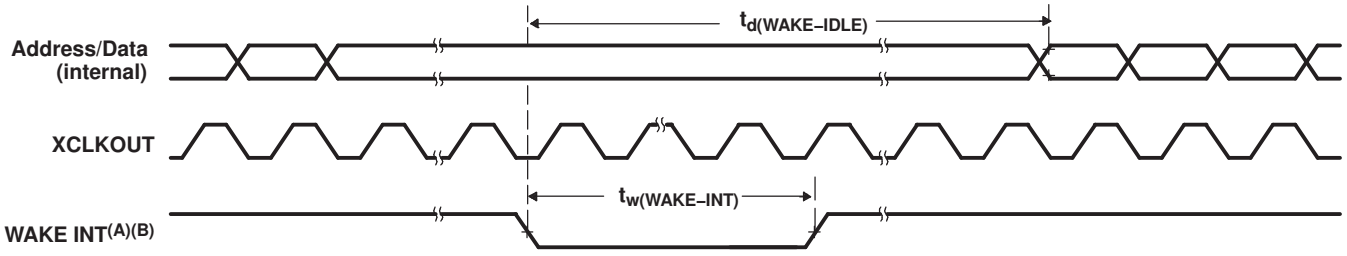
			MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SCO)}$			cycles
		With input qualifier	$5t_{c(SCO)} + t_{w(IQSW)}$			

(1) For an explanation of the input qualifier parameters, see Table 5-11.

Table 5-13. IDLE Mode Switching Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)					
	• Wake-up from Flash – Flash module in active state	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier			$1050t_{c(SCO)}$	cycles
		With input qualifier			$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from SARAM	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Table 5-11.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up) signal involves additional latency.



A. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$, XNMI, or $\overline{\text{XRS}}$.
B. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-9. IDLE Entry and Exit Timing

Table 5-14. STANDBY Mode Timing Requirements

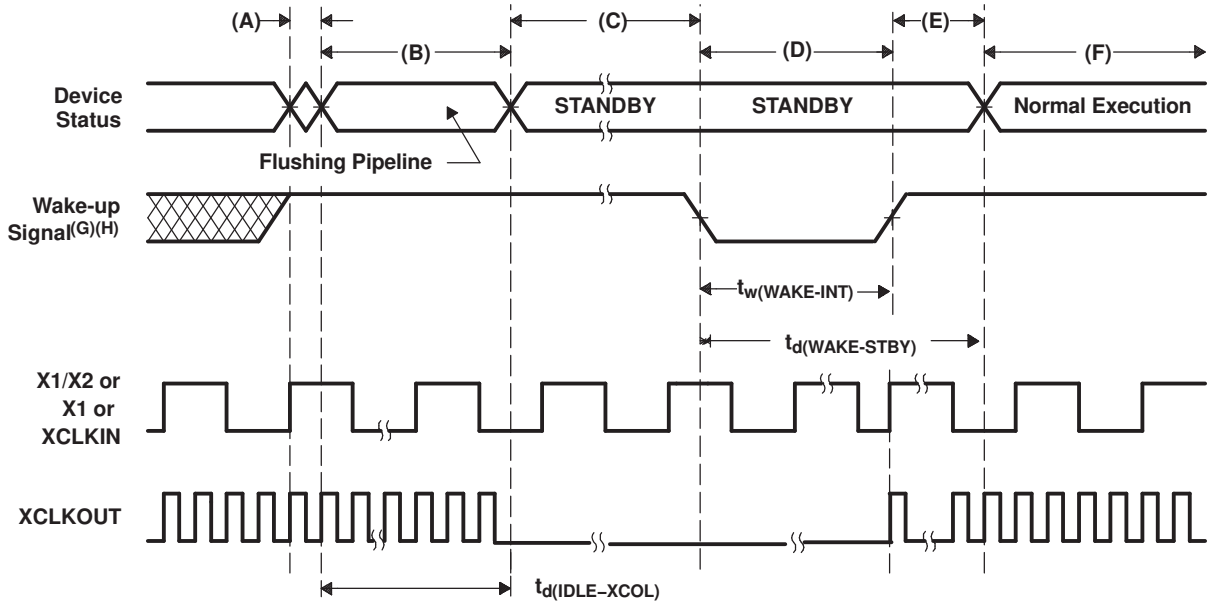
		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification	$3t_{c(OSCCLK)}$			cycles
		With input qualification(1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$			

(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

Table 5-15. STANDBY Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low		$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)					cycles
	• Wake up from flash – Flash module in active state	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier			$1125t_{c(SCO)}$	cycles
		With input qualifier			$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from SARAM	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up signal) involves additional latency.



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for approximately 32 cycles (if CLKINDIV = 0) or 64 cycles (if CLKINDIV = 1) before being turned off. This delay enables the CPU pipe and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode.
D. The external wake-up signal is driven active.
E. After a latency period, the STANDBY mode is exited.
F. Normal execution resumes. The device will respond to the interrupt (if enabled).
G. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic.
H. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-10. STANDBY Entry and Exit Timing Diagram

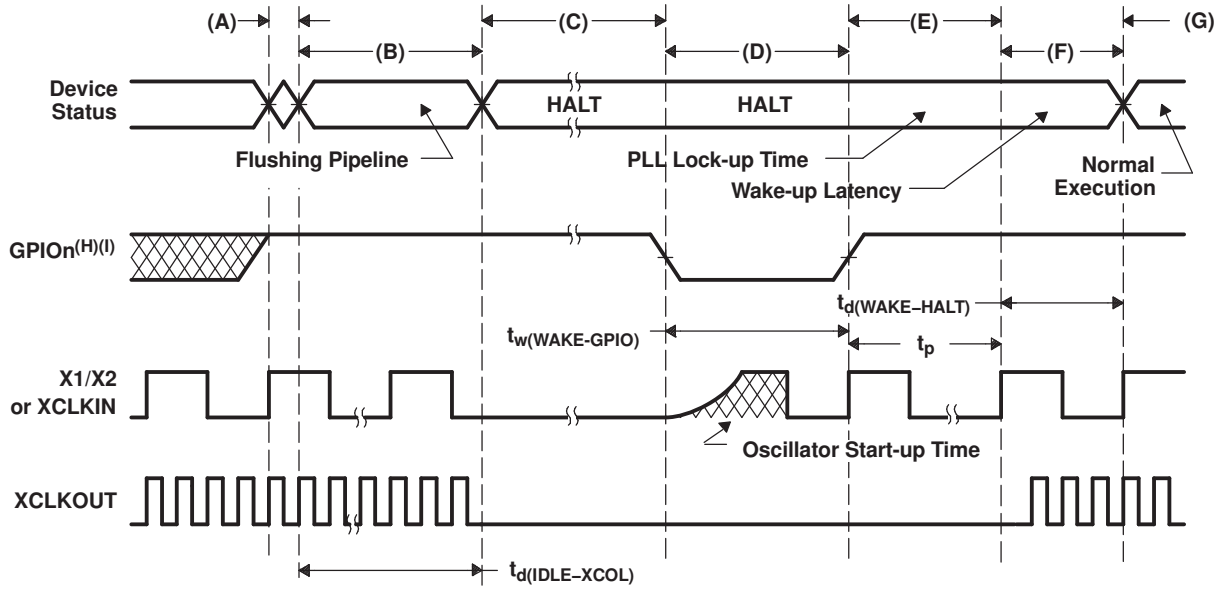
Table 5-16. HALT Mode Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$ (1)			cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wakeup signal	$t_{oscst} + 8t_{c(OSCCLK)}$			cycles

(1) See Table 5-5 for an explanation of t_{oscst}.

Table 5-17. HALT Mode Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low	$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
t_p	PLL lock-up time			$131072t_{c(OSCCLK)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, PLL lock to program execution resume • Wake up from flash – Flash module in sleep state			$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM			$35t_{c(SCO)}$	cycles



A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for approximately 32 cycles (if CLKINDIV = 0) or 64 cycles (if CLKINDIV = 1) before the oscillator is turned off and the CLKIN to the core is stopped. This delay enables the CPU pipe and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power.

D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Since the falling edge of the GPIO pin asynchronously begins the wakeup process, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. Once the oscillator has stabilized, the PLL lock sequence is initiated, which takes 131,072 OSCCLK (X1/X2 or X1 or XCLKIN) cycles. Note that these 131,072 clock cycles are applicable even when the PLL is disabled (that is, code execution will be delayed by this duration even when the PLL is disabled).

F. Clocks to the core and peripherals are enabled. The HALT mode is now exited. The device will respond to the interrupt (if enabled), after a latency.

G. Normal operation resumes.

H. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic.

I. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

Figure 5-11. HALT Wake-Up Using GPIOn

5.9.4.2 Enhanced Control Peripherals

5.9.4.2.1 Enhanced Pulse Width Modulator (ePWM) Timing

Table 5-18 shows the PWM output timing requirements and Table 5-19, switching characteristics.

Table 5-18. ePWM Timing Requirements(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SYCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-11.

Table 5-19. ePWM Switching Characteristics

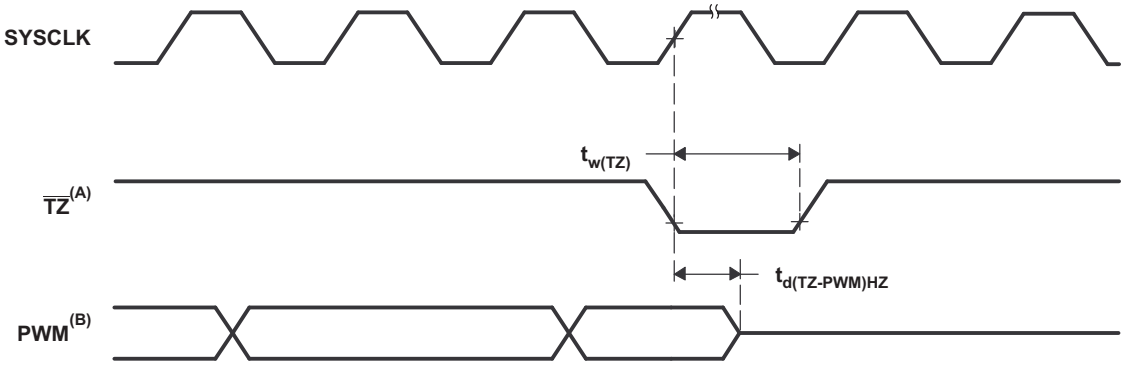
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

5.9.4.2.2 Trip-Zone Input Timing

Table 5-20. Trip-Zone input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-11.



A. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, $\overline{TZ4}$, $\overline{TZ5}$, $\overline{TZ6}$

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 5-12. PWM Hi-Z Characteristics

5.9.4.2.3 High-Resolution PWM Timing

Table 5-21 shows the high-resolution PWM switching characteristics.

Table 5-21. High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)

	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.

5.9.4.2.4 ADC Start-of-Conversion Timing

Table 5-22. External ADC Start-of-Conversion Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCAL)}$	Pulse duration, $\overline{\text{ADCSOCAO}}$ low	$32t_{c(HCO)}$		cycles

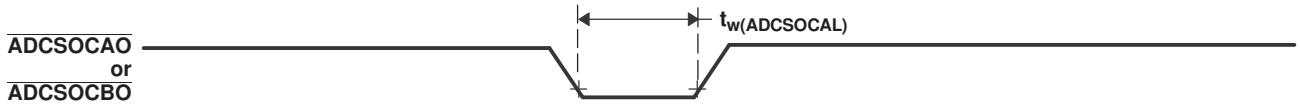


Figure 5-13. $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing

5.9.4.3 External Interrupt Timing

Table 5-23. External Interrupt Timing Requirements(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(INT)}$ (2)	Pulse duration, INT input low/high	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-11.
(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

Table 5-24. External Interrupt Switching Characteristics(1)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{w(IQSW)} + 12t_{c(SCO)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 5-11.

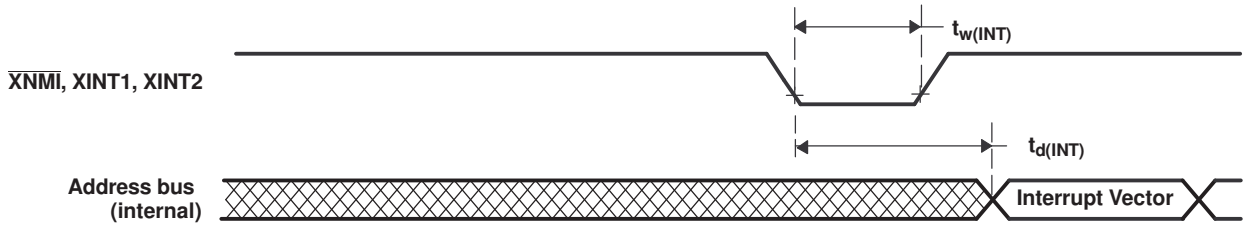


Figure 5-14. External Interrupt Timing

5.9.4.4 I²C Electrical Specification and Timing

Table 5-25. I²C Timing

		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	I²C clock module frequency is between 7 MHz and 12 MHz and I²C prescaler and clock divider registers are configured appropriately		400	kHz
v_{il}	Low level input voltage			0.3 V_{DDIO}	V
V_{ih}	High level input voltage		0.7 V_{DDIO}		V
V_{hys}	Input hysteresis		0.05 V_{DDIO}		V
V_{ol}	Low level output voltage	3 mA sink current	0	0.4	V
t_{LOW}	Low period of SCL clock	I²C clock module frequency is between 7 MHz and 12 MHz and I²C prescaler and clock divider registers are configured appropriately	1.3		µs
t_{HIGH}	High period of SCL clock	I²C clock module frequency is between 7 MHz and 12 MHz and I²C prescaler and clock divider registers are configured appropriately	0.6		µs
I_I	Input current with an input voltage between 0.1 V_{DDIO} and 0.9 V_{DDIO} MAX		–10	10	µA

5.9.4.5 Serial Peripheral Interface (SPI) Master Mode Timing

Table 5-26 lists the master mode timing (clock phase = 0) and Table 5-27 lists the master mode timing (clock phase = 1). Figure 5-15 and Figure 5-16 show the timing waveforms.

Table 5-26. SPI Master Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.	PARAMETER		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid		10		10	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
8	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	35		35		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MAX, slave mode receive 12.5-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).

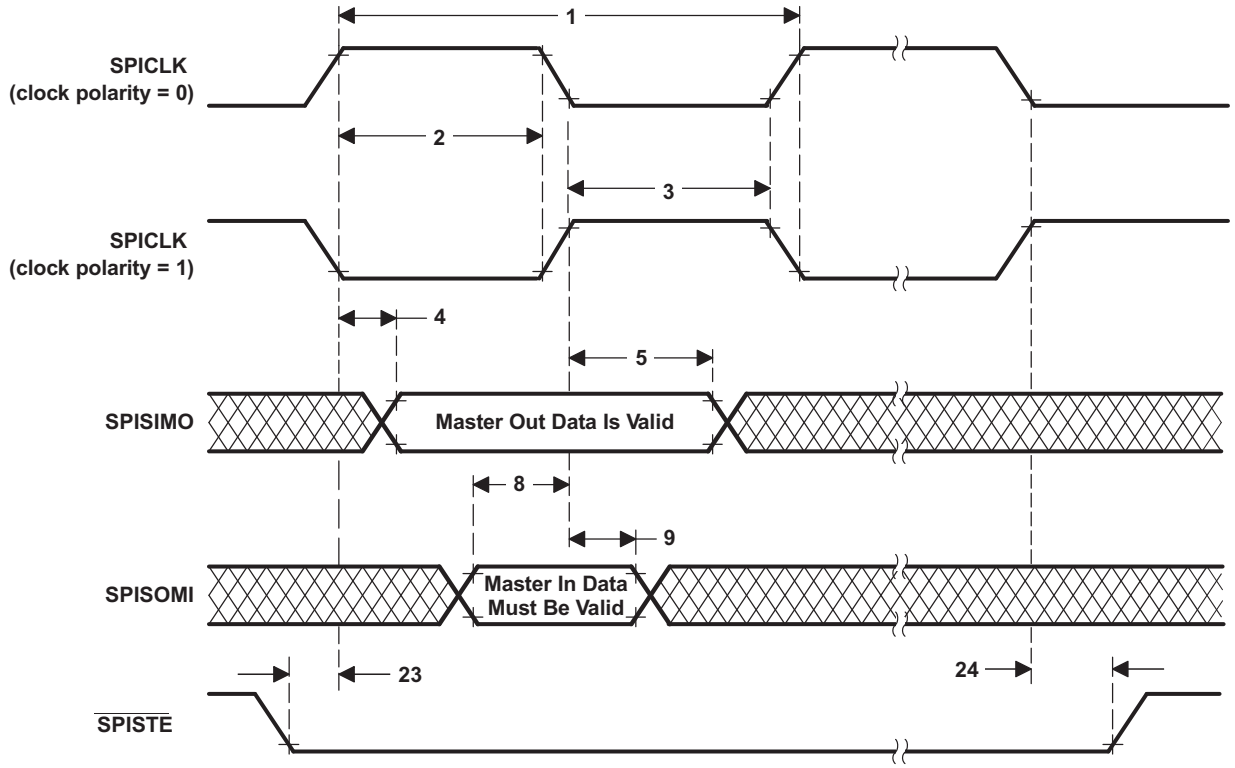


Figure 5-15. SPI Master Mode External Timing (Clock Phase = 0)

Table 5-27. SPI Master Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)(5)

NO.	PARAMETER		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
6	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$		ns
7	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
10	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	35		35		ns
11	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$t_{c(SPC)} - 10$		$t_{c(SPC)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)} - 10$		$0.5t_{c(SPC)} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25 MHz MAX, master mode receive 12.5 MHz MAX
Slave mode transmit 12.5 MHz MAX, slave mode receive 12.5 MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

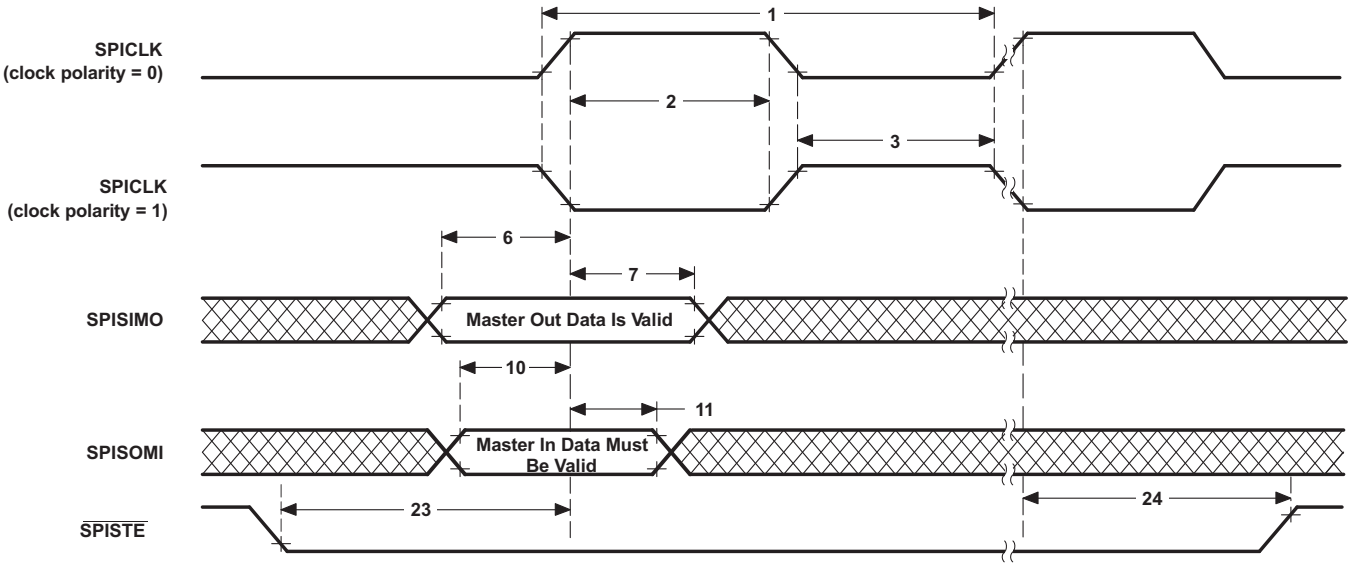


Figure 5-16. SPI Master Mode External Timing (Clock Phase = 1)

5.9.4.6 SPI Slave Mode Timing

Table 5-28 lists the slave mode timing (clock phase = 0) and Table 5-29 lists the slave mode timing (clock phase = 1). Figure 5-17 and Figure 5-18 show the timing waveforms.

Table 5-28. SPI Slave Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.	PARAMETER		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		35	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

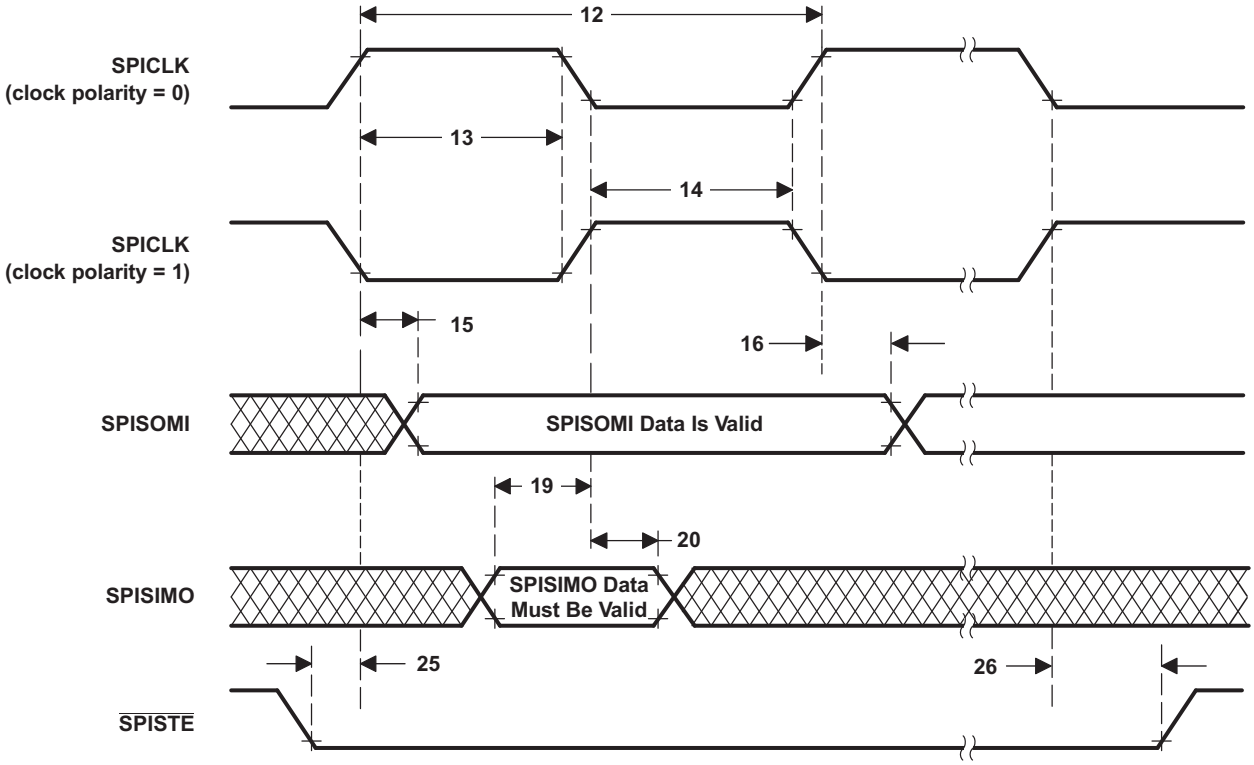


Figure 5-17. SPI Slave Mode External Timing (Clock Phase = 0)

Table 5-29. SPI Slave Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)

NO.	PARAMETER		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
17	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		35	ns
18	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
21	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
22	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

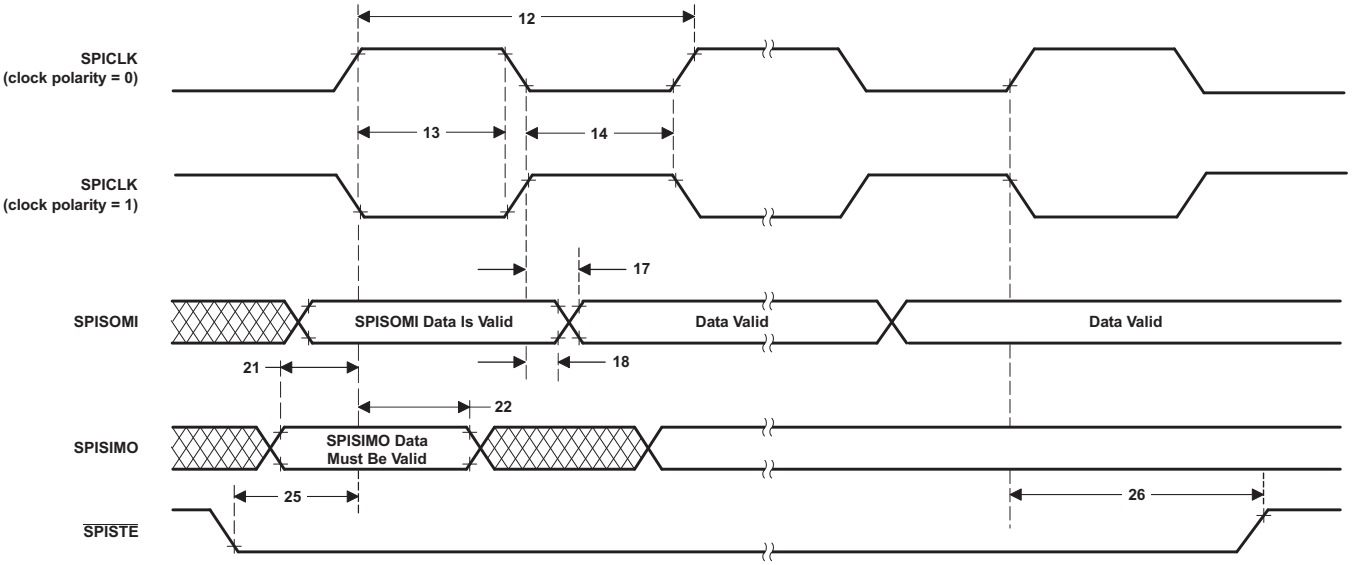


Figure 5-18. SPI Slave Mode External Timing (Clock Phase = 1)

5.9.5 JTAG Debug Probe Connection Without Signal Buffering for the DSP

Figure 5-19 shows the connection between the DSP and JTAG header for a single-processor configuration. If the distance between the JTAG header and the DSP is greater than 6 inches, the emulation signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 5-19 shows the simpler, no-buffering situation. For the pullup/pulldown resistor values, see the pin description section.

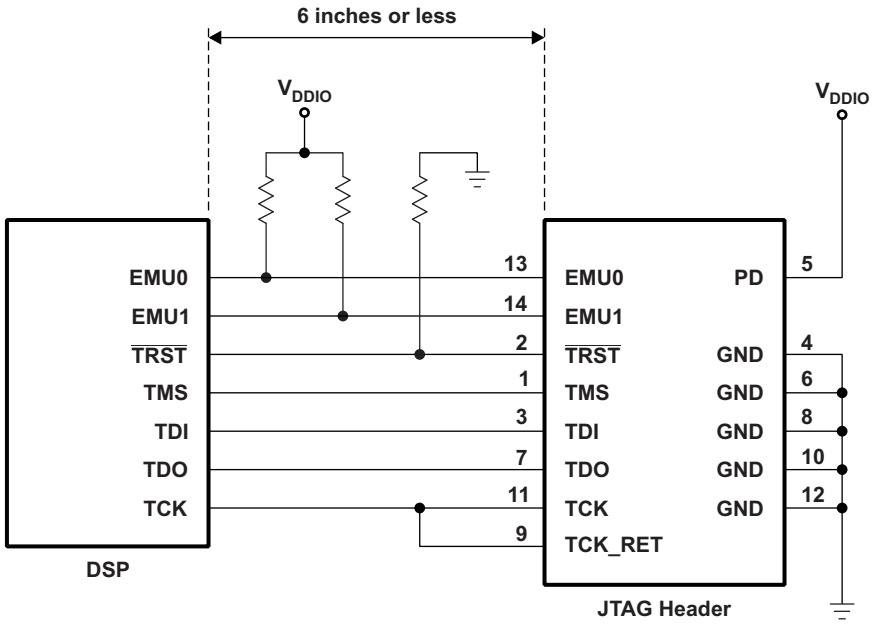


Figure 5-19. JTAG Debug Probe Connection Without Signal Buffering for the DSP

5.9.6 Flash Timing

Table 5-30. Flash Endurance for A Temperature Material

		ERASE/PROGRAM TEMPERATURE	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	0°C to 85°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	0°C to 85°C (ambient)			1	write

Table 5-31. Flash Parameters at 100-MHz SYSCLKOUT

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Time	16-Bit Word			50		µs
	16K Sector			500		ms
Erase Time(2)	16K Sector			10		S
$I_{DD3VFLP}$	V_{DD3VFL} current consumption during the Erase/Program cycle	Erase		75		mA
		Program		35		mA
I_{DDP}	V_{DD} current consumption during Erase/Program cycle			140		mA
I_{DDIOP}	V_{DDIO} current consumption during Erase/Program cycle			20		mA

(1) Typical parameters as seen at room temperature including function call overhead, with all peripherals off. It is important to maintain a stable power supply during the entire flash programming process. It is conceivable that device current consumption during flash programming could be higher than normal operating conditions. The power supply used should ensure V_{MIN} on the supply rails at all times, as specified in the Recommended Operating Conditions of the data sheet. Any brownout or interruption to power during erasing/programming could potentially corrupt the password locations and lock the device permanently. Powering a target board (during flash programming) through the USB port is not recommended, as the port may be unable to respond to the power demands placed during the programming process.

(2) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required before programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

Table 5-32. Flash/OTP Access Timing

PARAMETER		MIN	TYP	MAX	UNIT
$t_{a(fp)}$	Paged flash access time	36			ns
$t_{a(fr)}$	Random flash access time	36			ns
$t_{a(OTP)}$	OTP access time	60			ns

Table 5-33. Flash Data Retention Duration

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{retention}$	Data retention duration	T_J = 55°C	15		years

Table 5-34. Minimum Required Flash/OTP Wait-States at Different Frequencies

SYSCLKOUT (MHz)	SYSCLKOUT (ns)	FLASH PAGE WAIT-STATE	FLASH RANDOM WAIT-STATE(1)	OTP WAIT-STATE
100	10	3	3	5
75	13.33	2	2	4
50	20	1	1	2
30	33.33	1	1	1
25	40	0	1	1
15	66.67	0	1	1
4	250	0	1	1

(1) Random wait-state must be greater than or equal to 1.

Equations to compute the Flash page wait-state and random wait-state in Table 5-34 are as follows:

$$\text{Flash Page Wait-State} = \left[\left(\frac{t_{a(fp)}}{t_{c(SCO)}}\right) - 1\right] \text{(round up to the next highest integer) or 0, whichever is larger}$$

$$\text{Flash Random Wait-State} = \left[\left(\frac{t_{a(fr)}}{t_{c(SCO)}}\right) - 1\right] \text{(round up to the next highest integer) or 1, whichever is larger}$$

Equation to compute the OTP wait-state in Table 5-34 is as follows:

$$\text{OTP Wait-State} = \left[\left(\frac{t_{a(OTP)}}{t_{c(SCO)}}\right) - 1\right] \text{(round up to the next highest integer) or 1, whichever is larger}$$

5.10 On-Chip Analog-to-Digital Converter

Table 5-35. ADC Electrical Characteristics (over recommended operating conditions)(1) (2)

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution		12			Bits
ADC clock		1			kHz
				25	MHz
ACCURACY					
INL (Integral nonlinearity)	1–25 MHz ADC clock (12.5 MSPS)			±2.0	LSB
DNL (Differential nonlinearity)(3)	1–25 MHz ADC clock (12.5 MSPS)			±1	LSB
Offset error (4)		–60		60	LSB
Offset error with hardware trimming			±4		LSB
Overall gain error with internal reference (5)		–60		60	LSB
Overall gain error with external reference		–60		60	LSB
Channel-to-channel offset variation			±4		LSB
Channel-to-channel gain variation			±4		LSB
ANALOG INPUT					
Analog input voltage (ADCINx to ADCLO) (6)		0		3	V
ADCLO		–5	0	5	mV
Input capacitance			10		pF
Input leakage current				±5	µA
INTERNAL VOltAGE REFERENCE(5)					
$V_{ADCREFP}$ - ADCREFP output voltage at the pin based on internal reference			1.275		V
$V_{ADCREFM}$ - ADCREFM output voltage at the pin based on internal reference			0.525		V
Voltage difference, ADCREFP - ADCREFM			0.75		V
Temperature coefficient			50		PPM/°C
EXTERNAL VOltAGE REFERENCE(5) (7)					
$V_{ADCREFIN}$ - External reference voltage input on ADCREFIN pin 0.2% or better accurate reference recommended	ADCREFSEL[15:14] = 11b		1.024		V
	ADCREFSEL[15:14] = 10b		1.500		V
	ADCREFSEL[15:14] = 01b		2.048		V
AC SPECIFICATIONS					
SINAD (100 kHz) Signal-to-noise ratio + distortion			67.5		dB
SNR (100 kHz) Signal-to-noise ratio			68		dB
THD (100 kHz) Total harmonic distortion			–79		dB
ENOB (100 kHz) Effective number of bits			10.9		Bits
SFDR (100 kHz) Spurious free dynamic range			83		dB

(1) Tested at 25-MHz ADCCLK.
(2) All voltages listed in this table are with respect to V_{SSA2}.
(3) TI specifies that the ADC will have no missing codes.
(4) 1 LSB has the weighted value of 3.0/4096 = 0.732 mV.
(5) A single internal/external band gap reference sources both ADCREFP and ADCREFM signals, and hence, these voltages track together. The ADC converter uses the difference between these two as its reference. The total gain error listed for the internal reference is inclusive of the movement of the internal bandgap over temperature. Gain error over temperature for the external reference option will depend on the temperature profile of the source used.
(6) Voltages above V_{DDA} + 0.3 V or below V_{SS} – 0.3 V applied to an analog input pin may temporarily affect the conversion of another pin. To avoid this, the analog inputs should be kept within these limits.
(7) TI recommends using high precision external reference TI part REF3020/3120 or equivalent for 2.048-V reference.

5.10.1 ADC Power-Up Control Bit Timing

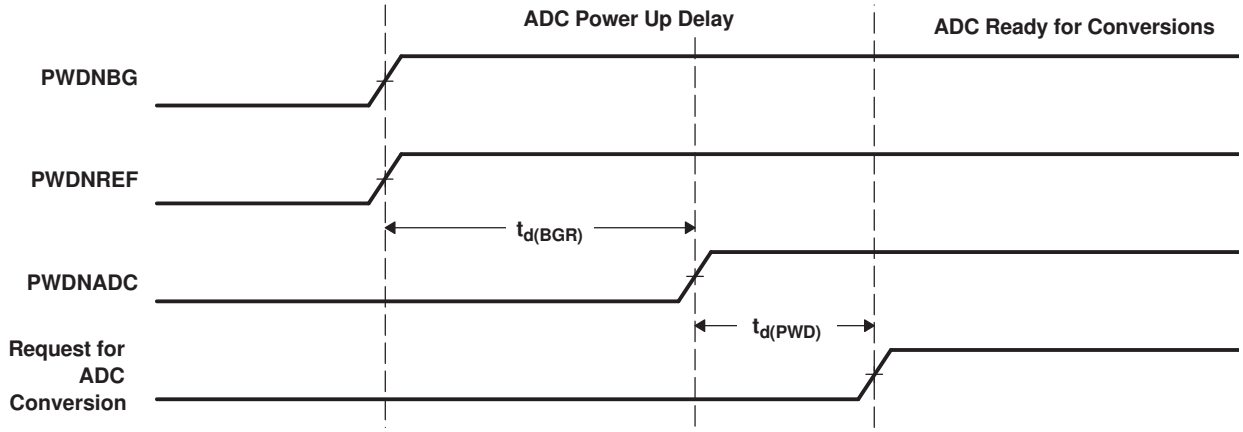


Figure 5-20. ADC Power-Up Control Bit Timing

Table 5-36. ADC Power-Up Delays

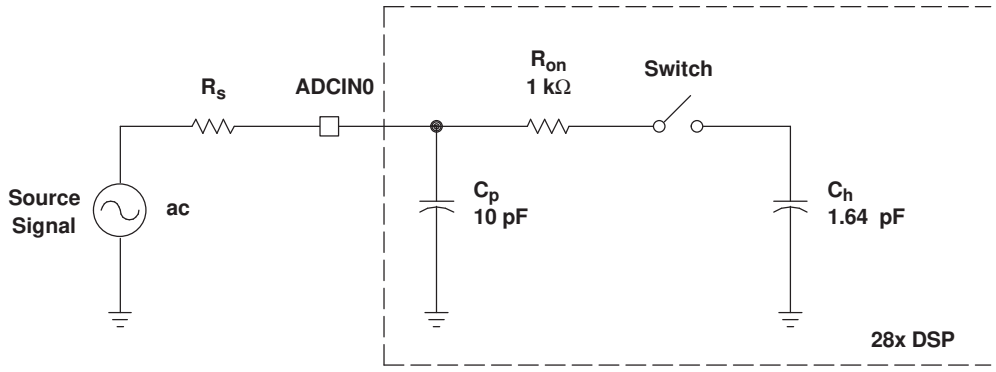
PARAMETER[1]		MIN	TYP	MAX	UNIT
$t_{d(BGR)}$	Delay time for band gap reference to be stable. Bits 7 and 6 of the ADCTRL3 register (ADCBGRFDN1/0) must be set to 1 before the PWDNADC bit is enabled.			5	ms
$t_{d(PWD)}$	Delay time for power-down control to be stable. Bit delay time for band-gap reference to be stable. Bits 7 and 6 of the ADCTRL3 register (ADCBGRFDN1/0) must be set to 1 before the PWDNADC bit is enabled. Bit 5 of the ADCTRL3 register (PWDNADC)must be set to 1 before any ADC conversions are initiated.	20	50		μs
				1	ms

(1) Timings maintain compatibility to the 281x ADC module. The F28044 ADC also supports driving all 3 bits at the same time and waiting $t_{d(BGR)}$ ms before first conversion.

Table 5-37. Current Consumption for Different ADC Configurations (at 25-MHz ADCCLK)[1] [2]

ADC OPERATING MODE	CONDITIONS	V_{DDA18}	$V_{DDA3.3}$	UNIT
Mode A (Operational Mode):	• BG and REF enabled • PWD disabled	30	2	mA
Mode B:	• ADC clock enabled • BG and REF enabled • PWD enabled	9	0.5	mA
Mode C:	• ADC clock enabled • BG and REF disabled • PWD enabled	5	20	μA
Mode D:	• ADC clock disabled • BG and REF disabled • PWD enabled	5	15	μA

(1) Test Conditions:
SYSCLKOUT = 100 MHz
ADC module clock = 25 MHz
ADC performing a continuous conversion of all 16 channels in Mode A
(2) V_{DDA18} includes current into V_{DD1A18} and V_{DD2A18}. $V_{DDA3.3}$ includes current into V_{DDA2} and V_{DDAIO}.



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}):	**1 kΩ**
Sampling Capacitor (C_h):	**1.64 pF**
Parasitic Capacitance (C_p):	**10 pF**
Source Resistance (R_s):	**50 Ω**

Figure 5-21. ADC Analog Input Impedance Model

5.10.2 Definitions

Reference Voltage

The on-chip ADC has a built-in reference, which provides the reference voltages for the ADC.

Analog Inputs

The on-chip ADC consists of 16 analog inputs, which are sampled either one at a time or two channels at a time. These inputs are software-selectable.

Converter

The on-chip ADC uses a 12-bit four-stage pipeline architecture, which achieves a high sample rate with low power consumption.

Conversion Modes

The conversion can be performed in two different conversion modes:

- Sequential sampling mode (SMODE = 0)
- Simultaneous sampling mode (SMODE = 1)

5.10.3 Sequential Sampling Mode (Single-Channel) (SMODE = 0)

In sequential sampling mode, the ADC can continuously convert input signals on any of the channels (Ax to Bx). The ADC can start conversions on event triggers from the ePWM, software trigger, or from an external ADCSOC signal. If the SMODE bit is 0, the ADC will do conversions on the selected channel on every Sample/Hold pulse. The conversion time and latency of the Result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update. The selected channels will be sampled at every falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

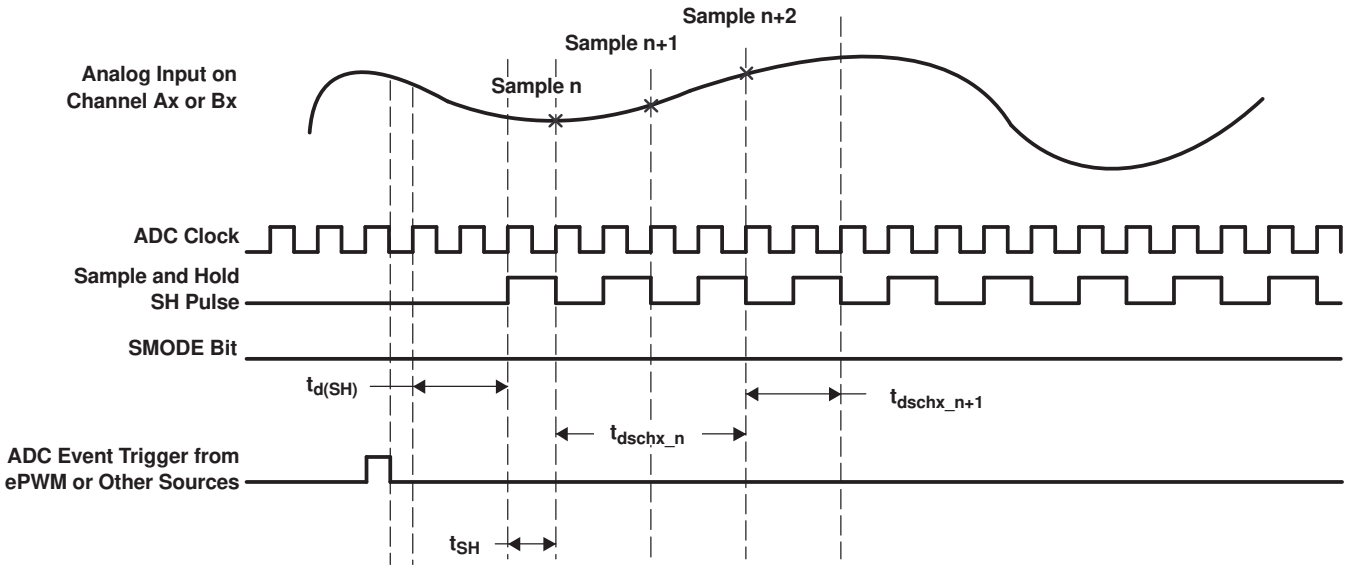


Figure 5-22. Sequential Sampling Mode (Single-Channel) Timing

Table 5-38. Sequential Sampling Mode Timing

		SAMPLE n	SAMPLE n + 1	AT 25-MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 40 ns	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	$2.5t_{c(ADCCLK)}$			
t_{SH}	Sample/Hold width/Acquisition Width	(1 + Acqps) * $t_{c(ADCCLK)}$		40 ns with Acqps = 0	Acqps value = 0–15 ADCTRL1[8:11]
$t_{d(schx\_n)}$	Delay time for first result to appear in Result register	$4t_{c(ADCCLK)}$		160 ns	
$t_{d(schx\_n+1)}$	Delay time for successive results to appear in Result register		(2 + Acqps) * $t_{c(ADCCLK)}$	80 ns	

5.10.4 Simultaneous Sampling Mode (Dual-Channel) (SMODE = 1)

In simultaneous mode, the ADC can continuously convert input signals on any one pair of channels (A0/B0 to A7/B7). The ADC can start conversions on event triggers from the ePWM, software trigger, or from an external ADCSOC signal. If the SMODE bit is 1, the ADC will do conversions on two selected channels on every Sample/Hold pulse. The conversion time and latency of the result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update. The selected channels will be sampled simultaneously at the falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

NOTE

In simultaneous mode, the ADCIN channel pair select has to be A0/B0, A1/B1, ..., A7/B7, and not in other combinations (such as A1/B3, etc.).

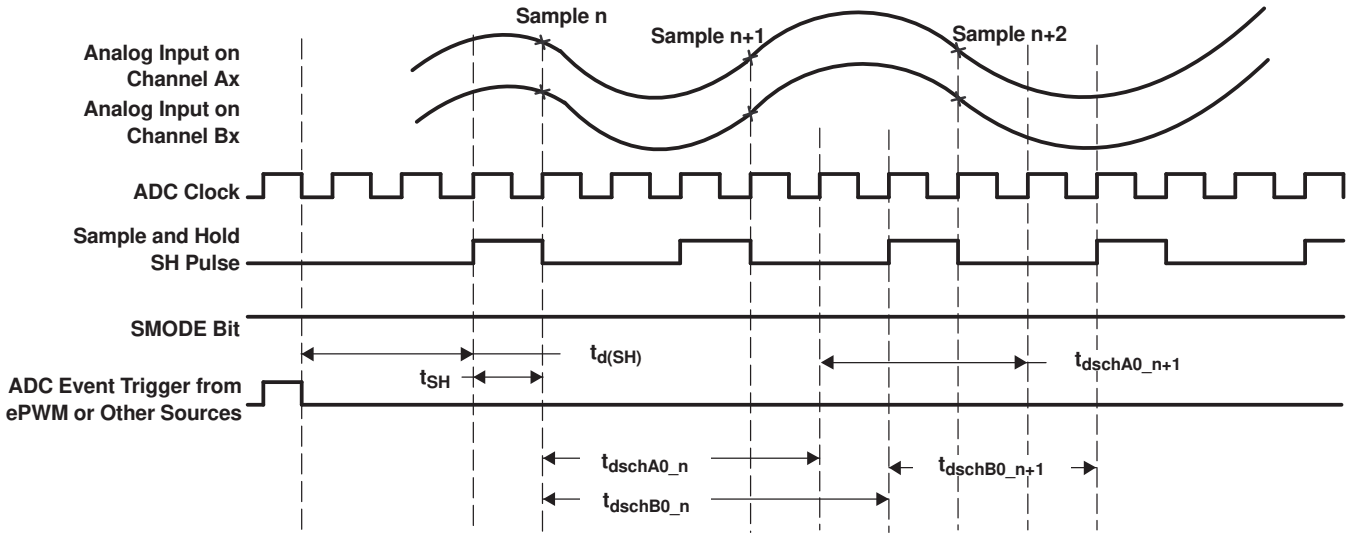


Figure 5-23. Simultaneous Sampling Mode Timing

Table 5-39. Simultaneous Sampling Mode Timing

		SAMPLE n	SAMPLE n + 1	AT 25-MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 40 ns	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	$2.5t_{c(ADCCLK)}$			
t_{SH}	Sample/Hold width/Acquisition Width	(1 + Acqps) * $t_{c(ADCCLK)}$		40 ns with Acqps = 0	Acqps value = 0–15 ADCTRL1[8:11]
$t_{d(schA0\_n)}$	Delay time for first result to appear in Result register	$4t_{c(ADCCLK)}$		160 ns	
$t_{d(schB0\_n)}$	Delay time for first result to appear in Result register	$5t_{c(ADCCLK)}$		200 ns	
$t_{d(schA0\_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) * $t_{c(ADCCLK)}$	120 ns	
$t_{d(schB0\_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) * $t_{c(ADCCLK)}$	120 ns	

5.10.5 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, $N = \frac{(SINAD - 1.76)}{6.02}$ it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

6 Detailed Description

6.1 Brief Descriptions

6.1.1 C28x CPU

The C28x DSP generation is the newest member of the TMS320C2000™ DSP platform. The C28x is a very efficient C/C++ engine, hence enabling users to develop not only their system control software in a high-level language, but also enables math algorithms to be developed using C/C++. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive floating-point processor solution. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

6.1.2 Memory Bus (Harvard Bus Architecture)

As with many DSP type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed "Harvard Bus", enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus will prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

6.1.3 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) DSP family of devices, the F28044 device adopts a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Two versions of the peripheral bus are supported on the F28044. One version only supports 16-bit accesses (called peripheral frame 2). The other version supports both 16-bit and 32-bit accesses (called peripheral frame 1).

6.1.4 Real-Time JTAG and Analysis

The F28044 device implements the standard IEEE 1149.1 JTAG interface. Additionally, the device supports real-time mode of operation whereby the contents of memory, peripheral and register locations can be modified while the processor is running and executing code and servicing interrupts. The user can also single step through non-time critical code while enabling time-critical interrupts to be serviced without interference. The F28044 implements the real-time mode in hardware within the CPU. This is a unique feature to the F28044, no software monitor is required. Additionally, special analysis hardware is provided which allows the user to set hardware breakpoint or data/address watch-points and generate various user-selectable break events when a match occurs.

6.1.5 Flash

The F28044 contains 64K x 16 of embedded flash memory, segregated into four 16K x 16 sectors. Both devices also contain a single 1K x 16 of OTP memory at address range 0x3D 7800 – 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Note that addresses 0x3F7FF0 – 0x3F7FF5 are reserved for data variables and should not contain program code.

NOTE

The F28044 Flash and OTP wait-states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait-states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the *TMS320x280x, 2801x, 2804x DSP System Control and Interrupts Reference Guide*.

6.1.6 M0, M1 SARAMs

The F28044 device contains these two blocks (M0/M1) of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

6.1.7 L0, L1 SARAMs

The F28044 device contains an additional 8K x 16 of single-access RAM, divided into 2 blocks (L0-4K, L1-4K). Each block can be independently accessed to minimize CPU pipeline stalls. Each block is mapped to both program and data space.

6.1.8 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math related algorithms.

Table 6-1. Boot Mode Selection

MODE	DESCRIPTION	GPIO18 SPICLKA	GPIO29 SCITXDA	GPIO34
Boot to Flash/ROM	Jump to Flash/ROM address 0x3F 7FF6 You must have programmed a branch instruction here prior to reset to redirect code execution as desired.	1	1	1
SCI-A Boot	Load a data stream from SCI-A	1	1	0
SPI-A Boot	Load from an external serial SPI EEPROM on SPI-A	1	0	1
I^2C Boot	Load data from an external EEPROM at address 0x50 on the I^2C bus	1	0	0
eCAN-A Boot	Reserved. This mode should not be used.	0	1	1
Boot to M0 SARAM	Jump to M0 SARAM address 0x00 0000.	0	1	0
Boot to OTP	Jump to OTP address 0x3D 7800	0	0	1
Parallel I/O Boot	Load data from GPIO0–GPIO15	0	0	0

6.1.9 Security

The device supports high levels of security to protect the user firmware from being reverse engineered. The security features a 128-bit password (hardcoded for 16 wait-states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit "KEY" value, which matches the value stored in the password locations within the Flash.

NOTE

For code security operation, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data, but must be programmed to 0x0000 when the Code Security Password is programmed. If security is not a concern, addresses 0x3F7F80 through 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 – 0x3F7FF5 are reserved for data variables and should not contain program code.

The 128-bit password (at 0x3F 7FF8 – 0x3F 7FFF) ***must not*** be programmed to zeros. Doing so would permanently lock the device.

DISCLAIMER

Code Security Module Disclaimer

THE CODE SECURITY MODULE ("CSM") INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

6.1.10 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F28044 device, 43 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

6.1.11 External Interrupts (XINT1, XINT2, XNMI)

The F28044 device supports three masked external interrupts (XINT1, XINT2, XNMI). XNMI can be connected to the INT13 or NMI interrupt of the CPU. Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled/disabled (including the XNMI). The masked interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. Unlike the 281x devices, there are no dedicated pins for the external interrupts. Rather, any Port A GPIO pin can be configured to trigger any external interrupt.

6.1.12 Oscillator and PLL

The F28044 device can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 10 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to the Specifications section for timing details. The PLL block can be set in bypass mode.

6.1.13 Watchdog

The F28044 device contains a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise, the watchdog will generate a reset to the processor. The watchdog can be disabled if necessary.

6.1.14 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled so as to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I^2C) and the ADC blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

6.1.15 Low-Power Modes

The F28044 device is full static CMOS devices. Three low-power modes are provided:

- IDLE: Place CPU into low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
- STANDBY: Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
- HALT: Turns off the internal oscillator. This mode basically shuts down the device and places it in the lowest possible power consumption mode. A reset or external signal can wake the device from this mode.

6.1.16 Peripheral Frames 0, 1, 2 (PFn)

The F28044 device segregates peripherals into three sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Control, Programming, Erase, Verify Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result Registers (dual-mapped)
PF1:	GPIO:	GPIO MUX Configuration and Control Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers
PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Result Register
	I^2C:	Inter-Integrated Circuit Module and Registers

6.1.17 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

6.1.18 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is reserved for the SYS/BIOS Real-Time OS, and is connected to INT14 of the CPU. If SYS/BIOS is not being used, CPU-Timer 2 is available for general use. CPU-Timer 1 is for general use and can be connected to INT13 of the CPU. CPU-Timer 0 is also for general use and is connected to the PIE block.

6.1.19 Control Peripherals

The F28044 device supports the following peripherals which are used for embedded control and communication:

ePWM:	The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support HRPWM features.
ADC:	The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

6.1.20 Serial Port Peripherals

The F28044 device supports the following serial communication peripherals:

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. On the F28044 device, the SPI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. On the F28044 device, the SCI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

I^2C: The inter-integrated circuit (I^2C) module provides an interface between a DSP and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSP through the I^2C module. On the F28044 device, the I^2C contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

6.2 Peripherals

The integrated peripherals of the F28044 device are described in the following subsections:

- Three 32-bit CPU-Timers
- Up to 16 enhanced PWM modules (ePWM1–16)
- Enhanced analog-to-digital converter (ADC) module
- Serial communications interface module (SCI-A)
- Serial peripheral interface (SPI) module (SPI-A)
- Inter-integrated circuit module (I^2C)
- Digital I/O and shared pin functions

6.2.1 32-Bit CPU-Timers 0/1/2

There are three 32-bit CPU-timers on the F28044 device (CPU-TIMER0/1/2).

CPU-Timer 0 and CPU-Timer 1 can be used in user applications. Timer 2 is reserved for SYS/BIOS. These timers are different from the timers that are present in the ePWM modules.

NOTE

If the application is not using SYS/BIOS, then CPU-Timer 2 can be used in the application.

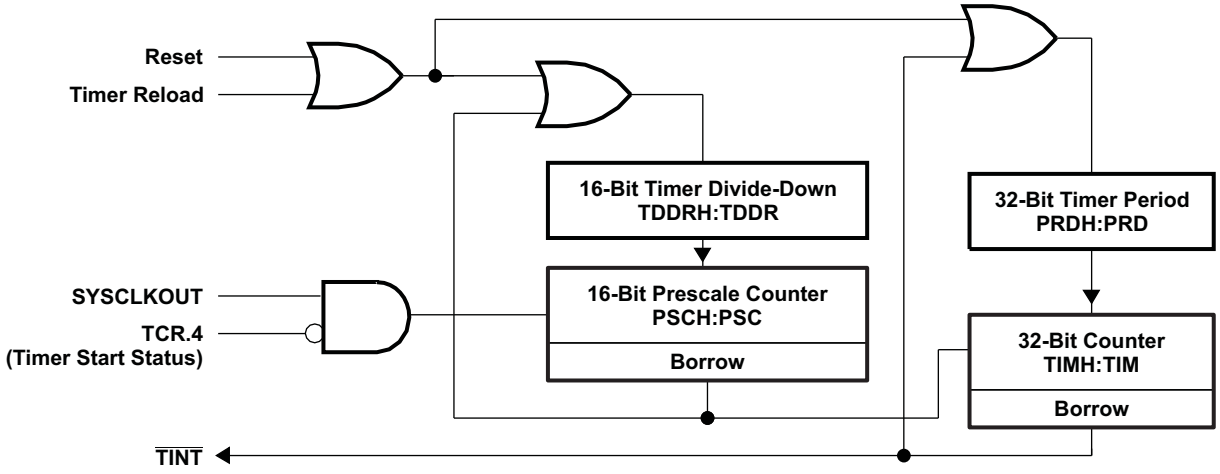
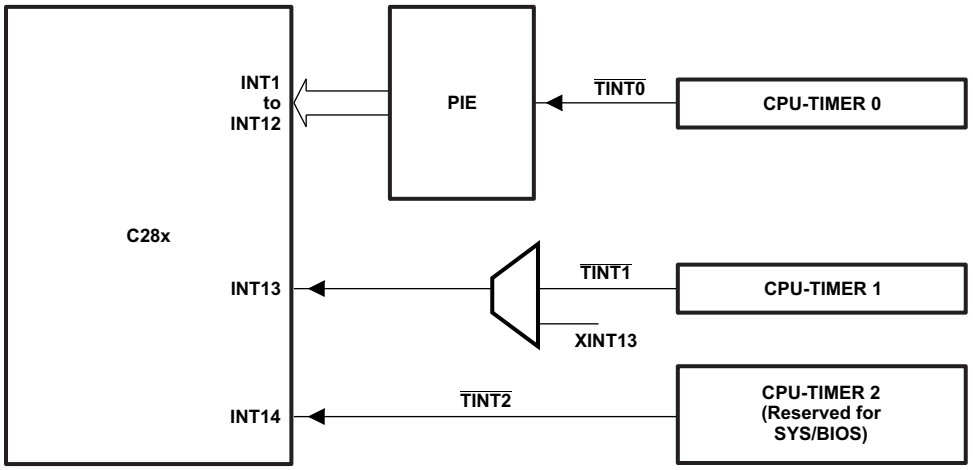


Figure 6-1. CPU-Timers

In the F28044 device, the timer interrupt signals ($\overline{\text{TINT0}}$, $\overline{\text{TINT1}}$, $\overline{\text{TINT2}}$) are connected as shown in Figure 6-2.



A. The timer registers are connected to the memory bus of the C28x processor.
B. The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

Figure 6-2. CPU-Timer Interrupt Signals and Output Signal

The general operation of the timer is as follows: The 32-bit counter register "TIMH:TIM" is loaded with the value in the period register "PRDH:PRD". The counter register decrements at the SYSCLKOUT rate of the C28x. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed in Table 6-2 are used to configure the timers. For more information, see the *TMS320x280x, 2801x, 2804x DSP System Control and Interrupts Reference Guide*.

Table 6-2. CPU-Timers 0, 1, 2 Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER0TIM	0x0C00	1	CPU-Timer 0, Counter Register
TIMER0TIMH	0x0C01	1	CPU-Timer 0, Counter Register High
TIMER0PRD	0x0C02	1	CPU-Timer 0, Period Register
TIMER0PRDH	0x0C03	1	CPU-Timer 0, Period Register High
TIMER0TCR	0x0C04	1	CPU-Timer 0, Control Register
Reserved	0x0C05	1	Reserved
TIMER0TPR	0x0C06	1	CPU-Timer 0, Prescale Register
TIMER0TPRH	0x0C07	1	CPU-Timer 0, Prescale Register High
TIMER1TIM	0x0C08	1	CPU-Timer 1, Counter Register
TIMER1TIMH	0x0C09	1	CPU-Timer 1, Counter Register High
TIMER1PRD	0x0C0A	1	CPU-Timer 1, Period Register
TIMER1PRDH	0x0C0B	1	CPU-Timer 1, Period Register High
TIMER1TCR	0x0C0C	1	CPU-Timer 1, Control Register
Reserved	0x0C0D	1	Reserved
TIMER1TPR	0x0C0E	1	CPU-Timer 1, Prescale Register
TIMER1TPRH	0x0C0F	1	CPU-Timer 1, Prescale Register High
TIMER2TIM	0x0C10	1	CPU-Timer 2, Counter Register
TIMER2TIMH	0x0C11	1	CPU-Timer 2, Counter Register High
TIMER2PRD	0x0C12	1	CPU-Timer 2, Period Register
TIMER2PRDH	0x0C13	1	CPU-Timer 2, Period Register High
TIMER2TCR	0x0C14	1	CPU-Timer 2, Control Register
Reserved	0x0C15	1	Reserved

Table 6-2. CPU-Timers 0, 1, 2 Configuration and Control Registers (continued)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER2TPR	0x0C16	1	CPU-Timer 2, Prescale Register
TIMER2TPRH	0x0C17	1	CPU-Timer 2, Prescale Register High
Reserved	0x0C18 – 0x0C3F	40	Reserved

6.2.2 Enhanced PWM Modules (ePWM1–16)

The F28044 device contains up to 16 enhanced PWM modules (ePWM). Figure 6-3 shows a block diagram of multiple ePWM modules. Figure 6-4 shows the signal interconnections with the ePWM. See the *TMS320x280x, 2801x, 2804x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* for details.

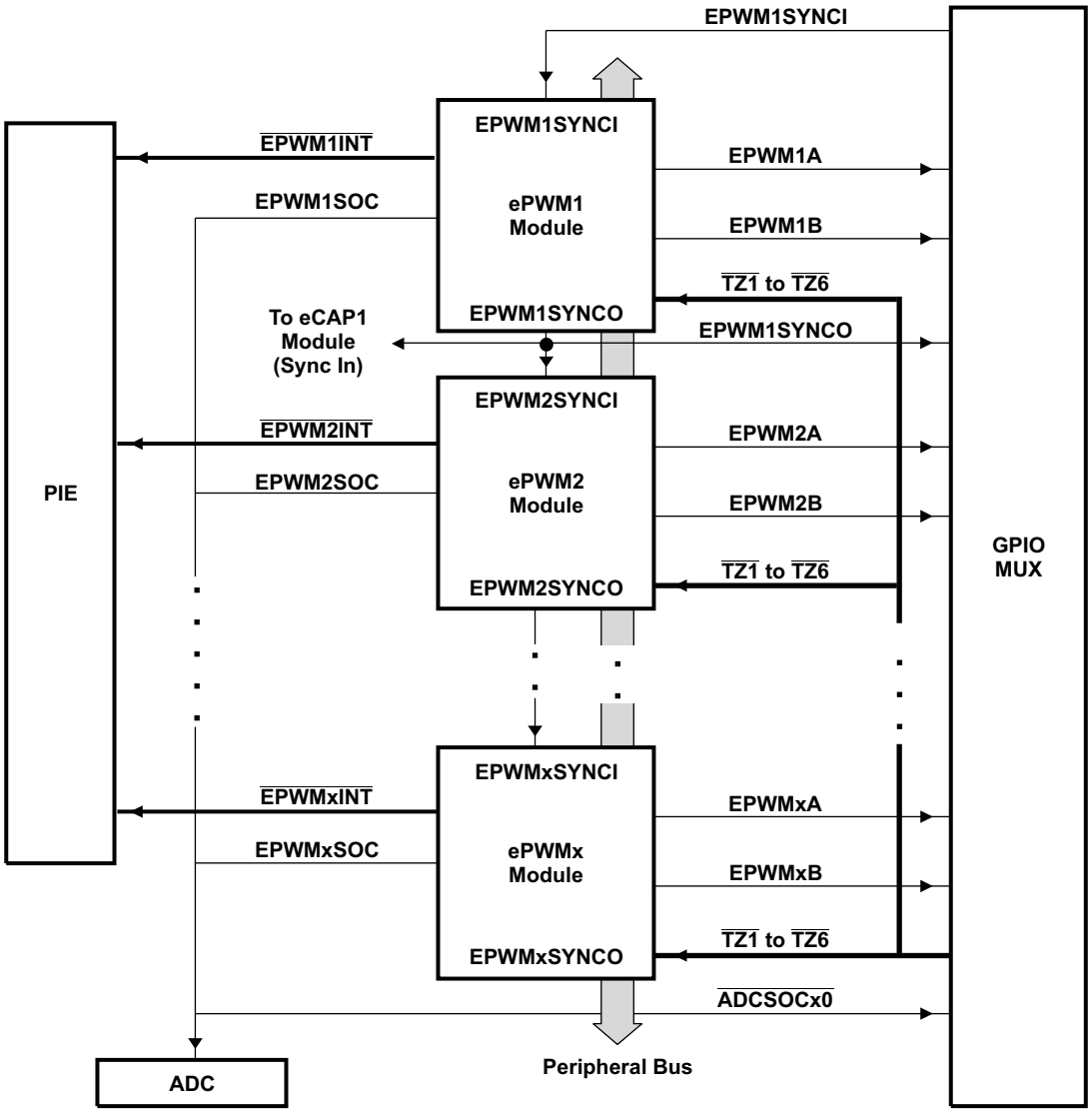


Figure 6-3. Multiple PWM Modules

The F28044 device contains 16 enhanced PWM modules (ePWM) and 16 high resolution PWM modules (HRPWM). The ePWM modules synchronize input/output and the ADC start of conversion (SOCA/B) signals are regrouped in the F28044. At reset, EPWMMODE bits in the GPAMCFG register configure the sync signals to be compatible to the TMS320F2808 device. In F28044 mode, the ePWMMODE bits are set to 11 to select the EPWMA signals on all 16 GPIOs (GPIO0–GPIO15). This mode selection also reconfigures the EPWM1 SYNCOUT to be connected to four groups of ePWM modules and as EPWMSYNCO signals on the pin:

- Group 1: ePWM2, ePWM3, ePWM4
- Group 2: ePWM5, ePWM6, ePWM7, ePWM8
- Group 3: ePWM9, ePWM10, ePWM11, ePWM12
- Group 4: ePWM13, ePWM14, ePWM15, ePWM16

See the *TMS320x280x, 2801x, 2804x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* for additional details.

Table 6-3 through Table 6-6 show the complete ePWM register set per module.

Table 6-3. ePWM1–4 Control and Status Registers

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	1 / 0	Time Base Status Register
TBPHSHR	0x6802	0x6842	0x6882	0x68C2	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	1 / 0	Time Base Phase Register
TBCTR	0x6804	0x6844	0x6884	0x68C4	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	1 / 1	Time Base Period Register Set
CMPCTL	0x6807	0x6847	0x6887	0x68C7	1 / 0	Counter Compare Control Register
CMPAHR	0x6808	0x6848	0x6888	0x68C8	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6809	0x6849	0x6889	0x68C9	1 / 1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	1 / 0	Trip Zone Select Register(1)
TZCTL	0x6814	0x6854	0x6894	0x68D4	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6815	0x6855	0x6895	0x68D5	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6816	0x6856	0x6896	0x68D6	1 / 0	Trip Zone Flag Register
TZCLR	0x6817	0x6857	0x6897	0x68D7	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6818	0x6858	0x6898	0x68D8	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6819	0x6859	0x6899	0x68D9	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	1 / 0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	1 / 0	PWM Chopper Control Register
HRCNFG	0x6820	0x6860	0x68A0	0x68E0	1 / 0	HRPWM Configuration Register(1)

(1) Registers that are EALLOW protected.

Table 6-4. ePWM5–8 Control and Status Registers

NAME	ePWM5	ePWM6	ePWM7	ePWM8	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6900	0x6940	0x6980	0x69C0	1 / 0	Time Base Control Register
TBSTS	0x6901	0x6941	0x6981	0x69C1	1 / 0	Time Base Status Register
TBPHSHR	0x6902	0x6942	0x6982	0x69C2	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6903	0x6943	0x6983	0x69C3	1 / 0	Time Base Phase Register
TBCTR	0x6904	0x6944	0x6984	0x69C4	1 / 0	Time Base Counter Register
TBPRD	0x6905	0x6945	0x6985	0x69C5	1 / 1	Time Base Period Register Set
CMPCTL	0x6907	0x6947	0x6987	0x69C7	1 / 0	Counter Compare Control Register
CMPAHR	0x6908	0x6948	0x6988	0x69C8	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6909	0x6949	0x6989	0x69C9	1 / 1	Counter Compare A Register Set
CMPB	0x690A	0x694A	0x698A	0x69CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x690B	0x694B	0x698B	0x69CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x690C	0x694C	0x698C	0x69CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x690D	0x694D	0x698D	0x69CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x690E	0x694E	0x698E	0x69CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x690F	0x694F	0x698F	0x69CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6910	0x6950	0x6990	0x69D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6911	0x6951	0x6991	0x69D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6912	0x6952	0x6992	0x69D2	1 / 0	Trip Zone Select Register(1)
TZCTL	0x6914	0x6954	0x6994	0x69D4	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6915	0x6955	0x6995	0x69D5	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6916	0x6956	0x6996	0x69D6	1 / 0	Trip Zone Flag Register
TZCLR	0x6917	0x6957	0x6997	0x69D7	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6918	0x6958	0x6998	0x69D8	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6919	0x6959	0x6999	0x69D9	1 / 0	Event Trigger Selection Register
ETPS	0x691A	0x695A	0x699A	0x69DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x691B	0x695B	0x699B	0x69DB	1 / 0	Event Trigger Flag Register
ETCLR	0x691C	0x695C	0x699C	0x69DC	1 / 0	Event Trigger Clear Register
ETFRC	0x691D	0x695D	0x699D	0x69DD	1 / 0	Event Trigger Force Register
PCCTL	0x691E	0x695E	0x699E	0x69DE	1 / 0	PWM Chopper Control Register
HRCNFG	0x6920	0x6960	0x69A0	0x69E0	1 / 0	HRPWM Configuration Register(1)

(1) Registers that are EALLOW protected.

Table 6-5. ePWM9–12 Control and Status Registers

NAME	ePWM9	ePWM10	ePWM11	ePWM12	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6600	0x6640	0x6680	0x66C0	1 / 0	Time Base Control Register
TBSTS	0x6601	0x6641	0x6681	0x66C1	1 / 0	Time Base Status Register
TBPHSHR	0x6602	0x6642	0x6682	0x66C2	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6603	0x6643	0x6683	0x66C3	1 / 0	Time Base Phase Register
TBCTR	0x6604	0x6644	0x6684	0x66C4	1 / 0	Time Base Counter Register
TBPRD	0x6605	0x6645	0x6685	0x66C5	1 / 1	Time Base Period Register Set
CMPCTL	0x6607	0x6647	0x6687	0x66C7	1 / 0	Counter Compare Control Register
CMPAHR	0x6608	0x6648	0x6688	0x66C8	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6609	0x6649	0x6689	0x66C9	1 / 1	Counter Compare A Register Set
CMPB	0x660A	0x664A	0x668A	0x66CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x660B	0x664B	0x668B	0x66CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x660C	0x664C	0x668C	0x66CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x660D	0x664D	0x668D	0x66CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x660E	0x664E	0x668E	0x66CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x660F	0x664F	0x668F	0x66CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6610	0x6650	0x6690	0x66D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6611	0x6651	0x6691	0x66D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6612	0x6652	0x6692	0x66D2	1 / 0	Trip Zone Select Register(1)
TZCTL	0x6614	0x6654	0x6694	0x66D4	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6615	0x6655	0x6695	0x66D5	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6616	0x6656	0x6696	0x66D6	1 / 0	Trip Zone Flag Register
TZCLR	0x6617	0x6657	0x6697	0x66D7	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6618	0x6658	0x6698	0x66D8	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6619	0x6659	0x6699	0x66D9	1 / 0	Event Trigger Selection Register
ETPS	0x661A	0x665A	0x669A	0x66DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x661B	0x665B	0x669B	0x66DB	1 / 0	Event Trigger Flag Register
ETCLR	0x661C	0x665C	0x669C	0x66DC	1 / 0	Event Trigger Clear Register
ETFRC	0x661D	0x665D	0x669D	0x66DD	1 / 0	Event Trigger Force Register
PCCTL	0x661E	0x665E	0x669E	0x66DE	1 / 0	PWM Chopper Control Register
HRCNFG	0x6620	0x6660	0x66A0	0x66E0	1 / 0	HRPWM Configuration Register(1)

(1) Registers that are EALLOW protected.

Table 6-6. ePWM13–16 Control and Status Registers

NAME	ePWM13	ePWM14	ePWM15	ePWM16	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6700	0x6740	0x6780	0x67C0	1 / 0	Time Base Control Register
TBSTS	0x6701	0x6741	0x6781	0x67C1	1 / 0	Time Base Status Register
TBPHSHR	0x6702	0x6742	0x6782	0x67C2	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6703	0x6743	0x6783	0x67C3	1 / 0	Time Base Phase Register
TBCTR	0x6704	0x6744	0x6784	0x67C4	1 / 0	Time Base Counter Register
TBPRD	0x6705	0x6745	0x6785	0x67C5	1 / 1	Time Base Period Register Set
CMPCTL	0x6707	0x6747	0x6787	0x67C7	1 / 0	Counter Compare Control Register
CMPAHR	0x6708	0x6748	0x6788	0x67C8	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6709	0x6749	0x6789	0x67C9	1 / 1	Counter Compare A Register Set
CMPB	0x670A	0x674A	0x678A	0x67CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x670B	0x674B	0x678B	0x67CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x670C	0x674C	0x678C	0x67CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x670D	0x674D	0x678D	0x67CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x670E	0x674E	0x678E	0x67CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x670F	0x674F	0x678F	0x67CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6710	0x6750	0x6790	0x67D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6711	0x6751	0x6791	0x67D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6712	0x6752	0x6792	0x67D2	1 / 0	Trip Zone Select Register(1)
TZCTL	0x6714	0x6754	0x6794	0x67D4	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6715	0x6755	0x6795	0x67D5	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6716	0x6756	0x6796	0x67D6	1 / 0	Trip Zone Flag Register
TZCLR	0x6717	0x6757	0x6797	0x67D7	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6718	0x6758	0x6798	0x67D8	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6719	0x6759	0x6799	0x67D9	1 / 0	Event Trigger Selection Register
ETPS	0x671A	0x675A	0x679A	0x67DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x671B	0x675B	0x679B	0x67DB	1 / 0	Event Trigger Flag Register
ETCLR	0x671C	0x675C	0x679C	0x67DC	1 / 0	Event Trigger Clear Register
ETFRC	0x671D	0x675D	0x679D	0x67DD	1 / 0	Event Trigger Force Register
PCCTL	0x671E	0x675E	0x679E	0x67DE	1 / 0	PWM Chopper Control Register
HRCNFG	0x6720	0x6760	0x67A0	0x67E0	1 / 0	HRPWM Configuration Register(1)

(1) Registers that are EALLOW protected.

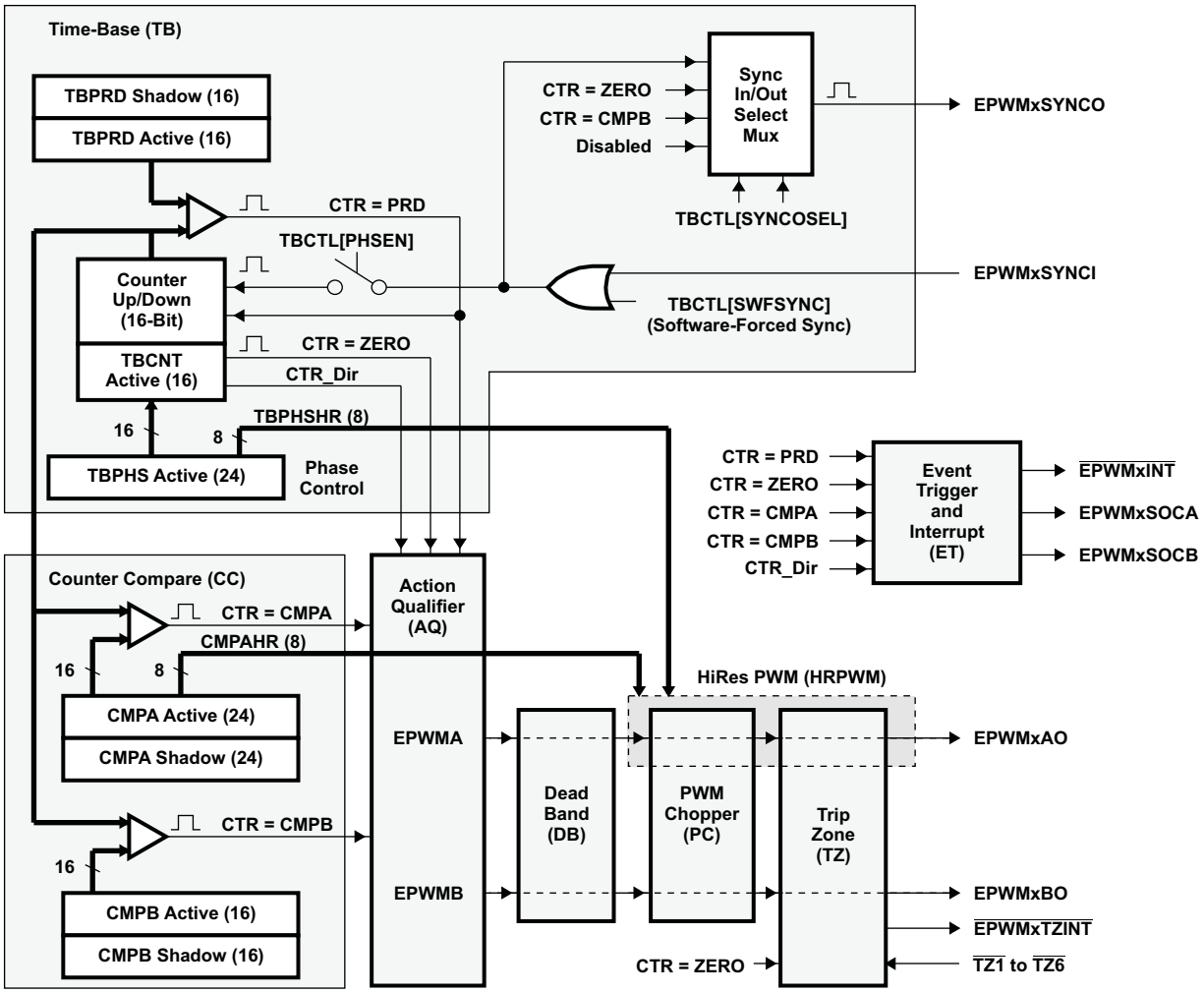


Figure 6-4. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

6.2.3 Hi-Resolution PWM (HRPWM)

The HRPWM module offers PWM resolution (time granularity) which is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- Typically used when effective PWM resolution falls below ~ 9–10 bits. This occurs at PWM frequencies greater than ~200 kHz when using a CPU/System clock of 100 MHz.
- This capability can be utilized in both duty cycle and phase-shift control methods.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities are offered only on the A signal path of an ePWM module (that is, on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

6.2.4 Enhanced Analog-to-Digital Converter (ADC) Module

A simplified functional block diagram of the ADC module is shown in Figure 6-5. The ADC module consists of a 12-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 12-bit ADC core with built-in S/H
- Analog input: 0.0 V to 3.0 V (Voltages above 3.0 V produce full-scale conversion results.)
- Fast conversion rate: 80 ns at 25-MHz ADC clock, 12.5 MSPS
- 16-channel, MUXed inputs
- Autosequencing capability provides up to 16 "autoconversions" in a single session. Each conversion can be programmed to select any 1 of 16 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (that is, two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  - The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 0 \quad \text{, when ADCIN} \leq \text{ADCLO}$$

$$\text{Digital Value} = \text{floor}\left(4096 \times \frac{\text{ADCIN} - \text{ADCLO}}{3}\right) \quad \text{, when ADCLO} < \text{ADCIN} < 3\ \text{V}$$

$$\text{Digital Value} = 4095 \quad \text{, when ADCIN} \geq 3\ \text{V}$$

- Multiple triggers as sources for the start-of-conversion (SOC) sequence
  - S/W - software immediate start
  - ePWM start of conversion
  - XINT2 ADC start of conversion
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS.
- Sequencer can operate in "start/stop" mode, allowing multiple "time-sequenced triggers" to synchronize conversions.
- SOCA and SOCB triggers can operate independently in dual-sequencer mode.
- Sample-and-hold (S/H) acquisition time window has separate prescale control.

The ADC module in the F28044 device has been enhanced to provide flexible interface to ePWM peripherals. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of 80 ns at 25-MHz ADC clock. The ADC module has 16 channels, configurable as two independent 8-channel modules. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 6-5 shows the block diagram of the ADC module.

The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog MUX. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

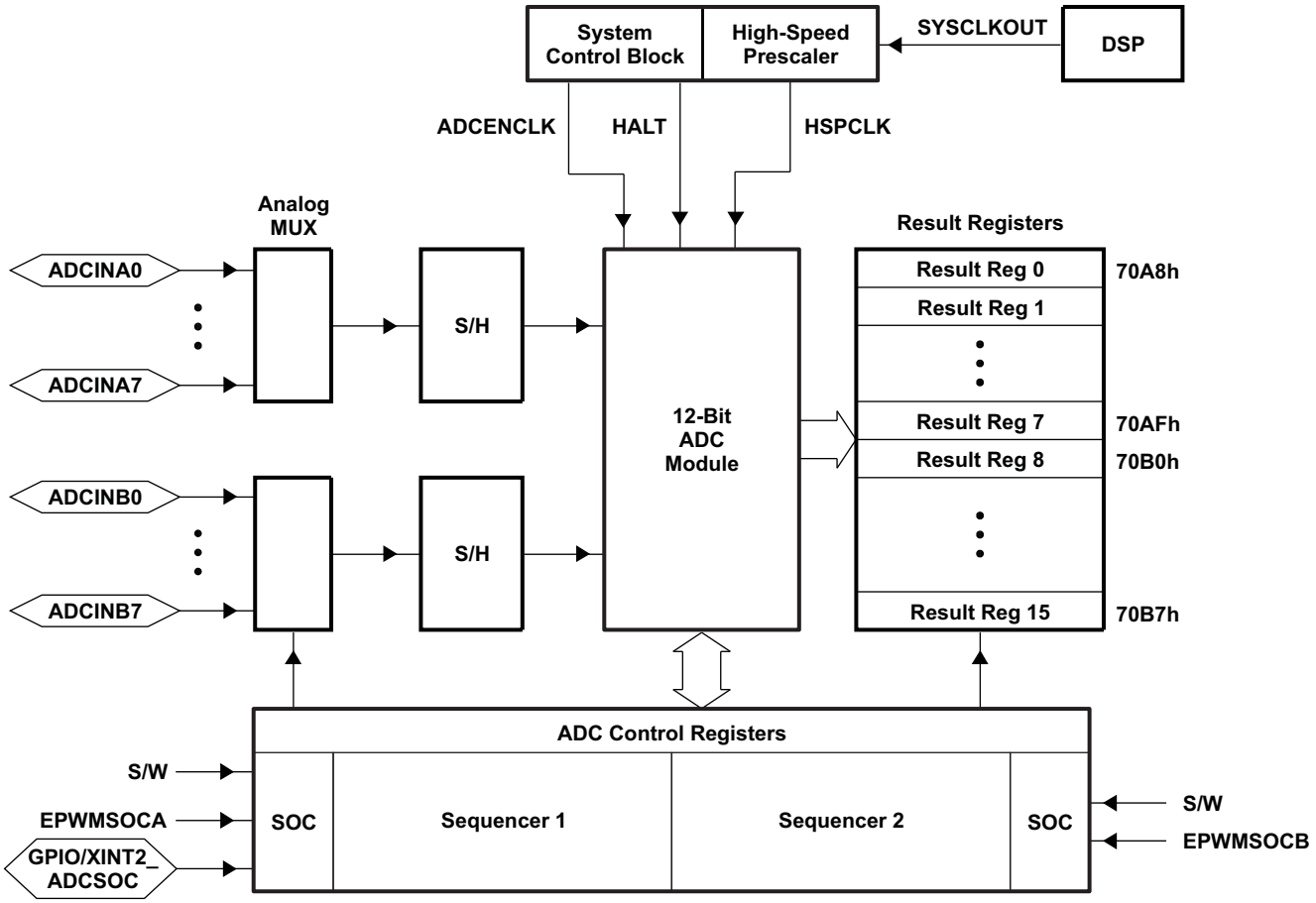


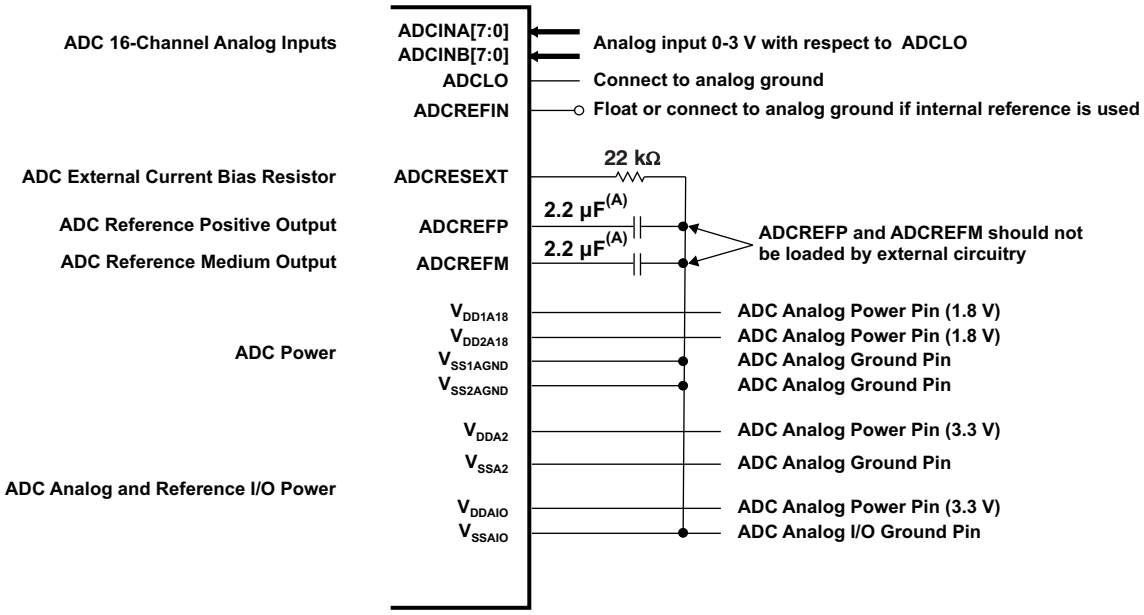
Figure 6-5. Block Diagram of the ADC Module

To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCIN pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (V_{DD1A18}, V_{DD2A18} , V_{DDA2}, V_{DDAIO}) from the digital supply. Figure 6-6 shows the ADC pin connections for the F28044 device.

NOTE

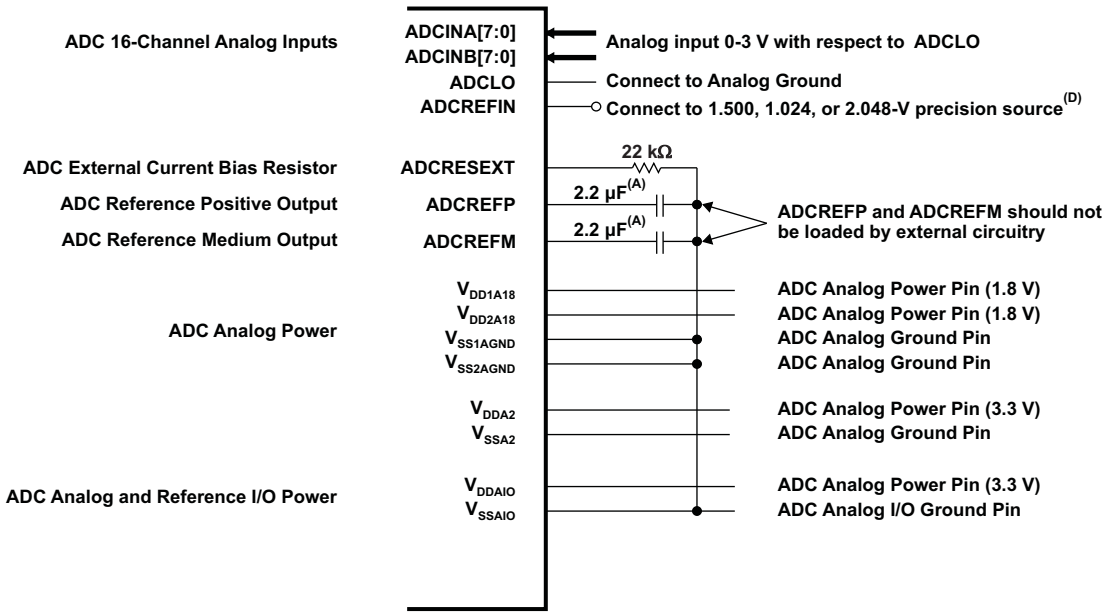
1. The ADC registers are accessed at the SYSCLKOUT rate. The internal timing of the ADC module is controlled by the high-speed peripheral clock (HSPCLK).
2. The behavior of the ADC module based on the state of the ADCENCLK and HALT signals is as follows:
   - *ADCENCLK:* On reset, this signal will be low. While reset is active-low ($\overline{XRS}$) the clock to the register will still function. This is necessary to make sure all registers and modes go into their default reset state. The analog module, however, will be in a low-power inactive state. As soon as reset goes high, then the clock to the registers will be disabled. When the user sets the ADCENCLK signal high, then the clocks to the registers will be enabled and the analog module will be enabled. There will be a certain time delay (ms range) before the ADC is stable and can be used.
   - *HALT:* This mode only affects the analog module. It does not affect the registers. In this mode, the ADC module goes into low-power mode. This mode also will stop the clock to the CPU, which will stop the HSPCLK; therefore, the ADC register logic will be turned off indirectly.

Figure 6-6 shows the ADC pin-biasing for internal reference and Figure 6-7 shows the ADC pin-biasing for external reference.



A. TAIYO YUDEN LMK212BJ225MG-T or equivalent
B. External decoupling capacitors are recommended on all power pins.
C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

Figure 6-6. ADC Pin Connections With Internal Reference



A. TAIYO YUDEN LMK212BJ225MG-T or equivalent
B. External decoupling capacitors are recommended on all power pins.
C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.
D. External voltage on ADCREFIN is enabled by changing bits 15:14 in the ADC Reference Select register depending on the voltage used on this pin. TI recommends TI part REF3020 or equivalent for 2.048-V generation. Overall gain accuracy will be determined by accuracy of this voltage source.

Figure 6-7. ADC Pin Connections With External Reference

NOTE

The temperature rating of any recommended component must match the rating of the end product.

6.2.4.1 ADC Connections if the ADC Is Not Used

It is recommended that the connections for the analog power pins be kept even if the ADC is not used. Following is a summary of how the ADC pins should be connected, if the ADC is not used in an application:

- V_{DD1A18}/V_{DD2A18} – Connect to V_{DD}
- V_{DDA2}, V_{DDAIO} – Connect to V_{DDIO}
- $V_{SS1AGND}$/$V_{SS2AGND}$, V_{SSA2}, V_{SSAIO} – Connect to V_{SS}
- ADCLO – Connect to V_{SS}
- ADCREFIN – Connect to V_{SS}
- ADCREFP/ADCREFM – Connect a 100 nF cap to V_{SS}
- ADCRESEXT – Connect a 20-kΩ resistor (very loose tolerance) to V_{SS}.
- ADCINAn, ADCINBn - Connect to V_{SS}

When the ADC is not used, be sure that the clock to the ADC module is not turned on to realize power savings.

When the ADC module is used in an application, unused ADC input pins should be connected to analog ground ($V_{SS1AGND}$/$V_{SS2AGND}$)

6.2.4.2 ADC Registers

The ADC operation is configured, controlled, and monitored by the registers listed in Table 6-7.

Table 6-7. ADC Registers(1)

NAME	ADDRESS(1)	ADDRESS(2)	SIZE (x16)	DESCRIPTION
ADCTRL1	0x7100		1	ADC Control Register 1
ADCTRL2	0x7101		1	ADC Control Register 2
ADCMAXCONV	0x7102		1	ADC Maximum Conversion Channels Register
ADCCHSELSEQ1	0x7103		1	ADC Channel Select Sequencing Control Register 1
ADCCHSELSEQ2	0x7104		1	ADC Channel Select Sequencing Control Register 2
ADCCHSELSEQ3	0x7105		1	ADC Channel Select Sequencing Control Register 3
ADCCHSELSEQ4	0x7106		1	ADC Channel Select Sequencing Control Register 4
ADCASEQSR	0x7107		1	ADC Auto-Sequence Status Register
ADCRESULT0	0x7108	0x0B00	1	ADC Conversion Result Buffer Register 0
ADCRESULT1	0x7109	0x0B01	1	ADC Conversion Result Buffer Register 1
ADCRESULT2	0x710A	0x0B02	1	ADC Conversion Result Buffer Register 2
ADCRESULT3	0x710B	0x0B03	1	ADC Conversion Result Buffer Register 3
ADCRESULT4	0x710C	0x0B04	1	ADC Conversion Result Buffer Register 4
ADCRESULT5	0x710D	0x0B05	1	ADC Conversion Result Buffer Register 5
ADCRESULT6	0x710E	0x0B06	1	ADC Conversion Result Buffer Register 6
ADCRESULT7	0x710F	0x0B07	1	ADC Conversion Result Buffer Register 7
ADCRESULT8	0x7110	0x0B08	1	ADC Conversion Result Buffer Register 8
ADCRESULT9	0x7111	0x0B09	1	ADC Conversion Result Buffer Register 9
ADCRESULT10	0x7112	0x0B0A	1	ADC Conversion Result Buffer Register 10
ADCRESULT11	0x7113	0x0B0B	1	ADC Conversion Result Buffer Register 11
ADCRESULT12	0x7114	0x0B0C	1	ADC Conversion Result Buffer Register 12
ADCRESULT13	0x7115	0x0B0D	1	ADC Conversion Result Buffer Register 13
ADCRESULT14	0x7116	0x0B0E	1	ADC Conversion Result Buffer Register 14
ADCRESULT15	0x7117	0x0B0F	1	ADC Conversion Result Buffer Register 15
ADCTRL3	0x7118		1	ADC Control Register 3
ADCST	0x7119		1	ADC Status Register
Reserved	0x711A – 0x711B		2	Reserved
ADCREFSEL	0x711C		1	ADC Reference Select Register
ADCOFFTRIM	0x711D		1	ADC Offset Trim Register
Reserved	0x711E – 0x711F		2	Reserved

(1) The registers in this column are Peripheral Frame 2 Registers.
(2) The ADC result registers are dual mapped in the F28044 DSP. Locations in Peripheral Frame 2 (0x7108–0x7117) are 2 wait-states and left justified. Locations in Peripheral frame 0 space (0x0B00–0x0B0F) are 0 wait sates and right justified. During high speed/continuous conversion use of the ADC, use the 0 wait-state locations for fast transfer of ADC results to user memory.

6.2.5 Serial Communications Interface (SCI) Module (SCI-A)

The F28044 device includes a serial communications interface (SCI) module. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \quad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- $\text{Max bit rate} = \frac{100\ \text{MHz}}{16} = 6.25 \times 10^6\ \text{b/s}$
- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 16-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 6-8.

Table 6-8. SCI-A Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRA	0x7050	1	SCI-A Communications Control Register
SCICTL1A	0x7051	1	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	SCI-A Control Register 2
SCIRXSTA	0x7055	1	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	SCI-A Transmit Data Buffer Register
SCIFFTXA(2)	0x705A	1	SCI-A FIFO Transmit Register
SCIFFRXA(2)	0x705B	1	SCI-A FIFO Receive Register
SCIFFCTA(2)	0x705C	1	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	SCI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Figure 6-8 shows the SCI module block diagram.

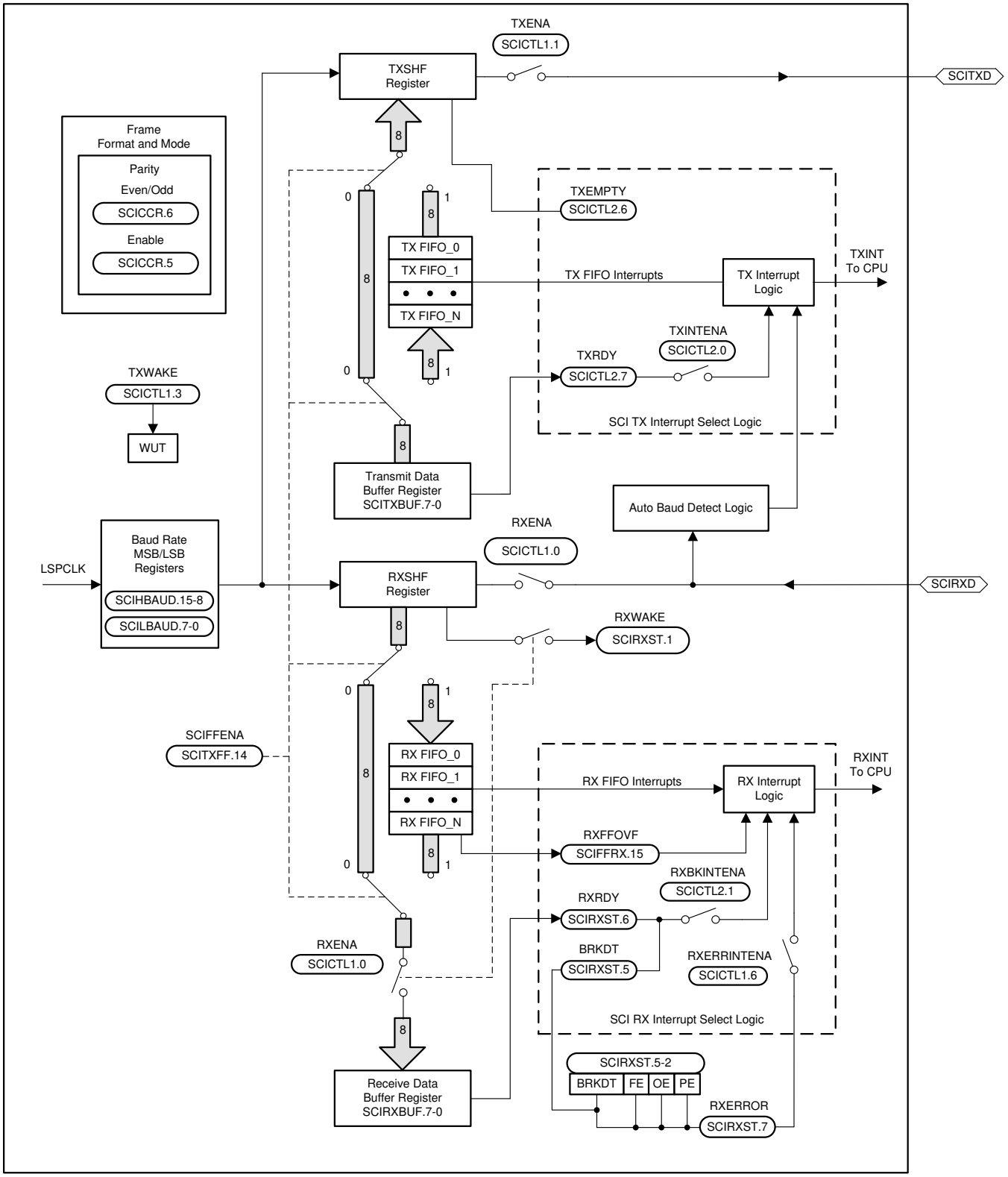


Figure 6-8. Serial Communications Interface (SCI) Module Block Diagram

6.2.6 Serial Peripheral Interface (SPI) Module (SPI-A)

The F28044 device includes the four-pin serial peripheral interface (SPI) module. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO, if the SPI module is not used.

- Two operational modes: master and slave

  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \quad \text{when SPIBRR = 3 to 127}$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \quad \text{when SPIBRR = 0,1, 2}$$

- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

NOTE

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 16-level transmit/receive FIFO
- Delayed transmit control

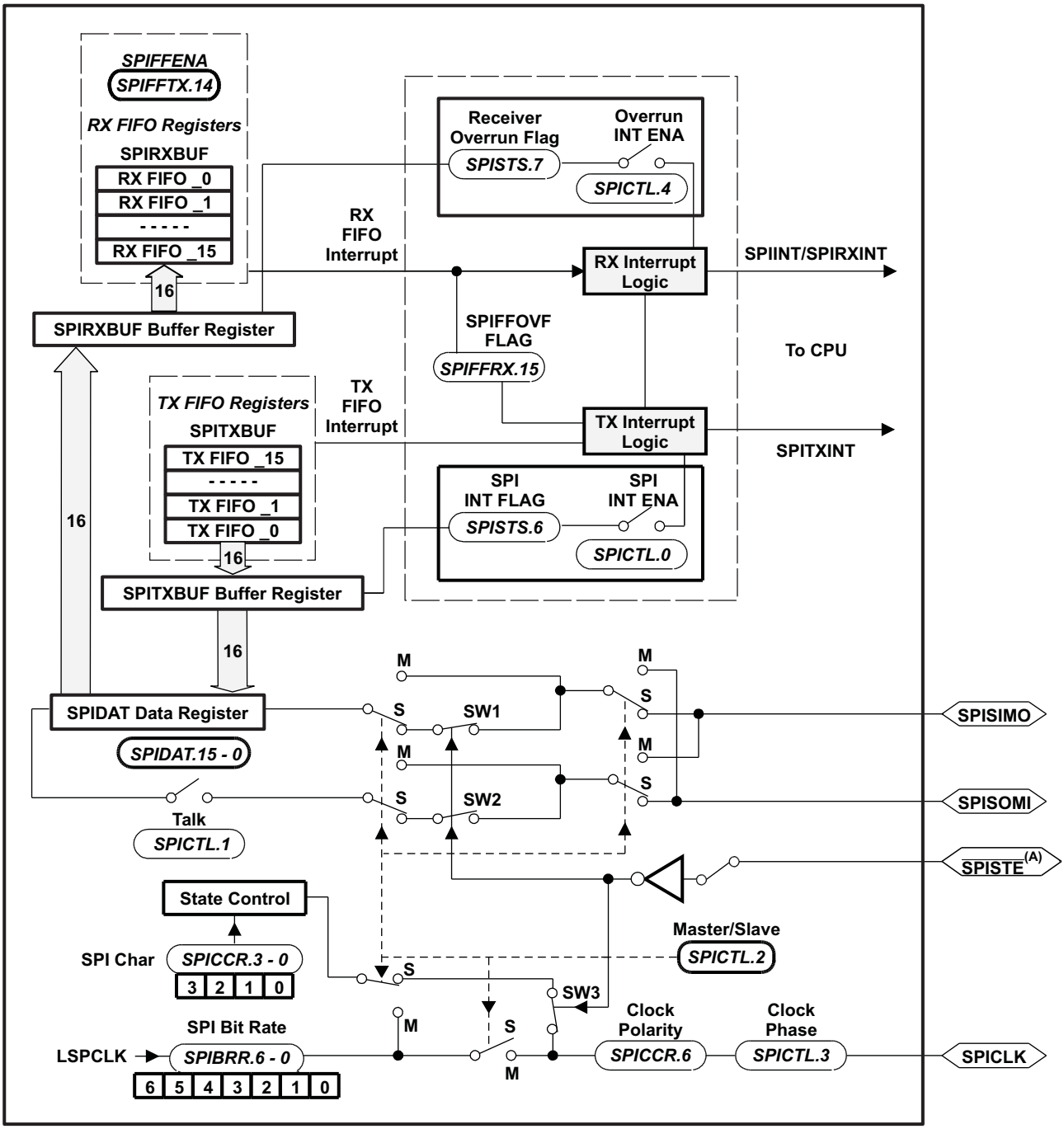
The SPI port operation is configured and controlled by the registers listed in Table 6-9.

Table 6-9. SPI-A Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
SPICCR	0x7040	1	SPI-A Configuration Control Register
SPICTL	0x7041	1	SPI-A Operation Control Register
SPISTS	0x7042	1	SPI-A Status Register
SPIBRR	0x7044	1	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	SPI-A Serial Data Register
SPIFFTX	0x704A	1	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	SPI-A FIFO Control Register
SPIPRI	0x704F	1	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 6-9 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

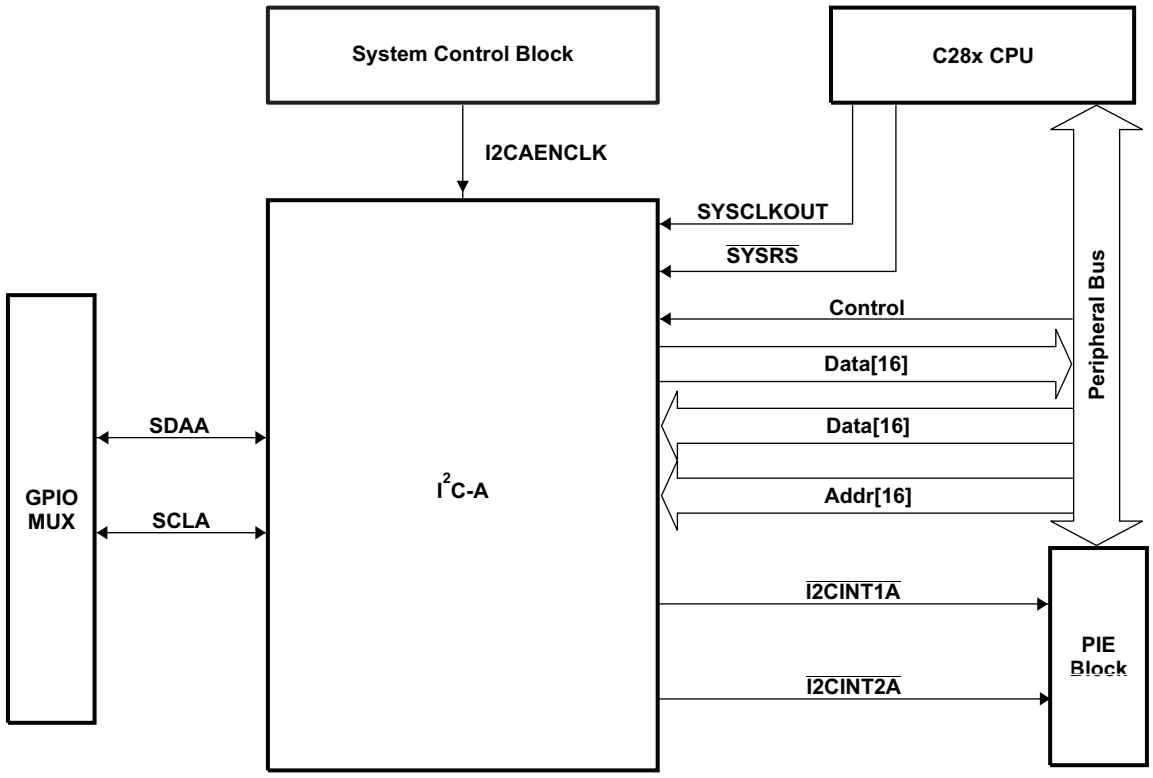
Figure 6-9. SPI Module Block Diagram (Slave Mode)

6.2.7 Inter-Integrated Circuit (I2C)

The F28044 device contains one I2C Serial Port. Figure 6-10 shows how the I2C peripheral module interfaces within the F28044 device.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 16-word receive FIFO and one 16-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode



A. The I2C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I2C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 6-10. I2C Peripheral Module Interfaces

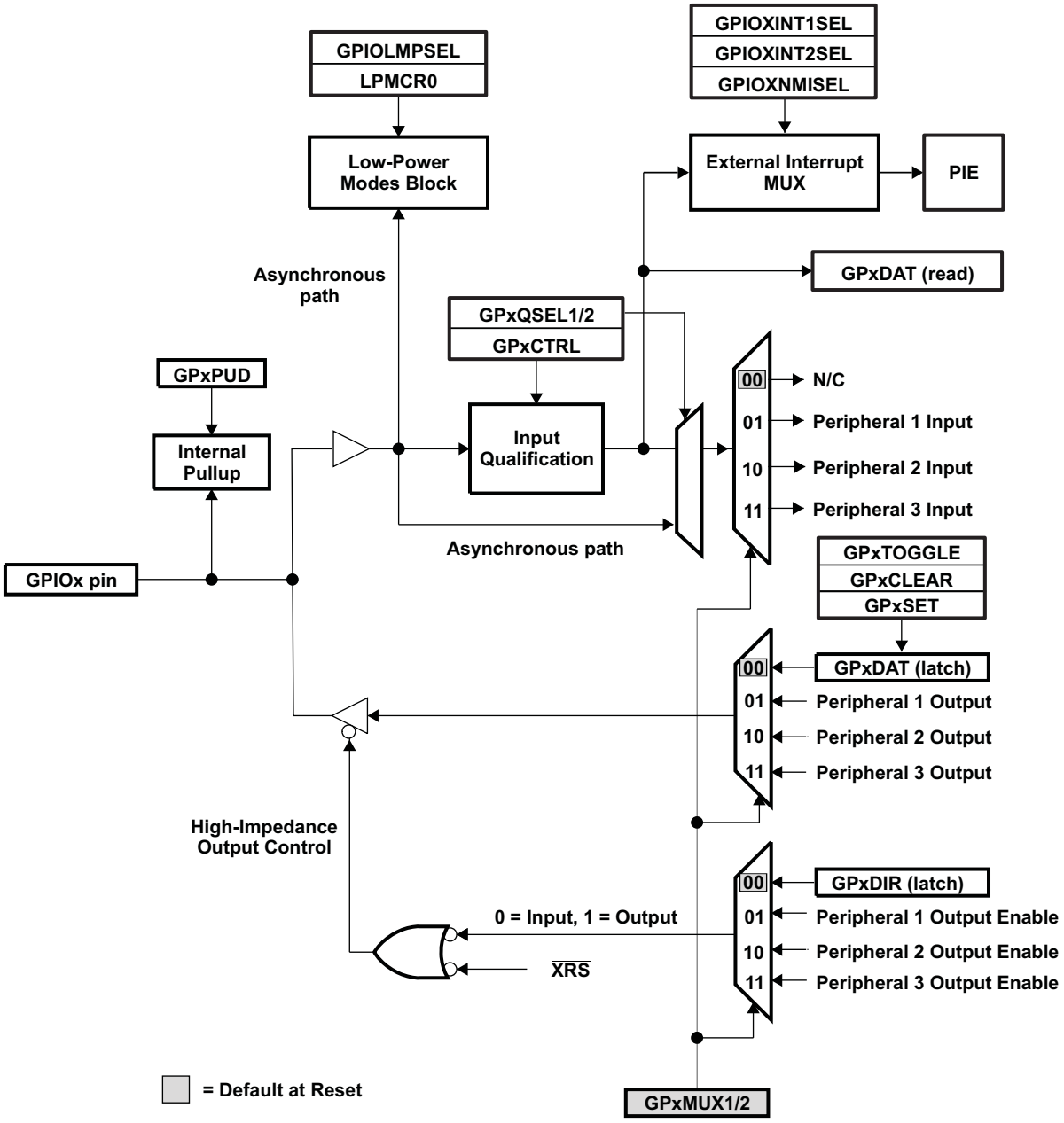
The registers in Table 6-10 configure and control the I2C port operation.

Table 6-10. I2C-A Registers

NAME	ADDRESS	DESCRIPTION
I2COAR	0x7900	I2C own address register
I2CIER	0x7901	I2C interrupt enable register
I2CSTR	0x7902	I2C status register
I2CCLKL	0x7903	IC clock low-time divider register
I2CCLKH	0x7904	I2C clock high-time divider register
I2CCNT	0x7905	I2C data count register
I2CDRR	0x7906	I2C data receive register
I2CSAR	0x7907	I2C slave address register
I2CDXR	0x7908	I2C data transmit register
I2CMDR	0x7909	I2C mode register
I2CISRC	0x790A	I2C interrupt source register
I2CPSC	0x790C	I2C prescaler register
I2CFFTX	0x7920	I2C FIFO transmit register
I2CFFRX	0x7921	I2C FIFO receive register
I2CRSR	-	I2C receive shift register (not accessible to the CPU)
I2CXSR	-	I2C transmit shift register (not accessible to the CPU)

6.2.8 GPIO MUX

On the 280x, the GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging IO capability. The GPIO MUX block diagram per pin is shown in Figure 6-11. Because of the open drain capabilities of the I2C pins, the GPIO MUX block diagram for these pins differ. See the *TMS320x280x, 2801x, 2804x DSP System Control and Interrupts Reference Guide* for details.



A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.

B. GPxDAT latch/read are accessed at the same memory location.

Figure 6-11. GPIO MUX Block Diagram

The F28044 supports 34 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 6-11 shows the GPIO register mapping.

Table 6-11. GPIO Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
GPAMCFG	0x6F8E	2	GPIO A Miscellaneous Configuration Register (GPIO0 to 31)
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 35)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 35)
GPBQSEL2	0x6F94	2	Reserved
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 35)
GPBMUX2	0x6F98	2	Reserved
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 35)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 35)
Reserved	0x6F9E – 0x6F9F	2	Reserved
Reserved	0x6FA0 – 0x6FBF	32	Reserved
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO Data Register (GPIO32 to 35)
GPBSET	0x6FCA	2	GPIO Data Set Register (GPIO32 to 35)
GPBCLEAR	0x6FCC	2	GPIO Data Clear Register (GPIO32 to 35)
GPBTOGGLE	0x6FCE	2	GPIO Data Toggle Register (GPIO32 to 35)
Reserved	0x6FD0 – 0x6FDF	16	Reserved
GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXNMISEL	0x6FE2	1	XNMI GPIO Input Select Register (GPIO0 to 31)
Reserved	0x6FE3 – 0x6FE7	5	Reserved
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)
Reserved	0x6FEA – 0x6FFF	22	Reserved

Table 6-12. F28044 GPIO MUX Table

GPxMUX1/2[1] REGISTER BITS	DEFAULT AT RESET PRIMARY I/O FUNCTION (GPxMUX1/2 BITS = 0,0)	PERIPHERAL SELECTION 1[2] (GPxMUX1 BITS = 0,1)		PERIPHERAL SELECTION 2[2] (GPxMUX1/2 BITS = 1,0)	PERIPHERAL SELECTION 3[2] (GPxMUX1/2 BITS = 1,1)
		GPAMCFG(EPWMMODE)[3]			
		0,0[4]	1,1		
GPAMUX1					
1–0	GPIO0	EPWM1A (O)	EPWM1A (O)	Reserved	Reserved
3–2	GPIO1	EPWM1B (O)	EPWM2A (O)	Reserved	Reserved
5–4	GPIO2	EPWM2A (O)	EPWM3A (O)	Reserved	Reserved
7–6	GPIO3	EPWM2B (O)	EPWM4A (O)	Reserved	Reserved
9–8	GPIO4	EPWM3A (O)	EPWM5A (O)	Reserved	Reserved
11–10	GPIO5	EPWM3B (O)	EPWM6A (O)	Reserved	Reserved
13–12	GPIO6	EPWM4A (O)	EPWM7A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15–14	GPIO7	EPWM4B (O)	EPWM8A (O)	Reserved	Reserved
17–16	GPIO8	EPWM5A (O)	EPWM9A (O)	Reserved	$\overline{\text{ADCSOCAO}}$ (O)
19–18	GPIO9	EPWM5B (O)	EPWM10A (O)	Reserved	Reserved
21–20	GPIO10	EPWM6A (O)	EPWM11A (O)	Reserved	$\overline{\text{ADCSOCBO}}$ (O)
23–22	GPIO11	EPWM6B (O)	EPWM12A (O)	Reserved	Reserved
25–24	GPIO12	$\overline{\text{TZ1}}$ (I)	EPWM13A (O)	Reserved	Reserved
27–26	GPIO13	$\overline{\text{TZ2}}$ (I)	EPWM14A (O)	Reserved	Reserved
29–28	GPIO14	$\overline{\text{TZ3}}$ (I)	EPWM15A (O)	Reserved	Reserved
31–30	GPIO15	$\overline{\text{TZ4}}$ (I)	EPWM16A (O)	Reserved	Reserved
GPAMUX2					
1–0	GPIO16	SPISIMOA (I/O)		Reserved	$\overline{\text{TZ5}}$ (I)
3–2	GPIO17	SPISOMIA (I/O)		Reserved	$\overline{\text{TZ6}}$ (I)
5–4	GPIO18	SPICLKA (I/O)		Reserved	$\overline{\text{TZ1}}$ (I)
7–6	GPIO19	SPISTEA (I/O)		Reserved	$\overline{\text{TZ2}}$ (I)
9–8	GPIO20	Reserved		Reserved	Reserved
11–10	GPIO21	Reserved		Reserved	Reserved
13–12	GPIO22	Reserved		Reserved	Reserved
15–14	GPIO23	Reserved		Reserved	Reserved
17–16	GPIO24	Reserved		Reserved	Reserved
19–18	GPIO25	Reserved		Reserved	Reserved
21–20	GPIO26	Reserved		Reserved	Reserved
23–22	GPIO27	Reserved		Reserved	Reserved
25–24	GPIO28	SCIRXDA (I)		Reserved	$\overline{\text{TZ5}}$ (I)
27–26	GPIO29	SCITXDA (O)		Reserved	$\overline{\text{TZ6}}$ (I)
29–28	GPIO30	Reserved		Reserved	$\overline{\text{TZ3}}$ (I)
31–30	GPIO31	Reserved		Reserved	$\overline{\text{TZ4}}$ (I)
GPBMUX1					
1–0	GPIO32	SDAA (I/OC)		EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3–2	GPIO33	SCLA (I/OC)		EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5–4	GPIO34	Reserved		Reserved	Reserved

(1) GPxMUX1/2 refers to the appropriate MUX register for the pin; GPAMUX1, GPAMUX2 or GPBMUX1.
(2) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.
(3) The options GPAMCFG(EPWMMODE) = 0, 1 and 1, 0 are reserved.
(4) This is the default configuration upon reset.

The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2 = 0,0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2 = 0,1 and 1,0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.

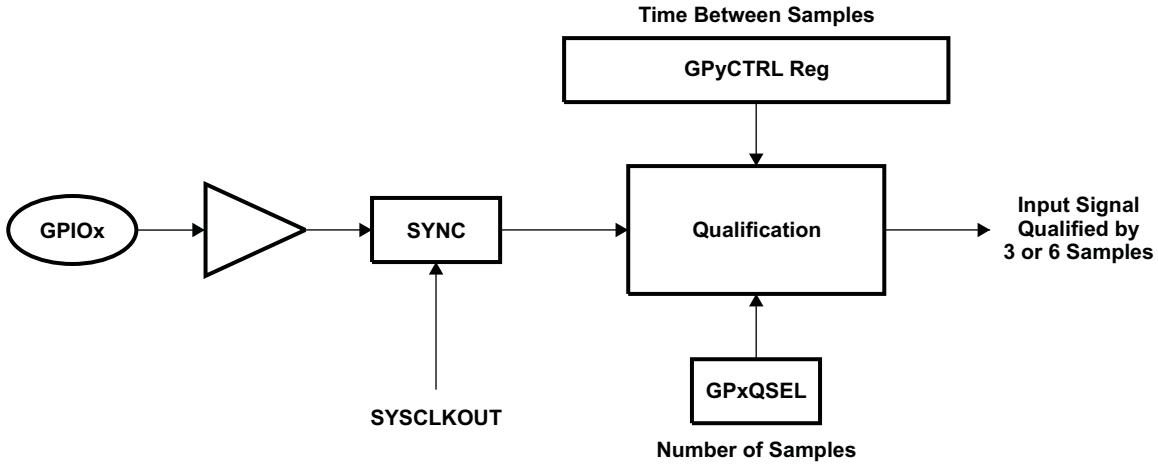
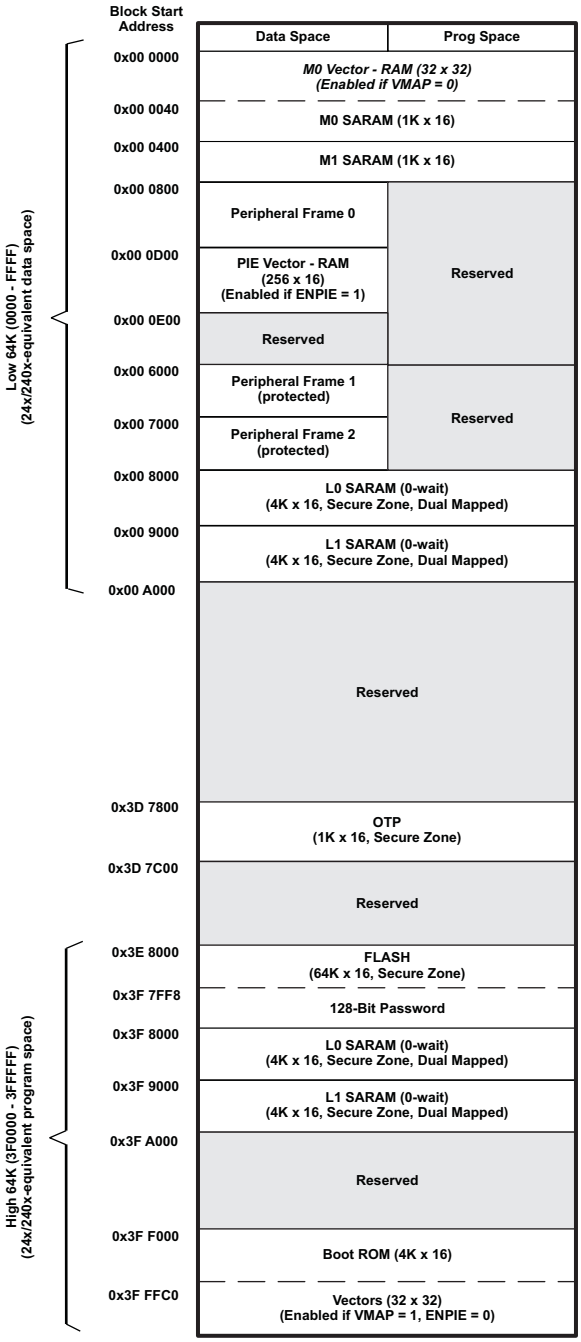


Figure 6-12. Qualification Using Sampling Window

- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 5-7 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2 = 1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the F28044 device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.

6.3 Memory Map



A. Memory blocks are not to scale.
B. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
C. “Protected” means the order of Write followed by Read operations is preserved rather than the pipeline order.
D. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 6-13. F28044 Memory Map

Table 6-13. Addresses of Flash Sectors

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 – 0x3E BFFF	Sector D (16K x 16)
0x3E C000 – 0x3E FFFF	Sector C (16K x 16)
0x3F 0000 – 0x3F 3FFF	Sector B (16K x 16)
0x3F 4000 – 0x3F 7F7F	Sector A (16K x 16)
0x3F 7F80 – 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 – 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 – 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

NOTE

- When the code-security passwords are programmed, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F7F80 through 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 – 0x3F7FF5 are reserved for data and should not contain program code.

Table 6-14 shows how to handle these memory locations.

Table 6-14. Impact of Using the Code Security Module

ADDRESS	FLASH	
	Code security enabled	Code security disabled
0x3F 7F80 – 0x3F 7FEF	Fill with 0x0000	Application code and data
0x3F 7FF0 – 0x3F 7FF5		Reserved for data only
0x3D 7BFC – 0x3D 7BFF	Application code and data	

Peripheral Frame 1 and Peripheral Frame 2 are grouped together so as to enable these blocks to be write/read peripheral block protected. The protected mode ensures that all accesses to these blocks happen as written. Because of the C28x pipeline, a write immediately followed by a read, to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The C28x CPU supports a block protection mode where a region of memory can be protected so as to make sure that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it will protect the selected zones.

The wait-states for the various spaces in the memory map area are listed in Table 6-15.

Table 6-15. Wait-states

AREA	WAIT-STATES	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	Fixed
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Fixed. Consecutive (back-to-back) writes to Peripheral Frame 1 registers will experience a 1-cycle pipeline hit (1-cycle delay).
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed
L0 and L1 SARAMs	0-wait	
OTP	Programmable, 1-wait minimum	Programmed via the Flash registers. 1-wait-state operation is possible at a reduced CPU frequency. See Section 6.1.5 for more information.
Flash	Programmable, 0-wait minimum	Programmed via the Flash registers. 0-wait-state operation is possible at reduced CPU frequency. The CSM password locations are hardwired for 16 wait-states. See Section 6.1.5 for more information.
Boot-ROM	1-wait	Fixed

6.4 Register Map

The F28044 device contains three peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 6-16.

Peripheral Frame 1 These are peripherals that are mapped to the 32-bit peripheral bus. See Table 6-17.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 6-18.

Table 6-16. Peripheral Frame 0 Registers(1) (2)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE(3)
Device Emulation Registers	0x0880 – 0x09FF	384	EALLOW protected
FLASH Registers(4)	0x0A80 – 0x0ADF	96	EALLOW protected CSM Protected
Code Security Module Registers	0x0AE0 – 0x0AEF	16	EALLOW protected
ADC Result Registers (dual-mapped)	0x0B00 – 0xB0F	16	Not EALLOW protected
CPU-TIMER0/1/2 Registers	0x0C00 – 0x0C3F	64	
PIE Registers	0x0CE0 – 0x0CFF	32	
PIE Vector Table	0x0D00 – 0x0DFF	256	EALLOW protected

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) Missing segments of memory space are reserved and should not be used in applications.
(3) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(4) The Flash Registers are also protected by the Code Security Module (CSM).

Table 6-17. Peripheral Frame 1 Registers(1) (2)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
ePWM1 + HRPWM Registers	0x6800 – 0x683F	64	Some ePWM registers are EALLOW protected. See Table 6-3 through Table 6-6.
ePWM2 + HRPWM Registers	0x6840 – 0x687F	64	
ePWM3 + HRPWM Registers	0x6880 – 0x68BF	64	
ePWM4 + HRPWM Registers	0x68C0 – 0x68FF	64	
ePWM5 + HRPWM Registers	0x6900 – 0x693F	64	
ePWM6 + HRPWM Registers	0x6940 – 0x697F	64	
ePWM7 + HRPWM Registers	0x6980 – 0x69BF	64	
ePWM8 + HRPWM Registers	0x69C0 – 0x69FF	64	
ePWM9 + HRPWM Registers	0x6600 – 0x663F	64	
ePWM10 + HRPWM Registers	0x6640 – 0x667F	64	
ePWM11 + HRPWM Registers	0x6680 – 0x66BF	64	
ePWM12 + HRPWM Registers	0x66C0 – 0x66FF	64	
ePWM13 + HRPWM Registers	0x6700 – 0x673F	64	
ePWM14 + HRPWM Registers	0x6740 – 0x677F	64	
ePWM15 + HRPWM Registers	0x6780 – 0x67BF	64	
ePWM16 + HRPWM Registers	0x67C0 – 0x67FF	64	
GPIO Control Registers	0x6F80 – 0x6FBF	128	EALLOW protected
GPIO Data Registers	0x6FC0 – 0x6FDF	32	Not EALLOW protected
GPIO Interrupt and LPM Select Registers	0x6FE0 – 0x6FFF	32	EALLOW protected

(1) All 32-bit accesses are aligned to even address boundaries.
(2) Missing segments of memory space are reserved and should not be used in applications.

Table 6-18. Peripheral Frame 2 Registers(1) (2)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
System Control Registers	0x7010 – 0x702F	32	EALLOW Protected
SPI-A Registers	0x7040 – 0x704F	16	Not EALLOW Protected
SCI-A Registers	0x7050 – 0x705F	16	
External Interrupt Registers	0x7070 – 0x707F	16	
ADC Registers	0x7100 – 0x711F	32	
I^2C Registers	0x7900 – 0x792F	48	

(1) Peripheral Frame 2 only allows 16-bit accesses. All 32-bit accesses are ignored (invalid data may be returned or written).
(2) Missing segments of memory space are reserved and should not be used in applications.

6.4.1 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 6-19.

Table 6-19. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION
DEVICECNF	0x0880 – 0x0881	2	Device Configuration Register
PARTID	0x0882	1	Part ID Register 0x00FC – F28044
REVID	0x0883	1	Revision ID Register 0x0000 – Silicon Rev. 0 - TMX or TMS
PROTSTART	0x0884	1	Block Protection Start Address Register
PROTRANGE	0x0885	1	Block Protection Range Address Register

6.5 Interrupts

Figure 6-14 shows how the various interrupt sources are multiplexed within the F28044 device.

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. On the F28044 device, 43 of these are used by peripherals as shown in Table 6-20.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. TRAP #0 attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, TRAP #0 should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, TRAP #1 through TRAP #12 will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: TRAP #1 fetches the vector from INT1.1, TRAP #2 fetches the vector from INT2.1 and so forth.

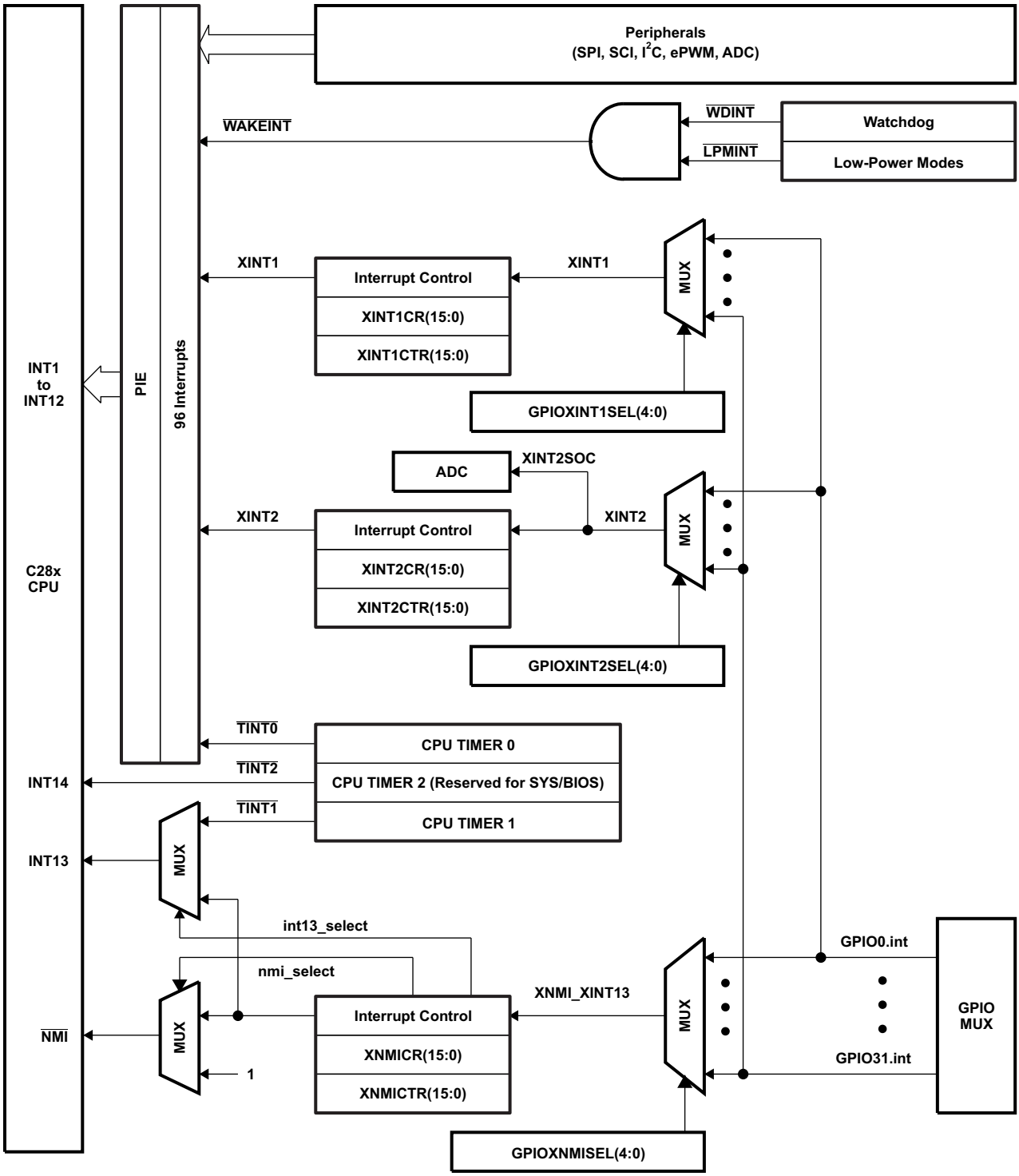


Figure 6-14. External and PIE Interrupt Sources

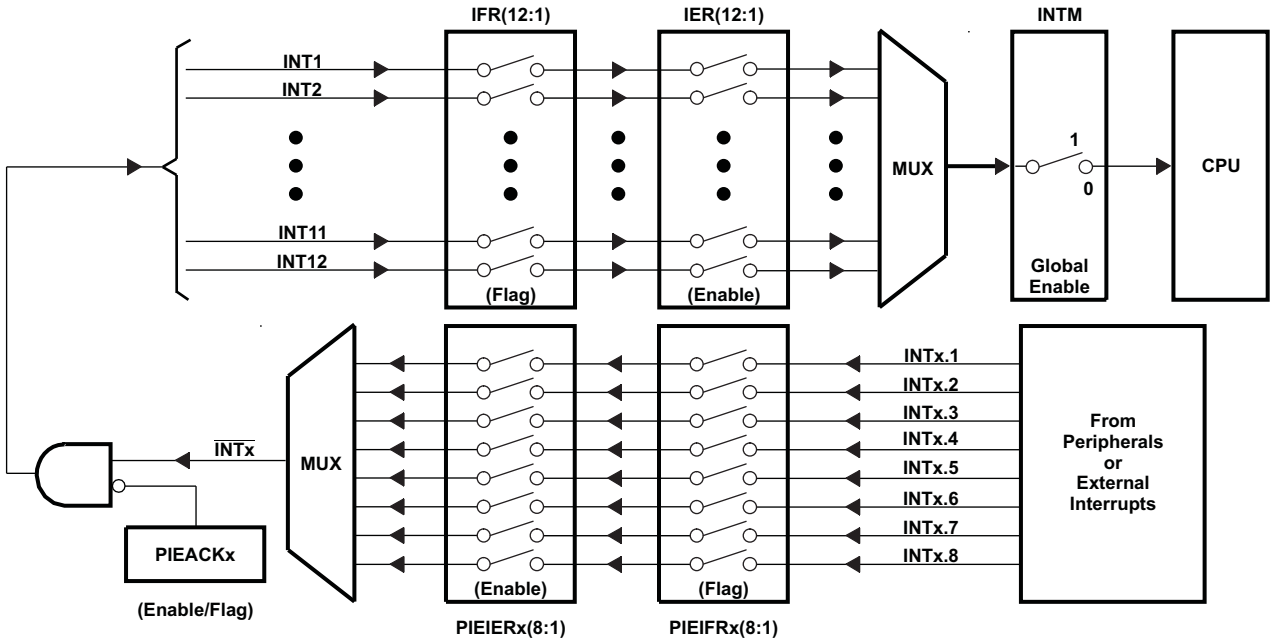


Figure 6-15. Multiplexing of Interrupts Using the PIE Block

Table 6-20. PIE Peripheral Interrupts(1)

CPU INTERRUPTS	PIE INTERRUPTS							
	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1	WAKEINT (LPM/WD)	TINT0 (TIMER 0)	ADCINT (ADC)	XINT2	XINT1	Reserved	SEQ2INT (ADC)	SEQ1INT (ADC)
INT2	EPWM8_TZINT (ePWM8)	EPWM7_TZINT (ePWM7)	EPWM6_TZINT (ePWM6)	EPWM5_TZINT (ePWM5)	EPWM4_TZINT (ePWM4)	EPWM3_TZINT (ePWM3)	EPWM2_TZINT (ePWM2)	EPWM1_TZINT (ePWM1)
INT3	EPWM8_INT (ePWM8)	EPWM7_INT (ePWM7)	EPWM6T_INTn (ePWM6)	EPWM5_INT (ePWM5)	EPWM4_INT (ePWM4)	EPWM3_INT (ePWM3)	EPWM2_INT (ePWM2)	EPWM1_INT (ePWM1)
INT4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SPITXINTA (SPI-A)	SPIRXINTA (SPI-A)
INT7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	I2CINT2A (I2C-A)	I2CINT1A (I2C-A)
INT9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCITXINTA (SCI-A)	SCIRXINTA (SCI-A)
INT10	EPWM16_TZINT (ePWM16)	EPWM15_TZINT (ePWM15)	EPWM14_TZINT (ePWM14)	EPWM13_TZINT (ePWM13)	EPWM12_TZINT (ePWM12)	EPWM11_TZINT (ePWM11)	EPWM10_TZINT (ePWM10)	EPWM9_TZINT (ePWM9)
INT11	EPWM16_INT (ePWM16)	EPWM15_INT (ePWM15)	EPWM14_INT (ePWM14)	EPWM13_INT (ePWM13)	EPWM12_INT (ePWM12)	EPWM11_INT (ePWM11)	EPWM10_INT (ePWM10)	EPWM9_INT (ePWM9)
INT12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

(1) Out of the 96 possible interrupts, 43 interrupts are currently used. The remaining interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:
- No peripheral within the group is asserting interrupts.
- No peripheral interrupts are assigned to the group (example PIE group 12).

Table 6-21. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA – 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

6.5.1 External Interrupts

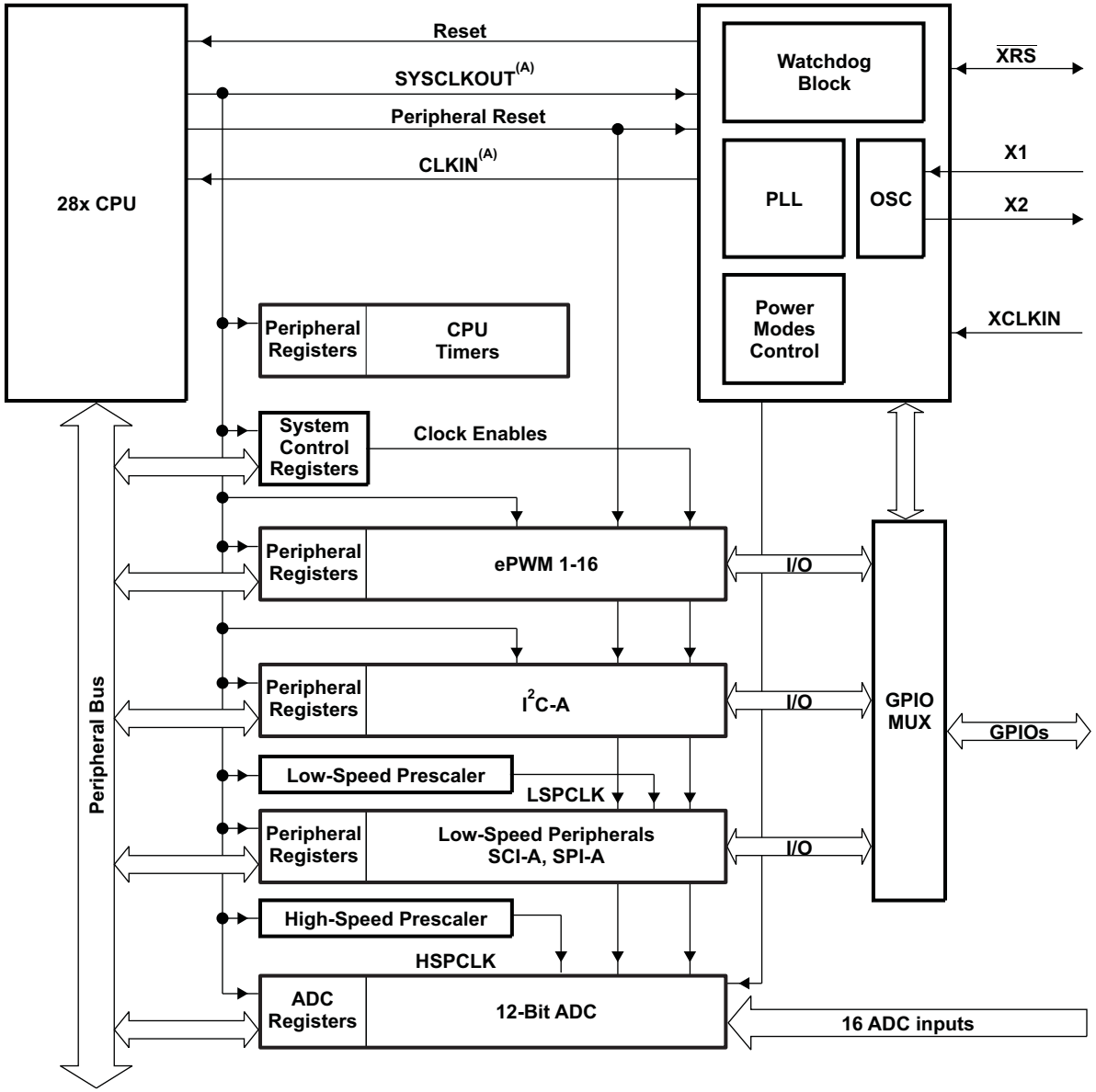
Table 6-22. External Interrupt Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x7070	1	XINT1 control register
XINT2CR	0x7071	1	XINT2 control register
Reserved	0x7072 – 0x7076	5	Reserved
XNMICR	0x7077	1	XNMI control register
XINT1CTR	0x7078	1	XINT1 counter register
XINT2CTR	0x7079	1	XINT2 counter register
Reserved	0x707A – 0x707E	5	Reserved
XNMICTR	0x707F	1	XNMI counter register

Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the *TMS320x280x, 2801x, 2804x DSP System Control and Interrupts Reference Guide*.

6.6 System Control

This section describes the F28044 device oscillator, PLL and clocking mechanisms, the watchdog function and the low-power modes. Figure 6-16 shows the various clock and reset domains in the F28044 device that will be discussed.



A. CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 6-16. Clock and Reset Domains

The PLL, clocking, watchdog and low-power modes, are controlled by the registers listed in Table 6-23.

Table 6-23. PLL, Clocking, Watchdog, and Low-Power Mode Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XCLK	0x7010	1	XCLKOUT Pin Control, X1 and XCLKIN Status Register
PLLSTS	0x7011	1	PLL Status Register
Reserved	0x7012 – 0x7018	7	Reserved
PCLKCR2	0x7019	1	Peripheral Clock Control Register 2
HISPCP	0x701A	1	High-Speed Peripheral Clock Prescaler Register (for HSPCLK)
LOSPCP	0x701B	1	Low-Speed Peripheral Clock Prescaler Register (for LSPCLK)
PCLKCR0	0x701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x701D	1	Peripheral Clock Control Register 1
LPMCR0	0x701E	1	Low Power Mode Control Register 0
Reserved	0x701F – 0x7020	1	Reserved
PLLCR	0x7021	1	PLL Control Register
SCSR	0x7022	1	System Control and Status Register
WDCNTR	0x7023	1	Watchdog Counter Register
Reserved	0x7024	1	Reserved
WDKEY	0x7025	1	Watchdog Reset Key Register
Reserved	0x7026 – 0x7028	3	Reserved
WDCR	0x7029	1	Watchdog Control Register
Reserved	0x702A – 0x702F	6	Reserved

(1) All of the registers in this table are EALLOW protected.

6.6.1 OSC and PLL Block

Figure 6-17 shows the OSC and PLL block on the F28044.

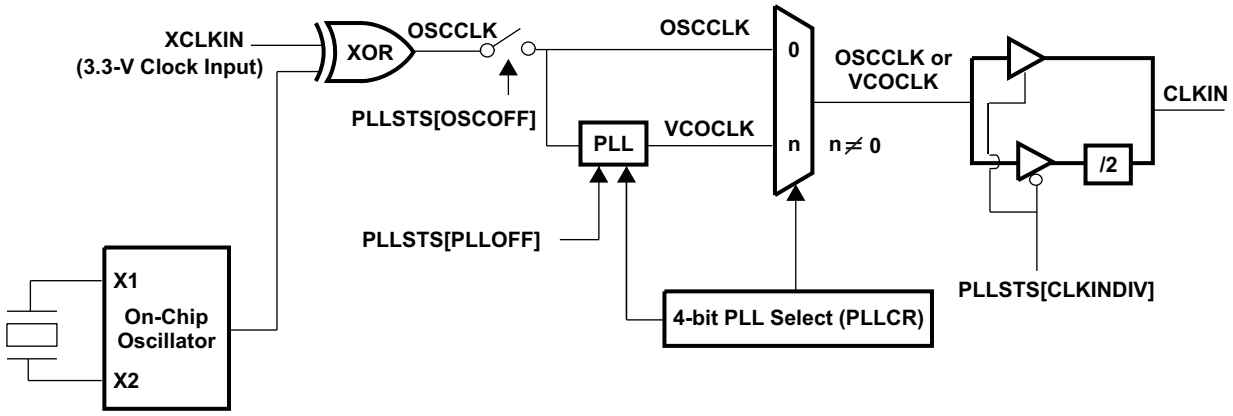


Figure 6-17. OSC and PLL Block Diagram

The on-chip oscillator circuit enables a crystal/resonator to be attached to the F28044 device using the X1 and X2 pins. If the on-chip oscillator is not used, an external oscillator can be used in either one of the following configurations:

1. A 3.3-V external oscillator can be directly connected to the XCLKIN pin. The X2 pin should be left unconnected and the X1 pin tied low. The logic-high level in this case should not exceed V_{DDIO}.
2. A 1.8-V external oscillator can be directly connected to the X1 pin. The X2 pin should be left unconnected and the XCLKIN pin tied low. The logic-high level in this case should not exceed V_{DD}.

The three possible input-clock configurations are shown in Figure 6-18 through Figure 6-20

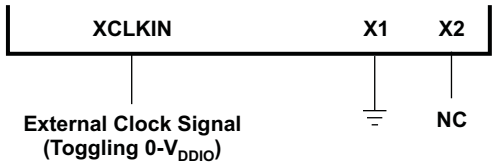


Figure 6-18. Using a 3.3-V External Oscillator

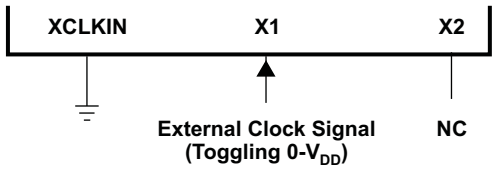


Figure 6-19. Using a 1.8-V External Oscillator

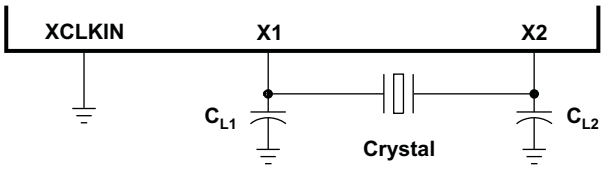


Figure 6-20. Using the Internal Oscillator

6.6.1.1 External Reference Oscillator Clock Option

The typical specifications for the external quartz crystal for a frequency of 20 MHz are listed below:

- Fundamental mode, parallel resonant
- C_L (load capacitance) = 12 pF
- $C_{L1} = C_{L2}$ = 24 pF
- C_{shunt} = 6 pF
- ESR range = 30 to 60 Ω

TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start up and stability over the entire operating range.

6.6.1.2 PLL-Based Clock Module

The F28044 device has an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 131072 OSCCLK cycles.

Table 6-24. PLLCR Register Bit Definitions

PLLCR[DIV](1)	PLLSTS[CLKINDIV]	SYSCLKOUT (CLKIN)(2)
0000 (PLL bypass)	0	OSCCLK/2
0000 (PLL bypass)	1	OSCCLK
0001	0	(OSCCLK*1)/2
0010	0	(OSCCLK*2)/2
0011	0	(OSCCLK*3)/2
0100	0	(OSCCLK*4)/2
0101	0	(OSCCLK*5)/2
0110	0	(OSCCLK*6)/2
0111	0	(OSCCLK*7)/2
1000	0	(OSCCLK*8)/2
1001	0	(OSCCLK*9)/2
1010	0	(OSCCLK*10)/2
1011–1111	0	Reserved

(1) This register is EALLOW protected.
(2) CLKIN is the input clock to the CPU. SYSCLKOUT is the output clock from the CPU. The frequency of SYSCLKOUT is the same as CLKIN.

NOTE

PLLSTS[CLKINDIV] can be set to 1 only if PLLCR is 0x0000. PLLCR should not be changed once PLLSTS[CLKINDIV] is set.

The PLL-based clock module provides two modes of operation:

- Crystal-operation - This mode allows the use of an external crystal/resonator to provide the time base to the device.
- External clock source operation - This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the X1 or the XCLKIN pin.

Table 6-25. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[CLKINDIV]	SYSCLKOUT (CLKIN)
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0	OSCCLK/2
		1	OSCCLK
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{XRS}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off.	0	OSCCLK/2
		1	OSCCLK
PLL Enable	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0	OSCCLK*n/2

6.6.1.3 Loss of Input Clock

In PLL-enabled and PLL-bypass mode, if the input clock OSCCLK is removed or absent, the PLL will still issue a "limp-mode" clock. The limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1–5 MHz. Limp mode is not specified to work from power-up, only after input clocks have been present initially. In PLL bypass mode, the limp mode clock from the PLL is automatically routed to the CPU if the input clock is removed or absent.

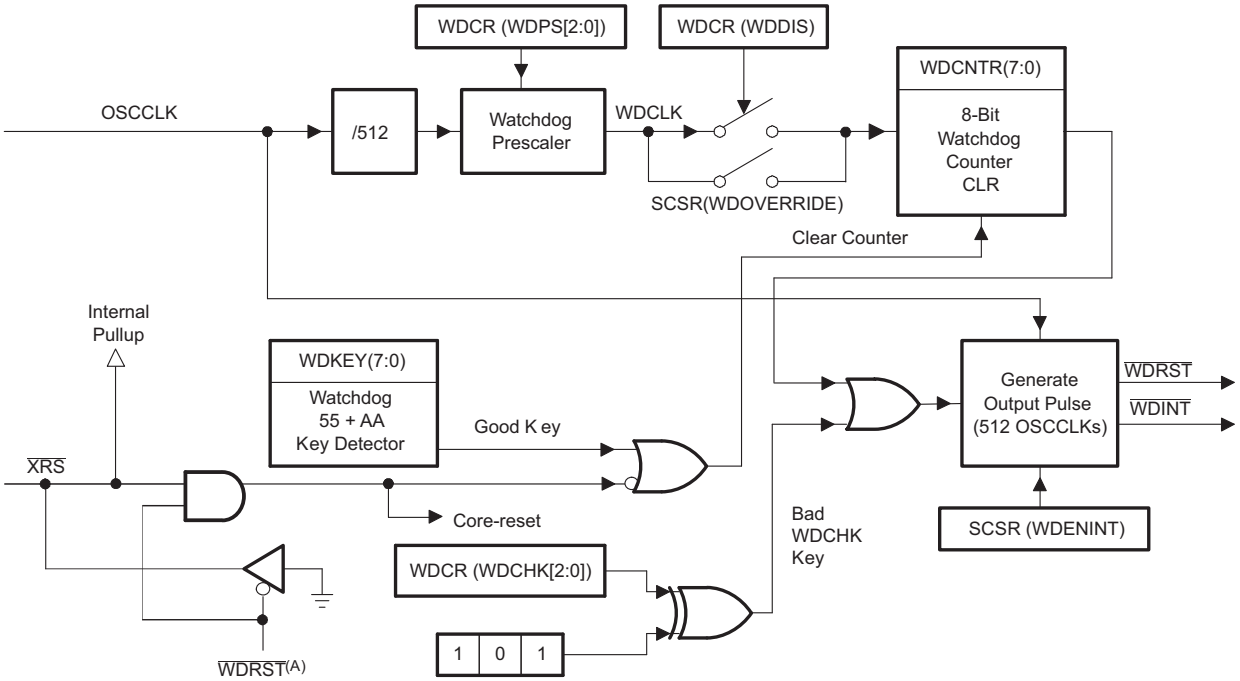
Normally, when the input clocks are present, the watchdog counter decrements to initiate a watchdog reset or WDINT interrupt. However, when the external input clock fails, the watchdog counter stops decrementing (that is, the watchdog counter does not change with the limp-mode clock). In addition to this, the device will be reset and the “Missing Clock Status” (MCLKSTS) bit will be set. These conditions could be used by the application firmware to detect the input clock failure and initiate necessary shut-down procedure for the system.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the DSP will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{XRS}$ pin of the DSP, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the flash memory and the V_{DD3VFL} rail.

6.6.2 Watchdog Block

The watchdog block on the F28044 is similar to the one used on the 240x and 281x devices. The watchdog module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user disables the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register which will reset the watchdog counter. Figure 6-21 shows the various functional blocks within the watchdog module.



A. The WDRST signal is driven low for 512 OSCCLK cycles.

Figure 6-21. Watchdog Module

The WDINT signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the watchdog. The WATCHDOG module will run off OSCCLK. The WDINT signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section 6.7, Low-Power Modes Block, for details.

In IDLE mode, the WDINT signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, this feature cannot be used because the oscillator (and PLL) are turned off and hence so is the WATCHDOG.

6.7 Low-Power Modes Block

The low-power modes on the F28044 device are similar to the 240x devices. Table 6-26 summarizes the various modes.

Table 6-26. Low-Power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On(2)	$\overline{\text{XRS}}$, Watchdog interrupt, any enabled interrupt, XNMI
STANDBY	01	On (watchdog still running)	Off	Off	$\overline{\text{XRS}}$, Watchdog interrupt, GPIO Port A signal, debugger(3), XNMI
HALT	1X	Off (oscillator and PLL turned off, watchdog not functional)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A signal, XNMI, debugger(3)

(1) The Exit column lists which signals or under what conditions the low power mode will be exited. A low signal, on any of the signals, will exit the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise the IDLE mode will not be exited and the device will go back into the indicated low power mode.
(2) The IDLE mode on the C28x behaves differently than on the 24x/240x. On the C28x, the clock output from the CPU (SYSCLKOUT) is still functional while on the 24x/240x the clock is turned off.
(3) On the C28x, the JTAG port can still function even if the CPU clock (CLKIN) is turned off.

The various low-power modes operate as follows:

IDLE Mode: This mode is exited by any enabled interrupt or an XNMI that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode: Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode: Only the $\overline{\text{XRS}}$ and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the *TMS320x280x, 2801x, 2804x DSP System Control and Interrupts Reference Guide* for details.

7 Applications, Implementation, and Layout

NOTE

Information in the following sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 TI Reference Design

The TI Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all reference designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at the Select TI reference designs page.

8 Device and Documentation Support

8.1 Getting Started

This section gives a brief overview of the steps to take when first developing for a C28x device. For more detail on each of these steps, see the following:

- C2000 real-time control MCUs – Design & development
- Motor drive and control
- Digital power

Step 1. Acquire the appropriate development tools

The quickest way to begin working with a C28x device is to acquire an eZdsp™ kit for initial development, which, in one package, includes:

- On-board JTAG emulation via USB or parallel port
- Appropriate emulation driver
- Code Composer Studio™ IDE for eZdsp

Once you have become familiar with the device and begin developing on your own hardware, purchase Code Composer Studio™ IDE separately for software development and a JTAG emulation tool to get started on your project.

Step 2. Download starter software

To simplify programming for C28x devices, it is recommended that users download and use the C/C++ Header Files and Example(s) to begin developing software for the C28x devices and their various peripherals.

After downloading the appropriate header file package for your device, refer to the following resources for step-by-step instructions on how to run the peripheral examples and use the header file structure for your own software

- The Quick Start Readme in the /doc directory to run your first application.
- *Programming TMS320x28xx and TMS320x28xxx Peripherals in C/C++*

Step 3. Download flash programming software

Many C28x devices include on-chip flash memory and tools that allow you to program the flash with your software IP.

- Flash Tools: C28x Flash Tools
- *TMS320F281x Flash Programming Solutions*
- *Running an Application from Internal Flash Memory on the TMS320F28xxx DSP*

Step 4. Move on to more advanced topics

For more application software and other advanced topics, visit C2000 real-time control MCUs – Design & development.

8.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320 DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F28044). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GGM) and temperature range (for example, A). Figure 8-1 provides a legend for reading the complete device name.

For device part numbers and further ordering information, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F28044 Digital Signal Processor Silicon Errata*.

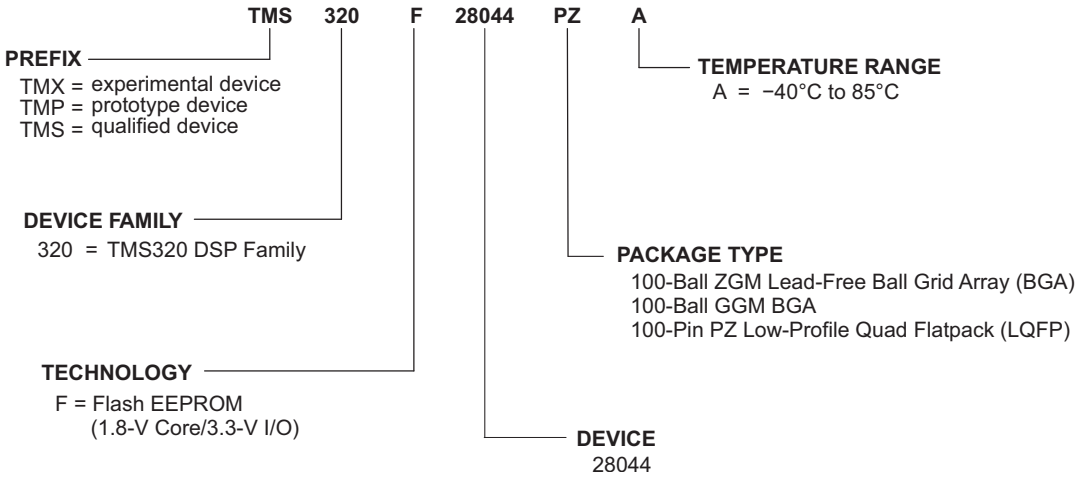


Figure 8-1. Device Nomenclature

8.3 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page.

The following products support development of 280x-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- 2808 eZdsp™
- JTAG debug probes - SPI515, XDS510PP, XDS510PP Plus, XDS510USB™
- Universal 5-V dc power supply
- Documentation and cables

Software

C28x IQMath Library - A Virtual Floating Point Engine
Texas Instruments TMS320C28x IQmath Library is collection of highly optimized and high precision mathematical Function Library for C/C++ programmers to seamlessly port the floating-point algorithm into fixed point code on TMS320C28x devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed & high accuracy is critical. By using these routines you can achieve execution speeds considerable faster than equivalent code written in standard ANSI C language. In addition, by providing ready-to-use high precision functions, TI IQmath library can shorten significantly your DSP application development time. (Please find the IQ Math User's Guide in the /docs folder once the file is extracted and installed).

C280x, C2801x C/C++ Header Files and Peripheral Examples
This utility contains Hardware Abstraction Layer (HAL) for TMS320x280x and TMS320x280xx DSP devices. This HAL facilitates peripheral configuration using "C". It also contains a simple test program for each peripheral to exemplify the usage of HAL to control & configure the on-chip peripheral.

Development Tools

C2000 Gang Programmer
The C2000 Gang Programmer is a C2000 device programmer that can program up to eight identical C2000 devices at the same time. The C2000 Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process.

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for C2000 Microcontrollers
Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Uniflash Standalone Flash Tool
CCS Uniflash is a standalone tool used to program on-chip flash memory on TI MCUs.

Models

Various models are available for download from the product Tools & Software pages. These include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Models section of the Tools & Software page.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time control MCUs – Support & training site.

8.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

Errata

TMS320F28044 Digital Signal Processor Silicon Errata describes the advisories and usage notes for different versions of silicon.

CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

TMS320x280x, 2801x, 2804x DSP System Control and Interrupts Reference Guide describes the various interrupts and system control features of the 280x digital signal processors (DSPs).

Peripheral Guides

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

TMS320x280x, 2801x, 2804x DSP Analog-to-Digital Converter (ADC) Reference Guide describes how to configure and use the on-chip ADC module, which is a 12-bit pipelined ADC.

TMS320x280x, 2801x, 2804x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion.

TMS320x280x, 2801x, 2804x Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance motion and position control systems. It includes the module description and registers.

TMS320x280x, 2801x, 2804x Enhanced Capture (eCAP) Module Reference Guide describes the enhanced capture module. It includes the module description and registers.

TMS320x280x, 2801x, 2804x High Resolution Pulse Width Modulator (HRPWM) Reference Guide describes the operation of the high-resolution extension to the pulse width modulator (HRPWM).

TMS320x281x Enhanced Controller Area Network (eCAN) Reference Guide describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments.

TMS320x281x Serial Communications Interface (SCI) Reference Guide describes the SCI, which is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

TMS320x281x Serial Peripheral Interface Reference Guide describes the SPI, a high-speed synchronous serial input/output (I/O) port, that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

TMS320x280x, 2801x, 2804x Serial Communications Interface (SCI) Reference Guide describes the features and operation of the serial communication interface (SCI) module that is available on the TMS320x280x, 2801x, 2804x devices.

TMS320x280x, 2801x, 2804x Serial Peripheral Interface Reference Guide describes how the serial peripheral interface works.

TMS320x280x, 2801x, 2804x Inter-Integrated Circuit (I2C) Module Reference Guide describes the features and operation of the inter-integrated circuit (I2C) module.

TMS320x280x, 2801x, 2804x Boot ROM Reference Guide describes the purpose and features of the bootloader (factory-programmed boot-loading software). It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

Tools Guides

TMS320C28x Assembly Language Tools v20.2.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v20.2.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

TMS320C28x DSP/BIOS 5.x Application Programming Interface (API) Reference Guide describes development using DSP/BIOS.

Application Reports

TMS320x281x to TMS320x2833x or 2823x Migration Overview describes how to migrate from the 281x device design to 2833x or 2823x designs.

TMS320x280x to TMS320x2833x or 2823x Migration Overview describes how to migrate from a 280x device design to 2833x or 2823x designs.

TMS320C28x FPU Primer provides an overview of the floating-point unit (FPU) in the C2000™ premium performance MCUs.

Running an Application from Internal Flash Memory on the TMS320F28xxx DSP covers the requirements needed to properly configure application software for execution from on-chip flash memory. Requirements for both DSP/BIOS and non-DSP/BIOS projects are presented. Example code projects are included.

Programming TMS320x28xx and TMS320x28xxx Peripherals in C/C++ explores a hardware abstraction layer implementation to make C/C++ coding easier on 28x DSPs. This method is compared to traditional #define macros and topics of code efficiency and special case registers are also addressed.

Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller presents a method for using the on-chip pulse width modulated (PWM) signal generators on the TMS320F280x family of digital signal controllers as a digital-to-analog converter (DAC).

TMS320F280x Digital Signal Controller USB Connectivity using the TUSB3410 USB-to-UART Bridge Chip presents hardware connections as well as software preparation and operation of the development system using a simple communication echo program.

Using the Enhanced Quadrature Encoder Pulse (eQEP) Module in TMS320x280x, 28xxx as a Dedicated Capture provides a guide for the use of the eQEP module as a dedicated capture unit and is applicable to the TMS320x280x, 28xxx family of processors.

Using the ePWM Module for 0% - 100% Duty Cycle Control provides a guide for the use of the ePWM module to provide 0% to 100% duty cycle control and is applicable to the TMS320x280x family of processors.

TMS320280x and TMS3202801x ADC Calibration describes a method for improving the absolute accuracy of the 12-bit ADC found on the TMS320x280x and TMS320F2801x devices. Inherent gain and offset errors affect the absolute accuracy of the ADC. The methods described in this report can improve the absolute accuracy of the ADC to levels better than 0.5%. This application report has an option to download an example program that executes from RAM on the F2808 EzDSP.

Online Stack Overflow Detection on the TMS320C28x DSP presents the methodology for online stack overflow detection on the TMS320C28x DSP. C-source code is provided that contains functions for implementing the overflow detection on both DSP/BIOS and non-DSP/BIOS applications.

TMS320x281x to TMS320x280x Migration Overview describes differences between the Texas Instruments TMS320x281x and the TMS320x280x/2801x/2804x DSPs to assist in application migration.

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures and future trends.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

Semiconductor and IC Package Thermal Metrics describes traditional and new thermal metrics and puts their application in perspective with respect to system-level junction temperature estimation.

Calculating FIT for a Mission Profile explains how use TI's reliability de-rating tools to calculate a component level FIT under power on conditions for a system mission profile.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

8.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.6 Trademarks

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8.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28044PZA	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320F28044PZA TMS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

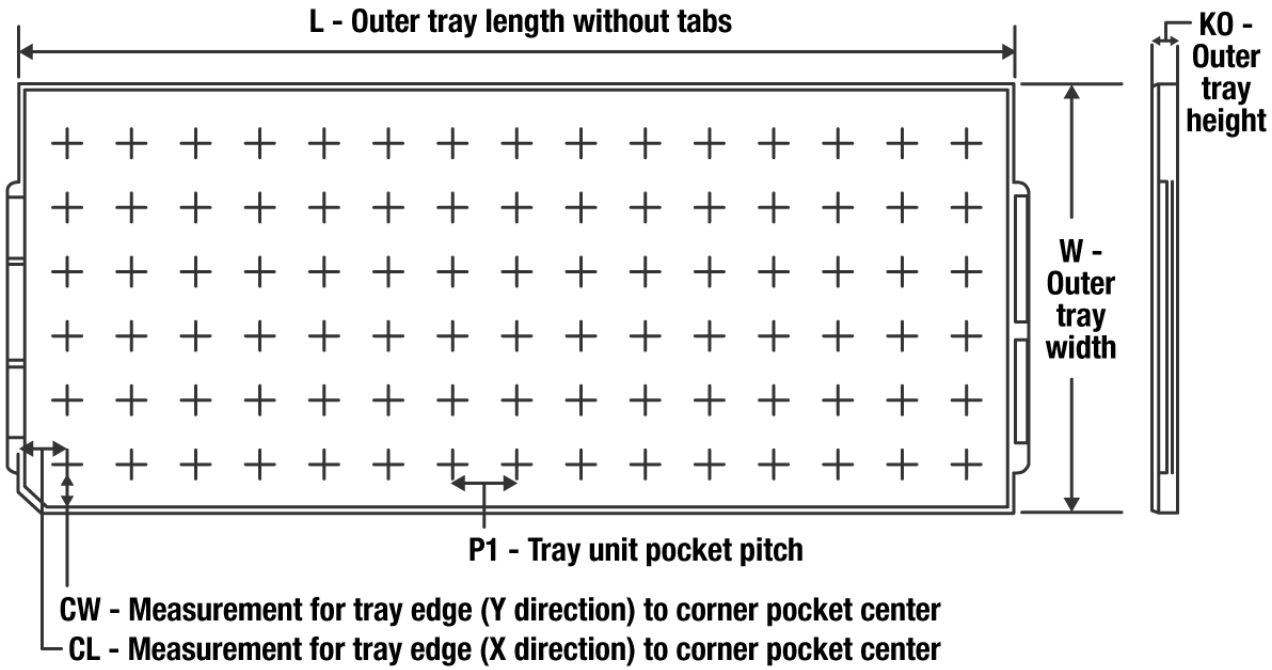
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



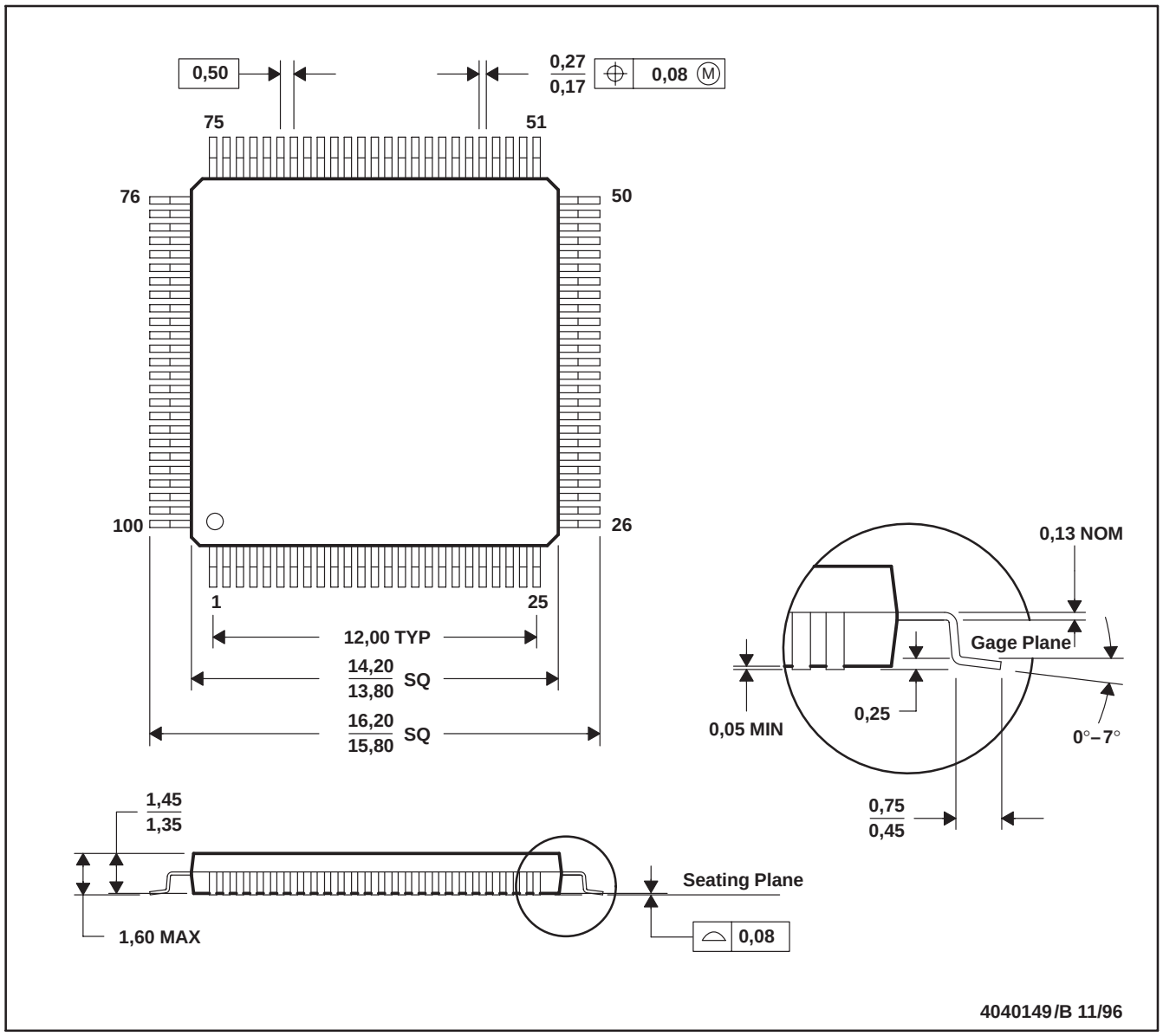
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320F28044PZA	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4

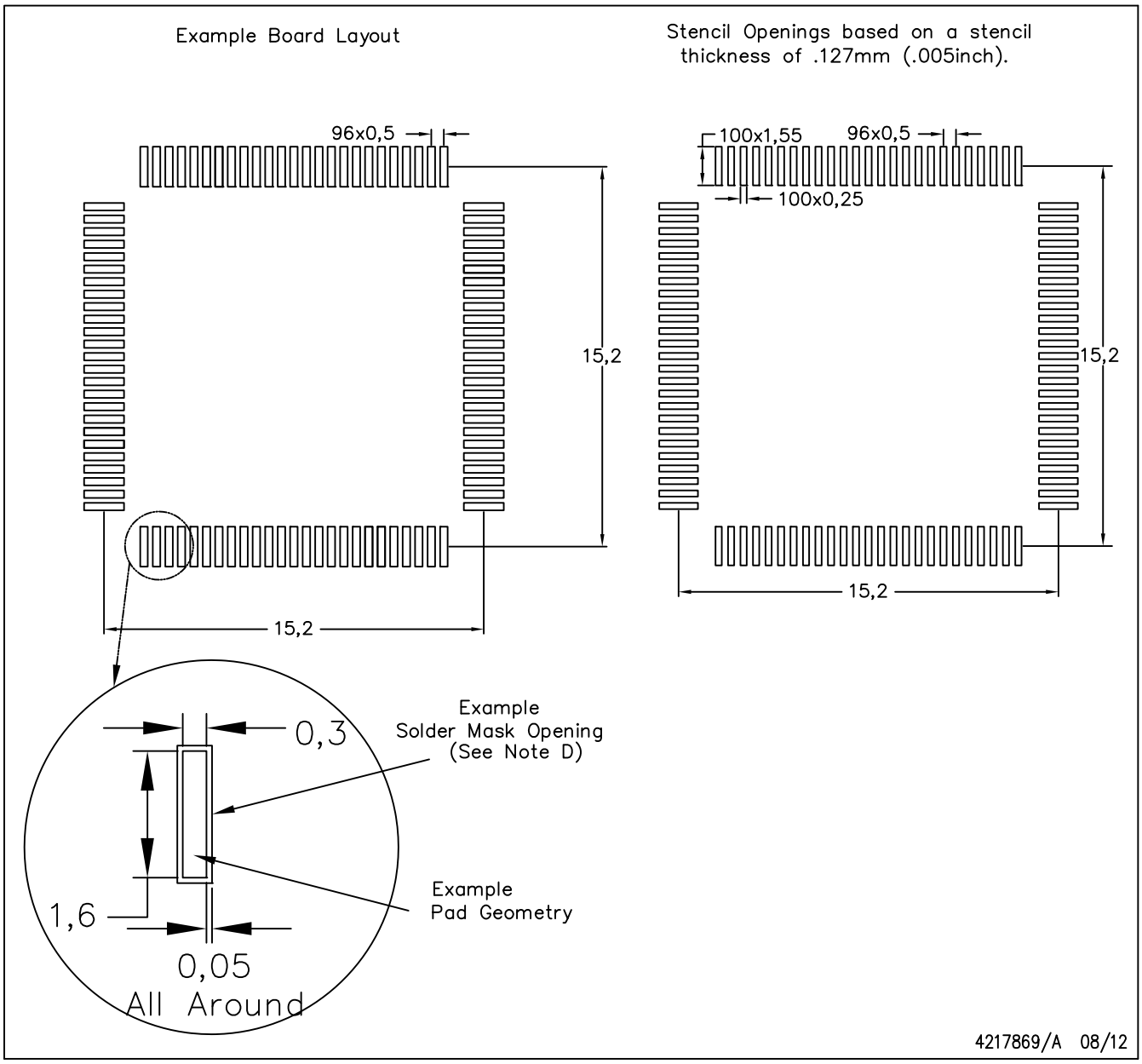
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

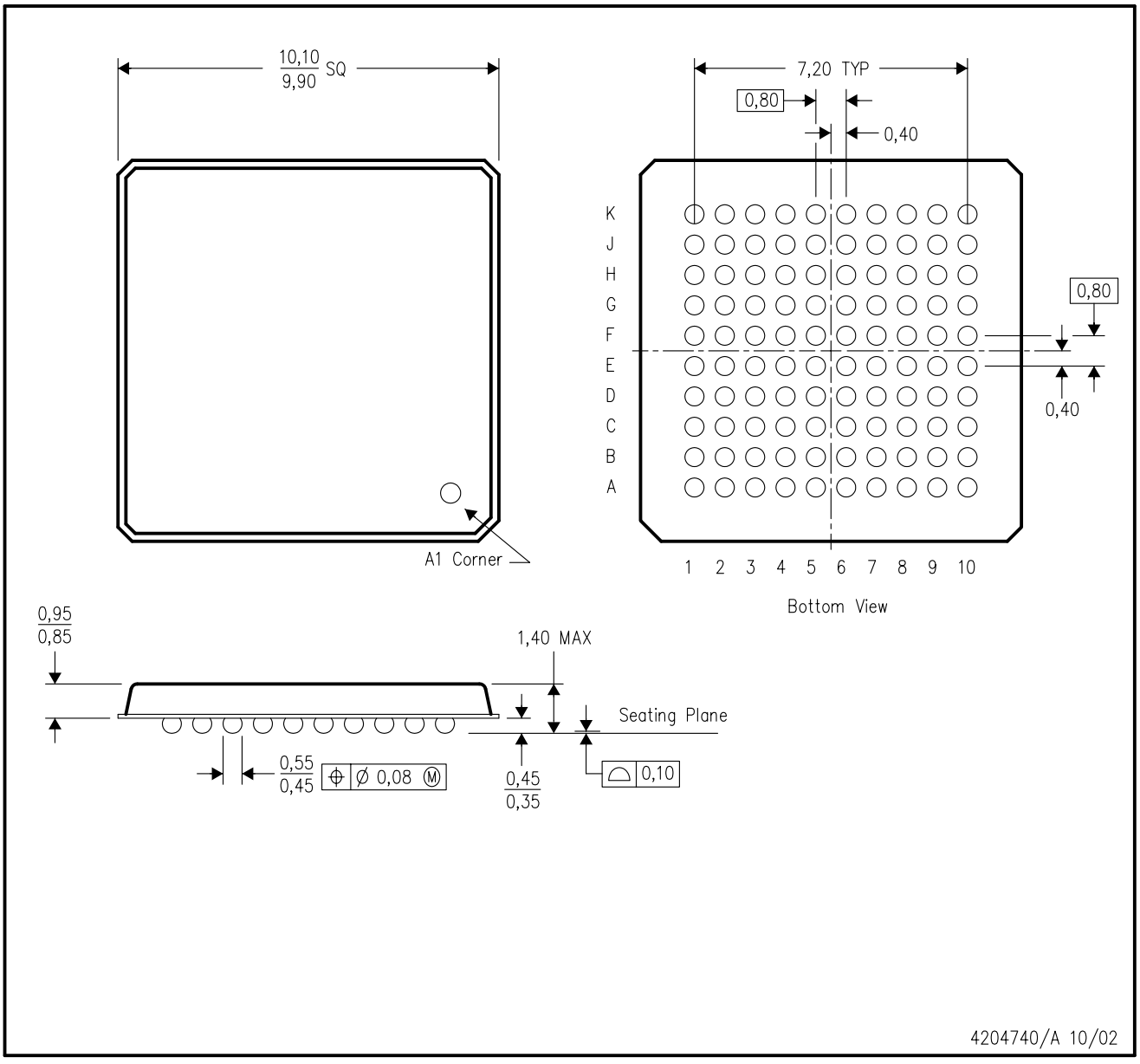
PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

ZGM (S–PBGA–N100) PLASTIC BALL GRID ARRAY

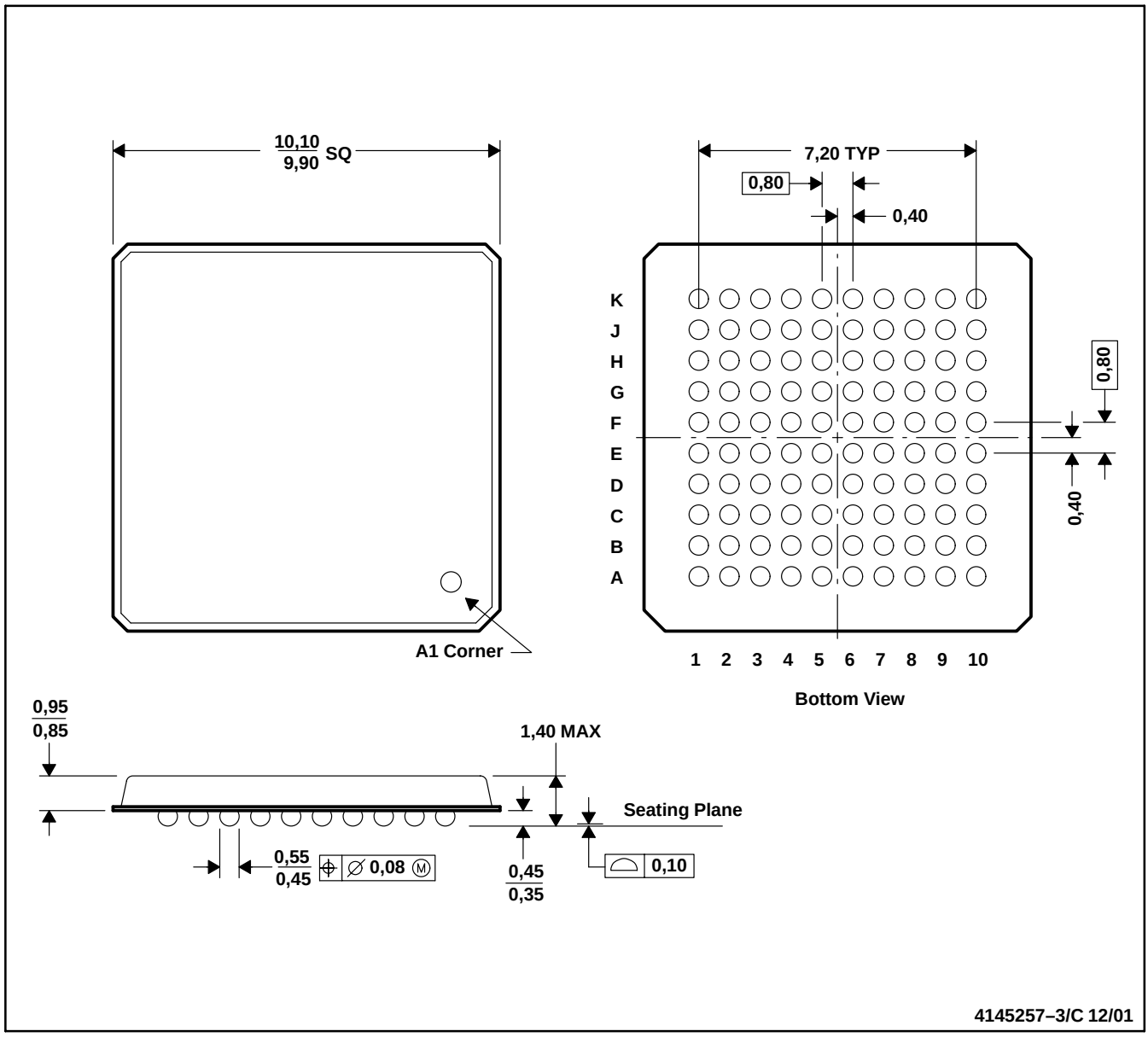


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration.
D. This package is lead–free.

MicroStar BGA is a trademark of Texas Instruments.

MPBG028B FEBRUARY 1997 – REVISED MAY 2002

GGM (S–PBGA–N100) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA configuration.

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