# TMUX121 具有断电隔离功能和 1.8V 逻辑的低电容双通道 2:1 开关

## 1 特性

- 与高速 $I^3C$ 信号兼容
- 高性能开关特性：
  - 带宽（–3dB）：3.0GHz
  - $R_{ON}$（典型值）：3Ω
  - $C_{ON}$（典型值）：1.7pF
  - $T_{PD}$（典型值）：60 ps
  - $T_{SWEK}$（典型值）：2ps
- 低电流消耗：12μA（典型值）
- 专有特性：
  - $I_{POFF}$ 保护可防止在断电状态下产生漏电流
  - 1.8V 和 3.3V 兼容控制输入（SEL，$\overline{EN}$）
- 3.3V 电源电压
- 工业温度范围：–40 至 125° C
- 紧凑型 10 引脚 1.4mm × 1.8mm，UQFN 封装

## 2 应用

- $I^3C$ (SenseWire)
- $I^3C$ 和 $I^2C$ 外设开关
- 服务器
- 手持终端：智能电话
- 笔记本电脑
- 平板电脑：多媒体
- 电子销售终端
- 现场仪器
- 便携式监视器

## 3 说明

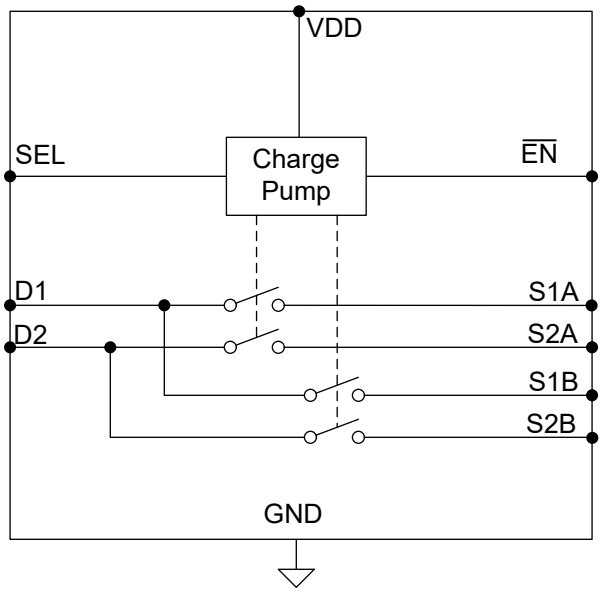
TMUX121 是一款高性能双向 2 通道 2:1 (SPDT) 开关，同时支持差分和单端信号。TMUX121 是一款具有断电保护功能的模拟无源开关，当 $V_{DD}$ 引脚断电时，强制所有 I/O 引脚进入高阻抗模式。TMUX121 的选择引脚和使能引脚与 1.8V 和 3.3V 控制电压兼容，因而能够直接与低电压处理器的通用 I/O (GPIO) 相连。凭借这一特性以及器件的低导通电阻和低导通电容，TMUX121 成为支持切换各种模拟信号和数字通信协议标准（包括 $I^3C$ 等高速标准）的理想选择。

TMUX121 采用小型 10 引脚 UQFN 封装，尺寸仅为 1.8mm × 1.4mm，非常适合 PCB 面积有限的情况。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) |
|---|---|---|
| TMUX121 | NKG（UQFN，10） | 1.8mm × 1.4mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。




应用用例

# Table of Contents



## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| August 2023 | * | Initial Release |

# 5 Pin Configuration and Functions

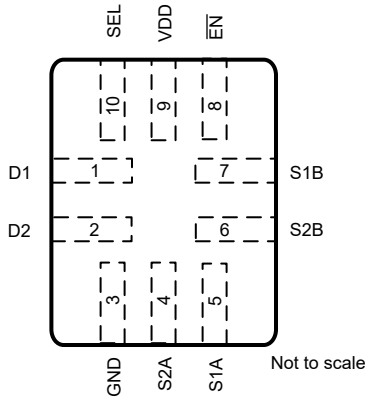



**图 5-1. TMUX121 NKG Package, 10-Pin UQFN (Top View)**

**表 5-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| D1 | 1 | I/O | Drain pin 1. Can be an input or output. |
| D2 | 2 | I/O | Drain pin 2. Can be an input or output. |
| S1A | 5 | I/O | Source pin 1A. Can be an input or output. |
| S2A | 4 | I/O | Source pin 2A. Can be an input or output. |
| S1B | 7 | I/O | Source pin 1B. Can be an input or output. |
| S2B | 6 | I/O | Source pin 2B. Can be an input or output. |
| SEL | 10 | IN | Switch logic control input. Controls the switch connection as provided in 表 7-1. |
| $\overline{EN}$ | 8 | IN | Active low enable input. Controls the switch connection as provided in 表 7-1. |
| VDD | 9 | P | 3.3 V power supply |
| GND | 3 | G | Ground |

(1) IN = input, I/O = input or output, P = power, G = ground

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.5 | 4.0 | V |
| $V_{EN}$ or $V_{SEL}$ | Logic control input pin current (SEL, EN) | –0.5 | 4.0 | V |
| $V_D$ or $V_S$ | Source or drain voltage (Sx, Dx) | –0.5 | 5.5 | V |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Junction temperature | –40 | 125 | °C |

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±5000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDD | Power Supply voltage | 3.0 | 3.3 | 3.6 | V |
| $VDD_{RAMP}$ | Power Supply voltage ramp time | 0.1 | | 100 | ms |
| $V_D$ or $V_S$ | Source or drain voltage (Sx, Dx) | 0 | | 3.6 | V |
| $V_{EN}$ or $V_{SEL}$ | Logic control input pin current (SEL, EN) | 0 | | 3.6 | V |
| $I_S$ or $I_D$ (cont) | Source or drain continuous current (Sx, Dx) | | | 90 | mA |
| $T_A$ | Operating free-air/ambient temperature | -40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TMUX121 NKG (UQFN) 10 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance - High K | 225.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 93.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 147.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 147.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

Over operating free-air temperature and supply voltage range (unless otherwise noted)
Typical at $V_{DD}$ = 3.3 V $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{DDQ}$ | $V_{DD}$ quiescent supply current | EN = $V_{DD}$ | | 1.3 | 4 | µA |
| $I_{DD}$ | $V_{DD}$ supply current | EN = 0 V | | 11 | 30 | µA |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V , $I_S$ = –8 mA | | 3 | 5.4 | Ω |
| | | $V_S$ = 2.4 V , $I_S$ = –8 mA | | 3.9 | 8 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0 V , $I_S$ = –8 mA | | | 0.5 | Ω |
| | | $V_S$ = 2.4 V , $I_S$ = –8 mA | | | 0.5 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V and $V_S$ = 2.4 V; $I_S$ = –8 mA | | 1 | | Ω |
| $I_{S(ON)}$ $I_{D(ON)}$ | Channel on leakage current (Sx, Dx) | Switch state is on $V_D$ = $V_S$ = 3.6 V | | | 2 | µA |
| | | Switch state is on $V_D$ = $V_S$ = 0 V | | | 0.2 | µA |
| $I_{S(OFF)}$ | Source off leakage current (Sx) | Switch state is off $V_S$ = 3.6 V | | | 2 | µA |
| $I_{D(OFF)}$ | Drain off leakage current (Dx) | Switch state is off $V_D$ = 3.6 V | | | 2 | µA |
| $I_{(POFF)}$ | Powered-off leakage current (Sx, Dx) | $V_{CC}$ = 0 V, $V_D$ or $V_S$ = 3.6 V | | | 10 | µA |
| $V_{IH}$ | Logic voltage high (EN, SEL) | | 1.4 | | 3.6 | V |
| $V_{IL}$ | Logic voltage low (EN, SEL) | | 0 | | 0.4 | |
| $I_{IL}$ | Input leakage current (EN, SEL) | | | | 0.2 | µA |
| $I_{IH}$ | Input leakage current (EN, SEL) | | | | 1 | µA |
| $I_{IH}$ | Failsafe Input leakage current (EN, SEL) | $V_{CC}$ = 0 V, $V_{EN}$ or $V_{SEL}$ = 3.6 V | | | 10 | µA |

## 6.6 Switching Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input (SEL) | $R_L$ = 50 Ω, $C_L$ = 10 pF | | | 1 | µs |
| $t_{ON}$ | Turn-on time from control input (EN) | $R_L$ = 50 Ω, $C_L$ = 10 pF | | | 16 | µs |
| $t_{OFF}$ | Turn-off time from control input (EN) | $R_L$ = 50 Ω, $C_L$ = 10 pF | | | 0.5 | µs |
| $t_{PD}$ | Switch propagation delay (Sx to Dx or Dx to Sx) | | | 60 | 80 | ps |
| $t_{SKEW\_INTRA}$ | Intra-pair propagation delay skew for same channel | | | 2 | 10 | ps |
| $t_{SKEW\_INTER}$ | Inter-pair propagation delay skew between channels | | | 2 | 10 | ps |
| BW | –3-dB bandwidth | | | 3 | | GHz |
| $I_L$ | Differential insertion loss | f = 10 MHz | | -0.3 | | dB |
| $O_{ISO}$ | Differential OFF isolation (D to SA/SB) | f = 10 MHz | | -56 | | dB |
| $X_{TALK}$ | Differential cross-talk (SA to SB or SB to SA) | f = 10 MHz | | -64 | | dB |
| $C_{S(ON)}$ $C_{D(ON)}$ | On capacitance | f = 10 MHz | | 1.7 | | pF |

## 6.7 Typical Characteristics

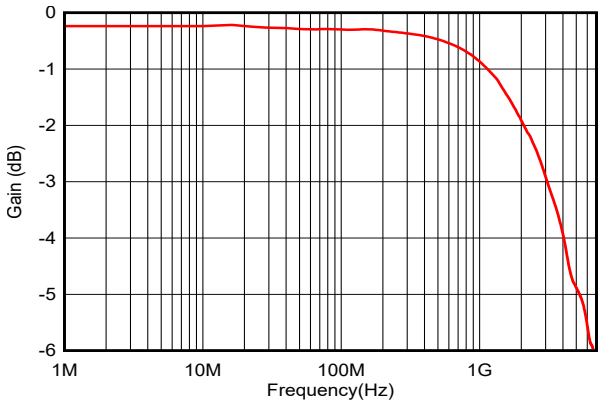



图 6-1. Typical Differential Bandwidth vs Frequency

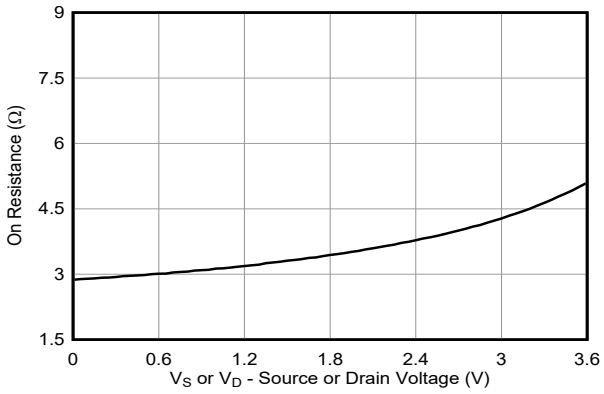


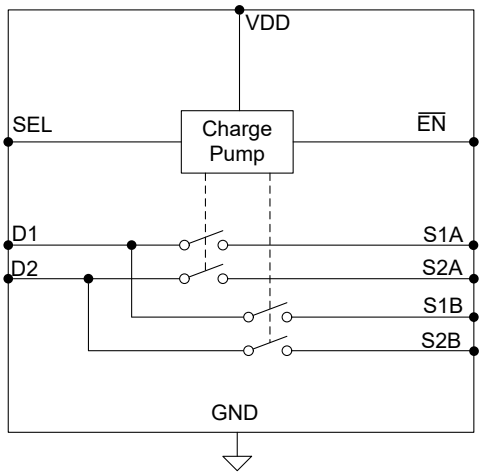

图 6-2. $R_{ON}$ vs Common Mode Voltage VCM

# 7 Detailed Description

## 7.1 Overview

The TMUX121 is an analog passive 2 channel 2:1 (SPDT) that can work for any low-speed, high-speed, differential or single ended signals. Excellent low capacitance characteristics of the device allow signal switching with minimal attenuation and very little added jitter. The signals must be within the allowable voltage range of 0 to 3.6 V.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Enable and Low Power Mode

The TMUX121 can be placed in a power saving mode by pulling $\overline{EN}$ high. This reduces the supply power consumption from 12 µA to 1.5 µA. which is extremely beneficial for systems where saving power is critical.

## 7.4 Device Functional Modes

**表 7-1. Mux Configuration Control Logic for TMUX121** (1)

| SEL | $\overline{EN}$ | Mux Configuration |
|---|---|---|
| L | L | D to SA |
| H | L | D to SB |
| X | H | All channels are disabled and Hi-Z |

(1) The TMUX121 can tolerate polarity inversions for differential signals. Keep the polarity consistent for all differential pairs.

# 8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TMUX121 is an analog high-speed mux or demux that can be used for routing differential as well as single ended signals through it. The device can be used for many interfaces including $I^2C$ and $I^3C$.

An available GPIO pin of a controller or hard tie to voltage level H or L can easily control the mux or demux selection pin (SEL) of the device as an application requires. The switch path is passive and therefore bidirectional.

## 8.2 Typical Applications

### 8.2.1 Signal Expansion ($I^3C$ and $I^2C$)

There are many applications in which microprocessors or controllers have a limited number of I/Os. The TMUX121 solution can effectively expand the limited I/Os by switching between multiple buses to interface them to a single microprocessor or controller. A common application where the TMUX121 is as a $I^3C$ 1:2 multiplexer. In this application, the TMUX121 is used to route communicating between different peripherals from a single controller or driver within a server, as shown in 图 8-1. The high bandwidth of the TMUX121 will preserve signal integrity at even the fastest communication protocols that may be used in server applications, such as $I^3C$. Also, because $I^3C$ is backwards compatible, any of the peripherals can also be $I^2C$, and the TMUX121 will still support it.

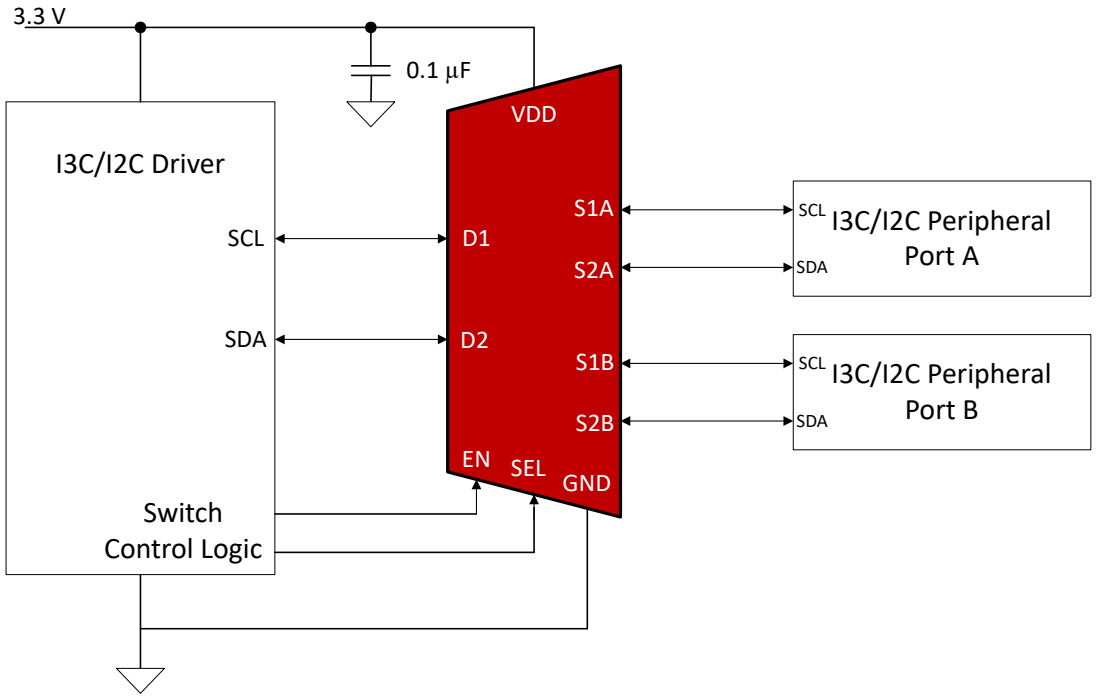



图 8-1. Typical Application

#### 8.2.1.1 Design Requirements

表 8-1. TMUX121 I3C Compatibility

| | I3C Requirements | TMUX121 Specification |
|---|---|---|
| Voltage | 1.0 V, 1.2 V, 1.8 V, 3.3 V | 0-3.6 V |
| Frequency | Up to 12.5 MHz | 3 GHz Bandwidth |
| Capacitance | 50 pF maximum bus capacitance | < 2 pF On or Off Capacitance |

#### 8.2.1.2 Detailed Design Procedure

The TMUX121 supports I3C standard by maintaining signal integrity through the switch. 表 8-1 details how the TMUX121 specifications make this device optimal for switching I3C signals. Choosing a multiplexer with very low capacitance helps reduces the impact to your total capacitance budget. This can enable more design flexibility keeping the total bus capacitance under 50 pF such as: longer traces, more ICs, multiple buses, and so forth.

#### 8.2.1.3 Application Curves

图 8-2 shows bandwidth of the TMUX121. This can easily support the max data rate of the I3C standard. A combination of low on-resistance, low capacitance, and low added jitter from the device allows it to be used for I3C.

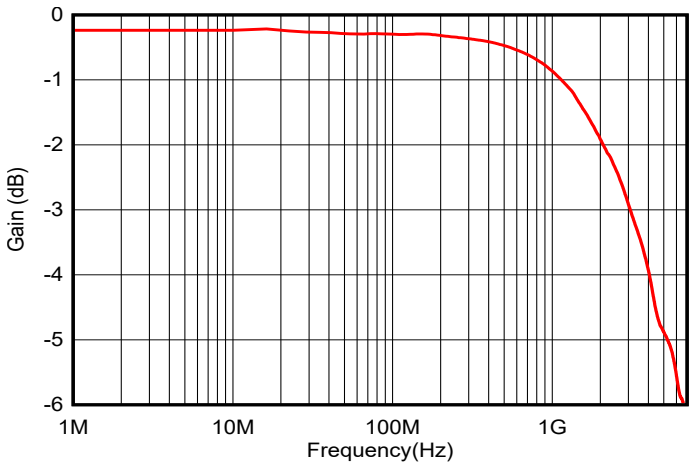



图 8-2. Typical Differential Bandwidth vs Frequency

## 8.3 Power Supply Recommendations

The TMUX121 does not require a power supply sequence. However, TI recommends to enable the device after VDD is stable and in specification. TI also recommends placing a bypass capacitor as close to the supply pin VDD as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Place supply bypass capacitors as close to VDD pin as possible and avoid placing the bypass capacitors near the high speed traces.

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. Doing this reduces reflections on the signal traces by minimizing impedance discontinuities. Avoid stubs on the high-speed signals because they cause signal reflections. Route all high-speed signal traces over continuous planes (VDD or GND) with no interruptions.

Due to high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 8-3.

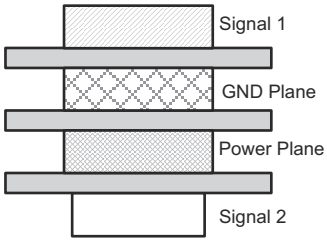



**图 8-3. Four-Layer Board Stack-Up**

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines* application note.

### 8.4.2 Layout Example

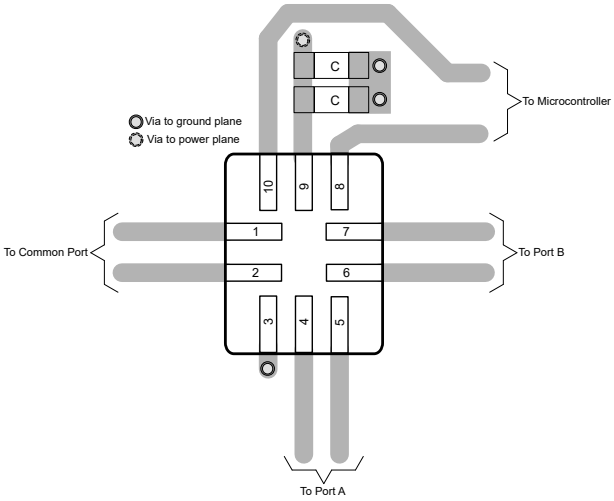



**图 8-4. TMUX121 Layout Example**

# 9 Device and Documentation Support

## 9.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High-Speed Layout Guidelines* application note

## 9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 9.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX121NKGR | ACTIVE | UQFN | NKG | 10 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

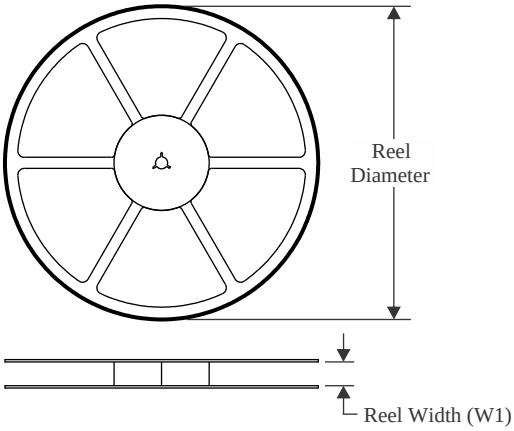
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

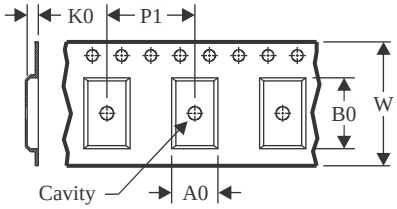
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

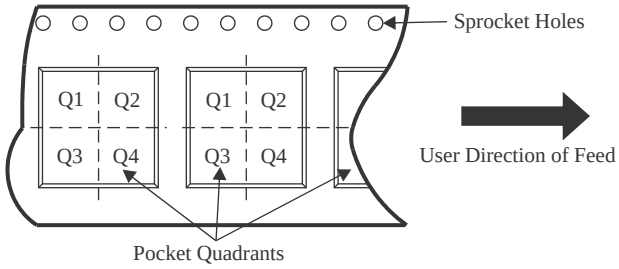



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

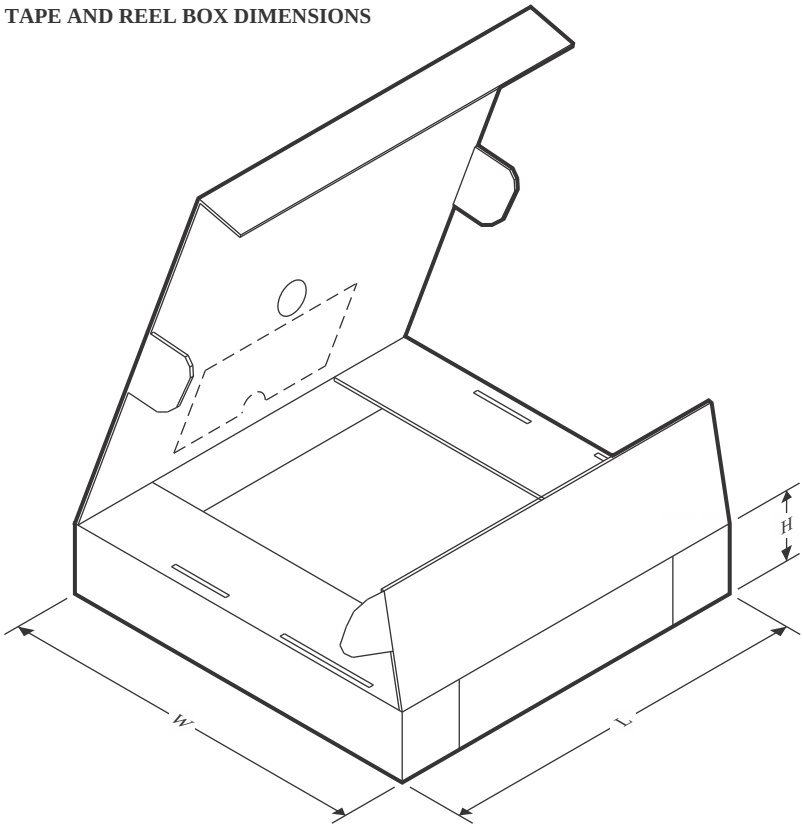
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX121NKGR | UQFN | NKG | 10 | 3000 | 180.0 | 8.4 | 1.6 | 2.0 | 0.7 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

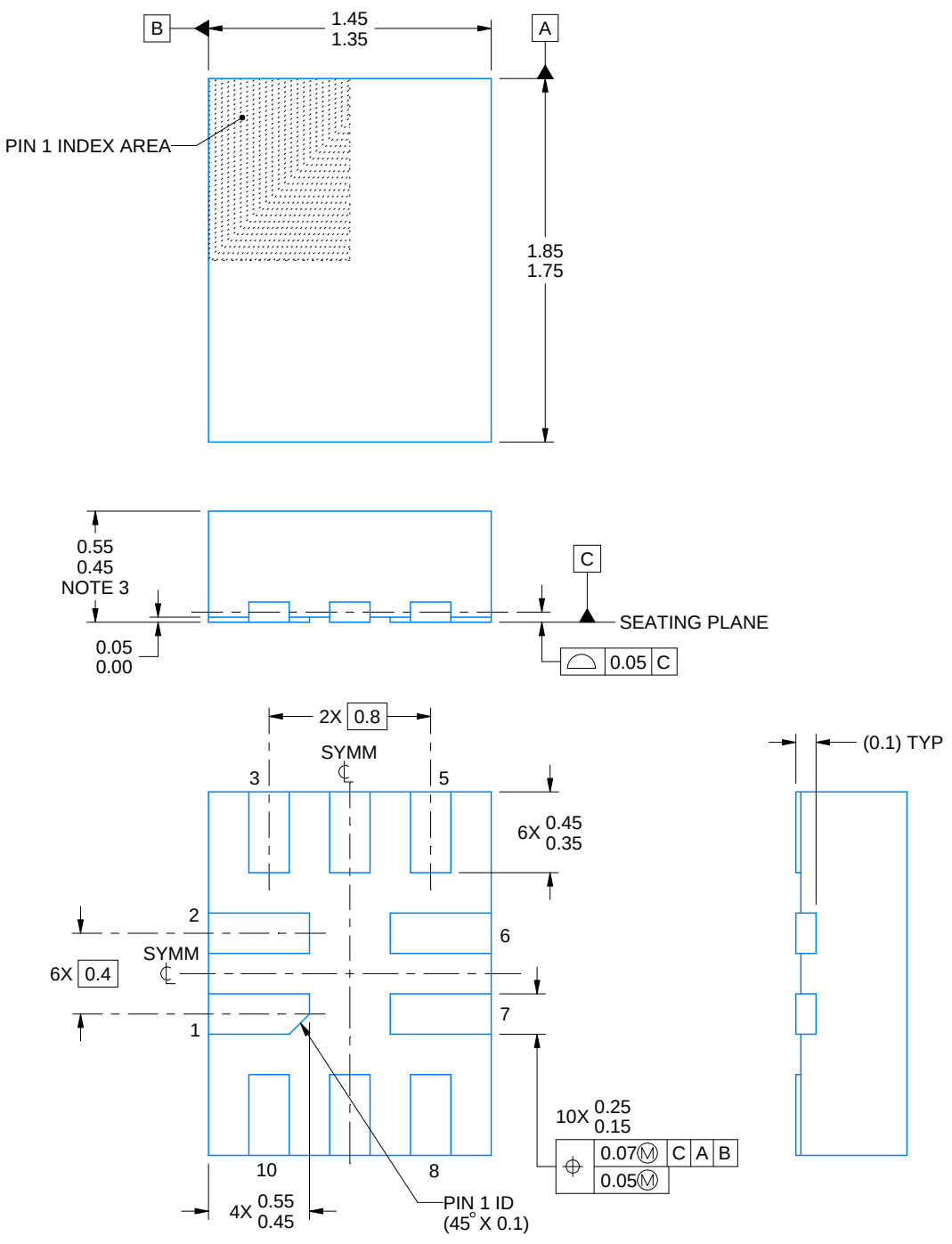
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMUX121NKGR | UQFN | NKG | 10 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## NKG0010A

## UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

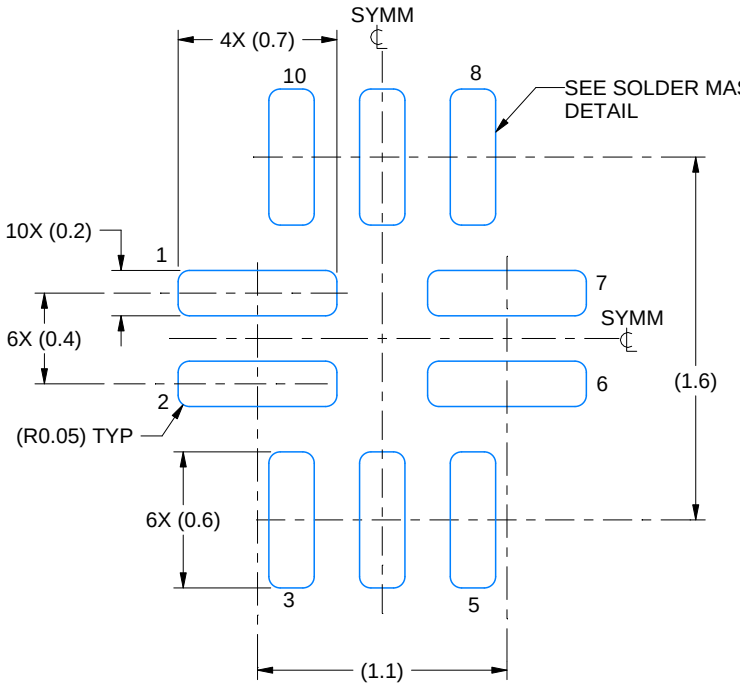
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

# EXAMPLE BOARD LAYOUT

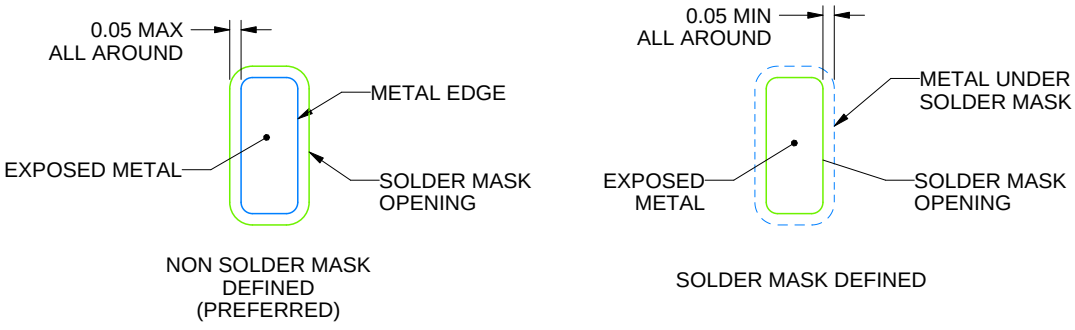
## NKG0010A

## UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

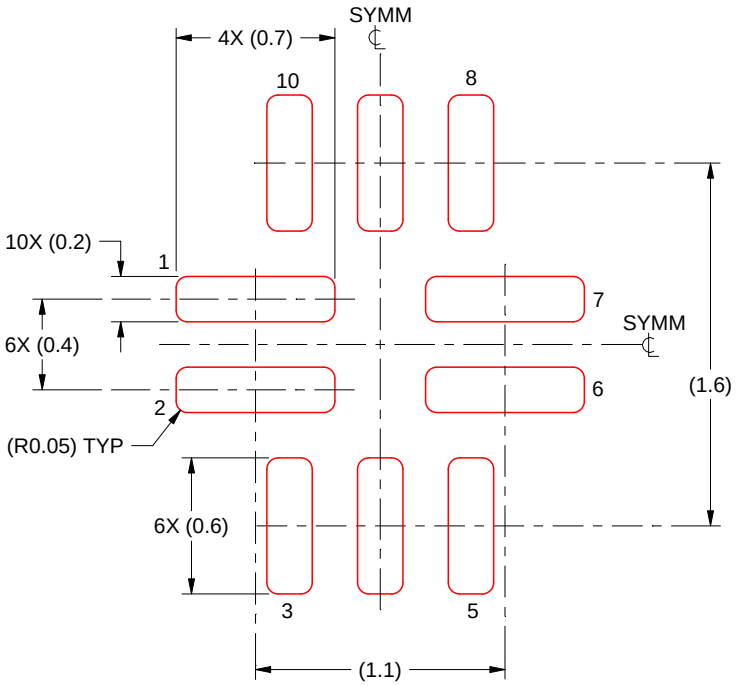



SOLDER MASK DETAILS

4228479/A 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 30X

4228479/A 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265