TMUX6119 ±16.5V 低电容、低泄漏电流、精密 SPDT 开关

1 特性

- 宽电源电压范围：±5V 至 ±16.5V（双）或 10V 至 16.5V（单）
- 所有引脚的闩锁性都能达到 100mA，符合 JESD78 II 类 A 级要求
- 低导通电容：6.4pF
- 低输入泄漏：0.5pA
- 低电荷注入：0.19pC
- 轨至轨运行
- 低导通电阻：120Ω
- 转换时间：68ns
- 先断后合开关操作
- EN 引脚和 SEL 引脚可连接至 V_{DD}（集成下拉电阻器）
- 逻辑电平：2V 至 V_{DD}
- 低电源电流：17µA
- 人体模型 (HBM) ESD 保护：针对所有引脚提供 ±2kV 保护
- 行业标准 SOT-23 封装

2 应用

- 工厂自动化和工业过程控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 自动测试设备 (ATE)
- 数字万用表
- 电池监控系统

3 说明

TMUX6119 是一款现代互补金属氧化物半导体 (CMOS) 单刀双掷 (SPDT)。该器件在双电源（±5V 至 ±16.5V）、单电源（10V 至 16.5V）或非对称电源供电时均能正常运行。两个数字输入引脚（EN 和 SEL）均具有兼容晶体管到晶体管逻辑 (TTL) 的阈值，这些阈值可确保 TTL/CMOS 逻辑兼容性。

可以通过控制 EN 引脚来启用或禁用 TMUX6119。当禁用时，两个通道开关都关闭。当启用时，SEL 引脚可用于打开通道 A（SA 至 D）或通道 B（SB 至 D）。每个通道在两个方向上都表现得很好，而且具有可扩展至电源的输入信号范围。TMUX6119 的开关具有先断后合 (BBM) 开关操作。

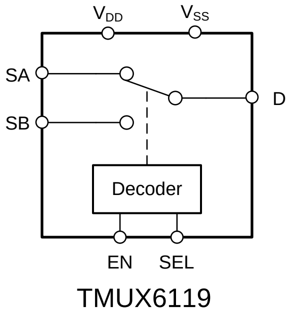
TMUX6119 是德州仪器 (TI) 精密开关和多路复用器系列中的一款产品。TMUX6119 具有非常低的泄漏电流和电荷注入，因此该器件可用于高精度测量 应用。当开关处于 OFF 位置时，该器件还可通过阻断到达电源的信号电平来提供出色的隔离能力。电源电流低至 17µA，使得该器件可用于便携式 应用。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TMUX6119	SOT-23 (8)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



English Data Sheet: SCDS384

目录

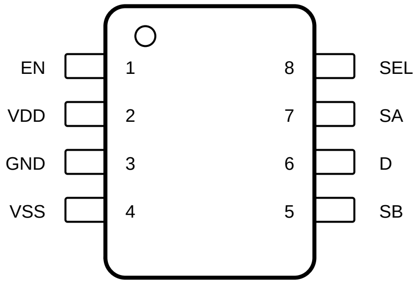
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2018) to Revision A	**Page**
• 文档状态从*预告信息* 改为*生产* 数据	1

5 Pin Configuration and Functions

DCN Package
8-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN	1	I	Active high digital input. When this pin is low, both switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on.
V_{DD}	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	3	P	Ground (0 V) reference
V_{SS}	4	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
SB	5	I/O	Source pin B. Can be an input or output.
D	6	I/O	Drain pin. Can be an input or output.
SA	7	I/O	Source pin A. Can be an input or output.
SEL	8	I	Logic control input.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		–0.3	18	V
V_{SS} to GND		–18	0.3	V
V_{DIG}	Digital input pin (SEL, EN) voltage	GND –0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (SEL, EN) current	–30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	–30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (D) current	–30	30	mA
T_A	Ambient temperature	–55	140	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX6119 DCN (SOT-23) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	138.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	73.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} [1]	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	–16.5		–5	V

(1) When V_{SS} = 0 V, V_{DD} can range from 10 V to 36 V.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S (2)	Source pins voltage	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (SEL, EN) voltage	0		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	–25		25	mA
T_A	Ambient temperature	–40		125	℃

(2) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 36 V.

6.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			120	135	Ω
		V_S = ±10 V, I_S = 1 mA			140	165	Ω
			T_A = –40°C to +85°C			210	Ω
			T_A = –40°C to +125°C			245	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			2.4	6	Ω
			T_A = –40°C to +85°C			9	Ω
			T_A = –40°C to +125°C			11	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = –10 V, 0 V, +10 V, I_S = 1 mA			22	45	Ω
			T_A = –40°C to +85°C			47	Ω
			T_A = –40°C to +125°C			49	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.5		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.12		0.05	nA
			T_A = –40°C to +125°C	–1		0.2	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.12		0.05	nA
			T_A = –40°C to +125°C	–1		0.2	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.25		0.1	nA
			T_A = –40°C to +125°C	–1.8		0.4	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			16	21	µA
			T_A = –40°C to +85°C			22	µA
			T_A = –40°C to +125°C			23	µA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			7	10	µA
			T_A = –40°C to +85°C			11	µA
			T_A = –40°C to +125°C			12	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		68	86	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			110	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			121	ns
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		57	64	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			78	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			82	ns
t_{TRAN}	Transition time	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF		68	88	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			99	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			106	ns
tBBM	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	8	37		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω , C_L = 1 nF		–0.19		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–93		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-7.7		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		–55		dB
		R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		–55		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		700		MHz
THD	Total harmonic distortion + noise	R_L = 10k Ω , C_L = 5 pF, f= 20Hz to 20kHz		0.08		%
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		0.8		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz		1.9	2.8	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 0 V, f = 1 MHz		4.3	4.7	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		6.4	8.1	pF

(1) Specified by design; not subject to production testing.

6.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range	T_A = –40°C to +125°C	T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			230	265	Ω
			T_A = –40°C to +85°C			355	Ω
			T_A = –40°C to +125°C			405	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			1	9	Ω
			T_A = –40°C to +85°C			12	Ω
			T_A = –40°C to +125°C			14	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.48		%/°C

Electrical Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.08		0.04	nA
			T_A = –40°C to +125°C	–0.75		0.13	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.08		0.04	nA
			T_A = –40°C to +125°C	–0.75		0.13	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.16		0.08	nA
			T_A = –40°C to +125°C	–1.5		0.25	nA
DIGITAL INPUT (EN, Ax pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			11	14	µA
			T_A = –40°C to +85°C			16	µA
			T_A = –40°C to +125°C			17	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		73	91	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			119	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			130	ns
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		60	69	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			82	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			88	ns
t_{TRAN}	Transition time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		73	93	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			104	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			112	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	10	45		ns
Q_J	Charge injection	V_S = 6 V, R_S = 0 Ω , C_L = 1 nF		0.1		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–100		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-15		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V, f= 1 MHz		–55		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		440		MHz
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1		pF

(1) Specified by design; not subject to production testing.

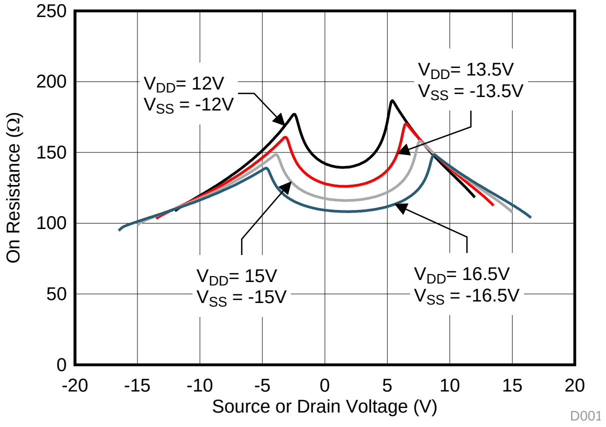
Switching Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz		2	2.9	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 6 V, f = 1 MHz		4.9	5.3	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		7.4	8.9	pF

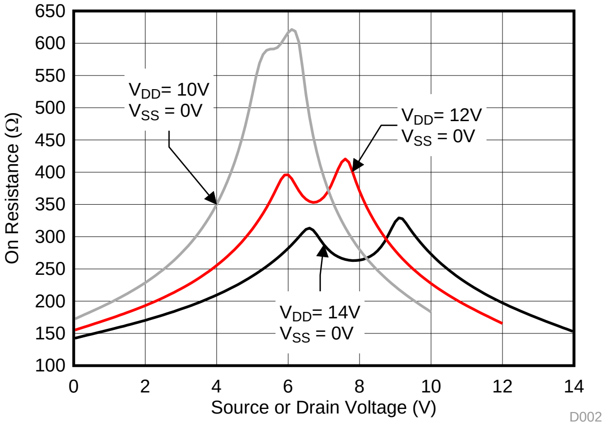
6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



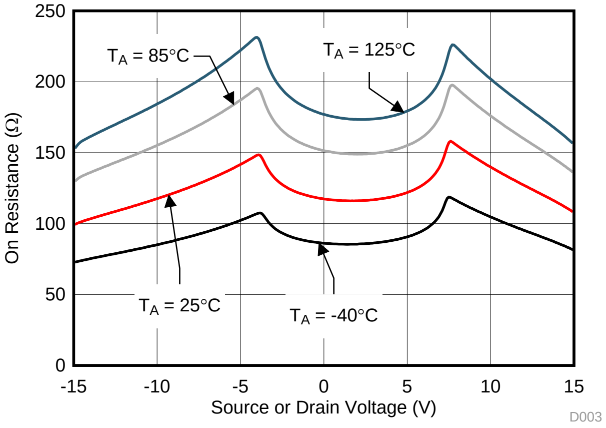
Dual Supply Operation (T_A = 25°C)

图 1. On-Resistance vs Source or Drain Voltage



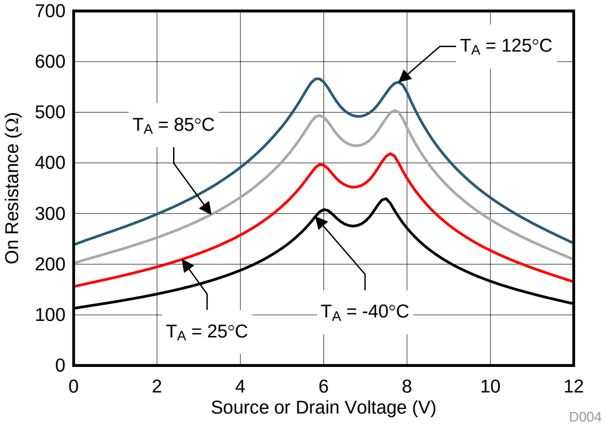
Single Supply Operation (T_A = 25°C)

图 2. On-Resistance vs Source or Drain Voltage



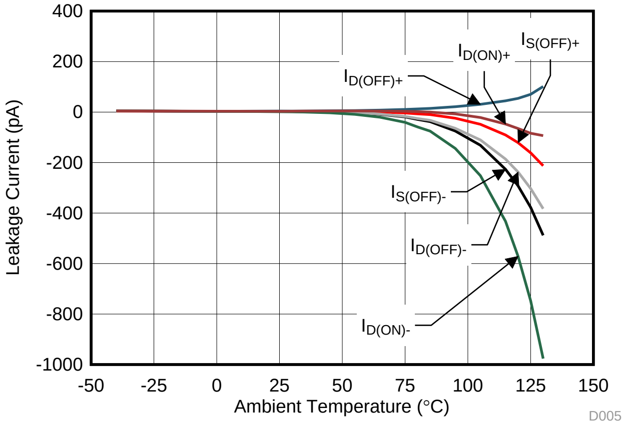
V_{DD} = 15 V, V_{SS} = –15 V

图 3. On-Resistance vs Source or Drain Voltage



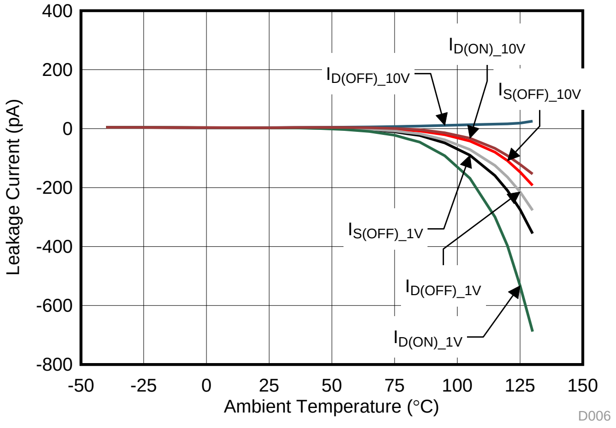
V_{DD} = 12 V, V_{SS} = 0 V

图 4. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = –15 V

图 5. . Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0 V

图 6. Leakage Current vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

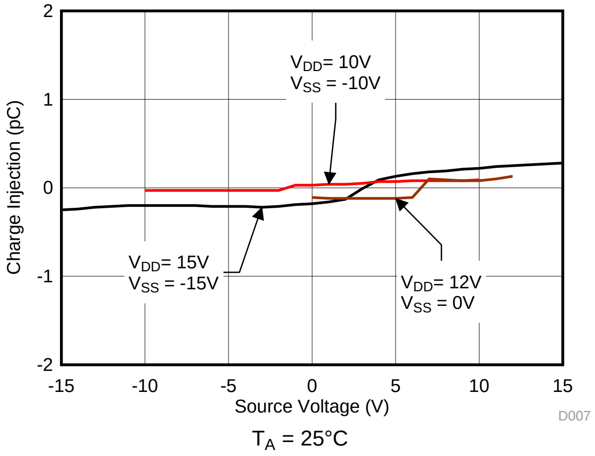


图 7. Charge Injection vs Source Voltage

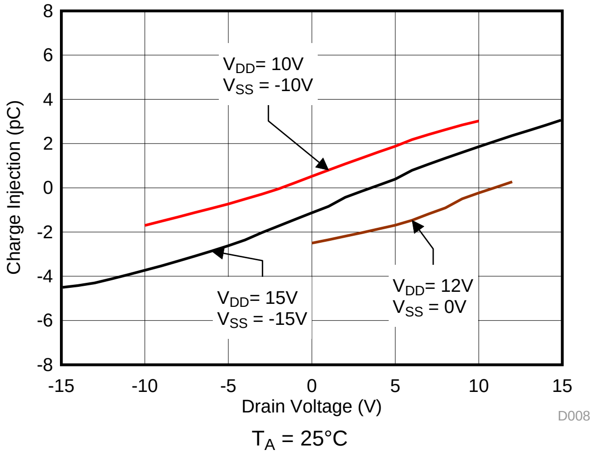


图 8. Charge Injection vs Drain Voltage

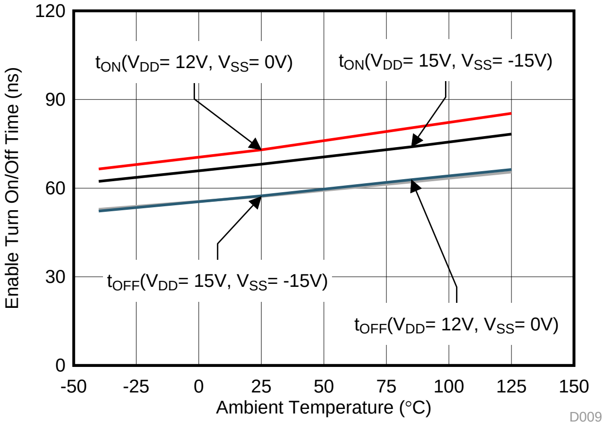


图 9. Enable turn-on and turn-off time

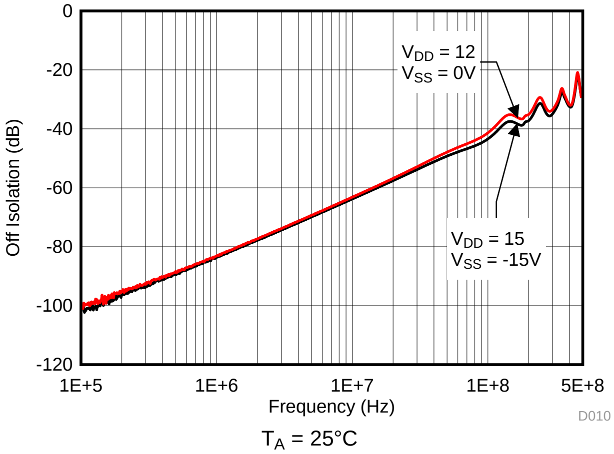


图 10. Off Isolation vs Frequency

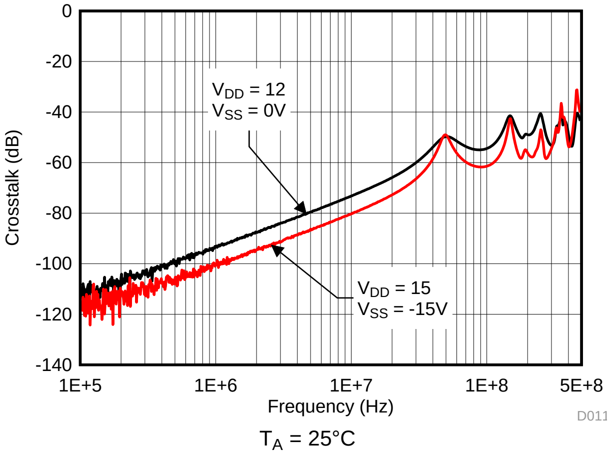


图 11. Crosstalk vs Frequency

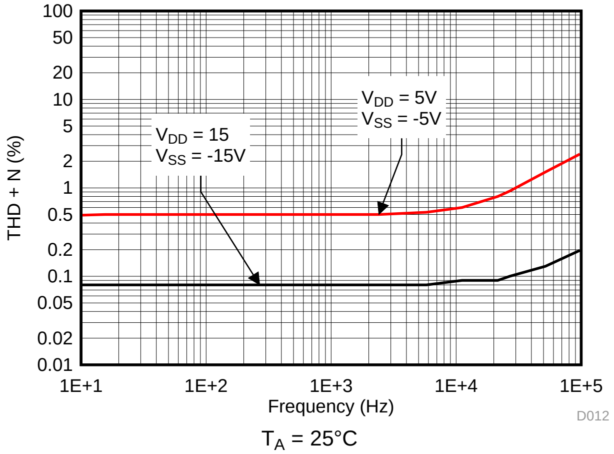
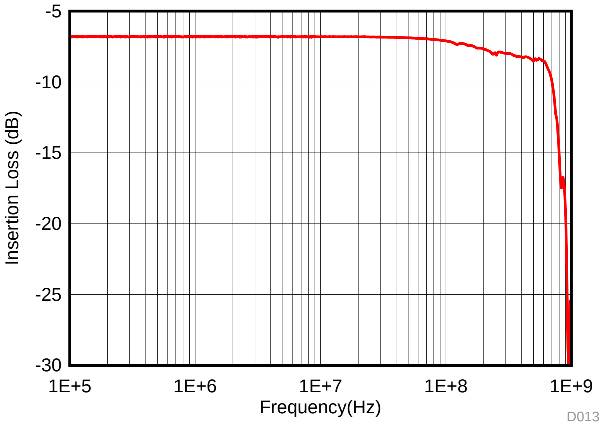


图 12. THD+N vs Frequency

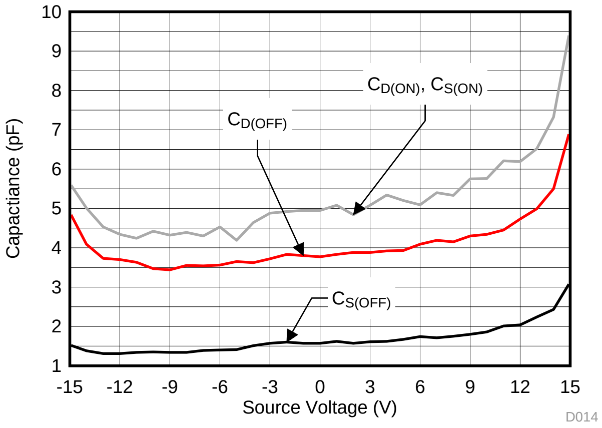
Typical Characteristics (接下页)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



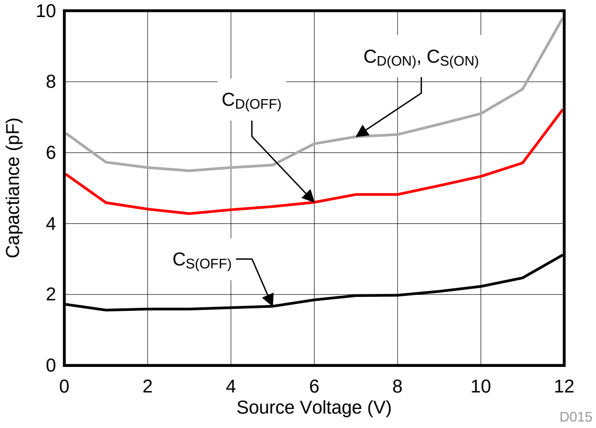
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

图 13. On Response vs Frequency



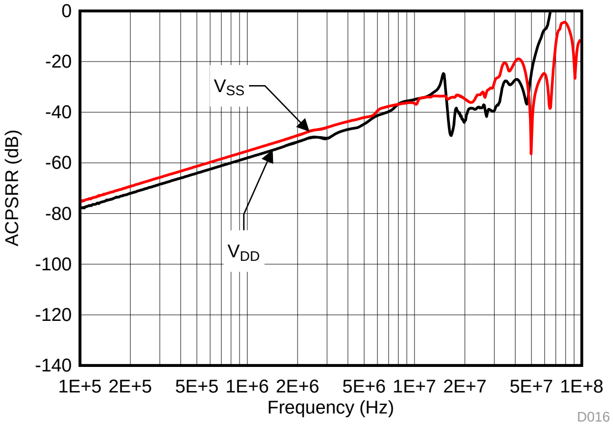
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

图 14. Capacitance vs Source Voltage



V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C

图 15. Capacitance vs Source Voltage



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

图 16. ACPSRR vs Frequency

7 Parameter Measurement Information

7.1 Truth Tables

表 1 shows the truth tables for theTMUX6119.

表 1. TMUX6119 Truth Table

EN	SEL	STATE	
		Switch A (SA to D)	Switch B (SB to D)
0	X(1)	OFF	OFF
1	0	ON	OFF
1	1	OFF	ON

(1) X denotes *don't care*..

8 Detailed Description

8.1 Overview

The TMUX6119 has a low on and off leakage currents and ultra-low charge injection, allowing the device to be used in high precision measurement applications. The device also provides excellent isolation capability by blocking signal levels up to the supplies when the switches are in the OFF position. A low supply current of 17 µA enables usage in portable applications.

8.1.1 On-Resistance

The on-resistance of the TMUX6119 is the ohmic resistance across the source (SA or SB) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 17. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 公式 1:

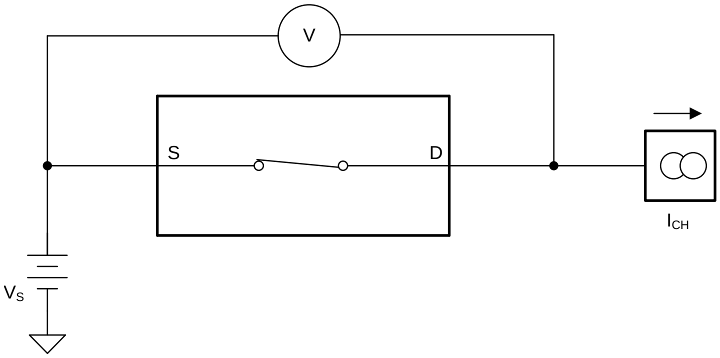


图 17. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

8.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 18.

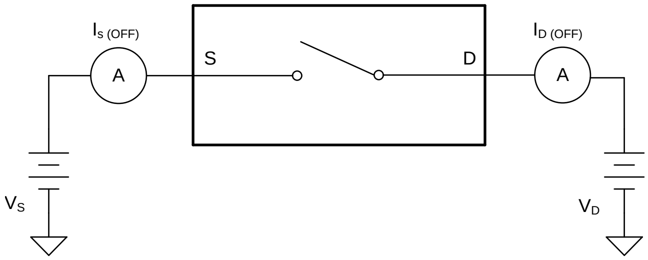


图 18. Off-Leakage Measurement Setup

Overview (接下页)

8.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. 图 19 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

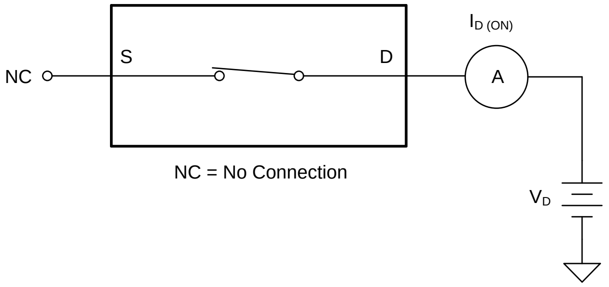


图 19. On-Leakage Measurement Setup

8.1.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX6119 to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. 图 20 shows the setup used to measure transition time, denoted by the symbol t_t.

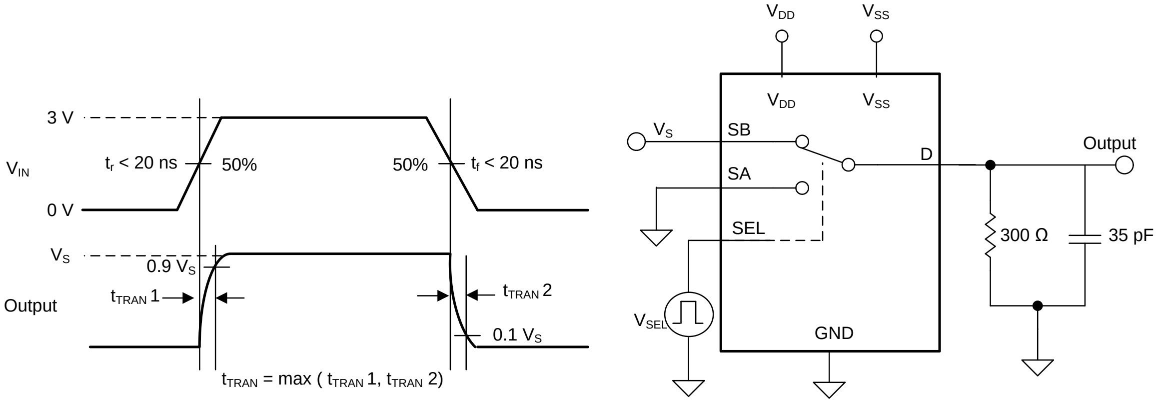


图 20. Transition-Time Measurement Setup

Overview (接下页)

8.1.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX6119 is switching. The TMUX6119 output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 21 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

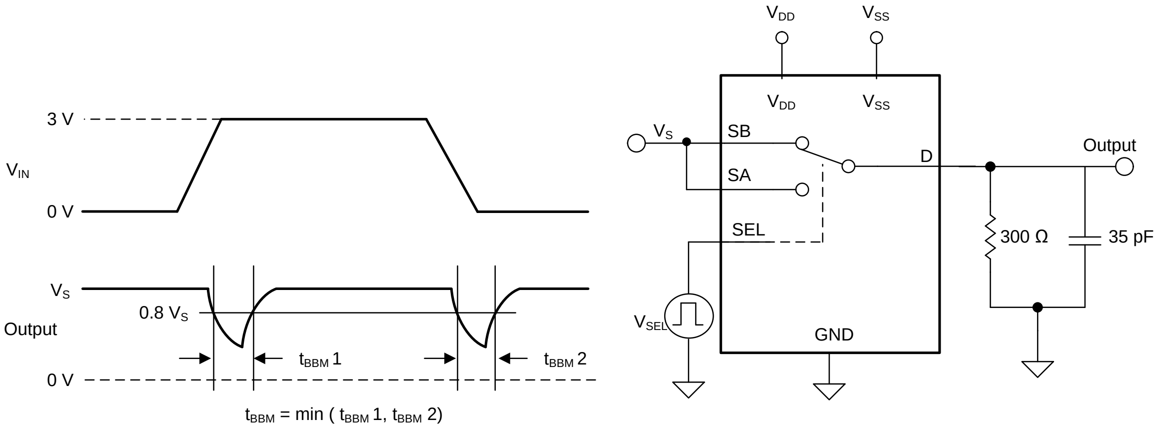


图 21. Break-Before-Make Delay Measurement Setup

8.1.6 Enable Turn-On and Enable Turn-Off Time

Enable turn-on time is defined as the time taken by the output of the TMUX6119 to rise to a 90% final value after the EN signal has risen to a 50% final value. 图 22 shows the setup used to measure turn-on time. Enable turn-on time is denoted by the symbol t_{ON}.

Enable turn off time is defined as the time taken by the output of the TMUX6119 to fall to a 10% initial value after the EN signal has fallen to a 50% initial value. 图 22 shows the setup used to measure turn-off time. Enable Turn-off time is denoted by the symbol t_{OFF}.

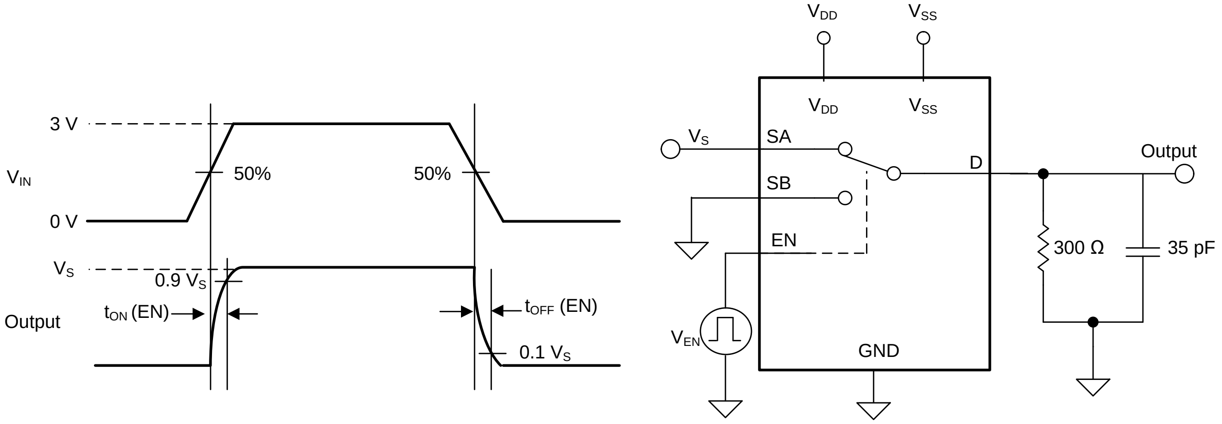


图 22. Turn-On and Turn-Off Time Measurement Setup

Overview (接下页)

8.1.7 Charge Injection

The TMUX6119 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 图 23 and 图 24 shows the setup used to measure charge injection from source to drain and from drain to source. The charge injection is optimized for the TMUX6119 from the direction of source to drain.

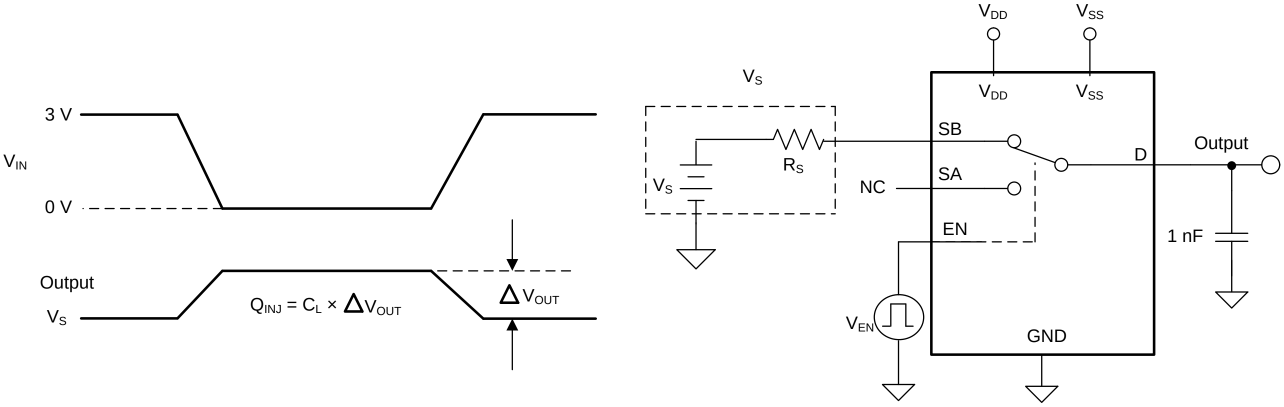


图 23. Source to Drain Charge-Injection Measurement Setup

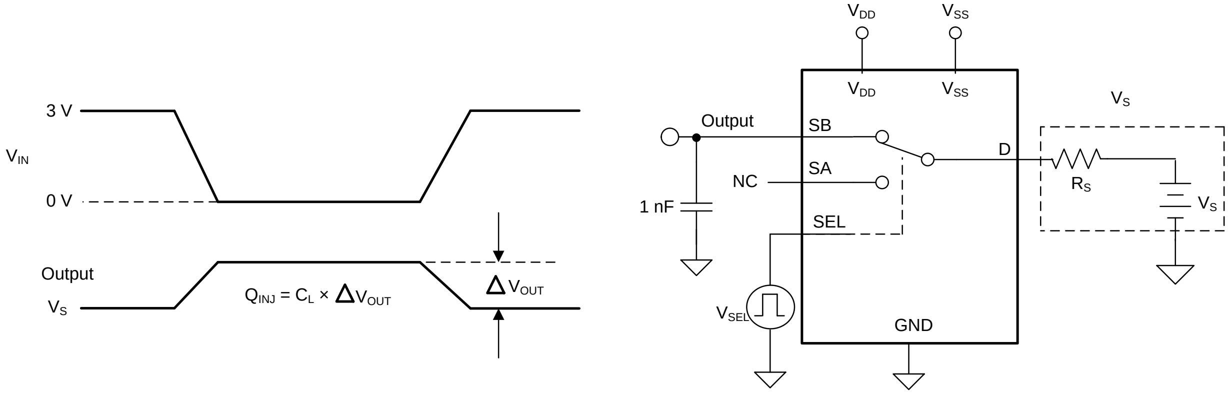


图 24. Drain to Source Charge-Injection Measurement Setup

8.1.8 Off Isolation

Off isolation is defined as the voltage at the drain pin (D) of the TMUX6119 when a 1-V_{RMS} signal is applied to the source pin (SA or SB) of an off-channel. 图 25 shows the setup used to measure off isolation. Use 公式 2 to compute off isolation.

Overview (接下页)

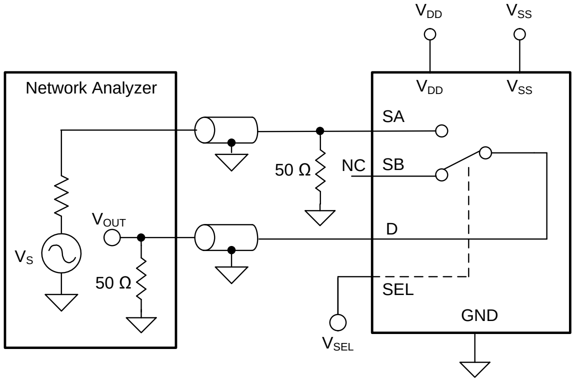


图 25. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

8.1.9 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (SA or SB) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin of an on-channel. 图 26 shows the setup used to measure, and 公式 3 is the equation used to compute, channel-to-channel crosstalk.

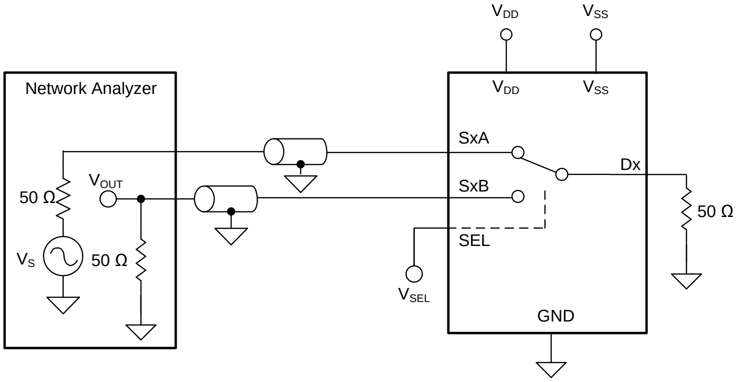


图 26. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

8.1.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin of an on-channel, and the output is measured at the drain pin of the TMUX6119. 图 27 shows the setup used to measure bandwidth of the mux. Use 公式 4 to compute the attenuation.

Overview (接下页)

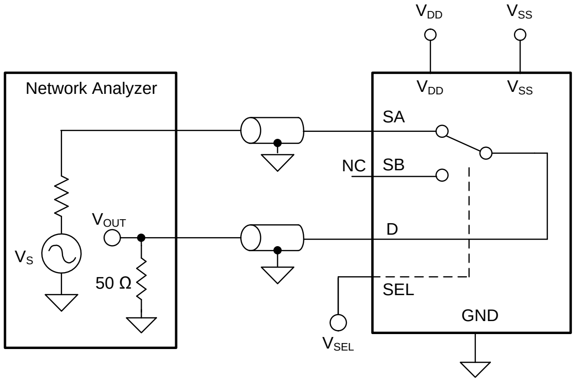


图 27. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \tag{4}$$

8.1.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6119 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 图 28 shows the setup used to measure THD+N of the TMUX6119.

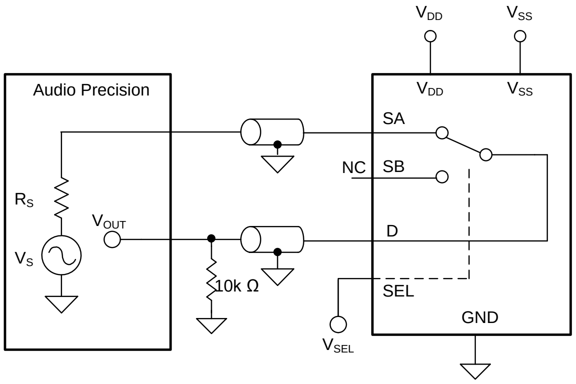
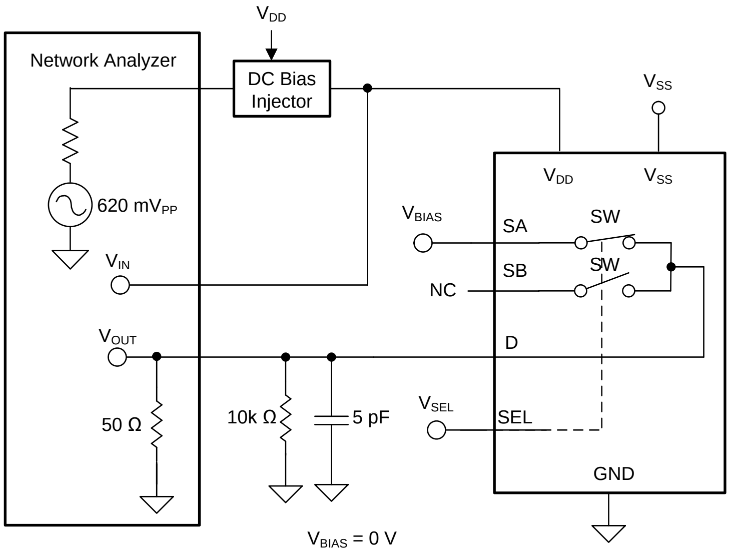


图 28. THD+N Measurement Setup

Overview (接下页)

8.1.12 AC Power Supply Rejection Ratio (AC PSRR)

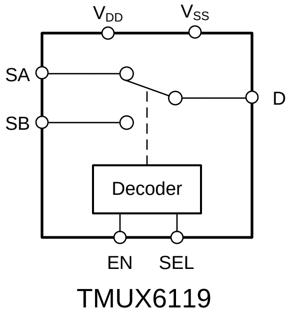
AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR. 图 29 shows the setup used to measure ACPSRR of the TMUX6119.



V_{BIAS} = 0 V
ACPSRR= 20 × Log (V_{OUT}/ V_{IN})

图 29. AC PSRR Measurement Setup

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Ultra-low Leakage Current

The TMUX6119 provide extremely low on- and off-leakage currents. The TMUX6119 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 图 30 shows typical leakage currents of the TMUX6119 versus temperature.

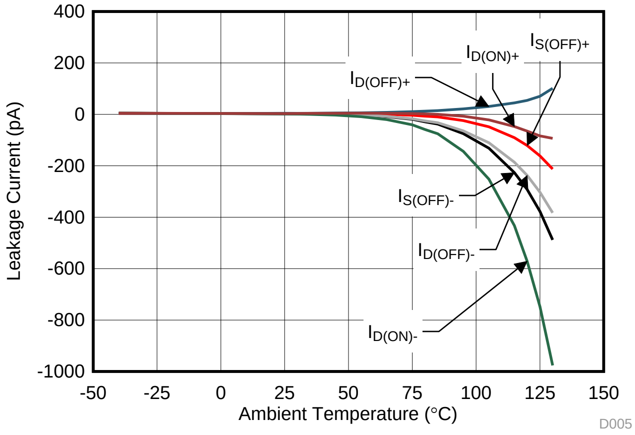


图 30. Leakage Current vs Temperature

8.3.2 Ultra-low Charge Injection

The TMUX6119 is implemented with simple transmission gate topology, as shown in 图 31. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

Feature Description (接下页)

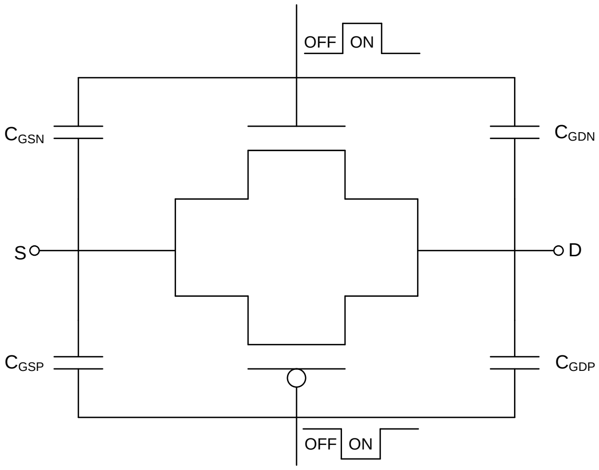


图 31. Transmission Gate Topology

The TMUX6119 utilizes special charge-injection cancellation circuitry that reduces the source (SA or SB)-to-drain (D) charge injection to as low as 0.19 pC at V_S = 0 V, as shown in 图 32.

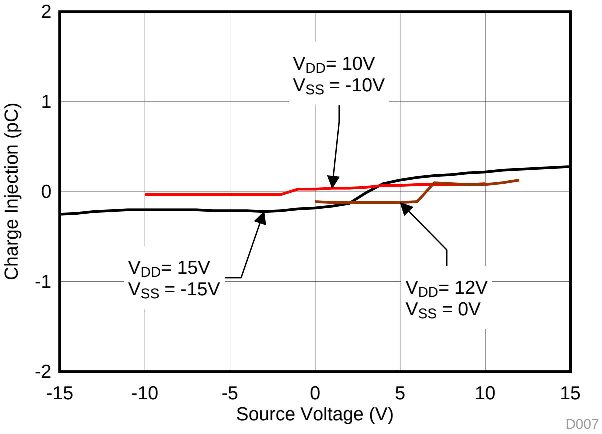


图 32. Charge Injection vs Source Voltage

The drain (D)-to-source (SA or SB) charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. 图 33 shows the drain-to-source charge injection across the full signal range.

Feature Description (接下页)

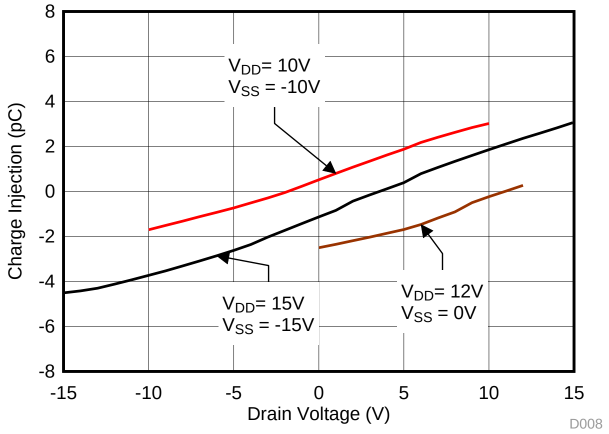


图 33. Charge Injection vs Drain Voltage

8.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6119 conducts equally well from source (SA or SB) to drain (D) or from drain (D) to source (SA or SB). Each TMUX6119 channel has very similar characteristics in both directions. The valid analog signal for TMUX6119 ranges from V_{SS} to V_{DD}. The input signal to the TMUX6119 swings from V_{SS} to V_{DD} without any significant degradation in performance.

8.4 Device Functional Modes

When the EN pin of the TMUX6119 is pulled high, one of the two switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both switches remain open irrespective of the state of the SEL pin. The EN pin is weakly pull-down internally through a 6MΩ resistor, thereby setting each channel to the open state if the EN pin is not actively driven. The SEL pin is also weakly pulled-down through an internal 6Mohm resistor, allowing channel A (SA to D) to be selected by default when EN pin is driven high. Both the EN pin and the SEL pin can be connected to V_{DD} (as high as 16.5 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX6119 offers outstanding input / output leakage current and ultra-low charge injection performance. The on-capacitance of the TMUX6119 is also very low. These properties make the TMUX6119 ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

9.2 Typical Application

One application to take advantage of TMUX6119's precision performance is the implementation of the chopper amplifier. The chopper amplifier was developed in the 1950s to achieve ultra-low offset voltage and low offset voltage drift over time and temperature. It also drastically reduces low frequency 1/f (flicker) noise. These attributes make the chopper amplifier ideal for small signal conditioning. 图 34 illustrates a classic example of a simple chopper amplifier implemented with two TMUX6119 SPDT switches.

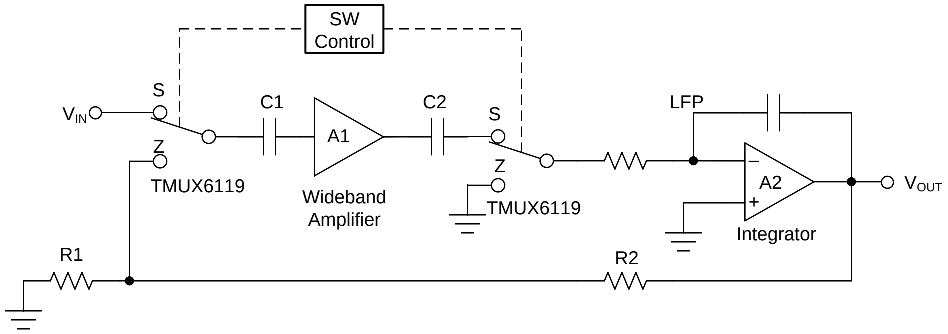


图 34. Example of classic chopper amplifier implemented with two TMUX6119

9.2.1 Design Requirements

The goal of a chopper-amplifier design is to produce extremely high DC precision by continuously self-cancelling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage, while reducing low-frequency 1/f (flicker) voltage.

Typical Application (接下页)

9.2.2 Detailed Design Procedure

The theory of operation for the chopper amplifier relies on the concept of converting a DC input signal to AC before feeding it into an AC-coupled wideband amplifier. The conversion utilizes a SPDT switches to “chop” the input DC signal into an AC voltage. The output of the amplifier is then modulated by another SPDT switch to convert the signal back to DC. The output of the switch is then low-pass filtered (or integrated) to smooth and produce the final DC output.

The operation of the chopper amplifier consists of 2 phases, the sampling (S) phase and the auto-zero (Z) phase. During the auto-zero phase, the switches are toggled to the Z position, and capacitors C1 and C2 are charged to the amplifier input and output offset voltage, respectively. During the sampling phase, the switches are toggled to the S position, during which VIN is connected to VOUT through C1, the wideband amplifier, C2, and the integrator. Input DC voltage is AC-coupled by capacitor C1 and amplified by the wideband amplifier A1. C2 helps reduce any DC component caused by the amplifier’s input offset voltage, and the integrator helps smooth out the output signals to produce desired DC voltage output.

Several mechanisms helps reduce overall noise of the chopper-amplifier design. The DC gain, being the product of the AC stage and the DC gain of the integrator, can easily reach an open-loop gain of 160 dB or higher and therefore reduce the gain error, V_{OUT}/ (A1×A2) to almost zero. The offset and drift in the output integrator stage are nulled by the DC gain of the preceding AC stage. DC drifts in the AC stage are also non-factors because the amplification stage is AC-coupled. The 1/f noise of the wideband amplifier is modulated to higher frequencies by the demodulator.

Note that the input signal frequency shall be much less than one-half of the chopping frequency to prevent aliasing errors in this chopper amplifier implementation. The chopper frequency, in turn, is restricted by the wideband amplifier’s gain-phase limitations as well as errors induced by switch transition time and charge injection. The TMUX6119 ‘s switch transition time is only 68 ns (typ) and average charge injection is less than 0.19pC, making it ideal for the chopper amplifier implementation. However, the input signal frequency is still limited by the amplifier’s performance. If higher sampling frequency is required, a chopper-stabilized amplifier, or an integrated zero-drift amplifier (such as the OPA2188), can be used to satisfy the requirement.

9.2.3 Application Curve

Fast transition time and small charge injection are two critical parameters for the SPDT switches used in the chopper amplifier design. 图 35 shows the plot for the charge injection vs. source voltage for the TMUX6119.

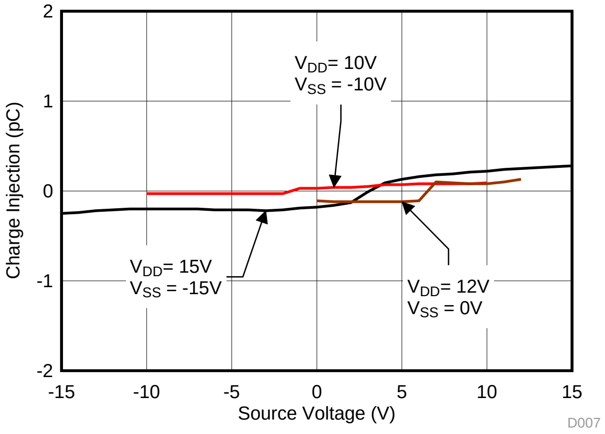


图 35. Charge Injection vs Source Voltage

10 Power Supply Recommendations

The TMUX6119 operates across a wide supply range of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode). They also perform well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground.

The on-resistance of the TMUX6119 varies with supply voltage, as illustrated in 图 36.

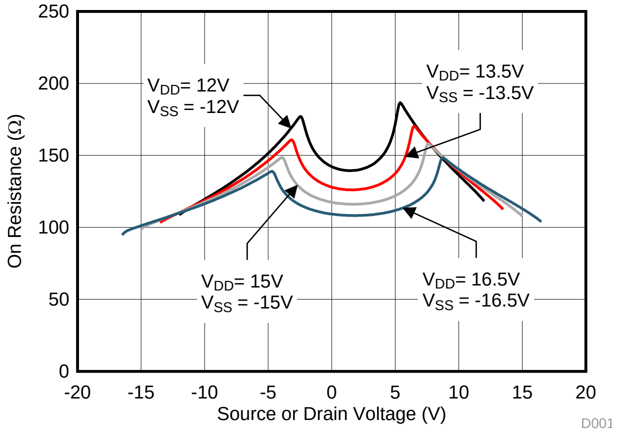


图 36. On-Resistance Variation With Supply and Input Voltage

11 Layout

11.1 Layout Guidelines

图 37 shows an example of a PCB layout with the TMUX6119.

Some key considerations are:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible. In case of the differential signal, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

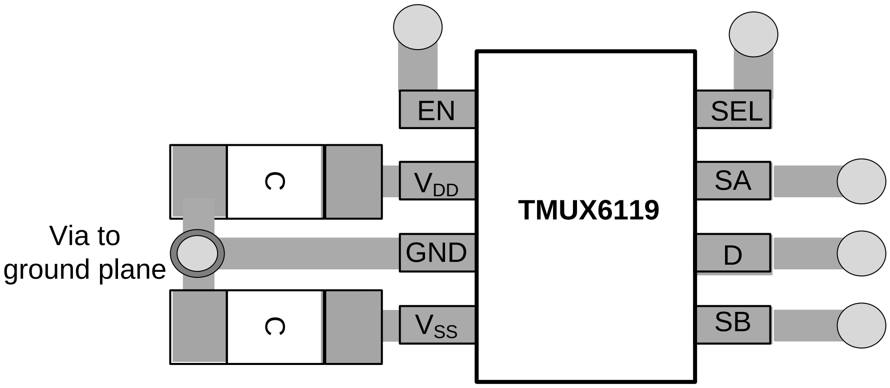


图 37. TMUX6119 Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

- *《OPA2188 0.03μV/°C 漂移，低噪声、轨至轨输出、36V、零漂移运算放大器》*(SBOS525)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区。*此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6119DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1QAC	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

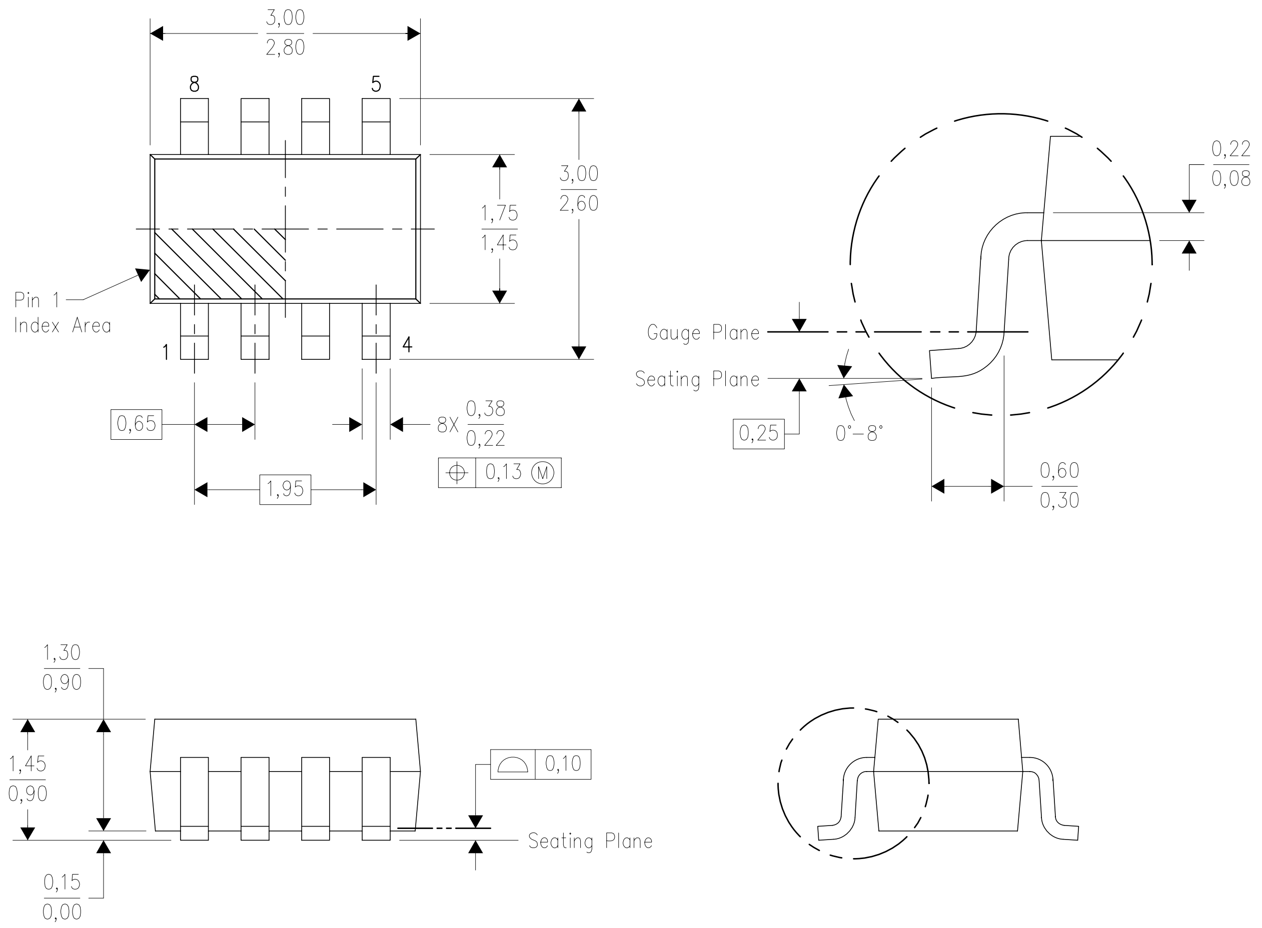
[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4202106/D 11/2009

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
- D. Package outline inclusive of solder plating.
- E. A visual index feature must be located within the Pin 1 index area.
- F. Falls within JEDEC MO–178 Variation BA.
- G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122