TMUX612x ±16.5V、低电容、低漏电流、精密双路 SPST 开关

1 特性

- 宽电源电压范围：±5V 至 ±16.5V（双电源）或 10V 至 16.5V（单电源）
- 所有引脚的闩锁性能都达到 100mA，符合 JESD78 II 类 A 级要求
- 低导通电容：4.2pF
- 低输入泄漏电流：0.5pA
- 低电荷注入：0.51 pC
- 轨到轨运行
- 低导通电阻：120Ω
- 快速开关导通时间：68ns
- 先断后合开关 (TMUX6123)
- SELx 引脚可连接至带集成下拉电阻器的 V_{DD}
- 逻辑电平：2V 至 V_{DD}
- 低电源电流：16μA
- 人体放电模型 (HBM) ESD 保护：所有引脚上均为 ±2kV
- 业界通用的 VSSOP 封装

2 应用

- 工厂自动化和工业过程控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- ATE 测试设备
- 数字万用表
- 电池监控系统

3 说明

TMUX6121、TMUX6122 和 TMUX6123 是现代化的互补金属氧化物半导体 (CMOS) 器件，具有两个独立的可选单刀单掷 (SPST) 开关。该器件在双电源（±5V 至 ±16.5V）、单电源（10V 至 16.5V）或非对称电源供电时均能正常运行。所有数字输入均具有兼容晶体管到晶体管逻辑 (TTL) 的阈值，这些阈值可确保 TTL 和 CMOS 逻辑兼容性。

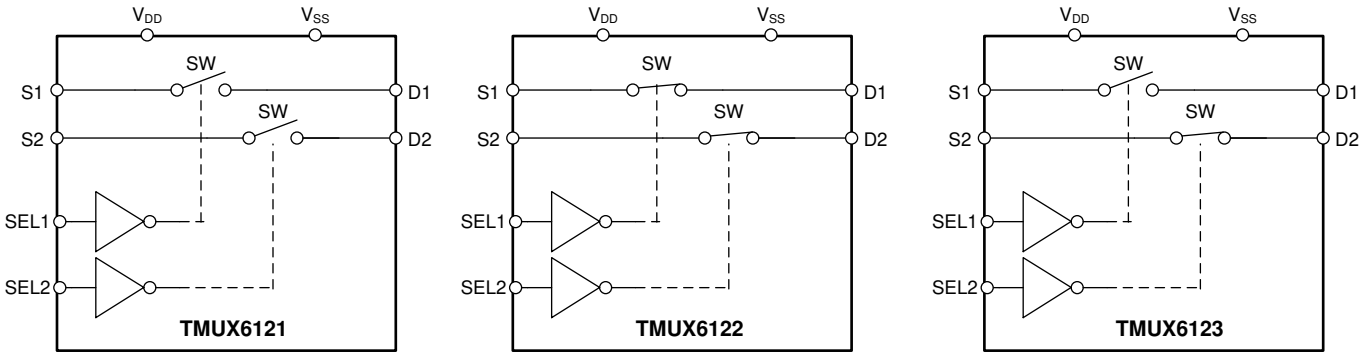
逻辑 1 会打开 TMUX6121 中数字控制输入上的开关。要打开 TMUX6122 中的开关，则需要逻辑 0。TMUX6123 有一个开关的数字控制逻辑与 TMUX6121 类似，而另外一个开关上的逻辑则与之相反。TMUX6123 具有先断后合开关，因此可用于交叉点开关应用。

TMUX6121、TMUX6122、TMUX6123 是精密开关和多路复用器器件系列的一部分。这些器件具有非常低的漏电流和低电荷注入，因此可用于高精度测量应用。由于具有 16μA 的低电源电流，因此这些器件可用于便携式应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMUX6121	VSSOP (10)	3.00mm × 3.00mm
TMUX6122		
TMUX6123		

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2018) to Revision A (July 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

5 Pin Configuration and Functions

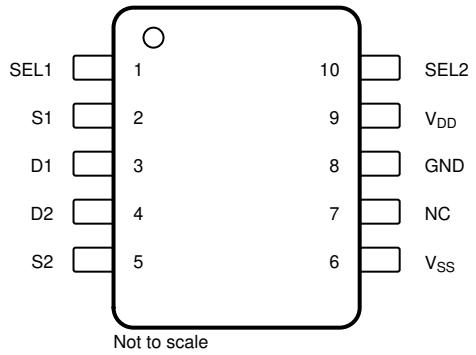


图 5-1. DGS Package, 10-Pin VSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SEL1	1	I	Logic control input 1.
S1	2	I/O	Source pin 1. Can be an input or output.
D1	3	I/O	Drain pin 1. Can be an input or output.
D2	4	I/O	Drain pin 2. Can be an input or output.
S2	5	I/O	Source pin 2. Can be an input or output.
V_{SS}	6	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
NC	7	No Connect	No internal connection.
GND	8	P	Ground (0 V) reference.
V_{DD}	9	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
SEL2	10	I	Logic control input 2.

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		–0.3	18	V
V_{SS} to GND		–18	0.3	V
V_{DIG}	Digital input pin (SEL1, SEL2) voltage	GND –0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (SEL1, SEL2) current	–30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS} –0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	–30	30	mA
V_{ANA_OUT}	Analog output pin (Dx) voltage	V_{SS} –0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (Dx) current	–30	30	mA
T_A	Ambient temperature	–55	140	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX6121/ TMUX6122/ TMUX6123 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	103.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	101.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} (1)	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	– 16.5		– 5	V
V_S	Source pins voltage(2)	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{SEL}	Select pin (SEL1, SEL2) voltage	V_{SS}		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	– 25		25	mA
T_A	Ambient temperature	– 40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 10 V ⩽ (V_{DD} – V_{SS}) ⩽ 33 V.
(2) V_S is the voltage on both S pins.

6.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = −15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range	T_A = – 40°C to +125°C	T_A = – 40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			120	135	Ω
		V_S = ±10 V, I_S = 1 mA			140	165	Ω
			T_A = – 40°C to +85°C			210	Ω
			T_A = – 40°C to +125°C			245	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			2.4	6	Ω
			T_A = – 40°C to +85°C			9	Ω
			T_A = – 40°C to +125°C			11	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = – 10 V, 0 V, +10 V, I_S = 1 mA			22	45	Ω
			T_A = – 40°C to +85°C			47	Ω
			T_A = – 40°C to +125°C			49	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.5		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ – 10 V, V_D = – 10 V/ + 10 V		– 0.02	0.005	0.02	nA
			T_A = – 40°C to +85°C	– 0.12		0.05	nA
			T_A = – 40°C to +125°C	– 1		0.2	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ – 10 V, V_D = – 10 V/ +10 V		– 0.02	0.005	0.02	nA
			T_A = – 40°C to +85°C	– 0.12		0.05	nA
			T_A = – 40°C to +125°C	– 1		0.2	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ – 10 V, V_D = – 10 V/ +10 V		– 0.04	0.01	0.04	nA
			T_A = – 40°C to +85°C	– 0.25		0.1	nA
			T_A = – 40°C to +125°C	– 1.8		0.4	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(IN)}$	Pull-down resistance on INx pins				6		MΩ
POWER SUPPLY							

6.5 Electrical Characteristics (Dual Supplies: ±15 V) (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = −15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			16	21	µA
			T_A = –40°C to +85°C			22	µA
			T_A = –40°C to +125°C			23	µA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			7	10	µA
			T_A = –40°C to +85°C			11	µA
			T_A = –40°C to +125°C			12	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = −15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Switch turn-on time	V_S = ±10 V, R_L = 300 Ω, C_L = 35 pF		68	86	ns
		V_S = ±10 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +85°C			110	ns
		V_S = ±10 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +125°C			121	ns
t_{OFF}	Switch turn-off time	V_S = ±10 V, R_L = 300 Ω, C_L = 35 pF		57	76	ns
		V_S = ±10 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +85°C			82	ns
		V_S = ±10 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +125°C			85	ns
t_{BBM}	Break-before-make time delay (TMUX6123 Only)	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +125°C	20	40		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF		0.51		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		–85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		–110		dB
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		–7.7		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ, C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		–61		dB
		R_L = 10 kΩ, C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		–61		dB
BW	−3 dB Bandwidth	R_L = 50 Ω, C_L = 5 pF		630		MHz
THD	Total harmonic distortion + noise	R_L = 10 kΩ, C_L = 5 pF, f= 20 Hz to 20 kHz		0.08		%
C_{IN}	Digital input capacitance	V_{SELx} = 0 V or V_{DD}		1.2		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz		1.9	2.5	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 0 V, f = 1 MHz		2.2	2.6	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		4.2	5	pF

6.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH						
V_A	Analog signal range	T_A = –40°C to +125°C	V_{SS}		V_{DD}	V

6.7 Electrical Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			230	265	Ω
			T_A = –40°C to +85°C			355	Ω
			T_A = –40°C to +125°C			405	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			1	9	Ω
			T_A = –40°C to +85°C			12	Ω
			T_A = –40°C to +125°C			14	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.48		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.08		0.04	nA
			T_A = –40°C to +125°C	–0.75		0.13	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.08		0.04	nA
			T_A = –40°C to +125°C	–0.75		0.13	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.16		0.08	nA
			T_A = –40°C to +125°C	–1.5		0.25	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(IN)}$	Pull-down resistance on INx pins				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V	V_A = 0 V or 3.3 V, V_S = 0 V		11	14	µA
			V_A = 0 V or 3.3 V, V_S = 0 V			16	µA
			V_A = 0 V or 3.3 V, V_S = 0 V			17	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Switch turn-on time	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF		74	82	ns
		V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +85°C			89	ns
		V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +125°C			93	ns
t_{OFF}	Switch turn-off time	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF		56	75	ns
		V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +85°C			83	ns
		V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +125°C			85	ns
t_{BBM}	Break-before-make time delay (TMUX6123 only)	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = –40°C to +125°C	20	37		ns
Q_J	Charge injection	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF		0.14		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		-85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		–115		dB

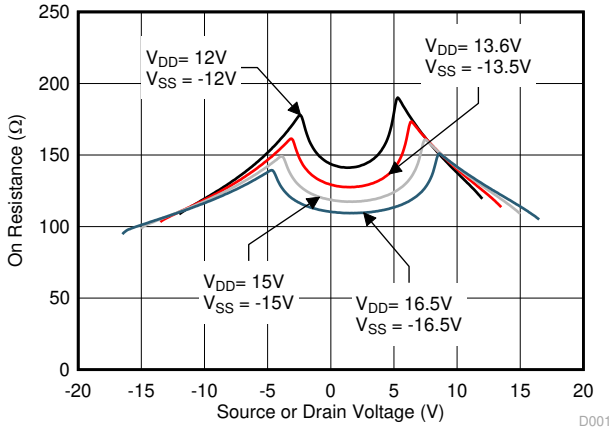
6.8 Switching Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		–15		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ, C_L = 5 pF, V_{PP}= 0.62 V, f= 1 MHz		–61		dB
BW	-3dB Bandwidth	R_L = 50 Ω, C_L = 5 pF		500		MHz
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.3		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz		2.2	2.8	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 6 V, f = 1 MHz		2.5	2.8	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		4.8	6.1	pF

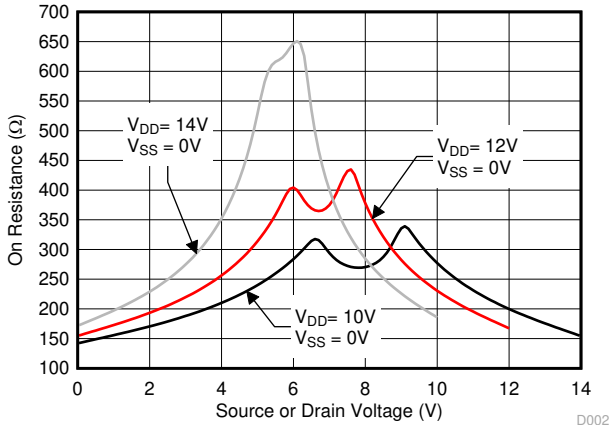
Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = – 15 V (unless otherwise noted)



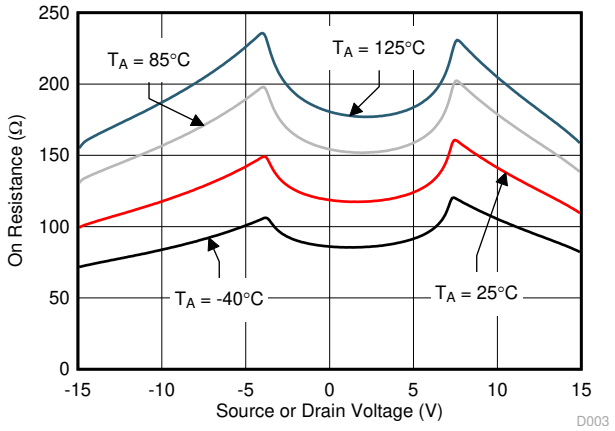
Dual Supply Operation (T_A = 25°C)

图 6-1. On-Resistance vs Source or Drain Voltage



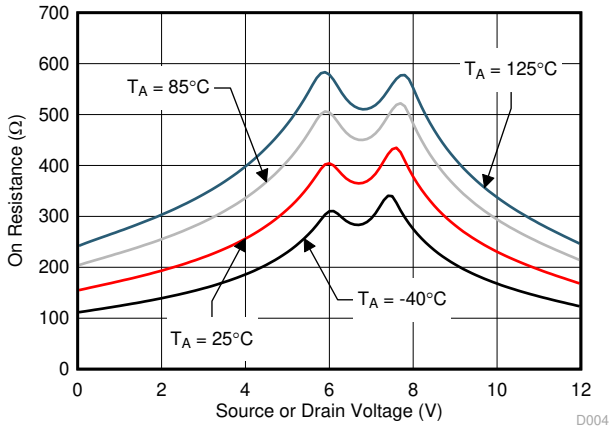
Dual Supply Operation (T_A = 25°C)

图 6-2. On-Resistance vs Source or Drain Voltage



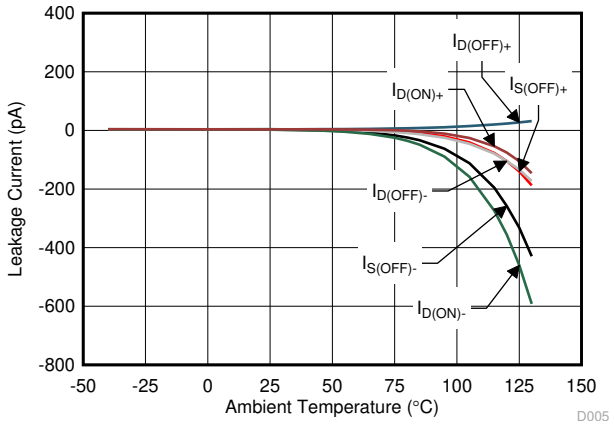
V_{DD} = 15 V, V_{SS} = – 15 V

图 6-3. On-Resistance vs Source or Drain Voltage



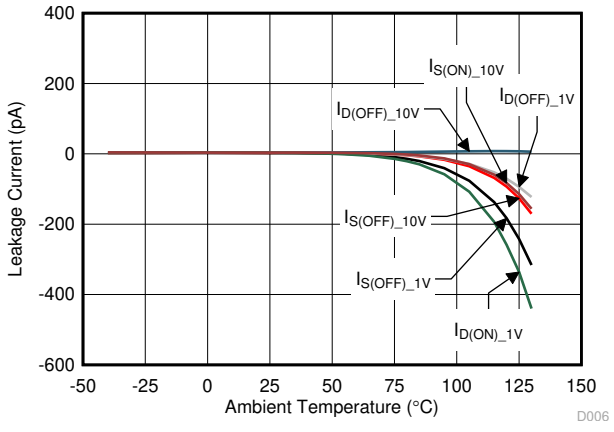
V_{DD} = 12 V, V_{SS} = 0 V

图 6-4. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = – 15 V

图 6-5. Leakage Current vs Temperature

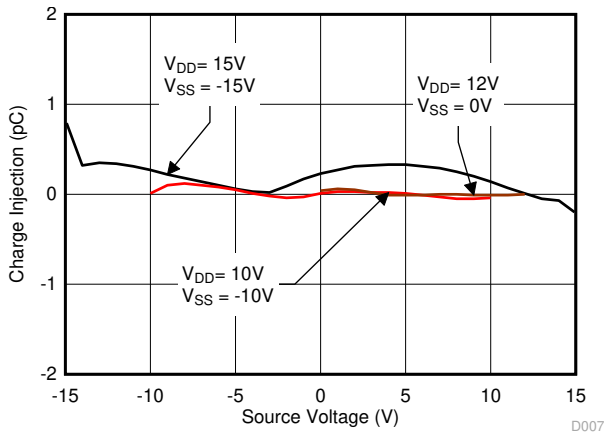


V_{DD} = 12 V, V_{SS} = 0 V

图 6-6. Leakage Current vs Temperature

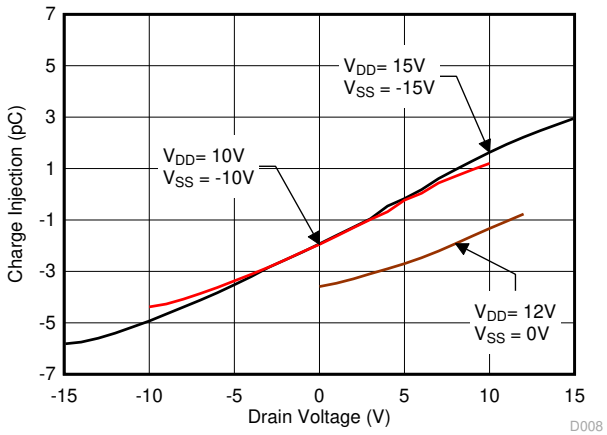
Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = – 15 V (unless otherwise noted)



T_A = 25°C

图 6-7. Charge Injection vs Source Voltage



T_A = 25°C

图 6-8. Charge Injection vs Drain Voltage

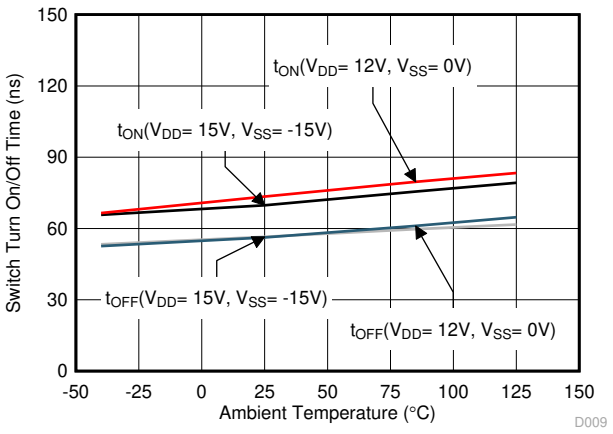
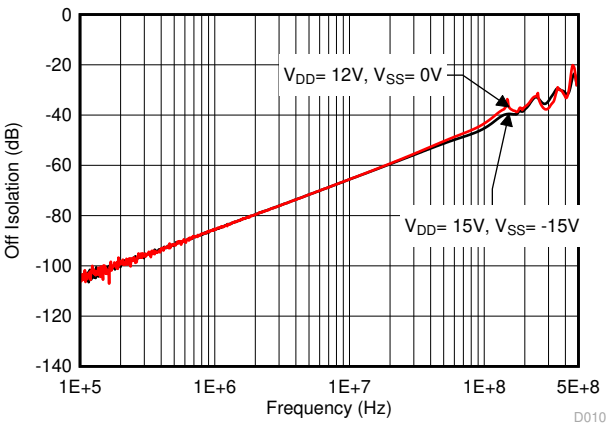
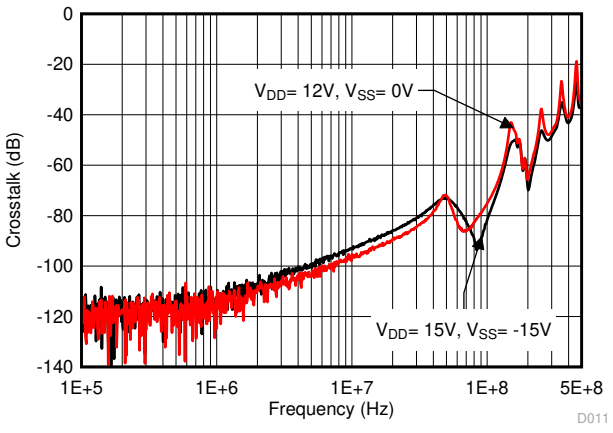


图 6-9. Turn-On and Turn-Off Times vs Temperature



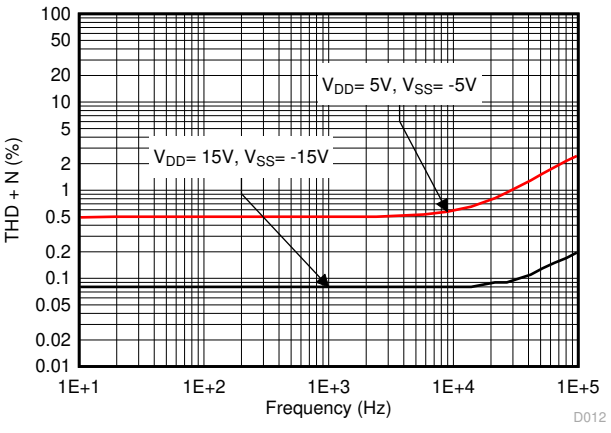
T_A = 25°C

图 6-10. Off Isolation vs Frequency



V_{DD} = 15 V, V_{SS} = – 15 V, T_A = 25°C

图 6-11. Crosstalk vs Frequency

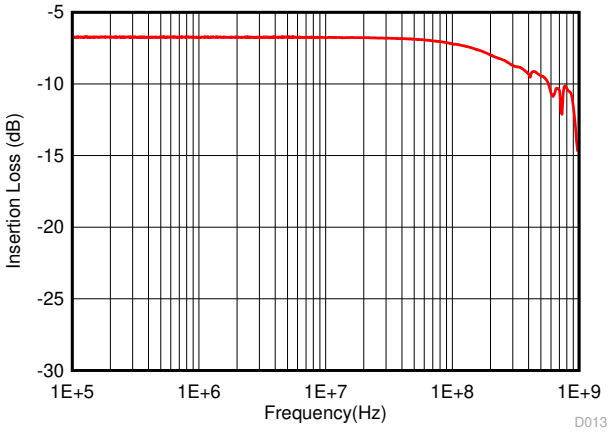


T_A = 25°C

图 6-12. THD+N vs Frequency

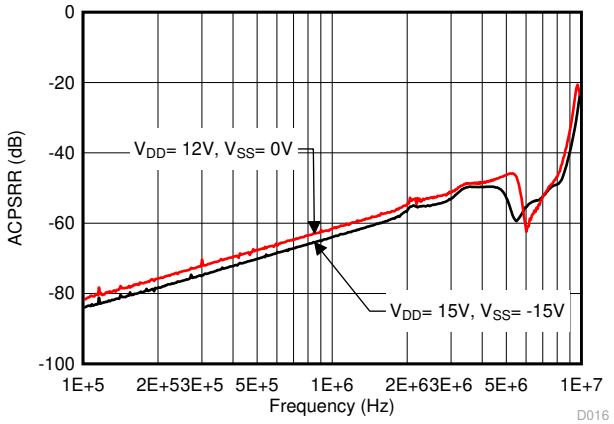
Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = – 15 V (unless otherwise noted)



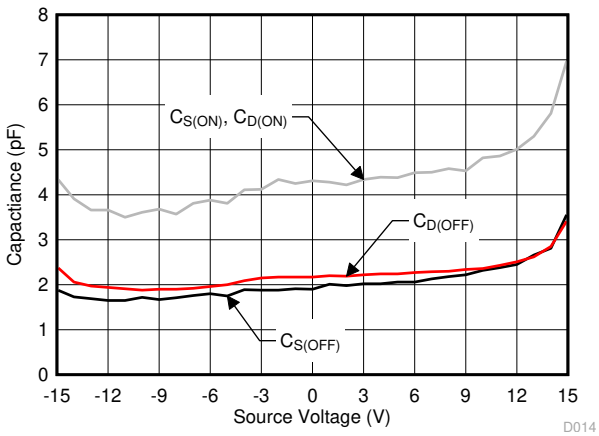
V_{DD} = 15 V, V_{SS} = – 15 V, T_A = 25°C

图 6-13. On Response vs Frequency



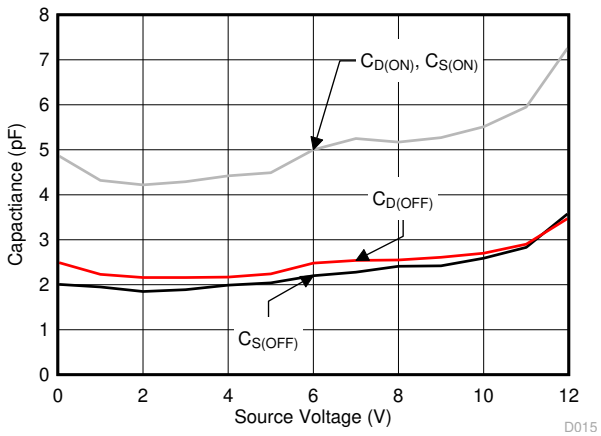
V_{DD} = 15 V, V_{SS} = – 15 V, V_{PP}= 0.62 V, T_A = 25°C

图 6-14. ACPSRR vs Frequency



V_{DD} = 15 V, V_{SS} = – 15 V, T_A = 25°C

图 6-15. Capacitance vs Source Voltage



V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C

图 6-16. Capacitance vs Source Voltage

7 Parameter Measurement Information

7.1 Truth Tables

表 7-1, 表 7-2, and 表 7-3 show the truth tables for the TMUX6121, TMUX6122, and TMUX6123, respectively.

表 7-1. TMUX6121 Truth Table

SELx	STATE
0	All Switch OFF
1	All Switch ON

表 7-2. TMUX6122 Truth Table

SELx	STATE
0	All Switch ON
1	All Switch OFF

表 7-3. TMUX6123 Truth Table

SELx	STATE
0	Switch 1 OFF Switch 2 ON
1	Switch 1 ON Switch 2 OFF

8 Detailed Description

8.1 Overview

The TMUX6121, TMUX6122, and TMUX6123 are 2-channel single-pole/ single-throw (SPDT) switches that support dual supplies (±5 V to ±16.5 V) or single supply (10 V to 16.5 V) operation. Each channel of the switch is turned on or turned off based on the state of its corresponding SELx pin. 节 8.2 provides a top-level block diagram of the switches.

8.1.1 On-Resistance

The on-resistance of the TMUX6121, TMUX6122, and TMUX6123 is the ohmic resistance across the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 8-1. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 方程式 1:

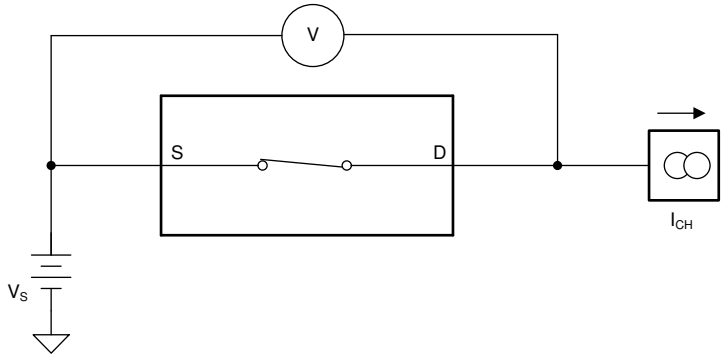


图 8-1. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

8.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 8-2.

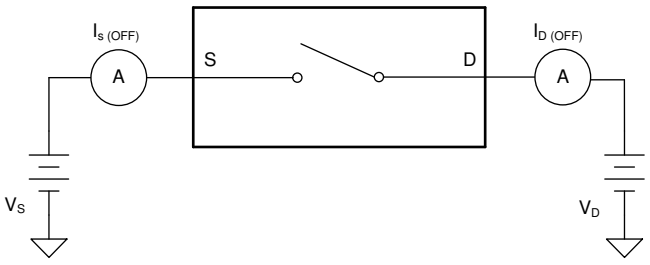


图 8-2. Off-Leakage Measurement Setup

8.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. 图 8-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

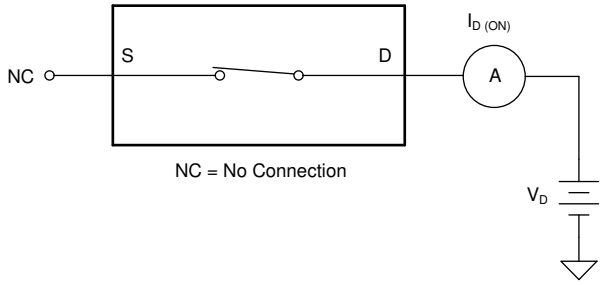


图 8-3. On-Leakage Measurement Setup

8.1.4 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the TMUX6121, TMUX6122, and TMUX6123 to rise to a 90% final value after the SELx signal has risen (for NO switches) or fallen (for NC switches) to a 50% final value. 图 8-4 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON}.

Turn off time is defined as the time taken by the output of the TMUX6121, TMUX6122, and TMUX6123 to fall to a 10% initial value after the SELx signal has fallen (for NO switches) or risen (for NC switches) to a 50% initial value. 图 8-4 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF}.

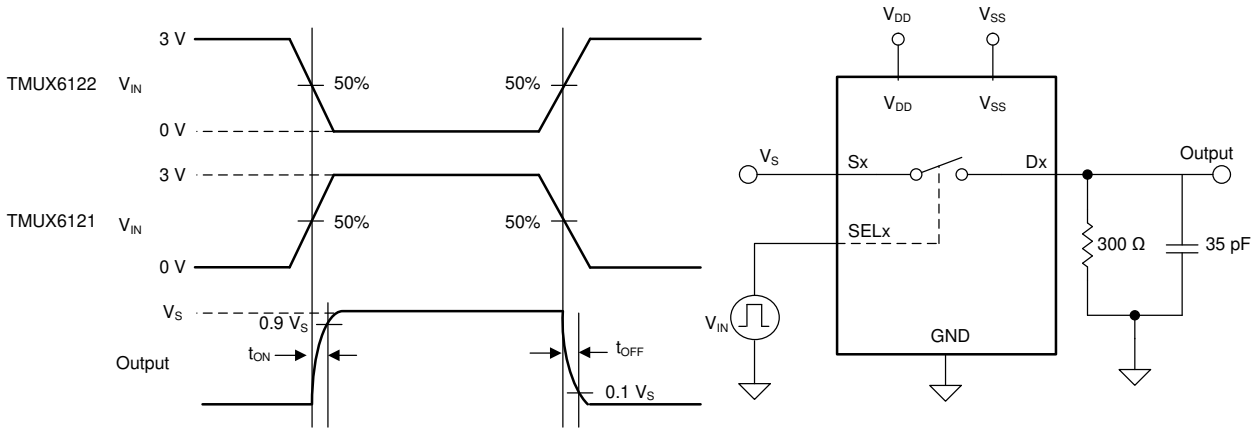


图 8-4. Transition-Time Measurement Setup

8.1.5 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX6123 switch. The TMUX6123's ON switches first break the connection before the OFF switches make connection. The time delay between the break and the make is known as break-before-make delay. 图 8-5 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

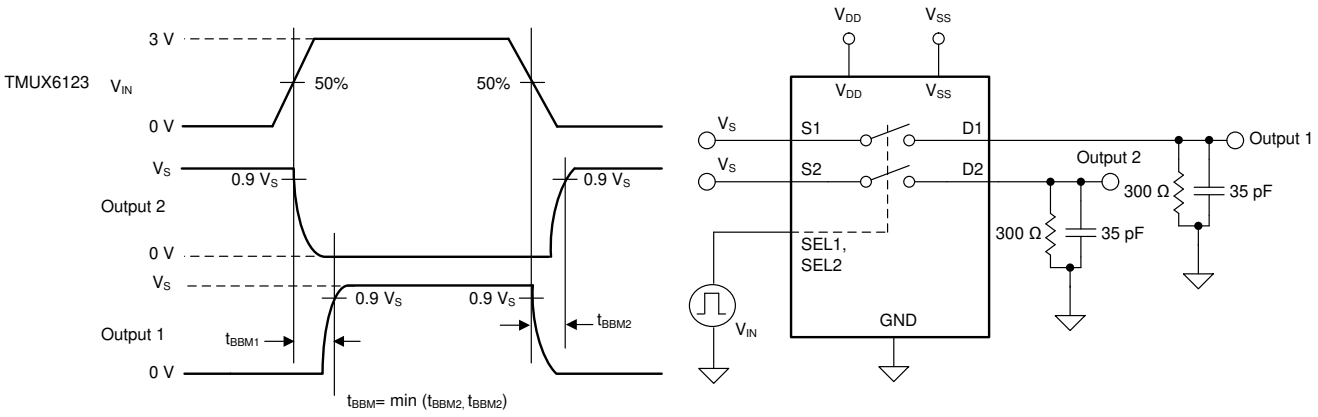


图 8-5. Break-Before-Make Delay Measurement Setup

8.1.6 Charge Injection

The TMUX6121, TMUX6122, and TMUX6123 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol QINJ. 图 8-6 shows the setup used to measure charge injection.

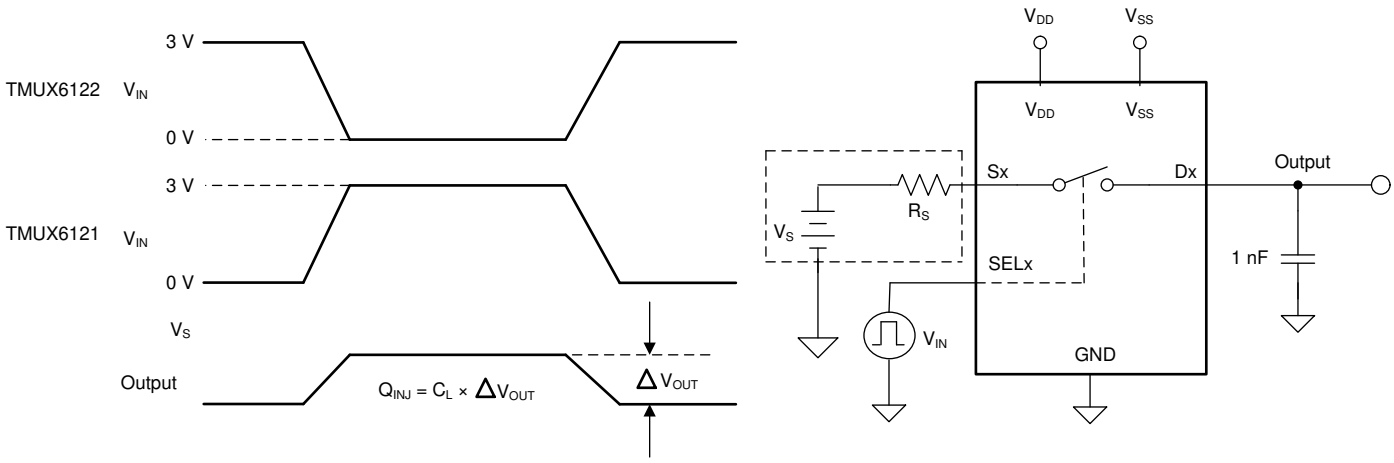


图 8-6. Charge-Injection Measurement Setup

8.1.7 Off Isolation

Off isolation is defined as the voltage at the drain pin (Dx) of the TMUX6121, TMUX6122, and TMUX6123 when a 1-V_{RMS} signal is applied to the source pin (Sx) of an OFF switch. 图 8-7 shows the setup used to measure off isolation. Use 方程式 2 to compute off isolation.

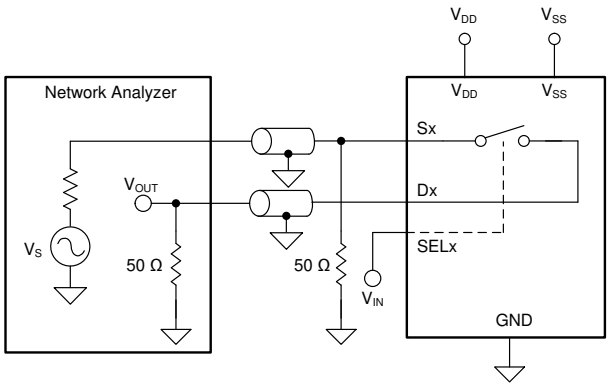


图 8-7. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{2}$$

8.1.8 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin (Sx) of an on-channel. 图 8-8 shows the setup used to measure, and 方程式 3 is the equation used to compute, channel-to-channel crosstalk.

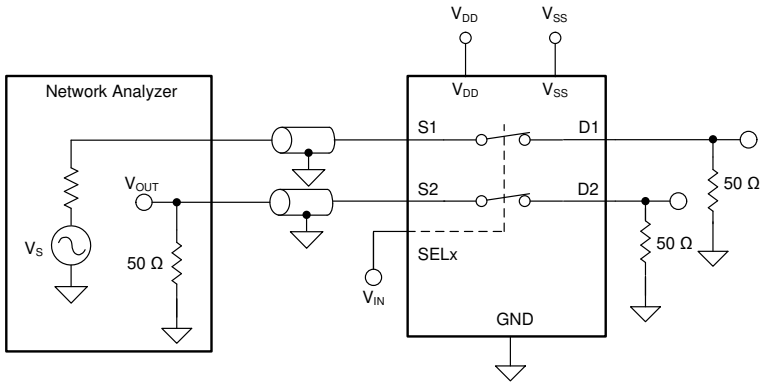


图 8-8. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{3}$$

8.1.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the TMUX6121, TMUX6122, and TMUX6123. 图 8-9 shows the setup used to measure bandwidth of the switch. Use 方程式 4 to compute the attenuation.

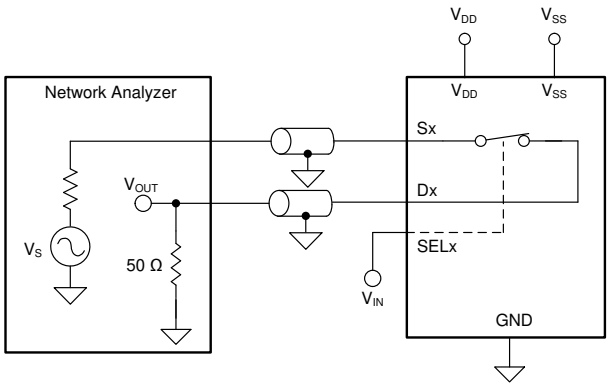


图 8-9. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \tag{4}$$

8.1.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6121, TMUX6122, and TMUX6123 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 图 8-10 shows the setup used to measure THD+N of the TMUX6121, TMUX6122, and TMUX6123.

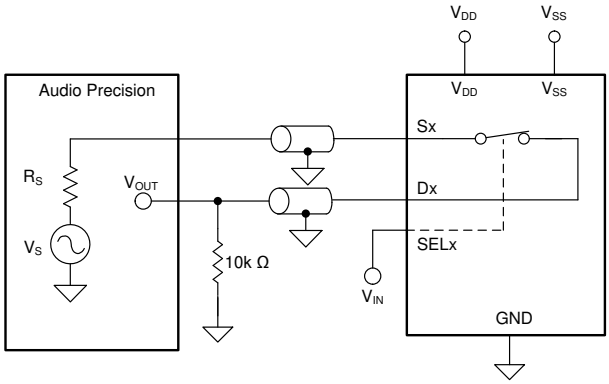


图 8-10. THD+N Measurement Setup

8.1.11 AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR. 图 8-11 shows the setup used to measure ACPSRR of the TMUX6121, TMUX6122, and TMUX6123.

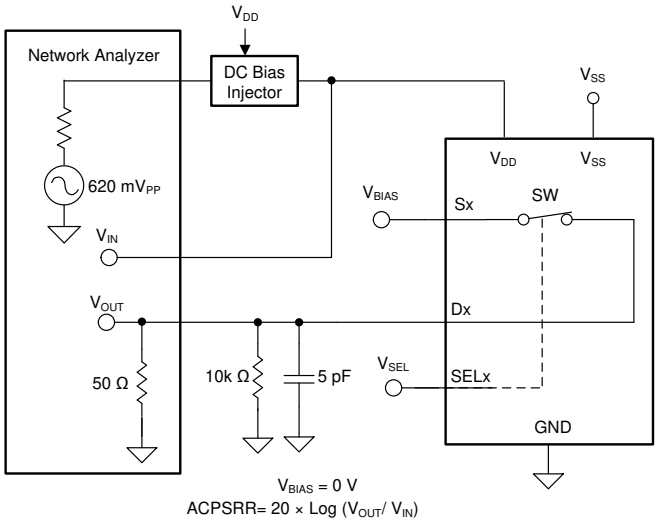
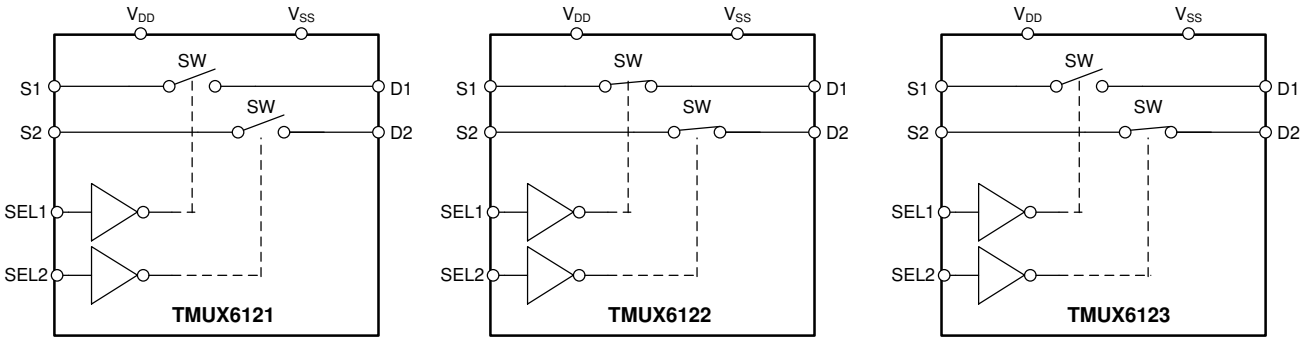


图 8-11. AC PSRR Measurement Setup

节 8.2 provides a top-level block diagram of the TMUX6121, TMUX6122, and TMUX6123. The devices are 2-channel, single-ended, analog switches. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



ALL SWITCHES SHOWN FOR A LOGIC 0 INPUT

8.3 Feature Description

8.3.1 Ultralow Leakage Current

The TMUX6121, TMUX6122, and TMUX6123 provide extremely low on- and off-leakage currents. The devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 图 8-12 shows typical leakage currents of the devices versus temperature.

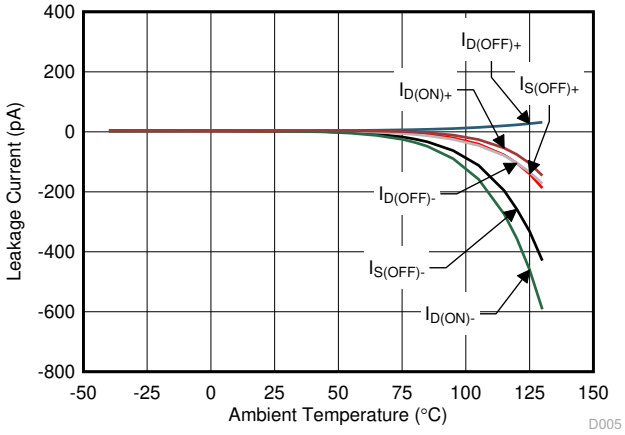


图 8-12. Leakage Current vs Temperature

8.3.2 Ultralow Charge Injection

The TMUX6121 is implemented with simple transmission gate topology, as shown in 图 8-13. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

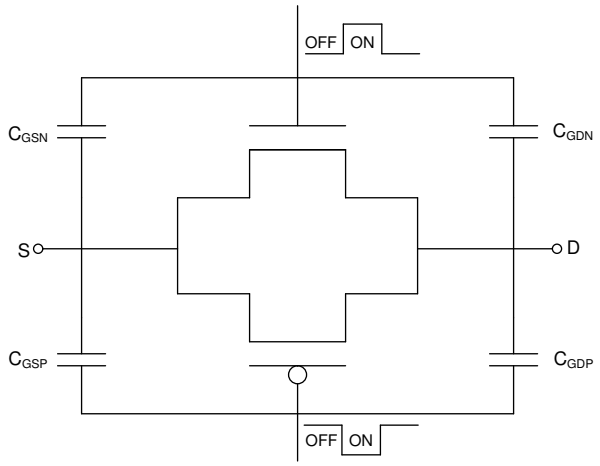


图 8-13. Transmission Gate Topology

The devices utilize special charge-injection cancellation circuitry that reduces the source (Sx)-to-drain (Dx) charge injection to as low as 0.51 pC at VS = 0 V, as shown in 图 8-14.

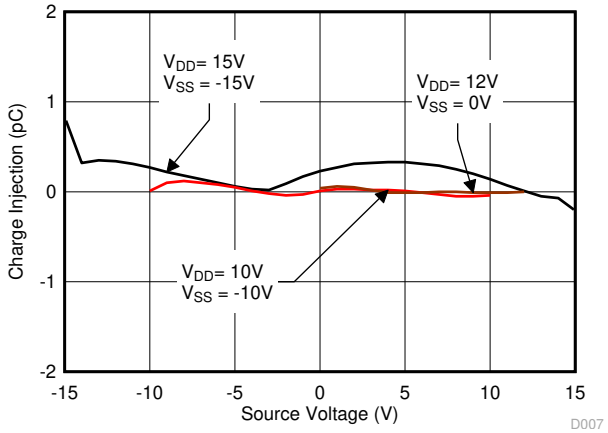


图 8-14. Source-to-Drain Charge Injection vs Source or Drain Voltage

8.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6121, TMUX6122, and TMUX6123 conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel of the switches has very similar characteristics in both directions. The input signal to the devices swings from V_{SS} to V_{DD} without any significant degradation in performance. The on resistance of these devices varies with input signal.

8.4 Device Functional Modes

Each channel of the TMUX6121, TMUX6122, and TMUX6123 is turned on or turned off based on the state of its corresponding SELx pin. The SELx pins are weakly pulled-down through an internal 6 MΩ resistor, allowing the switches to stay in a determined state when power is applies to the devices. The SELx pins can be connected to V_{DD}.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TMUX6121, TMUX6122, and TMUX6123 offer outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 33 (dual supply) or 16.5 V (single supply), and offer true rail-to-rail input and output. The on-capacitance of the TMUX6121, TMUX6122, and TMUX6123 is low. These features makes the TMUX6121, TMUX6122, and TMUX6123 a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

9.2 Typical Application

One useful application to take advantage of TMUX6121, TMUX6122, and TMUX6123's precision performance is the sample and hold circuit. A sample and hold circuit can be useful for an analog to digital converter (ADC) to sample a varying input voltage with improved reliability and stability. It can also be used to store the output samples from a single digital-to-analog converter (DAC) in a multi-output application. A simple sample and hold circuit can be realized using an analog switch like one of the TMUX6121, TMUX6122, and TMUX6123 analog switches.

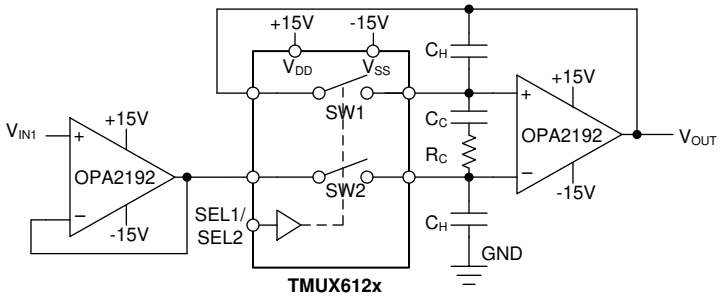


图 9-1. A Sample and Hold Circuit Realized Using the TMUX611x Analog Switch

9.2.1 Design Requirements

The purpose of this precision design is to implement an optimized 2-output sample and hold circuit using a 4-channel SPST switch. The sample and hold circuit needs to be capable of supporting high voltage output swing up to ± 15 V with minimized pedestal error and fast settling time. The overall system block diagram is shown in 图 9-1.

9.2.2 Detailed Design Procedure

The TMUX6121, TMUX6122, or TMUX6123 switch is used in conjunction with the voltage holding capacitors (C_H) to implement the sample and hold circuit. The basic operation is:

1. When the switch SW2 is closed, it samples the input voltage and charges the holding capacitors (C_H) to the input voltages values.
2. When the switch SW2 is open, the holding capacitors (C_H) holds its previous value, maintaining stable voltage at the amplifier output (V_{OUT})

Ideally, the switch delivers only the input signals to the holding capacitors. However, when the switch gets toggled, some amount of charge also gets transferred to the switch output in the form of charge injection, resulting slight sampling error. The TMUX6121, TMUX6122, and TMUX6123 switches have excellent charge injection performance of only 0.51 pC, making them ideal choices for this implementation to minimize sampling error. Due to switch and capacitor leakage current, the voltage on the hold capacitors droops with time. The TMUX6121, TMUX6122, and TMUX6123 minimize the droops due to its ultra-low leakage performance. At 25°C, the TMUX6111, TMUX6112, and TMUX6113 have extremely tiny leakage current at 0.5 pA typical and 20 pA maximum. The TMUX6121, TMUX6122, and TMUX6123 devices also support high voltage capability. The devices support up to ± 16.5 V dual supply operation, making it an ideal solution in this high voltage sample and hold application.

A second switch SW1 is also included to operate in parallel with SW2 to reduce pedestal error during switch toggling. Because both switches are driven at the same potential, they act as common-mode signal to the op-amp, thereby minimizing the charge injection effects caused by the switch toggling action. Compensation network consisting of R_C and CC is also added to further reduce the pedestal error, whiling reducing the hold-time glitch and improving the settling time of the circuit.

9.2.3 Application Curve

TMUX6121, TMUX6122, and TMUX6123 have excellent charge injection performance of only 0.51 pC (typical), making them ideal choices to minimize sampling error for the sample and hold application. 图 9-2 shows the plot for the charge injection versus source input voltage for TMUX6121, TMUX6122, and TMUX6123.

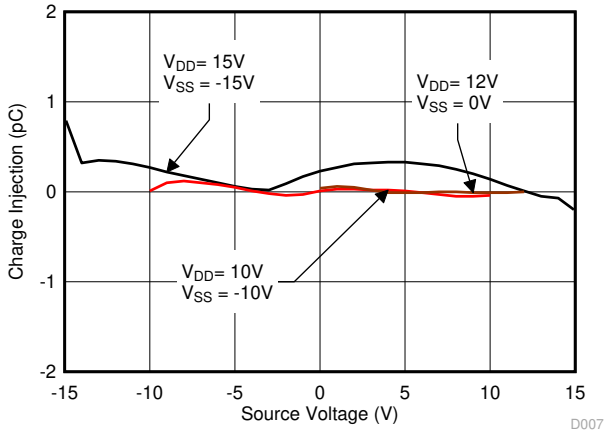


图 9-2. Charge Injection vs. Source Voltage for TMUX6121, TMUX6122 and TMUX6123

10 Power Supply Recommendations

The TMUX6121, TMUX6122, and TMUX6123 operate across a wide supply range of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS}= – 5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped. As a best practice, it is recommended to ramp V_{SS} first before V_{DD} in dual or asymmetrical supply applications.

The on-resistance of the TMUX6121, TMUX6122, and TMUX6123 varies with supply voltage, as shown in 图 10-1

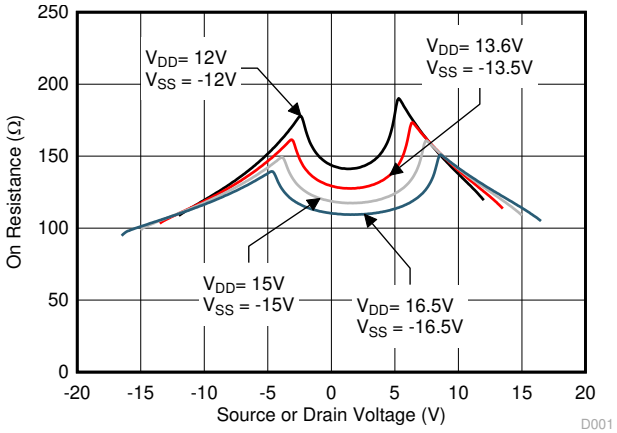


图 10-1. On-Resistance Variation With Supply and Input Voltage

11 Layout

11.1 Layout Guidelines

图 11-1 shows an example of a PCB layout with the TMUX6121, TMUX6122, and TMUX6123.

Some key considerations are:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

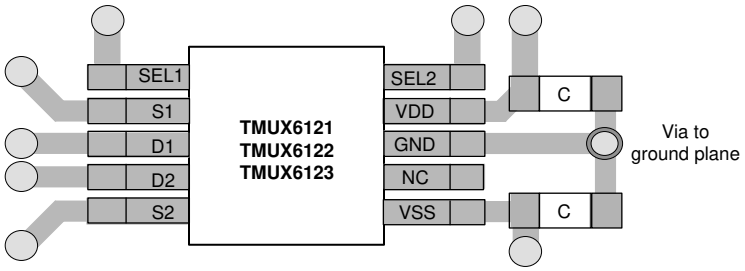


图 11-1. TMUX6121 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX6121DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1Q16
TMUX6121DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1Q16
TMUX6122DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1Q26
TMUX6122DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1Q26
TMUX6123DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1Q36
TMUX6123DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1Q36

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

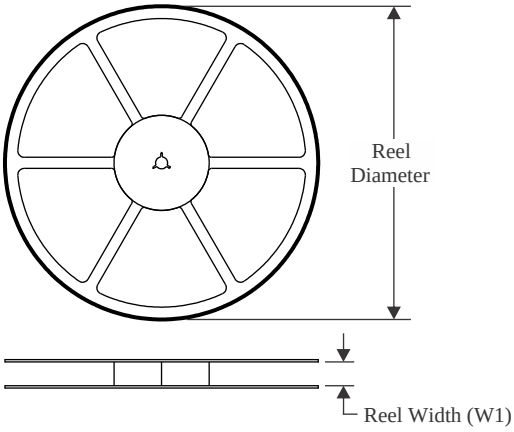
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

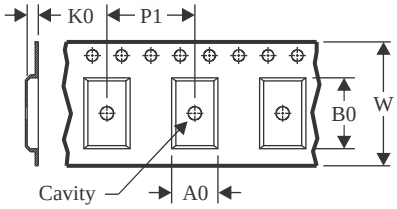
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

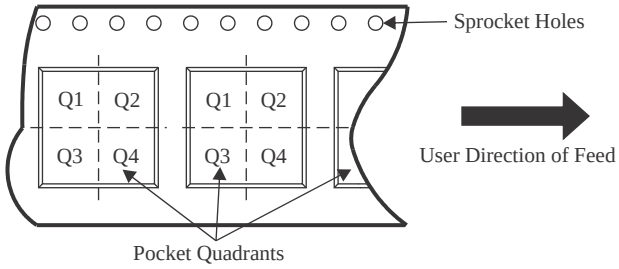


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

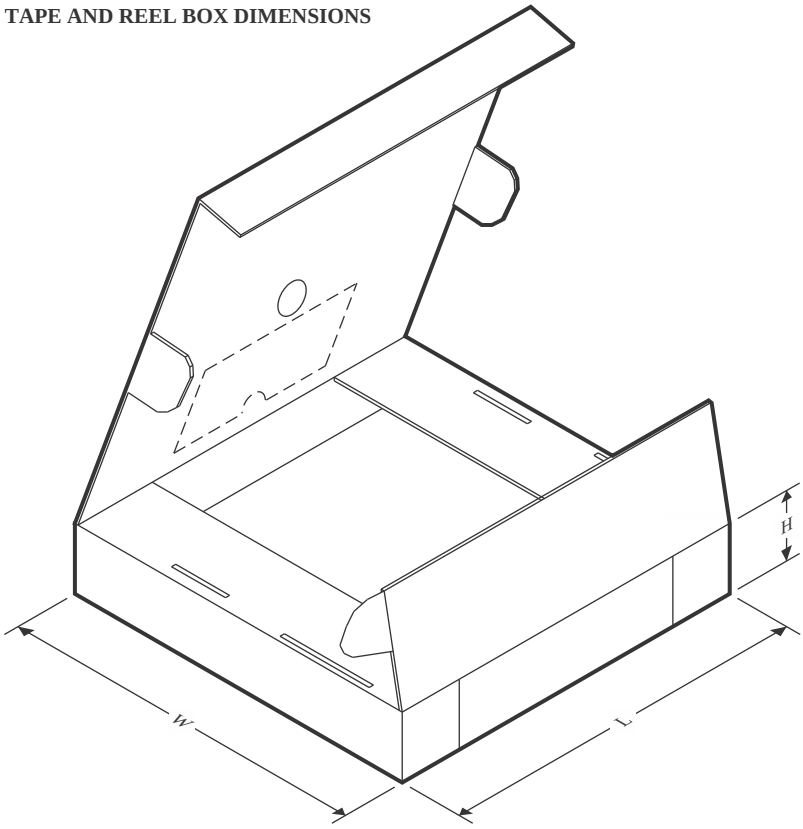
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6121DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX6122DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX6123DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX6123DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

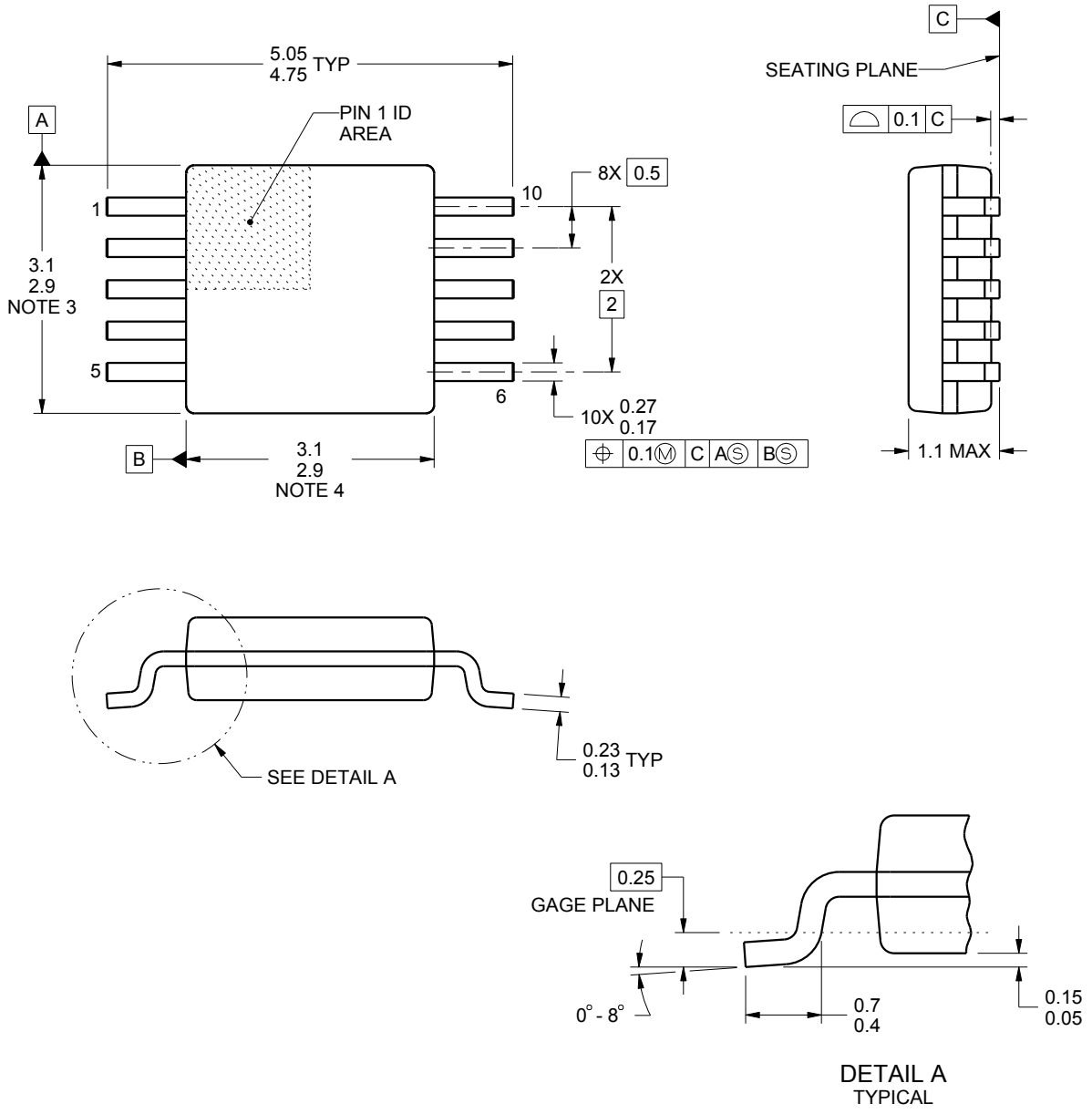
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6121DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX6122DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX6123DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX6123DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

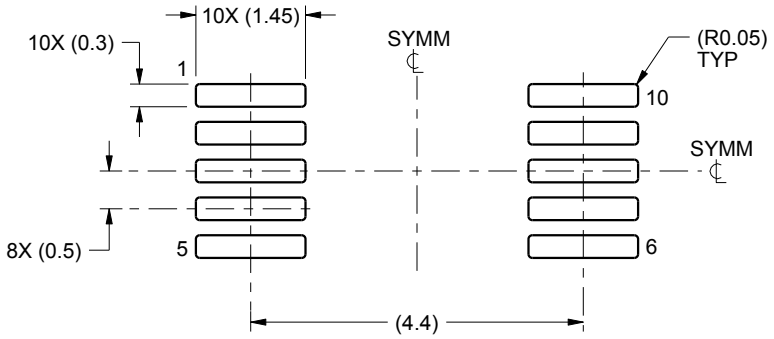
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

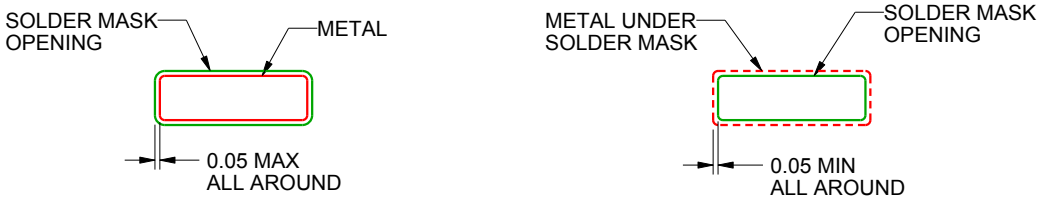


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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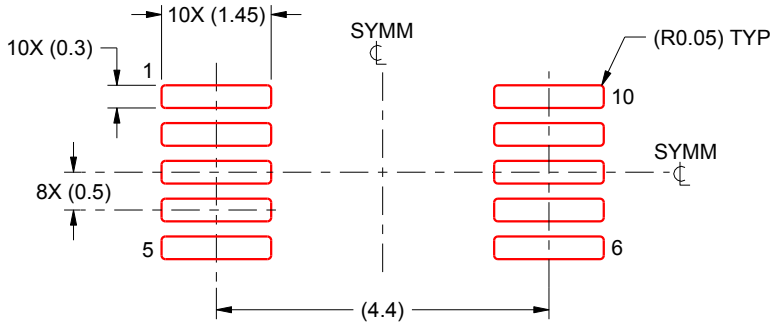
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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