

TPD12S016 具有 I²C 电平转换缓冲器、12 通道 ESD 保护和限流负载开关的 HDMI 配套芯片

1 特性

- 符合 HDMI 兼容性测试，无需任何外部组件
- IEC 61000-4-2 静电放电 (ESD) 保护
 - ±8kV 接触放电
- 支持高清多媒体接口 (HDMI) 1.4 数据速率
- 与 D 类和 C 类引脚映射相匹配
- 采用超低差分电容匹配 (0.05pF) 为四个差分对提供 8 通道 ESD 保护
- HDMI 5V_OUT 引脚上具有 55mA 电流限制的片上负载开关
- 自动方向感应 I²C 电平转换器，采用单触发电路驱动长 HDMI 电缆 (750pF 负载)
- HDMI 连接器侧端口具有反向驱动保护
- 遵照 HDMI 规范集成上拉和下拉电阻
- 采用节约空间的 24 引脚 RKT 封装和 24 引脚 TSSOP 封装

2 应用范围

- 手机
- 电子书
- 便携式媒体播放器
- 机顶盒

3 说明

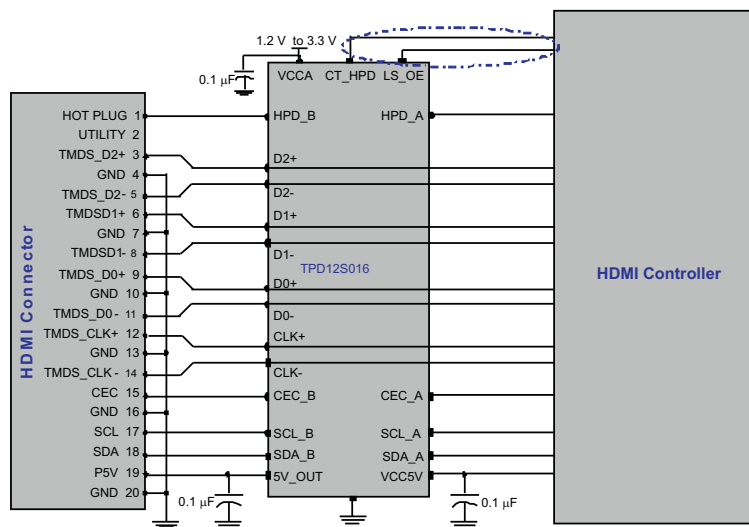
TPD12S016 是一款单芯片高清多媒体接口 (HDMI) 器件，具有自动方向感应 I²C 电压电平转换缓冲器、负载开关和集成式低电容高速静电放电 (ESD) 瞬态电压抑制 (TVS) 保护二极管。通过 55mA 限流 5V 输出 (5V_OUT) 为 HDMI 电力线供电。5V_OUT 和热插拔检测 (HPD) 电路的控制与 LS_OE 控制信号无关，其通过 CT_HPDP 引脚进行控制，使得在启用 HDMI 链路前即可激活检测方案 (5V_OUT 和 HPD)。SDA、SCL 和 CEC 线路上拉到 A 侧的 V_{CCA}。在 B 侧，CEC_B 引脚上拉到内部 3.3V 电源轨，SCL_B 和 SDA_B 均上拉到 5V 电源轨 (5V_OUT)。SCL 和 SDA 引脚满足 I²C 规范，可驱动高达 750pF 电容负载，超出了 HDMI 1.4 规范。HPD_B 端口配有毛刺脉冲滤波器，可在插入 HDMI 连接器时避免由插座跳起引起的错误检测。TPD12S016 的 5V_OUT 引脚具有反向电流阻断功能。系统断电时，SCL_B、SDA_B 和 CEC_B 引脚也具有反向电流阻断功能。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPD12S016	QFN (24)	4.00mm x 2.00mm
	TSSOP (24)	7.80mm x 6.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (December 2014) to Revision F	Page
• Added test condition frequency to capacitance	6
• Added test condition frequency to capacitance	7
• 已添加 社区资源	22

Changes from Revision D (August 2013) to Revision E	Page
• 已添加 处理额定值表，特性 描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1

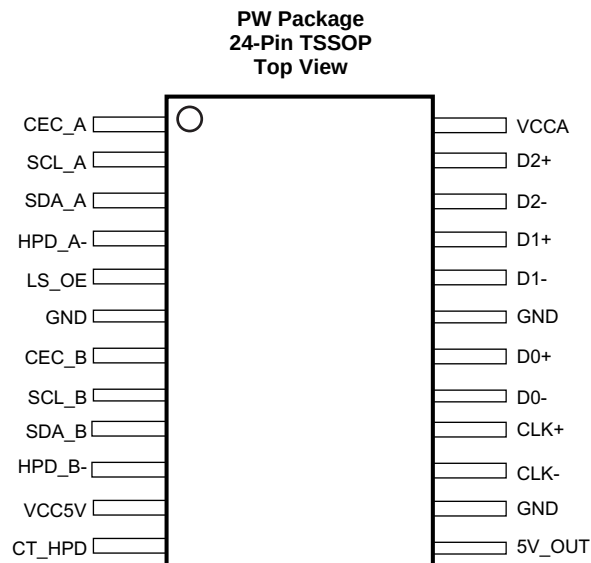
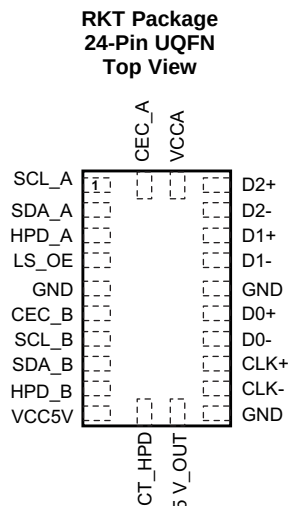
Changes from Original (January 2013) to Revision A	Page
• Added Eye Diagram Using EVM Without TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps	18
• Added Eye Diagram Using EVM with TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps	18

Changes from Revision A (February 2013) to Revision B	Page
• Added PW and RKT packages values for IO capacitance	6
• Added LOAD SWITCH $I_{LEAKAGE_REVERSE}$ vs V_{5V_OUT} graph.	11
• Updated Circuit Schematic Diagram.	13

Changes from Revision B (February 2013) to Revision C	Page
• Updated table formatting.	6

Changes from Revision C (August 2013) to Revision D	Page
• Updated power savings options table	16

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	RKT	PW		
D-, D+	16, 17, 19 to 22	17, 18, 20 to 23	IO	HDMI TMDS data. Connect to HDMI controller and HDMI connector directly
CLK+, CLK-	14, 15	15, 16	IO	HDMI TMDS clock. Connect to HDMI controller and HDMI connector directly
HPD_A	3	4	O	Hot plug detect output referenced to V _{CCA} . Connect to HDMI controller hot plug detect input pin
HPD_B	9	10	I	Hot plug detect input. Connect directly to HDMI connector hot plug detect pin
CEC_A	24	1	IO	HDMI controller side CEC signal pin referenced to V _{CCA} . Connect to HDMI controller
CEC_B	6	7	IO	HDMI connector side CEC signal pin referenced to internal 3.3-V supply. Connect to HDMI connector CEC pin
SCL_A	1	2	IO	HDMI controller side SCL signal pin referenced to V _{CCA} . Connect to HDMI controller
SCL_B	7	8	IO	HDMI connector side SCL signal pin referenced to 5V_OUT supply. Connect to HDMI connector SCL pin
SDA_A	2	3	IO	HDMI controller side SDA signal pin referenced to V _{CCA} . Connect to HDMI controller
SDA_B	8	9	IO	HDMI connector side SDA signal pin referenced to 5V_OUT supply. Connect to HDMI connector SDA pin
LS_OE	4	5	I	Disables the Level shifters when OE = L. The OE pin is referenced to V _{CCA}
CT_HPDP	11	12	I	Disables the load switch and HPD_B when CT_HPDP = L. The CT_HPDP is referenced to V _{CCA}
V _{CC5V}	10	11	PWR	Internal 5-V supply (input to the load switch)
V _{CCA}	23	24	PWR	Internal PCB low voltage supply (same as the HDMI controller chip supply)
5V_OUT	12	13	O	External 5-V supply (output of the load switch)
GND	5, 13, 18	6, 14, 19	GND	Connect to system ground plane

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CCA}	Supply voltage	−0.3	4.0	V
V _{CC5V}	Supply voltage	−0.3	6.0	V
V _I	Input voltage ⁽¹⁾	SCL_A, SDA_A, CEC_A	−0.3	4.0
		SCL_B, SDA_B, CEC_B	−0.3	6.0
		CT_HPDP, LS_OE	−0.3	4.0
		D, CLK	−0.3	6.0
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽¹⁾	SCL_A, SDA_A, CEC_A, CT_HPDP, LS_OE	−0.3	4.0
		SCL_B, SDA_B, CEC_B	−0.3	6.0
V _O	Voltage applied to any output in the high or low state ⁽¹⁾⁽²⁾	SCL_A, SDA_A, CEC_A, CT_HPDP, LS_OE	−0.3	V _{CCA} + 0.5
		SCL_B, SDA_B, CEC_B	−0.3	5V_OUT + 0.5
I _{IK}	Input clamp current	V _I < 0	−50	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
	Continuous current through 5V_OUT, or GND		±100	mA
T _{stg}	Storage temperature	−65	150	°C

(1) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	LS_OE, CT_HPDP, SCL_A, SDA_A, CEC_A, HPD_A, V _{CCA}	±2000
			Dx, CLKx, SCL_B, SDA_B, CEC_B, HPD_B, 5V_OUT	±15000
		Charged-device model (CDM), per JEDEC specification JESD22-C101		±1000
		IEC 61000-4-2 Contact Discharge	Dx, CLKx, SCL_B, SDA_B, CEC_B, HPD_B, 5V_OUT	±8000

6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V _{CCA}	Supply voltage			1.1		3.6	V
V _{CC5V}	Supply voltage			4.5		5.5	V
V _{IH}	High-level input voltage	SCL_A, SDA_A	V _{CCA} = 1.1 V to 3.6 V	0.7 × V _{CCA}		V _{CCA}	V
		CEC_A	V _{CCA} = 1.1 V to 3.6 V	0.7 × V _{CCA}		V _{CCA}	V
		CT_HPDP, LS_OE	V _{CCA} = 1.1 V to 3.6 V	1.0		V _{CCA}	V
		SCL_B, SDA_B	5V_OUT = 5.0 V	0.7 × 5V_OUT		5V_OUT	V
		CEC_B	5V_OUT = 5.0 V	0.7 × V _{3P3} ⁽¹⁾		V _{3P3}	
		HPD_B	5V_OUT = 5.0 V	2.0		5V_OUT	
V _{IL}	Low-level input voltage	SCL_A, SDA_A	V _{CCA} = 1.1 V to 3.6 V	–0.5		0.082 × V _{CCA}	V
		CEC_A	V _{CCA} = 1.1 V to 3.6 V	–0.5		0.082 × V _{CCA}	V
		CT_HPDP, LS_OE	V _{CCA} = 1.1 V to 3.6 V	–0.5		0.4	V
		SCL_B, SDA_B	5V_OUT = 5.0 V	–0.5		0.3 × 5V_OUT	V
		CEC_B	5V_OUT = 5.0 V	–0.5		0.3 × V _{3P3}	V
		HPD_B	5V_OUT = 5.0 V	0		0.8	V
V _{ILC}	(contention) Low-level input voltage	SCL_A, SDA_A, CEC_A	V _{CCA} = 1.1 V to 3.6 V	–0.5		0.065 × V _{CCA}	V
V _{OL} - V _{ILC}	Delta between V _{OL} and V _{ILC}	SCL_A, SDA_A, CEC_A	V _{CCA} = 1.1 V to 3.6 V		0.1 × V _{CCA}		mV
T _A	Operating free-air temperature			–40		85	°C

(1) The V_{3P3} is an internal 3.3V power supply node. The V_{3P3} is generated from the 5V supply pin through the on-chip LDO.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD12S016		UNIT
		RKT (UQFN)	PW (TSSOP)	
		24 PINS	24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	77.9	88.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	24.0	26.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	29.3	43.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.5	1.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	29.3	43.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
HIGH SPEED ESD LINES: D _x , CLK _x								
I _{IO}	Current through ESD clamp ports		V _{CCA} = 3.3 V, V _{CC5V} = 5.0 V, V _{IO} = 3.3 V	D, CLK		0.01	0.5	μA
V _{DL}	Diode forward voltage		I _D = 8 mA	Lower clamp diode		0.8	1.0	V
R _{DYN}	Dynamic resistance		I = 1 A	D, CLK		1		Ω
C _{IO}	IO capacitance	PW Package	V _{CC} = 5 V, V _{IO} = 2.5 V f = 1 MHz	D, CLK		1.0		pF
		RKT Package			1.2			
ΔC _{IO_TMS}	Differential capacitance for the Dx+, Dx– lines		V _{CC} = 5 V, V _{IO} = 2.5 V f = 1 MHz	D, CLK		0.05		pF
V _{BR}	Break-down voltage		I _{IO} = 1 mA		6.5		9	V
LOAD SWITCH V _{CC5V} , 5V_OUT								
I _{CC5V}	Supply current at V _{CC5V}		V _{CC5V} = 5 V, 5V_OUT =Open, LS_OE = GND, CT_HPD = GND			1	45	μA
	Supply current at V _{CC5V}		V _{CC5V} = 5 V, 5V_OUT =Open, LS_OE = GND, CT_HPD = 3.3 V			4	50	μA
I _{SC}	Short circuit current at 5V_OUT		V _{CC5V} = 5 V, 5V_OUT = GND		100	150	200	mA
V _{DROP}	5V_OUT output voltage drop		V _{CC5V} = 5 V, I _{5V_OUT} = 55 mA			35	50	mV
T _{ON}	Turn on time, V _{CC5V} to 5V_OUT		C _{LOAD} = 0.1 μF, R _{LOAD} = 500 Ω			77		μs
T _{OFF}	Turn off time, V _{CC5V} to 5V_OUT		C _{LOAD} = 0.1 μF, R _{LOAD} = 500 Ω			7.0		μs
T _{SHUT}	Thermal Shutdown		Shutdown threshold, TRIP ⁽¹⁾			140		°C
			HYST ⁽²⁾			12		
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A AND x_B PORTS)								
V _{OHA}			I _{OH} = –20 μA	V _I = V _{IH}	V _{CCA} = 1.1 V to 3.6 V	V _{CCA} × 0.80		V
V _{OLA}			I _{OL} = 20 μA	V _I = V _{IL}	V _{CCA} = 1.1 V to 3.6 V	V _{CCA} × 0.17		V
V _{OHB}			I _{OH} = –20 μA	V _I = V _{IH}		5VOUT × 0.90		V
V _{OLB}			I _{OL} = 3 mA	V _I = V _{IL}				0.4 V
ΔV _T	Hysteresis at the SDx_A (V _{T+} – V _{T–})		V _{CCA} = 1.1 V to 3.6 V			40		mV
ΔV _T	Hysteresis at the SDx_B (V _{T+} – V _{T–})		V _{CCA} = 1.1 V to 3.6 V			400		mV
R _{PU}	(Internal pullup)		SCL_A, SDA_A	Pull-up connected to V _{CCA} rail		10		kΩ
			SCL_B, SDA_B	Pull-up connected to 5-V rail		1.75		
I _{PULLUPAC}	Transient boosted pullup current (rise-time accelerator)		SCL_B, SDA_B	Pull-up connected to 5-V rail		15		mA
I _{off}	A port	V _{CCA} = 0 V, V _I or V _O = 0 to 3.6 V			V _{CCA} = 0 V	±5		μA
	B port	5VOUT = 0 V, V _I or V _O = 0 to 5.5 V			V _{CCA} = 0 V to 3.6 V	±5		
I _{OZ}	B port	V _O = V _{CCO} or GND			V _{CCA} = 1.1 V to 3.6 V	±5		μA
	A port	V _I = V _{CCI} or GND			V _{CCA} = 1.1 V to 3.6 V	±5		

(1) The TPD12S016 turns off after the device temperature reaches the TRIP temperature.

(2) After the thermal shut-down circuit turns off the load switch, the switch turns on again after the device junction temperature cools down to a temperature equals to or less than TRIP-HYST.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
VOLTAGE LEVEL SHIFTER – CEC LINE (x_A AND x_B PORTS)								
V_OHA		I_OH = −20 μA	V_I = V_IH	V_CCA = 1.1 V to 3.6 V	V_CCA × 0.80			V
V_OLA		I_OL = 20 μA	V_I = V_IL	V_CCA = 1.1 V to 3.6 V	V_CCA × 0.17			V
V_OHB		I_OH = −20 μA	V_I = V_IH		V_3P3 × 0.80			V
V_OLB		I_OL = 3 mA	V_I = V_IL				0.4	V
ΔV_T	Hysteresis at the Sxx_A (V_T+ − V_T−)	V_CCA = 1.1 V to 3.6 V			40			mV
ΔV_T	Hysteresis at the Sxx_B (V_T+ − V_T−)	V_CCA = 1.1 V to 3.6 V			300			mV
R_PU	(Internal pullup)	CEC_A	Pull-up connected to V_CCA rail		10			kΩ
		CEC_B	Pull-up connected to 3.3 V rail		22 26 30			
I_off	A port	V_CCA = 0 V, V_I or V_O = 0 to 3.6 V		V_CCA = 0 V	±5		μA	
	B port	5VOUT = 0 V, V_I or V_O = 0 to 5.5 V		V_CCA = 0 V to 3.6 V	±1.8			
I_OZ	B port	V_O = V_CCO or GND		V_CCA = 1.1 V to 3.6 V	±5		μA	
	A port	V_I = V_CCI or GND		V_CCA = 1.1 V to 3.6 V	±5			
VOLTAGE LEVEL SHIFTER – HPD LINE (x_A AND x_B PORTS)								
V_OHA		I_OH = −3 mA	V_I = V_IH	V_CCA = 1.1 V to 3.6 V	V_CCA × 0.07			V
V_OLA		I_OL = 3 mA	V_I = V_IL	V_CCA = 1.1 V to 3.6 V	0.4			V
ΔV_T	Hysteresis (V_T+ − V_T−)	V_CCA = 1.1 V to 3.6 V			400			mV
R_PD	(Internal pulldown resistor)	HPD_B	Pull-down connected to GND		11			kΩ
I_off	A port	V_O = V_CCO or GND	V_CCA = 0 V		±5			μA
I_OZ	A port	V_I = V_CCO or GND	V_CCA = 3.6 V		±5			μA
LS_OE, CT_CP_HPD								
I_I		V_I = V_CCA or GND	V_CCA = 1.1 V to 3.6 V		±12			μA
I/O CAPACITANCES								
C_I	Control inputs	V_I = 1.89 V or GND	V_CCA = 1.1 to 3.6 V; f = 1 MHz		7.1			pF
C_IO	A port	V_O = 1.89 V or GND	V_CCA = 1.1 to 3.6 V; f = 1 MHz		8.3			pF
	B port	V_O = 5.0 V or GND	V_5VOUT = 5.0 V; f = 1 MHz		15			pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
C _L	Bus load capacitance (B side)					750	pF	
	Bus load capacitance (A side)					15		
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A And x_B PORTS) V _{CCA} = 1.2 V								
t _{PHL}	Propagation delay	A to B	SCL/SDA channels enabled		310		ns	
		B to A			420			
t _{PLH}	Propagation delay	A to B			510		ns	
		B to A			427			
t _{FALL}	A Port fall time	A-Port			334		ns	
	B Port fall time	B-Port			225			
t _{RISE}	A Port rise time	A-Port			315		ns	
	B Port rise time	B-Port			415			
F _(MAX)	Maximum switching frequency				400			kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V _{CCA} = 1.2 V								
t _{PHL}	Propagation delay	A to B	CEC channel enabled		385		ns	
		B to A			526			
t _{PLH}	Propagation delay	A to B			13.8		μs	
		B to A			16.6		ns	
t _{FALL}	A Port fall time	A-Port			334		ns	
	B Port fall time	B-Port			170			
t _{RISE}	A Port rise time	A-Port			315		ns	
	B Port rise time	B-Port			28		μs	
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V _{CCA} = 1.2 V								
t _{PHL}	Propagation delay	B to A		HPD channel enabled		14.4		μs
t _{PLH}	Propagation delay	B to A			9.2		μs	
t _{FALL}	A Port fall time	A-Port			2.1		ns	
t _{RISE}	A Port rise time	A-Port			2.1		ns	
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A AND x_B PORTS) V _{CCA} = 1.5 V								
t _{PHL}	Propagation delay	A to B	SCL/SDA channels enabled		310		ns	
		B to A			420		ns	
t _{PLH}	Propagation delay	A to B			410		ns	
		B to A			425		ns	
t _{FALL}	A Port fall time	A-Port			250		ns	
	B Port fall time	B-Port			225		ns	
t _{RISE}	A Port rise time	A-Port			315		ns	
	B Port fall time	B-Port			415		ns	
F _(MAX)	Maximum switching frequency				400			kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V _{CCA} = 1.5 V								
t _{PHL}	Propagation delay	A to B	CEC channel enabled		380		ns	
		B to A			420			
t _{PLH}	Propagation delay	A to B			13.8		μs	
		B to A			16.6		ns	
t _{FALL}	A Port fall time	A-Port			250		ns	
	B Port fall time	B-Port			170			
t _{RISE}	A Port rise time	A-Port			315		ns	
	B Port rise time	B-Port			28		μs	

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V _{CCA} = 1.5 V								
t _{PHL}	Propagation delay	B to A	HPD channel enabled		14.4		μs	
t _{PLH}	Propagation delay	B to A			9.2		μs	
t _{FALL}	A Port fall time	A-Port			1.8		ns	
t _{RISE}	A Port rise time	A-Port			1.8		ns	
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A AND x_B PORTS) V _{CCA} = 1.8 V								
t _{PHL}	Propagation delay	A to B	SCL/SDA channels enabled		300		ns	
		B to A			350		ns	
t _{PLH}	Propagation delay	A to B			400		ns	
		B to A			420		ns	
t _{FALL}	A Port fall time	A-Port			210		ns	
	B Port fall time	B-Port			225		ns	
t _{RISE}	A Port rise time	A-Port			315		ns	
	B Port fall time	B-Port			415		ns	
F _(MAX)	Maximum switching frequency				400			kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V _{CCA} = 1.8 V								
t _{PHL}	Propagation delay	A to B	CEC channel enabled		375		ns	
		B to A			366			
t _{PLH}	Propagation delay	A to B			13.8		μs	
		B to A			16.6		ns	
t _{FALL}	A Port fall time	A-Port			210		ns	
	B Port fall time	B-Port			170			
t _{RISE}	A Port rise time	A-Port			315		ns	
	B Port rise time	B-Port			28		μs	
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V _{CCA} = 1.8 V								
t _{PHL}	Propagation delay	B to A	HPD channels enabled		14.2		μs	
t _{PLH}	Propagation delay	B to A			9.2		μs	
t _{FALL}	A Port fall time	A-Port			1.5		ns	
t _{RISE}	A Port rise time	A-Port			1.5		ns	
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A And x_B PORTS) V _{CCA} = 2.5 V								
t _{PHL}	Propagation delay	A to B	SCL/SDA channels enabled		300		ns	
		B to A			400			
t _{PLH}	Propagation delay	A to B			290		ns	
		B to A			420			
t _{FALL}	A Port fall time	A-Port			170		kHz	
	B Port fall time	B-Port			225			
t _{RISE}	A Port rise time	A-Port			315		ns	
	B Port fall time	B-Port			415			
F _(MAX)	Maximum switching frequency				400			kHz

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V _{CCA} = 2.5 V							
t _{PHL}	Propagation delay	A to B	CEC channel enabled	375		ns	
		B to A		305			
t _{PLH}	Propagation delay	A to B		13.8		μs	
		B to A		16.6		ns	
t _{FALL}	A Port fall time	A-Port		170		ns	
	B Port fall time	B-Port		170			
t _{RISE}	A Port rise time	A-Port		315		ns	
	B Port rise time	B-Port		28		μs	
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V _{CCA} = 2.5 V							
t _{PHL}	Propagation delay	B to A	HPD channel enabled	14.2		μs	
t _{PLH}	Propagation delay	B to A		9.2		μs	
t _{FALL}	A Port fall time	A-Port		1.2		ns	
t _{RISE}	A Port rise time	A-Port		1.2		ns	
VOLTAGE LEVEL SHIFTER – SCL, SDA LINES (x_A And x_B PORTS) V _{CCA} = 3.3 V							
t _{PHL}	Propagation delay	A to B	SCL/SDA channels enabled	300		ns	
		B to A		400			
t _{PLH}	Propagation delay	A to B		260		ns	
		B to A		415			
t _{FALL}	A Port fall time	A-Port		160		ns	
	B Port fall time	B-Port		225			
t _{RISE}	A Port rise time	A-Port		305		ns	
	B Port fall time	B-Port		415			
F _(MAX)	Maximum switching frequency				400		kHz
VOLTAGE LEVEL SHIFTER – CEC LINES (x_A AND x_B PORTS) V _{CCA} = 3.3V							
t _{PHL}	Propagation delay	A to B	CEC channel enabled	375		ns	
		B to A		305			
t _{PLH}	Propagation delay	A to B		13.8		μs	
		B to A		16.6		ns	
t _{FALL}	A Port fall time	A-Port		160		ns	
	B Port fall time	B-Port		170			
t _{RISE}	A Port rise time	A-Port		305		ns	
	B Port rise time	B-Port		28		μs	
VOLTAGE LEVEL SHIFTER – HPD LINES (x_A AND x_B PORTS) V _{CCA} = 3.3 V							
t _{PHL}	Propagation delay	B to A	HPD channel enabled	14.2		μs	
t _{PLH}	Propagation delay	B to A		9.2		μs	
t _{FALL}	A Port fall time	A-Port		1.1		ns	
t _{RISE}	A Port rise time	A-Port		1.1		ns	

6.7 Typical Characteristics

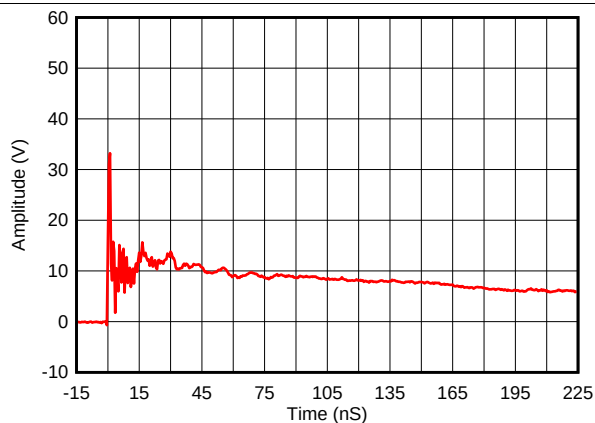


Figure 1. IEC Clamping Waveform +8kv Contact

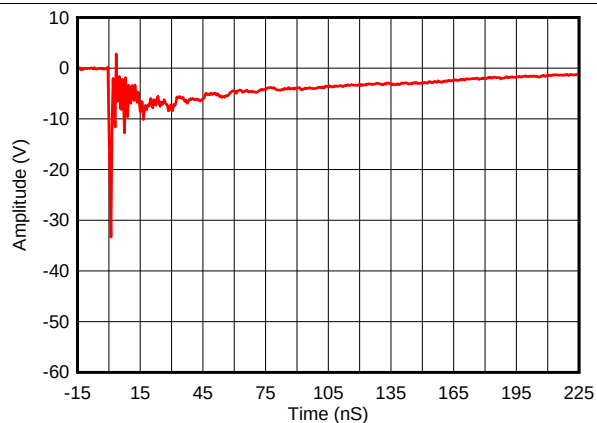


Figure 2. IEC Clamping Waveform -8kv Contact

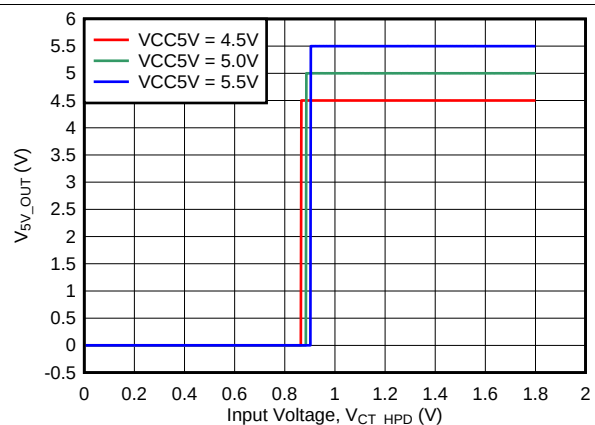


Figure 3. CT_HPDP V_{IH}

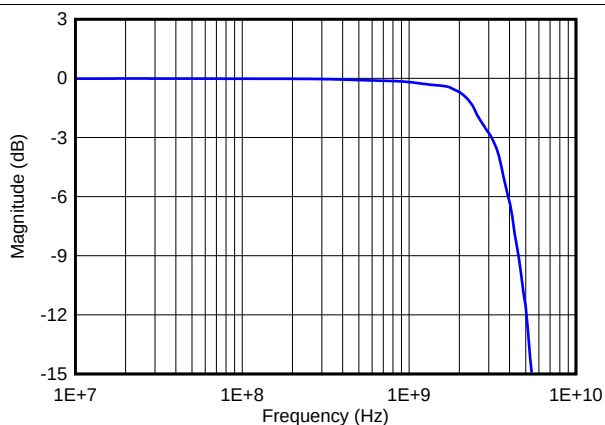


Figure 4. Insertion Loss, Data Line to GND

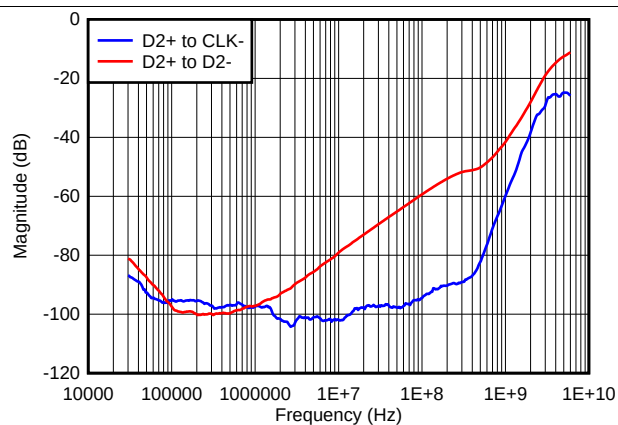
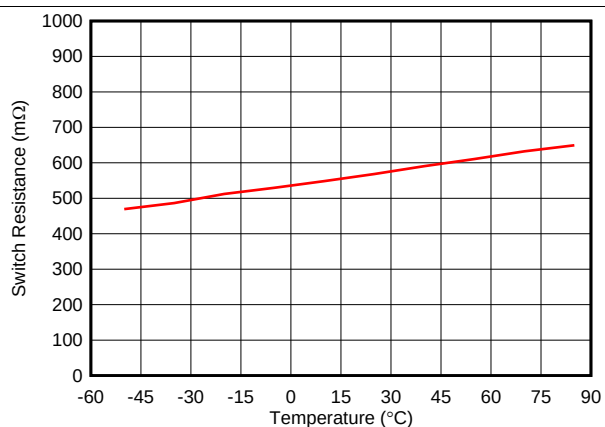
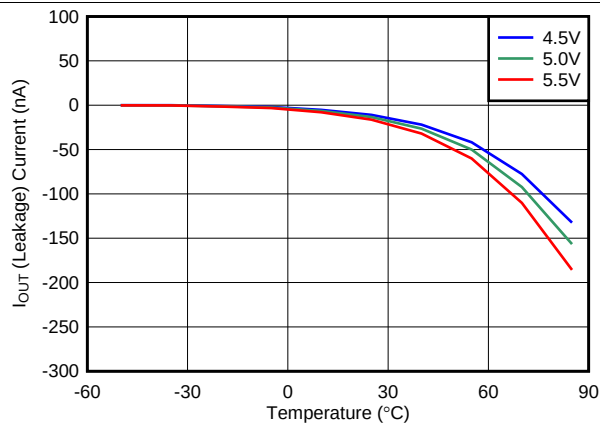
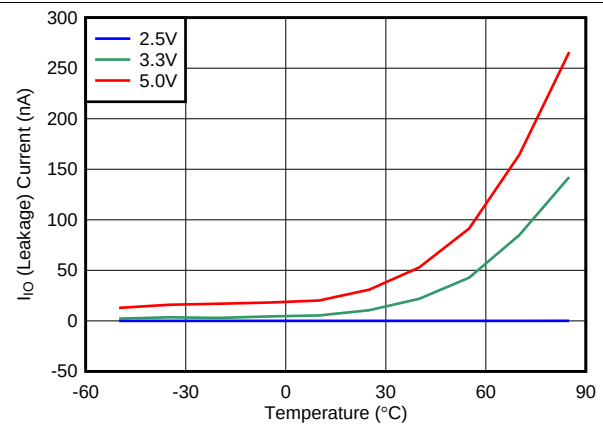
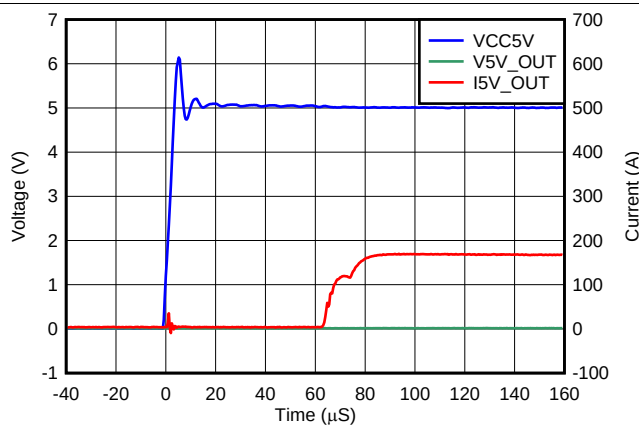
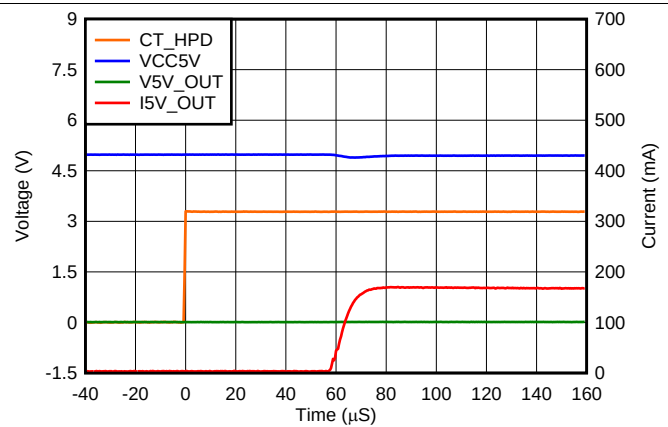
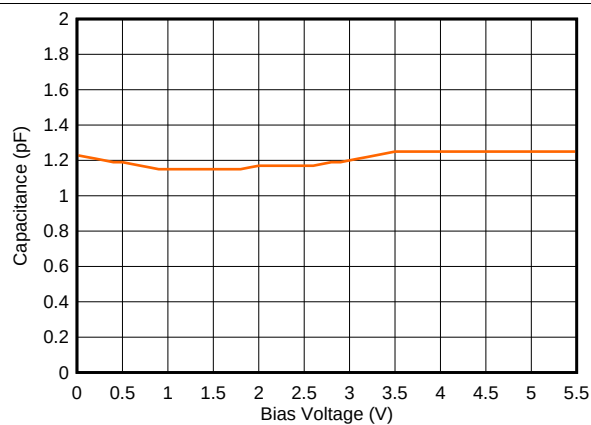
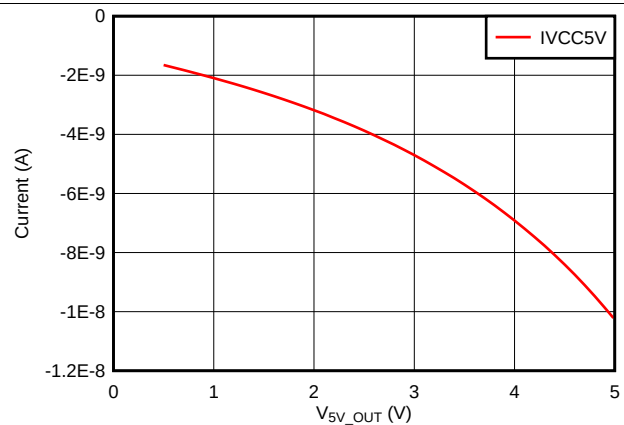


Figure 5. Channel-to-Channel Crosstalk



**Figure 6. Switch Resistance vs Temperature,
 I_{switch} at Approximately 55 mA**

Typical Characteristics (continued)


Figure 7. Load Switch $I_{leakage}$ vs Temperature

Figure 8. TMD5 Line I_O vs Temperature

Figure 9. Short-Circuit Response Time (Powered-Up to Short)

Figure 10. Current Limit Response Time (Switch Enabled to Short)

Figure 11. Capacitance vs Bias Voltage

Figure 12. Load Switch $I_{LEAKAGE_REVERSE}$ vs V_{5V_OUT}

7 Detailed Description

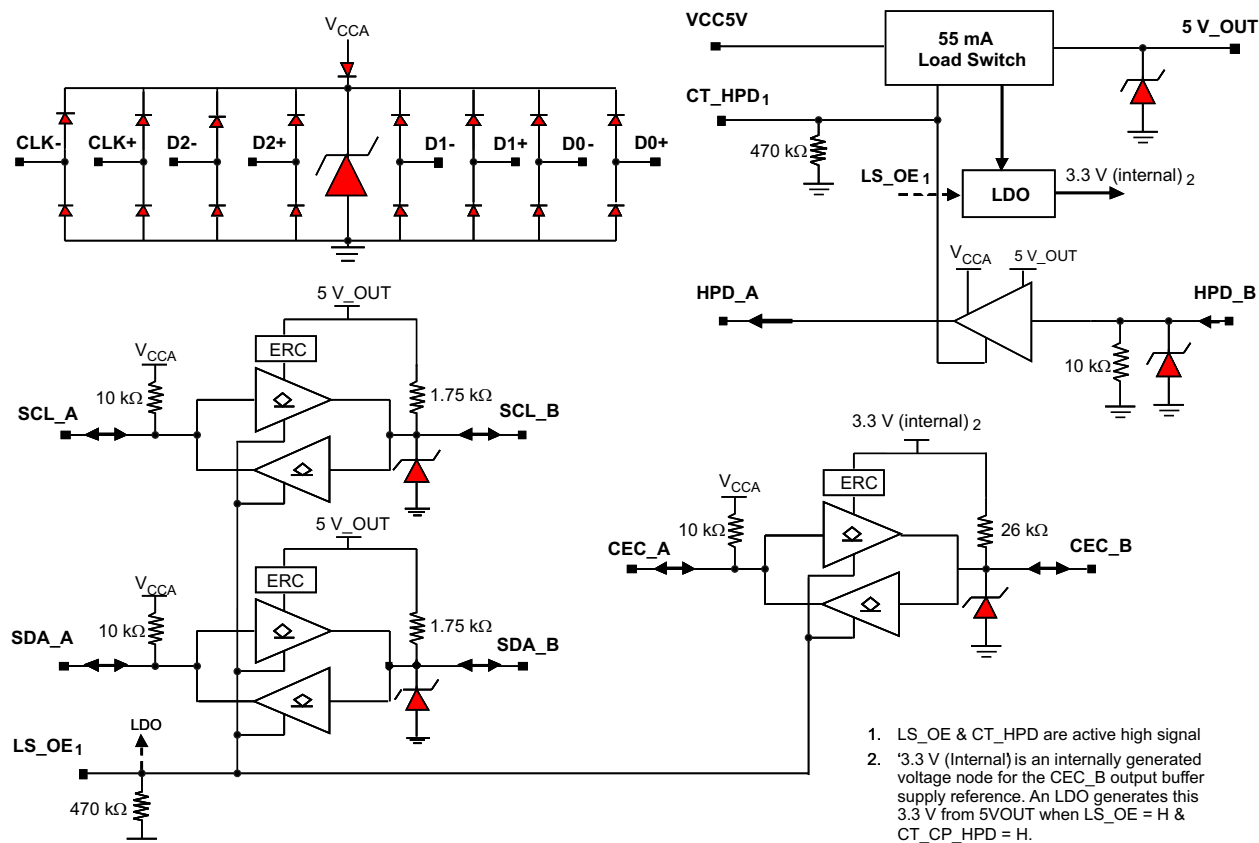
7.1 Overview

The TPD12S016 is a single-chip HDMI interface device with auto-direction sensing I²C voltage level shifting buffers, a load switch, and integrated high-speed ESD protection clamps. The device pin mapping matches the HDMI connector with four differential pairs and control lines. This device offers eight low-capacitance ESD clamps, allowing HDMI 1.4 data rates. The integrated ESD circuits provides matching between each differential signal pair, which allows an advantage over discrete ESD solutions where variations between ESD protection clamps degrade the differential signal quality. The TPD12S016 provides a current limited 5-V output (5V_OUT) for sourcing the HDMI power line. The current limited 5-V output supplies up to 55 mA to the HDMI receiver. The control of 5V_OUT and the hot plug detect (HPD) circuitry is independent of the LS_OE control signal, and is controlled by the CT_HPDP pin. This independent CT_HPDP control enables the detection scheme (5V_OUT and HPD) to be active before enabling the HDMI link. An internal 3.3 V node powers the CEC pin eliminating the need for a 3.3 V supply on board.

The TPD12S016 integrates all the external termination resistors at the HPD, CEC, SCL, and SDA lines. There are three non-inverting bidirectional voltage level translation (VLT) circuits for the SDA, SCL, and CEC lines. Each have a common power rail (V_{CCA}) on the A side from 1.1 V to 3.6V. On the B side, the SCL_B and SDA_B each have an internal 1.75 kΩ pull up connected to the 5-V rail (5V_OUT). The SCL and SDA pins meet the I²C specification and drive up to 750-pF capacitive loads exceeding the HDMI 1.4 specifications. The CEC_B pin has an internal 27-kΩ pull up resistor to the internal 3.3-V supply rail. The HPD_B port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion.

The TPD12S016 offers a reverse current blocking feature at the 5V_OUT pin. In the fault conditions, such as when two HDMI transmitters connect to the same HDMI cable, the TPD12S016 ensures that the system is safe from powering up through an external HDMI transmitter. The SCL_B, SDA_B, CEC_B pins also feature reverse-current blocking when the system is powered off.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Conforms to HDMI Compliance Tests Without any External Components

The TPD12S016 has integrated pullup or pulldown resistors on the DDC, CEC, and HPD lines that conform to the HDMI 7.13 and 7.15 Compliance Tests without the designer needing to use any external components to TPD12S016.

7.3.2 IEC 61000-4-2 ESD Protection

In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S016 provides the desired system-level ESD protection, such as the IEC 61000-4-2 Level 4 ESD protection of ± 8 -kV Contact rating by absorbing the energy associated with the ESD strike.

7.3.3 Supports HDMI 1.4 Data Rate

The high-speed TMDS pins of the TPD12S016 add only 1.0-pF (for PW package) or 1.2-pF (for RKT package) of capacitance to the TMDS lines. An Insertion Loss -3 dB point that is greater than 3 GHz provides enough bandwidth to pass HDMI 1.4 TMDS data rates.

7.3.4 Matches Class D and Class C Pin Mapping

The PW and RKT packages offer seamless layout routing options to eliminate the routing glitch for the differential signal pairs. The pin mapping follows the same order as the HDMI connector pin mapping.

7.3.5 8-Channel ESD Lines for Four Differential Pairs with Ultra-low Differential Capacitance Matching (0.05 pF)

Excellent intra-pair capacitance matching of 0.05 pF provides ultra low intra-pair skew, which allows an advantage over discrete ESD solutions where variations between ESD protection clamps can degrade the differential signal quality.

7.3.6 On-Chip Load Switch With 55-mA Current Limit Feature at the HDMI 5V_OUT Pin

The TPD12S016 provides a current limited 5-V output (5V_OUT) for sourcing the HDMI power line. The current limited 5-V output supplies up to 55 mA to the HDMI receiver. The control of 5V_OUT and the HPD circuitry is independent of the LS_OE control signal, and is controlled by the CT_HPDP pin. This independent CT_HPDP control enables the detection scheme (5V_OUT and HPD) to be active before enabling the HDMI link.

7.3.7 Auto-direction Sensing I²C Level Shifter With One-Shot Circuit to Drive a Long HDMI Cable (750-pF Load)

The TPD12S016 contains three bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, V_{CCA} side DDC-bus and the 5-V DDC-bus or 3.3-V CEC line. The HDMI cable side of the DDC lines incorporates rise-time accelerators to support a high capacitive load on the HDMI cable side. The rise time accelerators boost the cable side DDC signal independent of which side of the bus is releasing the signal.

7.3.8 Back-Drive Protection on HDMI Connector Side Ports

The TPD12S016 offers a reverse current blocking feature at the 5V_OUT pin. In fault conditions, such as when two HDMI transmitters connect to the same HDMI cable, the TPD12S016 ensures that the system is safe from powering up through an external HDMI transmitter. The SCL_B, SDA_B, CEC_B pins also feature reverse-current blocking when the system is powered off.

7.3.9 Integrated Pullup and Pulldown Resistors per HDMI Specification

The system is designed to work properly according to the HDMI 1.4 specification with no external pullup resistors on the DDC, CEC, and HPD lines.

Feature Description (continued)

7.3.10 Space Saving 24-Pin RKT Package and 24-TSSOP Package

When compared to discrete ESD solutions, the fully integrated port protection offered by TPD12S016 reduces the overall area required to fully protect an HDMI transmitter port.

7.3.11 DDC/CEC LEVEL SHIFT Circuit Operation

The TPD12S016 enables DDC translation from V_{CCA} (system side) voltage levels to 5-V (HDMI cable side) voltage levels without degradation of system performance. The TPD12S016 contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, V_{CCA} side DDC-bus and the 5-V DDC-bus. The port B I/Os are over-voltage tolerant to 5.5 V, even when the device is unpowered. After power-up and with the LS_OE and CT_HPDP pins HIGH, a LOW level on port A (below approximately $V_{ILC} = 0.08 \times V_{CCA}$ V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to V_{OLB} V. When port A rises above approximately $0.10 \times V_{CCA}$ V, the port B pulldown driver is turned off and the internal pullup resistor pulls the pin HIGH. When port B falls first and goes below 0.3×5 VOUT V, a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately $V_{OLA} = 0.16 \times V_{CCA}$ V. The port B pulldown is not enabled unless the port A voltage goes below V_{ILC} . If the port A low voltage goes below V_{ILC} , the port B pulldown driver is enabled until port A rises above $(V_{ILC} + \Delta V_{T-HYSTA})$, then port B, if not externally driven LOW, will continue to rise being pulled up by the internal pullup resistor.

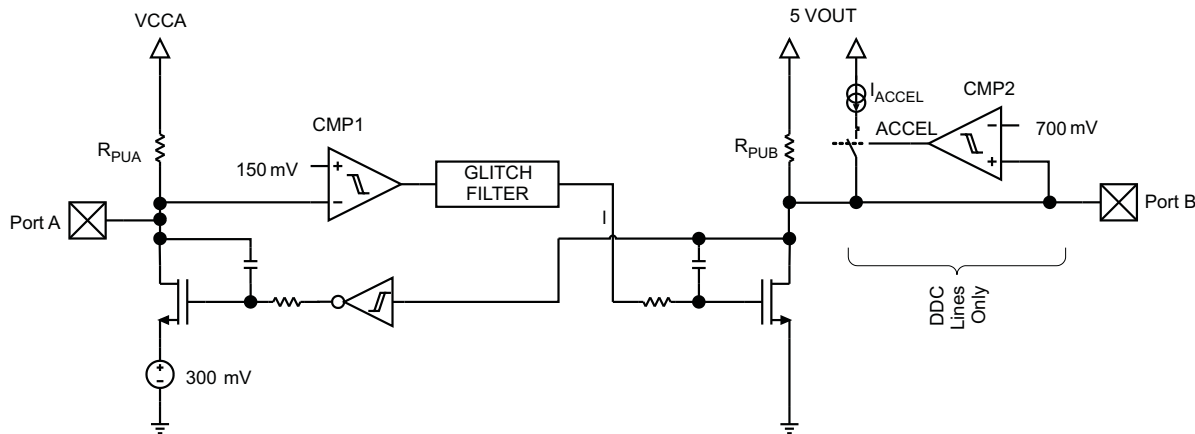


Figure 13. DDC/CEC Level Shifter Block Diagram

7.3.12 DDC/CEC Level Shifter Operational Notes For $V_{CCA} = 1.8$ V

- The threshold of CMP1 (see Figure 13) is approximately 150 mV $\pm$ the 40 mV of total hysteresis.
- The comparator will trip for a falling waveform at approximately 130 mV.
- The comparator will trip for a rising waveform at approximately 170 mV.
- To be recognized as a zero, the level at Port A must first go below 130 mV (V_{ILC} in spec) and then stay below 170 mV (V_{ILA} in spec).
- To be recognized as a one, the level at A must first go above 170 mV and then stay above 130 mV.
- V_{ILC} is set to 117 mV in Electrical Characteristics Table to give some margin to the 130 mV.
- V_{ILA} is set to 148 mV in the [Electrical Characteristics](#) table to give some margin to the 170 mV.
- V_{IHA} is set to 70% of V_{CCA} to be consistent with standard CMOS levels.

Feature Description (continued)

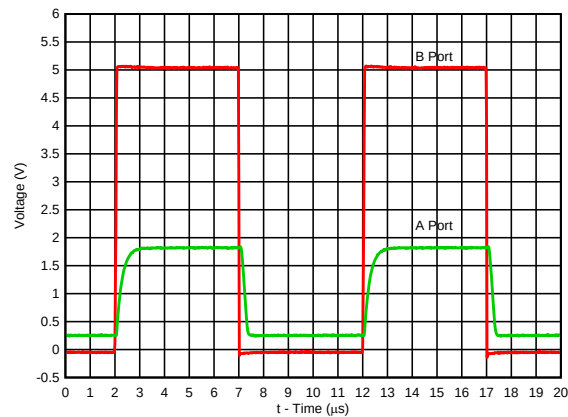


Figure 14. DDC Level Shifter Operation (B To A Direction)

7.3.13 Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support high capacitive load (up to 750 pF) on the HDMI cable side. The rise time accelerators boost the cable side DDC signal independent of which side of the bus is releasing the signal.

7.3.14 Noise Considerations

Ground offset between the TPD12S016 ground and the ground of devices on port A of the TPD12S016 must be avoided. The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 Ω or less ($R = E / I$). Such a driver will share enough current with the port A output pulldown of the TPD12S016 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILC} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD12S016 as their output LOW levels will not be recognized by the TPD12S016 as a LOW. If the TPD12S016 is placed in an application where the V_{IL} of port A of the TPD12S016 does not go below its V_{ILC} it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided. Port B is interoperable with all I²C-bus slaves, masters and repeaters.

7.3.15 Resistor Pullup Value Selection

The system is designed to work properly with no external pullup resistors on the DDC, CEC, and HPD lines.

7.4 Device Functional Modes

The LS_OE and CT_HPD are active-high enable pins. They control the TPD12S016 power saving options according to [Table 1](#).

Table 1. Power Saving Options⁽¹⁾

LS_OE	CT_HPD	V _{CCA}	V _{CC5V}	A-SIDE PULL-UPS	DDC, B- SIDE PULL-UPS	CEC_B PULL- UPS	CEC LDO	LOAD SW AND HPD	DDC/ CEC VLTs	ICCA TYP	ICC5V TYP	COMMENTS
L	L	1.8 V	5.0 V	Off	Off	Off	Off	Off	Off	1 μ A	1 μ A	Fully Disabled
L	H	1.8 V	5.0 V	On	On	Off	Off	On	Off	1 μ A	30 μ A	Load Switch on
H	L	1.8 V	5.0 V	Off	Off	Off	Off	Off	Off	1 μ A	1 μ A	Not a Valid State
H	H	1.8 V	5.0 V	On	On	On	On	On	On	13 μ A	200 μ A	Fully On
X	X	0 V	0 V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	X	1.8 V	0 V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	X	0 V	5.0 V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down

(1) X = Don't Care, H = Signal High, and L = Signal Low

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD12S016 provides IEC 61000-4-2 Level 4 Contact ESD rating to the HDMI 1.4 transmitter port. Buffered VLT's translate DDC and CEC channels bidirectionally. The system is designed to work properly with no external pullup resistors on the DDC, CEC, and HPD lines. The CEC line has an integrated 3.3-V rail, eliminating the need for a 3.3-V supply on board.

8.2 Typical Application

The TPD12S016 is placed as close as possible to the HDMI connector to provide voltage level translation, 5V_OUT current limiting and overall ESD protection for the HDMI controller.

8.2.1 Example 1: HDMI Controller Using One Control Line

In the example shown in [Figure 15](#), the HDMI driver chip is controlling the TPD12S016 through only one control line, CT_HPDP. In this mode the HPD_A to LS_OE pin are connected as shown in the oval dotted line of [Figure 15](#). To fully enable TPD12S016, set CT_HPDP above V_{IH} . To fully disable TPD12S016, set CT_HPDP below V_{IL} .

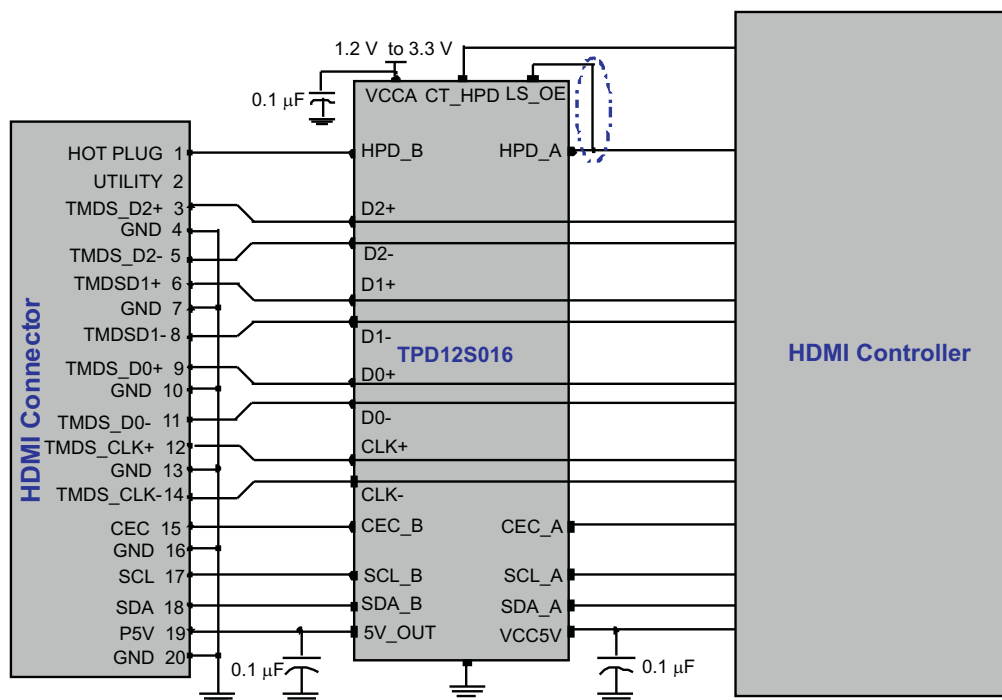


Figure 15. TPD12S016 with an HDMI Controller Using One GPIO for HDMI Interface Control

Typical Application (continued)

8.2.1.1 Design Requirements

For this example, use the following table as input parameters:

Table 2. HDMI Controller Using One Control Line Design Parameters

DESIGN PARAMETERS			EXAMPLE VALUE
Voltage on V_{CCA}			1.8 V
Voltage on V_{CC5V}			5.0 V
Drive CT_HPD low (disabled)			–0.5 V to 0.4 V
Drive CT_HPD high (enabled)			1.0 V to 1.8 V
Drive a logical 1	A to B	SCL and SDA	1.26 V to 1.8 V
		CEC	
	B to A	SCL and SDA	3.5 V to 5.0 V
		CEC	2.31 V to 3.3 V
Drive a logical 0	A to B	SCL and SDA	–0.5 V to 0.117 V
		CEC	
	B to A	SCL and SDA	–0.5 V to 1.5 V
		CEC	–0.5 V to 0.99 V

8.2.1.2 Detailed Design Procedure

To begin the design process, the designer needs to know the V_{CC5V} voltage range and the logic level, V_{CCA} , voltage range.

8.2.1.3 Application Curves

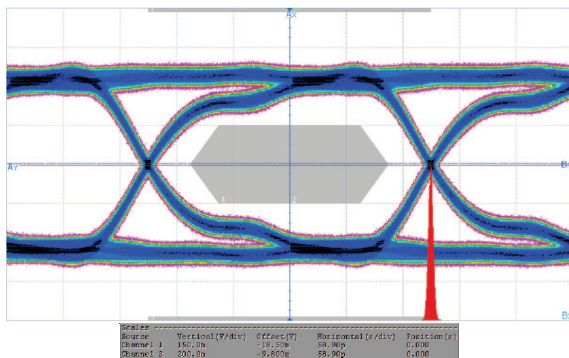


Figure 16. Eye Diagram Using EVM Without TPD12S016 for the TMDS Lines at 1080p, 340 MHz Pixel Clock, 3.4 Gbps

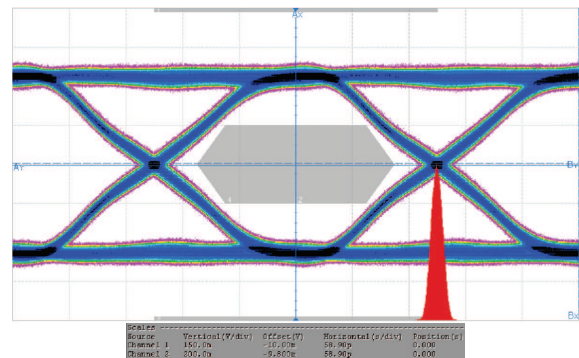


Figure 17. Eye Diagram Using EVM With TPD12S016 for the TMDS Lines at 1080p, 340 MHz Pixel Clock, 3.4 Gbps

8.2.2 Example 2: HDMI Controller Using CT_HPD and LS_OE

Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented. The load switch can be activated by CT_HPD while the level shifters are inactive, using LS_OE. This results in TPD12S016 drawing only approximately 30 μ A, a reduction of 170 μ A from being fully on. After a hot plug is detected, the HDMI controller can enable the rest of the HDMI interface chip using LS_OE.

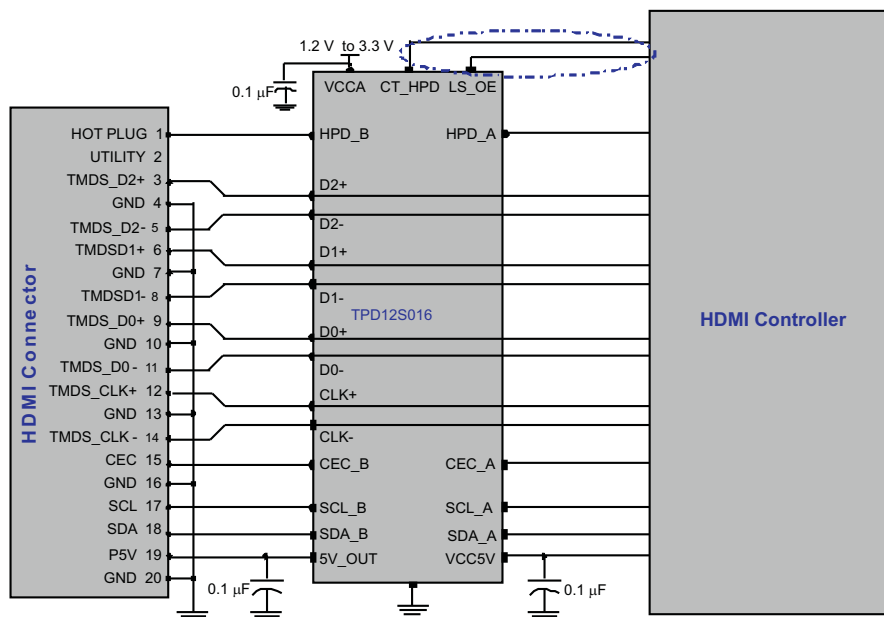


Figure 18. TPD12S016 with an HDMI Controller Using Two GPIOs For HDMI Interface Control

8.2.2.1 Design Requirements

For this example, use [Table 3](#) for input parameters:

Table 3. HDMI Controller Using CT_HPD and LS_OE Design Parameters

DESIGN PARAMETERS			EXAMPLE VALUE
Voltage on V _{CCA}			3.3 V
Voltage on V _{CC5V}			5.0 V
Drive CT_HPD low (disabled)			−0.5 V to 0.4 V
Drive LS_OE low (disabled)			
Drive CT_HPD high (enabled)			1.0 V to 3.3 V
Drive LS_OE high (enabled)			
Drive a logical 1	A to B	SCL and SDA	2.31 V to 3.3 V
		CEC	
	B to A	SCL and SDA	3.5 V to 5.0 V
		CEC	2.31 V to 3.3 V
Drive a logical 0	A to B	SCL and SDA	−0.5 V to 0.214 V
		CEC	
	B to A	SCL and SDA	−0.5 V to 1.5 V
		CEC	−0.5 V to 0.99 V

8.2.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the V_{CC5V} voltage range and the logic level, V_{CCA} , voltage range.

8.2.2.3 Application Curves

Refer to [Application Curves](#) for related application curves.

9 Power Supply Recommendations

TPD12S016 has two power input pins: V_{CC5V} and V_{CCA} . It can operate normally with V_{CC5V} between 4.5 V and 5.5 V; and V_{CCA} between 1.1 V and 3.6 V. Thus, the power supply (with a ripple of V_{RIPPLE}) requirement for TPD12S016 for V_{CC5V} is between $4.5\text{ V} + V_{RIPPLE}$ and $5.5\text{ V} - V_{RIPPLE}$; and for V_{CCA} it is between $1.1\text{ V} + V_{RIPPLE}$ and $3.6\text{ V} - V_{RIPPLE}$.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. Therefore, the PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Avoid using VIAs between the connector and an I/O protection pin on TPD12S016.
- Avoid 90° turns in traces.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- Minimize impedance on the path to GND for maximum ESD dissipation.
- The capacitors on V_{BUS} and V_{OTG_IN} should be placed close to their respective pins on TPD12S016.

10.2 Layout Examples

10.2.1 TPD12S016RKT

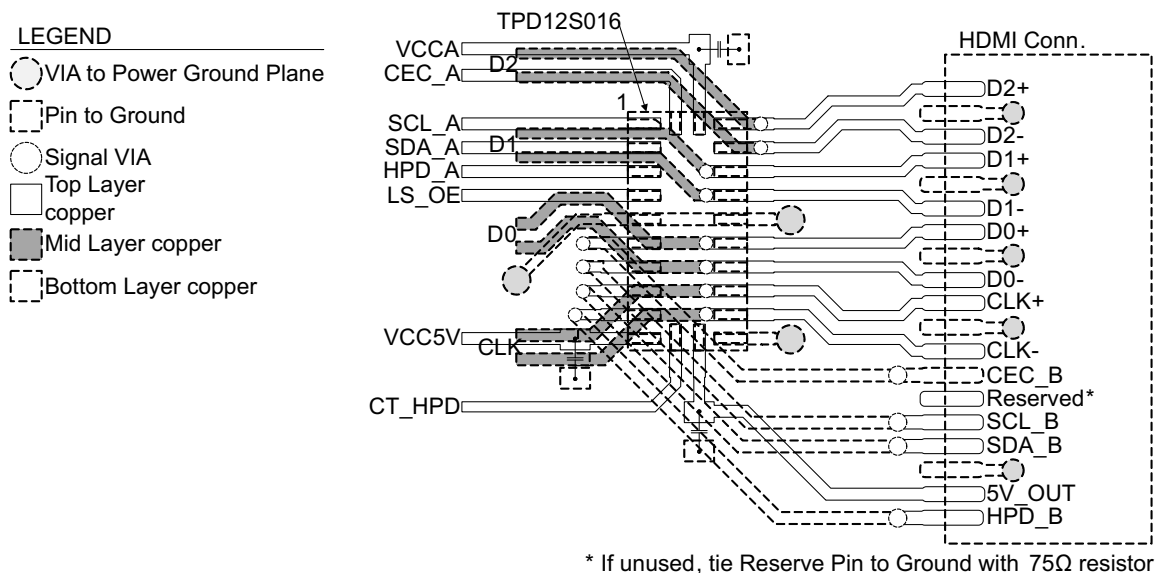
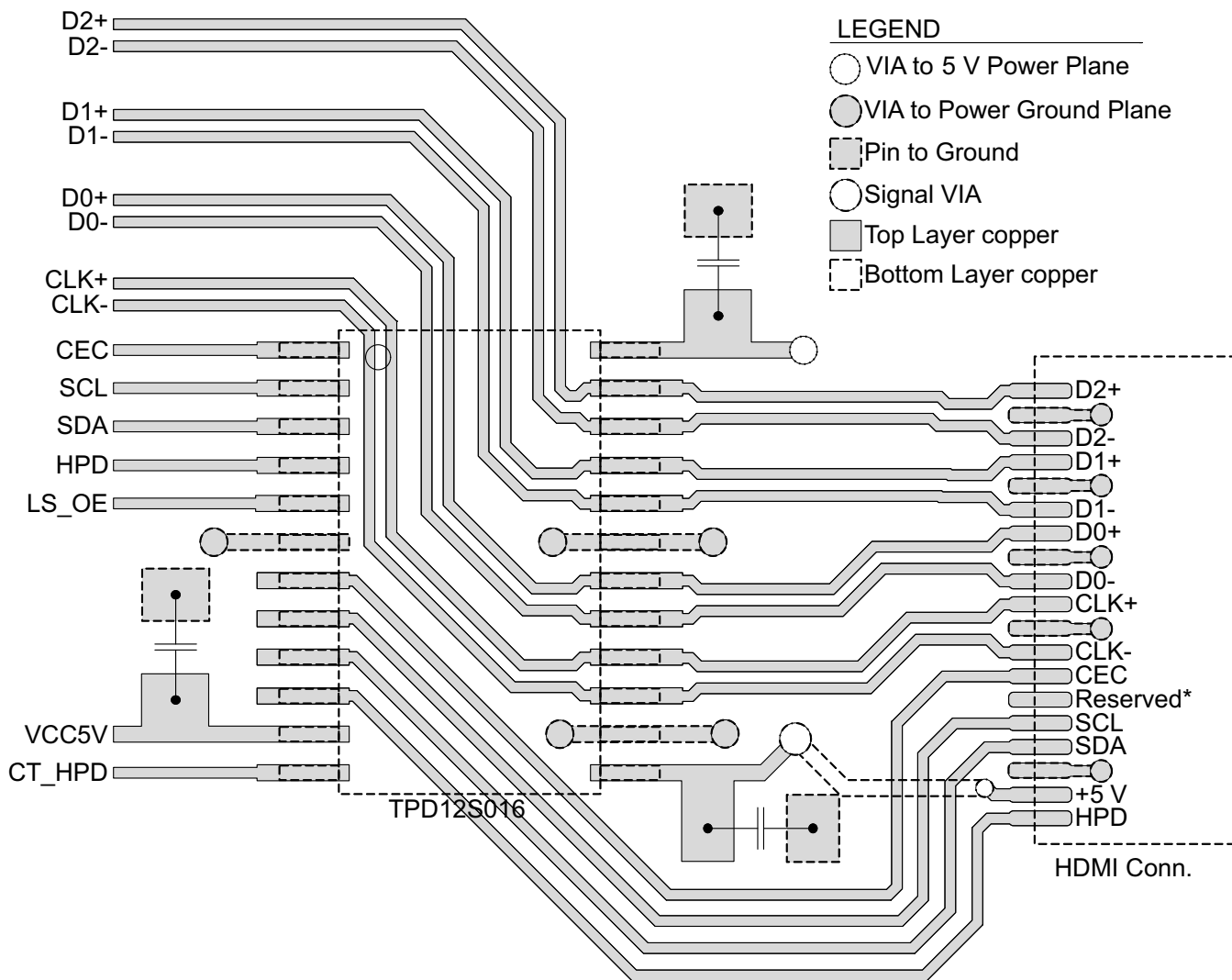


Figure 19. TPD12S016RKT Layout Example

Layout Examples (continued)

Routing with TPD12S016RKT requires three layers. Vias are an integral part of layout for such a design. Proper placement of vias can eliminate exposing the system unnecessarily to an ESD event. The example shown above routes the TMDS lines directly from the connector to the protection pins *before* using vias to an internal layer. This helps promote ESD energy dissipation at the TPD12S016 protection pins. Note that while there is a via between the connector and the DDC/CEC/HPD lines, the traces terminate at the protection pins, leaving no other path for ESD energy to dissipate except at the TPD12S016 protection pins. All ground pins should have a large via near them connecting to as many internal and external ground planes as possible to reduce any impedance between TPD12S016 and ground. Tenting of VIAs near to SMD pads should be done to eliminate any solder-wicking during PCB assembly.

10.2.2 TPD12S016PW



* If unused, tie Reserve Pin to Ground with 75Ω resistor

Figure 20. TPD12S016PW Layout Example

The TPD12S016PW can be routed on a single layer. HDMI connector pin matching has been arranged to allow for a flow through routing style. All ground pins should have a large via near them connecting to as many internal and external ground planes as possible to reduce any impedance between TPD12S016 and ground. Tenting of vias near to SMD pads should be done to eliminate any solder-wicking during PCB assembly.

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

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11.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD12S016PWR	NRND	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PN016
TPD12S016PWR.B	NRND	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PN016
TPD12S016PWRG4	NRND	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PN016
TPD12S016PWRG4.B	NRND	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PN016
TPD12S016RKTR	NRND	Production	UQFN (RKT) 24	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PN016
TPD12S016RKTR.B	NRND	Production	UQFN (RKT) 24	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PN016

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

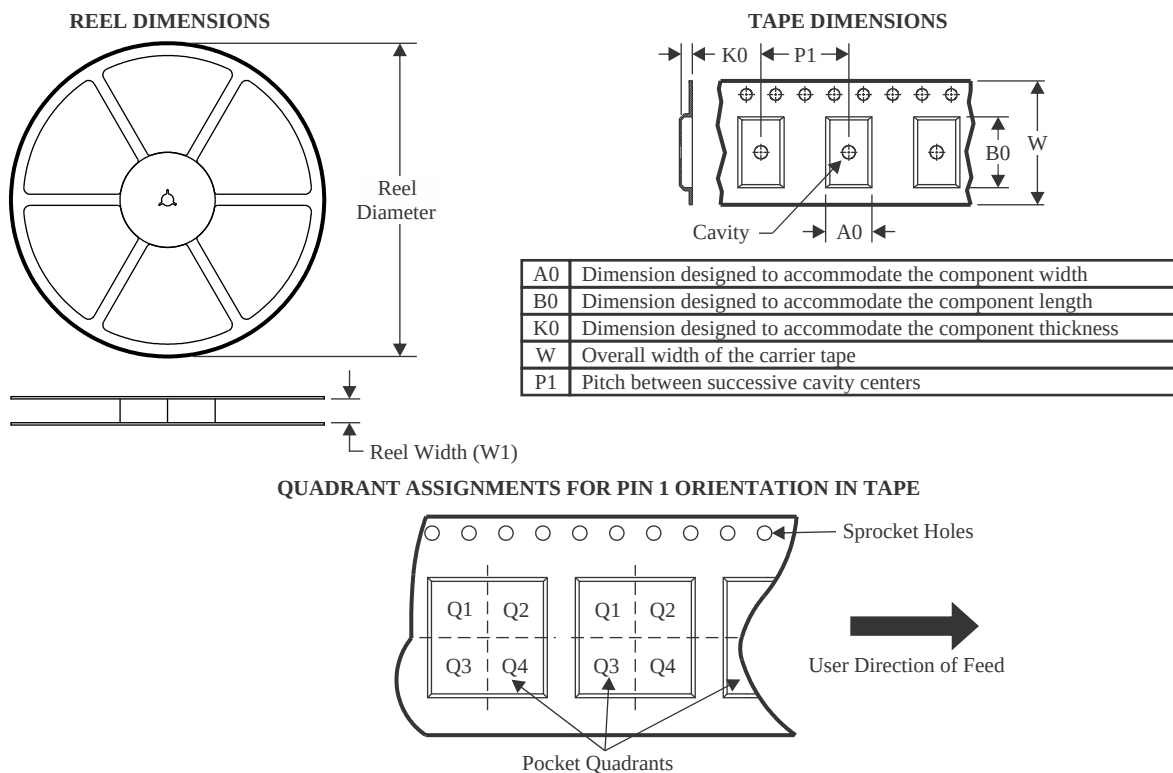
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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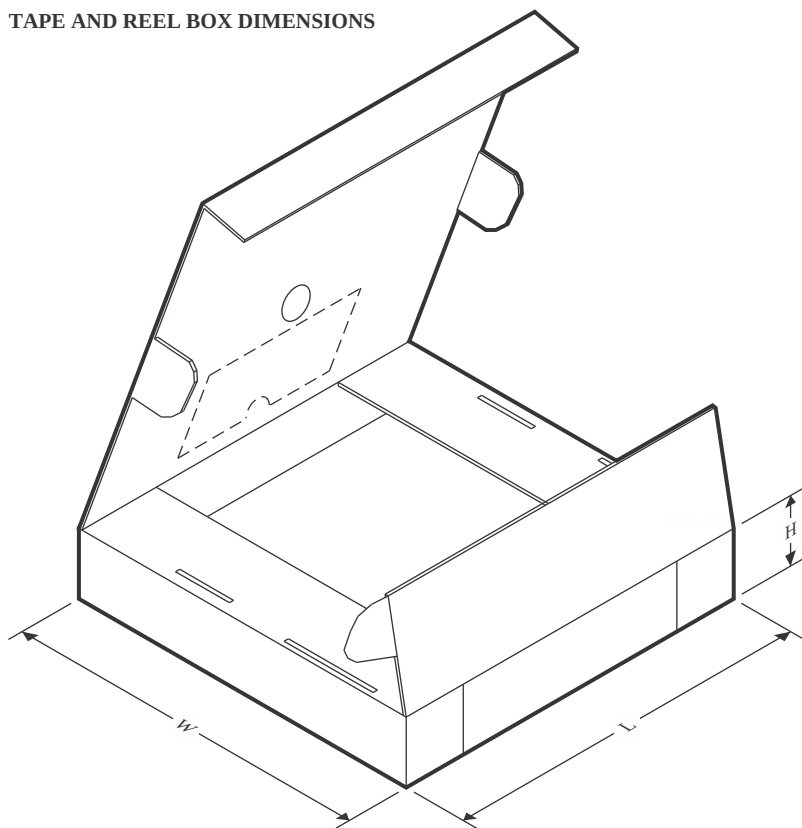
TAPE AND REEL INFORMATION



*All dimensions are nominal

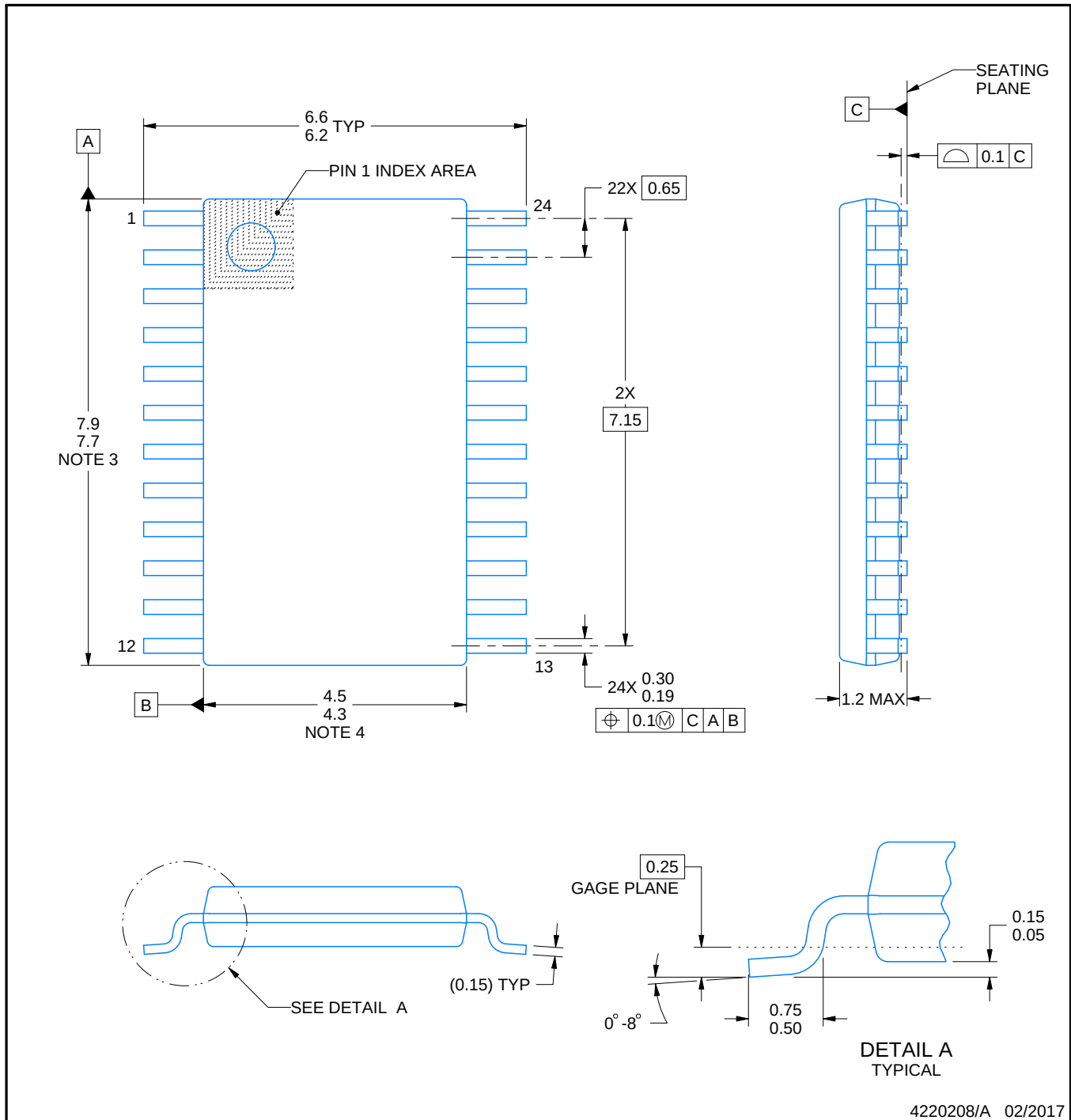
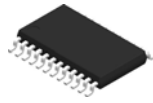
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD12S016PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPD12S016PWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPD12S016RKTR	UQFN	RKT	24	3000	177.8	12.4	2.21	4.22	0.81	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD12S016PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
TPD12S016PWRG4	TSSOP	PW	24	2000	353.0	353.0	32.0
TPD12S016RKTR	UQFN	RKT	24	3000	183.0	183.0	20.0



4220208/A 02/2017

NOTES:

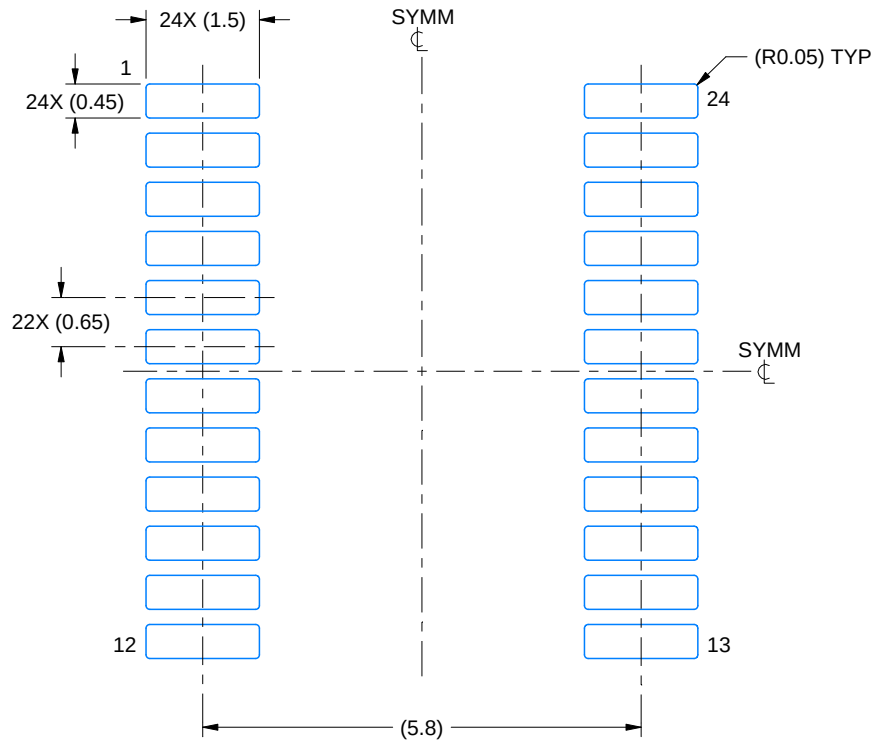
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

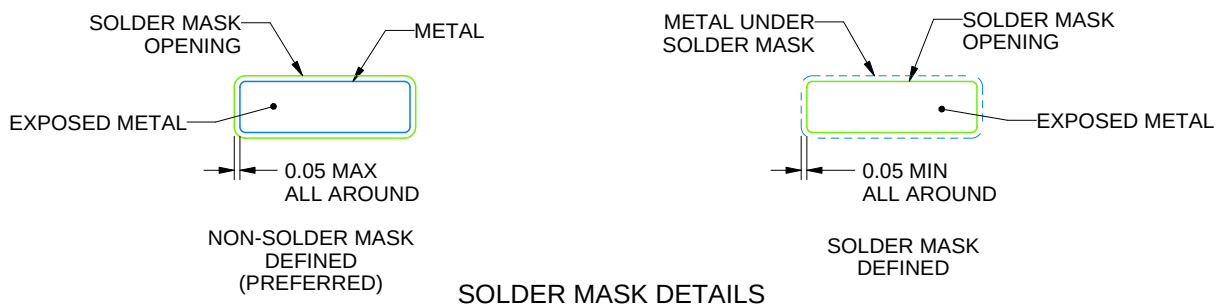
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

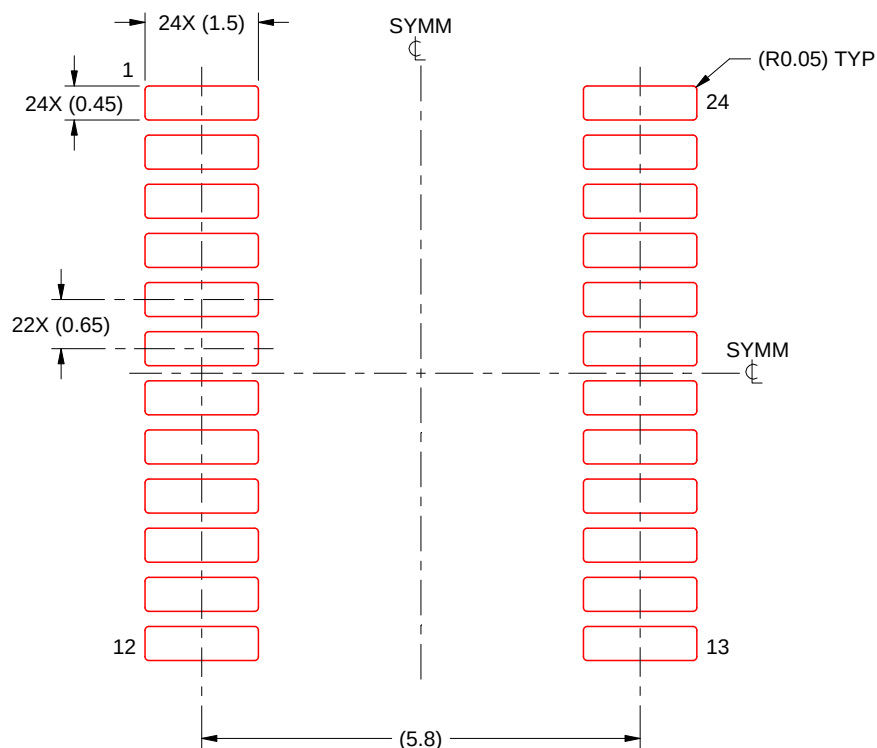
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

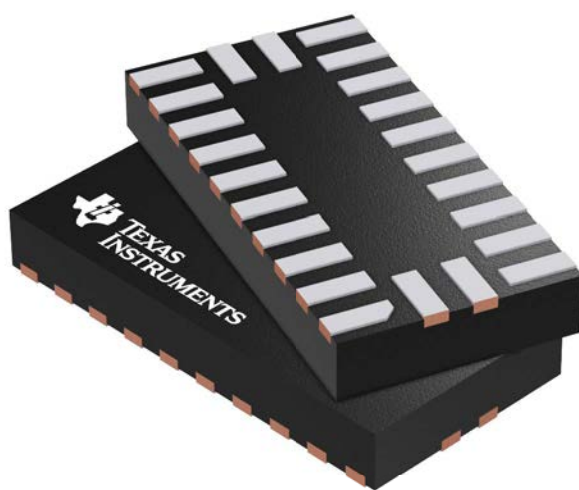
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RKT 24

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211396/B

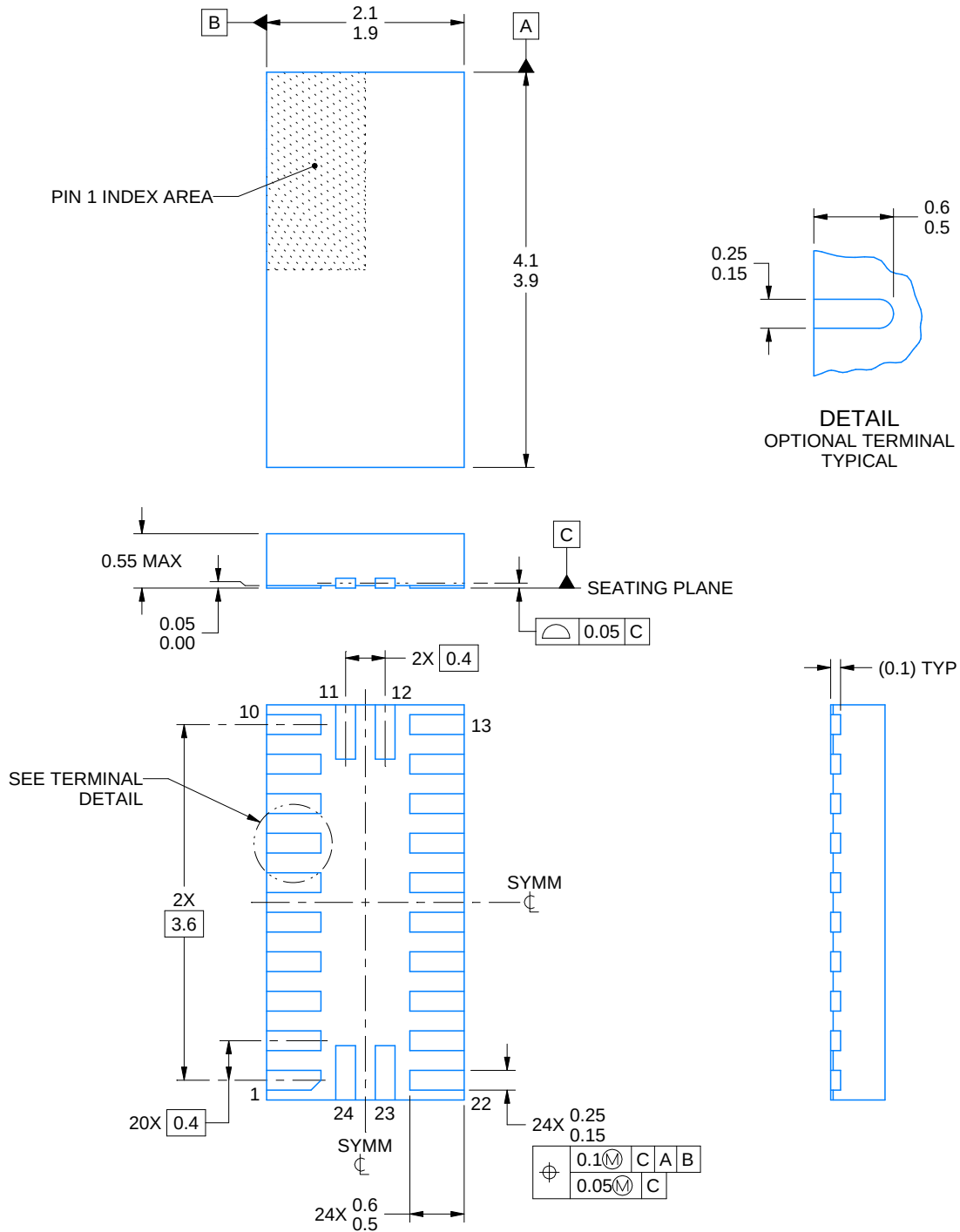
RKT0024A



PACKAGE OUTLINE

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4220317/A 02/2017

NOTES:

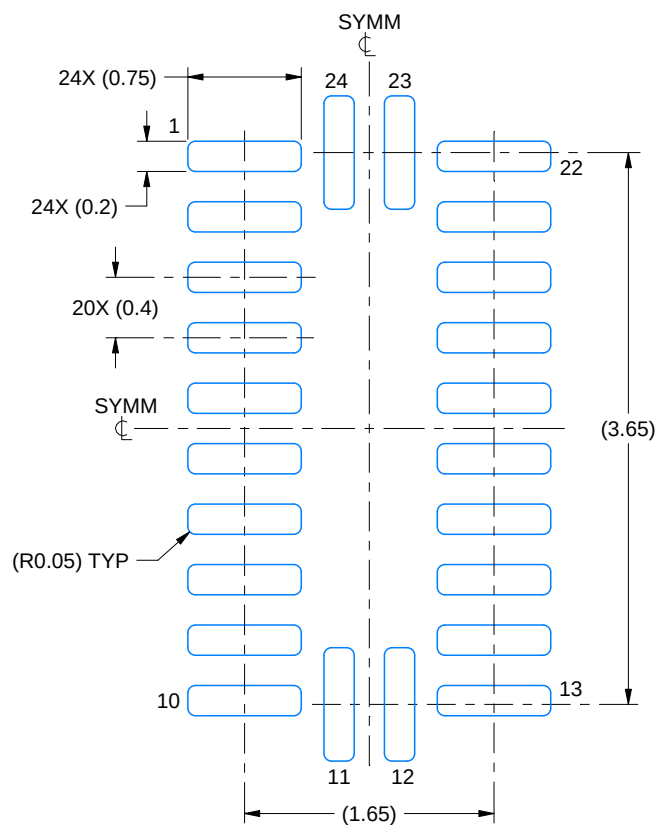
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

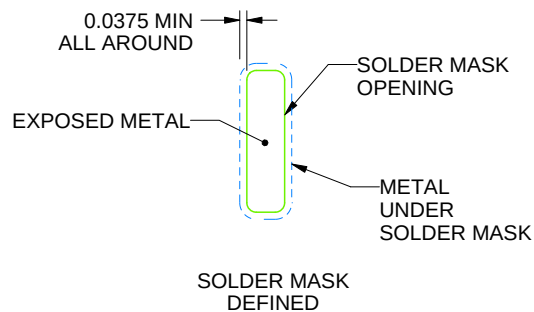
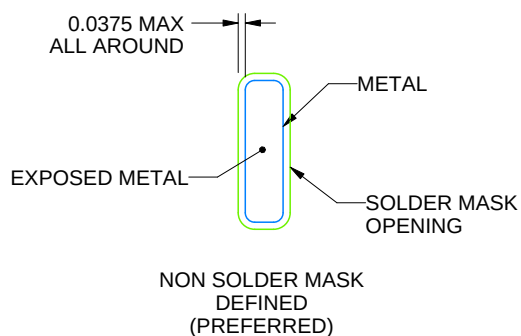
RKT0024A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS
NOT TO SCALE

4220317/A 02/2017

NOTES: (continued)

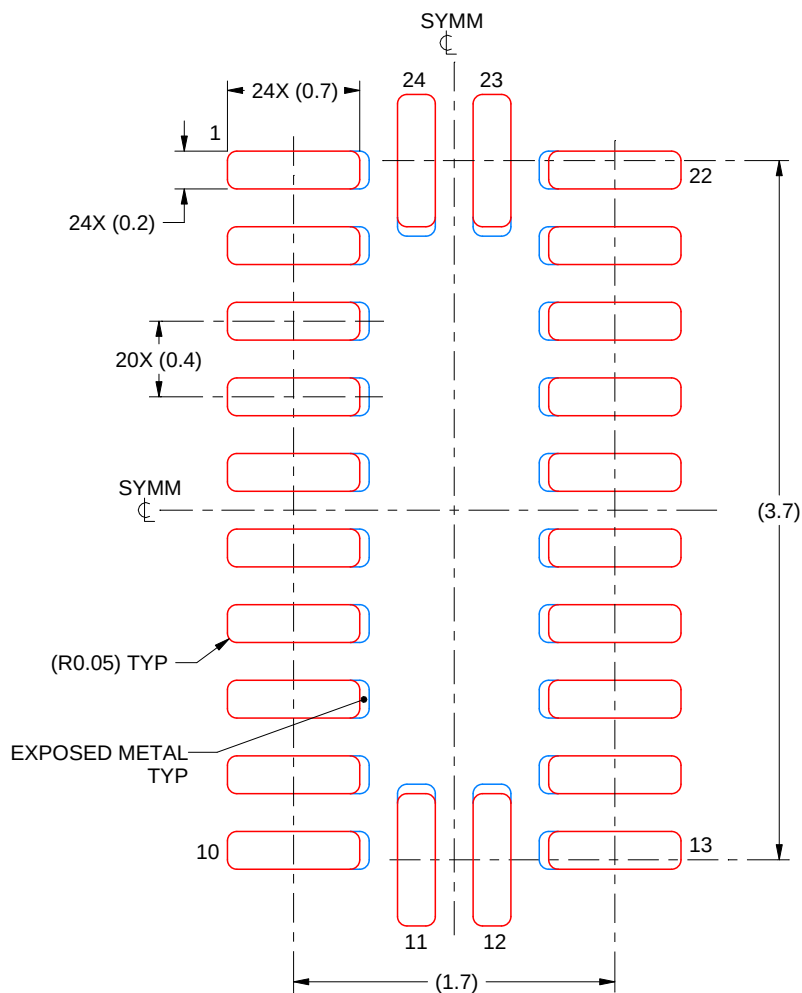
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RKT0024A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE:25X

4220317/A 02/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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