TPD1E04U04 适用于 HDMI 2.0 和 USB 3.0 的低 R_{DYN} 单通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
  - ±16kV 接触放电
  - ±16kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 2.5A (8/20μs)
- IO 电容：0.5pF（典型值）、0.65pF（最大值）
- 超低 ESD 钳位电压
  - 16A TLP 时为 8.9V
  - -16A TLP 时为 -4.6V
- 低 R_{DYN}
  - IO 与 GND 之间为 0.25Ω
  - GND 与 IO 之间为 0.18Ω
- 直流击穿电压：5V（最小值）
- 超低泄漏电流：10nA（最大值）
- 支持速率最高达 6Gbps 的高速接口
- 工业温度范围：-40°C 至 +125°C
- 符合行业标准的 0402 封装

2 应用

- 终端设备
  - 机顶盒
  - 便携式计算机和台式机
  - 电视和监视器
  - 手机和平板电脑
  - 数字视频录像机 (DVR) 和网络视频录像机 (NVR)
- 接口
  - HDMI 2.0
  - HDMI 1.4b
  - USB 3.0
  - DisplayPort 1.2
  - PCI Express 3.0

3 说明

TPD1E04U04 是一款单向 TVS ESD 保护二极管，用于为 HDMI 2.0 和 USB 3.0 电路提供保护。TPD1E04U04 的额定 ESD 冲击消散值高于 IEC 61000-4-2（4 级）国际标准中规定的最高水平。

该器件 特有 一个 0.5pF IO 电容，适合于保护速率高达 6Gbps 的高速接口，例如 HDMI 2.0 和 USB 3.0 接口。低动态电阻和超低钳位电压可为敏感的 SoC 提供针对瞬变事件的系统级保护。

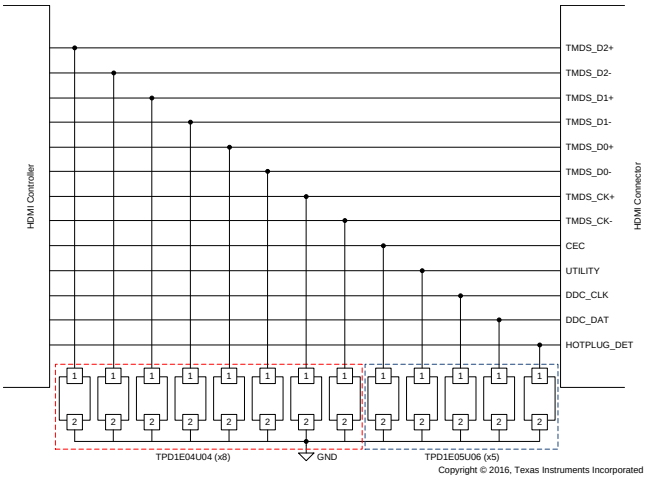
TPD1E04U04 采用符合行业标准的 0402 (DPY) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E04U04	X1SON (2)	0.6mm x 1.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型的 HDMI 2.0 应用



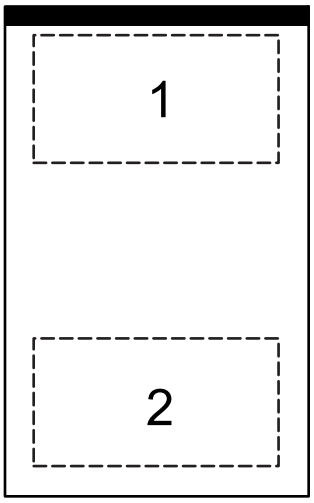
目录

4 修订历史记录

Changes from Original (March 2016) to Revision A	**Page**
• 已将器件状态从*产品预览*更改为*量产数据*	1

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel
2	GND	Ground	Ground. Connect to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs)		19	W
	IEC 61000-4-5 current (t_p - 8/20 µs)		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±16000	V
		IEC 61000-4-2 air-gap discharge	±16000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD1E04U04 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	683.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	494.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	568.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	217.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	568.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA			3.6	V
V_{BR}	Breakdown voltage, IO pin to GND	T_A = 25°C(1)	5	6.2	7.5	V
V_F	Forward diode voltage, GND to IO pin	I_{IO} = 1 mA, T_A = 25°C		0.8		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA		5.3		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		5.3		V
		I_{PP} = 16 A, TLP, from IO to GND		8.9		
		I_{PP} = 1 A, TLP, from GND to IO		1.3		
		I_{PP} = 16 A, TLP, from GND to IO		4.6		
I_{LEAK}	Leakage current, any IO to GND	V_{IO} = 2.5 V		0.1	10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.25		Ω
		GND to IO		0.18		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.5	0.65	pF

(1) Measured as the maximum voltage before device snaps back into V_{HOLD} voltage.

6.7 Typical Characteristics

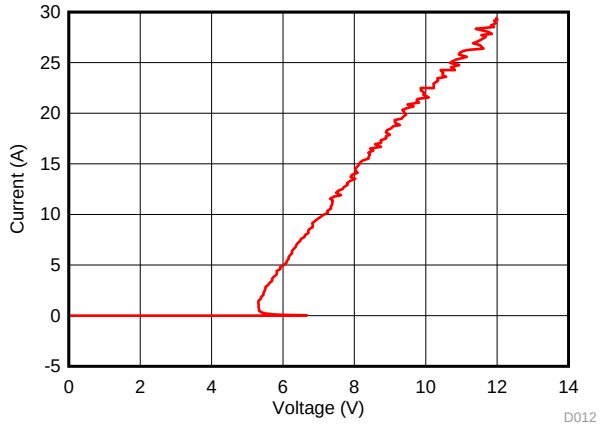


Figure 1. Positive TLP Curve

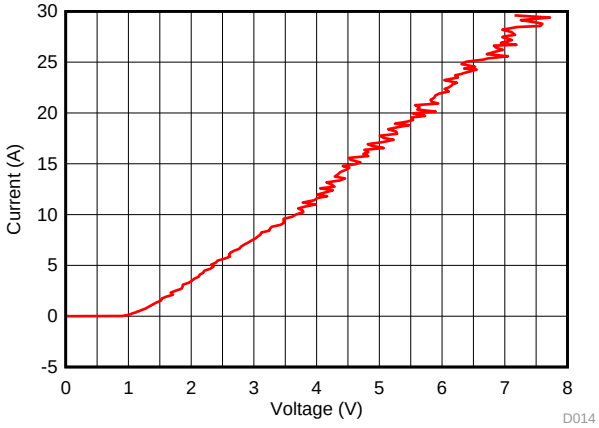


Figure 2. Negative TLP Curve

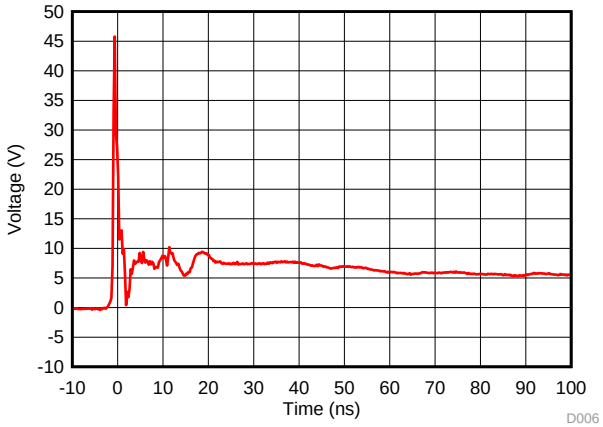


Figure 3. 8-kV IEC Waveform

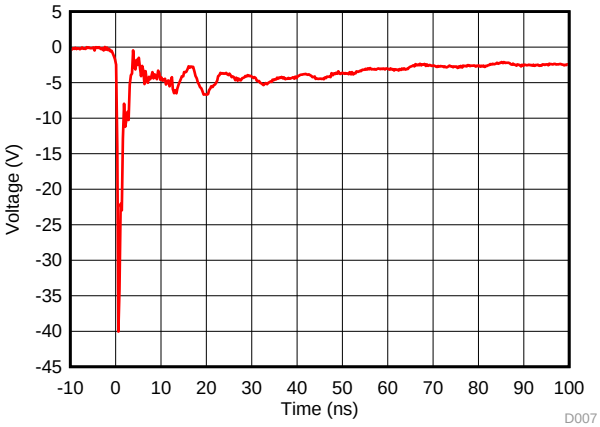


Figure 4. –8-kV IEC Waveform

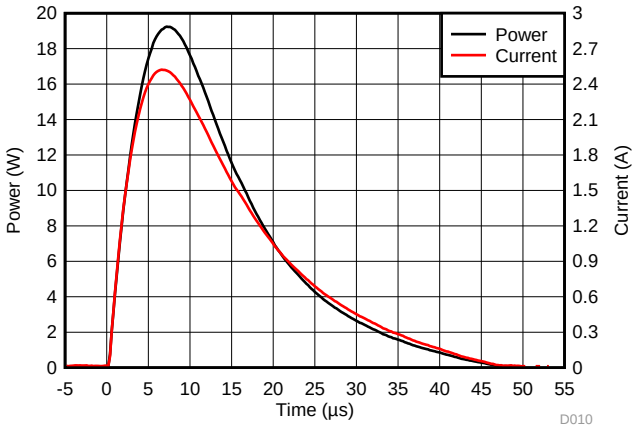


Figure 5. Surge Curve (t_p = 8/20µs), IO Pin to GND

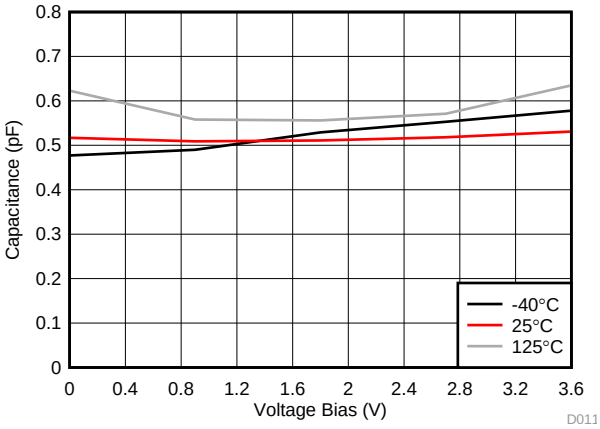


Figure 6. Capacitance vs. Bias Voltage

Typical Characteristics (continued)

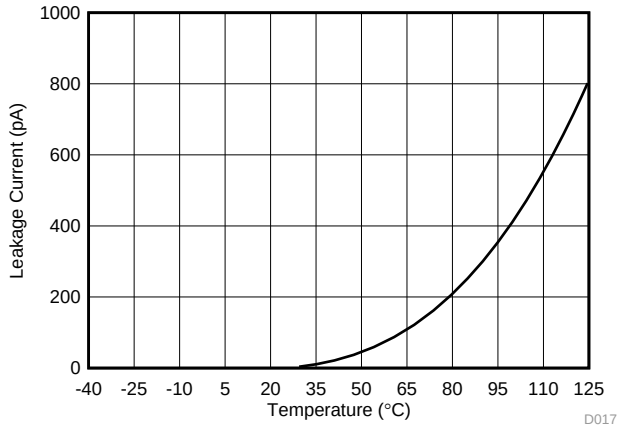


Figure 7. Leakage Current vs. Temperature

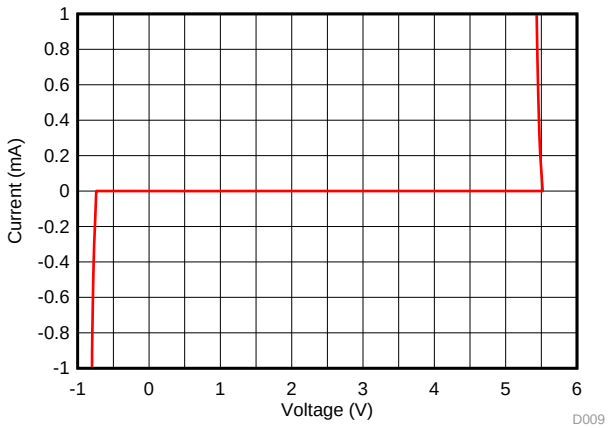


Figure 8. DC Voltage Sweep I-V Curve

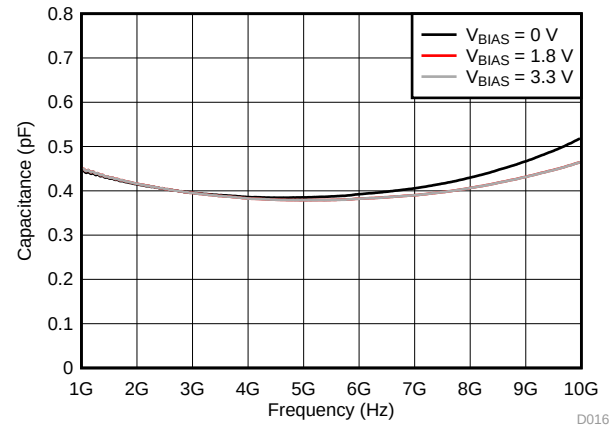


Figure 9. Capacitance vs. Frequency

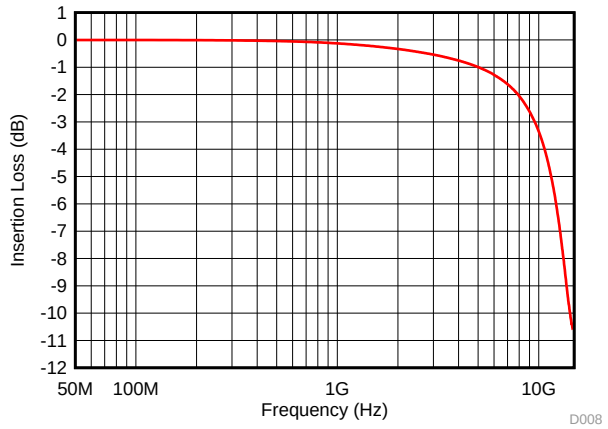


Figure 10. Insertion Loss

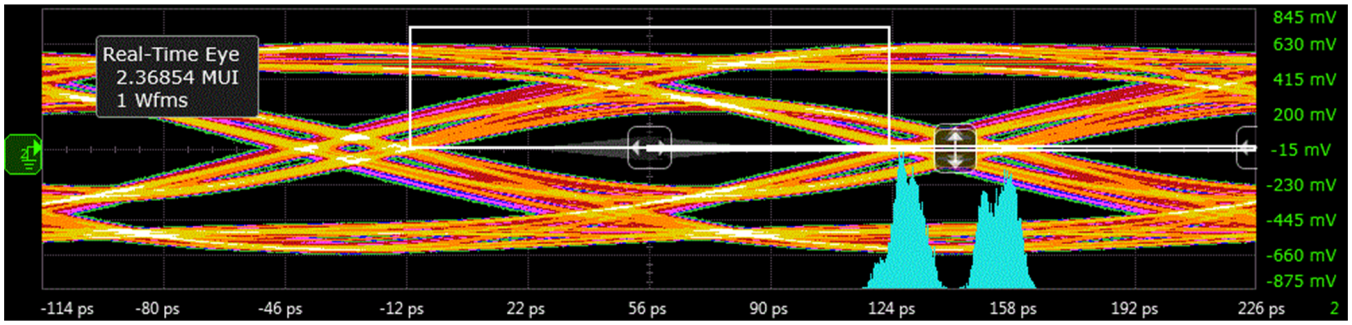


Figure 11. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

Typical Characteristics (continued)

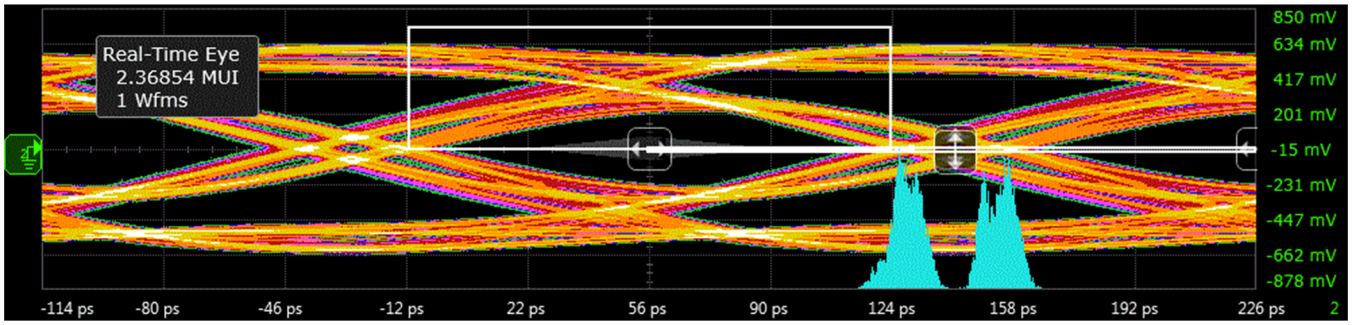


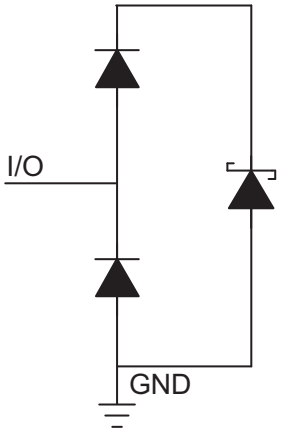
Figure 12. HDMI2.0 6-Gbps TP2 Eye Diagram (with TPD1E04U04)

7 Detailed Description

7.1 Overview

The TPD1E04U04 is a unidirectional ESD Protection Diode with ultra-low capacitance designed for HDMI 2.0 and USB 3.0. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The extremely low clamping voltage and low R_{DYN} make this device ideal for supporting the next-generation small feature size SoCs. The low capacitance also makes this device ideal for protecting any high-speed signal pins on these sensitive interface pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The IO pins can withstand ESD events up to ±16-kV contact and ±16-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The IO pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 2.5 A and 19 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each IO pin to ground is 0.5-pF (typical) and 0.65-pF (maximum). This device supports data rates up to 6 Gbps.

7.3.5 Ultra-Low ESD Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 8.9 V (I_{TLP} = 16 A) and –4.6 V (I_{TLP} = –16 A).

7.3.6 Low R_{DYN}

The IO pins feature an ESD clamp that has an extremely low R_{DYN} of 0.25 Ω (IO to GND) and 0.18 Ω (GND to IO) which prevents system damage during ESD events.

Feature Description (continued)

7.3.7 DC Breakdown Voltage

The DC breakdown voltage of each IO pin is a minimum of 5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 3.6 V.

7.3.8 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of 2.5 V

7.3.9 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 6 Gbps, because of the very low IO capacitance.

7.3.10 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.11 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD1E04U04 is a passive integrated circuit that triggers when voltages are above V_{BR} or below V_F. During ESD events, voltages as high as ±16-kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E04U04 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E04U04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

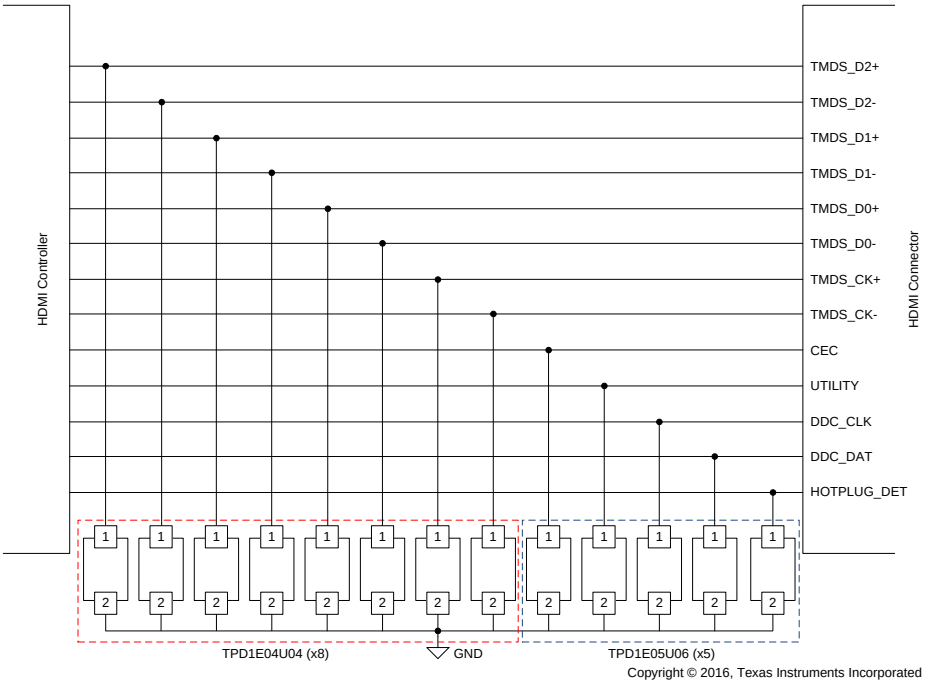


Figure 13. HDMI 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example eight TPD1E04U04 devices and five TPD1E05U06 devices are being used in a HDMI 2.0 application. This provides a complete ESD protection scheme.

Given the HDMI 2.0 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal Range on TMDS Lines	0 V to 3.6 V
Operating Frequency on TMDS Lines	up to 3 GHz
Signal Range on Control Lines	0 V to 5.5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E04U04 supports signal ranges between 0 V and 3.6 V, which supports the TMDS pairs on the HDMI 2.0 application. The TPD1E05U06 supports signal ranges between 0 V and 5.5 V, which supports the control lines.

8.2.2.2 Operating Frequency

The TPD1E04U04 has a 0.5-pF (typcal) capacitance, which supports the HDMI 2.0 data rates of 6-Gbps. The TPD1E05U06 has a 0.5-pF (typical) capacitance as well, which easily supports the control line data rates.

8.2.3 Application Curves

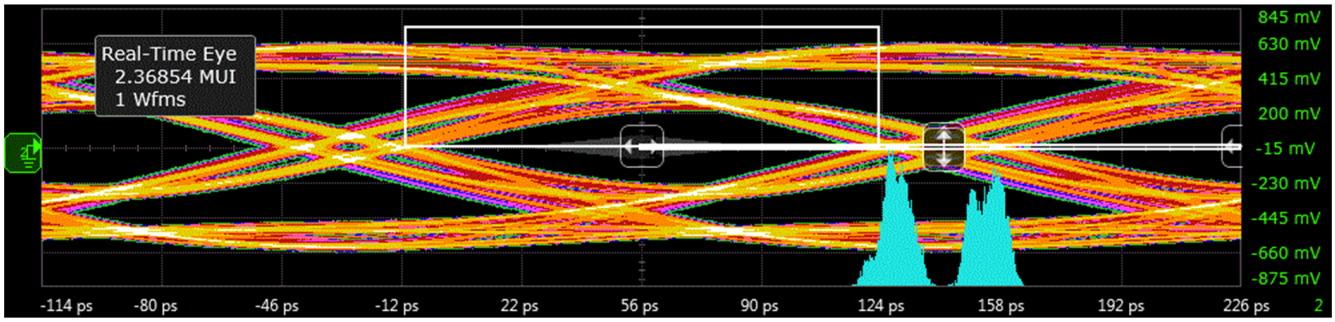


Figure 14. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

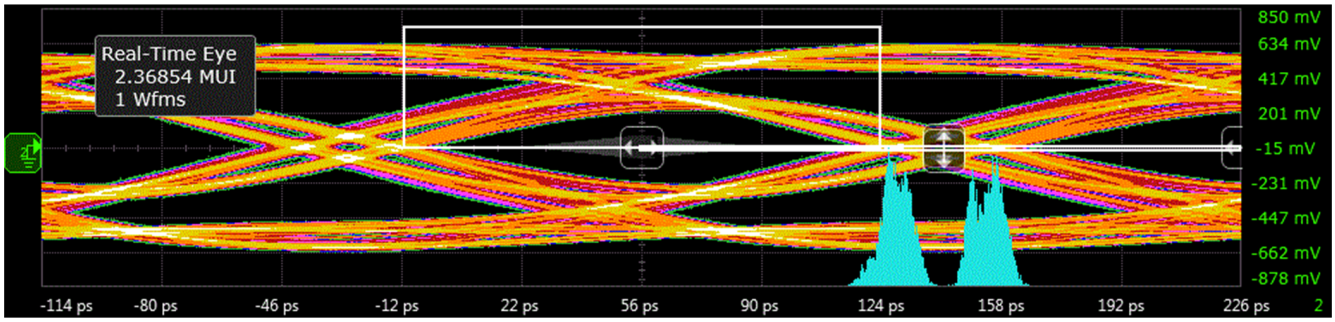


Figure 15. HDMI2.0 6-Gbps TP2 Eye Diagram (with TPD1E04U04)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended IO specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

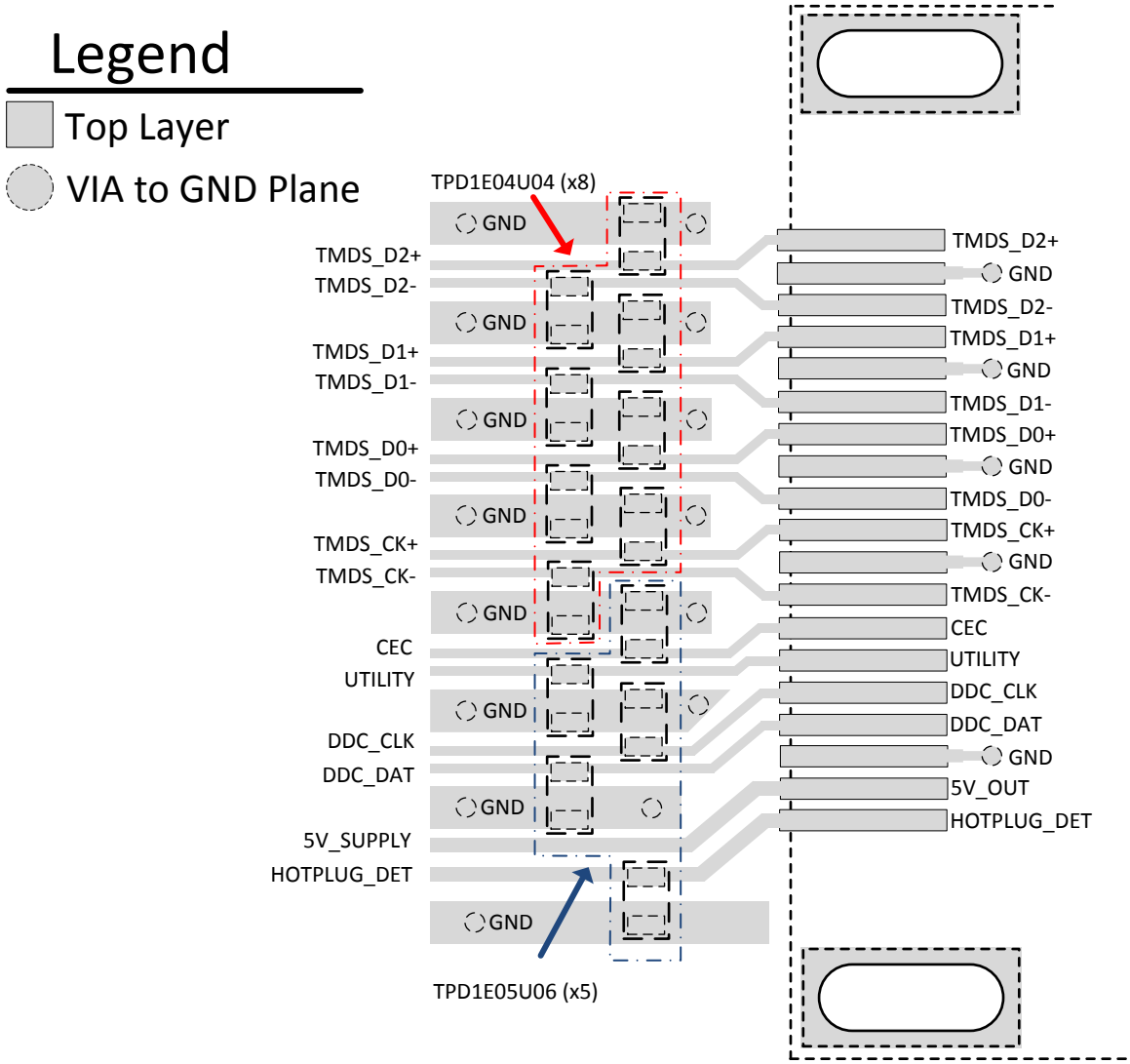


Figure 16. HDMI2.0 Type-A Transmitter Port ESD Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参见以下部分：

《TPD1E04U04 评估模块用户指南》，SLVUAN8

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E04U04DPLR	ACTIVE	X2SON	DPL	2	15000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K	Samples
TPD1E04U04DPLT	ACTIVE	X2SON	DPL	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K	Samples
TPD1E04U04DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3K	Samples
TPD1E04U04DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3K	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

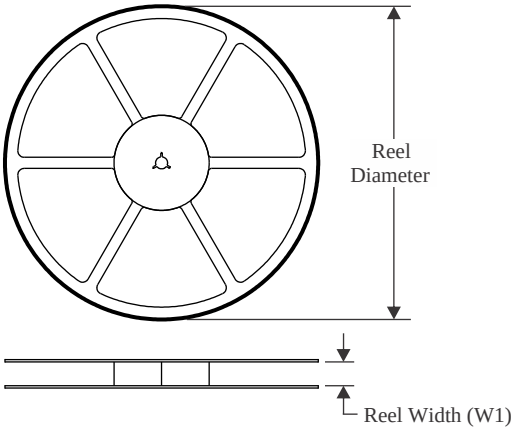
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

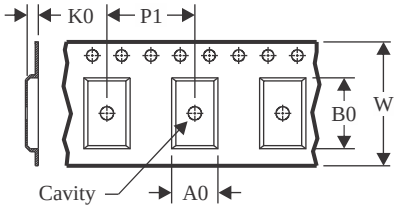
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

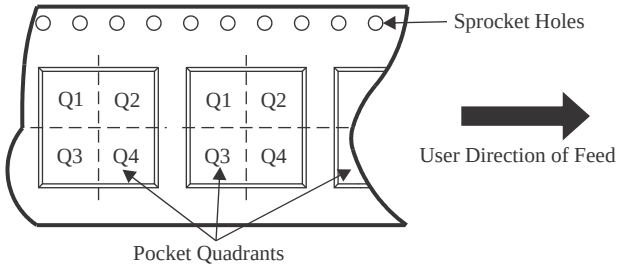


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

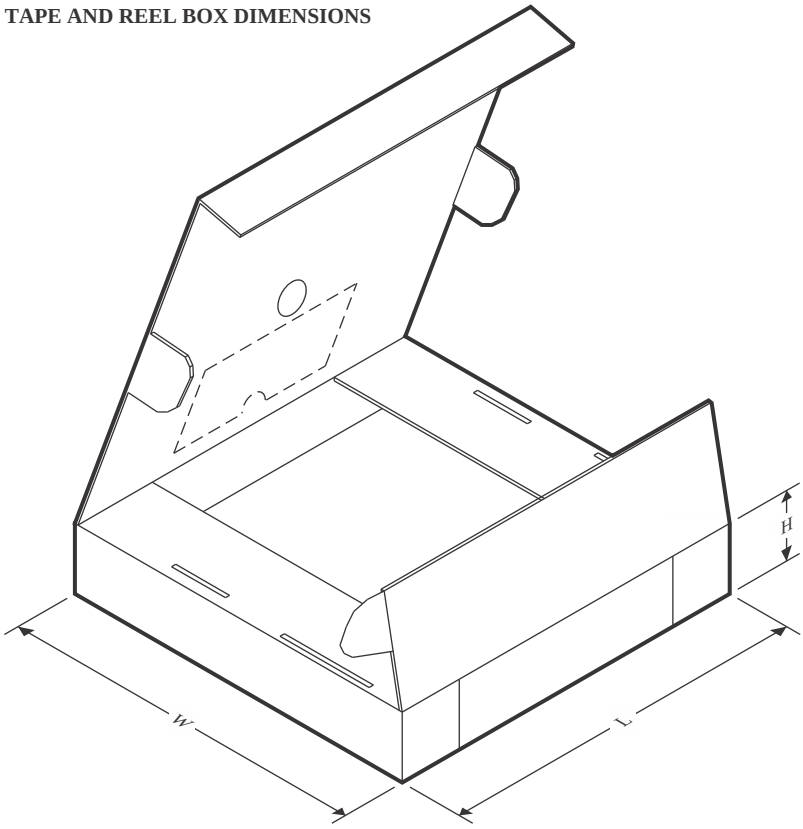
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E04U04DPLR	X2SON	DPL	2	15000	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1
TPD1E04U04DPLR	X2SON	DPL	2	15000	178.0	9.5	0.39	0.68	0.38	2.0	8.0	Q1
TPD1E04U04DPLT	X2SON	DPL	2	250	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1
TPD1E04U04DPLT	X2SON	DPL	2	250	178.0	9.5	0.39	0.68	0.38	2.0	8.0	Q1
TPD1E04U04DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
TPD1E04U04DPYT	X1SON	DPY	2	250	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

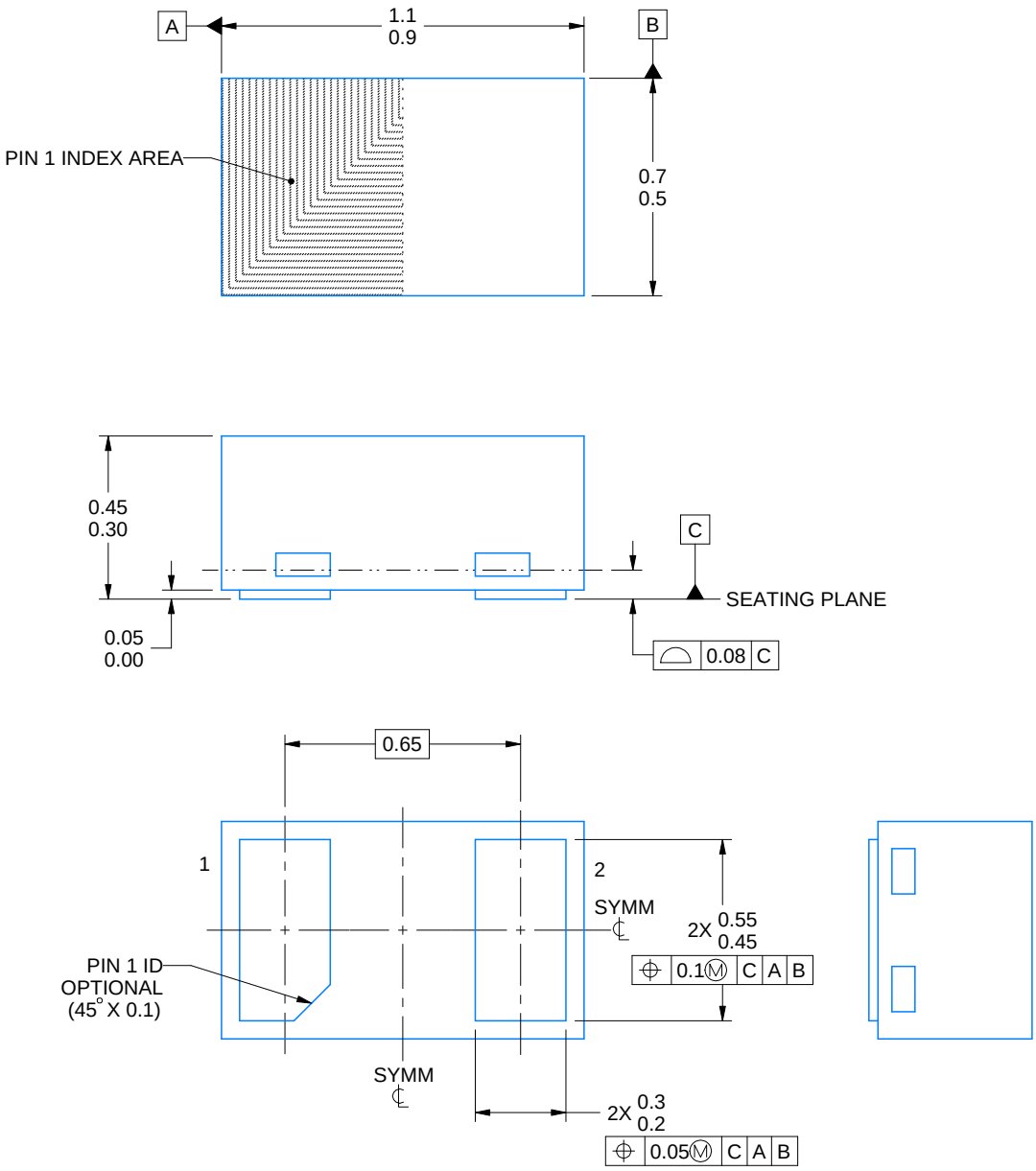
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E04U04DPLR	X2SON	DPL	2	15000	205.0	200.0	33.0
TPD1E04U04DPLR	X2SON	DPL	2	15000	184.0	184.0	19.0
TPD1E04U04DPLT	X2SON	DPL	2	250	205.0	200.0	33.0
TPD1E04U04DPLT	X2SON	DPL	2	250	184.0	184.0	19.0
TPD1E04U04DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0
TPD1E04U04DPYT	X1SON	DPY	2	250	210.0	185.0	35.0

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

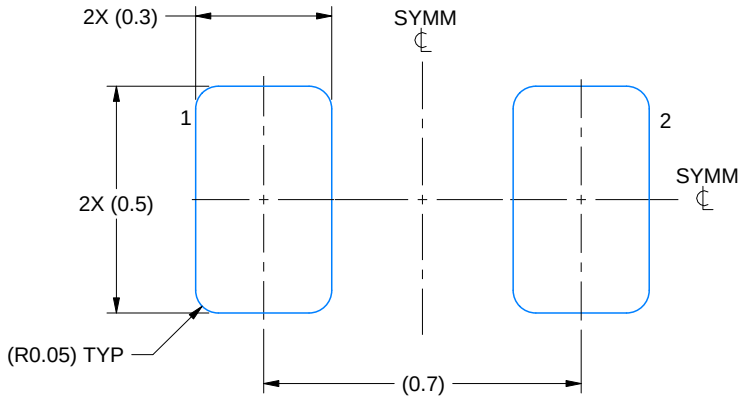
PLASTIC SMALL OUTLINE - NO LEAD



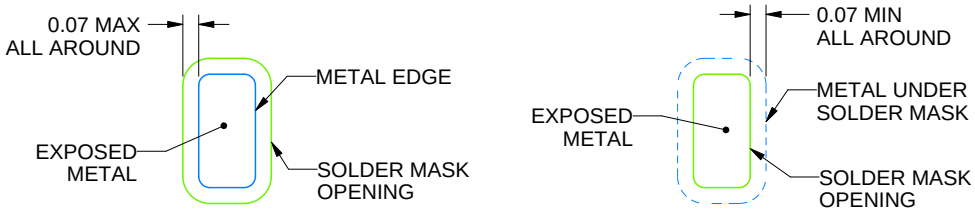
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

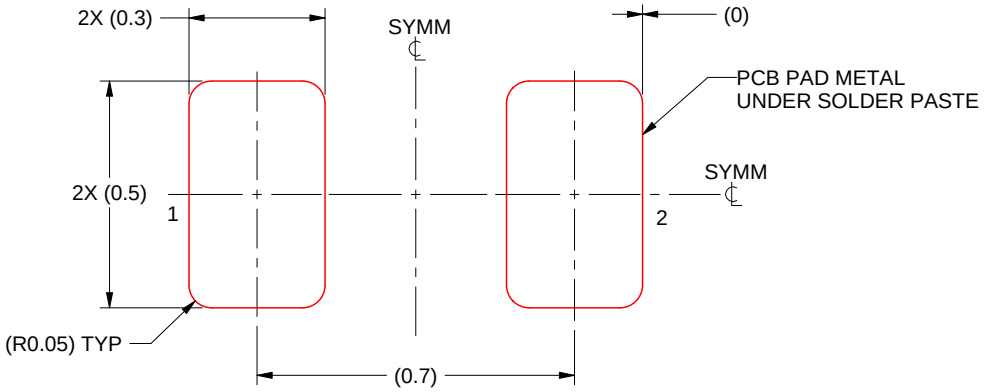


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



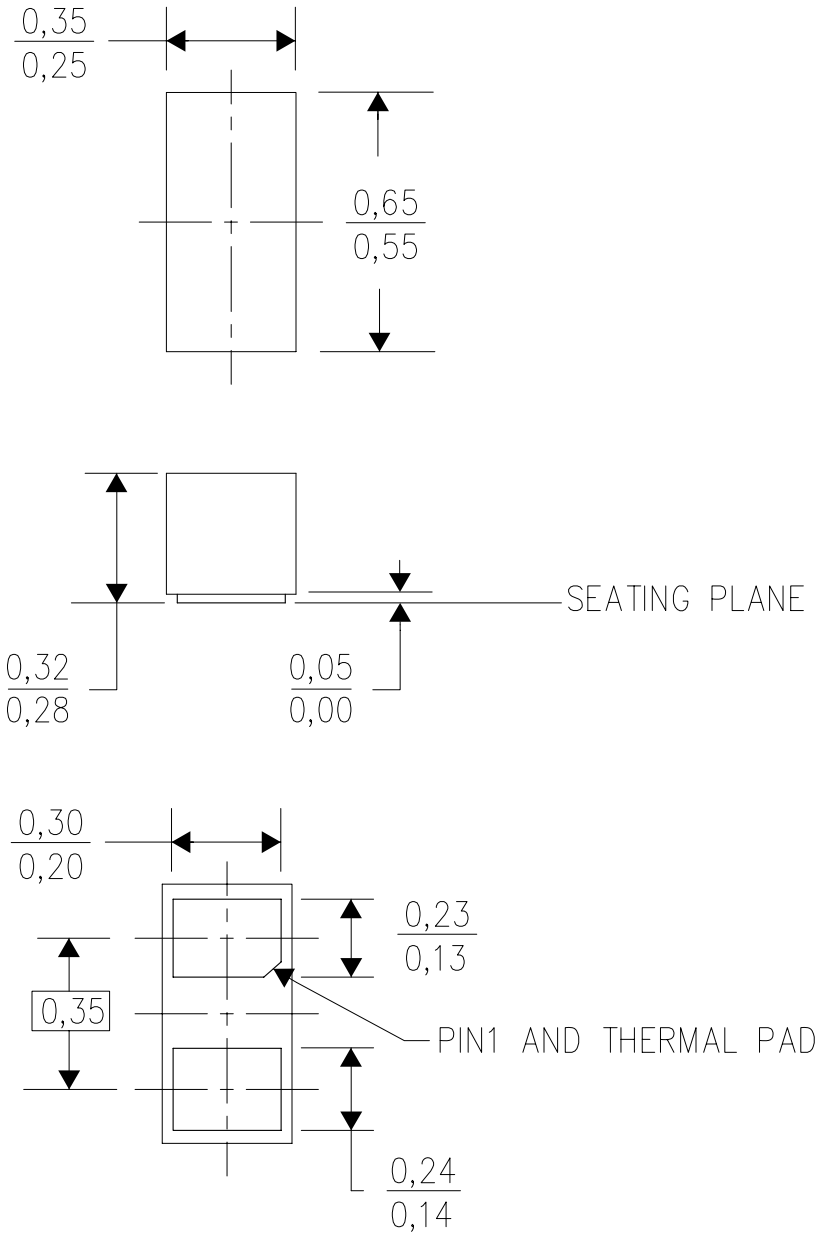
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

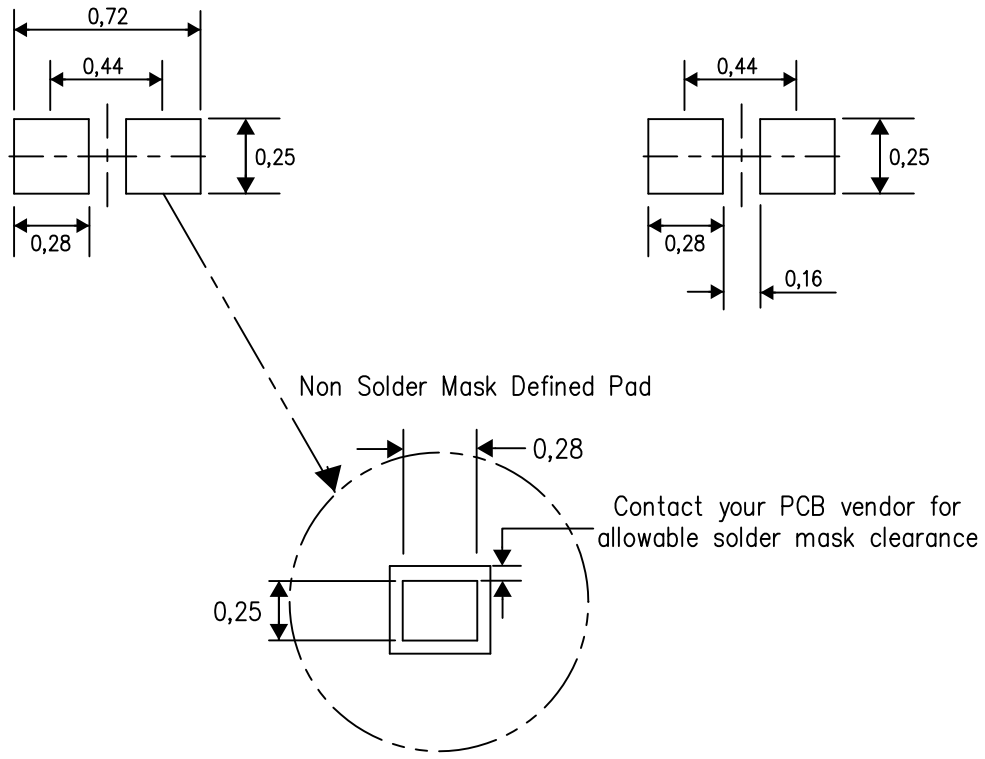


4212149/B 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

DPL (R–PX2SON–N2) SMALL PACKAGE OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)

4217903/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265