TPD4E004 用于高速数据接口的 4 通道 ESD 保护阵列

1 特性

- IEC 61000-4-2 ESD 保护：
  - ±8kV IEC 61000-4-2 接触放电
  - ±12-kV IEC 61000-4-2 空隙放电
- ANSI/ESDA/JEDEC JS-001：
  - ±15kV 人体放电模型 (HBM)
- 1.6pF 低输入电容
- 0.9V 至 5.5V 电源电压范围
- 4 通道器件
- 节省空间的 SON (DRY) 封装

2 应用

- USB
- 以太网
- FireWire™
- 视频
- 手机
- SVGA 视频连接
- 血糖仪

3 说明

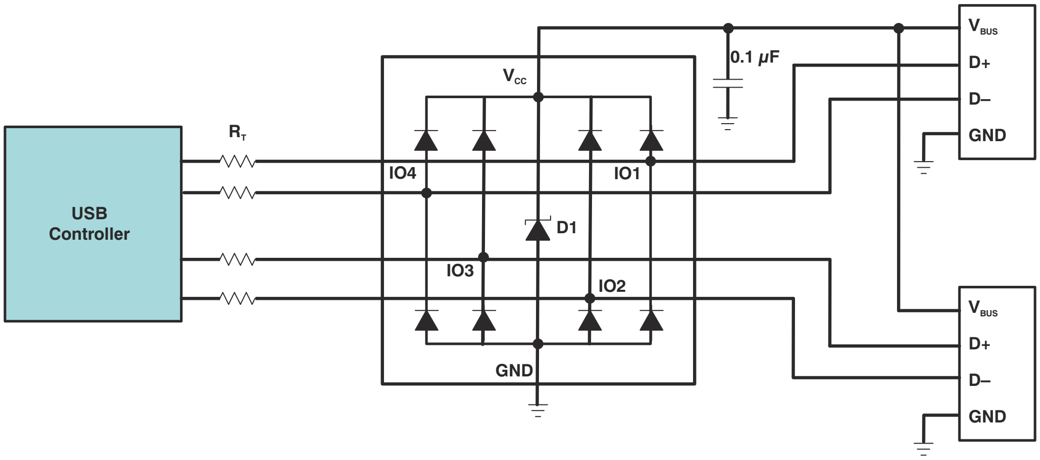
TPD4E004 是一款低电容瞬态电压抑制 (TVS) 器件。TPD4E004 旨在保护连接到通信线路的敏感电子元件免受静电放电 (ESD) 的影响。四个通道中的每一个通道都包含一对二极管，用于将 ESD 电流脉冲引导至 V_{CC} 或 GND。TPD4E004 可为高达 ±15kV 的人体放电模型 (HBM) ESD 脉冲（在 IEC 61000-4-2 中指定）提供保护，并提供 ±8kV 接触放电和 ±12kV 空气间隙放电。该器件每通道具有 1.6pF 电容，因此非常适合用在高速数据 IO 接口中。

TPD4E004 是专为 USB、以太网™和其他高速应用而设计的四路 ESD 结构。

封装信息

器件型号	封装[1]	封装尺寸[2]
TPD4E004	DRY（SON，6）	1.45 mm × 1 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



应用原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (March 2016) to Revision C (July 2023) **Page**

- 更新了*封装信息* 表以包含封装尺寸............ 1
- 更新了整个文档中的表格、图和交叉参考的编号格式............ 1
- Updated the *Overview* section to include IEC 61000-4-2 international standard Level 3............ 7

Changes from Revision A (February 2008) to Revision B (March 2016) **Page**

- 添加了*器件信息* 表、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械* 、*封装和可订购信息* 部分............ 1
- 删除了订购信息............ 1

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5 Pin Configuration and Functions

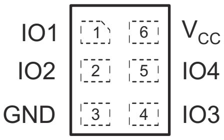


图 5-1. DRY Package, 6-Pin SON (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	**NO.**		
IO1	1	IO	ESD-protected channel
IO2	2	IO	ESD-protected channel
GND	3	GND	Ground
IO3	4	IO	ESD-protected channel
IO4	5	IO	ESD-protected channel
V_{CC}	6	PWR	Power-supply input

(1) I = input, O = outputs, GND = ground, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	5.5	V
V_{IO}	Input/output voltage		–0.3	V_{CC} + 0.3	V
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±15000	V
		IEC 61000-4-2	Contact Discharge	±8000	
			Air-Gap Discharge	±12000	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	85	°C
V_{CC}	Operating voltage for pin V_{CC}	0.9	5.5	V
V_{IO}	Operating voltage for pins IO1, IO2, IO3, and IO4	0	Minimum of: (5.8, V_{CC})	V

6.4 Thermal Information

THERMAL METRIC(1)		TPD4E004	UNIT
		DRY (SON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	414.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	258.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	251.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	70.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	248.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 0.9 V to 5.5 V, T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{CC}	Supply voltage		0.9		5.5	V
I_{CC}	Supply current				500	nA
V_F	Diode forward voltage	I_F = 1 mA		0.8		V
I_I	Channel leakage current			±1		nA
V_{BR}	Break-down voltage	I_I = 10 µA	6		8	V
$C_{I/O}$	Channel input capacitance	V_{CC} = 5 V, Bias of V_{CC}/2, f = 10 MHz		1.6	2	pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.

6.6 Typical Characteristics

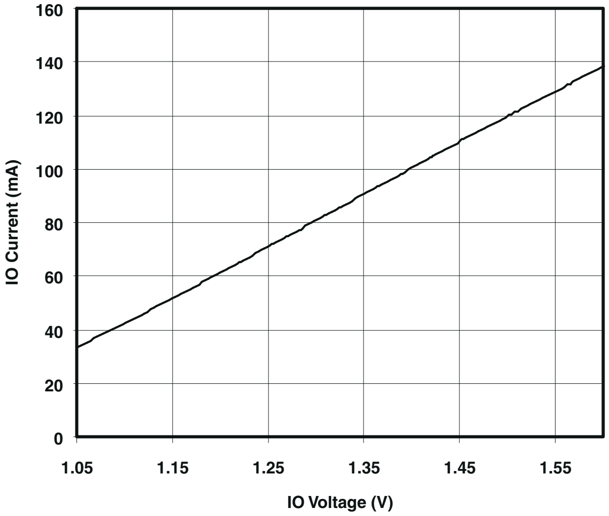


图 6-1. Forward Diode Voltage (Upper Clamp Diode) (V_{CC} = 0 V, DC Sweep Across the IO Pin)

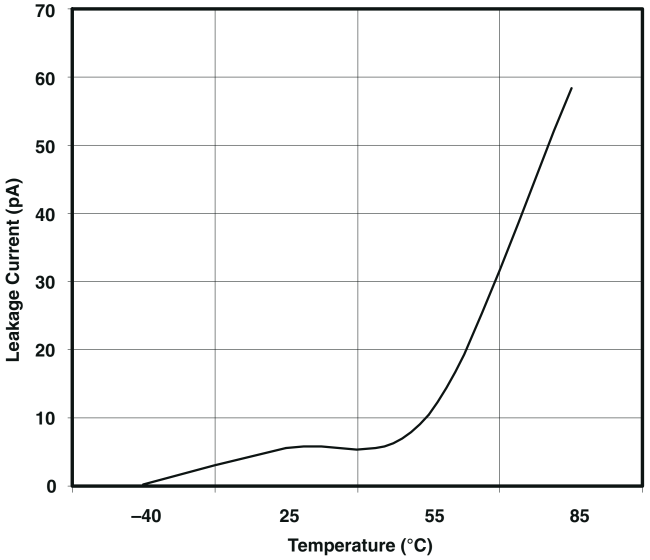


图 6-2. Leakage Current vs Temperature (V_{IO} = 2.5 V)

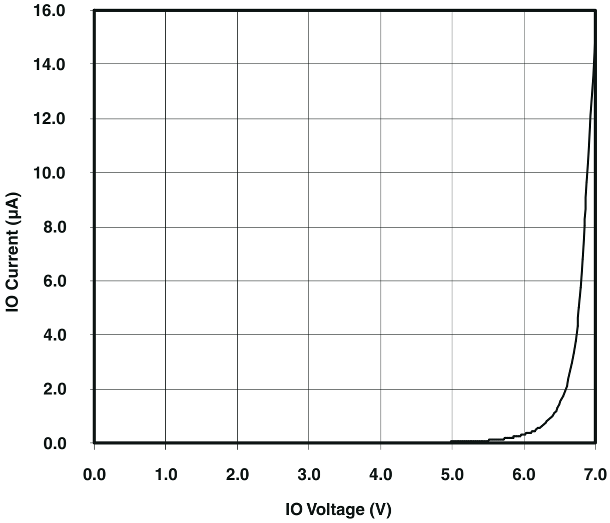


图 6-3. Reverse Diode Curve Current IO to GND (V_{CC} = Open)

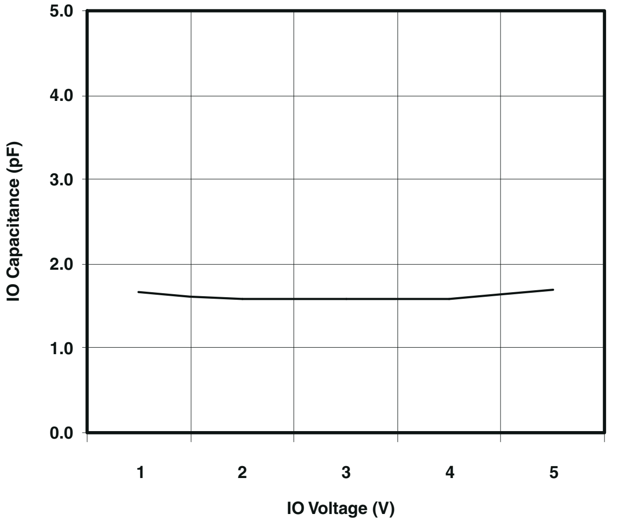


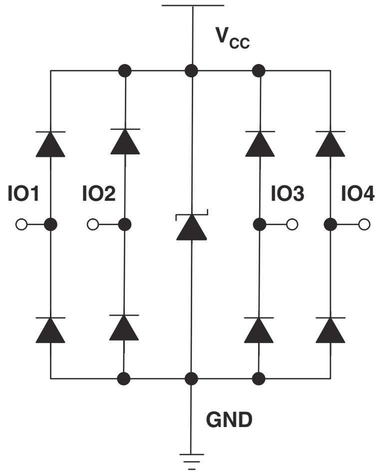
图 6-4. IO Capacitance vs Input Voltage (V_{CC} = 5 V)

7 Detailed Description

7.1 Overview

The TPD4E004 is a four-channel TVS protection diode array. The TPD4E004 is rated to dissipate contact ESD strikes of ±8-kV contact and ±12-kV air-gap, meeting Level 3 as specified in the IEC 61000-4-2 international standard. This device has a 1.6-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces.

7.2 Functional Block Diagram



7.3 Feature Description

TPD4E004 is a TVS which provides ESD protection for up to four channels, withstanding up to ±8-kV contact and ±12-kV air-gap ESD per IEC 61000-4-2. The monolithic technology yields exceptionally small variations in capacitance between any IO pin of TPD4E004. The small footprint is ideal for applications where space-saving designs are important.

7.4 Device Functional Modes

The TPD4E004 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the diodes V_F of approximately –0.3 V. During ESD events, voltages as high as ±8-kV contact and ±12-kV air-gap ESD can be directed to ground through the internal diodes. Once the voltages on the protected line fall below the trigger levels of TPD4E004 (usually within 10’s of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

TPD4E004 is a diode array type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level for the protected IC.

8.2 Typical Application

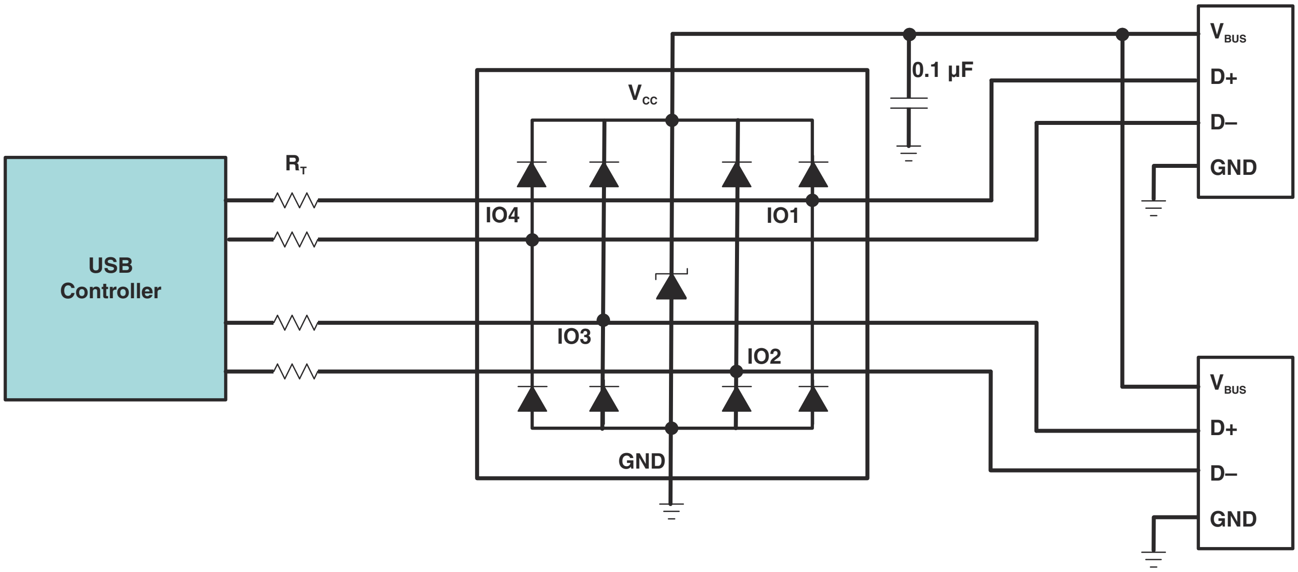


图 8-1. Application Schematic

8.2.1 Design Requirements

For this design example, a single TPD4E004 is used to protect all the pins of two USB2.0 connectors. 表 8-1 lists the design parameters for the USB application.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, and IO4	0 V to 3.6 V
Signal voltage range on V_{CC}	0 V to 5.5 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD4E004 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD4E004 is designed so that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, see the following layout and design guidelines should be followed:

1. Place the TPD4E004 solution close to the connectors. This allows the TPD4E004 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E004 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15-A to 30-A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. In this example of protecting two USB ports, none of the IO pins will be left unused.
5. The V_{CC} pin can be connected in two different ways:
    a. If the V_{CC} pin is connected to the system power supply, the TPD4E004 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-µF capacitor on the device V_{CC} pin is recommended for ESD bypass.
    b. If the V_{CC} pin is not connected to the system power supply, the TPD4E004 can tolerate higher signal swing in the range up to 5.8 V. Please note that a 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.3 Application Curves

图 8-2 is a capture of the voltage clamping waveform of TPD4E004 during an +8-kV Contact IEC 61000-4-2 ESD strike.

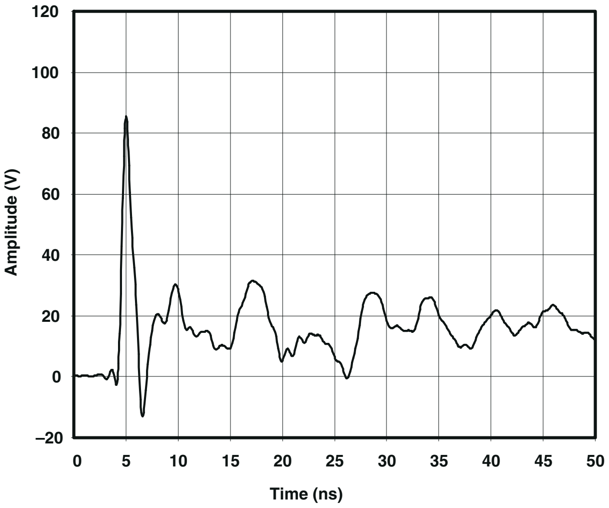


图 8-2. IEC ESD Clamping Waveforms +8-kV Contact

9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Make sure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

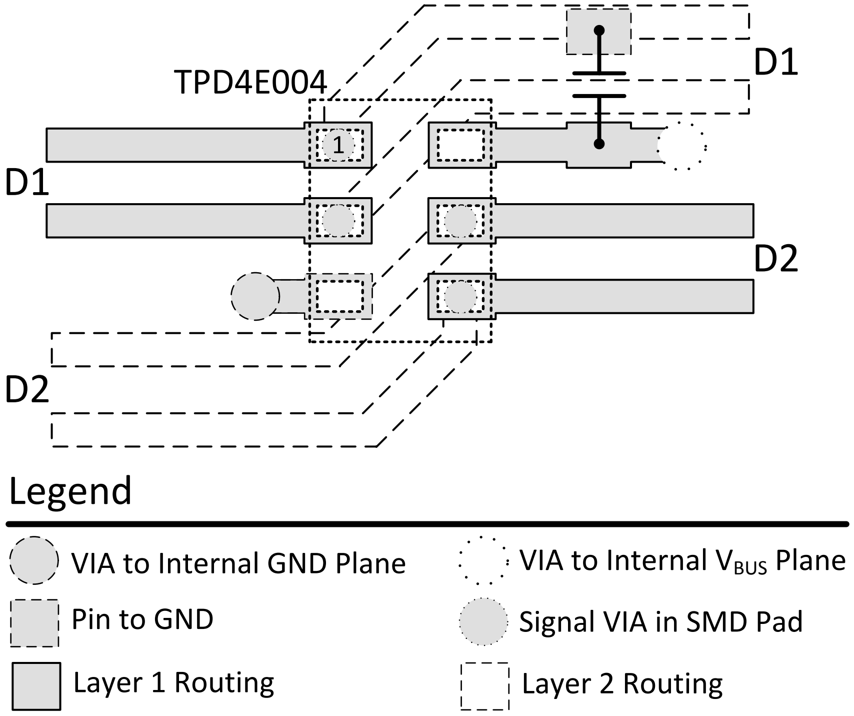


图 **10-1. TPD4E004 Layout Example**

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet*
- Texas Instruments, *ESD Protection Layout Guide*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

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以太网™ is a trademark of Xerox Corporation.
TI E2E™ is a trademark of Texas Instruments.
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11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E004DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P	Samples
TPD4E004DRYRG4	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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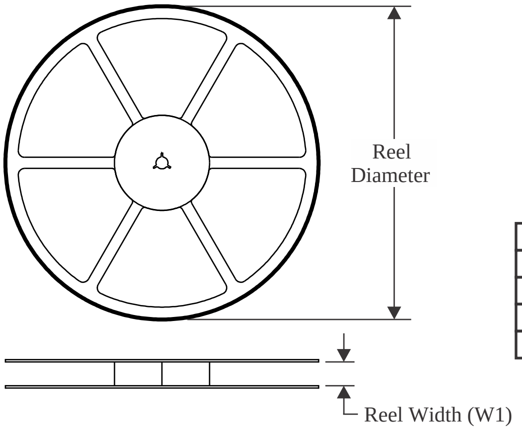
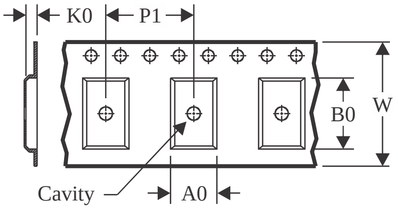
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

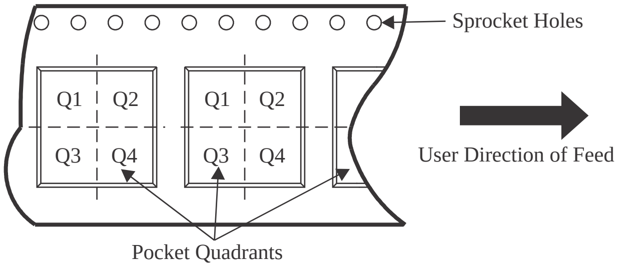


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

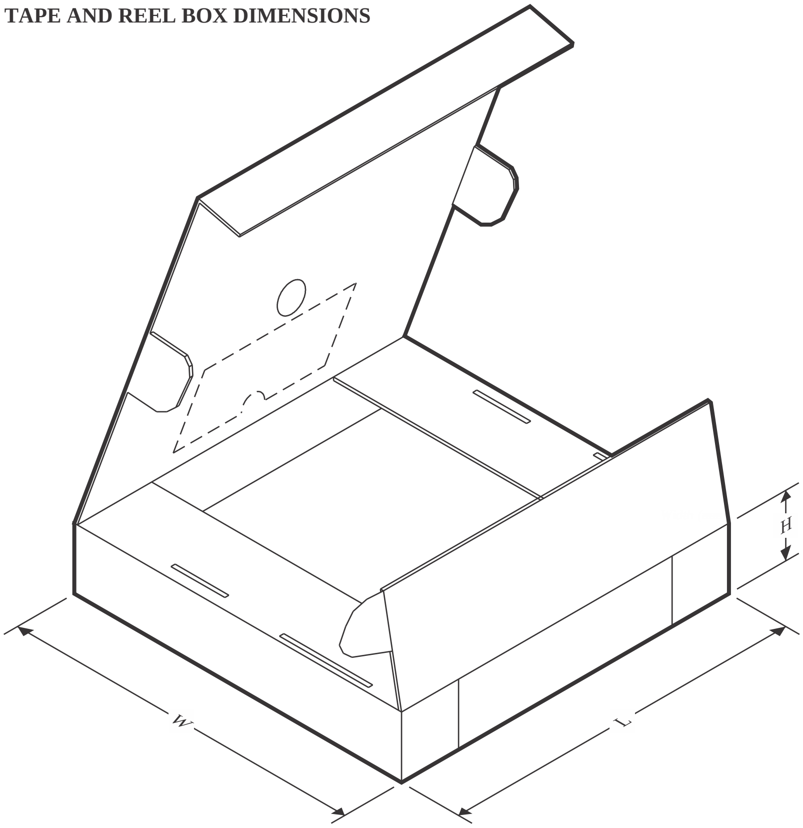
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E004DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



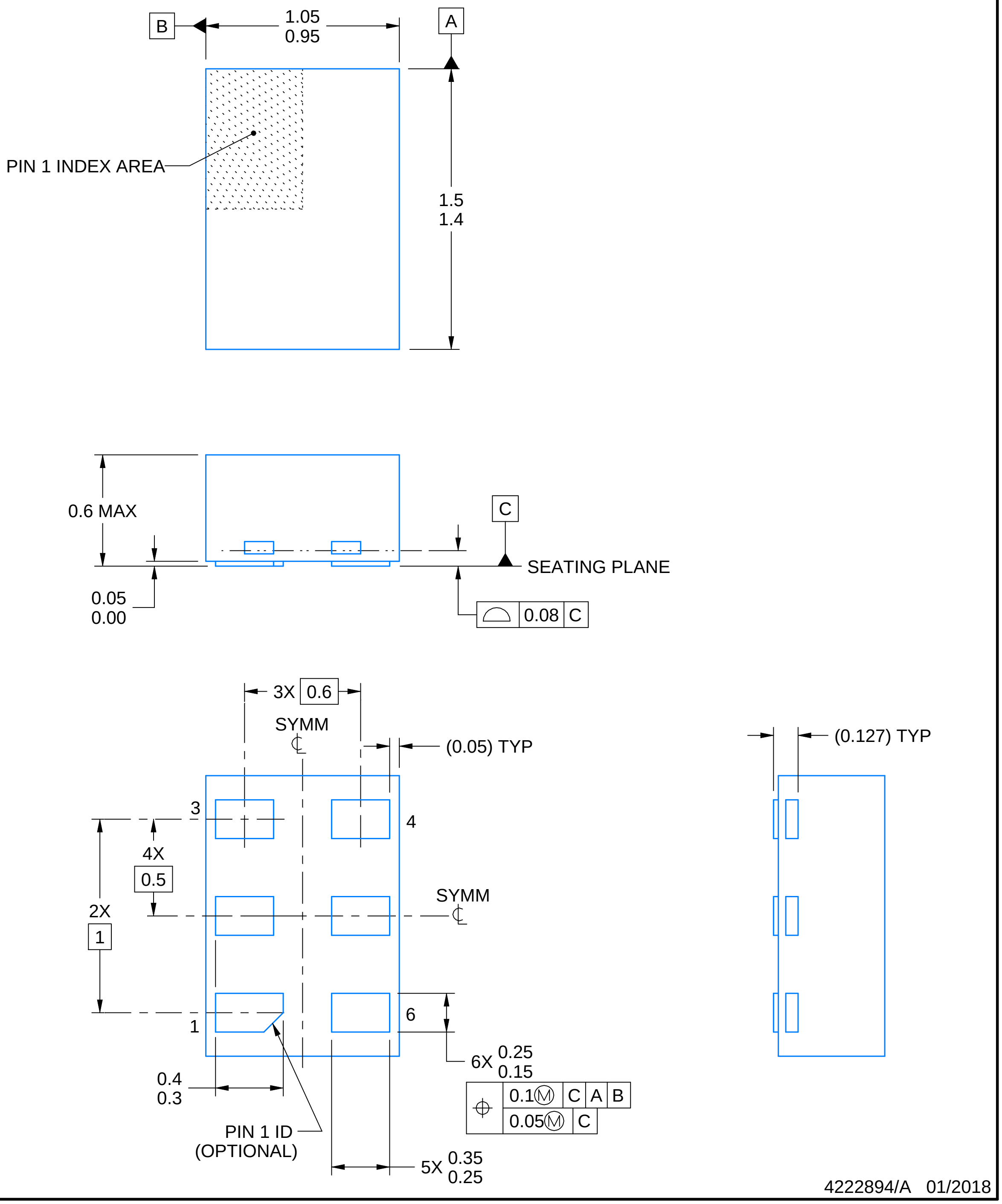
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E004DRYR	SON	DRY	6	5000	189.0	185.0	36.0

DRY 6 USON - 0.6 mm max height

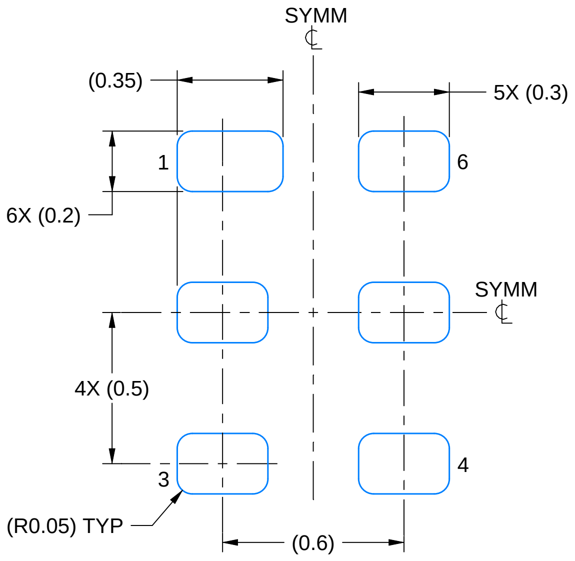
PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

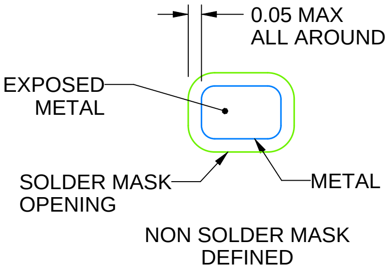


NOTES:

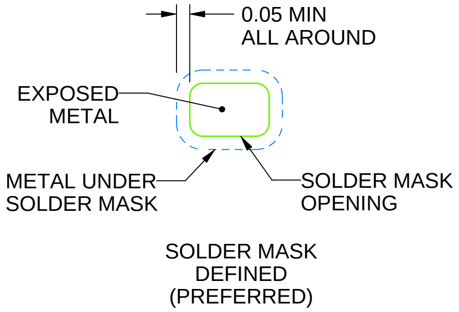
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



NON SOLDER MASK
DEFINED



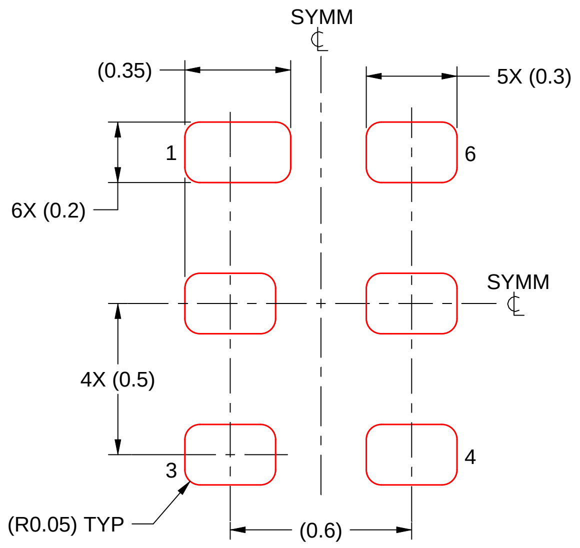
SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265