

## TPD4E110 4 通道保护解决方案，用于超高速（高达 6GBPS）接口

### 1 特性

- 为低压输入输出 (IO) 接口提供系统级静电放电 (ESD) 保护
- IO 电容值 0.45pF (典型值)
- IEC 61000-4-2 4 级
  - $\pm 12\text{kV}$  (接触放电)
  - $\pm 15\text{kV}$  (空气间隙放电)
- IEC 61000-4-5 (浪涌) : 2.5A (8/20 $\mu\text{s}$ )
- 直流击穿电压 6.5V (最小值)
- 超低泄露电流 1nA (最大值)
- 低 ESD 钳位电压
- 工业温度范围:  $-40^{\circ}\text{C}$  至  $125^{\circ}\text{C}$
- 最大限度减少空间的 0.8mm x 0.8mm DPW 封装

### 2 应用范围

- USB 3.0
- HDMI 2.0
- 低压差分信令 (LVDS)
- DisplayPort
- PCI Express 接口
- eSata 接口

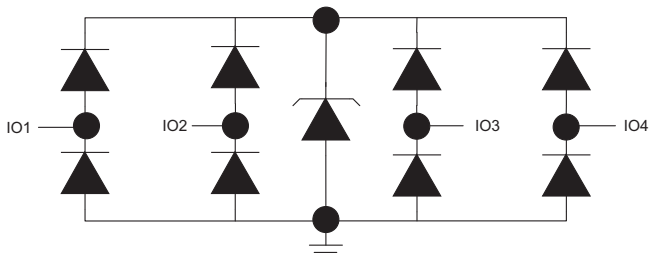
### 3 说明

TPD4E110 是一款具有超低电容值的单向静电放电 (ESD) 保护器件。此器件由一个中央 ESD 钳位组成，并且在每个通道中特有两个隐藏的二极管，以减少电容负载。每条通道额定 ESD 冲击消散值高于 IEC61000-4-2 4 级国际标准中规定的最高水平。TPD4E110 的超低负载电容值使得此器件非常适合于保护高速信号引脚。

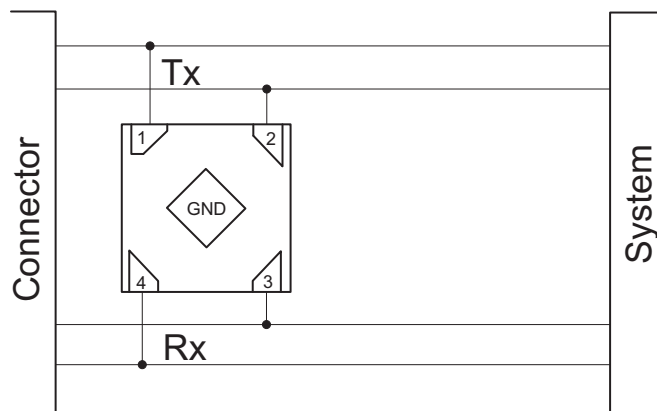
#### 器件信息

订货编号	封装	封装尺寸
TPD4E110DPW	X2SON (4)	0.8mm x 0.8mm

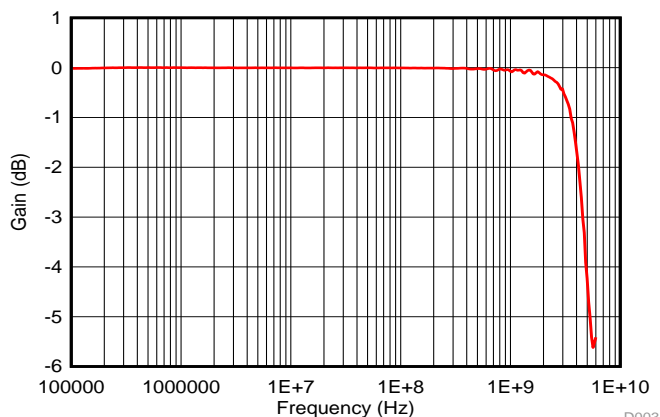
电路保护系统



### 4 简化电路原理图



插入损耗



D003



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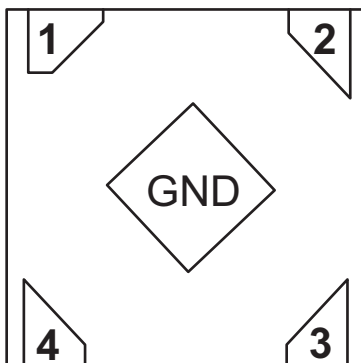
## 5 修订历史记录

<b>Changes from Revision A (March 2014) to Revision B</b>	<b>Page</b>
• 已修改超低泄露电流排印错误。 .....	<b>1</b>
• Updated $I_{LEAK}$ max value. ....	<b>4</b>

<b>Changes from Original (July 2013) to Revision A</b>	<b>Page</b>
• 已将首页数据表更新为完全版。 .....	<b>1</b>

## 6 Terminal Configuration and Functions

4 Terminal DPW Package  
Bottom View



Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
IOX	1, 2, 3, 4	IO	ESD-protected channel
GND	5	G	Ground

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Operating temperature range	-40	125	°C
$I_{PP}$	Peak pulse current ( $t_p = 8/20\mu s$ )		2.5	A
$P_{PP}(\text{forward})$	Peak pulse power ( $t_p = 8/20\mu s$ )		35	W
$P_{PP}(\text{reverse})$	Peak pulse power ( $t_p = 8/20\mu s$ )		18	W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 Handling Ratings

		MIN	MAX	UNIT
$T_{stg}$	Storage temperature	-65	155	°C
ESD <sup>(1)</sup>	IEC 61000-4-2 contact ESD		±12	kV
	IEC 61000-4-2 air-gap ESD		±15	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{IO}$		0.0	5.5	V
$T_A$	Operating free-air temperature	-40	125	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD4E110	UNIT
		DPW (4 TERMINALS)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	291.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	224.2	
R <sub>θJB</sub>	Junction-to-board thermal resistance	245.8	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	31.4	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	245.6	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	195.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V <sub>RWM</sub>	Reverse stand-off voltage	I <sub>IO</sub> = 10 μA			5.5	V
V <sub>CLAMP</sub>	Clamp voltage with ESD strike	I = 1A, TLP, I/O to GND		10		V
		I = 5A, TLP, I/O to GND		13		V
		I = 1A, TLP, GND to I/O		3		V
		I = 5A, TLP, GND to I/O		6		V
V <sub>BR</sub>	Break-down voltage	I <sub>IO</sub> = 1mA	6.5	7.5	8.5	V
I <sub>LEAK</sub>	Leakage current	V <sub>IO</sub> = 2.5V		0.02	1	nA
R <sub>DYN</sub>	Dynamic resistance	Any I/O to GND Terminal <sup>(1)</sup>		0.8		Ω
		GND to any I/O Terminal <sup>(1)</sup>		0.7		Ω
C <sub>L</sub>	Line capacitance	V <sub>IO</sub> = 2.5V, f = 1MHz, I/O to GND		0.45	0.55	pF
C <sub>CROSS</sub>	Channel to channel input capacitance	GND Terminal = 0V, f = 1MHz, V <sub>BIAS</sub> = 2.5 V, between channel terminals		0.003		pF
ΔC <sub>IO-TO-GND</sub>	Variation of channel input capacitance	GND Terminal = 0V, f = 1MHz, V <sub>BIAS</sub> = 2.5 V, Channel_x terminal to GND – Channel_y terminal to GND		0.05		pF

(1) Extraction of R<sub>DYN</sub> using least squares fit of TLP characteristics between I = 10A and I = 20A.

## 7.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ , unless otherwise noted

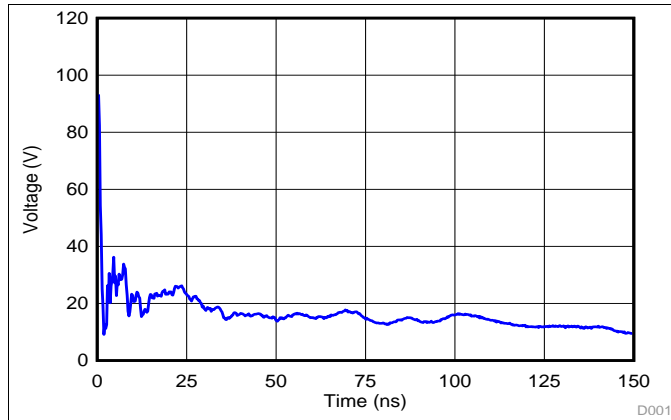


Figure 1. IEC 61000-4-2 Clamping Voltage, +8kV Contact

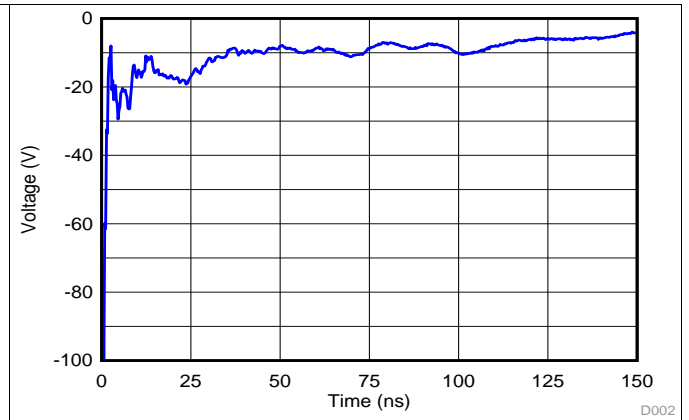


Figure 2. IEC 61000-4-2 Clamping Voltage, -8kV Contact

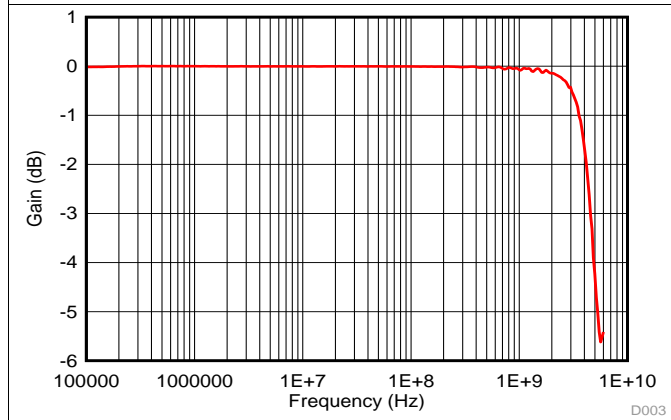


Figure 3. Insertion Loss

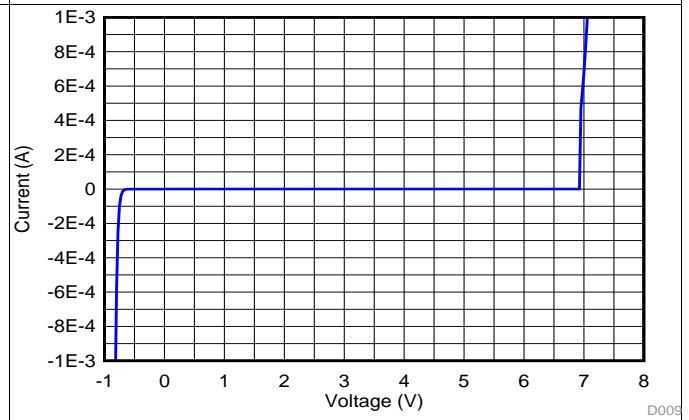


Figure 4. IV Curve

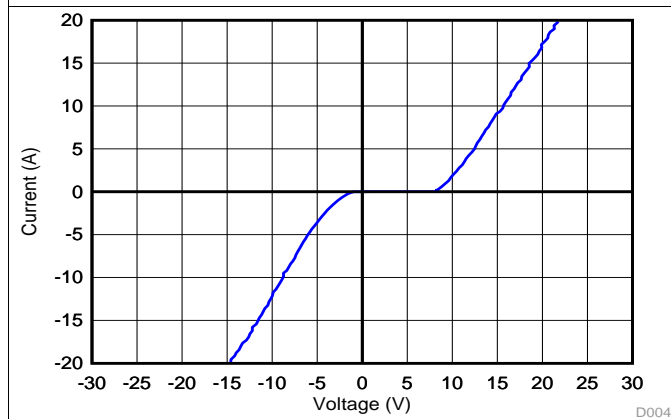


Figure 5. TLP,  $t_{PW} = 100 \text{ nS}$ ,  $t_{RISE} = 10 \text{ nS}$

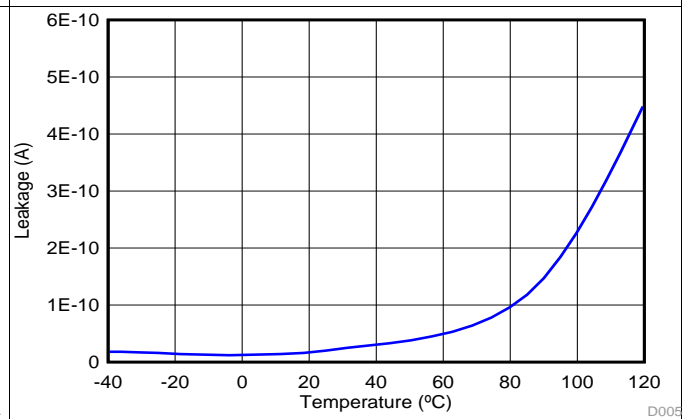
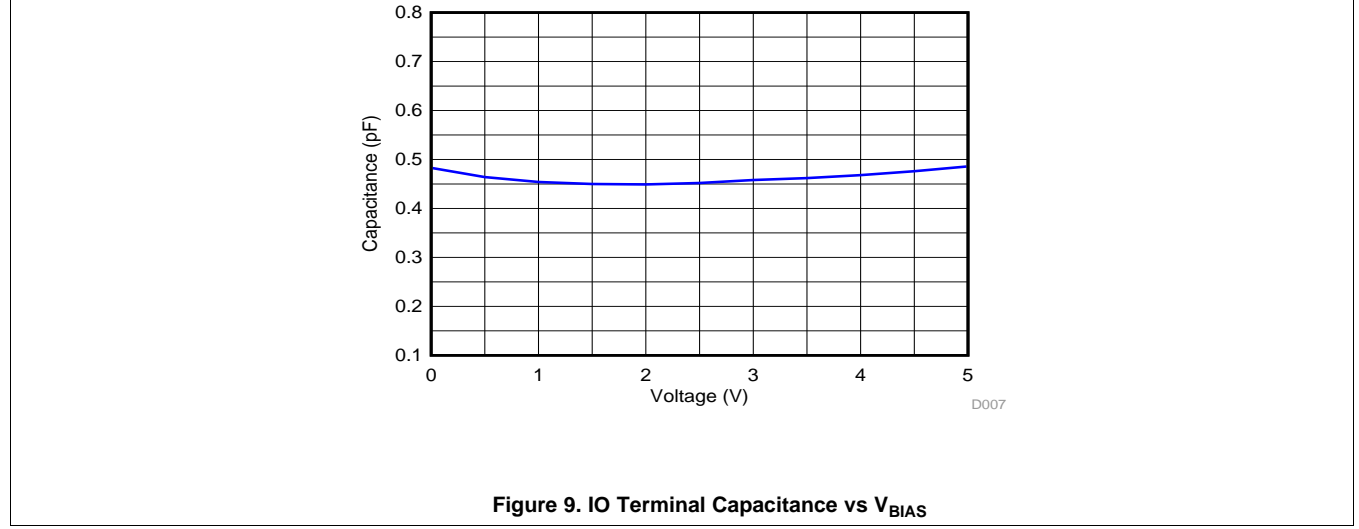
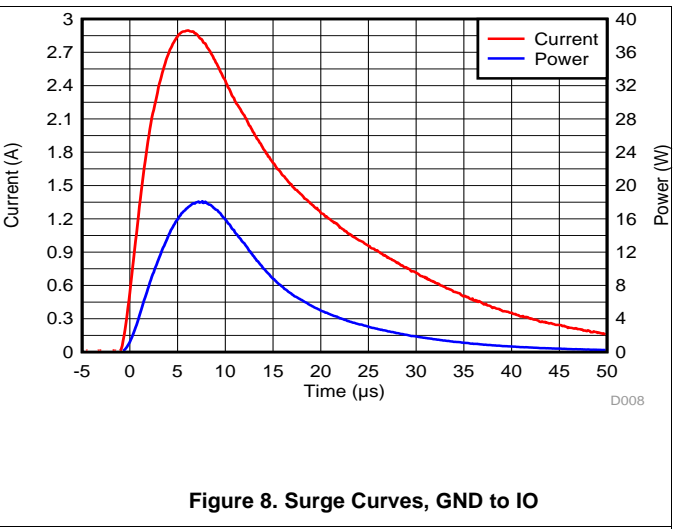
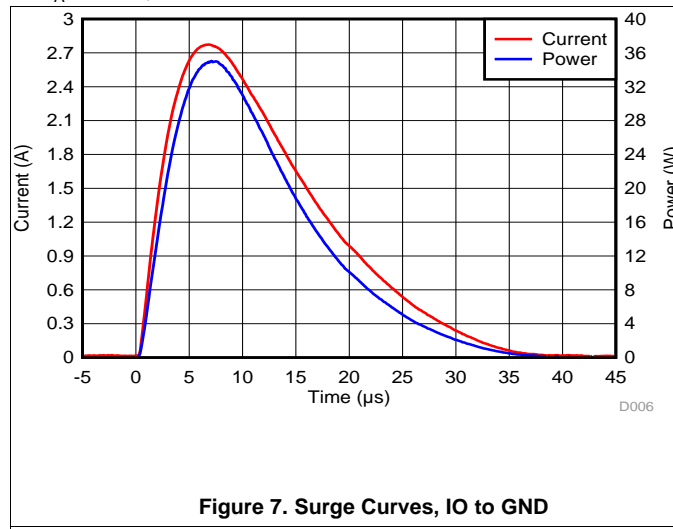


Figure 6. Leakage vs Temperature

**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ , unless otherwise noted

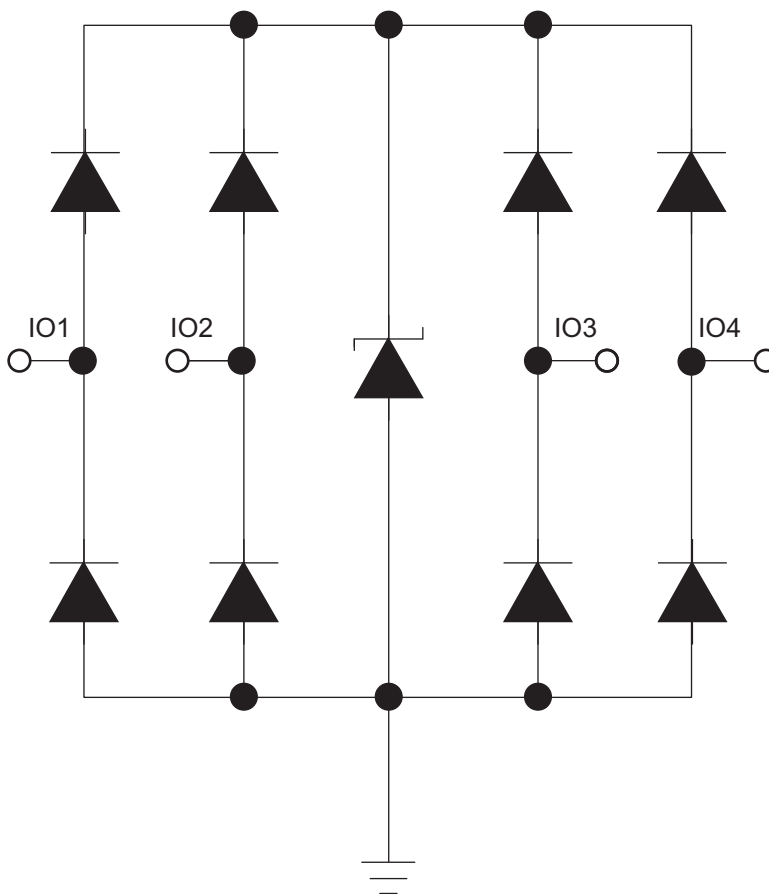


## 8 Detailed Description

### 8.1 Overview

TPD4E110DPW is a uni-directional ESD protection device with ultra-low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per channel to reduce the capacitive loading. Each channel is rated to dissipate ESD strikes above the maximum level specified in the IEC61000-4-2 level 4 international standard. The TPD4E110DPW's ultra-low loading capacitance makes the device ideal for protecting high-speed signal terminals. The 0.8 mm x 0.8 mm package is designed for space saving designs. The pinout allows for straight through routing of 2 differential pairs when PCB manufacturing which feature sizes of 2.8 mils (0.071 mm).

### 8.2 Functional Block Diagram



### 8.3 Feature Description

TPD4E110 is a uni-directional Electrostatic Discharge (ESD) protection device with ultra-low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. Each line is rated to dissipate ESD strikes above the maximum level specified in the IEC61000-4-2 level 4 international standard. The TPD4E110's ultra-low loading capacitance makes it ideal for protecting high-speed signal terminals.

### 8.4 Device Functional Modes

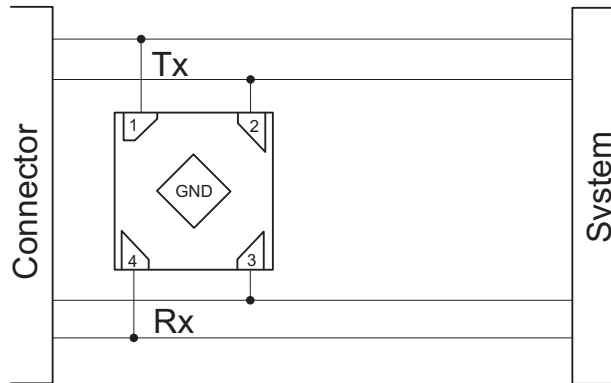
TPD4E110 is a passive integrated circuit that activates whenever voltages above  $V_{BR}$  or below the lower diodes  $V_{forward}$  ( $-0.6V$ ) are present upon the circuit being protected. During ESD events, voltages as high as  $\pm 15$  kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E110 (usually within 10's of nano-seconds) the device reverts to passive.

## 9 Applications and Implementation

### 9.1 Application Information

TPD4E110 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage,  $V_{CLAMP}$ , to a tolerable level to the protected IC.

### 9.2 Typical Application



**Figure 10. Protecting a Pair of Super-Speed Data Lines**

#### 9.2.1 Design Requirements

For this design example, use the following as the input parameters.

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on Pin 1, 2, 3, or 4	0V to 5.5V
Operating Frequency	3.0 GHz

#### 9.2.2 Detailed Design Procedure

To begin the design process some parameters must be decided upon. The designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

##### 9.2.2.1 Signal range on Terminal 1, 2, 3, or 4

TPD4E110 has 4 identical protection channels for signal lines. The symmetry of TPD4E110 provides flexibility when selecting which of the 4 IO channels will protect which signal lines. Any IO will support a signal range of 0V to 5.5V.

##### 9.2.2.2 Operating Frequency

The 0.45pF capacitance of each IO channel supports data rates up to 6Gbps.



### 9.2.3 Application Curves

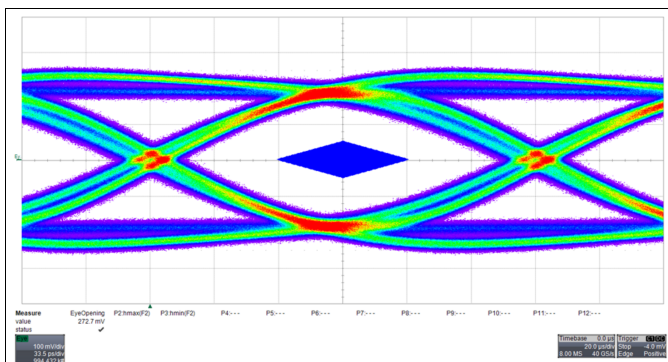


Figure 11. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Single Layer Routing with Device Installed

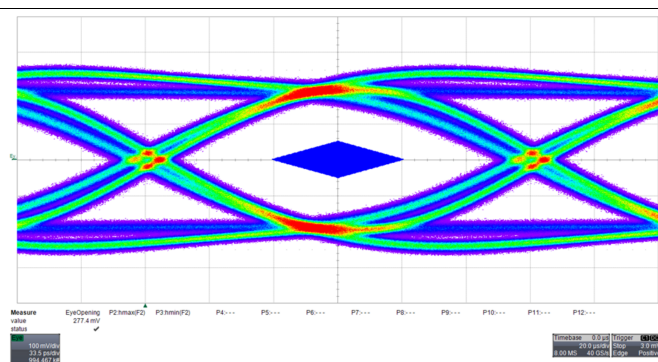


Figure 12. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Single Layer Routing without Device Installed

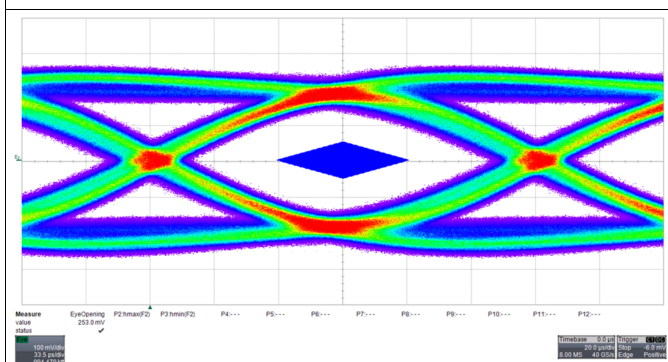


Figure 13. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Double Layer Routing with Device Installed

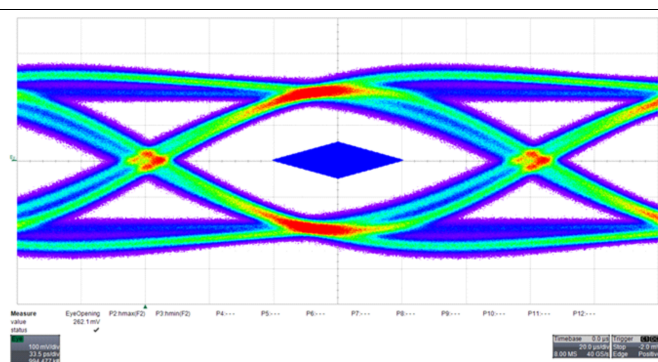


Figure 14. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Double Layer Routing with Device Installed

## 10 Layout

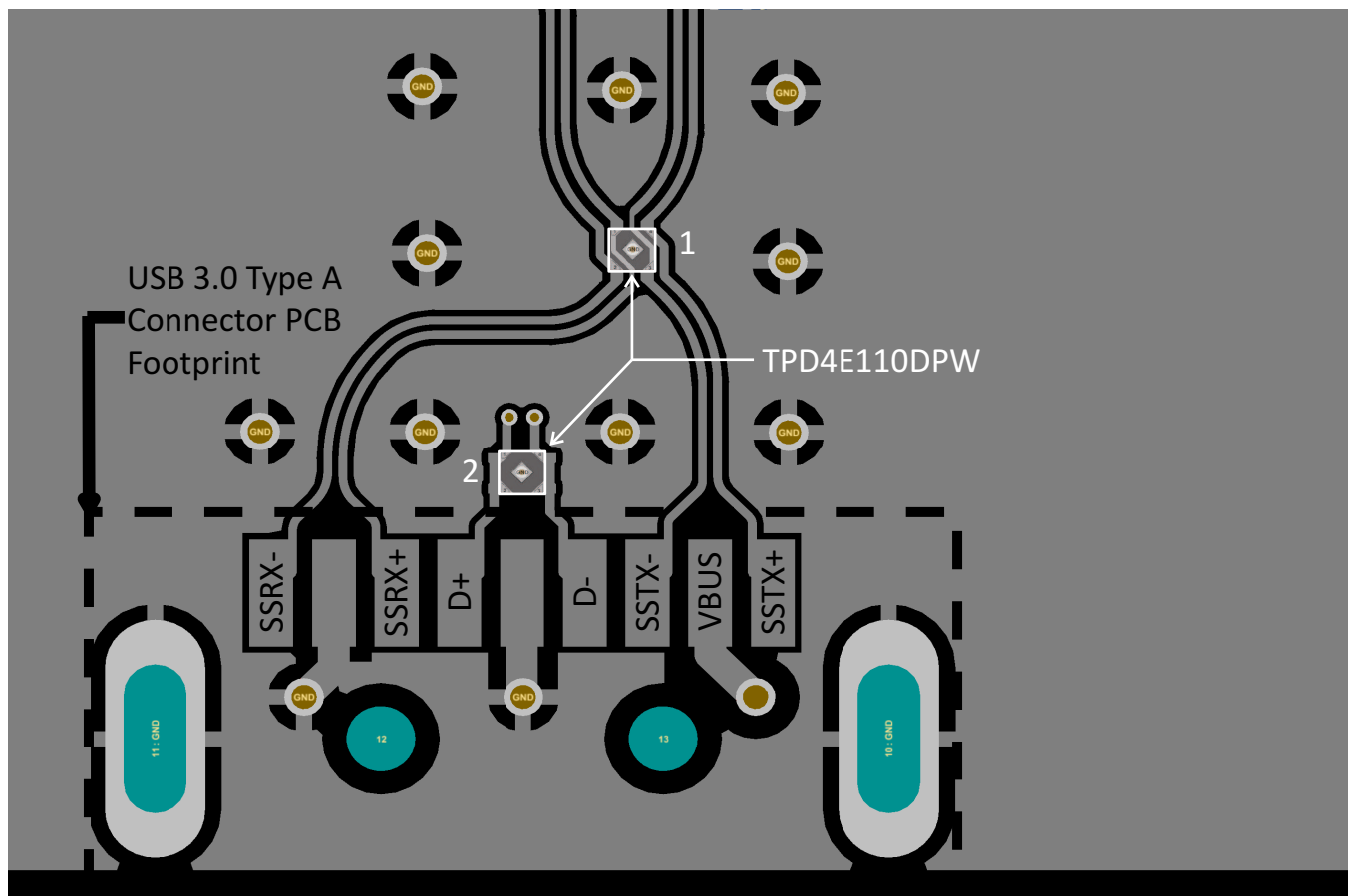
### 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 10.2 Layout Example

#### 10.2.1 Single Layer Routing

PCB manufacturing technologies allowing 2.8 mil (0.071 mm) clearances can route two Super-Speed data line pairs through TPD4E110 on a single layer.



**Figure 15. Example Layout for USB 3.0 Type A connector using two TPD4E110s**

In [Figure 15](#), [Figure 16](#) and [Figure 17](#) an example layout shows the use of two TPD4E110s to protect the USB 3.0 port. TPD4E110 Number 1 is protecting the two Super-Speed data pairs used for Super Speed data transfer, and TPD4E110 Number 2 protects the USB 2.0 D+/D– Hi-Speed data lines. Number 2 uses two channels to protect each line in the pair, thus affording a more robust protection and simpler layout.

Layout Example (continued)

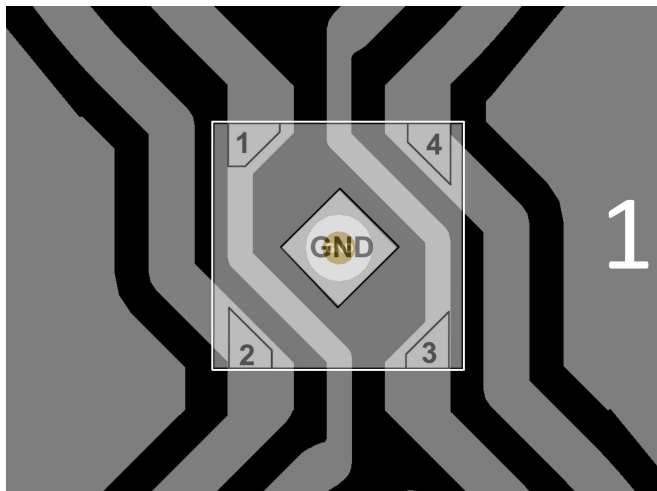


Figure 16. Close-up of Routing for TPD4E110 for Super-Speed Data Lines

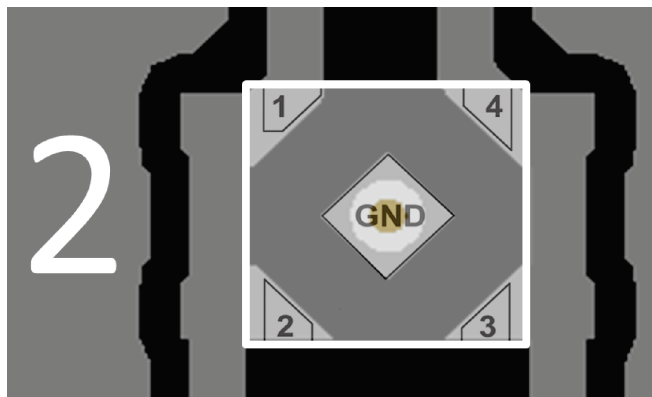


Figure 17. Close-up of Routing for TPD4E110 for USB 2.0 D+/D- Hi-Speed Data Lines

10.2.2 Double Layer Routing

PCB manufacturing technologies allowing 4.0 mil (0.1 mm) clearances can route two Super-Speed data line pairs through TPD4E110 using two layers.

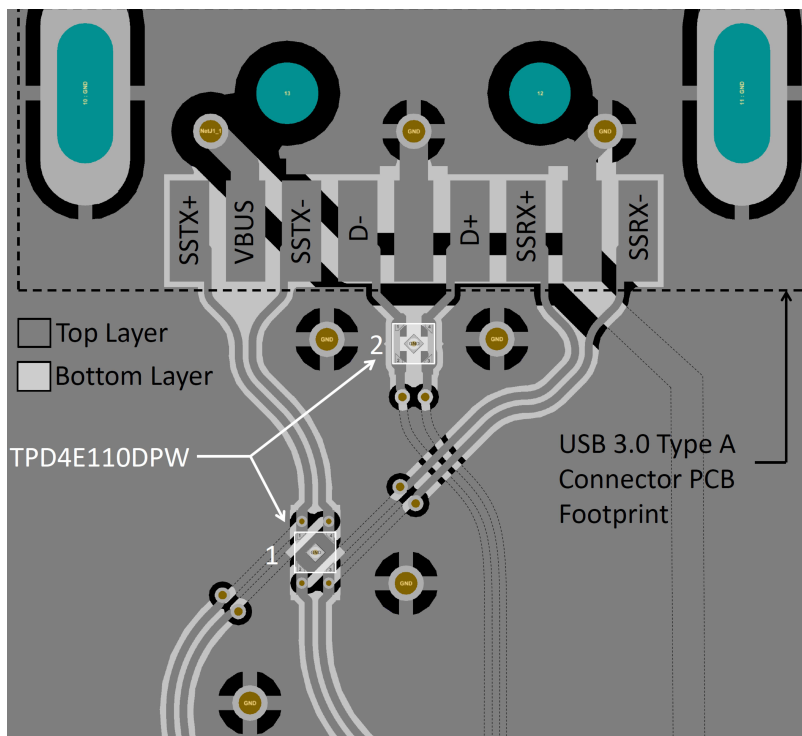


Figure 18. Example Layout for USB 3.0 Type A Connector Using Two TPD4E110s

In Figure 18 an example layout shows the use of two TPD4E110s to protect the USB 3.0 port. TPD4E110 Number 1 is protecting the two Super-Speed data pairs used for high speed data transfer, and TPD4E110 Number 2 protects the USB 2.0 D+/D- Hi-Speed lines. Number 2 uses two channels to protect each line in the pair, thus affording a more robust protection and simpler layout.

## 11 器件和文档支持

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122  
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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E110DPWR	ACTIVE	X2SON	DPW	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D2	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E110DPWR	X2SON	DPW	4	3000	180.0	9.5	0.91	0.91	0.5	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E110DPWR	X2SON	DPW	4	3000	184.0	184.0	19.0



## GENERIC PACKAGE VIEW

DPW 4

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-2/D

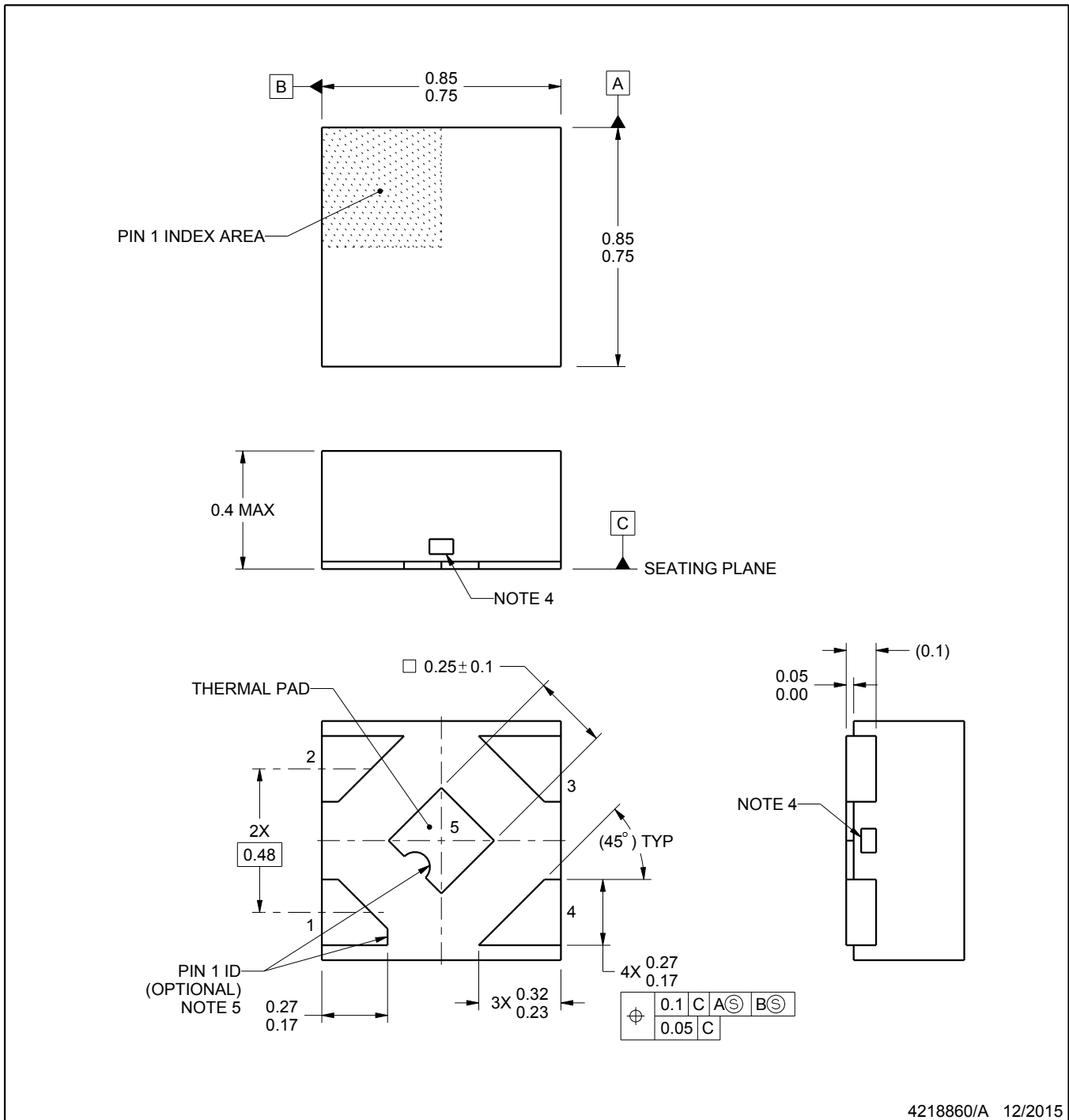


DPW0004A

# PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218860/A 12/2015

NOTES:

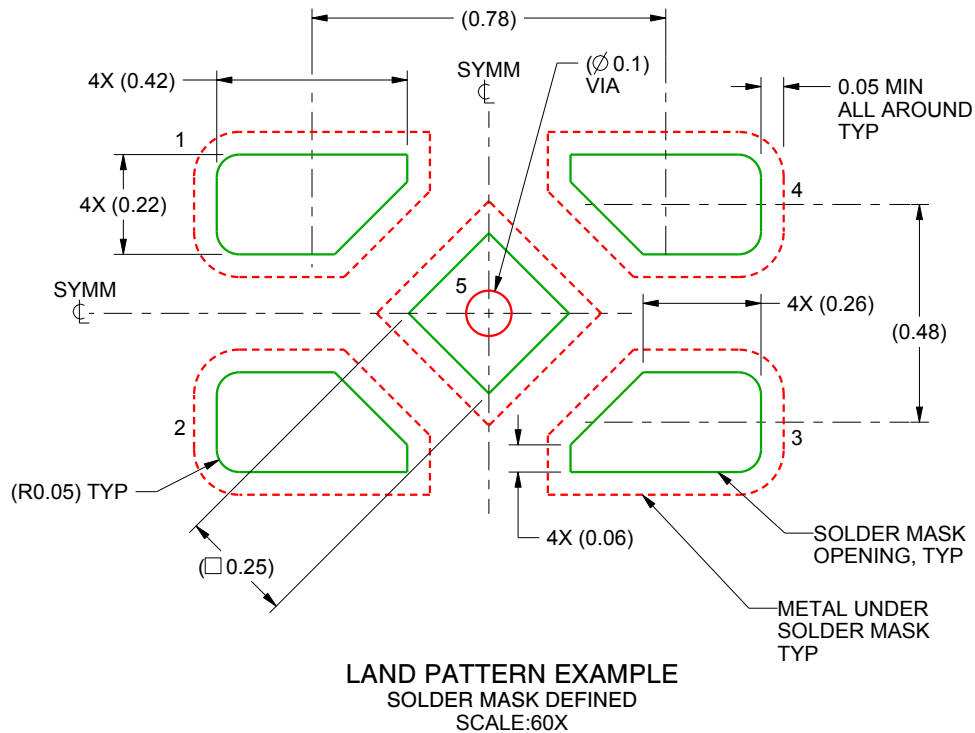
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

# EXAMPLE BOARD LAYOUT

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES: (continued)

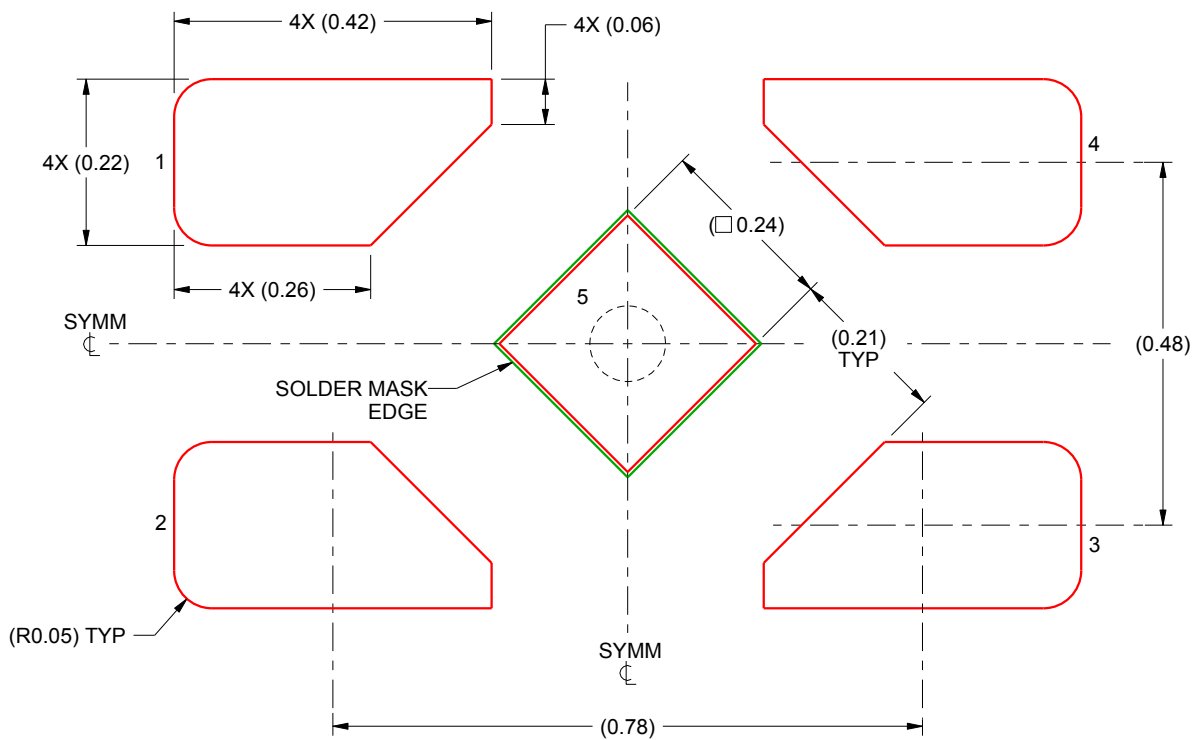
6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5:  
92% PRINTED SOLDER COVERAGE BY AREA  
SCALE:100X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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