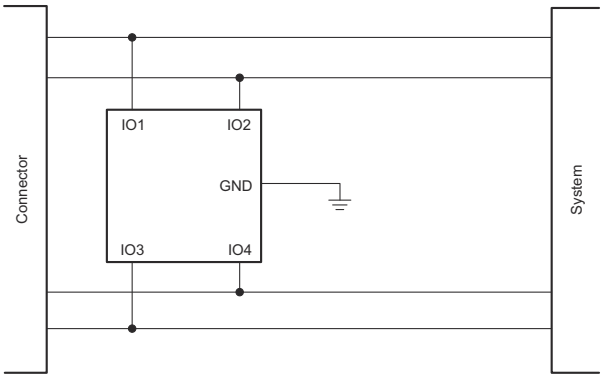
TPD4E1B06 4 通道超低泄漏 ESD 保护器件

1 特性

- 超低漏电流为 0.5nA（最大值）
- 针对 4 条 I/O 线路的瞬态保护：
  - IEC 61000-4-2 接触放电 ±12kV
  - IEC 61000-4-2 空气间隙放电 ±15kV
  - IEC 61000-4-5 浪涌 3.0A (8/20μs)
- I/O 电容 0.7pF（典型值）
- 双向 ESD 保护二极管阵列
- 低 ESD 钳位电压
- 工业级温度范围：-40°C 至 125°C
- 易于布线的小型 DRL 和 DCK 封装

2 应用

- 血糖仪
- 平板电脑
- GPS
- 便携式媒体播放器
- 电视
- 机顶盒



简化原理图

3 说明

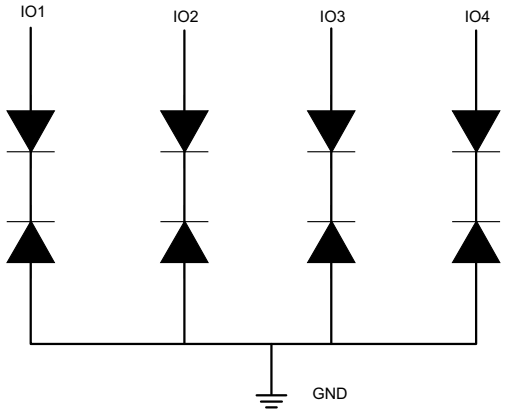
TPD4E1B06 是一款 4 通道双向静电放电 (ESD) 保护二极管阵列。这款器件具有超低漏电流 (0.5nA)，可实现精确模拟测量。±12kV 接触和 ±15kV 空气间隙 ESD 保护超过 IEC 61000-4-2 4 级要求。TPD4E1B06 器件的 0.7pF 线路电容值使其非常适合精密模拟、USB2.0、以太网、SATA、LVDS 和 1394 接口等应用。

封装信息

器件型号	封装(1)	封装尺寸(2)
TPD4E1B06	DCK（SC70，6）	2mm × 2.1mm
	DRL（SOT，6）	1.6mm × 1.6mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



功能方框图

Table of Contents

4 Pin Configuration and Functions

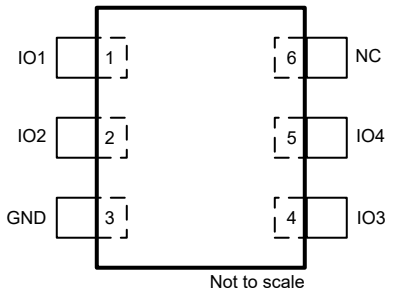


图 4-1. DCK Package, 6-Pin SC70 (Top View)

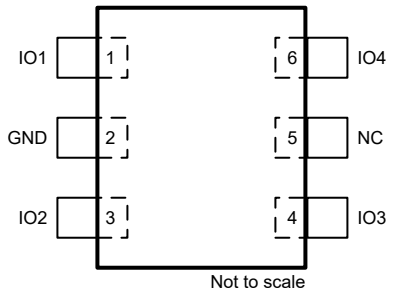


图 4-2. DRL Package, 6-Pin SOT (Top View)

表 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DCK	DRL		
IO1	1	1	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
IO2	2	3	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
IO3	4	4	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
IO4	5	6	I/O	ESD protected channel. Connect to data line as close to the connector as possible.
GND	3	2	GND	Ground
NC	6	5	NC	Not internally connected

(1) I = input, O = output, GND = ground, NC = no connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Operating temperature range	–40	125	°C
I_{PP}, peak pulse current (tp = 8/20 μs), IO pin to GND		3.0	A
P_{PP}, peak pulse power (tp = 8/20 μs)		45	W

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	155	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4.0	4.0	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1.5	1.5	
		IEC 61000-4-2 contact ESD	–12	12	
		IEC 61000-4-2 air-gap ESD	–15	15	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 4 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 1.5 kV may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	The voltage between any two device pins should not exceed 5.5 V	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPD4E1B06		UNIT
		DCK	DRL	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	233.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	95.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	68.1	
ψ_{JT}	Junction-to-top characterization parameter	3.6	7.6	
ψ_{JB}	Junction-to-board characterization parameter	70.4	67.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		–5.5		5.5	V
V_{CLAMP}	Clamp voltage with ESD strike, IO to GND	I_{PP} = 1 A, tp = 8/20 μSec, from I/O to GND or GND to I/O		10.9		V
		I_{PP} = 3 A, tp = 8/20 μSec, from I/O to GND or GND to I/O		14.5		V
R_{DYN}	Dynamic resistance	I_{TLP} = 10 A to 20 A, I/O to GND		1		Ω
		I_{TLP} = 10 A to 20 A, GND to I/O		0.8		Ω
C_L	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V		0.7	0.95	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA, from I/O to GND or GND to I/O	7		9.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V			0.5	nA

5.6 Typical Characteristics

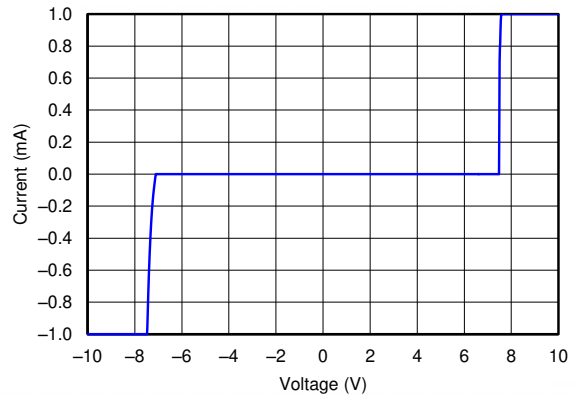


图 5-1. DC Voltage Sweep I-V Curve

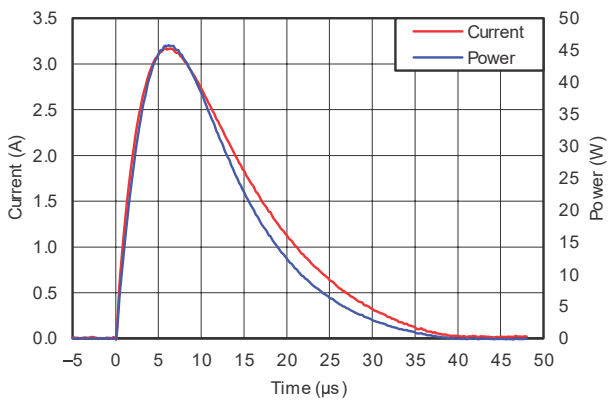


图 5-2. Surge Curve (tp = 8/20 µs), Pin IO to GND

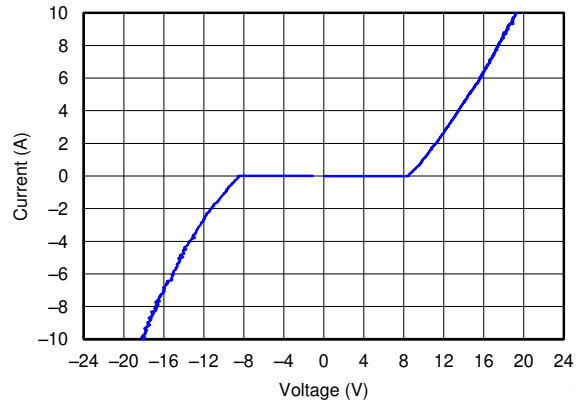


图 5-3. TLP Plot IO to GND

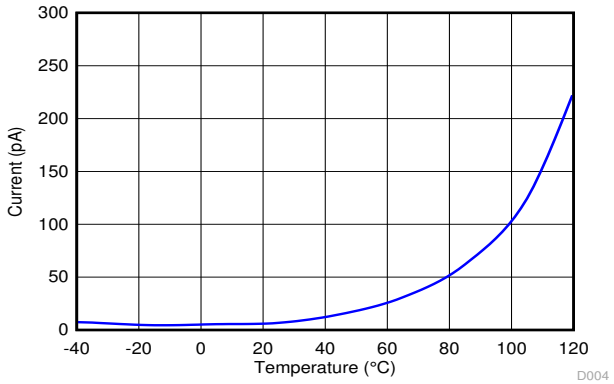


图 5-4. Leakage vs Temperature

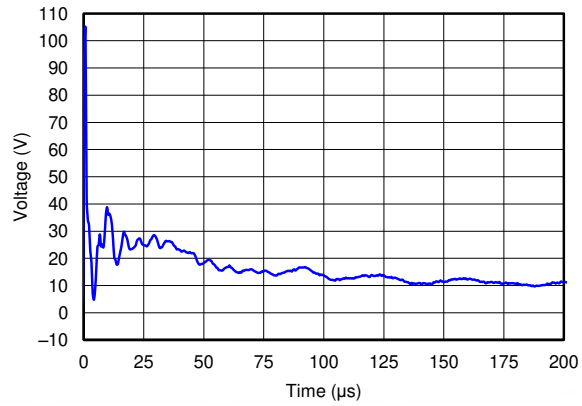


图 5-5. +8 kV IEC Waveform

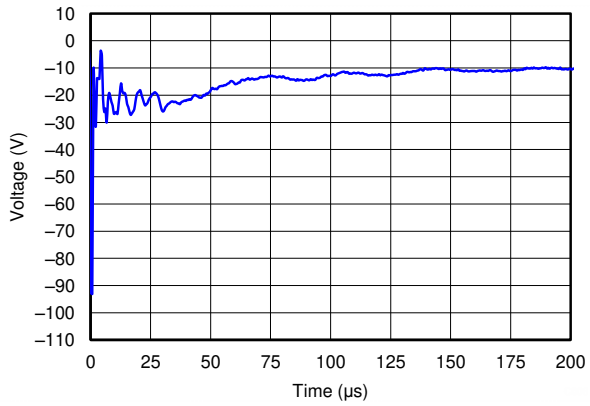


图 5-6. – 8 kV IEC Waveform

5.6 Typical Characteristics (continued)

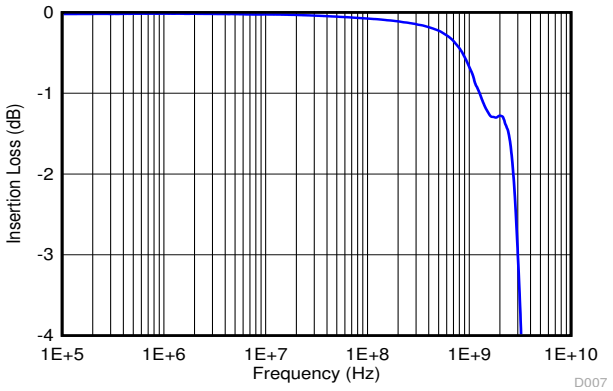


图 5-7. Insertion Loss

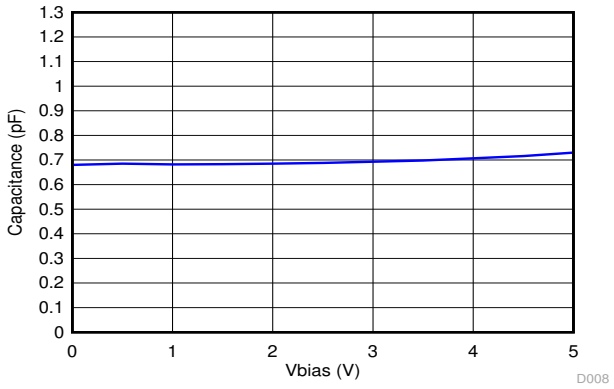


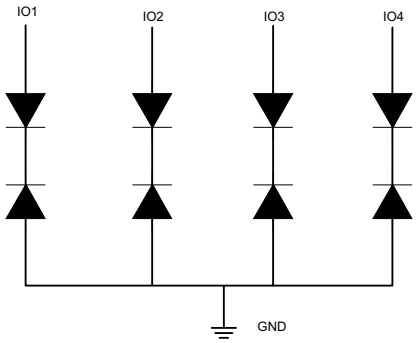
图 5-8. Capacitance vs V_{BIAS}

6 Detailed Description

6.1 Overview

The TPD4E1B06 is a 4-channel bi-directional Electrostatic Discharge (ESD) protection diode array. This device features ultra low leakage current (0.5 nA) for precision analog measurements. The ±12 kV contact and ±15 kV air gap ESD protection exceeds IEC 61000-4-2 level 4 requirements. The TPD4E1B06 0.7 pF line capacitance makes it suitable for precision analog, USB2.0, Ethernet, SATA, LVDS, and 1394 interfaces.

6.2 Functional Block Diagram



6.3 Feature Description

TPD4E1B06 diode array structure uses back-to-back diode topology to accommodate bi-directional signaling between –5.5 V and 5.5 V. Each pin has an additional 2 steering diodes, including the ground pin. The Zener diodes are not meant to be forward biased, creating the need for having the steering diodes. If there is +8 V on IO1 and 0V on IO2, the IO1 Zener diode will breakdown and forward bias one of the steering diodes on IO2. The current will then flow out of IO2.

6.3.1 Ultra Low Leakage Current 0.5 nA (Maximum)

TPD4E1B06 ultra-low leakage current supports long battery life and allows for precision analog measurements.

6.3.2 Transient Protection for 4 I/O Lines

The four I/O pins of TPD4E1B06 can withstand ESD events up to ±12 kV contact and ±15 kV air gap per IEC61000-4-2.

6.3.3 I/O Capacitance 0.7 pF (Typical)

TPD4E1B06 I/O pins present an ultra-low 0.7 pF capacitance to the protected signal lines, making it suitable for a wide range of applications.

6.3.4 Bi-Directional (ESD) Protection Diode Array

TPD4E1B06 diode array structure uses back to back diode topology to accommodate bi-directional signaling between –5.5 V and 5.5 V.

6.3.5 Low ESD Clamping Voltage

TPD4E1B06 clamps ESD events to a safe level to protect system components.

6.4 Device Functional Modes

TPD4E1B06 is a passive integrated circuit that activates whenever fast transient voltages above V_{BR} or below $-V_{BR}$ are present on the circuit being protected. During ESD events, voltages as high as ±12 kV can be directed to ground through the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1B06 (usually within 10’s of nano-seconds) the device reverts to passive.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

TPD4E1B06 is an ESD protection diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the diode, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered diode holds this voltage, V_{CLAMP}, to a safe level to the protected IC.

7.2 Typical Application

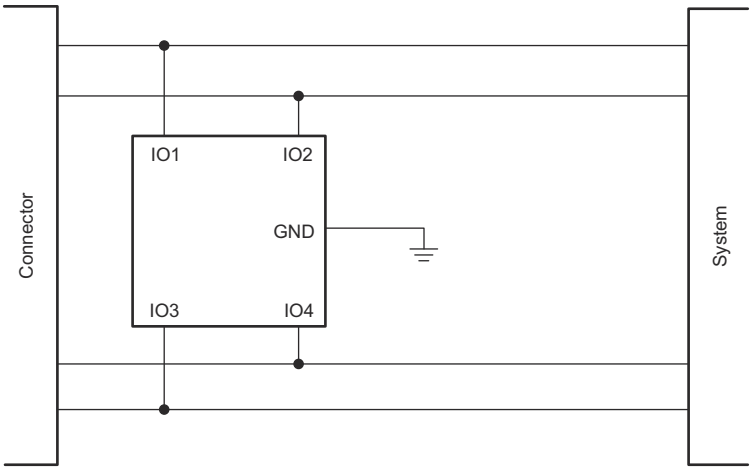


图 7-1. Protecting a Pair of Bi-Directional Differential Data Lines

The typical application of the TBD4E1B06 is to be placed in between the connector and the system. The low capacitance of the TBD4E1B06 gives flexibility in the end application, as it can be used on many different high speed interfaces.

7.2.1 Design Requirements

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on IO1, IO2, IO3, IO4 Pins	–5.5 V to 5.5 V
Operating frequency	1.7 GHz

7.2.2 Detailed Design Procedure

The designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

7.2.2.1 Signal Range on IO1, IO2, IO3, and IO4 Pins

TPD4E1B06 has 4 protection channels for signal lines. Any I/O will support a signal range of –5.5 V to 5.5 V.

7.2.2.2 Operating Frequency

The 0.7 pF capacitance of each I/O channel supports data rates up to 3.4 Gbps.

7.2.3 Application Curves

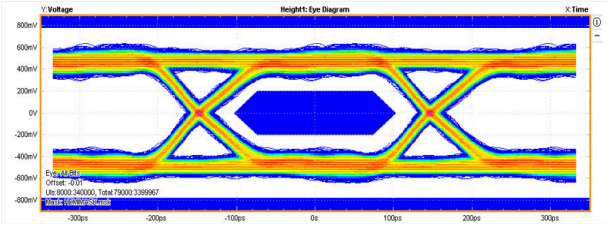


图 7-2. 3.4 Gbps HDMI 1.4 Eye Diagram in DCK Package

7.3 Layout

7.3.1 Layout Guidelines

- Place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer should minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the diode and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the diode and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

7.3.2 Layout Examples

图 7-3 shows a layout example for theTPD4E1B06DCK. Pins 1 and 2 and 4 and 5 are routed differentially. Pin 3 is routed to the ground plane. Pin 6 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 6 to the ground plane.

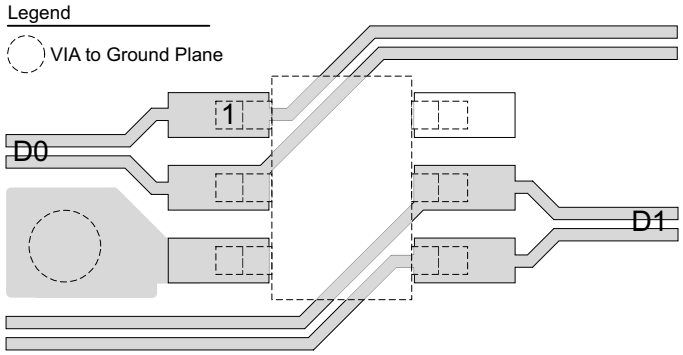


图 7-3. DCK Layout Example Showing Two Data Pairs, D0 and D1

图 7-4 shows a layout example for theTPD4E1B06DRL. Pins 1 and 6 and 3 and 4 are routed differentially. Pin 2 is routed to the ground plane. Pin 5 does not have an internal connection in the device and does not need to be routed anywhere on the board. It is also acceptable to connect pin 5 to the ground plane.

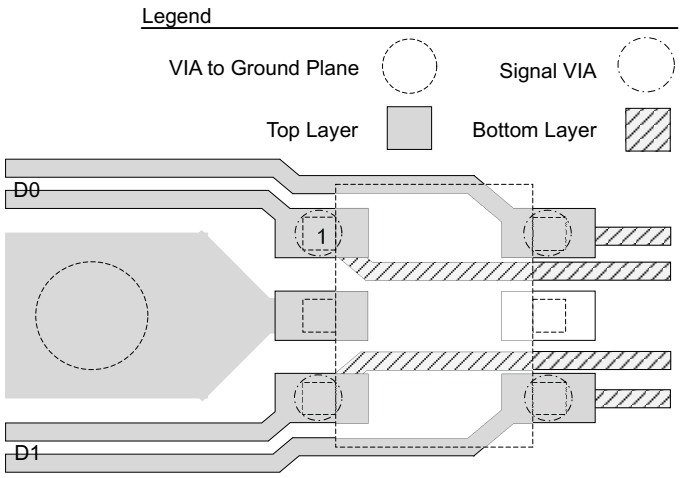


图 7-4. DRL Layout Example Showing Two Data Pairs, D0 and D1

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (October 2023) to Revision E (October 2024) **Page**

- Updated 图 4-1 3

Changes from Revision C (July 2014) to Revision D (October 2023) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式..... 1
- 更新了*封装信息* 表以包含封装引线尺寸..... 1
- Updated the *Feature Description* section..... 8
- Updated the *Bi-directional (ESD) Protection Diode Array* section..... 8

Changes from Revision B (May 2014) to Revision C (July 2014) **Page**

- Changed 2 device names from TPD4E6B06 to TPD4E1B06 9

Changes from Revision A (January 2013) to Revision B (May 2014) **Page**

- 向数据表添加了 DRL 封装..... 1
- Changed I_{PP}, peak pulse current from 3.5 A to 3.0 A..... 4
- Added the ESD Ratings table..... 4
- Added Recommended Operating Conditions table..... 4
- Changed Electrical Characteristics table to reflect operating conditions at 25 °C..... 5
- Added MIN V_{RWM} value of – 5.5 V..... 5
- Changed V_{CLAMP} at I_{PP} = 1 A from 10.5 V to 10.9 V. 5
- Changed Line Capacitance TYP value from 1 pF to 0.7 pF..... 5
- Added Line Capacitance MAX value of 0.95 pF. 5
- Changed I_{LEAK} from MAX of 10 nA to 0.5 nA 5

Changes from Revision * (December 2012) to Revision A (January 2013) **Page**

- Fixed "f" units typo from GHz to MHz for C_L parameter in ELECTRICAL CHARACTERISTICS table..... 5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E1B06DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BYP	Samples
TPD4E1B06DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(BYG, BYH)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

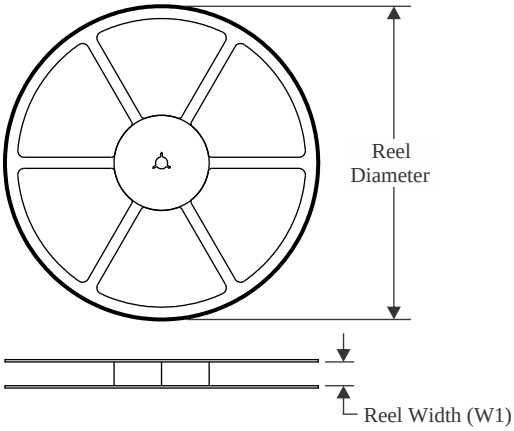
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

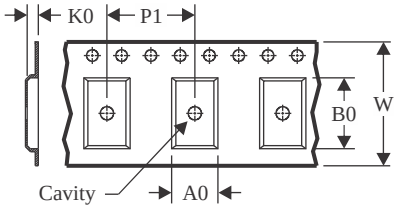
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

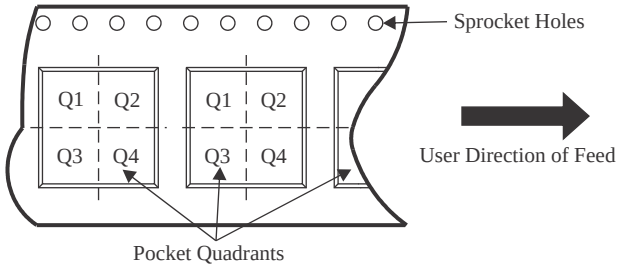


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

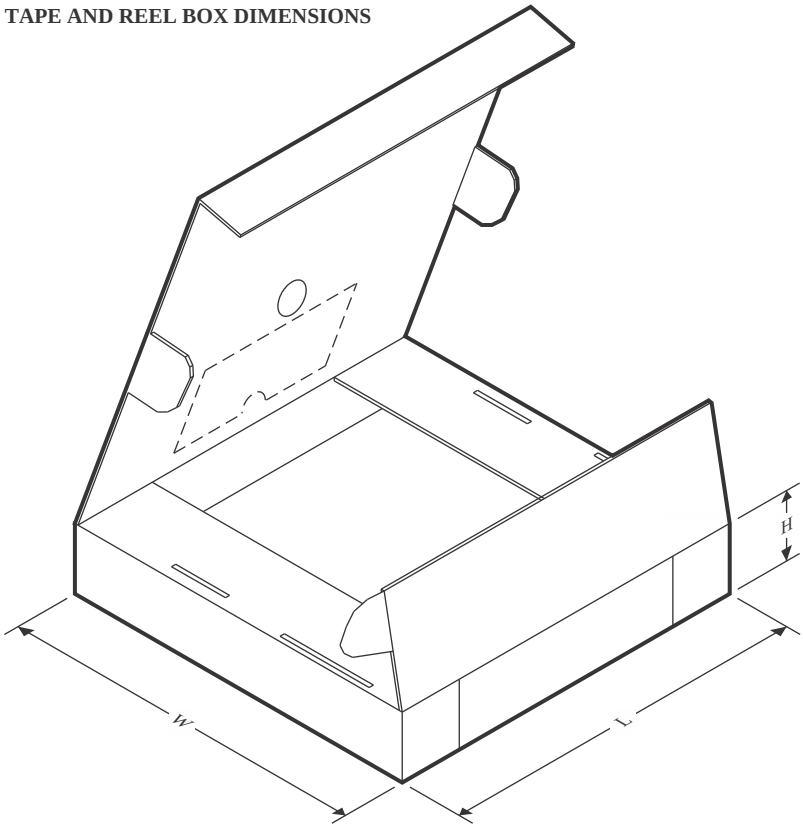
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E1B06DCKR	SC70	DCK	6	3000	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
TPD4E1B06DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

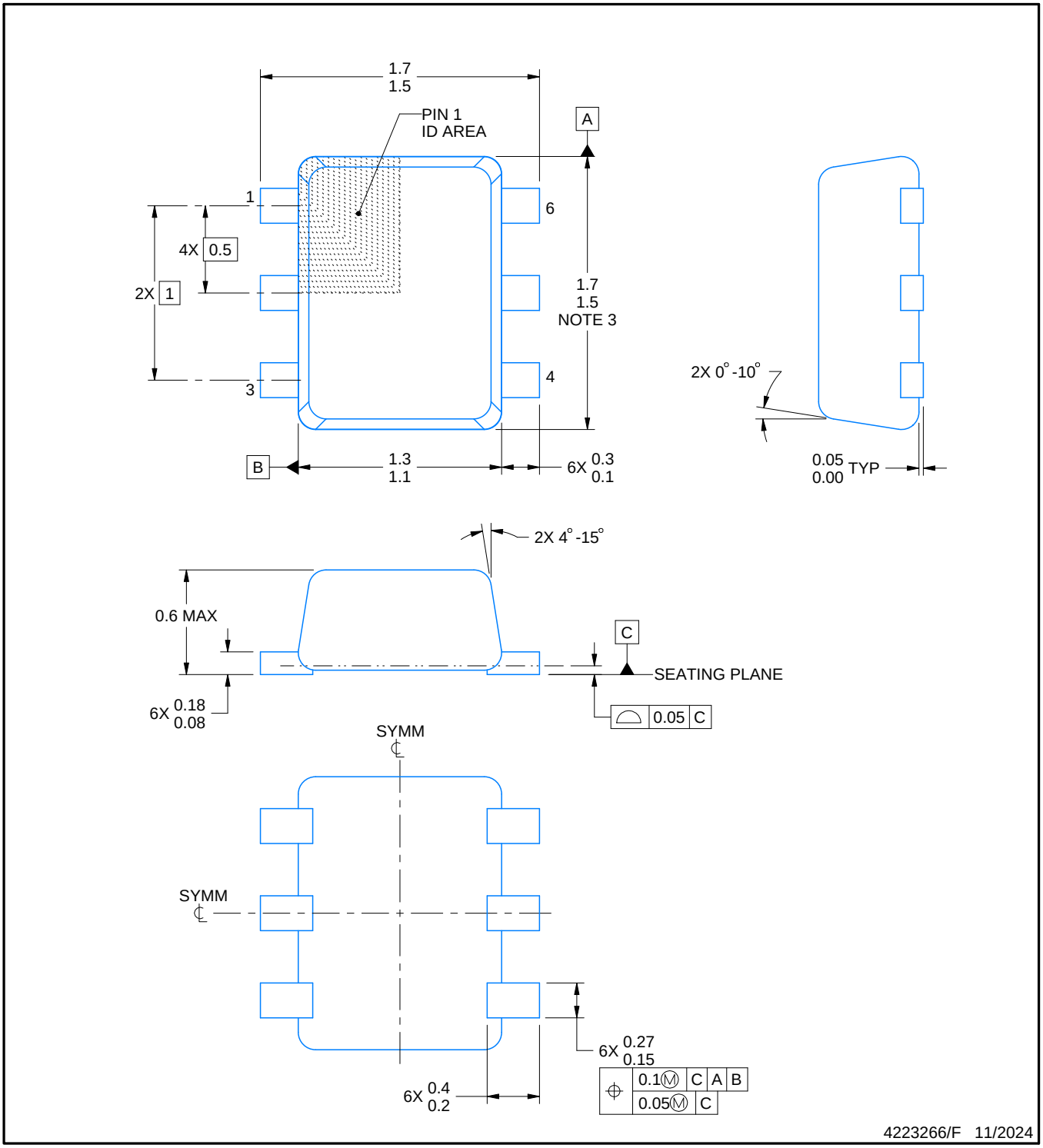
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E1B06DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TPD4E1B06DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

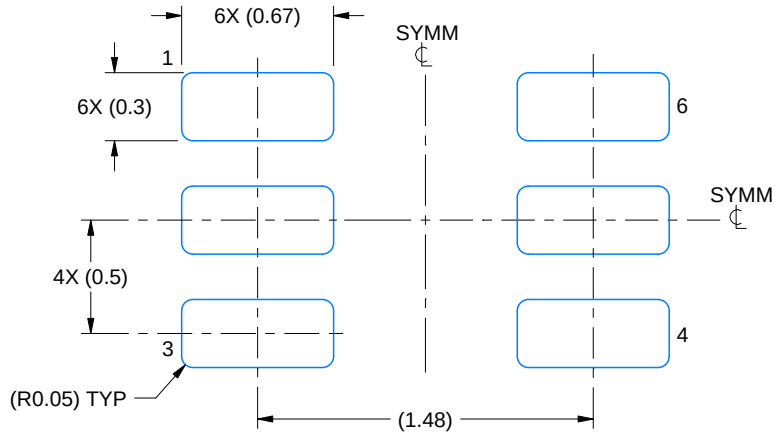
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

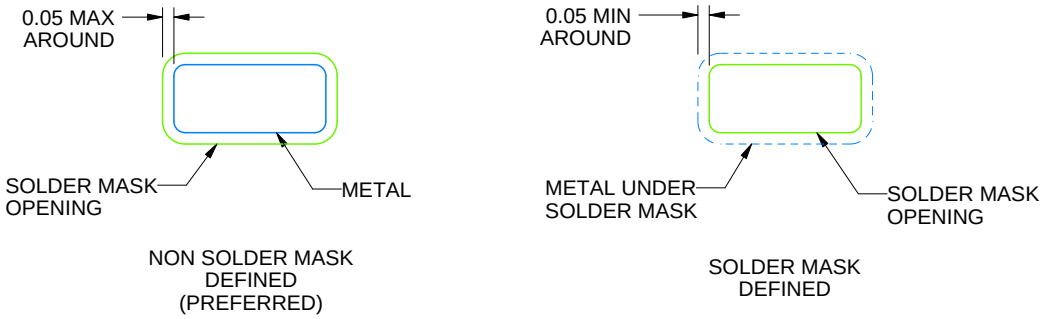
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

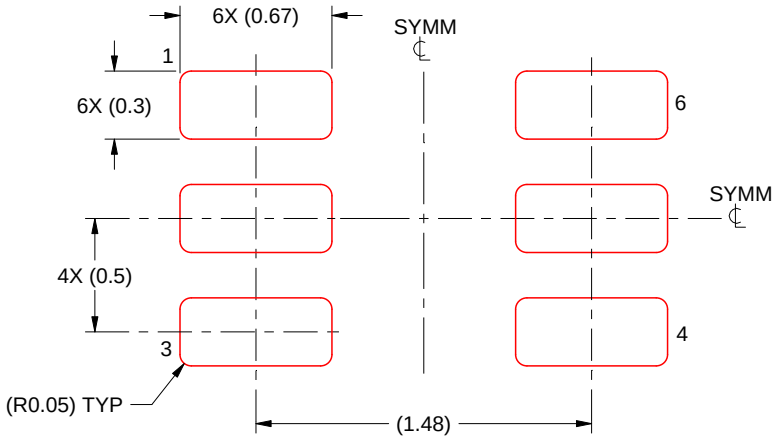
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

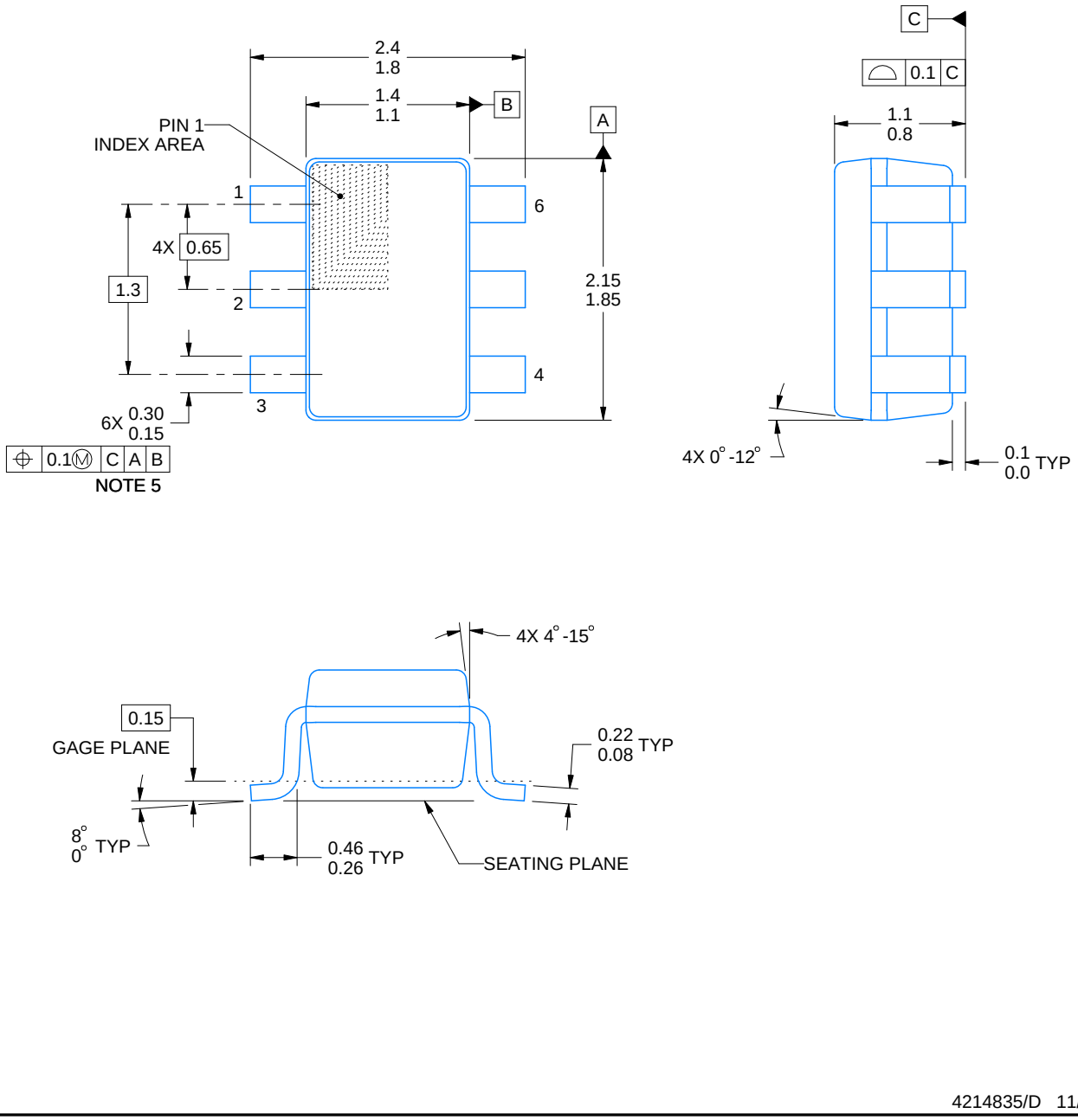
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

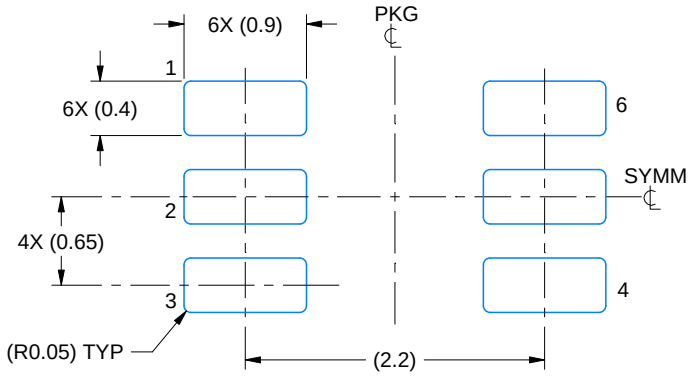
SMALL OUTLINE TRANSISTOR



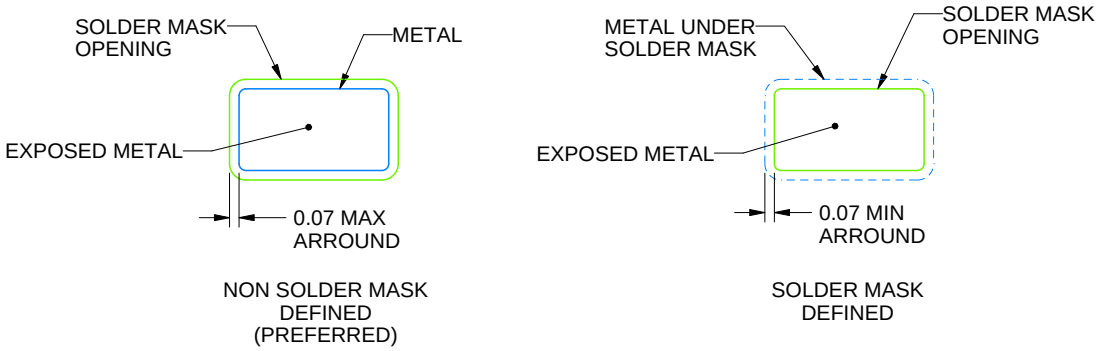
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

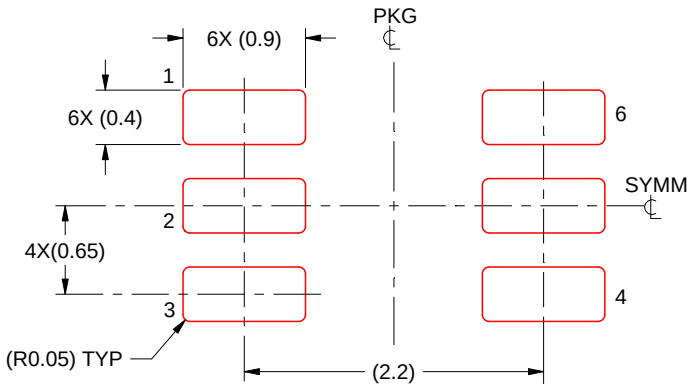


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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