

TPD4S214 具有 V_{BUS} 过压保护、 过流保护和四通道 ESD 保护的 USB OTG 配套器件

1 特性

- V_{BUS} 输入电压保护: -7V 至 30V
- IEC 61000-4-2 4 级静电放电 (ESD) 保护
 - $\pm 15kV$ 接触放电
 - $\pm 15kV$ 气隙放电
- IEC 61000-4-5 浪涌保护
 - 7.8A (8/20 μ s)
- 针对高效率的低 R_{DS} (导通) N 通道场效应晶体管 (FET) 开关
- 与 USB2.0 和 USB3.0 OTG 技术规格兼容
- 从 250mA 到 1.2A 以上的用户可调电流限值
- 内置软启动
- 反向电流阻断
- 针对 $V_{总线}$ 的过压闭锁
- 针对 V_{OTG_IN} 的欠压闭锁
- 热关断和短路保护
- 发生任何故障时会自动重试; 无锁存关闭状态
- 集成 $V_{总线}$ 检测电路
- 用于 USB2.0 高速数据率的低电容瞬态电压抑制器 (TVS) ESD 钳位
- 内部 16ms 启动延迟
- 节省空间的晶圆级芯片 (WCSP) (12-YFF) 封装
- 符合 UL 规范且 CB 档案编号 E169910

2 应用范围

- 手机
- 平板电脑, 电子书阅读器
- 便携式媒体播放器
- 数码摄像机

3 说明

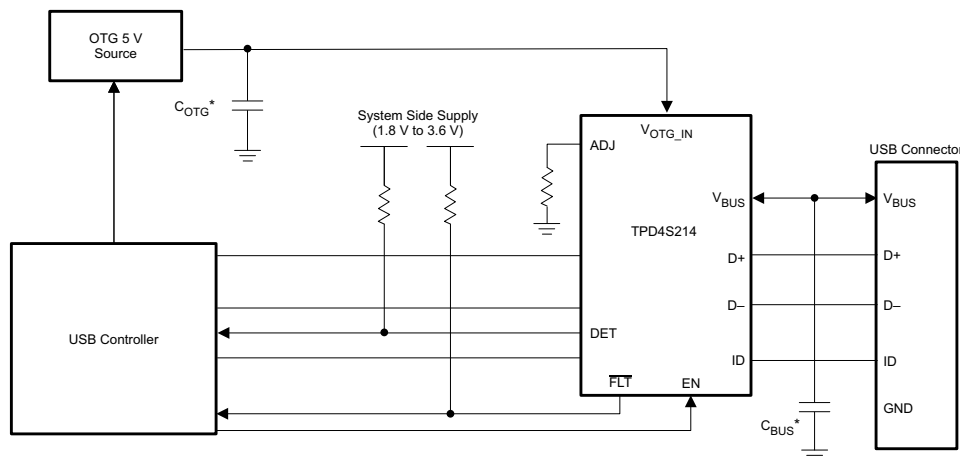
TPD4S214 是一款针对 USB On-the-Go (OTG) 和其他电流受限类 USB 应用的单芯片保护解决方案。该器件集成了一个低 $R_{DS(ON)}$ N 通道限流开关, 可为外设器件提供 OTG 电流。TPD4S214 在 D+、D- 和 ID 引脚上提供了低电容瞬态电压抑制 (TVS) 静电放电 (ESD) 钳位二极管, 同时适用于 USB2.0 和 USB3.0 应用。 V_{BUS} 引脚能够处理 -7V 至 30V 范围的持续电压。 V_{BUS} 引脚上的过压闭锁 (OVLO) 能够确保一旦 V_{BUS} 线路上发生故障, TPD4S214 能够将其隔离并保护内部电路不受损坏。相似地, V_{OTG_IN} 引脚上的欠压闭锁 (UVLO) 能够确保在 V_{OTG_IN} 下降到低于安全工作电平时, 内部 OTG 电源不会为外部 V_{BUS} 供电。当 EN 为高电平时, OTG 开关被激活并且 FLT 引脚表示是否有故障发生。此软启动特性在满足所有运行条件后等待 16ms 再打开 OTG 开关。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸 (最大值) |
|----------|---------------------|-----------------|
| TPD4S214 | 晶圆级芯片封装 (WCSP) (12) | 1.39mm x 1.69mm |

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

4 简化电路原理图



目录

| | | | | | |
|----------|---|----------|-----------|---|-----------|
| 1 | 特性 | 1 | 7.12 | Typical Characteristics | 8 |
| 2 | 应用范围 | 1 | 8 | Detailed Description | 11 |
| 3 | 说明 | 1 | 8.1 | Overview | 11 |
| 4 | 简化电路原理图 | 1 | 8.2 | Functional Block Diagram | 11 |
| 5 | 修订历史记录 | 2 | 8.3 | Feature Description | 12 |
| 6 | Pin Configuration and Functions | 3 | 8.4 | Device Functional Modes | 17 |
| 7 | Specifications | 4 | 9 | Application and Implementation | 18 |
| 7.1 | Absolute Maximum Ratings | 4 | 9.1 | Application Information | 18 |
| 7.2 | ESD Ratings | 4 | 9.2 | Typical Application | 18 |
| 7.3 | Recommended Operating Conditions | 4 | 10 | Power Supply Recommendations | 22 |
| 7.4 | Thermal Information | 5 | 11 | Layout | 22 |
| 7.5 | Thermal Shutdown | 5 | 11.1 | Layout Guidelines | 22 |
| 7.6 | Electrical Characteristics for EN, $\overline{\text{FLT}}$, DET, D+, D-, V _{BUS} , ID Pins | 5 | 11.2 | Layout Example | 22 |
| 7.7 | Electrical characteristics for UVLO / OVLO | 6 | 12 | 器件和文档支持 | 23 |
| 7.8 | Electrical Characteristics for DET Circuits | 6 | 12.1 | 文档支持 | 23 |
| 7.9 | Electrical Characteristics for OTG Switch | 6 | 12.2 | 商标 | 23 |
| 7.10 | Electrical Characteristics for Current Limit and Short Circuit Protection | 7 | 12.3 | 静电放电警告 | 23 |
| 7.11 | Supply Current Consumption | 7 | 12.4 | 术语表 | 23 |
| | | | 13 | 机械封装和可订购信息 | 23 |

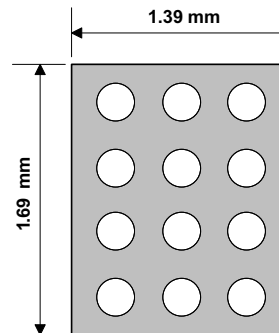
5 修订历史记录

| | |
|--|-------------|
| Changes from Revision E (January 2015) to Revision F | Page |
| • 已添加 UL 和 CB 认证。 | 1 |
| Changes from Revision D (October 2014) to Revision E | Page |
| • Added R _{LOAD} TEST CONDITIONS to I _{OCP} in the Electrical Characteristics for Current Limit and Short Circuit Protection table. | 7 |
| Changes from Revision C (August 2013) to Revision D | Page |
| • 处理额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。 | 1 |
| Changes from Original (January 2013) to Revision A | Page |
| • 已更改产品预览数据表 | 1 |
| Changes from Revision A (February 2013) to Revision B | Page |
| • 已将器件状态从：产品预览更改为：量产数据 | 1 |
| Changes from Revision B (February 2013) to Revision C | Page |
| • YFF PACKAGE Changed the YFF package dimensions | 3 |

6 Pin Configuration and Functions

TPD4S214 WCSP (YFF) PIN
MAPPING
(TOP SIDE/SEE-THROUGH VIEW)

| | 1 | 2 | 3 |
|---|---------------------|-------------------------|------------------|
| A | V _{OTG_N} | DET | V _{BUS} |
| B | V _{OTG_IN} | $\overline{\text{FLT}}$ | V _{BUS} |
| C | EN | GND | ID |
| D | ADJ | D- | D+ |



Pin Functions

| NAME | PIN | TYPE | DESCRIPTION |
|-------------------------|--------|--------|--|
| D- | D2 | I/O | USB data- |
| D+ | D3 | I/O | USB data+ |
| ID | C3 | I/O | USB ID signal |
| $\overline{\text{FLT}}$ | B2 | O | Open-Drain Output. Connect a pull-up resistor from $\overline{\text{FLT}}$ to the supply voltage of the host system. |
| ADJ | D1 | I | Attach external resistor to adjust the current limit |
| EN | C1 | I | Enable Input. Drive EN high to enable the OTG switch. |
| V _{BUS} | A3, B3 | O | USB Power Output |
| V _{OTG_IN} | A1, B1 | I | USB OTG Supply Input |
| DET | A2 | O | Open-Drain Output. Connect a pull-up resistor from DET to the supply voltage of the host system. |
| GND | C2 | Ground | Connect to PCB ground plane |

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------------------|--|------|-----|------|
| T_{stg} | Storage temperature range | -40 | 85 | °C |
| V_{OTG_IN} , ADJ, EN | Input voltage | -0.5 | 7 | V |
| V_{BUS} | Output voltage to USB connector | -7 | 30 | V |
| \overline{FLT} , DET | Output voltage | -0.5 | 7 | V |
| | Input clamp current $V_I < 0$ | | -50 | mA |
| | I_{OUT} Continuous current through \overline{FLT} and DET output | | 10 | mA |
| | I_{GND} Continuous current through GND | | 100 | mA |
| | $T_{J(max)}$ maximum junction temperature | -65 | 150 | °C |
| D+, D-, ID, V_{BUS} pins | IEC 61000-4-2 Contact Discharge at 25°C | | ±15 | kV |
| D+, D-, ID, V_{BUS} pins | IEC 61000-4-2 Air-gap Discharge at 25°C | | ±15 | kV |
| D+, D-, ID pins | Peak Pulse Current ($t_p = 8/20 \mu s$) at 25°C | | 7.8 | A |
| D+, D-, ID pins | Peak Pulse Power ($t_p = 8/20 \mu s$) at 25°C | | 84 | W |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|--|--------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 |
| | | IEC 61000-4-2 Contact Discharge | ±15000 |
| | | IEC 61000-4-2 Air-gap Discharge | |
| | | D+, D-, ID, V_{BUS} Pins | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT | |
|--------------------|--|--|-----|------|------|----|
| T_A | Operating free-air temperature | -40 | | 85 | °C | |
| V_{IH} | High-level input voltage EN | 1.2 | | | V | |
| V_{IL} | Low-level input voltage EN | | | 0.4 | V | |
| t_{EN} | EN ramp rate for proper turn on | Valid ramp rate is between 10 μs and 100 ms, rising and falling | | 0.01 | 100 | ms |
| t_{UVLO_SLEW} | V_{OTG_IN} ramp rate for proper UVLO operation | Valid ramp rate is between 10 μs and 100 ms, rising and falling | | 0.01 | 100 | ms |
| t_{OVLO_SLEW} | V_{BUS} ramp rate for proper OVLO operation | Valid ramp rate is between 10 μs and 100 ms, rising and falling | | 0.01 | 100 | ms |
| $T_{A_VBUS_ATT}$ | Time to detect V_{BUS} device attachment and turn on DET | | | 200 | | ms |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPD4S214 | | UNIT |
|-------------------------------|--|----------|--|------|
| | | YFF | | |
| | | 12 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 89.1 | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 0.5 | | |
| R _{θJB} | Junction-to-board thermal resistance | 40.0 | | |
| ψ _{JT} | Junction-to-top characterization parameter | 3.0 | | |
| ψ _{JB} | Junction-to-board characterization parameter | 39.0 | | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Thermal Shutdown

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | MAX | UNIT |
|--------------------|--|--|-----|------|------|
| T _{SHDN+} | Shutdown temp rising | | 141 | | °C |
| T _{SHDN-} | Shutdown temp falling | | 125 | | °C |
| T _{HYST} | Thermal-shutdown Hysteresis | | 16 | | °C |
| P _{MAX} | Maximum power dissipation | V _{OTG_IN} = 5 V, R _{load} = 5 Ω, EN = 5 V, R _{ADJ} = 75 KΩ | | 0.16 | W |
| T _{JMAX} | Junction Temp at max power dissipation | | | 150 | °C |

7.6 Electrical Characteristics for EN, \overline{FLT} , DET, D+, D-, V_{BUS}, ID Pins

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----|-----|------|------|
| I _{L_EN} | EN pin input leakage current | EN = 3.3 V | | | 1 | μA |
| I _{OL} | \overline{FLT} , DET pin output leakage current | \overline{FLT} , DET = 3.6 V | | | 1 | μA |
| V _{OL_FLT} | Low-level output voltage \overline{FLT} | V _{BUS} or V _{OTG_IN} = 5 V or 0 V I _{OL} = 100 μA | | | 100 | mV |
| V _{OL_DET} | Low-level output voltage DET | V _{BUS} and V _{OTG_IN} = 5 V or 0 V I _{OL} = 100 μA | | | 100 | mV |
| C _{EN} | Enable capacitance | V _{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V _{OTG_IN} = 5 V | | 4.5 | | pF |
| V _D | Diode forward voltage D+, D-, ID pins; lower clamp diode | I _O = 8 mA | | | 0.95 | V |
| I _{L_D} | Leakage current on D+, D-, ID Pins | D+, D-, ID = 3.3 V | | | 100 | nA |
| ΔC _{IO} | Differential capacitance between the D+, D- lines | V _{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V _{OTG_IN} = 5 V | | | 0.04 | pF |
| C _{IO} | Capacitance to GND for the D+, D- lines | V _{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V _{OTG_IN} = 5 V | | 1.9 | | pF |
| | Capacitance to GND for the ID lines | | | 1.9 | | |
| V _{BR} | Breakdown voltage D+, D-, ID pins | I _{br} = 1 mA | 6 | | | V |
| | Breakdown voltage on V _{BUS} | I _{br} = 1 mA | 33 | | | V |
| R _{DYN} | Dynamic on resistance D+, D-, ID clamps | | | 1 | | Ω |

7.7 Electrical characteristics for UVLO / OVLO

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--|---|------|------|------|------|
| INPUT UNDER-VOLTAGE LOCKOUT | | | | | | |
| V _{UVLO+} | Under-voltage lock-out, input power detected threshold rising | V _{OTG_IN} increasing from 0 V to 5 V, No load on V _{BUS} pin | 3.4 | 3.6 | 3.8 | V |
| V _{UVLO-} | Under-voltage lock-out, input power detected threshold falling | V _{OTG_IN} decreasing from 5 V to 0 V, No load on V _{BUS} pin | 3.0 | 3.2 | 3.5 | V |
| V _{HYS-UVLO} | Hysteresis on UVLO | Δ of V _{UVLO+} and V _{UVLO-} | 260 | | | mV |
| T _{RUVLO} | Recovery time from UVLO | V _{OTG_IN} increasing from 0V to 5V, No load on V _{BUS} pin; time from V _{OTG_IN} = V _{UVLO+} to $\overline{\text{FLT}}$ toggles high | 18 | | | ms |
| T _{RESP_UVLO} | Response time for UVLO | V _{OTG_IN} decreasing from 5V to 0V, No load on V _{BUS} pin; time from V _{OTG_IN} = V _{UVLO-} to $\overline{\text{FLT}}$ toggles low | 0.18 | | | μs |
| OUTPUT OVERVOLTAGE LOCKOUT | | | | | | |
| V _{OVP+} | OVLO rising threshold | Both V _{OTG_IN} and V _{BUS} increasing from 5 V to 7 V | 5.55 | 6.15 | 6.45 | V |
| V _{OVP-} | OVLO falling threshold | Both V _{OTG_IN} and V _{BUS} decreasing from 7 V to 5 V | 5.4 | 6 | 6.3 | V |
| V _{HYS-OVP} | Hysteresis on OVLO | Δ of V _{UVLO+} and V _{UVLO-} | 100 | | | mV |
| T _{ROVLO} | Recovery time from OVLO | Both V _{OTG_IN} and V _{BUS} decreasing from 7 V to 5 V, V _{OTG_IN} = 5 V; time from V _{BUS} = V _{OVP-} to $\overline{\text{FLT}}$ toggles high | 9 | | | ms |
| T _{RESP_OVLO} | Response time for OVLO | Both V _{OTG_IN} and V _{BUS} increasing from 5 V to 7 V, V _{OTG_IN} = 5 V; time from V _{BUS} = V _{OVP+} to $\overline{\text{FLT}}$ toggles low | 17 | | | μs |

7.8 Electrical Characteristics for DET Circuits

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|--|-----|-----|-----|------|
| V _{BUS_VALID-} | Valid V _{BUS} voltage detect | V _{BUS} = 7 V to 0 V | 2.7 | 2.9 | 3 | V |
| V _{BUS_VALID+} | Valid V _{BUS} voltage detect | V _{BUS} = 0 V to 7 V | 5.3 | 5.4 | 5.6 | V |
| T _{DET_DELAY-} | V _{BUS} detect propagation delay- | V _{BUS} 0 V to 4 V, 200 ns ramp; V _{BUS} = V _{BUS_VALID-} MIN to DET toggles high | 4.9 | | | μs |
| T _{DET_DELAY+} | V _{BUS} detect propagation delay+ | V _{BUS} 6 V to 4 V, 200 ns ramp; V _{BUS} = V _{BUS_VALID+} MAX to DET toggles low | 1.8 | | | μs |

7.9 Electrical Characteristics for OTG Switch

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|-------------------------|--|--|-----|-----|------|----|
| R _{DS_ON} | OTG switch resistance | T _A = 25 °C, V _{BUS} = 5 V, I _{OUT} = 100 mA, R _{ADJ} = 75 kΩ ⁽¹⁾ | 263 | | | 290 | mΩ |
| V _{DROP} | OTG switch voltage drop | V _{BUS} = 5 V, I _{OUT} = 100 mA, R _{ADJ} = 75 kΩ | 12.6 | | | 29 | mV |
| I _{OTG_OFF_30V} | Leakage current at 30V | Measured at V _{OTG_IN} | V _{BUS} = 30 V, EN = 5 V, V _{OTG_IN} = 5 V | | | 6 | μA |
| I _{OTG_OFF_2V} | Leakage current at -2V | | V _{BUS} = 30 V, EN = 5 V, V _{OTG_IN} = 0 V | | | 11 | nA |
| I _{OTG_OFF} | Standby Leakage current | | V _{BUS} = -2 V, EN = 5 V, V _{OTG_IN} = 5 V | | | 30 | μA |
| | | | V _{BUS} = 0 V, EN = 0 V, V _{OTG_IN} = 5 V | | | 32 | μA |
| I _{BUS_REV} | Reverse Leakage current | | V _{BUS} = 5 V, EN = 0 V, V _{OTG_IN} = 0 V | | | 10 | nA |
| | | | V _{BUS} = 5 V, EN = 5 V, V _{OTG_IN} = 0V | | | 1 | nA |
| V _{BUS} = 5.5 V, EN = 5 V, V _{OTG_IN} = 5 V | | | 6 | | | μA | |
| T _{ON} | Turn-ON time | R _L = 100 Ω, C _L = 1 μF, R _{ADJ} = 75 kΩ | 16 | | | ms | |
| T _{OFF_EN} | Turn-OFF time | R _L = 100 Ω, C _L = 1 μF, R _{ADJ} = 75 kΩ, toggle EN | 80 | | | μs | |
| T _{OFF_OTG} | Turn-OFF time | R _L = 100 Ω, C _L = 1 μF, R _{ADJ} = 75 kΩ, toggle V _{OTG_IN} | 0.5 | | | μs | |
| T _{RISE} | Output rise time | R _L = 100 Ω, C _L = 1 μF, R _{ADJ} = 75 kΩ | 137 | | | μs | |
| T _{FALL} | Output fall time | R _L = 100 Ω, C _L = 1 μF, R _{ADJ} = 75 kΩ | 1.6 | | | μs | |

(1) R_{DS(ON)} is measured at 25°C

7.10 Electrical Characteristics for Current Limit and Short Circuit Protection

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------|--|---|--|------|------|------|------|
| I _{OCP} | Current-limit threshold (maximum DC output current I _{OUT} delivered to load) | V _{OTG_IN} = 5 V, R _{LOAD} = 2.0 Ω | R _{ADJ} = 226 kΩ ⁽¹⁾ | 235 | 245 | 281 | mA |
| | | | R _{ADJ} = 75 kΩ ⁽¹⁾ | 735 | 792 | 830 | |
| | | | R _{ADJ} = 62 kΩ ⁽¹⁾ | 885 | 959 | 1005 | |
| | | | R _{ADJ} = 45 kΩ ⁽¹⁾ | 1128 | 1200 | 1363 | |
| T _{BLANK} | Blanking time after enable | V _{OTG_IN} = 5 V | RL = 1 Ω, CL = 1 μF, RADJ = 75 kΩ | | 4 | | ms |
| T _{DEGL} | Deglitch time while enabled | V _{OTG_IN} = 5 V, RL = 100 Ω, CL = 1 μF, RADJ = 75 kΩ, apply short to ground | | | 9.4 | | ms |
| T _{DET_SC} | Response time to short circuit | | | | 10 | | μs |
| T _{REG} | Short circuit regulation time | | Hiccup pulse width; auto-retry time | | 13 | | ms |
| T _{OCP} | Short circuit over current protection time | | Hiccup pulse period | | 153 | | ms |
| V _{SHORT} | Short circuit threshold | | | | 4 | | V |
| I _{INRUSH} | Inrush current during a startup | See Figure 23 under test configuration | RL = 100 Ω, CL = 22 μF, RADJ = 75 kΩ | | 726 | | mA |

(1) External resistor tolerance is ±1%

7.11 Supply Current Consumption

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | TYP | MAX | UNIT |
|------------------------|--|---|---------------|-----|-----|------|
| I _{VOTG_INON} | High-level V _{OTG_IN} operating current consumption | V _{OTG_IN} = 5 V, No load on V _{BUS} , EN = 5 V | RADJ = 75 kΩ | 162 | 200 | μA |
| | | | RADJ = 226 kΩ | 150 | 200 | μA |

7.12 Typical Characteristics

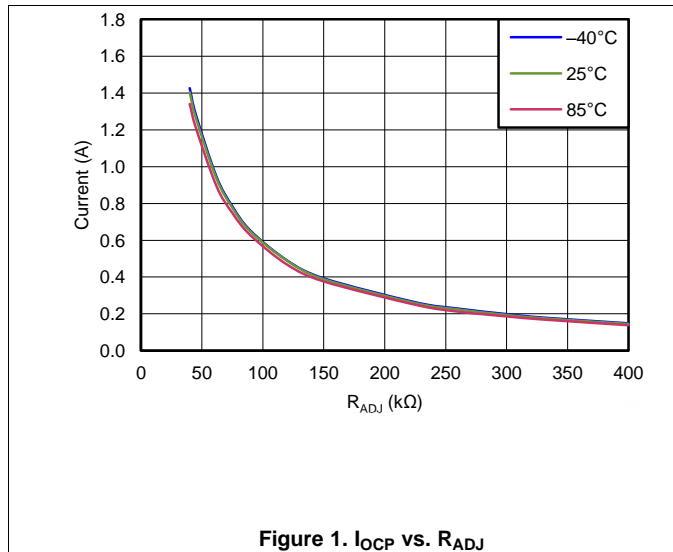


Figure 1. I_{OCP} vs. R_{ADJ}

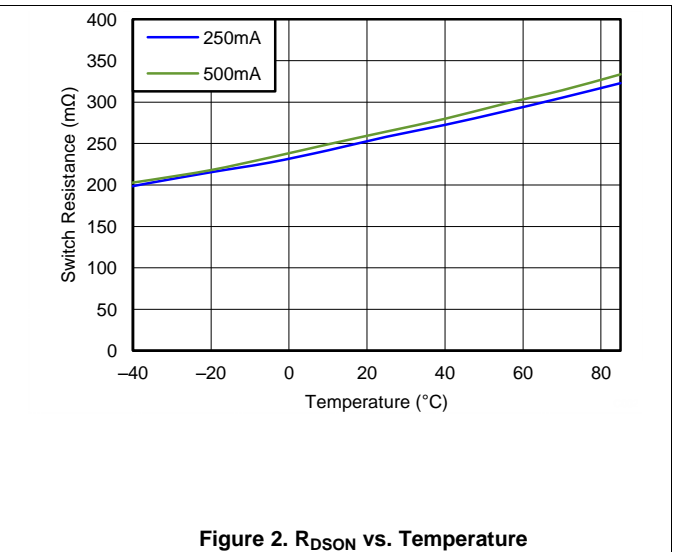


Figure 2. $R_{DS(on)}$ vs. Temperature

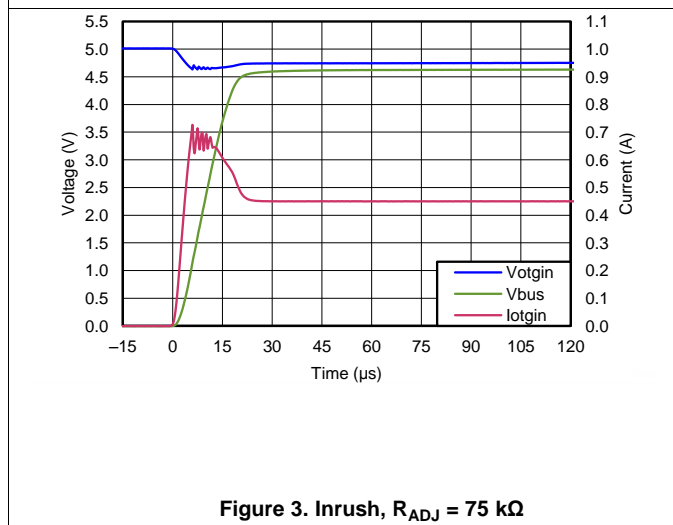


Figure 3. Inrush, $R_{ADJ} = 75\text{ k}\Omega$

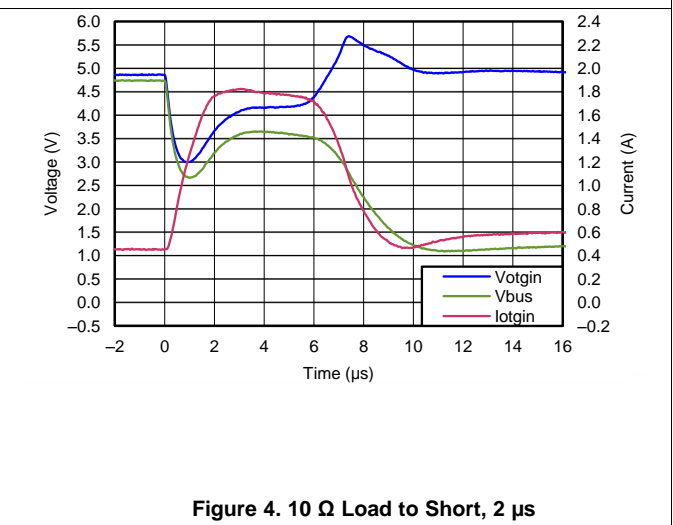


Figure 4. $10\ \Omega$ Load to Short, $2\ \mu\text{s}$

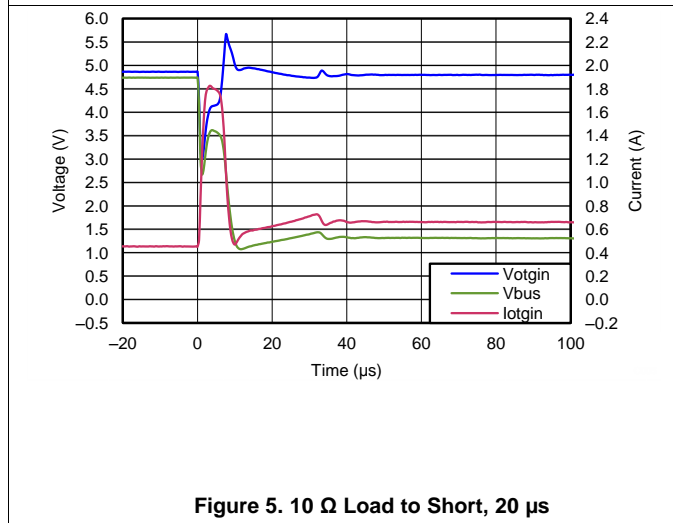


Figure 5. $10\ \Omega$ Load to Short, $20\ \mu\text{s}$

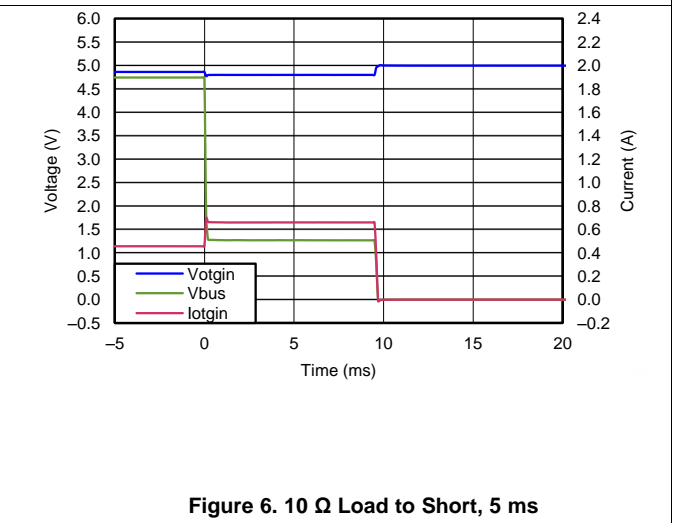
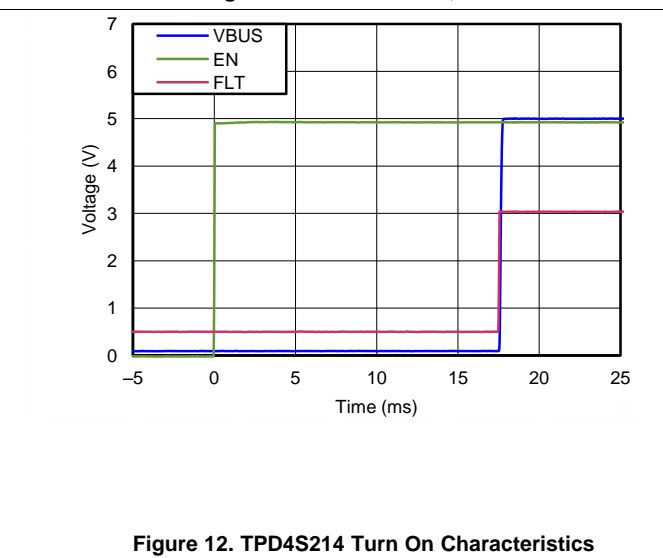
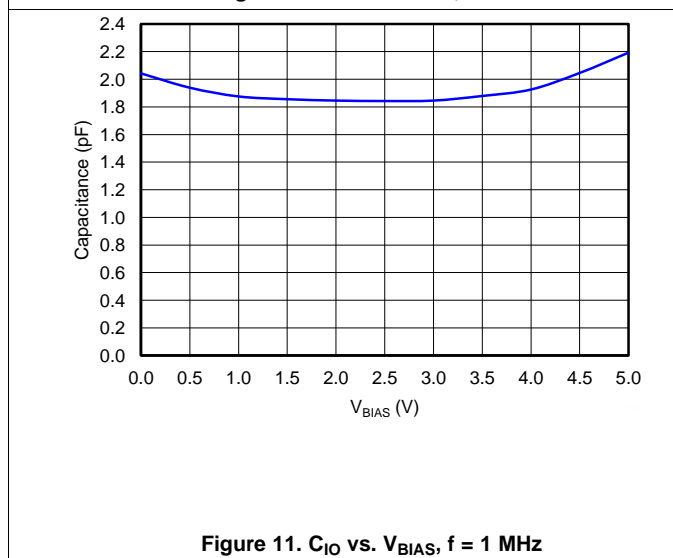
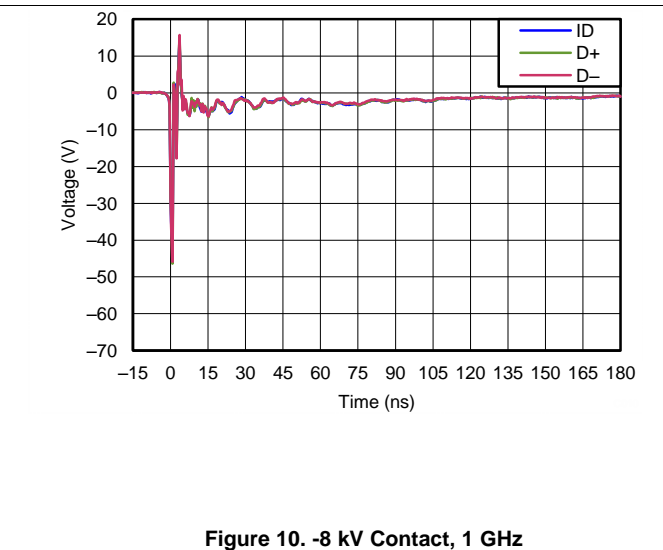
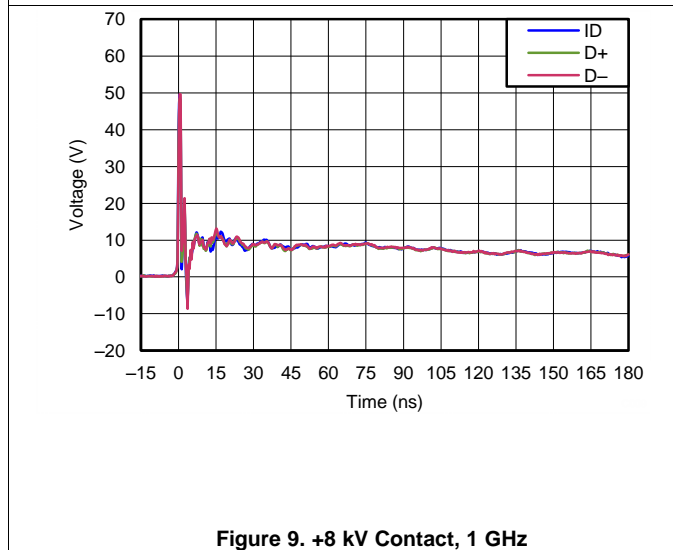
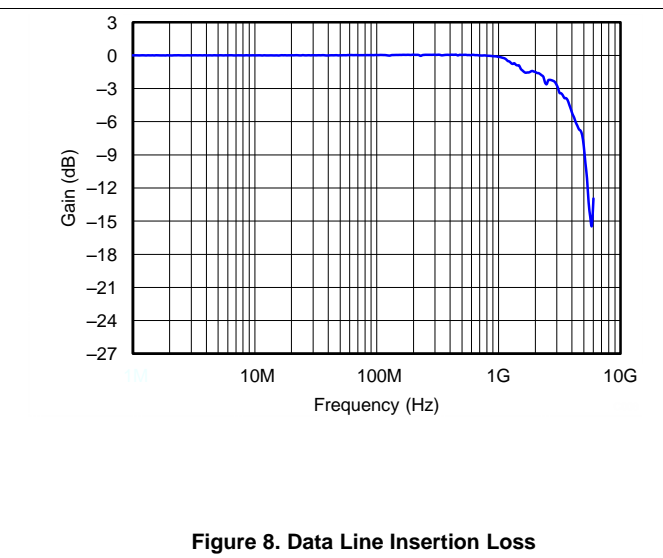
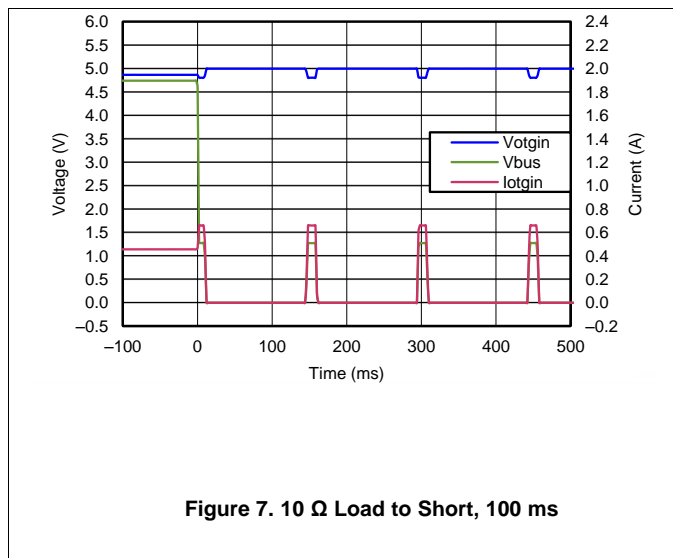
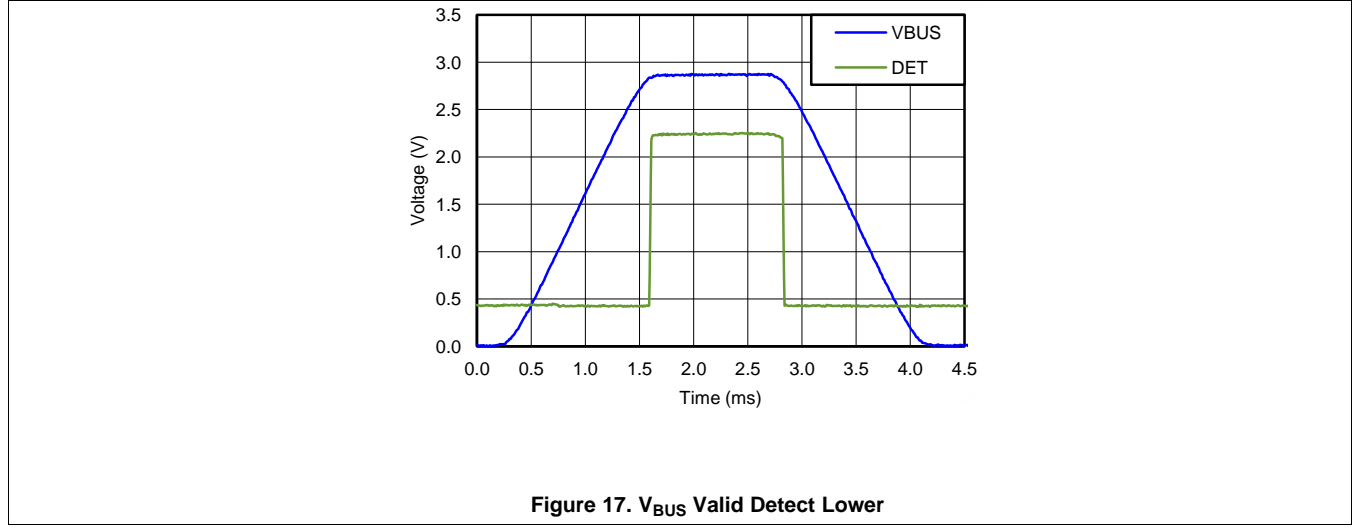
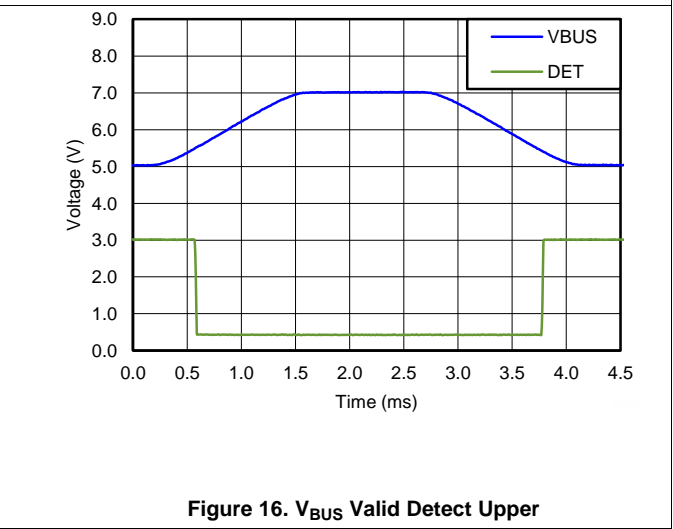
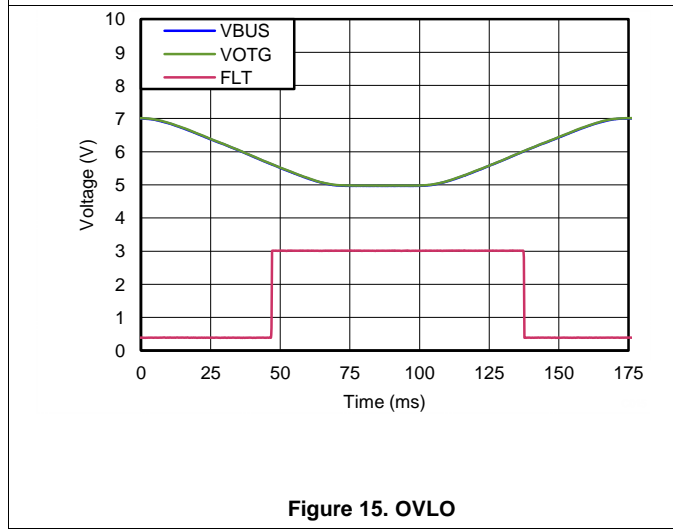
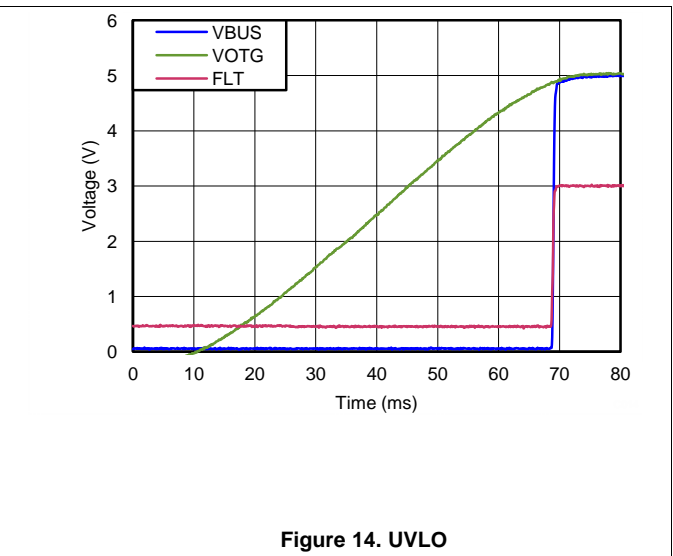
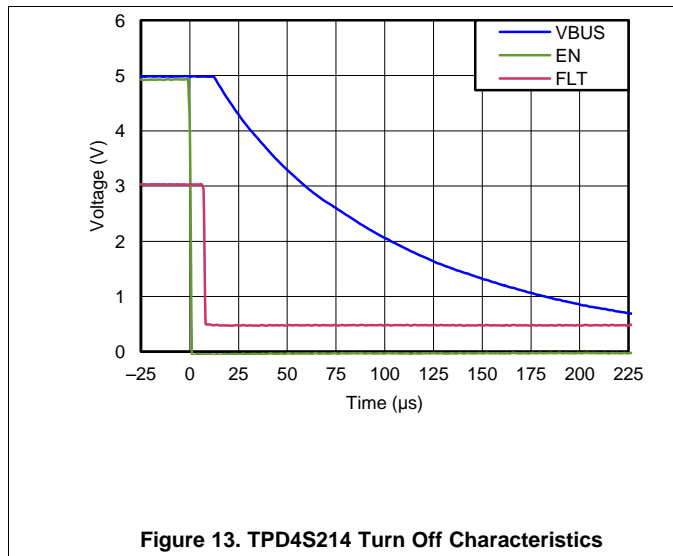


Figure 6. $10\ \Omega$ Load to Short, $5\ \text{ms}$

Typical Characteristics (continued)



Typical Characteristics (continued)



8 Detailed Description

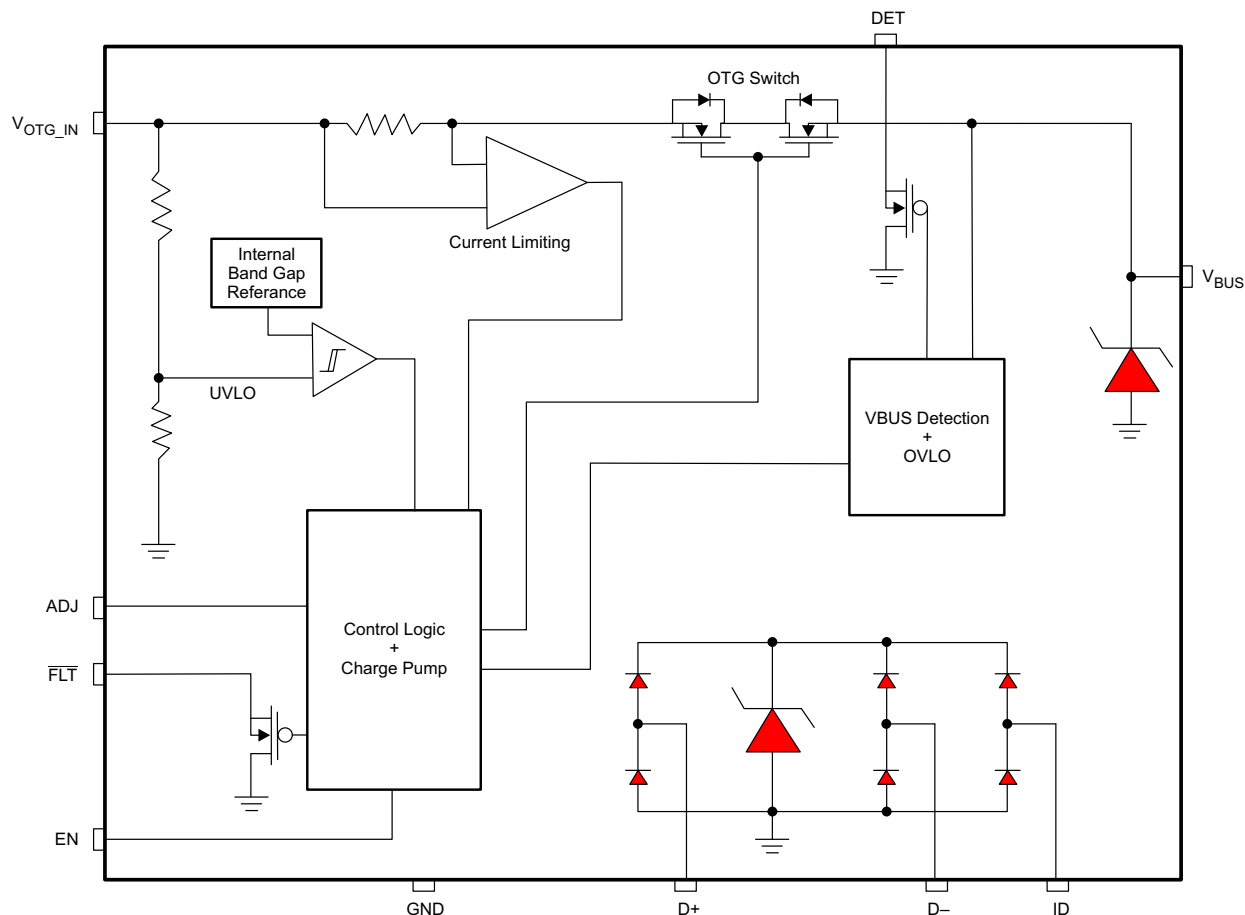
8.1 Overview

The TPD4S214 is a single-chip protection solution for USB On-the-Go and other current limited USB applications. This device includes an integrated low $R_{DS(ON)}$ N-channel current limited switch for OTG current supply to peripheral devices. TPD4S214 offers low capacitance TVS ESD clamps for the D+, D-, and ID pins for both USB2.0 and USB3.0 applications. The V_{BUS} pin can handle continuous voltage ranging from -7 V to 30 V . The OVLO at the V_{BUS} pin ensures that if there is a fault condition at the V_{BUS} line, TPD4S214 is able to isolate it and protect the internal circuitry from damage. Similarly, the UVLO at the V_{OTG_IN} pin ensures that there is no power drain from the internal OTG supply to external V_{BUS} if V_{OTG_IN} droops below a safe operating level.

When EN is high, the OTG switch is activated and the \overline{FLT} pin indicates whether there is a fault condition. The soft start feature waits 16 ms to turn on the OTG switch after all operating conditions are met. The \overline{FLT} pin asserts low during any one of the following fault conditions: OVLO ($V_{BUS} > V_{OVLO}$), UVLO condition ($V_{OTG_IN} < V_{UVLO}$) over temperature, over current, short circuit condition, or reverse-current-condition ($V_{BUS} > V_{OTG_IN}$). The OTG switch is turned off during any fault condition. Once the switch is turned off, the IC periodically rechecks the faults internally. If the IC returns to normal operating conditions, the switch turns back on and \overline{FLT} is reset to high.

There is also a V_{BUS} detection feature for facilitating USB communication between USB host and peripheral device. If this is not used, the DET pin can be either floating or connected to ground.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage Protection at V_{BUS} from -7 V to 30 V

The V_{BUS} pin can handle continuous voltage ranging from -7 V to 30 V . The OVLO at the V_{BUS} pin ensures that if there is a fault condition at the V_{BUS} line, TPD4S214 is able to isolate the fault and protect the internal circuitry from damage.

8.3.2 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to $\pm 15\text{-kV}$ contact and air gap. An ESD clamp diverts the current to ground.

8.3.3 Low $R_{DS(ON)}$ N-CH FET Switch for High Efficiency

A Low $R_{DS(ON)}$ ensures there is minimal voltage loss when supplying high current to OTG devices.

8.3.4 Compliant with USB2.0 and USB3.0 OTG spec

The capability of TPD4S214 to supply greater than 1.2 A of current on V_{BUS} meets or exceeds the USB2.0 and USB3.0 OTG specification.

8.3.5 User Adjustable Current Limit From 250 mA to Beyond 1.2 A

The designer can select the over current protection level by selecting the proper R_{ADJ} .

8.3.6 Built-in Soft-start

The soft start feature waits 16 ms to turn on the OTG switch after all operating conditions are met.

8.3.7 Reverse Current Blocking

If V_{BUS} is greater than V_{OTG_IN} by 50 mV , the OTG switch is disabled in 17.5 ms .

8.3.8 Over Voltage Lock Out for V_{BUS}

OVLO ensures that an over voltage condition on V_{BUS} disables the OTG switch to protect the system.

8.3.9 Under Voltage Lock Out for V_{OTG_IN}

UVLO ensures that an under voltage condition on V_{BUS} disables the OTG switch to protect the system.

8.3.10 Thermal Shutdown and Short Circuit Protection

TPD4S214 has an over-temperature protection circuit to protect against system faults or improper use. The basic function of the thermal shutdown (TSD) circuit is to sense when the junction temperature has exceeded the absolute maximum rating and shut down the device until the junction temperature has cooled to a safe level. Short circuit protection prevents any damaging current demand from the system.

8.3.11 Auto Retry on any Fault; no Latching off States

In any fault condition, TPD4S214 will reassess V_{BUS} , V_{OTG_IN} , and thermal conditions until a safe state is reached and then enable the OTG switch, eliminating any latched off states.

8.3.12 Integrated V_{BUS} Detection Circuit

TPD4S214 has a V_{BUS} detection feature facilitating communication between the USB host and peripheral device. The use of this feature is optional.

8.3.13 Low Capacitance TVS ESD Clamp for USB2.0 High Speed Data Rate

The High Speed data lines have a capacitance less than 2 pF , supporting a bandwidth greater than 3 GHz . This easily accommodates the 480-Mbps data rate defined in the USB2.0 specification.

Feature Description (continued)

8.3.14 Internal 16ms Startup Delay

The built-in start up delay allows for voltages on V_{BUS} to reach a steady state after which a 1- μ A trickle charge slowly turns on the main switch. During the inrush period, the peak inrush current will be limited to no more than the current limit set by the external resistor R_{ADJ} .

8.3.15 Space Saving WCSP (12-YFF) Package

The 1.69 mm \times 1.39 mm (Max) WCSP package is valuable in space constrained designs.

8.3.16 Inrush Current Protection

As soon as TPD4S214 is enabled, its logic block detects the presence of any fault conditions highlighted in [Table 2](#). In the absence of any fault condition, a counter waits for 16 ms, after which a 1- μ A trickle charge slowly turns on the main switch. During the inrush period, the peak inrush current will be limited to no more than the current limit set by the external resistor R_{ADJ} .

8.3.17 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{OTG_IN} and GND. A 10- μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

8.3.18 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_{LOAD} is highly recommended. A C_{LOAD} greater than C_{IN} can cause V_{BUS} to exceed V_{OTG_IN} when the system supply is removed. A C_{IN} to C_{LOAD} ratio of 10 to 1 is recommended for minimizing V_{OTG_IN} dip caused by inrush currents during startup.

8.3.19 Current Limit

The TPD4S214 provides current limiting protection, which is set by an external resistor connected from the ADJ pin to ground shown in [Figure 18](#). The current limiting threshold I_{OCP} is set by the external resistor R_{ADJ} . [Figure 19](#) shows the typical current limit for a corresponding R_{ADJ} value with $\pm 1\%$ tolerance across the operating temperature range.

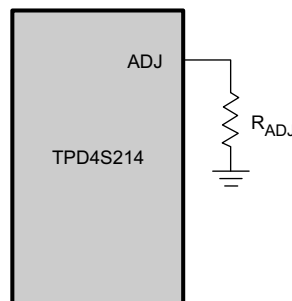


Figure 18. Current Limit Diagram

$$R_{ADJ} = \frac{55.358}{I_{OCP}} \quad (1)$$

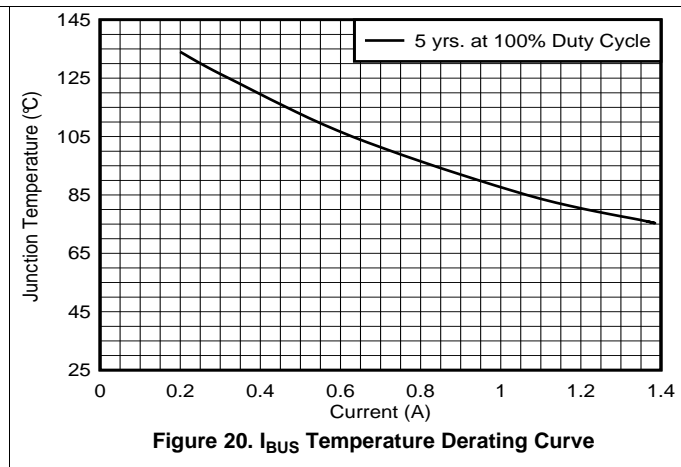
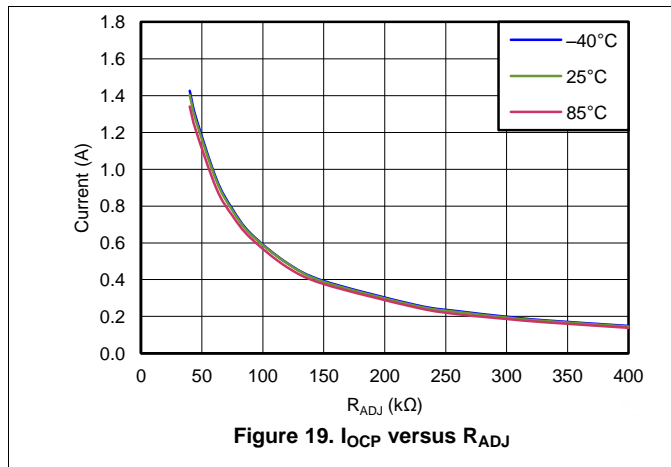
Where:

R_{ADJ} = external resistor used to set the current limit (k Ω)

I_{OCP} = current limit set by the external R_{ADJ} resistor (A)

R_{ADJ} is placed between the ADJ pin and ground, shown in [Figure 18](#), providing a maximum current limit between 250 mA and 1.2 A.

Feature Description (continued)



The temperature derating curve shown in [Figure 20](#) graphs the line where TPD4S214 will have a Mean Time Before Failure (MTBF) of 5 years at a 100% duty cycle for a given junction temperature, T_j , and current on V_{BUS} , or I_{BUS} . MTBF of 5 years at a 100% duty cycle is equivalent to 7.5 years at a 75% duty cycle, or 10 years at a 50% duty cycle. See [Equation 2](#) to calculate the junction temperature. If a current and junction temperature point lie below the curve on the graph then the MTBF will exceed 5 years at a 100% duty cycle, or its equivalent. If above the curve, the MTBF will be decreased.

8.3.20 Thermal Shutdown

When the device is ON, current flowing through the device will cause the device to heat up. Overheating can lead to permanent damage to the device. To prevent this, an over temperature protection has been designed into the device. Whenever the junction temperature exceeds 141°C, the switch will turn off, thereby limiting the temperature. Once the device cools down to below 125°C the switch will turn on if the EN is active and the V_{BUS} voltage is within the UVLO and OVP thresholds. While the over temperature protection in the device will not kick-in unless the die temperature reaches 141°C, it is generally recommended that care is taken to keep the junction temperature below 125°C. Operation of the device above 125°C for extended periods of time can affect the long-term reliability of the part.

The junction temperature of the device can be calculated using the below formula:

$$T_j = T_A + P_D R_{\theta JA} \tag{2}$$

Where:

- T_j = Junction temperature
- T_A = Ambient temperature
- $R_{\theta JA}$ = Thermal resistance
- P_D = Power Dissipated in device

$$P_D = I^2 R_{DS(ON)} \tag{3}$$

- I = Current through device
- $R_{DS(ON)}$ = Max on resistance of device

Example

At 0.5 A, the continuous current power dissipation is given by:

$$P_D = 0.5^2 \times 0.3 = 0.075 \text{ W} \tag{4}$$

If the ambient temperature is about 85 °C the junction temperature will be:

$$T_j = 85 + (0.075 \times 89.1) = 91.7^\circ\text{C} \tag{5}$$

Feature Description (continued)

This implies that, at an ambient temperature of 85°C, TPD4S214 can pass a continuous 0.5 A without sustaining damage. Conversely, the above calculation can also be used to calculate the total continuous current the TPD4S214 can handle at any given temperature.

The MTBF can be estimated by examining [Figure 20](#). Locating 0.5 A and 91.7 °C, the point is below the curve. This implies that the MTBF for this calculation is longer than 5 years at a 100% duty cycle. If the duty cycle is 50% then MTBF exceeds 10 years.

8.3.21 V_{BUS} Detection

There are several important protocols defined in [OTG and EH Supplement] that governs communication between Targeted Hosts (A-device) and USB peripherals (B-device). Communication between host and peripheral is usually done on the ID pin only. In the case when two OTG devices that could both act as either host or peripheral are connected, measuring voltage level on V_{BUS} will aid in the handshaking process. If an embedded host instead of a USB peripheral is connected to the OTG device, OTG charging would not be required and the system's OTG source should remain off to conserve power. The TPD4S214 V_{BUS} detection block aids power conservation and is powered from V_{BUS}. See [Functional Block Diagram](#). The DET pin is an open drain PMOS output with default state low.

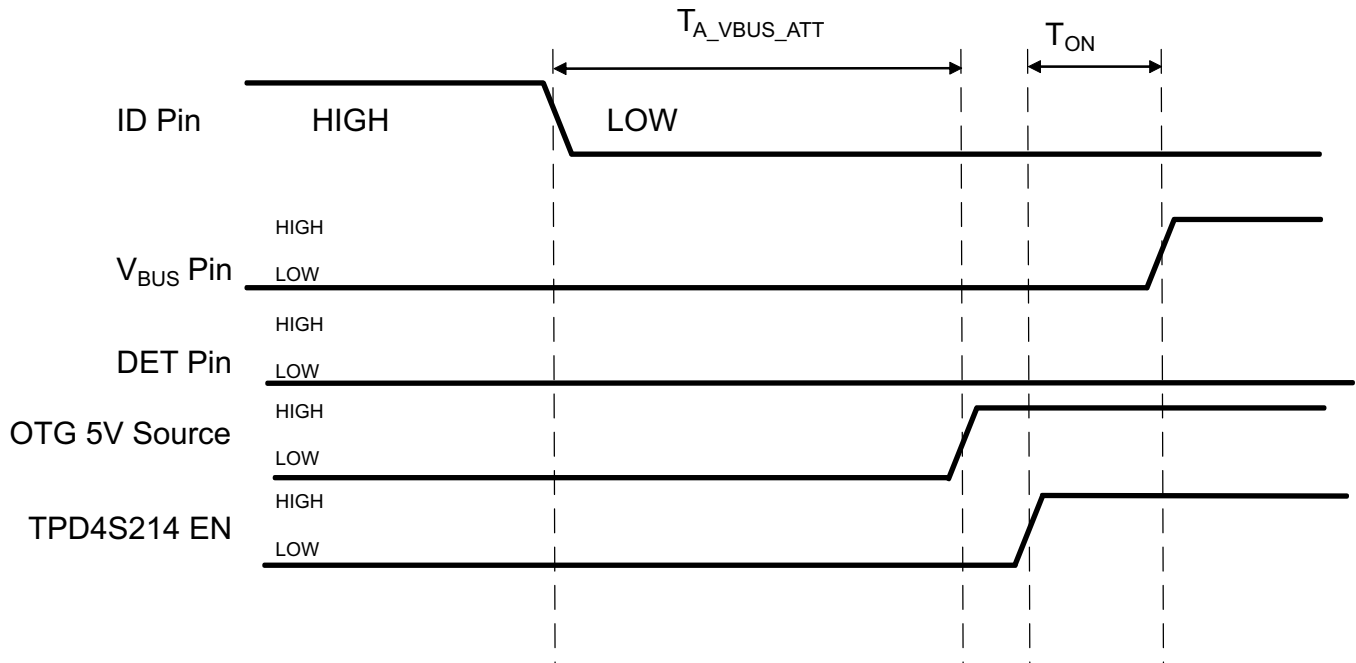
In the event when an A-plug is attached, the system detects ID pin as FALSE, in which case ID pin resistance to ground is less than 10 Ω. For a B-plug, the system detects ID pin as TRUE and ID pin resistance to ground is greater than 100 kΩ. For the system to power a USB device through OTG switch once it is connected, voltage on V_{BUS} should remain below V_{BUS_VALID MIN} within T_{A_VBUS_ATT} of the ID pin becoming FALSE. After this event, the system confirms that the USB device requires power and enables both TPD4S214 and OTG source. However, if V_{BUS_VALID} is detected on V_{BUS} within T_{A_VBUS_ATT} of the ID pin becoming FALSE, there is either a system error or the device connected does not require charging. OTG source remains switched off and the entire sequence would restart when the system detects another FALSE on the ID pin.

Table 1. V_{BUS} Detection scheme

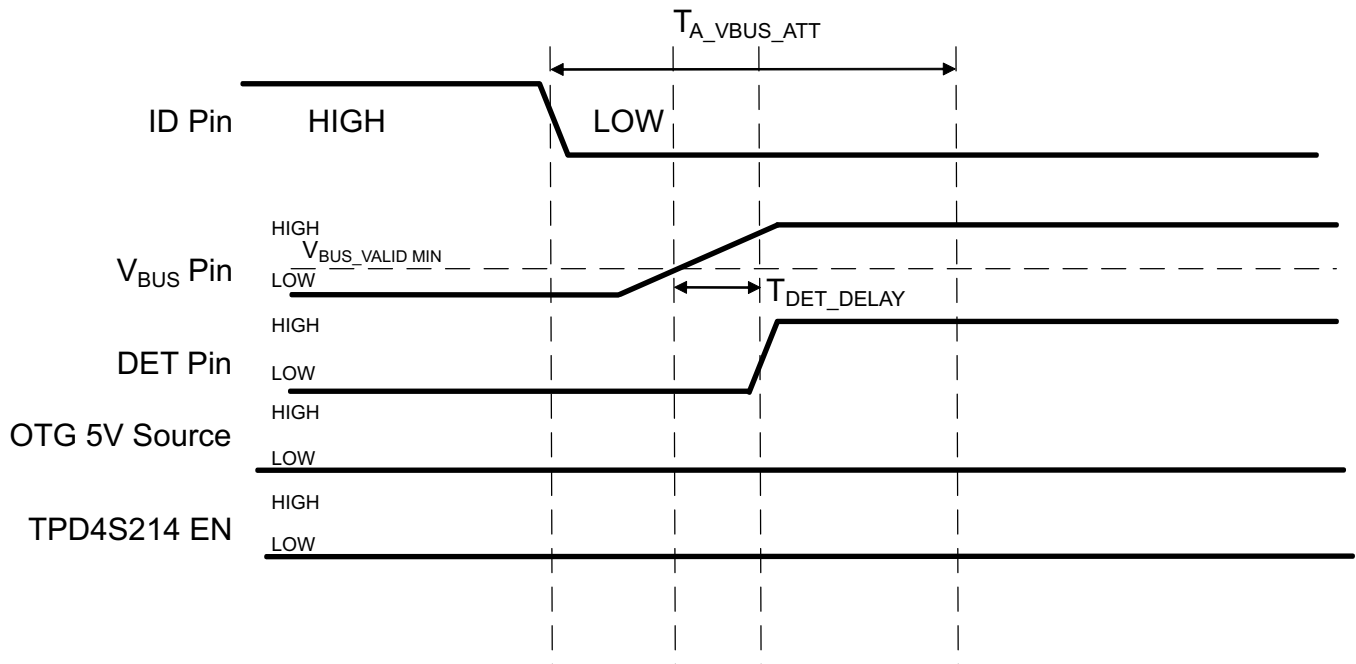
| EN | V _{OTG_IN} (V _{BUS} Detect Power) | V _{BUS} | DET | Condition |
|----|---|--|-----|--|
| X | X | V _{BUS_VALID} ⁻ < V _{BUS} < V _{BUS_VALID} ⁺ | H | V _{BUS} within V _{BUS_VALID} |
| X | X | V _{BUS_VALID} ⁻ > V _{BUS} OR V _{BUS} > V _{BUS_VALID} ⁺ | L | V _{BUS} outside of V _{BUS_VALID} |

X = Don't Care, H = Signal High, and L = Signal Low

[Figure 21](#) and [Figure 22](#) shows suggested system level timing diagrams for detecting V_{BUS} according to [OTG and EH Supplement]. [Figure 28](#) shows the application diagram. In [Figure 21](#), DET pin remains low after ID pin becomes FALSE, indicating there is not an active voltage source on V_{BUS}. The USB controller proceeds to turn on OTG 5-V source and the TPD4S214 respectively; this sequence is recommended because TPD4S214 is powered through the OTG source. After a period of t_{ON}, current starts to flow through the OTG switch and V_{BUS} is ramped to the voltage level of V_{OTG_IN}.


Figure 21. Timing Diagram for Valid USB Device

In [Figure 22](#), DET pin toggles high after an active voltage is detected on V_{BUS} within T_{A_VBUS_ATT}. This indicates that the USB device attached is not suitable for OTG charging and both OTG 5-V source and TPD4S214 remain off.


Figure 22. System Level Timing Diagram for Invalid USB Device

8.3.22 Test Configuration

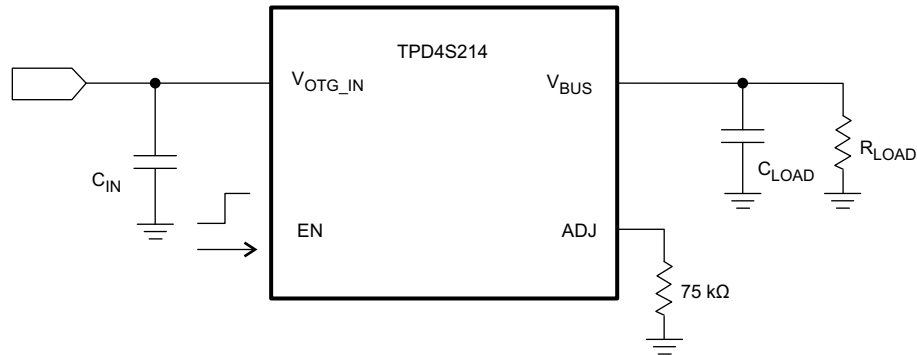


Figure 23. Inrush Current Test Configuration.

Enable is toggled from low to high. See the [Application Information](#) section for C_{IN} and C_{LOAD} value recommendations.

8.4 Device Functional Modes

Table 2. Device Operation

| EN | V_{OTG_IN} | V_{BUS} | OCP | OTP | OTG SW | \overline{FLT} | FAULT CONDITION |
|----|---|---|-----|-----|--------|------------------|-----------------------------|
| X | 0 | 0 | F | F | OFF | L | SW Disabled |
| X | X | X | X | T | OFF | L | Over Temperature |
| H | X | X | T | X | OFF | L | Over Current |
| H | $V_{OTG_IN} > V_{UVLO}$ | $V_{BUS} > V_{OTG_IN}$ | F | F | OFF | L | Reverse-current |
| H | X | $V_{BUS} > V_{OVLO}$ | F | F | OFF | L | V_{BUS} over-voltage |
| H | $V_{OTG_IN} < V_{UVLO}$ | X | F | F | OFF | L | V_{OTG_IN} under-voltage |
| H | $V_{OTG_IN} > V_{BUS}$ and $V_{OTG_IN} > V_{UVLO}$ | $V_{SHORT} < V_{BUS} < V_{OTG_IN}$ and $V_{SHORT} < V_{BUS} < V_{OVLO}$ | F | F | ON | H | Normal (SW Enabled) |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A USB OTG device's one and only connector is the AB receptacle, which accepts either an A or B plug. When an A-plug is inserted, the OTG device is called the A-device and when a B-plug is inserted it is called the B-device. A-device is often times referred to as "Targeted Host" and B-device as "USB peripheral". TPD4S214 supports an OTG device when TPD4S214's system is acting as an A-device and powering the USB interface. The TPD4S214 may also be used in non-OTG applications where it resides on the current source side.

9.2 Typical Application

The TPD4S214 is placed next to the USB connector to provide over voltage, over current, and ESD protection for the OTG 5-V source and USB Controller.

9.2.1 USB 2.0 Without Using On-chip V_{BUS} Detect

An example using TPD4S214 to protect an OTG 5-V source and USB 2.0 Controller is shown below. This USB Controller does not utilize V_{BUS} detection with the DET pin, so DET is tied to GND. TPD4S214 is placed in the transmitter channel immediately adjacent to the USB connector. The D+, D-, ID pins on TPD4S214 are interchangeable so that each can protect either of the D+, D-, ID pins on the USB connector, the naming convention is just a suggestion.

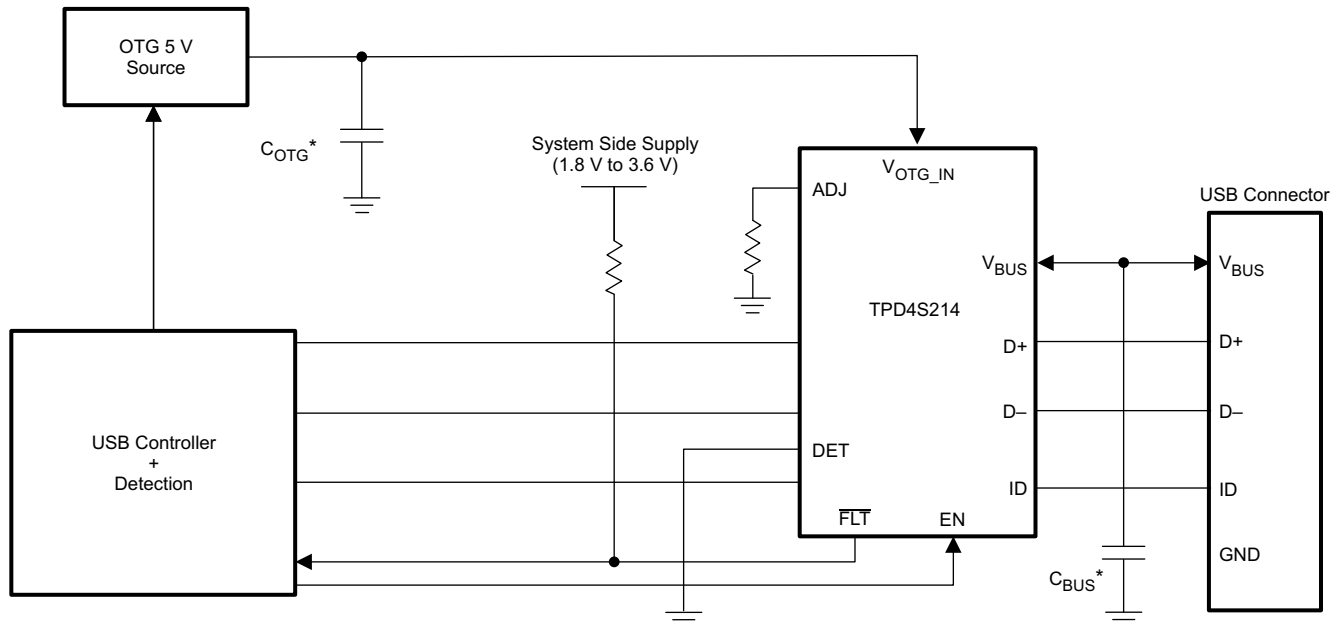


Figure 24. USB2.0 Application Diagram Without Using On-chip V_{BUS} Detect

* C_{OTG} and C_{BUS} have minimum recommended values of 1 μ F each

Typical Application (continued)

9.2.1.1 Design Requirements

For this example, use the following table as input parameters:

| Design Parameters | Example Value |
|-------------------------------------|---|
| Signal range on V _{OTG_IN} | 3.8 V – 5.5 V |
| Signal range on V _{BUS} | 0 V – 5.3 V nominal, withstand -7 V to 30 V |
| I _{BUS_MAX} | 500 mA |
| R _{ADJ} | 100 kΩ |
| Drive EN low (disabled) | 0 V – 0.4 V |
| Drive EN high (enabled) | 1.2 V – 5.5 V |

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the maximum current expected under normal usage. In this example, the maximum expected current is 500 mA so an R_{ADJ} of 100 kΩ was selected to begin current limiting at around 550 mA and protect the OTG system. Fault conditions are monitored by the USB controller by using the FLT Pin. DET is not used and is grounded and can optionally be left floating instead.

9.2.1.3 Application Curves

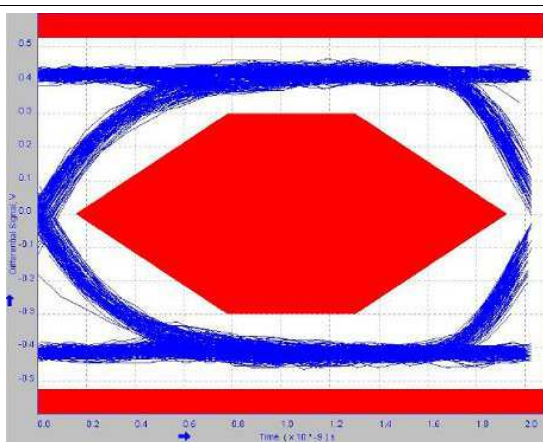


Figure 25. Eye Diagram with no EVM and no IC, Full USB2.0 Speed at 480 Mbps

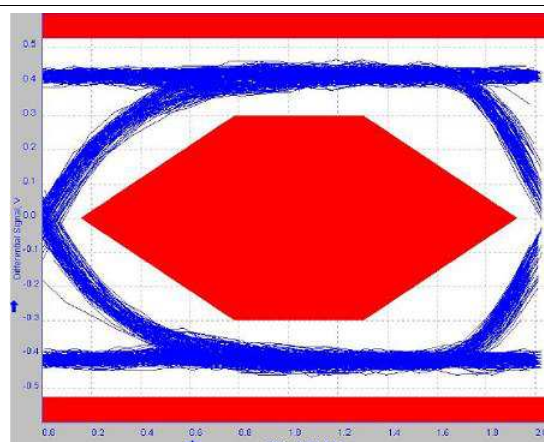


Figure 26. Eye Diagram with TPD4S214EVM but no IC, Full USB2.0 Speed at 480 Mbps

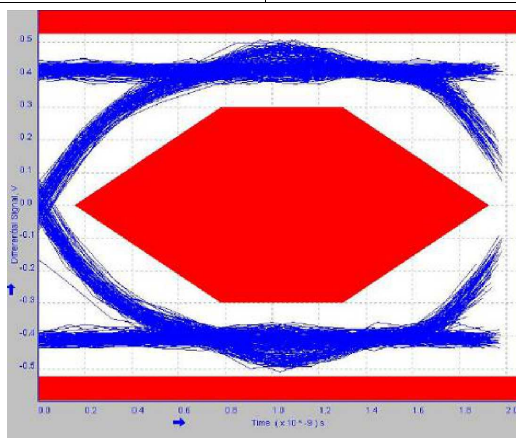


Figure 27. Eye Diagram with TPD4S214EVM and IC, Full USB2.0 Speed at 480 Mbps

9.2.2 USB 2.0 Using On-chip V_{BUS} Detect

An example using TPD4S214 to protect an OTG 5-V source and USB 2.0 Controller is shown below. This USB Controller monitors V_{BUS} detection with the DET pin. This can be advantageous when a peripheral with an Embedded Host is attached. In this case, if there is a valid voltage present on V_{BUS} there is no need to provide OTG power, so the USB Controller can be programmed to disable the OTG 5-V source, resulting in a power savings. The D+, D-, ID pins on TPD4S214 are interchangeable so that each can protect either of the D+, D-, ID pins on the USB connector, the naming convention is just a suggestion.

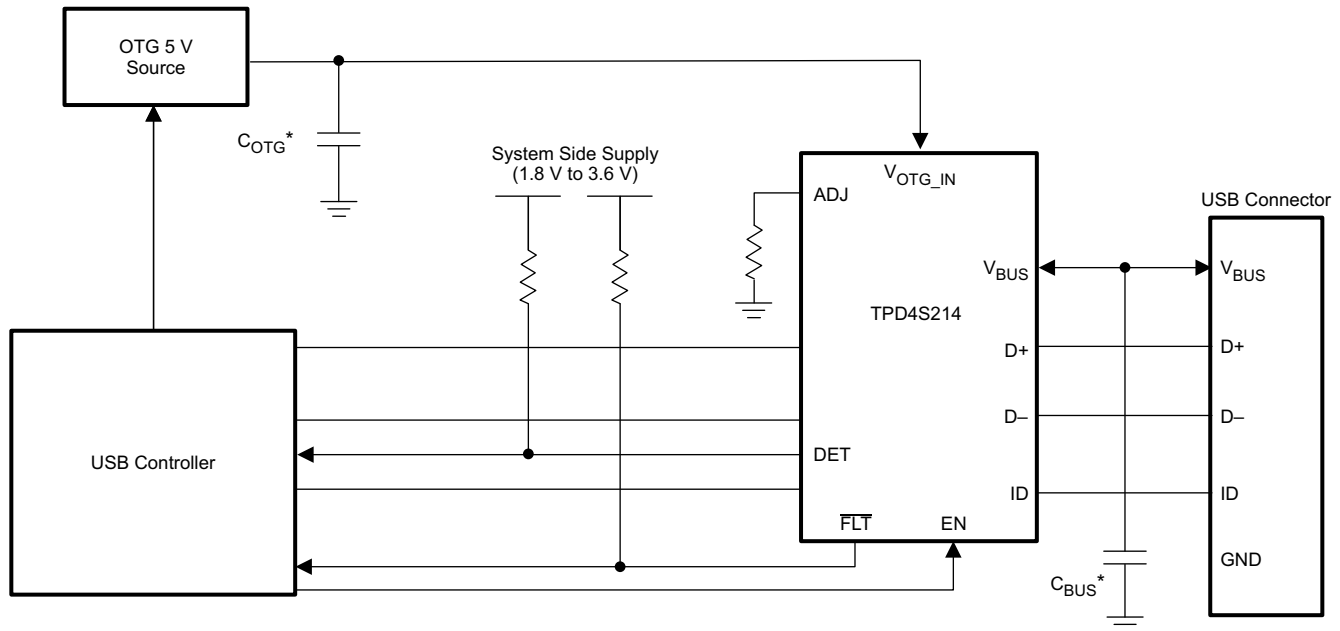


Figure 28. USB 2.0 Application Diagram Using On-chip V_{BUS} Detect

* C_{OTG} and C_{BUS} each have minimum recommended values of 1 μ F

9.2.2.1 Design Requirements

For this example, use the following table as input parameters:

| Design Parameters | Example Value |
|-------------------------------|---|
| Signal range on V_{OTG_IN} | 3.8 V – 5.5 V |
| Signal range on V_{BUS} | 0 V – 5.3 V nominal, withstand –7 V to 30 V |
| I_{BUS_MAX} | 500 mA |
| R_{ADJ} | 100 k Ω |
| Drive EN low (disabled) | 0 V – 0.4 V |
| Drive EN high (enabled) | 1.2 V – 5.5 V |

9.2.2.2 Detailed Design Procedure

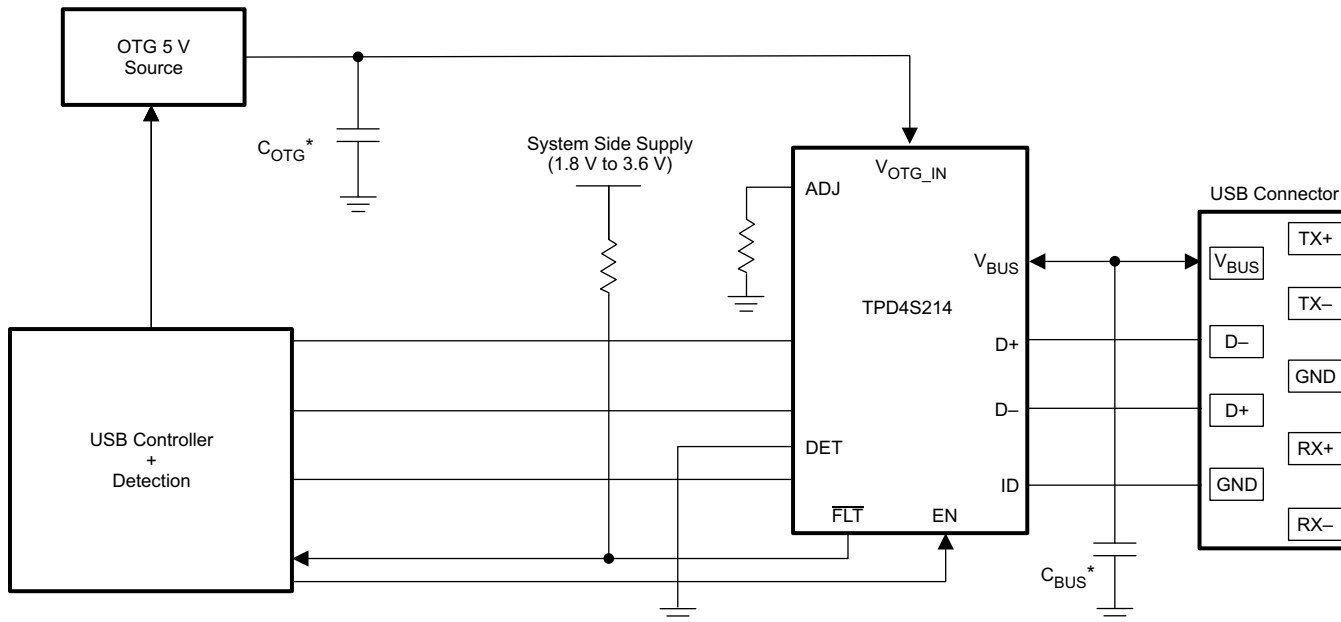
To begin the design process, determine the maximum current expected under normal usage. In this example, the maximum expected current is 500 mA so an R_{ADJ} of 100 k Ω was selected to begin current limiting at around 550 mA and protect the OTG system. Fault conditions are monitored by the USB controller by using the FLT Pin. DET Pin is used to facilitate detecting between a USB host and peripheral device on V_{BUS} .

9.2.2.3 Application Curves

Refer to [Application Curves](#) for related application curves.

9.2.3 USB 3.0 Without Using On-chip V_{BUS} Detect

An example using TPD4S214 to protect an OTG 5-V source and USB 3.0 Controller is shown below. This USB Controller does not utilize V_{BUS} detection with the DET pin, so it is tied to GND. The D+, D-, ID pins on TPD4S214 are interchangeable so that each can protect either of the D+, D-, ID pins on the USB connector, the naming convention is just a suggestion.



*C_{BUS} and C_{OTG} each have minimum recommended values of 1 μF

Figure 29. USB 3.0 Application Diagram Without Using On-chip V_{BUS} Detect

9.2.3.1 Design Requirements

For this example, use the following table as input parameters:

| Design Parameters | Example Value |
|-------------------------------------|---|
| Signal range on V _{OTG_IN} | 3.8 V – 5.5 V |
| Signal range on V _{BUS} | 0 V – 5.3 V nominal, withstand –7 V to 30 V |
| I _{BUS_MAX} | 900 mA |
| R _{ADJ} | 56 kΩ |
| Drive EN low (disabled) | 0 V – 0.4 V |
| Drive EN high (enabled) | 1.2 V – 5.5 V |

9.2.3.2 Detailed Design Procedure

To begin the design process, determine the maximum current expected under normal usage. In this example, the maximum expected current is 900 mA so an R_{ADJ} of 56 kΩ was selected to begin current limiting at around 1 A and protect the OTG system. Fault conditions are monitored by the USB controller by the $\overline{\text{FLT}}$ Pin. DET is not used and is grounded and can optionally be left floating instead.

9.2.3.3 Application Curves

Refer to [Application Curves](#) for related application curves.

10 Power Supply Recommendations

TPD4S214 is designed to receive power from an OTG 5-V power source. It can operate normally (nFET ON) between 3.8 V and 5.55 V. Thus, the power supply (with a ripple of V_{RIPPLE}) requirement for TPD4S214 to be able to switch the nFET ON is between $3.8\text{ V} + V_{RIPPLE}$ and $5.55\text{ V} - V_{RIPPLE}$.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. Therefore, the PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Avoid using VIAs between the connector and an I/O protection pin on TPD4S214.
- Avoid 90° turns in traces.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- Minimize impedance on the path to GND for maximum ESD dissipation.
- The capacitors on V_{BUS} and V_{OTG_IN} should be placed close to their respective pins on TPD4S214.

11.2 Layout Example

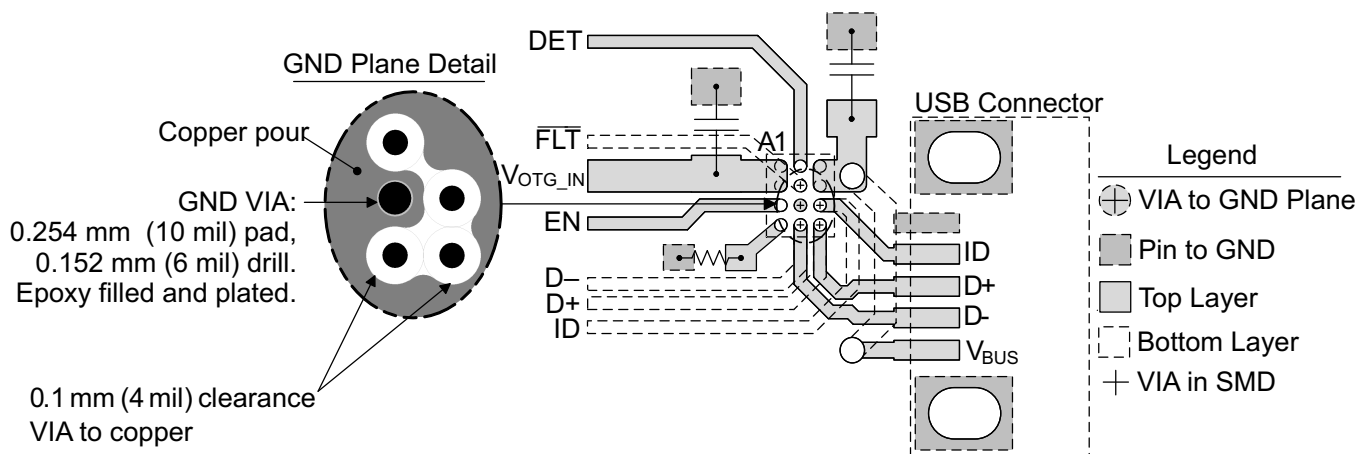


Figure 30. TPD4S214 Layout Example

Successful dissipation of an ESD event is largely dependent on minimizing the impedance along the designated electrical path to ground. For this reason any TVS, including TPD4S214, needs to have the lowest possible impedance to GND. The BGA footprint of this device constrains the path to ground through a VIA in the GND pad of TPD4S214. Due to the "skin effect," maximizing the surface area of the VIA minimizes the impedance of the path to GND. For this reason make both the VIA pad diameter and the VIA drill diameter as large as possible, thus maximizing the surface area of the outside of the VIA surface and the inside of the VIA surface. The GND plane should not be broken in the vicinity of the GND VIA. If possible, attaching the GND VIA to a GND plane on multiple layers minimizes the impedance. The GND VIA should be filled with a non-conductive filler (like epoxy) as opposed to a conductive filler, in order to keep the surface area of the inside of the VIA created by the drill. The GND VIA should be plated over at the SMD pad.

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

OTG 和 EH 补充协议: *USB 版本 2.0 规范的 On-The-Go* 和嵌入式主机补充协议, 2011 年 7 月 14 日。 www.usb.org

12.2 商标

All trademarks are the property of their respective owners.

12.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

12.4 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本, 请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPD4S214YFFR | Active | Production | DSBGA (YFF) 12 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | B3214 |
| TPD4S214YFFR.A | Active | Production | DSBGA (YFF) 12 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | B3214 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPD4S214YFFR | DSBGA | YFF | 12 | 3000 | 180.0 | 8.4 | 1.48 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPD4S214YFFR | DSBGA | YFF | 12 | 3000 | 182.0 | 182.0 | 20.0 |

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月