TPS1H200A-Q1 40V 200mΩ 单通道智能高侧开关

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件人体放电模型 (HBM) 静电防护 (ESD) 分类等级 H2
  - 器件 CDM ESD 分类等级 C4B
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 单通道 200mΩ 智能高侧开关
- 宽工作电压：3.4 V 至 40 V
- 低于 500nA 的超低待机电流
- 可调节电流限制（利用外部电阻器）
  - ≥ 500mA 时为 ±15%
  - ≥ 1.5A 时为 ±10%
- 可配置电流限制后的行为
  - “保持”模式
  - “闭锁”模式（具有可调节的延迟时间）
  - “自动重试”模式
- 支持独立操作（无需 MCU）
- 保护：
  - 接地短路和过载保护
  - 热关断和热振荡
  - 用于电感负载的负电压钳位
  - 接地失效保护和失电保护
- 诊断：
  - 过载和接地短路检测
  - 开路负载和电池短路检测（开启或关闭状态下）
  - 热关断和热振荡

2 应用

- 车身照明
- 信息娱乐系统
- 高级驾驶辅助系统 (ADAS)
- 单通道高侧子模块开关
- 一般阻性、感性和容性负载

3 说明

TPS1H200A-Q1 器件是受到全面保护的单通道高侧电源开关，具有集成式 200mΩ NMOS 功率 FET。

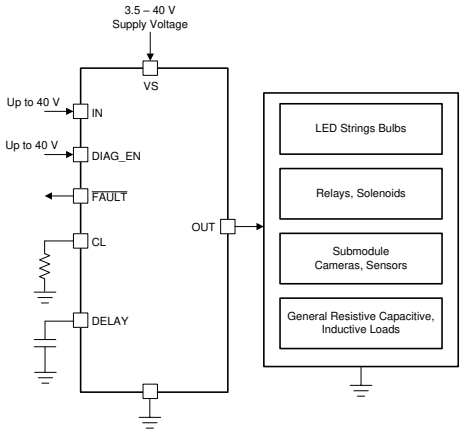
可调节电流限制可通过限制浪涌或过载电流来提高系统可靠性。高精度电流限制可增强过载保护，从而简化前沿电源设计。除了电流限制之外，其他可配置特性还能够在功能、成本和热耗散方面提供设计灵活性。

该器件支持对数字状态输出进行全面诊断。在开启和关闭状态下皆可进行开路负载检测。无论是否有 MCU，该器件都能正常工作。独立模式允许隔离型系统使用此器件。

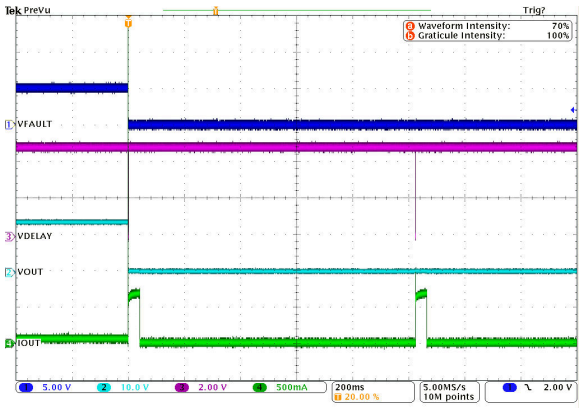
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS1H200A-Q1	HVSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



典型方框图



自动重试模式下的电流限制保护

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (December 2019) to Revision D (September 2021)	Page
• Changed the nominal operating current ($I_{(OP)}$) V_{DIAG_EN} variable to "X" for do not care in the *Electrical Characteristics* table	6

Changes from Revision B (December 2019) to Revision C (December 2019)	Page
• 向*特性* 部分添加了“提供功能安全”	1

Changes from Revision A (April 2018) to Revision B (December 2019)	Page
• Changed the Logic high-level voltage from 2 V to 1.8 V in the *Electrical Characteristics* table	6
• Changed the IN and DIAG_EN from high to low in the *Standby Mode* section	24

Changes from Revision * (February 2018) to Revision A (April 2018)	Page
• 将数据表状态从“预告信息”更改为“生产数据”	1

5 Pin Configuration and Functions

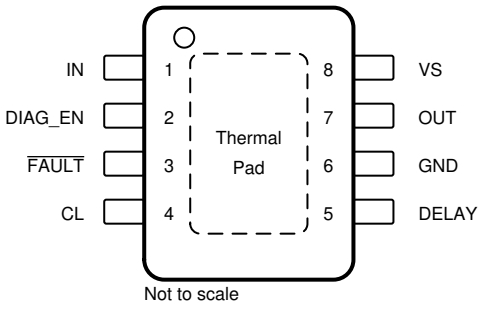


图 5-1. DGN PowerPAD™ Package 8-Pin HVSSOP With Exposed Thermal Pad Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CL	4	O	Adjustable current limit. Connect to device GND if external current limit is not used.
DELAY	5	I/O	Function configuration when current limit; internal pullup
DIAG_EN	2	I	Enable the diagnostic function
$\overline{\text{FAULT}}$	3	O	Open-drain diagnostic status output. Leave floating if not used.
GND	6	—	Ground
IN	1	I	Input control for output activation; internal pulldown
OUT	7	O	Output, source of the high-side switch, connected to the load
VS	8	I	Power supply, drain for the high-side switch
Thermal pad	—	—	Thermal pad. Connect to device GND or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage VS pin	t < 400 ms	—	42	V
Reverse polarity voltage (3)	t < 1 minute	– 36	—	V
Current on GND	t < 2 minutes	– 100	250	mA
Voltage on IN and DIAG_EN pins		– 0.3	VS	V
Current on IN and DIAG_EN pins		– 10	—	mA
Voltage on DELAY pin		– 0.3	7	V
Current on DELAY pin		– 60	—	mA
Voltage on $\overline{\text{FAULT}}$ pin		– 0.3	7	V
Current on $\overline{\text{FAULT}}$ pin		– 30	10	mA
Voltage on CL pin		– 0.3	7	V
Current on CL pin		—	6	mA
Voltage on OUT pin		—	42	V
Inductive load switch-off energy dissipation single pulse(4)		—	40	mJ
Operating junction temperature, T_J		– 40	150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.
(3) Reverse polarity condition: V_{IN} = 0 V, reverse current < $I_{R(2)}$, GND pin 1-kΩ resistor in parallel with diode.
(4) Test condition: V_{VS} = 13.5 V, L = 8 mH, T_J = 150°C. FR4 2s2p board, 2 × 70-µm Cu, 2 × 35-µm Cu. 600 mm^2 thermal pad copper area.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except VS, OUT, and GND	±2000	V
			Pins VS, OUT, and GND	±3000	
		Charged-device model (CDM), per AEC Q100-011		±750	

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Operating voltage	4	40	V
	Voltage on IN and DIAG_EN pins	0	40	V
	Voltage on $\overline{\text{FAULT}}$ pin	0	5	V
$I_{o,nom}$	Nominal DC load current	0	2.5	A
T_J	Operating junction temperature	– 40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS1H200A-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{VS(nom)}$	Nominal operating voltage		4		40	V
$V_{VS(uvr)}$	Undervoltage restart	V_{VS} rising	3.5	3.7	4	V
$V_{VS(uvf)}$	Undervoltage shutdown	V_{VS} falling	3	3.2	3.4	V
$V_{(uv,hys)}$	Undervoltage shutdown, hysteresis			0.5		V
OPERATING CURRENT						
$I_{(op)}$	Nominal operating current	V_{VS} = 13.5 V, V_{IN} = 5 V V_{DIAG_EN} = X V, I_{OUT} = 0.5 A I_{CL} = 2 A			5	mA
$I_{(off)}$	Standby current	V_{VS} = 13.5 V V_{IN} = V_{DIAG_EN} = V_{CL} = V_{OUT} = 0 V T_J = 25°C			0.5	µA
		V_{VS} = 13.5 V V_{IN} = V_{DIAG_EN} = V_{CL} = V_{OUT} = 0 V T_J = 125°C			3	
$I_{(off,diag)}$	Standby current with diagnostics enabled	V_{VS} = 13.5 V V_{IN} = 0 V, V_{DIAG_EN} = 5 V			3	mA
$t_{(off,deg)}$	Standby-mode deglitch time(1)	IN from high to low if deglitch time ⩾ $t_{(off,deg)}$, then the device enters into standby mode.		12.5		ms
$I_{lkg(out)}$	Output leakage current in OFF state	V_{VS} = 13.5 V V_{IN} = V_{DIAG_EN} = V_{OUT} = 0 V			3	µA
POWER STAGE						
$r_{DS(on)}$	ON state resistance	V_{VS} ⩾ 3.5 V, T_J = 25°C		200		mΩ
		V_{VS} ⩾ 3.5 V, T_J = 150°C			400	
$I_{CL(int)}$	Internal current limit	CL pin connected to GND	3.5	4.8	6	A
$I_{CL(TSD)}$	Current-limit value percentage during thermal shutdown			60%		
$V_{DS(clamp)}$	Drain−to−source voltage internally clamped		45		65	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain−to-source diode voltage	IN = 0, I_{OUT} = −0.15 A	0.3	0.7	1	V
$I_{R(1)}$	Continuous reverse current from source to drain during a short-to-battery condition(1)	t < 60 s, V_{IN}= 0 V, T_J = 25°C.			2	A
$I_{R(2)}$	Continuous reverse current from source to drain during a reverse-polarity condition(1)	t < 60 s, V_{IN}= 0 V, T_J = 25°C GND pin 1-kΩ resistor in parallel with diode.			2	A
LOGIC INPUT (IN, DIAG_EN)						
V_{IH}	Logic high-level voltage		1.8			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{pd,in}$	Logic-pin pulldown resistor	IN. V_{IN} = 5 V	150		400	kΩ
		DIAG_EN. V_{VS} = V_{DIAG_EN} = 5 V	350		850	
DIAGNOSTICS						
$I_{lkg(loss,GND)}$	Loss of ground output leakage current				100	µA
$t_{d(ol,on)}$	Open-load deglitch time in ON state	V_{IN} = 5 V, V_{DIAG_EN} = 5 V when I_{OUT} < $I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$, open load is detected.	200	300	450	µs

6.5 Electrical Characteristics (continued)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(ol,on)}$	Open-load detection threshold in ON state	V_{IN} = 5 V, V_{DIAG_EN} = 5 V when $I_{OUT} < I_{(ol,on)}$ duration longer than $t_{d(ol,on)}$ open load is detected.		10	20	mA
$V_{(ol,off)}$	Open-load detection threshold in OFF state	V_{IN} = 0 V, V_{DIAG_EN} = 5 V when $V_{VS} - V_{OUT} < V_{(ol,off)}$ duration longer than $t_{d(ol,off)}$ open load is detected.	1.4		2.6	V
$t_{d(ol,off)}$	Open-load deglitch time in OFF state	V_{IN} = 0 V, V_{DIAG_EN} = 5 V when $V_{VS} - V_{OUT} < V_{(ol,off)}$ duration longer than $t_{d(ol,off)}$ open load is detected.	200	300	450	µs
$I_{(ol,off)}$	OFF state output sink current	V_{IN} = 0 V, V_{DIAG_EN} = 5 V $V_{VS} = V_{OUT}$ = 13.5 V	–75			µA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ low output voltage	$I_{\overline{FAULT}}$ = 2 mA			0.2	V
$t_{\overline{FAULT}}$	$\overline{FAULT}$ signal holding time(1)			8.5		ms
$T_{(SD)}$	Thermal shutdown threshold(1)			175		°C
$T_{(SD,rst)}$	Thermal shutdown status reset(1)			155		°C
$T_{(sw)}$	Thermal swing shutdown threshold(1)			60		°C
$T_{(hys)}$	Hysterisis for resetting the thermal shutdown and swing(1)			10		°C
CURRENT LIMIT AND DELAY CONFIGURATION						
$K_{(CL)}$	Current-limit current ratio(1)			2500		
$V_{CL(th)}$	Current-limit internal threshold voltage(1)			0.8		V
$dK_{(CL)} / K_{(CL)}$	External current limit accuracy $(I_{OUT} - I_{CL} \times K_{(CL)} \times 100 / (I_{CL} \times K_{(CL)})$	$I_{limit} \geq$ 0.25 A, $V_{VS} - V_{OUT} \geq$ 2.5 V	–20%		20%	
		$I_{limit} \geq$ 0.5 A, $V_{VS} - V_{OUT} \geq$ 2.5 V	–15%		15%	
		$I_{limit} \geq$ 1.5 A, I_{limit} < 5 A $V_{VS} - V_{OUT} \geq$ 2.5 V	–10%		10%	
$I_{dl(chg)}$	Delay pin charging current in latch-off mode(1)			4.5		µA
$V_{dl(th)}$	Pulling up threshold in auto-retry mode		2.7			V
$V_{dl(ref)}$	Internal reference voltage in latch-off mode			1.45		V
t_{dl1}	Internal fixed delay time(1)		300	400	500	µs
t_{dl2}	Adjustable delay time by external capacitor on DELAY pin(1)	Connect with 3.3 µF capacitor as the maximum value.			1000	ms
$t_{CL(deg)}$	Deglitch time when current limit (1)	IN low to high or IN keeps high but thermal shutdown recovery, V_{DIAG_EN} = 5 V the deglitch time from IN rising edge to FAULT reporting out.	300		550	µs
		IN keeps high, V_{DIAG_EN} = 5 V the deglitch time from CL start-point to FAULT reporting out.	80		200	
$t_{hic(on)}$	On-time when in auto-retry mode(1)		35	40	45	ms
$t_{hic(off)}$	Off-time when in auto-retry mode(1)		0.8	1	1.2	s

(1) Value specified by design, not subject to production test.

6.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turnon delay time IN rising edge to 10% of V_{OUT} (1)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	20	50	90	µs
$t_{d(off)}$	Turnoff delay time IN falling edge to 90% of V_{OUT} (1)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	20	50	90	µs
$dV/dt_{(on)}$	Slew rate on V_{OUT} from 10% to 90% (1)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	0.1	0.3	0.6	V/µs
$dV/dt_{(off)}$	Slew rate off V_{OUT} from 90% to 10% (1)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	0.1	0.35	0.6	V/µs

(1) Value specified by design, not subject to production test.

6.7 Typical Characteristics

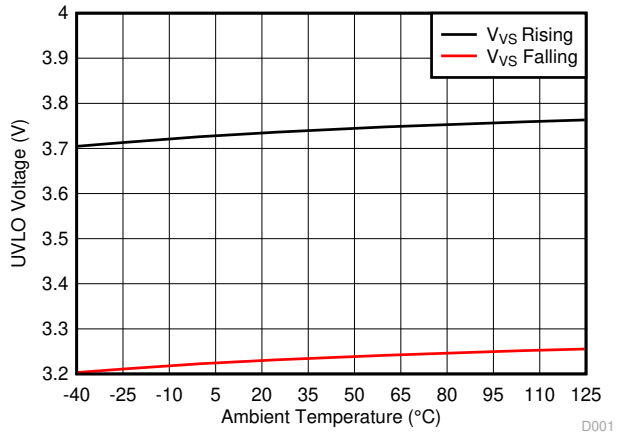


图 6-1. UVLO Voltage Threshold

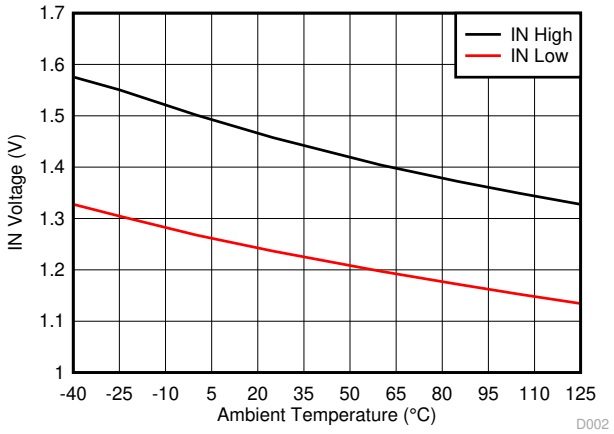


图 6-2. IN Voltage Threshold

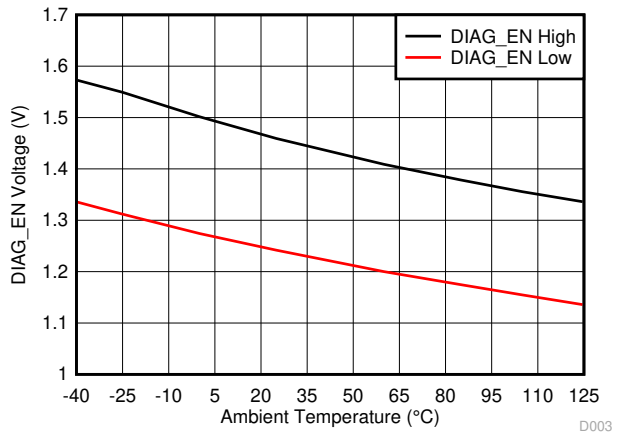


图 6-3. DIAG_EN Voltage Threshold

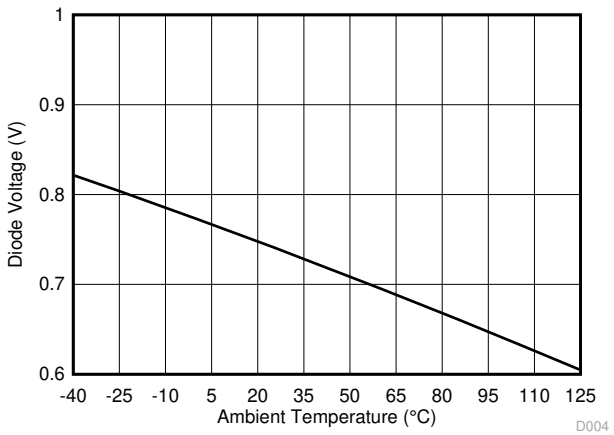


图 6-4. Body-Diode Forward Voltage

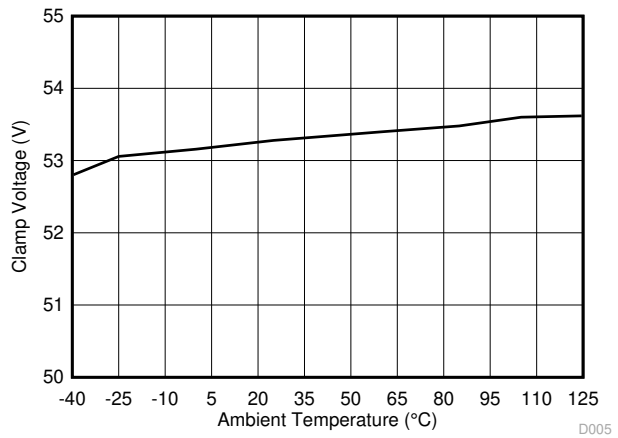


图 6-5. Drain-to-Source Clamp Voltage

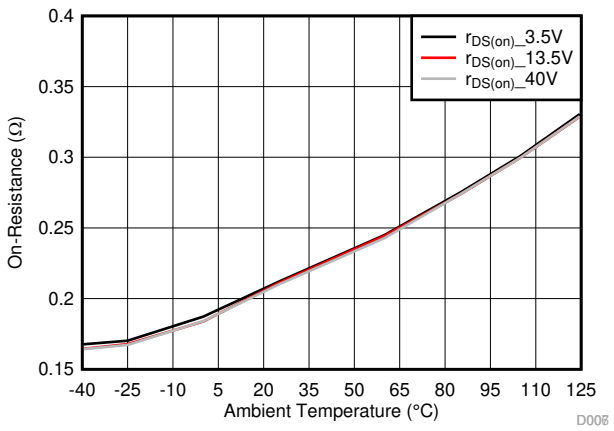


图 6-6. FET On-Resistance

6.7 Typical Characteristics (continued)

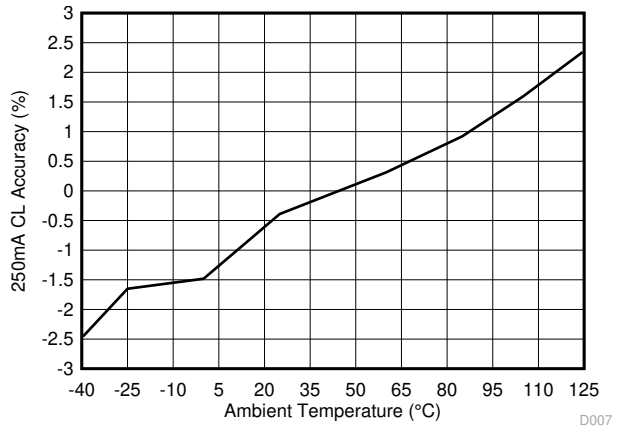


图 6-7. Current-Limit Accuracy at 250 mA

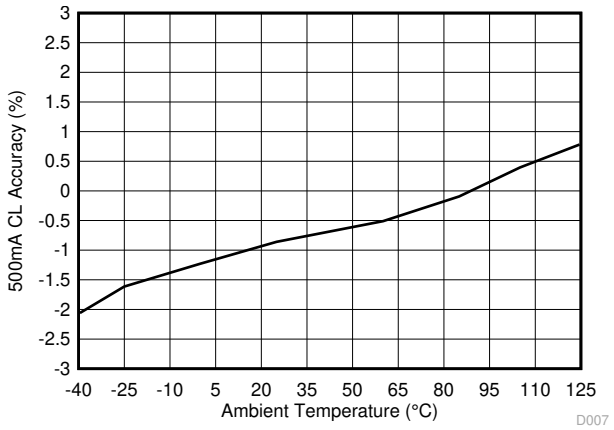


图 6-8. Current-Limit Accuracy at 500 mA

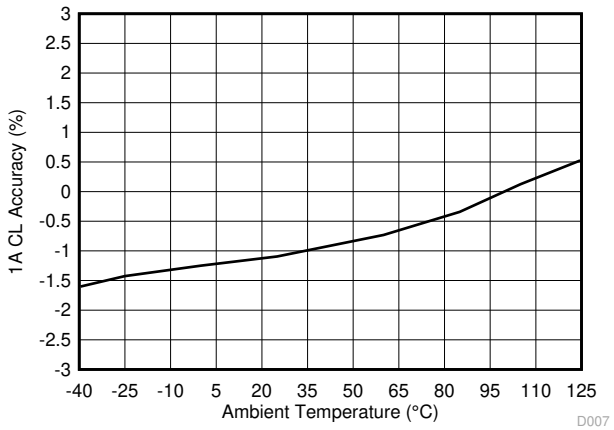


图 6-9. Current-Limit Accuracy at 1 A

7 Detailed Description

7.1 Overview

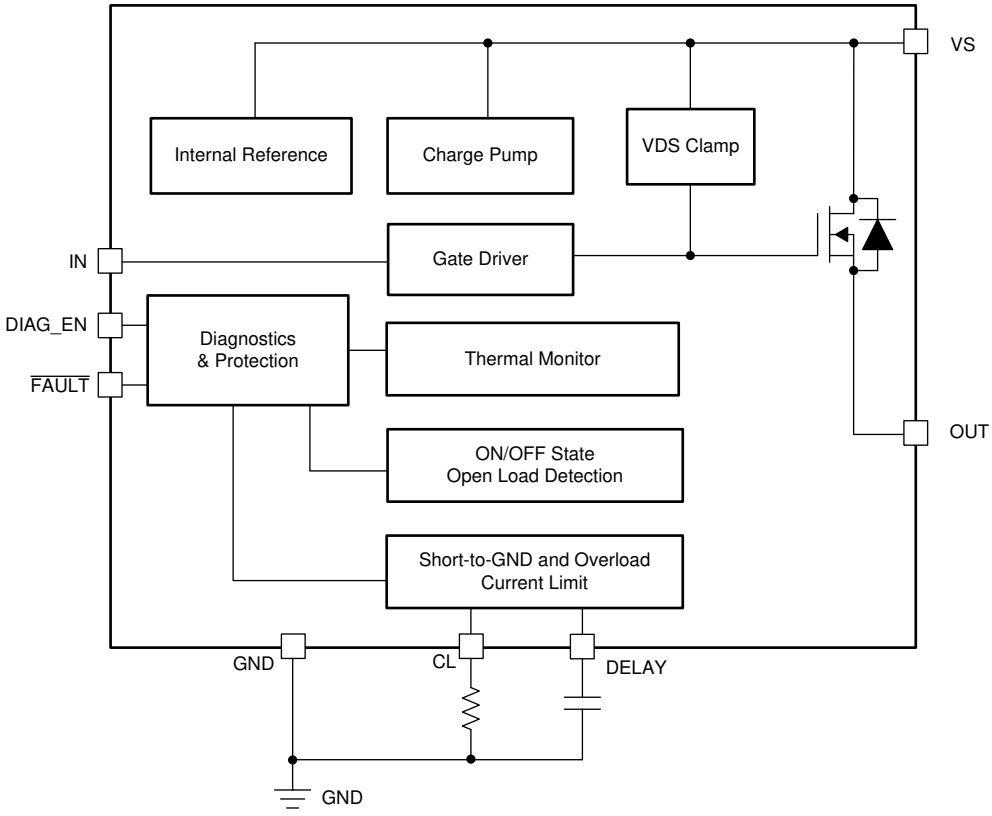
The TPS1H200A-Q1 device is a smart high-side switch with an internal charge pump and single-channel integrated NMOS power FET. The adjustable current limit function improves the reliability of the whole system. Full diagnostic features enable intelligent control of the load.

The external high-accuracy current limit sets the current limit value for the application. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device saves system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. The TPS1H200A-Q1 device allows three modes when a current limit occurs. Users can set the output to consistently hold the current, to immediately latch off, or to automatically retry through the configuration on the DELAY pin. The configurable behaviors during a current limit provide design flexibility. This includes functionality, cost, and thermal dissipation.

This device supports full diagnostics with the digital status output. High-accuracy and low-threshold open-load detection enables real-time ON state monitoring. The device supports operation without an MCU (stand-alone mode) which allows the system to locally implement full functionality.

The TPS1H200A-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including LEDs, bulbs, relays, solenoids, and submodules.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current limit

A high-accuracy current limit allows high reliability of the design. The current limit protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current limit threshold is hit, a closed loop immediately activates. The output current is clamped at the set value, and a fault is reported. The device heats up because of high power dissipation on the power FET.

The device has two current limit thresholds.

- Internal current limit: The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit: An external resistor is used to set the current limit threshold. Use 方程式 1 to calculate $R_{(CL)}$. The external adjustable current limit allows the flexibility to set the current limit value by application.

$$R_{CL} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \quad (1)$$

where

- $V_{CL(th)}$ is the internal band-gap voltage.
- $K_{(CL)}$ is the ratio of the output current and the current limit set value.
- $K_{(CL)}$ is constant across temperature and supply voltage.

Note

When a GND network is used, that causes a level shift between the device GND and board GND, so the CL pin must be connected to the device GND.

For better protection from a hard short-to-GND condition (when the IN pin is enabled, a short-to-GND occurs suddenly), the device will implement a fast-trip protection to turn off the output before the current limit closed loop is set up. Typically, the fast-trip response time is less than 1 µs. With a fast response like this, the device can achieve a better inrush current-suppression performance.

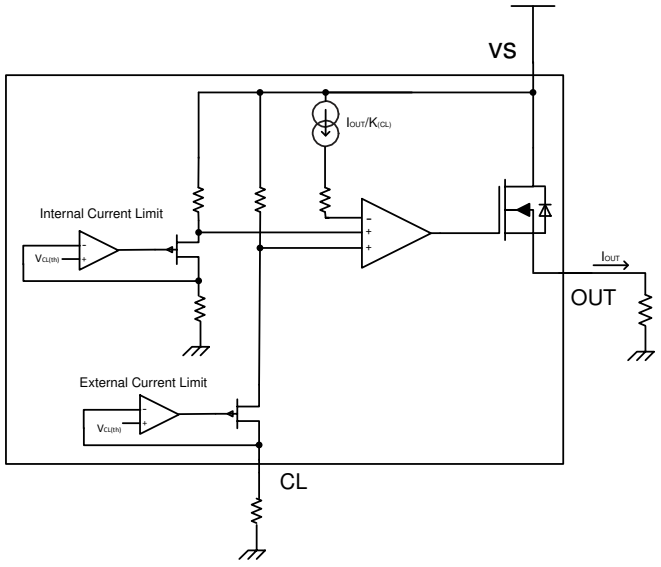


图 7-1. Current Limit

7.3.2 DELAY Pin Configuration

When a current limit occurs, the TPS1H200A-Q1 device supports three different outcomes of the output. 表 7-1 lists the current limit configurations and these outcomes behaviors.

表 7-1. Current Limit Configurations

MODE	DELAY CONFIGURATION	OUTPUT CURRENT BEHAVIOR	$\overline{\text{FAULT}}$ RECOVERY
Holding	Connects to GND directly	When hitting a current limit, the output current holds at the setting current. The device enters into thermal shutdown mode when $T_J > T_{(SD)}$.	$\overline{\text{FAULT}}$ clears when IN turns low for a duration of time longer than $t_{\overline{\text{FAULT}}}$ or when the current limit is removed when IN is high.
Latch-off	Connects to GND through a capacitor	When hitting a current limit, the output current holds at the setting current, but latches off after a preset DELAY time (t_{dl1}+ t_{dl2}). t_{dl1} is the default delay time, and t_{dl2} is a capacitor-configurable delay time. The output stays latched off regardless of whether the current limit is removed. The output recovers only when IN is toggling.	$\overline{\text{FAULT}}$ clears when IN turns low for a duration of time longer than $t_{\overline{\text{FAULT}}}$.
Auto-retry	External pullup	When hitting a current limit, the output current holds at the setting current, but periodically comes on for $t_{hic(on)}$ and turns off for $t_{hic(off)}$.	$\overline{\text{FAULT}}$ clears when IN turns low for a duration of time longer than $t_{\overline{\text{FAULT}}}$ OR when the current limit is removed for $t_{hic(on)}$.

7.3.2.1 Holding Mode

Holding mode is active when the DELAY pin connects directly to GND. When a current limit is reached, the output current holds at the setting current. The device then enters thermal shutdown mode when $T_J > T_{(SD)}$.

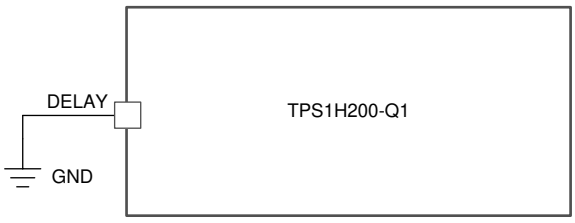


图 7-2. Holding Mode Connection

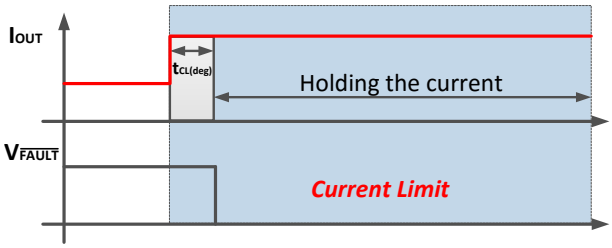


图 7-3. Holding Mode Example

7.3.2.2 Latch-Off Mode

Latch-off mode is active when the DELAY pin connects to GND through a capacitor. When a current limit is reached, the output current holds at the setting current, but latches off after a preset DELAY time (t_{dl1}+ t_{dl2}). t_{dl1} is the default delay time, and t_{dl2} is a configurable delay time set by a capacitor. Regardless of whether the current limit is removed or not, the output remains latched off. The output only recovers when IN is toggling.

t_{dl2} can be calculated by 方程式 2.

$$C_{DELAY} = \frac{I_{dl(chg)} \times t_{dl2}}{V_{dl(ref)}} \quad (2)$$

where

- C_{DELAY} is the capacitor connected on the DELAY pin.
- The $I_{dl(chg)}$ is the device that charges the current in latch-off mode.
- t_{dl2} is the user-setting delay time.
- $V_{dl(ref)}$ is the internal reference voltage in latch-off mode.

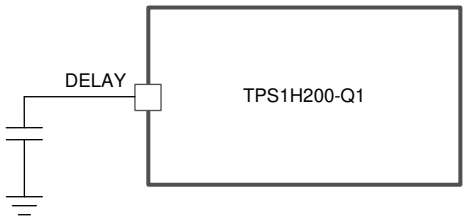


图 7-4. Latch-Off-Mode Connection

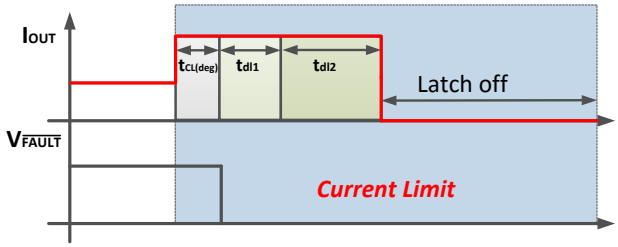


图 7-5. Latch-Off-Mode Example

7.3.2.3 Auto-Retry Mode

Auto-retry mode is active when the DELAY pin is externally pulled up. The pullup voltage must be higher than $V_{dl(th)}$. When the current limit is reached, the output current holds at the setting current, but periodically turns on for $t_{hic(on)}$ and turns off for $t_{hic(off)}$. The device checks the current limit status at the falling edge of $t_{hic(on)}$ clock. If current limit status is captured, the device shuts down for $t_{hic(off)}$. If the current limit status is not captured because of the off window during the thermal conditions, the device keeps turning on for additional $t_{hic(on)}$ or more until the current limit status is captured.

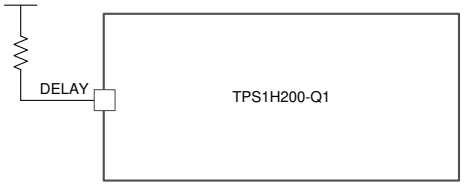


图 7-6. Auto-Retry-Mode Connection

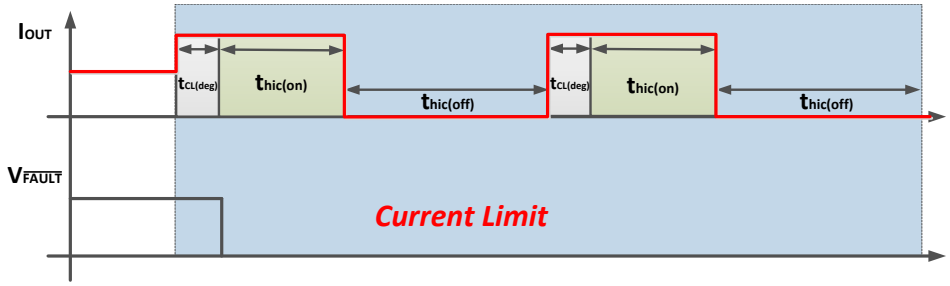


图 7-7. Auto-Retry-Mode Example

7.3.3 Stand-alone Operation

In a typical application, the TPS1H200A-Q1 device is controlled by a microcontroller. The device also supports stand-alone operation. IN and DIAG_EN have a 40-V maximum DC rating, and can be connected to the VS pin directly. When in auto-retry mode, the DELAY pin is connected to the VS pin through a 100-kΩ resistor.

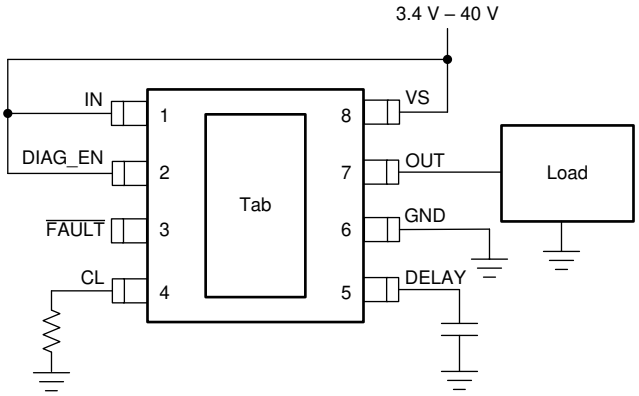


图 7-8. Stand-Alone Operation in Latch-Off Mode

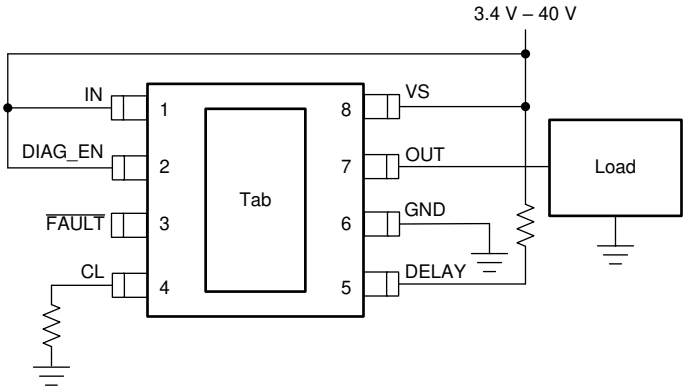


图 7-9. Stand-Alone Operation in Auto-Retry Mode

7.3.4 Fault Truth Table

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the microcontroller uses GPIOs to set DIAG_EN high to enable the diagnostics of one device, and disables the diagnostics of the other devices by setting DIAG_EN low. Additionally, the device can keep power consumption to a minimum by setting DIAG_EN and IN low.

表 7-2 applies when the DIAG_EN pin is enabled, and 表 7-3 applies when the DIAG_EN pin is disabled.

表 7-2. Fault Truth Table

CONDITION	IN	OUT	CRITERION	$\overline{\text{FAULT}}$	FAULT RECOVERY
Normal	L	L	N/A	H	N/A
	H	H	N/A	H	
Overload or short to GND	H	L	current limit triggered	L	See 表 7-1.
Open load or short to battery	H	H	$I_{OUT} < I_{(ol,on)}$	L	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{\text{FAULT}}}$. OR $\overline{\text{FAULT}}$ clears when the open load is removed.
	L(1)	H	$V_{VS} - V_{OUT} < V_{(ol,off)}$	L	$\overline{\text{FAULT}}$ clears when IN is toggling OR $\overline{\text{FAULT}}$ clears when the open load is removed.
Thermal shutdown	H	N/A	Thermal shutdown triggered	L	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{\text{FAULT}}}$. OR $\overline{\text{FAULT}}$ clears when thermal shutdown quits.
Thermal swing	H	N/A	Thermal swing triggered	L	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{\text{FAULT}}}$. OR $\overline{\text{FAULT}}$ clears when thermal swing quits.

(1) An external pullup is required for open-load detection.

表 7-3. DIAG_EN Disabled Condition

DIAG_EN	IN CONDITION	PROTECTIONS AND DIAGNOSTICS
LOW	ON	Diagnostics disabled, full protections
	OFF	Diagnostics disabled, no protection

7.3.5 Full Diagnostics

7.3.5.1 Short-to-GND and Overload Detection

When the output is on, a short-to-GND or overload condition causes an overcurrent. If the overcurrent triggers the internal or external current limit threshold, the fault condition is reported as $\overline{\text{FAULT}}$ pin = low.

7.3.5.2 Open-Load Detection

7.3.5.2.1 Output On

When the output is on, the device recognizes an open-load fault if the current flowing through the output I_{OUT} < $I_{(ol,on)}$. For open-load detection when output is on, no external circuitry is required.

7.3.5.2.2 Output Off

When the output is off, the output is pulled down to GND if a load is connected. But if an open load occurs, the output voltage is close to the supply voltage (V_{VS} – V_{OUT} < $V_{(ol,off)}$), and the device recognizes an open-load fault.

There is always a leakage current $I_{(ol,off)}$ on the output due to the internal logic control path or external humidity, corrosion, and so forth. As a result, TI recommends using an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 15 kΩ.

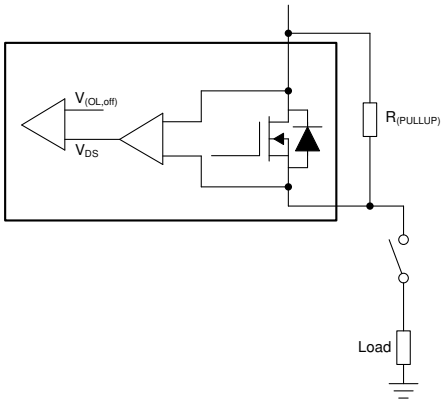


图 7-10. Open-Load Detection in Output OFF State

7.3.5.3 Short-to-Battery Detection

Short-to-battery has the same detection mechanism and behavior as open-load detection in the ON state and the OFF state.

7.3.5.4 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing).

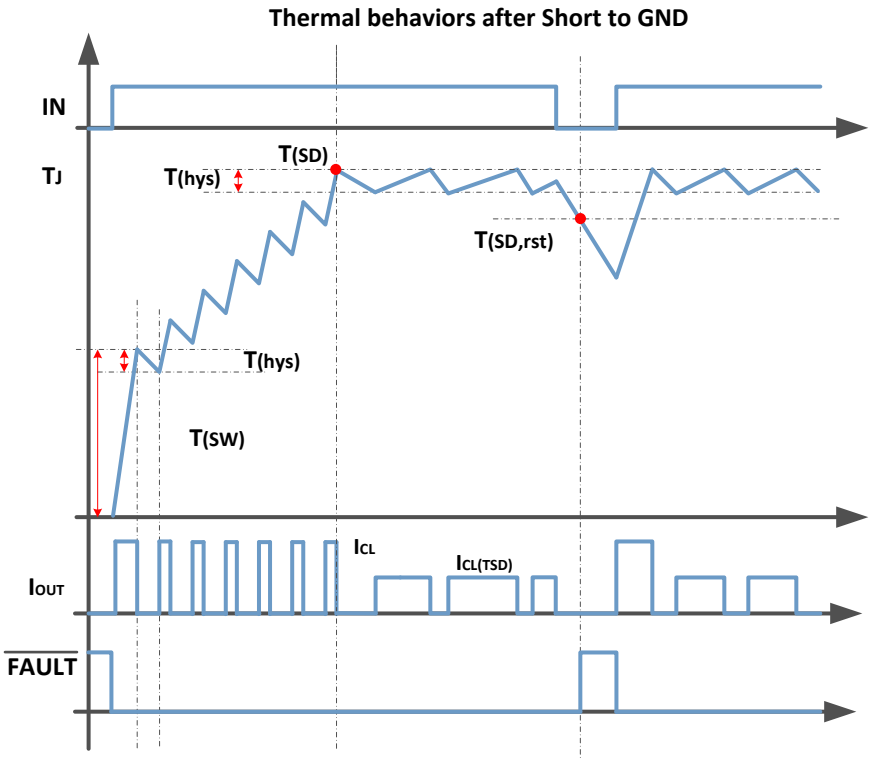


图 7-11. Thermal Behavior Diagram

7.3.5.4.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thermal shutdown occurs, the output turns off.

7.3.5.4.2 Thermal Swing

Thermal swing activates when the power FET temperature sharply increases, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. The thermal swing function improves the reliability of the device when subjected to repetitively fast thermal variation.

7.3.5.4.3 Fault Report Holding

When using PWM dimming, $\overline{\text{FAULT}}$ is easily cleared by the PWM falling edge. Even if the fault condition remains all the time, FAULT is discontinuous. To avoid this unexpected fault report behavior, the device implements fault report holding time. 图 7-12 shows an issue that typically occurs during PWM dimming, the $\overline{\text{FAULT}}$ is cleared unexpectedly even when the short-to-GND still exists. The TPS1H200A-Q1 device with fault-report holding function allows the right behavior as shown in 图 7-13.

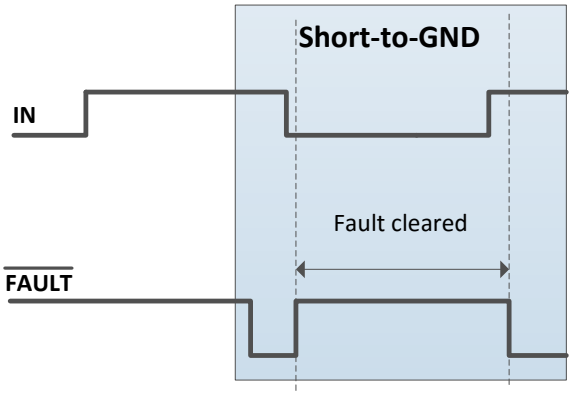


图 7-12. Without Fault-Report Holding

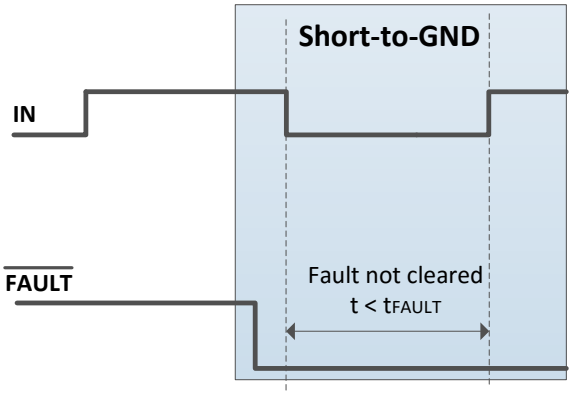


图 7-13. With Fault-Report Holding

7.3.6 Full Protections

7.3.6.1 UVLO Protection

The device monitors the supply voltage, V_{VS}, to prevent unpredicted behaviors when V_{VS} is too low. When V_{VS} drops down to $V_{VS(uvf)}$, the device shuts down. When V_{VS} rises up to $V_{VS(uvr)}$, the device turns on.

7.3.6.2 Inductive Load Switching Off Clamp

When an inductive load is switched off, the inductive reactance pulls the output voltage negative. However, excessive negative voltage can cause the power FET to break down. To protect the power FET from breaking down, an internal clamp ($V_{DS(clamp)}$) is implemented.

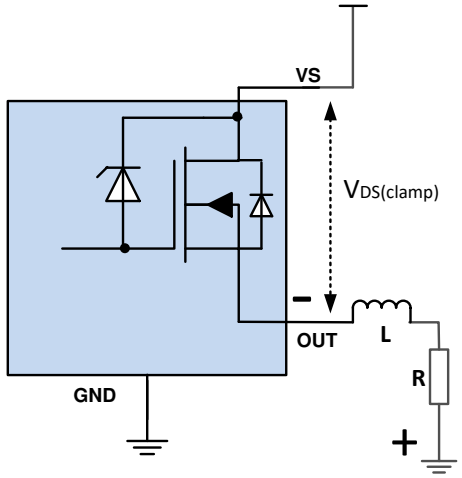


图 7-14. Drain-to-Source Clamping Structure

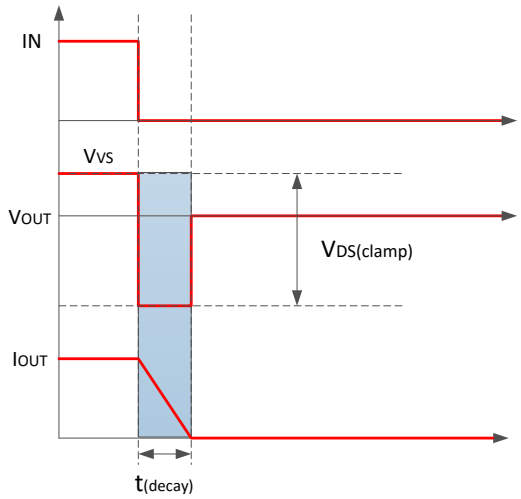


图 7-15. Inductive-Load Switching-Off Diagram

7.3.6.3 Loss-of-GND Protection

When a loss-of-GND occurs, the output shuts down, regardless of whether the IN pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

7.3.6.4 Loss-of-Power-Supply Protection

When a loss-of-power-supply occurs, the output shuts down, regardless of whether the IN pin is high or low. For a resistive or a capacitive load, the loss-of-power-supply has no risk. But for a charged inductive load, the current is driven from all the logic control pins to maintain the inductance current. To protect the system in this condition, TI recommends protection with an external free-wheeling diode.

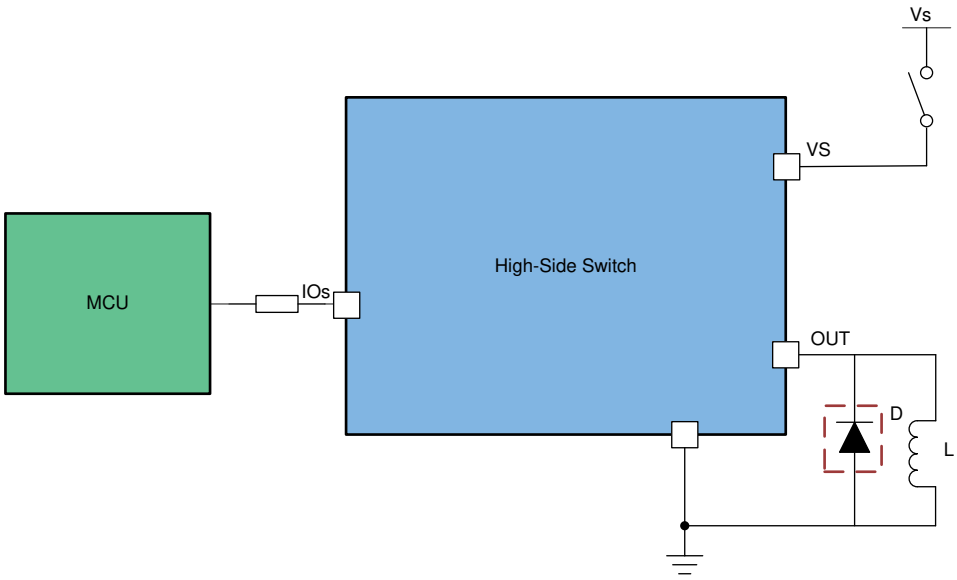


图 7-16. Protection for Loss of Power Supply

7.3.6.5 Reverse-Current Protection

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, TI recommends using two types of external circuitry.

- Adding a blocking diode (method 1). The device and load are protected when in reverse polarity.
- Adding a GND network (method 2). The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended configuration is a 1-kΩ resistor in parallel with a diode that is less than 100 mA.

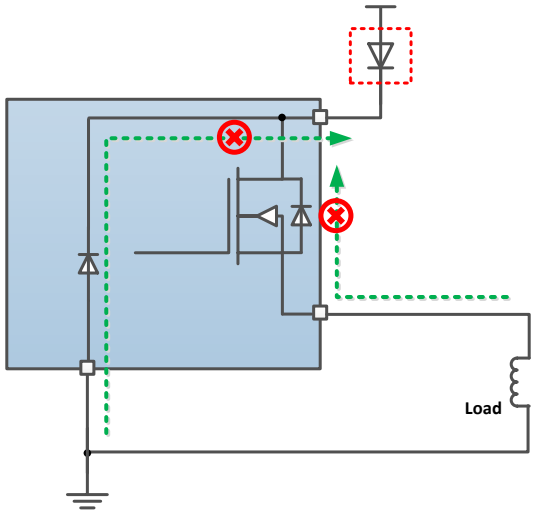


图 7-17. Reverse-Current External Protection Method 1

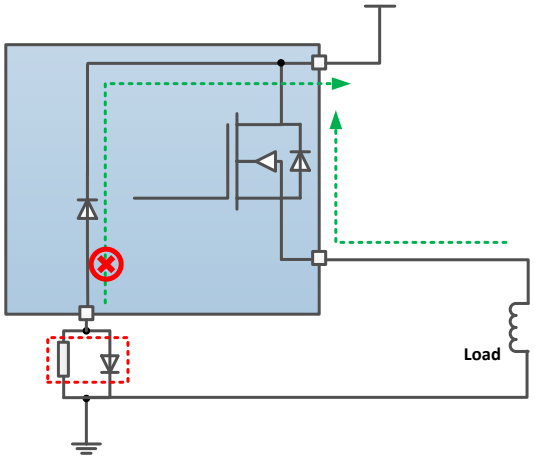


图 7-18. Reverse-Current External Protection Method 2

7.3.6.6 MCU I/O Protection

TI recommends using series resistors to protect the microcontroller, for example, 4.7 kΩ when using a 3.3-V microcontroller and 10 kΩ for a 5-V microcontroller.

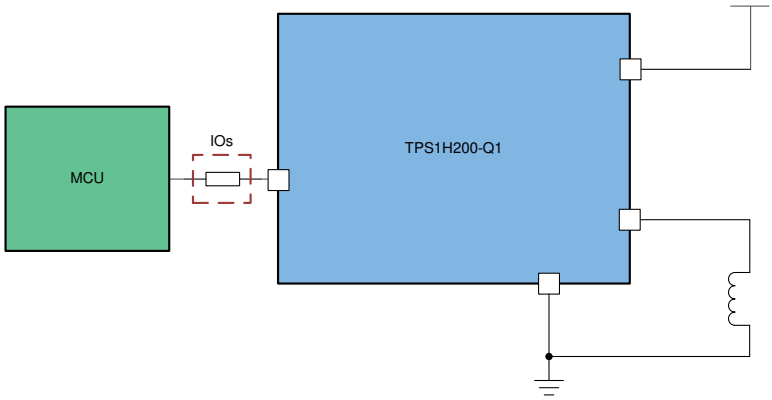


图 7-19. MCU I/O External Protection

7.4 Device Functional Modes

7.4.1 Working Modes

The device has three working modes: the normal mode, the standby mode, and the standby mode with diagnostics, as shown in 图 7-20.

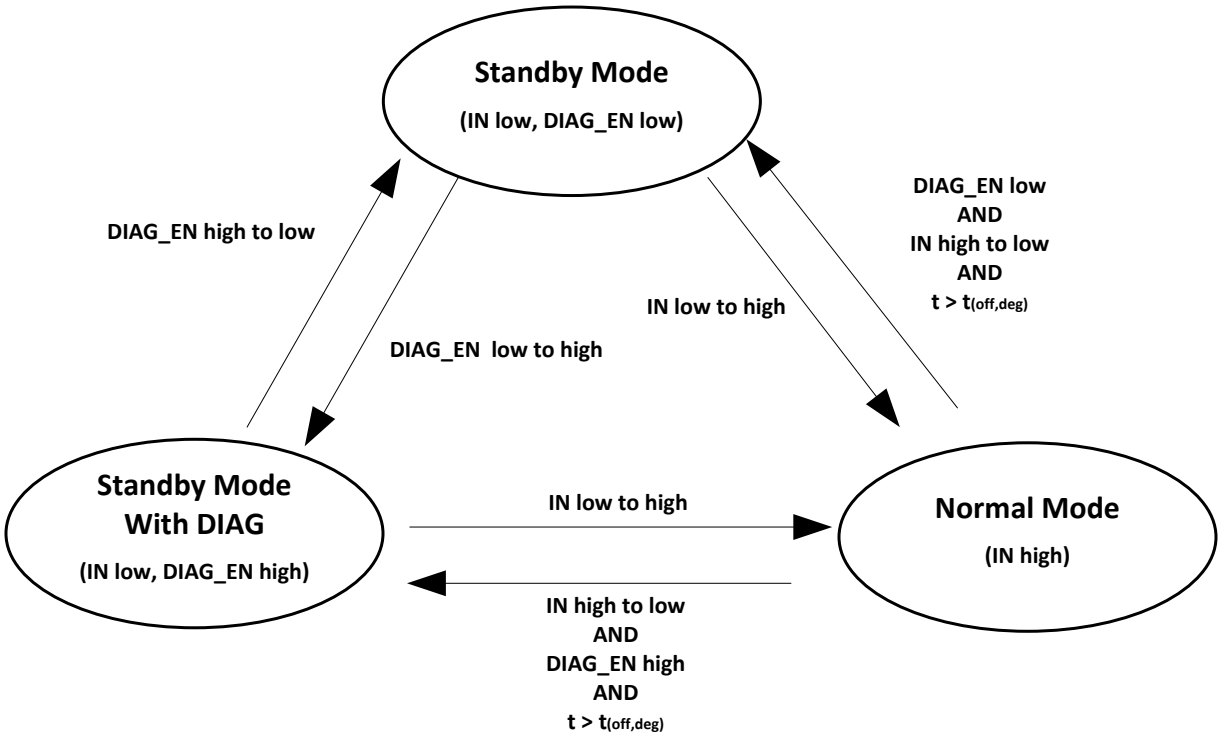


图 7-20. Working Modes

7.4.1.1 Normal Mode

When IN is high, the device enters normal mode.

7.4.1.2 Standby Mode

When IN is low and DIAG_EN is low, the device enters standby mode with ultra-low power consumption.

7.4.1.3 Standby Mode With Diagnostics

When IN is low and DIAG_EN is high, the device enters standby mode with diagnostics. The device still supports open-load and short-to-battery detection even when IN is low.

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS1H200A-Q1 device is a smart high-side switch, with an internal charge pump and single-channel integrated NMOS power FET. The adjustable current limit function greatly improves the reliability of the whole system. Full diagnostic features enable intelligent control of the load. The TPS1H200A-Q1 device applies for a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and submodules.

8.2 Typical Application

图 8-1 shows an example of how to design the external circuitry parameters.

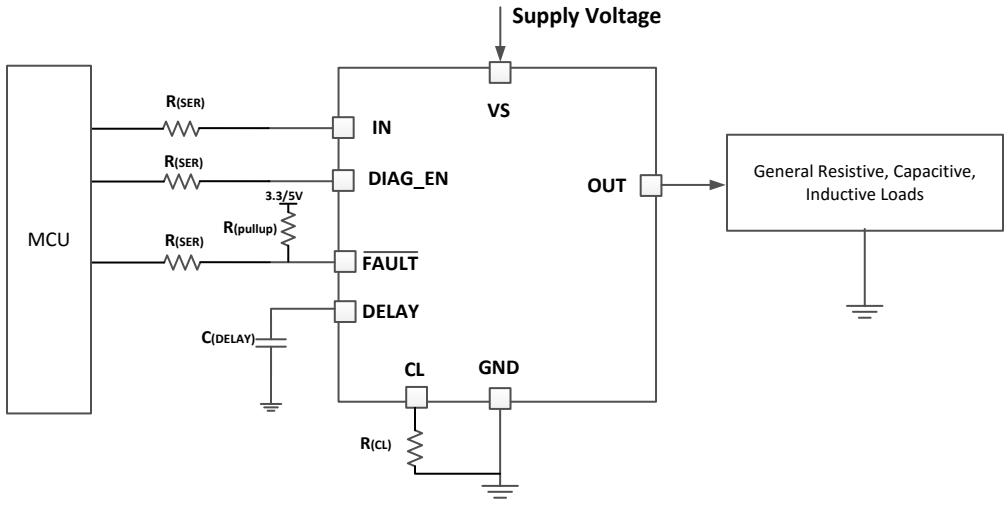


图 8-1. Typical Application Circuitry

8.2.1 Design Requirements

- V_{VS} range from 6 V to 18 V
- Nominal current of 500 mA
- Expected current limit value of 2 A
- Thermal sensitive system. When current limit occurs, the output latches off after 0.2 seconds. The 0.2 seconds is to ensure the safe start-up for a capacitive load, clamping the inrush current but without latch-off during start-up.
- Full diagnostics with 5-V MCU, including ON state open-load detection, short-to-GND, or overcurrent detection, and thermal shutdown detection

8.2.2 Detailed Design Procedure

To set the adjustable current limit value at 2 A, calculate $R_{(CL)}$ as follows:

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 2500}{2} = 1000\ \Omega \quad (3)$$

To set the adjustable latch-off delay at 0.2 s, calculate $C_{(DELAY)}$ as follows:

$$t_{dl} = t_{CL(deg)} + t_{dl1} + t_{dl2} = 0.2 \gg t_{dl2}$$

$$C_{DELAY} = \frac{I_{dl(chg)} \times t_{dl2}}{V_{dl(ref)}} = \frac{4.5 \times 0.2}{1.45} \times 10^{-6} = 0.62\ \mu F \quad (4)$$

TI recommends $R_{(SER)}$ = 10 kΩ for a 5-V MCU, and $R_{(pullup)}$ = 10 kΩ as the pullup resistor.

8.2.3 Application Curves

The following curves are test examples of hard-short conditions. The load is 0.1 A and the current limit value is 0.6 A. 图 8-2 shows a waveform of the latch-off mode. 图 8-3 shows a waveform of the auto-retry mode.

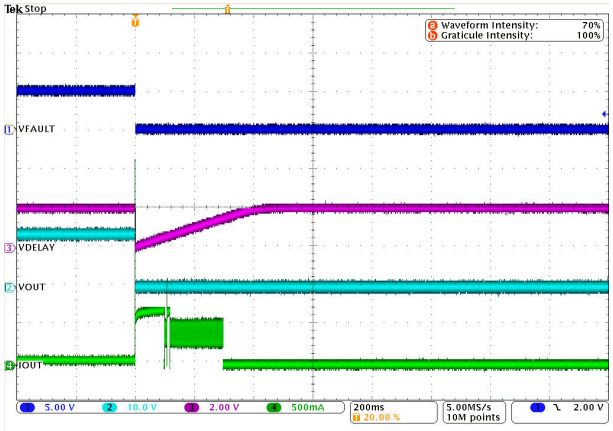


图 8-2. Hard-Short Condition in Latch-Off Mode

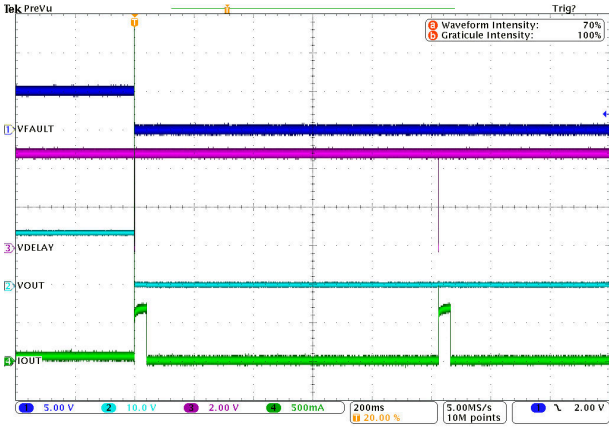


图 8-3. Hard-Short Condition in Auto-Retry Mode

9 Power Supply Recommendations

The device applies to 12-V and 24-V applications. The normal power supply connection is a 12-V or 24-V system.

10 Layout

10.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 175°C. If the output current is high, the power dissipation can be large. However, the PCB layout is very important. A good PCB design optimizes heat transfer, which is essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when no heat sinks are attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias must either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage must be at least 85%.

10.2 Layout Example

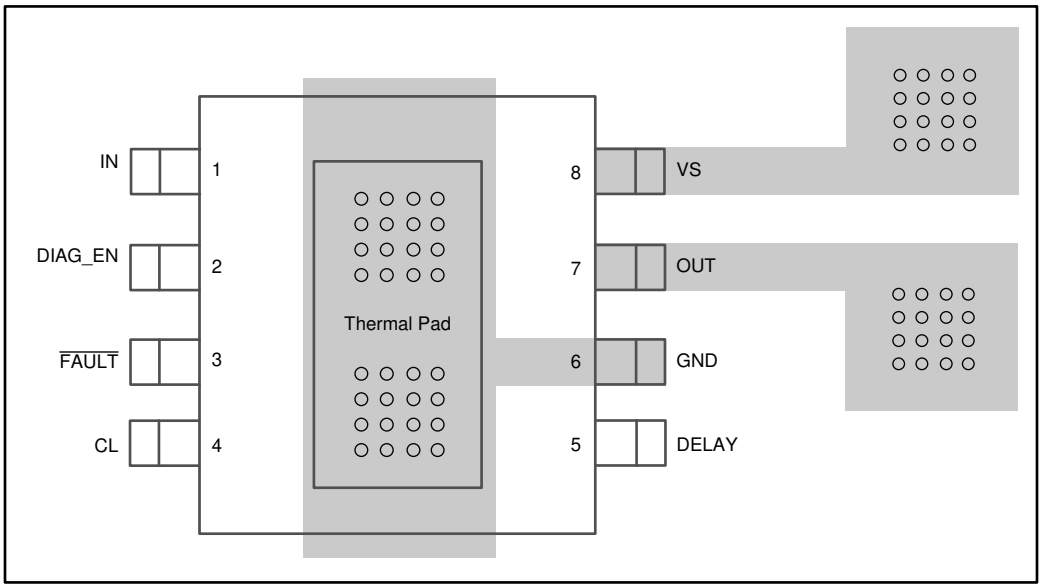


图 10-1. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS1H000-Q1 Evaluation Module (EVM)* User's Guide

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS1H200AQDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1EWX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

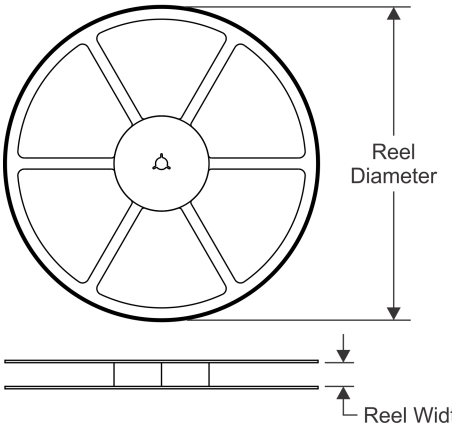
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

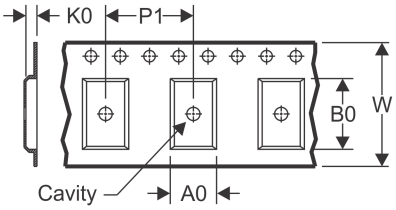
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

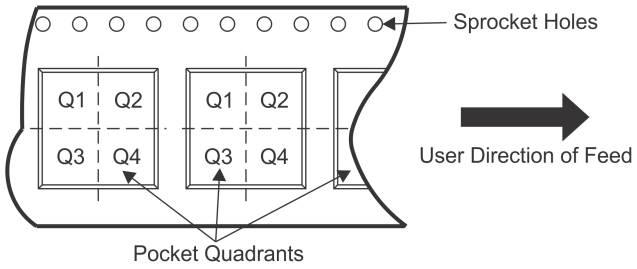


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

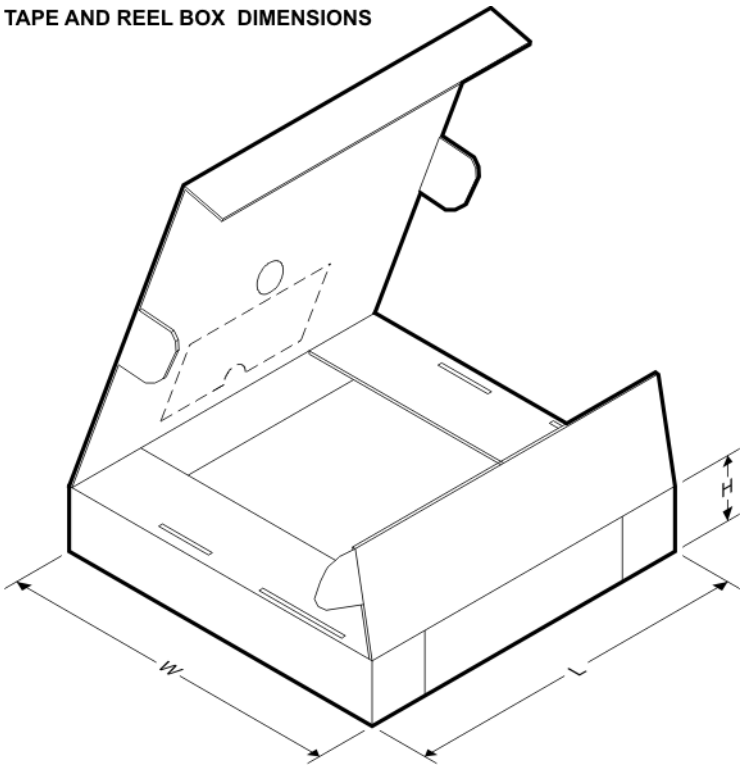
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1H200AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1H200AQDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0

GENERIC PACKAGE VIEW

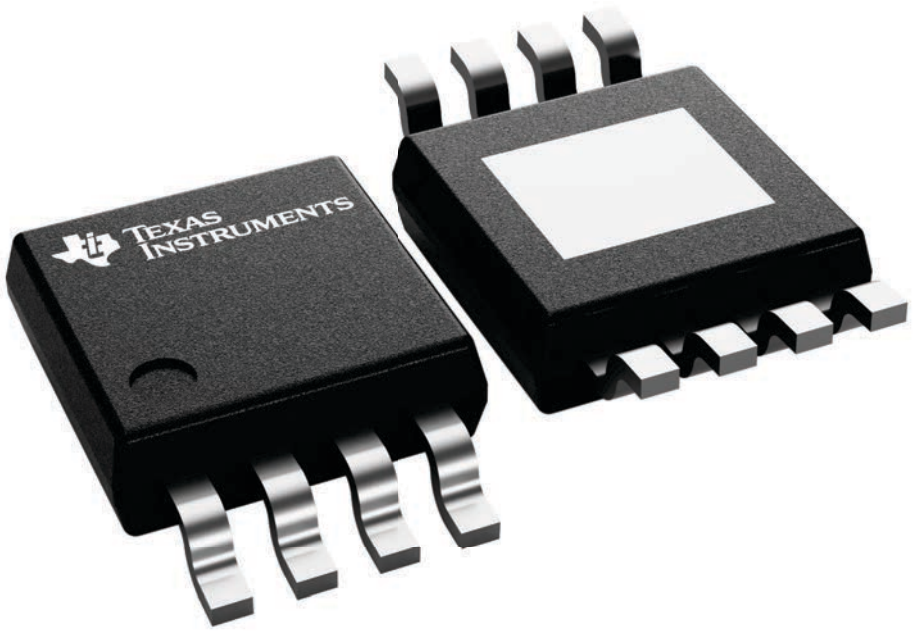
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

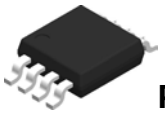
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

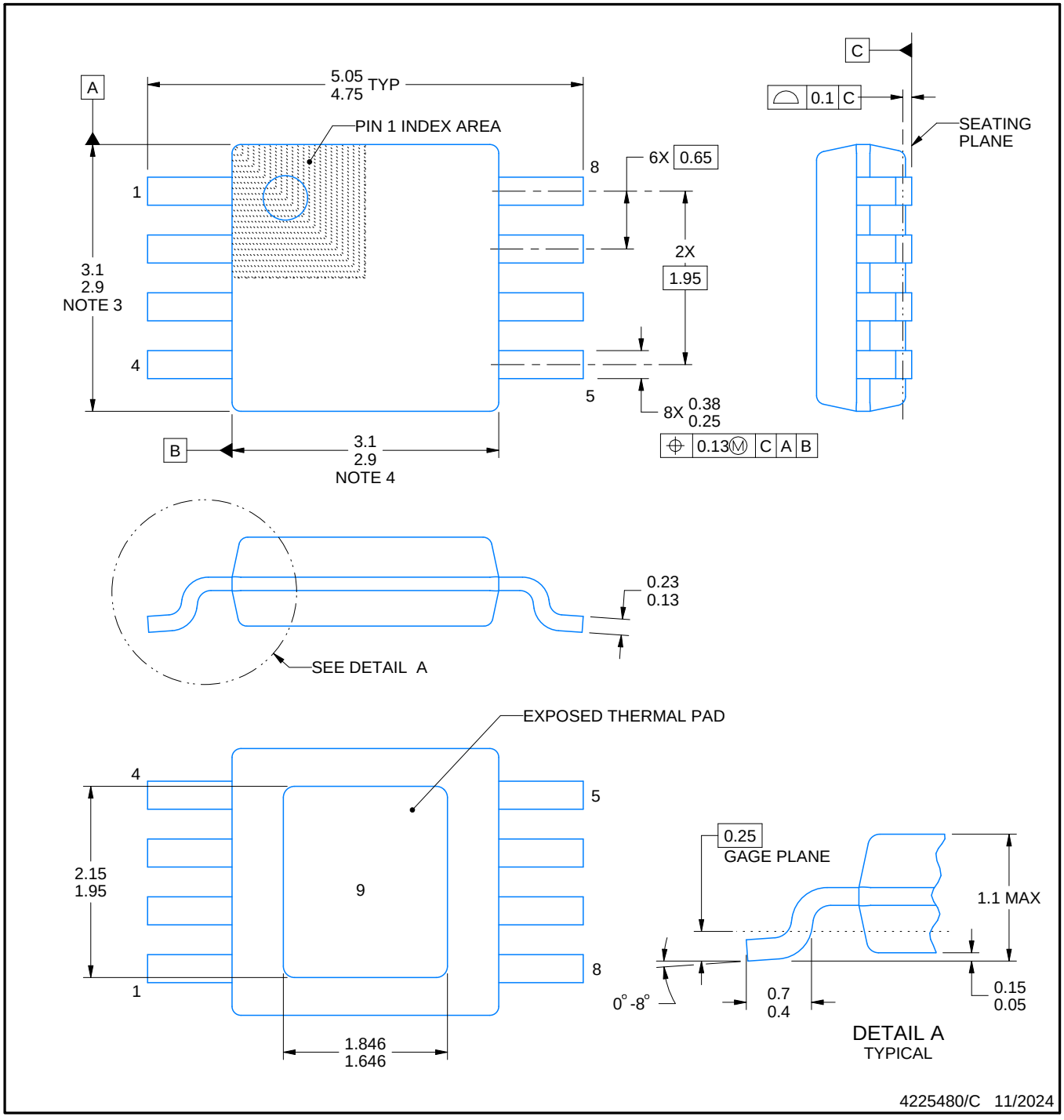
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

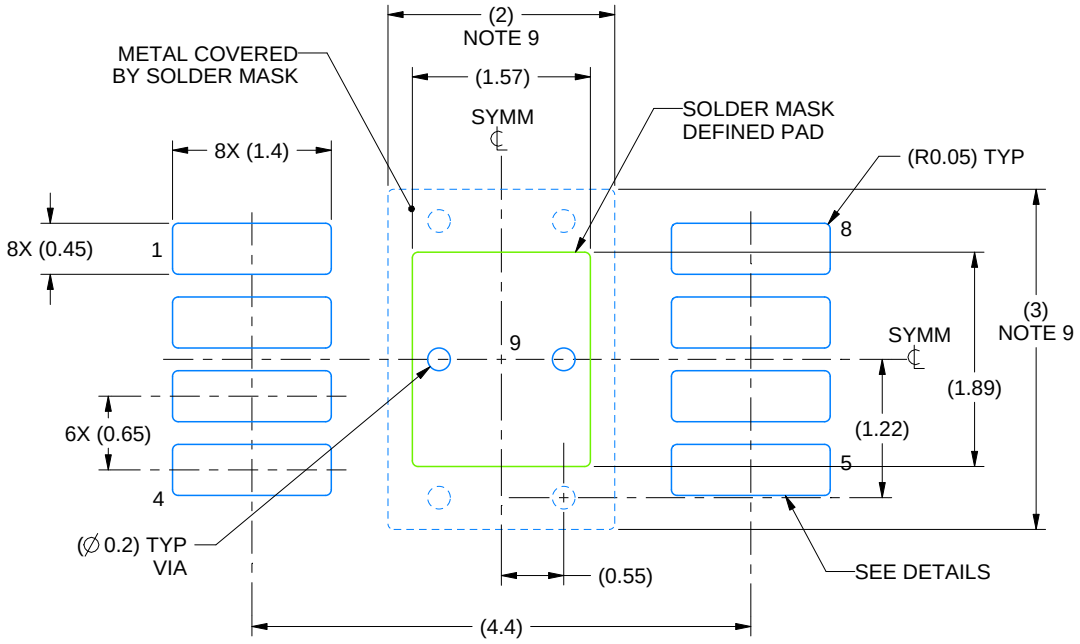
SMALL OUTLINE PACKAGE



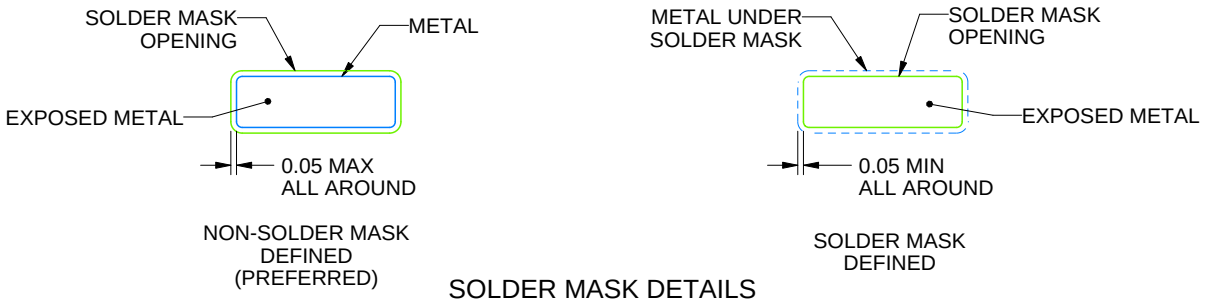
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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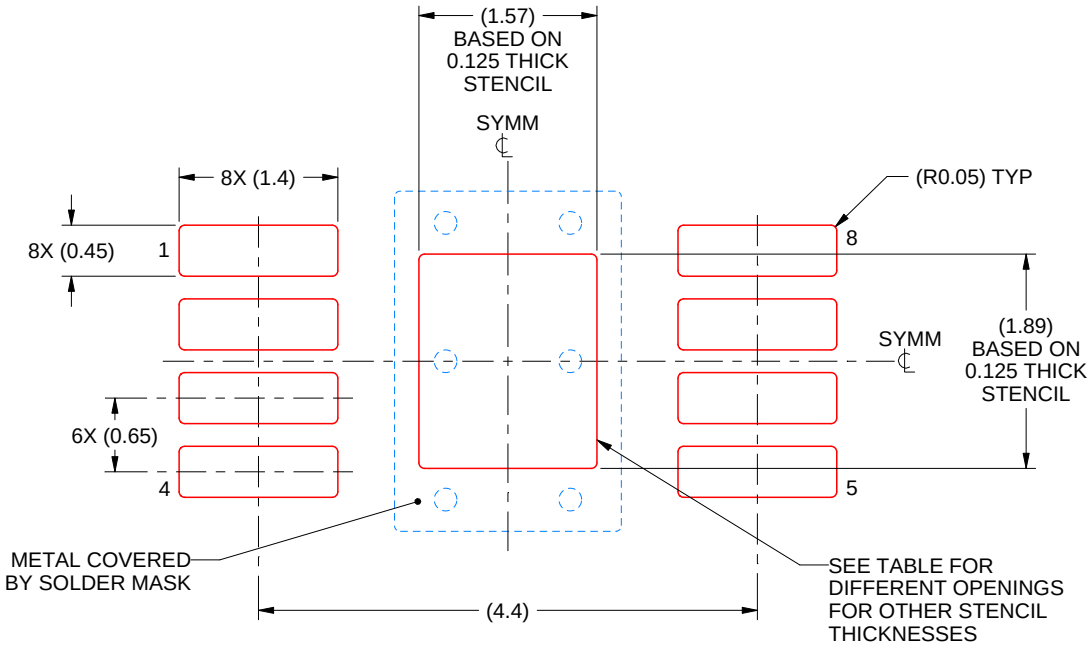
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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