

## TPS22990 5.5V、10A、导通电阻为 3.9mΩ 的负载开关

### 1 特性

- 集成单通道负载开关
- VBIAS 电压范围：2.5V 至 5.5V
- VIN 电压范围：0.6V 至 VBIAS
- 导通电阻
  - $R_{ON} = 3.9m\Omega$  ( $V_{IN} = 5V$  ( $V_{BIAS} = 5V$ ) 时的典型值)
  - $R_{ON} = 3.9m\Omega$  ( $V_{IN} = 3.3V$  ( $V_{BIAS} = 3.3V$ ) 时的典型值)
- 10A 最大连续开关电流
- 静态电流
  - $I_{Q,VBIAS} = 63\mu A$  ( $V_{BIAS} = 5V$  时)
- 关断电流
  - $I_{SD,VBIAS} = 5.5\mu A$  ( $V_{BIAS} = 5V$  时)
  - $I_{SD,VIN} = 4nA$  ( $V_{BIAS} = 5V$ 、 $V_{IN} = 5V$  时)
- 可通过 CT 调节的受控转换率
- 电源正常 (PG) 指示器
- 快速输出放电 (QOD) (仅限 TPS22990)
- 带散热焊盘的 10 引脚 3mm x 2mm SON 封装
- 根据 JESD 22 测试得出的静电放电 (ESD) 性能
  - 2kV 人体放电模式 (HBM) 和 1kV 器件充电模型 (CDM)

### 2 应用

- 笔记本、Chromebooks 和平板电脑
- 台式机和工业 PC
- 固态硬盘 (SSD)
- 服务器
- 电信系统

### 3 说明

TPS22990 产品系列由两款器件组成：TPS22990 和 TPS22990N。这两款器件都是 3.9mΩ 单通道负载开关，不但可以调节接通时间，而且还集成有 PG 指示器。

该系列器件包含一个可在 0.6V 至 5.5V 输入电压范围内运行的 N 沟道 MOSFET，最高可支持 10A 持续电流。宽输入电压范围及高电流能力使得该系列器件适用于多种设计与终端设备。3.9mΩ 的导通电阻能够将负载开关两端的压降和负载开关的功耗降到最低。

器件的可控上升时间可大幅降低大容量负载电容所产生的浪涌电流，从而降低或消除电源压降。该器件可通过 CT 调节转换率，从而在设计中灵活权衡浪涌电流和上电时序要求。集成的 PG 指示器会将负载开关的状态通知给系统，从而实现无缝电源排序。

TPS22990 具有一个可选的 218Ω 片上电阻。当开关被禁用时，可通过该电阻使输出快速放电，从而避免因电源浮动而导致下游负载出现未知状态。

TPS22990 采用小型、节省空间的

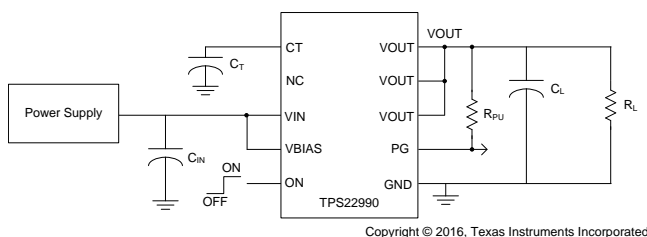
10 引脚 3mm x 2mm SON 封装，此类封装集成有散热焊盘，支持较高功耗。该器件在自然通风环境下的额定运行温度范围为 -40°C 至 +105°C。

#### 器件信息<sup>(1)</sup>

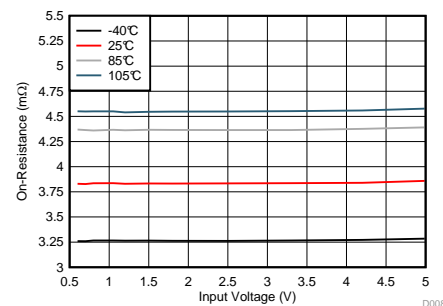
器件型号	封装	封装尺寸 (标称值)
TPS22990	WSON (10)	3.00mm x 2.00mm
TPS22990N		

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

#### 典型应用



#### 导通电阻与输入电压间的关系



$V_{BIAS} = 5V$ ,  $I_{OUT} = -200mA$



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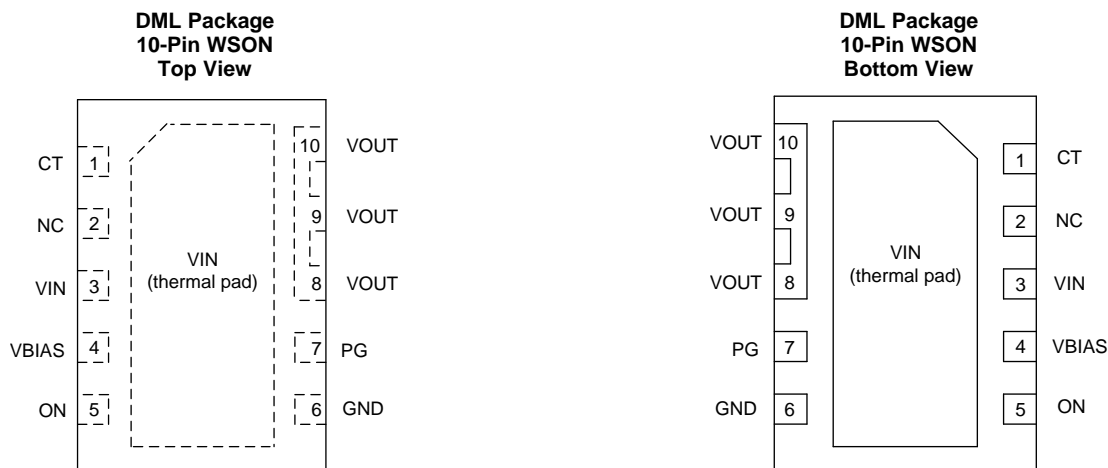
## 4 修订历史记录

Changes from Revision B (September 2016) to Revision C	Page				
<ul style="list-style-type: none"> <li>• Updated <math>V_{IH}</math> in <i>Recommended Operating Conditions</i> ..... 4</li> </ul>	4				
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## 5 Device Comparison Table

DEVICE	$R_{ON}$ at $V_{BIAS} = 5\text{ V}$	QOD	$I_{MAX}$	ENABLE
TPS22990	3.9 m $\Omega$	Yes	10 A	Active high
TPS22990N	3.9 m $\Omega$	No	10 A	Active high

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	CT	O	VOUT slew rate control
2	NC	—	Not internally connected
3	VIN	I	Switch input. Bypass this input with a ceramic capacitor to GND
4	VBIAS	P	Bias voltage. Power supply to the device
5	ON	I	Active high switch control input. Do not leave floating
6	GND	GND	Device ground
7	PG	O	Power good. Active high, open drain output. Tie to GND if not used
8	VOUT	O	Switch output
9			
10			
—	VIN (Thermal Pad)	I	Switch input. VIN and thermal pad (exposed center pad) to alleviate thermal stress. See the <a href="#">Layout</a> section for layout guidelines

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	-0.3	6	V
V <sub>BIAS</sub>	Bias voltage	-0.3	6	V
V <sub>OUT</sub>	Output voltage	-0.3	6	V
V <sub>ON</sub>	ON voltage	-0.3	6	V
V <sub>PG</sub>	PG voltage	-0.3	6	V
V <sub>CT</sub>	CT voltage	-0.3	15	V
I <sub>MAX</sub>	Maximum continuous switch current at T <sub>J</sub> = 125°C		10	A
I <sub>PLS</sub>	Maximum pulsed switch current, pulse < 300 μs, 2% duty cycle		12	A
T <sub>J</sub>	Maximum junction temperature		125	°C
T <sub>LEAD</sub>	Maximum lead temperature (10-s soldering time)		300	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage		0.6	V <sub>BIAS</sub>	V
V <sub>BIAS</sub>	Bias voltage		2.5	5.5	V
V <sub>OUT</sub>	Output voltage			V <sub>IN</sub>	V
V <sub>ON</sub>	ON voltage		0	5.5	V
V <sub>PG</sub>	PG voltage		0	5.5	V
V <sub>IH, ON</sub>	High-level input voltage, ON	V <sub>BIAS</sub> = 2.5 V to 5 V, T <sub>A</sub> < 85°C	1.05	5.5	V
		V <sub>BIAS</sub> = 2.5 V to 5.5 V, T <sub>A</sub> < 105°C	1.2	5.5	
V <sub>IL, ON</sub>	Low-level input voltage, ON		0	0.5	V
C <sub>IN</sub>	Input capacitor		1 <sup>(1)</sup>		μF
T <sub>A</sub>	Operating free-air temperature		-40	105	°C

- (1) See the [Application Information](#) section.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS22990	
		DML (WSON)	
		10 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	2.1	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	17	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics— $V_{BIAS} = 5\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temp  $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$  (full) and  $V_{BIAS} = 5\text{ V}$ . Typical values are for  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>							
$I_Q, V_{BIAS}$	$V_{BIAS}$ quiescent current	$I_{OUT} = 0\text{ A}$ , $V_{IN} = V_{ON} = 5\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		63	76	$\mu\text{A}$
			$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			77	
$I_{SD}, V_{BIAS}$	$V_{BIAS}$ shutdown current	$V_{ON} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		5.5	7	$\mu\text{A}$
			$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			7	
$I_{SD}, V_{IN}$	$V_{IN}$ shutdown current	$V_{ON} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$	$V_{IN} = 5\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.004	4	$\mu\text{A}$
				$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		10	
			$V_{IN} = 3.3\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.003	3	
				$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		7	
			$V_{IN} = 2.5\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.002	2	
				$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		5	
			$V_{IN} = 1.8\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.002	2	
				$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		4	
	$V_{IN} = 1.05\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.001	1			
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		3			
	$V_{IN} = 0.6\text{ V}$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.001	1			
		$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		2			
$I_{ON}$	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			0.1	$\mu\text{A}$
$V_{HYS,ON}$	ON pin hysteresis	$V_{IN} = 5\text{ V}$	$25^{\circ}\text{C}$		123		mV
$I_{PG, LKG}$	Leakage current into PG pin	$V_{PG} = 5\text{ V}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			0.5	$\mu\text{A}$
$V_{PG,OL}$	PG output low voltage	$V_{ON} = 0\text{ V}$ , $I_{PG} = 1\text{ mA}$	$-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$			0.2	V
<b>RESISTANCE CHARACTERISTICS</b>							

**Electrical Characteristics— $V_{BIAS} = 5\text{ V}$  (continued)**

Unless otherwise noted, the specification in the following table applies over the operating ambient temp  $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$  (full) and  $V_{BIAS} = 5\text{ V}$ . Typical values are for  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$R_{ON}$	On-state resistance	$I_{OUT} = -200\text{ mA}$ , $V_{ON} = 5\text{ V}$	$V_{IN} = 5\text{ V}$	25°C	3.9	4.8	mΩ
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 3.3\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 2.5\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 1.8\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 1.05\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 0.6\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
$R_{PD}$	Output pull-down resistance (TPS22990 Only)	$V_{IN} = V_{OUT} = 5\text{ V}$ , $V_{ON} = 0\text{ V}$	-40°C to +105°C	218	253	Ω	

**7.6 Electrical Characteristics— $V_{BIAS} = 3.3\text{ V}$**

Unless otherwise noted, the specification in the following table applies over the operating ambient temp  $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$  (full) and  $V_{BIAS} = 3.3\text{ V}$ . Typical values are for  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>							
$I_{Q, VBIAS}$	$V_{BIAS}$ quiescent current	$I_{OUT} = 0\text{ A}$ , $V_{IN} = V_{ON} = 3.3\text{ V}$	-40°C to +85°C	48	58		μA
			-40°C to +105°C			59	
$I_{SD, VBIAS}$	$V_{BIAS}$ shutdown current	$V_{ON} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$	-40°C to +85°C	4.5	6		μA
			-40°C to +105°C			7	
$I_{SD, VIN}$	$V_{IN}$ shutdown current	$V_{ON} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$	$V_{IN} = 3.3\text{ V}$	-40°C to +85°C	0.003	3	μA
				-40°C to +105°C	7		
			$V_{IN} = 2.5\text{ V}$	-40°C to +85°C	0.002	2	
				-40°C to +105°C	5		
			$V_{IN} = 1.8\text{ V}$	-40°C to +85°C	0.002	2	
				-40°C to +105°C	4		
$V_{IN} = 1.05\text{ V}$	-40°C to +85°C	0.001	1				
	-40°C to +105°C	3					
$V_{IN} = 0.6\text{ V}$	-40°C to +85°C	0.001	1				
	-40°C to +105°C	2					
$I_{ON}$	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	-40°C to +105°C		0.1		μA
$V_{HYS, ON}$	ON pin hysteresis	$V_{IN} = 3.3\text{ V}$	25°C		100		mV
$I_{PG, LKG}$	Leakage current into PG pin	$V_{PG} = 5\text{ V}$	-40°C to +105°C		0.5		μA
$V_{PG, OL}$	PG output low voltage	$V_{ON} = 0\text{ V}$ , $I_{PG} = 1\text{ mA}$	-40°C to +105°C		0.2		V
<b>RESISTANCE CHARACTERISTICS</b>							

**Electrical Characteristics— $V_{BIAS} = 3.3\text{ V}$  (continued)**

Unless otherwise noted, the specification in the following table applies over the operating ambient temp  $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$  (full) and  $V_{BIAS} = 3.3\text{ V}$ . Typical values are for  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$R_{ON}$	On-state resistance	$I_{OUT} = -200\text{ mA}$ , $V_{ON} = 5\text{ V}$	$V_{IN} = 3.3\text{ V}$	25°C	3.9	4.8	mΩ
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 2.5\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 1.8\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
			$V_{IN} = 1.05\text{ V}$	25°C	3.9	4.8	
				-40°C to +85°C	5.7		
				-40°C to +105°C	6		
$V_{IN} = 0.6\text{ V}$	25°C	3.9	4.8				
	-40°C to +85°C	5.7					
	-40°C to +105°C	6					
$R_{PD}$	Output pull-down resistance (TPS22990 Only)	$V_{IN} = V_{OUT} = 3.3\text{ V}$ , $V_{ON} = 0\text{ V}$	-40°C to +105°C	219	256	Ω	

**7.7 Switching Characteristics**

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b><math>V_{IN} = 5\text{ V}</math>, <math>V_{ON} = V_{BIAS} = 5\text{ V}</math>, <math>T_A = 25^{\circ}\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	Turnon time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		34	μs
$t_{OFF}$	Turnoff time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		5.4	
$t_R$	VOUT rise time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		31	
$t_F$	VOUT fall time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		2.3	
$t_D$	ON delay time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		21	
$t_{PG,ON}$	PG turnon time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		152	
$t_{PG,OFF}$	PG turnoff time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		1.3	
<b><math>V_{IN} = 1.05\text{ V}</math>, <math>V_{ON} = V_{BIAS} = 5\text{ V}</math>, <math>T_A = 25^{\circ}\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	Turnon time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		30	μs
$t_{OFF}$	Turnoff time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		8	
$t_R$	VOUT rise time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		13	
$t_F$	VOUT fall time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		2.2	
$t_D$	ON delay time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		24	
$t_{PG,ON}$	PG turnon time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		134	
$t_{PG,OFF}$	PG turnoff time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		1.3	
<b><math>V_{IN} = 0.6\text{ V}</math>, <math>V_{ON} = V_{BIAS} = 5\text{ V}</math>, <math>T_A = 25^{\circ}\text{C}</math> (unless otherwise noted)</b>					
$t_{ON}$	Turnon time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		29	μs
$t_{OFF}$	Turnoff time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		8.8	
$t_R$	VOUT rise time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		10	
$t_F$	VOUT fall time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		2.2	
$t_D$	ON delay time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		24	
$t_{PG,ON}$	PG turnon time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		131	
$t_{PG,OFF}$	PG turnoff time	$R_L = 10\ \Omega$ , $C_L = 0.1\ \mu\text{F}$ , $C_T = 0\ \text{pF}$ , $R_{PU} = 10\ \text{k}\Omega$ , $C_{IN} = 1\ \mu\text{F}$		1.3	

(1) Turnoff time and fall time are dependent on the time constant at the load. For TPS22990N, there is no QOD. The time constant is  $R_L \times C_L$ . For TPS22990, internal pull down  $R_{PD}$  is enabled when the switch is disabled. The time constant is  $(R_{PD}/R_L) \times C_L$ .

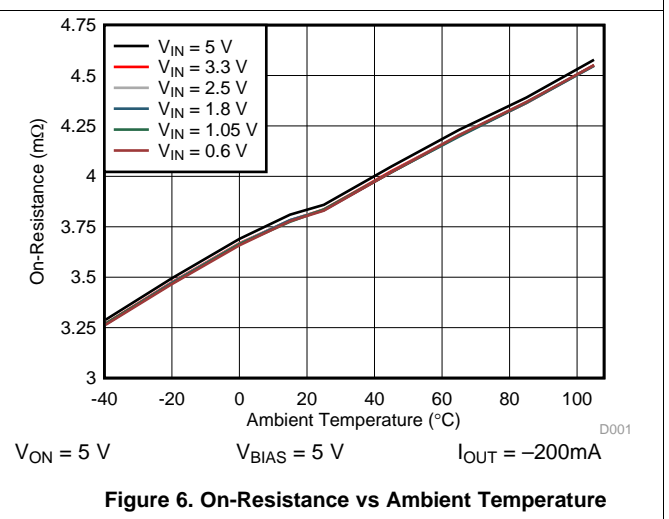
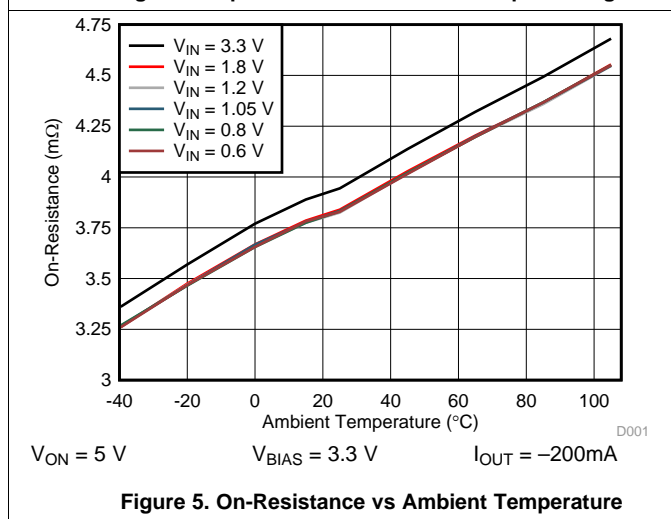
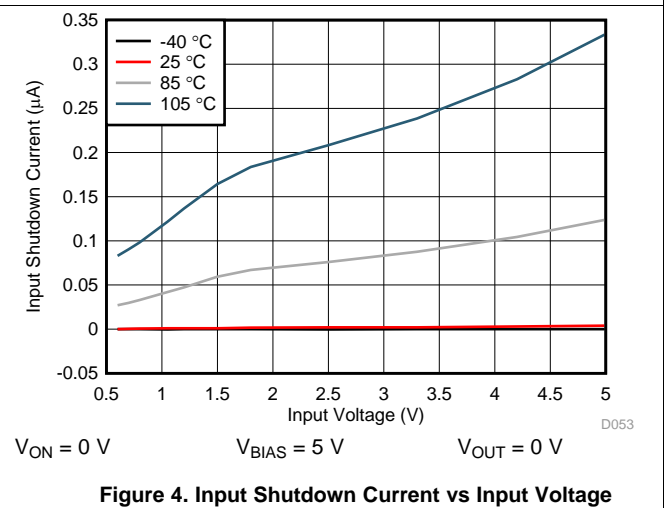
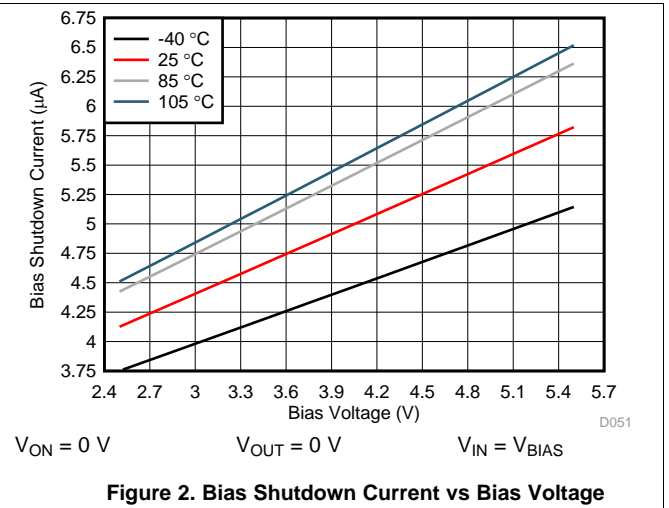
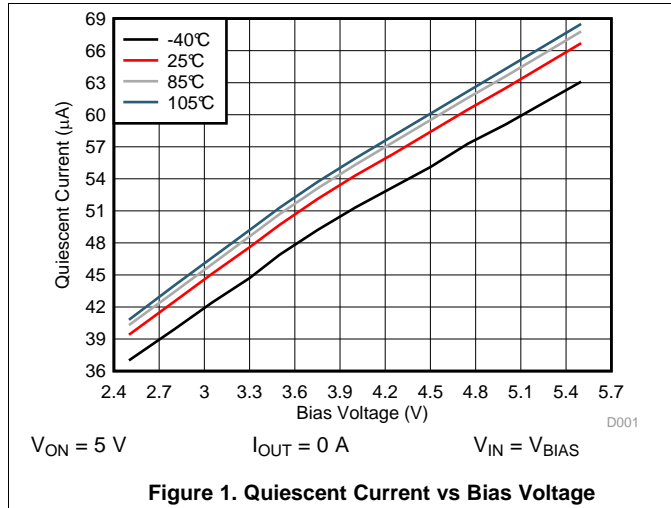
**Switching Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>V<sub>IN</sub> = 3.3 V, V<sub>ON</sub> = 5 V, V<sub>BIAS</sub> = 3.3 V, T<sub>A</sub> = 25°C (unless otherwise noted)</b>						
t <sub>ON</sub>	Turnon time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		33		μs
t <sub>OFF</sub>	Turnoff time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		6.2		
t <sub>R</sub>	VOUT rise time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		24		
t <sub>F</sub>	VOUT fall time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		2.4		
t <sub>D</sub>	ON delay time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		22		
t <sub>PG,ON</sub>	PG turnon time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		132		
t <sub>PG,OFF</sub>	PG turnoff time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		1.5		
<b>V<sub>IN</sub> = 1.05 V, V<sub>ON</sub> = 5 V, V<sub>BIAS</sub> = 3.3 V, T<sub>A</sub> = 25°C (unless otherwise noted)</b>						
t <sub>ON</sub>	Turnon time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		30		μs
t <sub>OFF</sub>	Turnoff time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		8.7		
t <sub>R</sub>	VOUT rise time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		12		
t <sub>F</sub>	VOUT fall time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		2.3		
t <sub>D</sub>	ON delay time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		24		
t <sub>PG,ON</sub>	PG turnon time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		122		
t <sub>PG,OFF</sub>	PG turnoff time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		1.5		
<b>V<sub>IN</sub> = 0.6 V, V<sub>ON</sub> = 5 V, V<sub>BIAS</sub> = 3.3 V, T<sub>A</sub> = 25°C (unless otherwise noted)</b>						
t <sub>ON</sub>	Turnon time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		30		μs
t <sub>OFF</sub>	Turnoff time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		9.4		
t <sub>R</sub>	VOUT rise time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		9		
t <sub>F</sub>	VOUT fall time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		2.3		
t <sub>D</sub>	ON delay time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		25		
t <sub>PG,ON</sub>	PG turnon time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		119		
t <sub>PG,OFF</sub>	PG turnoff time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, C <sub>T</sub> = 0 pF, R <sub>PU</sub> = 10 kΩ, C <sub>IN</sub> = 1 μF		1.5		



### 7.8 Typical Characteristics



Typical Characteristics (continued)

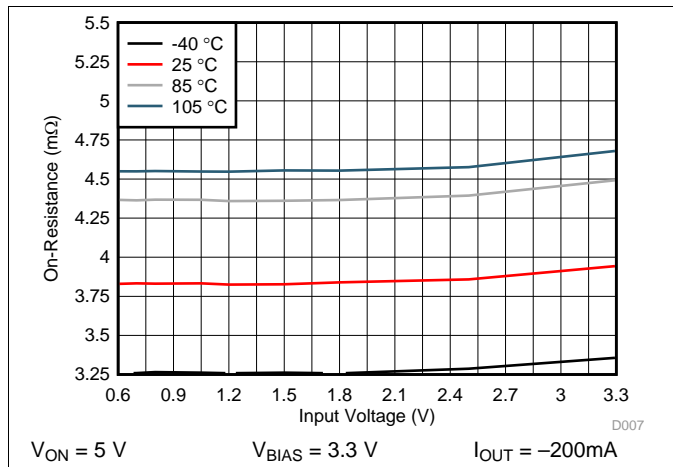


Figure 7. On-Resistance vs Input Voltage

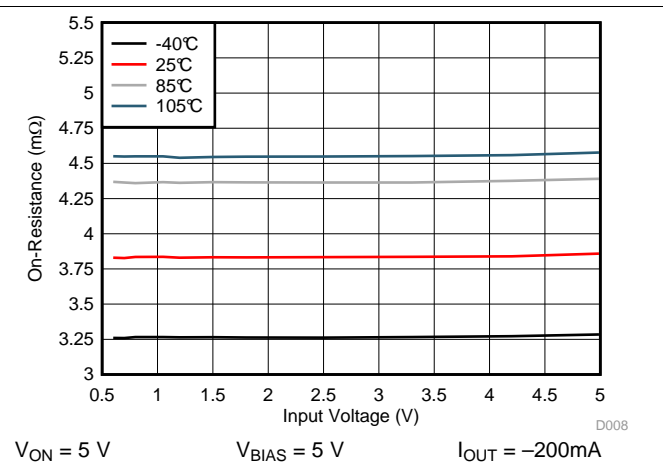


Figure 8. On-Resistance vs Input Voltage

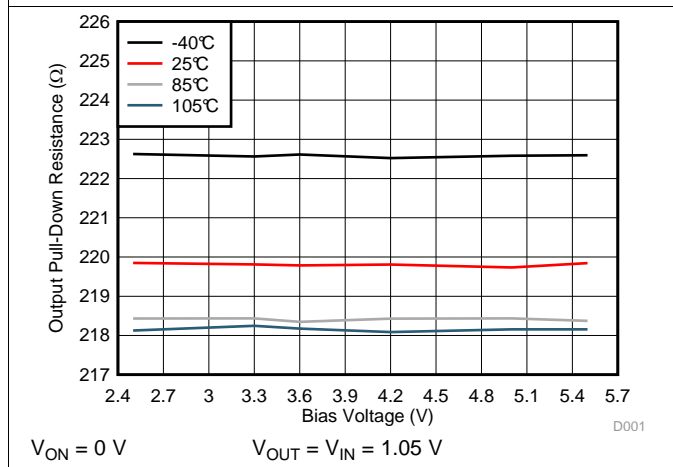


Figure 9. Output Pull-Down Resistance vs Bias Voltage

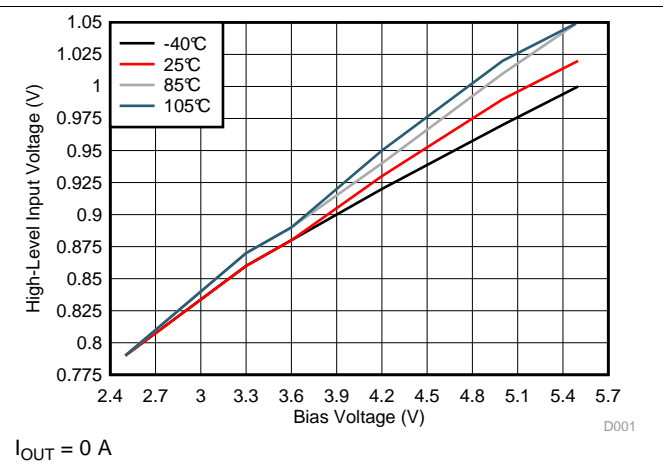


Figure 10. High-Level Input Voltage vs Bias Voltage

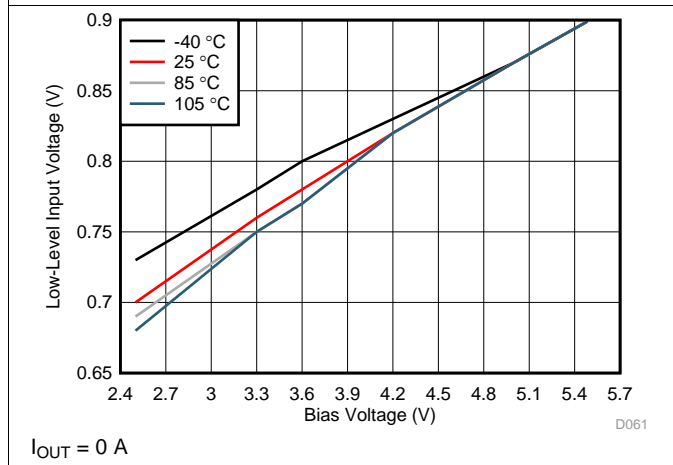


Figure 11. Low-Level Input Voltage vs Bias Voltage

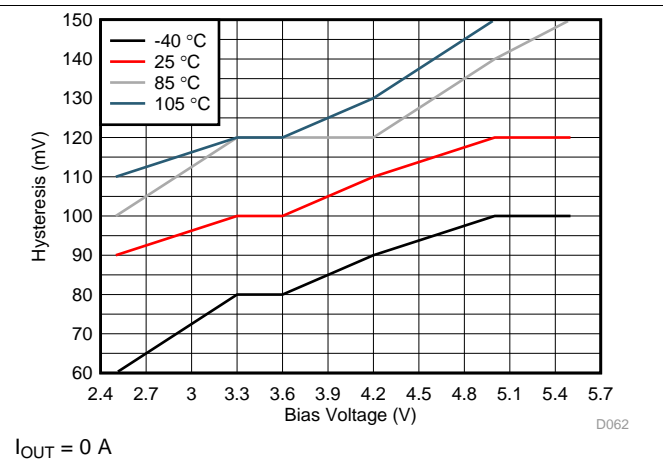
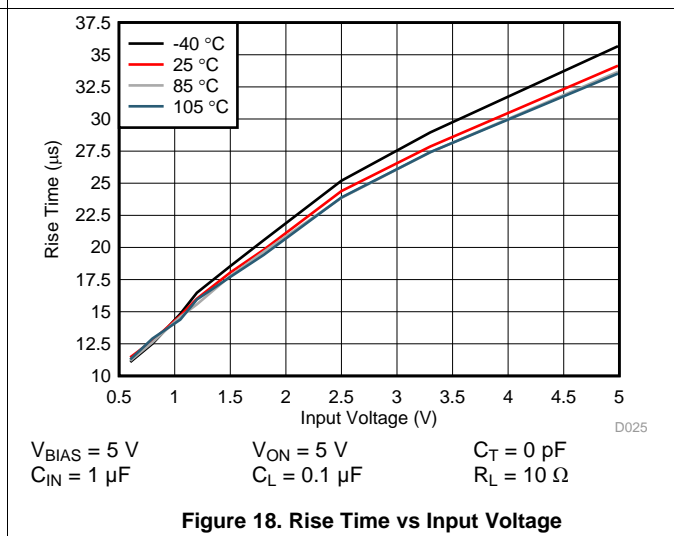
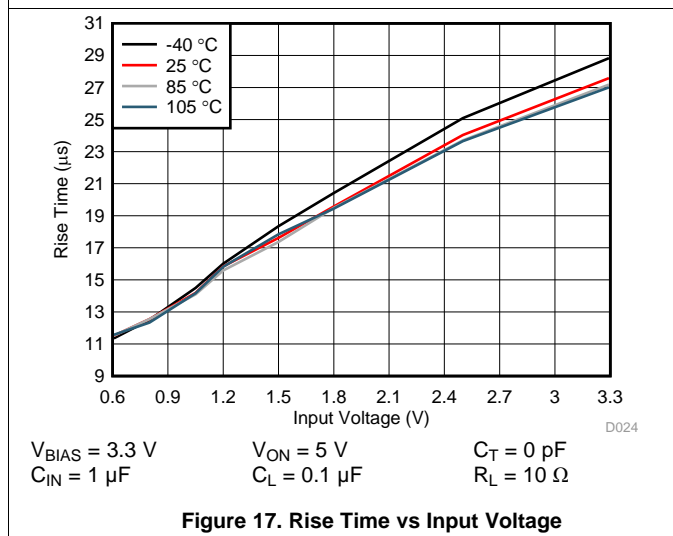
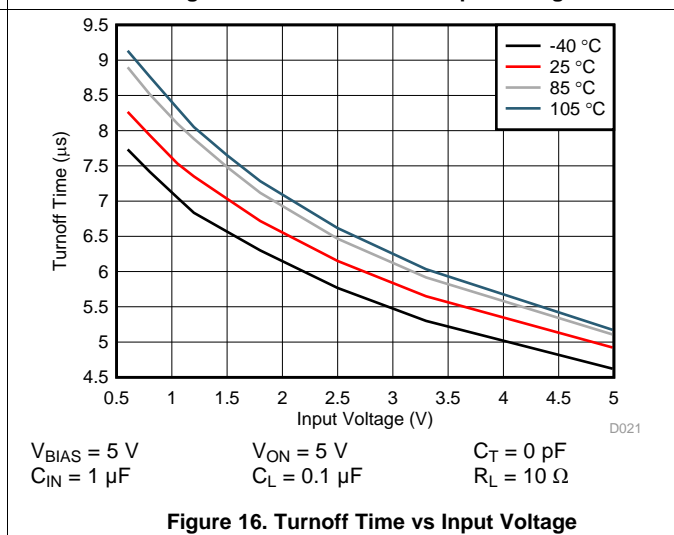
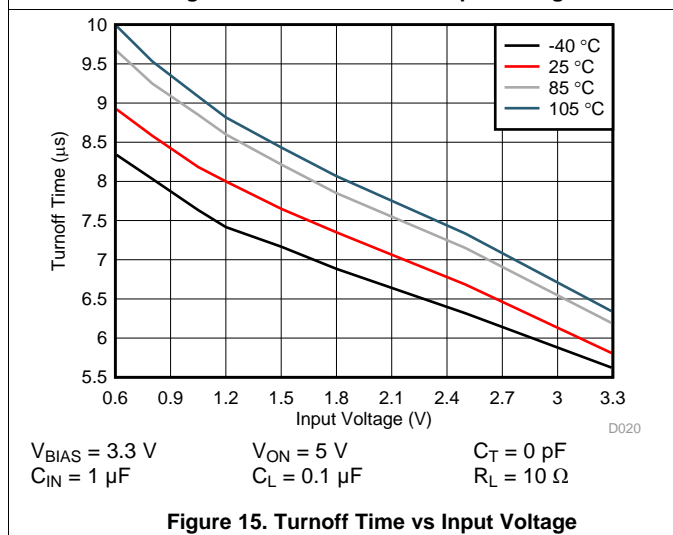
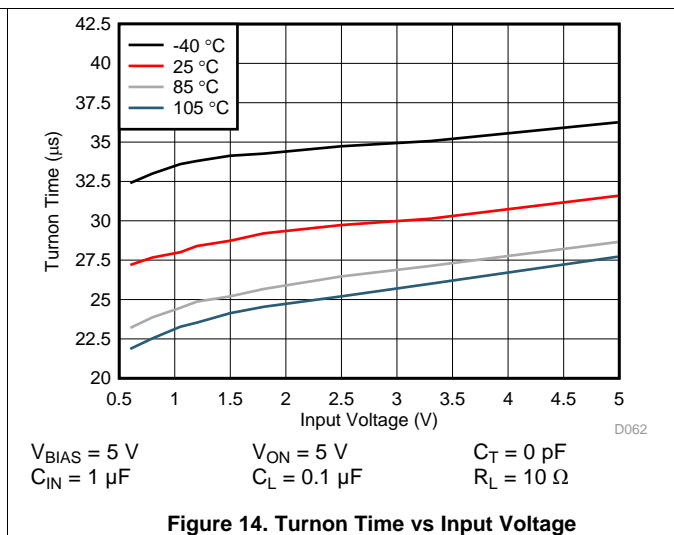
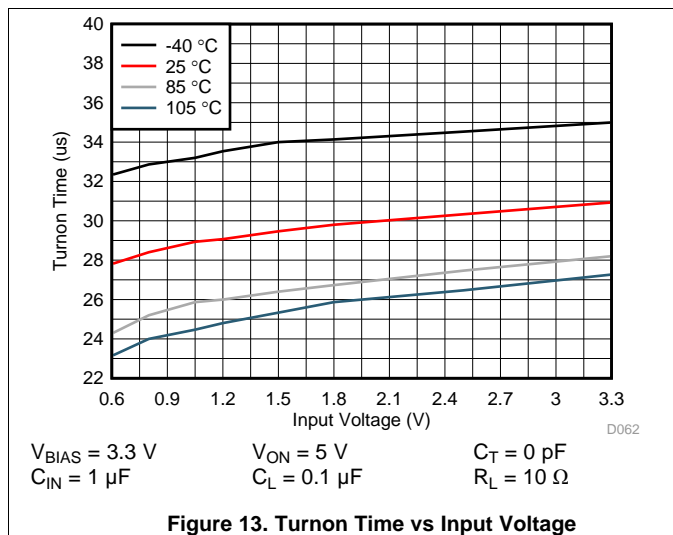


Figure 12. Hysteresis vs Bias Voltage

Typical Characteristics (continued)



Typical Characteristics (continued)

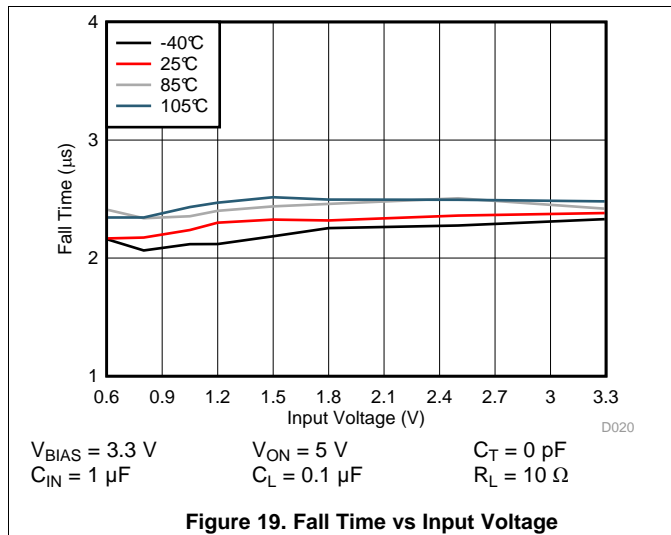


Figure 19. Fall Time vs Input Voltage

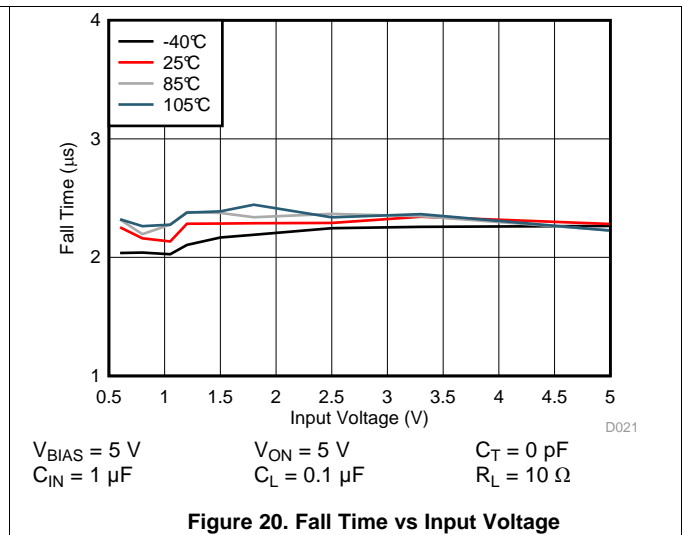


Figure 20. Fall Time vs Input Voltage

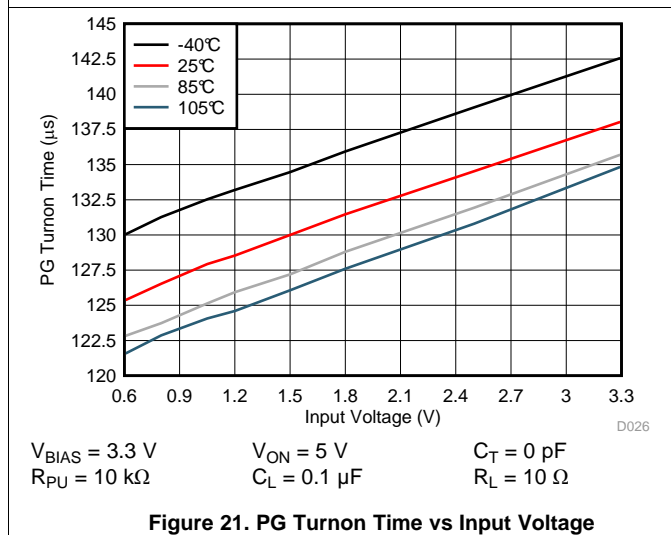


Figure 21. PG Turnon Time vs Input Voltage

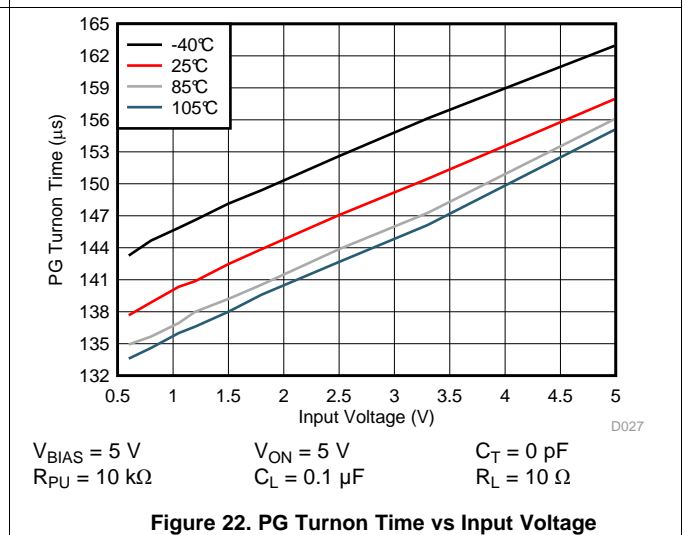


Figure 22. PG Turnon Time vs Input Voltage

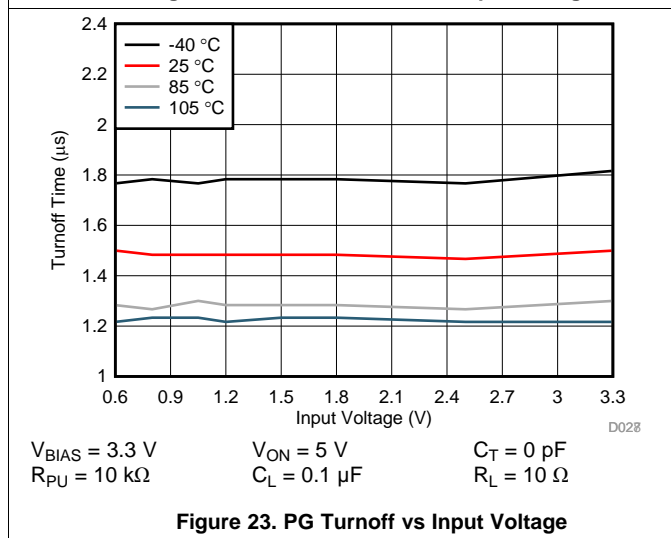


Figure 23. PG Turnoff vs Input Voltage

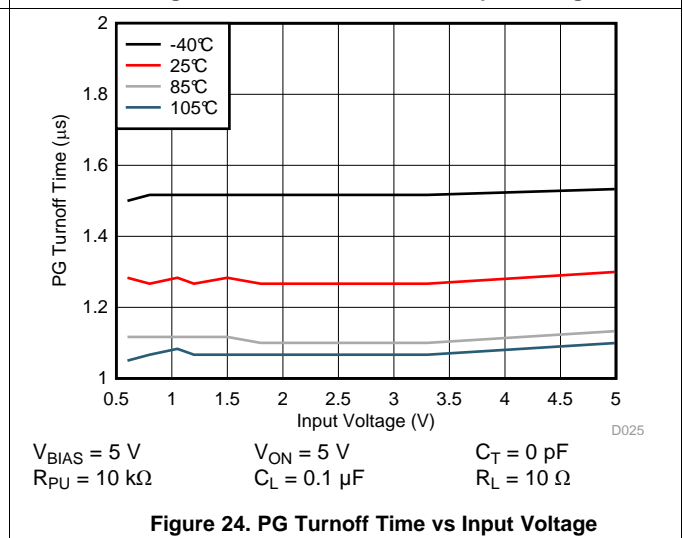


Figure 24. PG Turnoff Time vs Input Voltage

Typical Characteristics (continued)

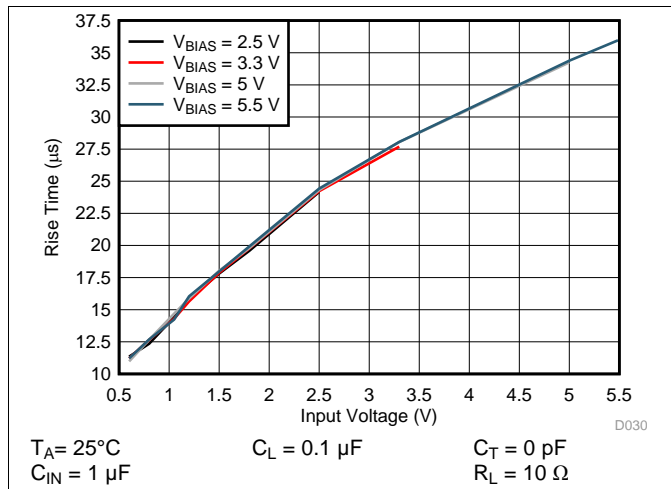


Figure 25. Rise Time vs Input Voltage

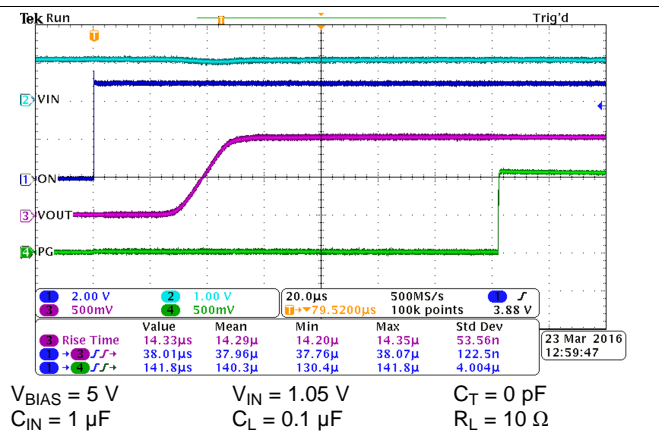


Figure 26. Turnon Response

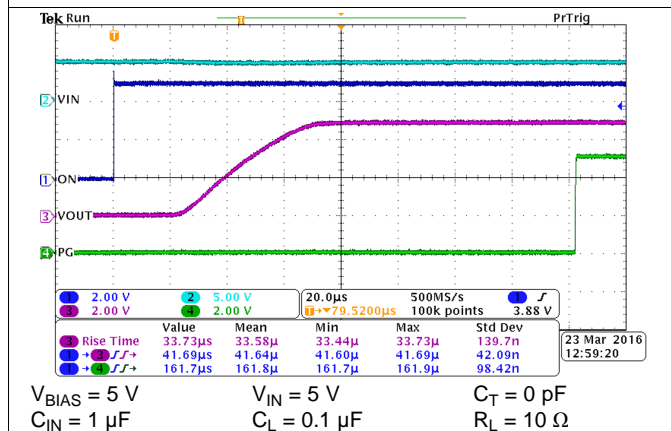


Figure 27. Turnon Response

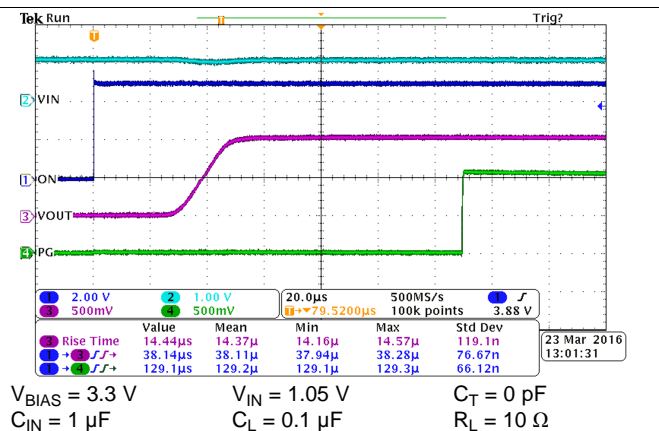


Figure 28. Turnon Response

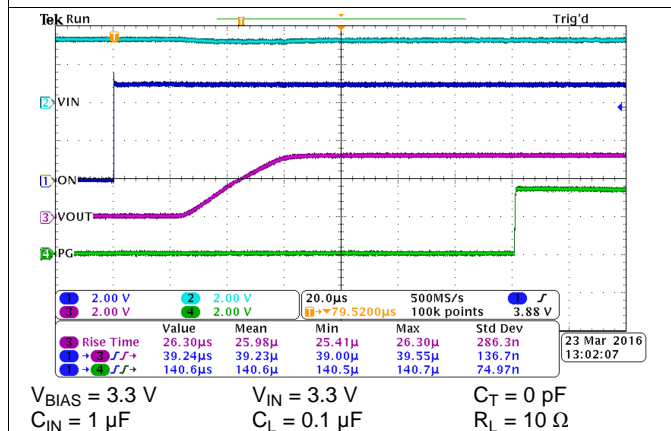


Figure 29. Turnon Response

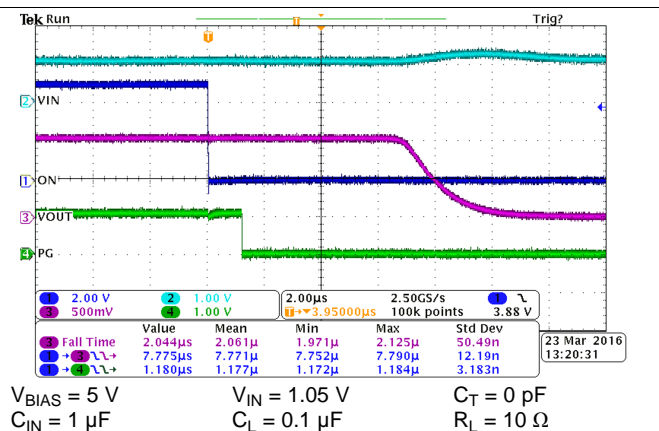


Figure 30. Turnon Response

Typical Characteristics (continued)

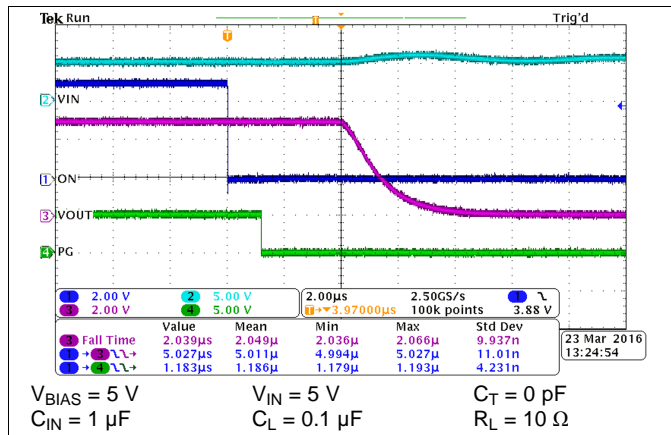


Figure 31. Turnoff Response

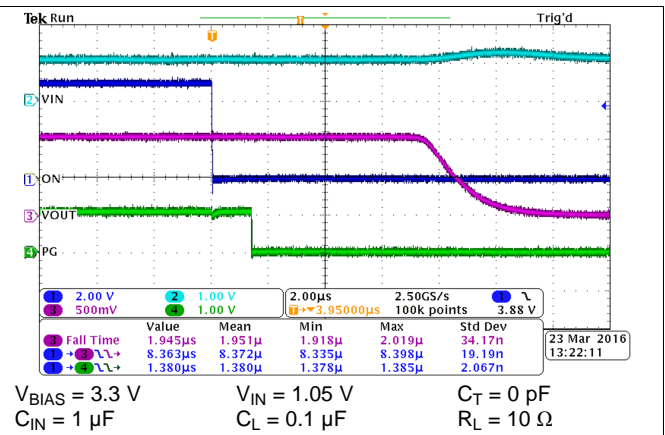


Figure 32. Turnoff Response

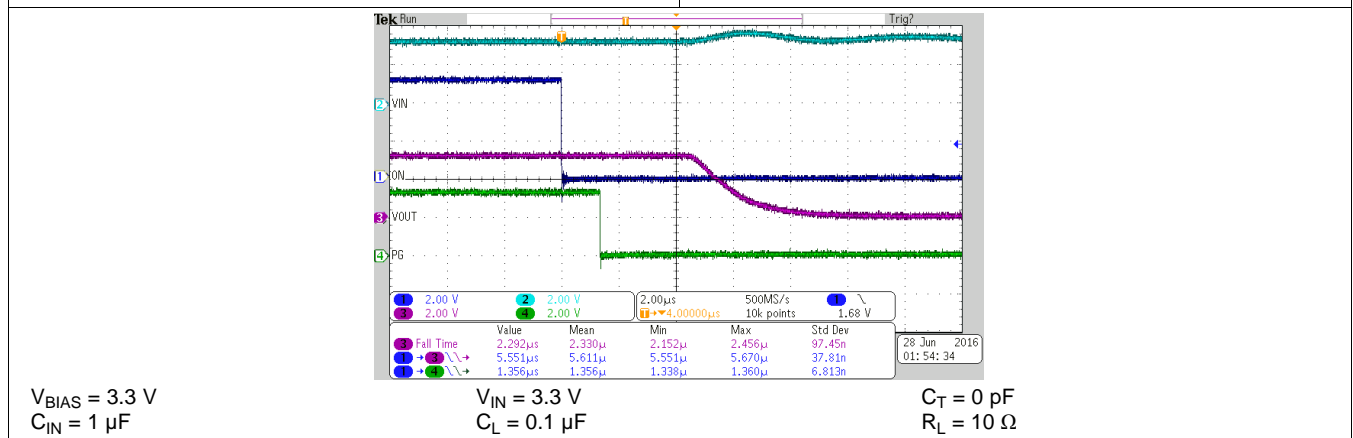
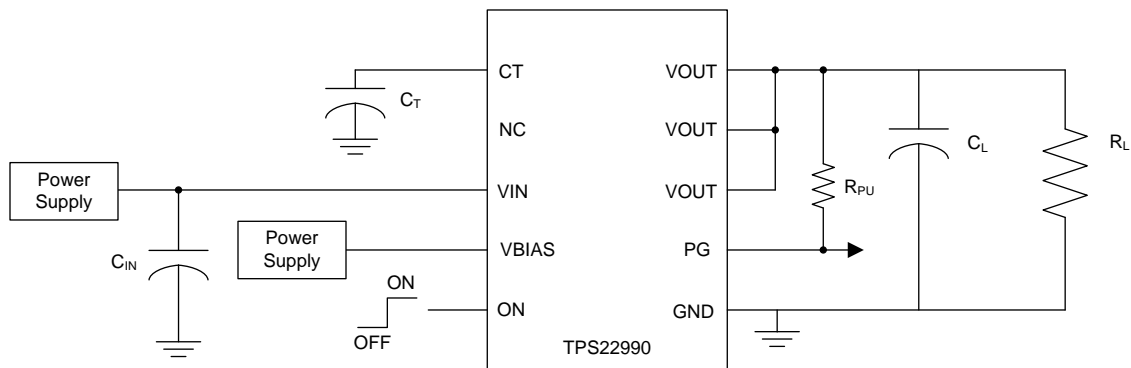


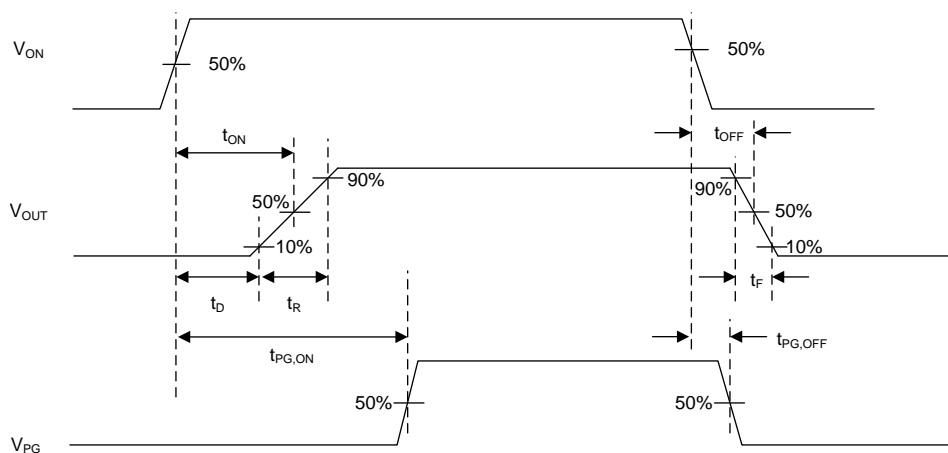
Figure 33. Turnoff Response

## 8 Parameter Measurement Information



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Figure 34. Timing Test Circuit



Rise and fall times of the control signals is 100 ns.

Figure 35. Timing Waveforms

## 9 Detailed Description

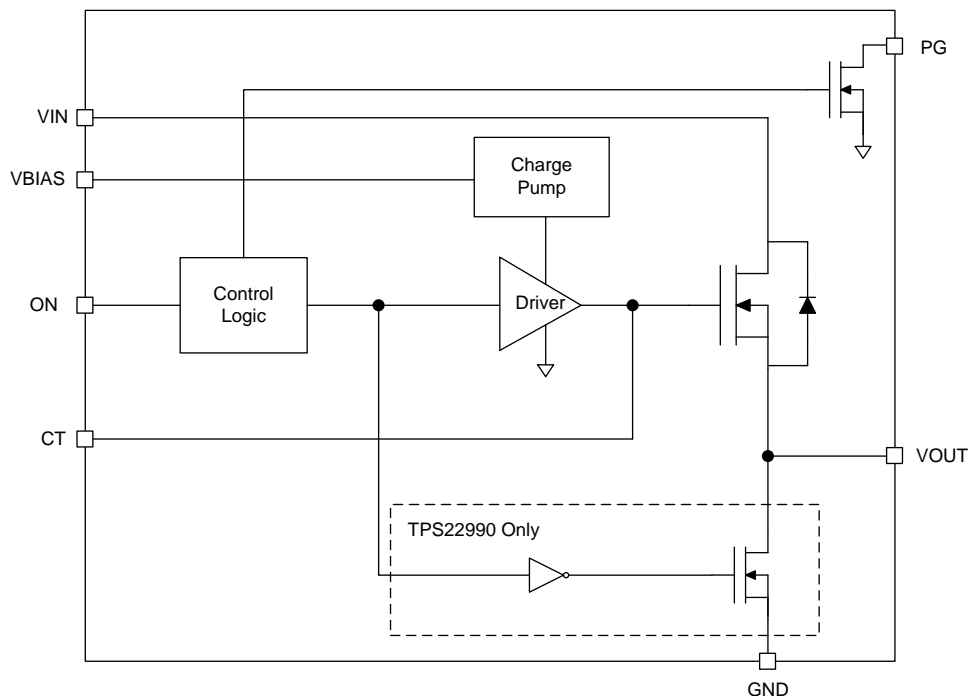
### 9.1 Overview

The TPS22990 device is a single channel load switch with a controlled adjustable turnon and integrated PG indicator. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6 V to 5.5 V and can support a maximum continuous current of 10 A. The wide input voltage range and high current capability enable the devices to be used across multiple designs and end equipment. 3.9-m $\Omega$  On-resistance minimizes the voltage drop across the load switch and power loss from the load switch.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through CT provides the design flexibility to trade off the inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

During shutdown, the device has very low leakage current, thereby reducing unnecessary leakages for downstream modules during standby. The TPS22990 has an optional 218- $\Omega$  On-chip resistor for quick discharge of the output when switch is disabled.

### 9.2 Functional Block Diagram



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### 9.3 Feature Description

#### 9.3.1 On and Off Control

The ON pin controls the state of the load switch. Asserting the pin high enables the switch. The minimum voltage that guarantees logic high is 1.2 V. This pin cannot be left floating and must be tied either high or low for proper functionality.



## Feature Description (continued)

### 9.3.2 Adjustable Rise Time

The TPS22990 has controlled rise time for inrush current control. A capacitor to GND on the CT pin adjusts the rise time. Without any capacitor on the CT, the rise time is at its minimum for fastest timing. The voltage on the CT pin can be as high as 15 V; therefore the minimum voltage rating for the CT capacitor must be 25 V for optimal performance. An approximate equation for the relationship between  $C_T$ ,  $V_{IN}$  and rise time when  $V_{BIAS}$  is set to 5 V is shown in Equation 1. As shown in Figure 35, rise time is defined as from 10% to 90% measurement on  $V_{OUT}$ .

$$t_R = (0.011 \times V_{IN} + 0.002) \times C_T + 4.7 \times V_{IN} + 7.8$$

where

- $t_R$  is the rise time (in  $\mu\text{s}$ )
  - $V_{IN}$  is the input voltage (in V)
  - $C_T$  is the capacitance value on the CT pin (in pF)
- (1)

Table 1 contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where  $V_{IN}$  and  $V_{BIAS}$  are already in steady state condition before the ON pin is asserted high.

**Table 1. Rise Time vs CT Capacitor**

$C_T$ (pF)	Rise Time ( $\mu\text{s}$ ) at 25°C $C_L = 0.1 \mu\text{F}$ , $C_{IN} = 1 \mu\text{F}$ , $R_L = 10 \Omega$ , $V_{BIAS} = 5 \text{ V}$				
	$V_{IN} = 5 \text{ V}$	$V_{IN} = 3.3 \text{ V}$	$V_{IN} = 1.8 \text{ V}$	$V_{IN} = 1.05 \text{ V}$	$V_{IN} = 0.6 \text{ V}$
0	30.5	24.8	17.5	12.6	9.5
220	44.6	34	22.7	15.8	11.4
470	56.6	42.2	27.1	18.8	13.2
1000	85	61.1	38.9	25.2	17.9
2200	154.6	107	64.7	40.9	27.7
4700	284.6	193.5	114.4	72.8	48.1
10000	598.5	404.8	233.2	146.9	98.6

### 9.3.3 Power Good (PG)

The TPS22990 has a power good (PG) output signal to indicate the gate of the pass FET is driven high and the switch is on with the On-resistance close to its final value (full load ready). The signal is an active high and open drain output which can be connected to a voltage source through an external pull up resistor,  $R_{PU}$ . This voltage source can be  $V_{OUT}$  from the TPS22990 or another external voltage.  $V_{BIAS}$  is required for PG to have a valid output. Equation 2 below shows the approximate equation for the relationship between  $C_T$ ,  $V_{IN}$  and PG turnon time ( $t_{PG,ON}$ ) when  $V_{BIAS}$  is set to 5 V.

$$t_{PG,ON} = (0.013 \times V_{IN} + 0.04) \times C_T + 4.7 \times V_{IN} + 129$$

where

- $t_{PG,ON}$  is the PG turnon time (in  $\mu\text{s}$ )
  - $V_{IN}$  is the input voltage (in V)
  - $C_T$  is the capacitance value on the CT pin (in pF)
- (2)

Table 2 contains PG turnon time values measured on a typical device.

**Table 2. PG Turnon Time vs CT Capacitor**

C <sub>T</sub> (pF)	Typical PG turnon time (us) at 25°C C <sub>L</sub> = 0.1 uF, C <sub>IN</sub> = 1 uF, R <sub>L</sub> = 10 Ω, V <sub>BIAS</sub> = 5 V, R <sub>PU</sub> = 10 kΩ				
	V <sub>IN</sub> = 5 V	V <sub>IN</sub> = 3.3 V	V <sub>IN</sub> = 1.8 V	V <sub>IN</sub> = 1.05 V	V <sub>IN</sub> = 0.6 V
0	151.9	144.4	137.5	133.9	131.3
220	177.7	164.6	153.3	147.1	143.5
470	200.9	183.2	167.4	159.2	154.4
1000	257.2	227.8	202.5	189.5	181.3
2200	390.6	332.3	282.4	257.1	241.6
4700	636.4	525.6	429.8	382.7	353.3
10000	1239	999.8	792.4	689.4	627.4

### 9.3.4 Quick Output Discharge (QOD) (TPS22990 Only)

The TPS22990 family includes an optional QOD feature. When the switch is disabled, a discharge resistor is connected between V<sub>OUT</sub> and GND. This resistor has a typical value of 218 Ω and prevents the output from floating while the switch is disabled.

## 9.4 Device Functional Modes

Table 3 shows the function table for TPS22990.

**Table 3. Function Table**

ON	V <sub>IN</sub> to V <sub>OUT</sub>	OUTPUT DISCHARGE <sup>(1)</sup>
L	OFF	ENABLED
H	ON	DISABLED

(1) This feature is in the TPS22990 only (not in TPS22990N).

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

#### 10.1.1 Input to Output Voltage Drop

The input to output voltage drop in the device is determined by the  $R_{ON}$  of the device and the load current. The  $R_{ON}$  of the device depends upon the  $V_{IN}$  and  $V_{BIAS}$  condition of the device. See the  $R_{ON}$  specification in the [Electrical Characteristics— \$V\_{BIAS} = 5\text{ V}\$](#)  table of this datasheet. Once the  $R_{ON}$  of the device is determined based upon the  $V_{IN}$  and  $V_{BIAS}$  conditions, use [Equation 3](#) to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- $\Delta V$  is the voltage drop from  $V_{IN}$  to  $V_{OUT}$
- $I_{LOAD}$  is the load current
- $R_{ON}$  is the on-resistance of the device for a specific  $V_{IN}$  and  $V_{BIAS}$
- An appropriate  $I_{LOAD}$  must be chosen such that the  $I_{MAX}$  specification of the device is not violated (3)

#### 10.1.2 Input Capacitor

It is recommended to use a capacitor between  $V_{IN}$  and GND close to the device pins. This helps limit the voltage drop on the input supply caused by transient inrush currents when the switch is turned on into a discharged capacitor at the load. A 1- $\mu\text{F}$  ceramic capacitor,  $C_{IN}$ , is usually sufficient. Higher values of  $C_{IN}$  can be used to further reduce the voltage drop. A  $C_{IN}$  to  $C_L$  ratio of 10 to 1 is recommended for minimizing  $V_{IN}$  dip caused by inrush currents during startup, where  $C_L$  is the load capacitance.

#### 10.1.3 Thermal Consideration

The maximum junction temperature should be limited to below 125°C. Use [Equation 4](#) to calculate the maximum allowable dissipation,  $P_{D(max)}$  for a given output load current and ambient temperature.  $R_{\theta JA}$  is highly dependent upon board layout.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where

- $P_{D(max)}$  is the maximum allowable power dissipation
- $T_{J(max)}$  is the maximum allowable junction temperature
- $T_A$  is the ambient temperature
- $R_{\theta JA}$  is the junction-to-air thermal impedance (4)

#### 10.1.4 PG Pull Up Resistor

The PG output is an open drain signal which connects to a voltage source through a pull up resistor  $R_{PU}$ . The PG signal can be used to drive the enable pins of downstream devices, EN. PG is active high, and its voltage is given by [Equation 5](#).

## Application Information (continued)

$$V_{PG} = V_{OUT} - (I_{PG,LK} + I_{EN,LK}) \times R_{PU}$$

where

- $V_{OUT}$  is the voltage where PG is tied to
- $I_{PG,LK}$  is the leakage current into PG pin
- $I_{EN,LK}$  is the leakage current into the EN pin driven by PG
- $R_{PU}$  is the pull up resistance

(5)

$V_{PG}$  needs to be higher than  $V_{IH, MIN}$  of the EN pin to be treated as logic high. The maximum  $R_{PU}$  is determined by [Equation 6](#).

$$R_{PU,MAX} = \frac{V_{OUT} - V_{IH,MIN}}{I_{PG,LK} + I_{EN,LK}}$$

(6)

When PG is disabled, with 1 mA current into PG pin ( $I_{PG} = 1 \text{ mA}$ ),  $V_{PG,OL}$  is less than 0.2 V and treated as logic low as long as  $V_{IL,MAX}$  of the EN pin is greater than 0.2 V. The minimum  $R_{PU}$  is determined by [Equation 7](#).

$$R_{PU,MIN} = \frac{V_{OUT}}{I_{PG} + I_{EN,LK}}$$

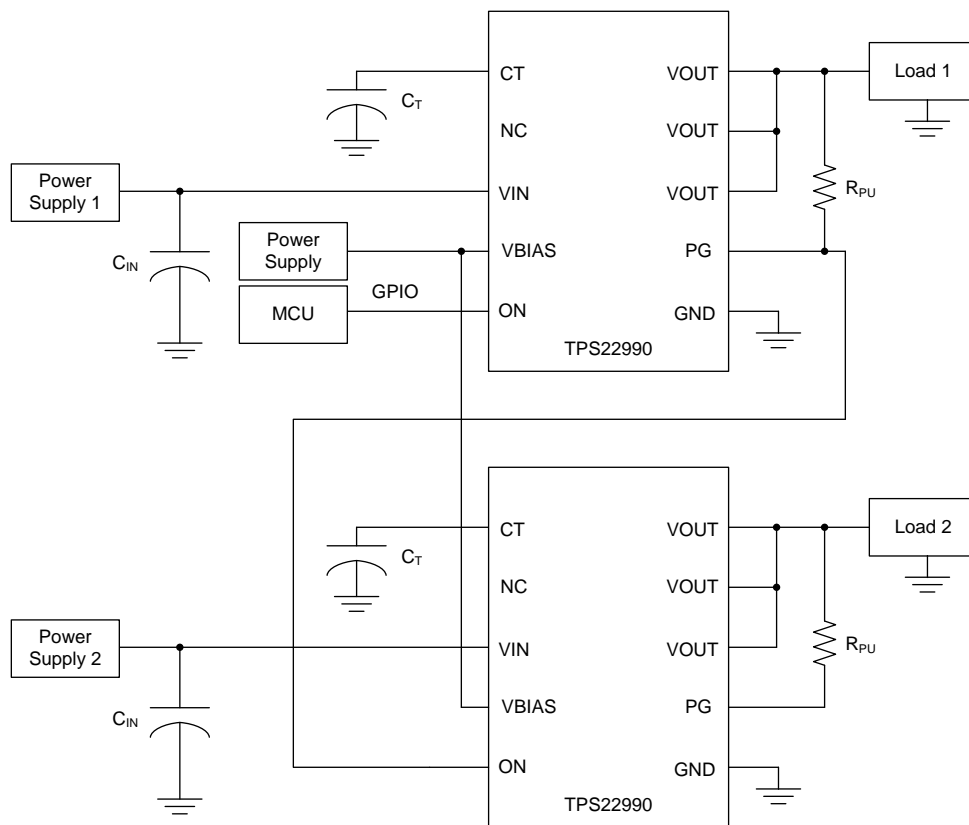
(7)

$R_{PU}$  can be chosen within the range defined by  $R_{PU,MIN}$  and  $R_{PU,MAX}$ .  $R_{PU} = 10 \text{ k}\Omega$  is used for characterization.

### 10.1.5 Power Sequencing

The TPS22990 has an integrated power good indicator which can be used for power sequencing. As shown in [Figure 36](#), the switch to the second load is controlled by the PG signal from the first switch. This ensures that the power to load 2 is only enabled after the power to load 1 is enabled and the first switch is full load ready.

Application Information (continued)



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Figure 36. Power Sequencing

10.1.6 Standby Power Reduction

Any end equipment that is being powered from a battery has a need to reduce current consumption in order to maintain the battery charge for a longer time. The TPS22990 devices help to accomplish this reduction by turning off the supply to the downstream modules that are in standby state and significantly reduce the leakage current overhead of the standby modules as shown in [Figure 37](#).

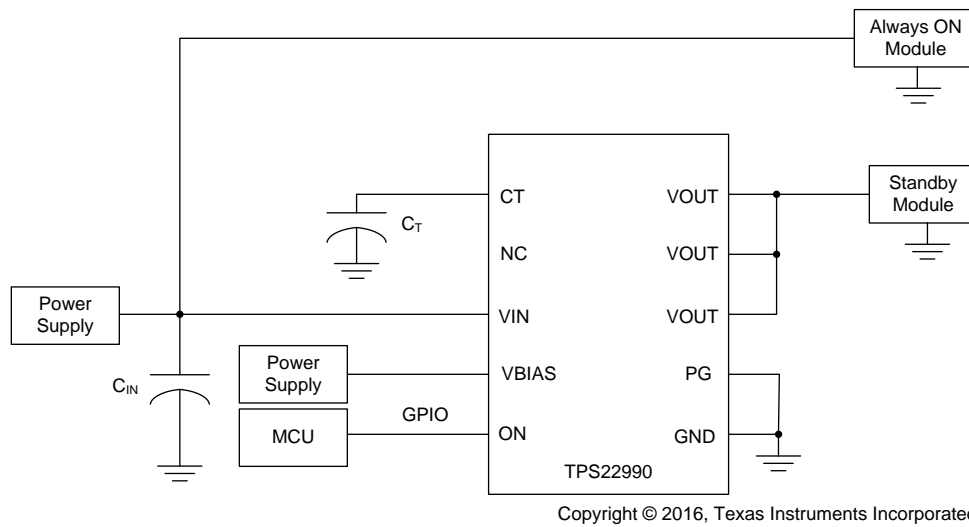
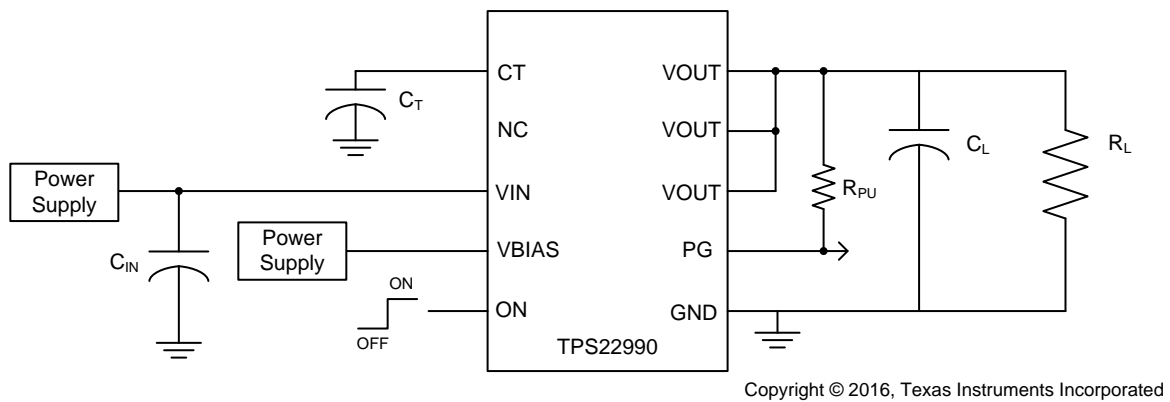
**Application Information (continued)**

**Figure 37. Standby Power Reduction**
**10.2 Typical Application**

Figure 38 demonstrates how to use TPS22990 to limit inrush current to output capacitance.


**Figure 38. Powering a Downstream Module**

## Typical Application (continued)

### 10.2.1 Design Requirements

For this design example, use the input parameters shown in [Table 4](#).

**Table 4. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
$V_{BIAS}$	3.3 V
$V_{IN}$	1.05 V
$C_L$	10 $\mu$ F
$R_L$	None
Maximum acceptable inrush current	100 mA

### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to  $V_{IN}$ . This charge arrives in the form of inrush current. Inrush current can be calculated using [Equation 8](#).

$$I_{INRUSH} = C_L \times \frac{dV}{dt} \approx C_L \times \frac{0.8 \times V_{IN}}{t_R}$$

where

- $I_{INRUSH}$  is the Inrush current
  - $C_L$  is the Load capacitance
  - $dV/dt$  is the Output slew rate
  - $V_{IN}$  is the Input voltage
  - $t_R$  is the rise time
- (8)

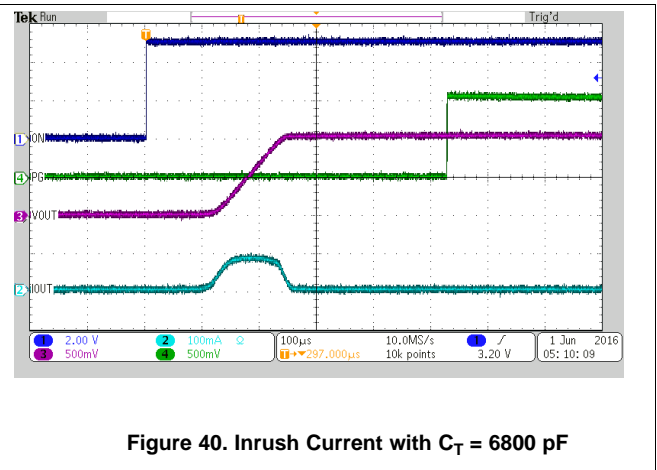
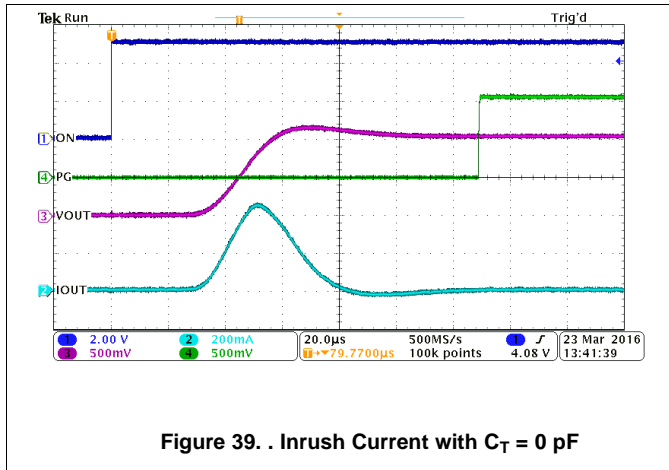
Minimum acceptable rise time can be calculated using the design requirements and the inrush current equation. See [Equation 9](#).

$$t_R = \frac{0.8 \times V_{IN} \times C_L}{I_{INRUSH}} = 84 \mu\text{s}$$

(9)

The TPS22990 has very fast timing without a CT capacitor ( $C_T$ ). The typical rise time is 12  $\mu$ s at  $V_{BIAS} = 3.3$  V,  $V_{IN} = 1.05$  V,  $R_L = 10 \Omega$ , and  $C_L = 0.1 \mu$ F. As shown in [Figure 39](#), the rise time is much smaller than 84  $\mu$ s and the inrush current is 460 mA without  $C_T$ . The  $C_T$  for the required rise time must be calculated using [Equation 1](#). For 84  $\mu$ s, the calculated  $C_T = 5259$  pF. [Figure 40](#) shows the inrush current is less than 100 mA with  $C_T = 6800$  pF.

### 10.2.3 Application Curves





## 11 Power Supply Recommendations

The device is designed to operate with a  $V_{BIAS}$  range of 2.5 V to 5.5 V, and a  $V_{IN}$  range of 0.6 V to  $V_{BIAS}$ . The supply must be well regulated and placed as close to the device terminal as possible with the recommended 1- $\mu$ F bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. In the case where the power supply is slow to respond to a large load current step, additional bulk may also be required. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10  $\mu$ F may be sufficient.

## 12 Layout

### 12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device terminal as possible to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for  $V_{IN}$ ,  $V_{OUT}$ , and GND helps minimize the parasitic electrical effects. The CT trace must be as short as possible to reduce parasitic capacitance.

### 12.2 Layout Example

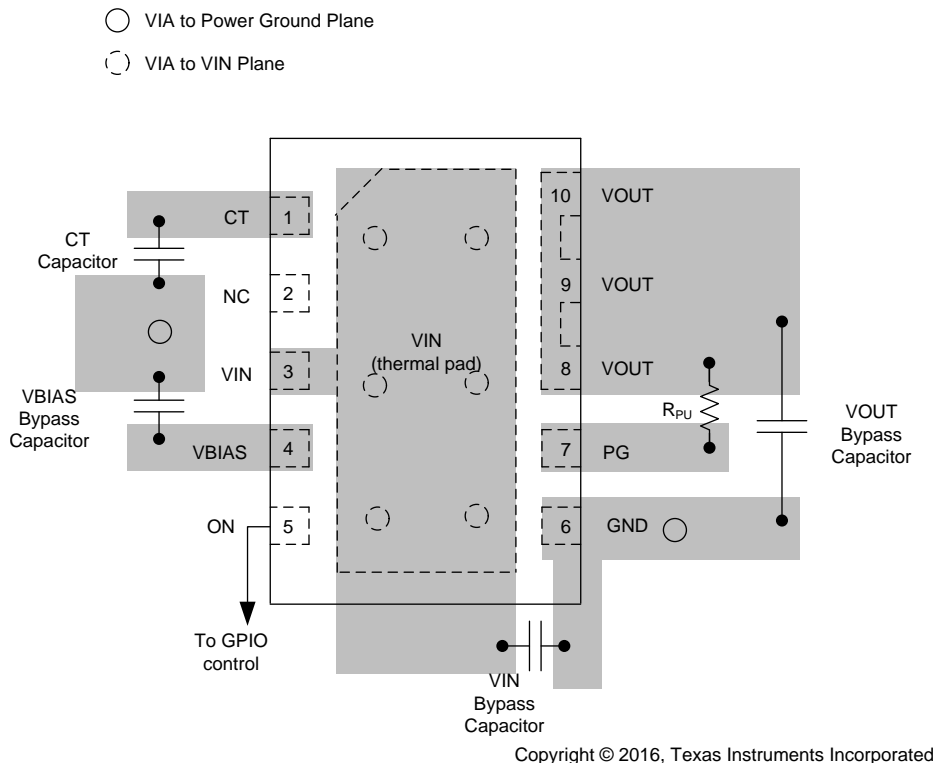


Figure 41. Layout Example

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

请参阅如下相关文档:

- 《TPS22990 负载开关评估模块》，[SLVUAS2](#)
- 《负载开关导通电阻基础》，[SLVA771](#)

### 13.2 接收文档更新通知

如需接收文档更新通知，请访问 [ti.com](http://ti.com) 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 13.3 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22990DMLR	ACTIVE	WSON	DML	10	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990	<a href="#">Samples</a>
TPS22990DMLT	ACTIVE	WSON	DML	10	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990	<a href="#">Samples</a>
TPS22990NDMLR	ACTIVE	WSON	DML	10	3000	RoHS & Green	Call TI   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990N	<a href="#">Samples</a>
TPS22990NDMLT	ACTIVE	WSON	DML	10	250	RoHS & Green	Call TI   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	RB990N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

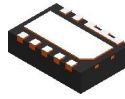
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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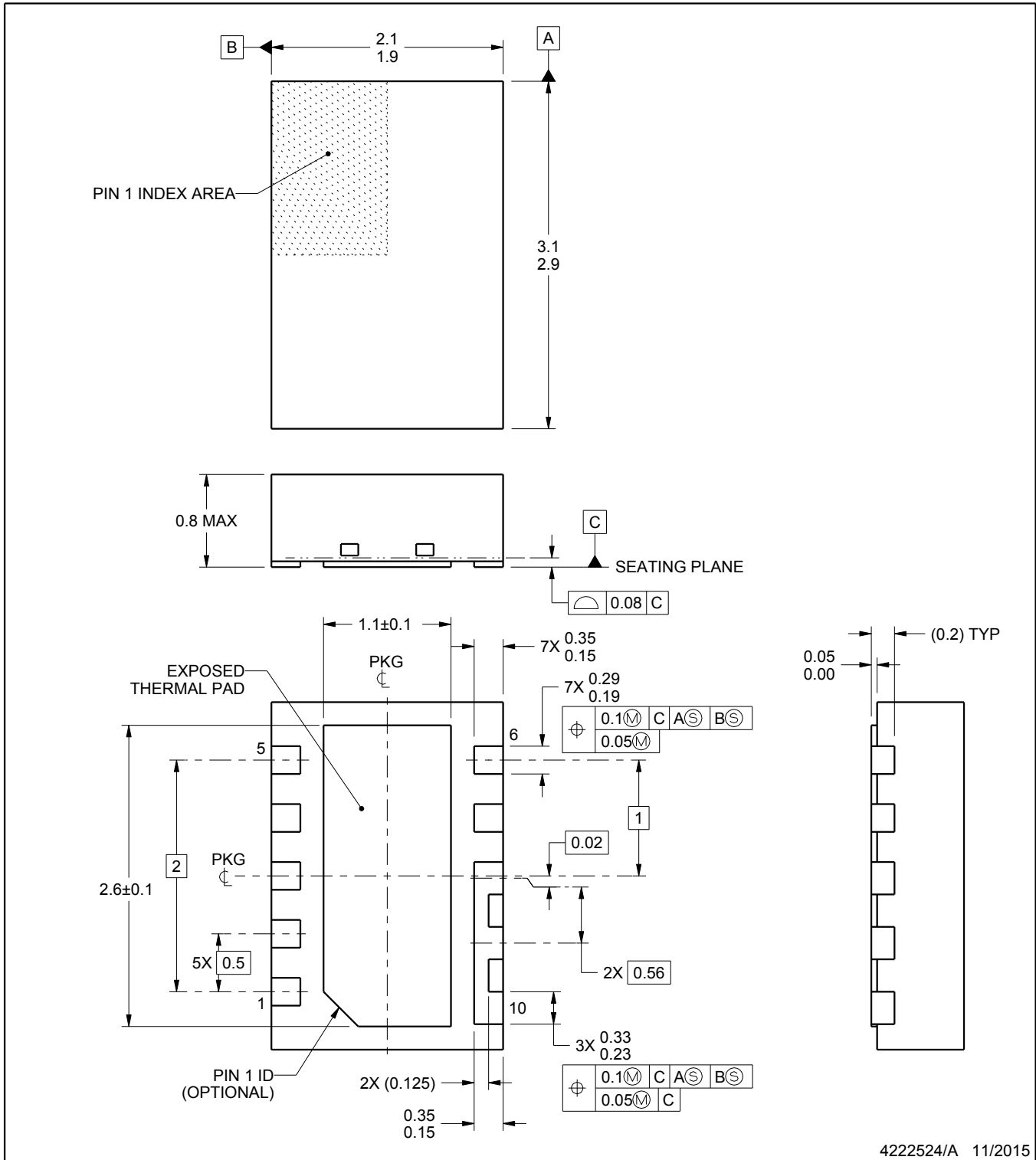
# DML0010A



# PACKAGE OUTLINE

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222524/A 11/2015

**NOTES:**

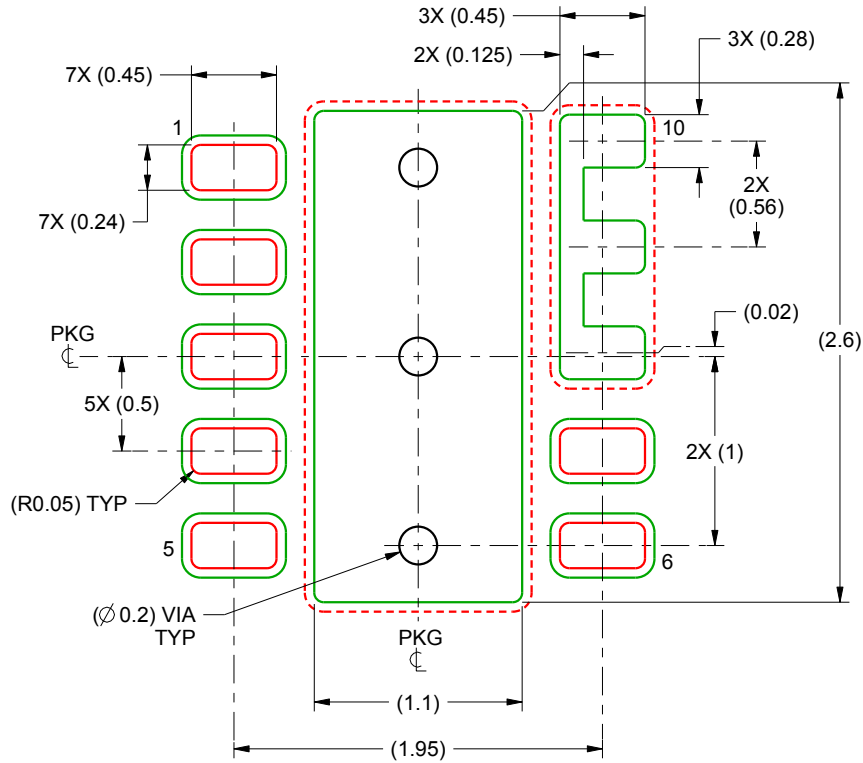
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

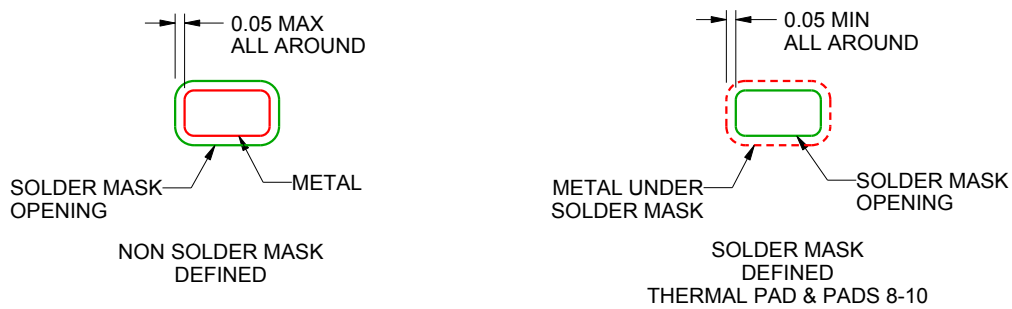
DML0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

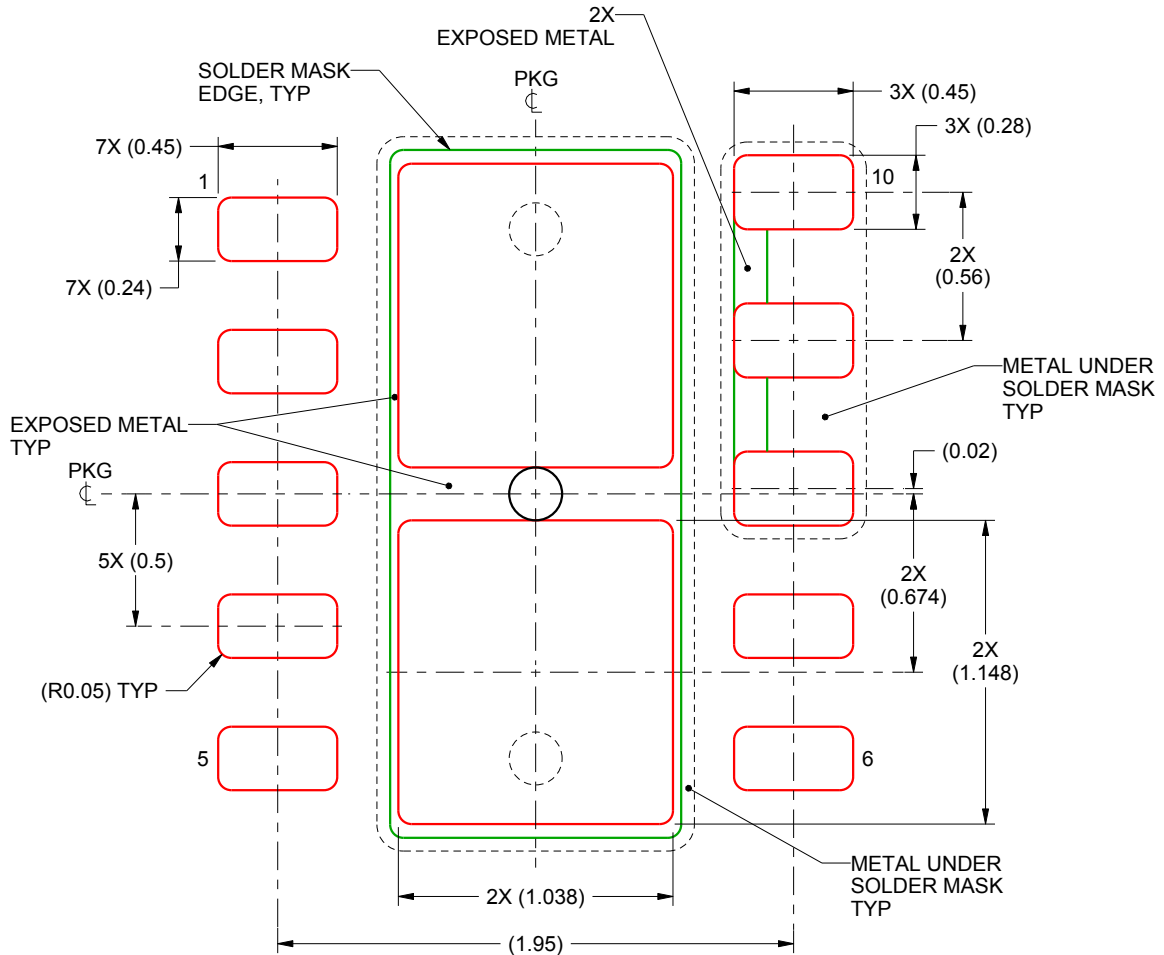
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DML0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 83% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:35X

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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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