

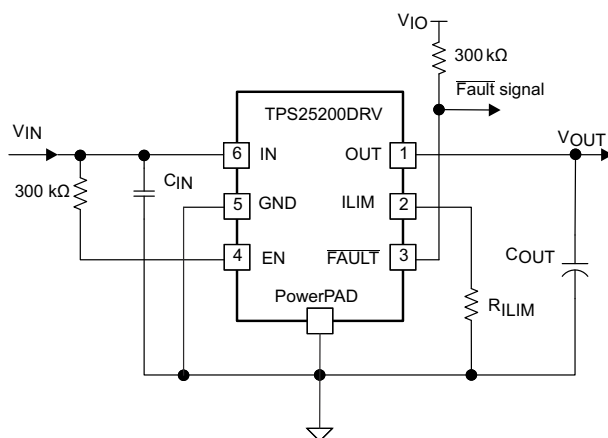
## 具有高精度可调电流限值和过压钳位的 TPS25200 5V 电子保险丝

### 1 特性

- 2.5V 至 6.5V 工作电压
- 输入可耐受高达 20V 的电压
- 7.6V 输入过压关断
- 5.25V 至 5.55V 固定过压钳位
- 0.6  $\mu$ s 过压锁定响应
- 3.5  $\mu$ s 短路响应
- 集成式 60m $\Omega$  高侧 MOSFET
- 高达 2.5A 的持续负载电流
- 2.9 A 电流下的限流精度为  $\pm 6\%$
- 禁用时反向电流阻断
- 内置软启动
- 与 TPS2553 引脚到引脚兼容
- 通过 UL 2367 认证
  - 文件编号 169910
  - $R_{ILIM} \geq 33k\Omega$  (最大电流为 3.12A)

### 2 应用

- USB 电源开关
- USB 从设备
- 手机/智能电话
- 3G、4G 无线数据卡
- 固态硬盘 (SSD)
- 3V 或 5V 适配器供电设备



简化版原理图

### 3 说明

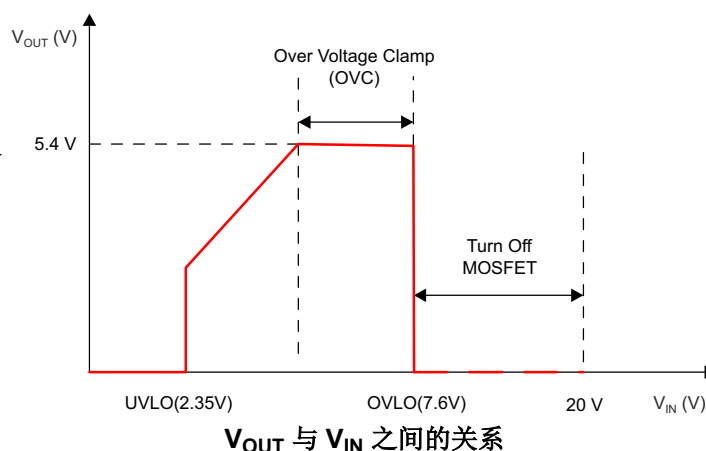
TPS25200 是一款具有高精度电流限值和过压钳位的 5V 电子保险丝。此器件可在过压和过流事件发生期间为负载和电源提供可靠保护。

TPS25200 是一款用于保护负载的智能开关，可耐受 20V 的输入电压。如果在输入端施加了错误电压，输出端可将电压限制在 5.4V，以保护负载。如果输入端的电压超过 7.6V，此器件将断开负载，以防止对器件和/或负载造成损坏。

TPS25200 具有 60m $\Omega$  的内部电源开关，可用于在多种异常情况下保护电源、器件和负载。此器件提供高达 2.5A 的持续负载电流。通过一个连接到地的电阻，可对限流值在 85mA 到 2.9A 范围内进行设置。当发生过载时，输出电流被限制在由  $R_{ILIM}$  设定的电流值上如果出现持续过载，TPS25200 将最终进入热关断模式，从而避免自身发生损坏。

#### 器件信息

| 订货编号     | 封装       | 封装尺寸            |
|----------|----------|-----------------|
| TPS25200 | WSON (6) | 2.00mm × 2.00mm |



$V_{OUT}$  与  $V_{IN}$  之间的关系



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision D (February 2020) to Revision E (June 2021)</b>                       | <b>Page</b> |
|--|-------------|
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....   | 1           |
| • Corrected package type.....  | 3           |
| • Corrected package type.....  | 4           |
| <b>Changes from Revision C (September 2017) to Revision D (February 2020)</b>                  | <b>Page</b> |
| • Updated <a href="#">Figure 9-5</a> .....   | 15          |
| <b>Changes from Revision B (February 2017) to Revision C (September 2017)</b>                  | <b>Page</b> |
| • 在 <a href="#">器件信息</a> 表中将封装从 SON 更改为 WSON.....  | 1           |
| <b>Changes from Revision A (March 2014) to Revision B (February 2017)</b>                      | <b>Page</b> |
| • 向 <a href="#">特性</a> 部分添加了 UL 认证状态.....  | 1           |
| <b>Changes from Revision * (March 2014) to Revision A (March 2014)</b>                         | <b>Page</b> |
| • Changed the $t_{off}$ TYP value From: 0.24 ms To: 0.22 ms .....                              | 6           |
| • Added condition: $V_{EN} = V_{IN} = 0$ V to <a href="#">Figure 6-3</a> .....                 | 7           |
| • Changed <a href="#">Figure 6-8</a> graph title From: Discharge Resistance To: $V_{IN}$ ..... | 7           |
| • Changed <a href="#">方程式 4</a> From = 2470 mA to = 2479 mA.....                               | 16          |

## 5 Pin Configuration and Functions

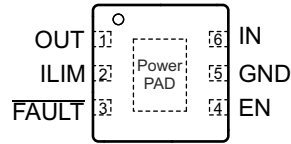


图 5-1. DRV Package 6-Pin WSON Top View

表 5-1. Pin Functions

| PIN       |     | I/O | DESCRIPTION  |
|-----------|-----|-----|--|
| NAME      | NO. |     |  |
| EN        | 4   | I   | Logic-level control input. When is driven high, the power switch is enabled. When it is driven low, turn power switch off. This pin cannot be left floating and it must be limited below the absolute maximum rating if tied to $V_{IN}$ |
| FAULT     | 3   | O   | Active-low open-drain output, asserted during overcurrent, overvoltage or overtemperature. Connect a pull up resistor to the logic I/O voltage   |
| GND       | 5   | —   | Ground connection; connect externally to PowerPAD  |
| ILIM      | 2   | O   | External resistor used to set current-limit threshold; Recommended $33\text{ k}\Omega \leq R_{ILIM} \leq 1100\text{ k}\Omega$  |
| IN        | 6   | I   | Input voltage; connect a 0.1- $\mu\text{F}$ or greater ceramic capacitor from IN to GND as close to the IC as possible   |
| OUT       | 1   | O   | Protected power switch $V_{OUT}$   |
| PowerPAD™ | PAD | —   | Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND terminal externally   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted) <sup>(1)</sup>

|           |                                       | MIN                | MAX | UNIT         |
|-----------|---------------------------------------|--------------------|-----|--------------|
|           | Voltage on IN                         | - 0.3              | 20  | V            |
|           | Voltage on OUT, EN, ILIM, FAULT       | - 0.3              | 7   | V            |
|           | Voltage from IN to OUT                | - 7                | 20  | V            |
| $I_O$     | Continuous output current             | Thermally Limited  |     |              |
|           | Continuous FAULT output sink current  |                    | 25  | mA           |
|           | Continuous ILIM output source current |                    | 150 | $\mu$ A      |
| $T_J$     | Operating junction temperature        | Internally limited |     |              |
| $T_{stg}$ | Storage temperature                   | - 65               | 150 | $^{\circ}$ C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolutemaximum- rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|             |                         | VALUE  | UNIT       |
|-------------|-------------------------|--|------------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | $\pm$ 2000 |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | $\pm$ 500  |
|             |                         |  | V          |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)

|             |                                  | MIN  | MAX  | UNIT         |
|-------------|----------------------------------|------|------|--------------|
| $V_{IN}$    | Input voltage of IN              | 2.5  | 6.5  | V            |
| $V_{EN}$    | Enable terminal voltage          | 0    | 6.5  | V            |
| $I_{FAULT}$ | Continuous FAULT sink current    | 0    | 10   | mA           |
| $I_{OUT}$   | Continuous output current of OUT |      | 2.5  | A            |
| $R_{ILIM}$  | Current-limit set resistors      | 33   | 1100 | k $\Omega$   |
| $T_J$       | Operating junction temperature   | - 40 | 125  | $^{\circ}$ C |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | TPS25200                                     |      | UNIT           |
|-------------------------------|--|------|----------------|
|                               | DRV (WSON)                                   |      |                |
|                               | 6 PINS                                       |      |                |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 66.5 | $^{\circ}$ C/W |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance    | 83.4 | $^{\circ}$ C/W |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 36.1 | $^{\circ}$ C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 1.6  | $^{\circ}$ C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 36.5 | $^{\circ}$ C/W |
| $\theta_{JCbot}$              | Junction-to-case (bottom) thermal resistance | 7.6  | $^{\circ}$ C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Conditions are  $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$  and  $2.5\text{ V} \leq V_{\text{IN}} \leq 6.5\text{ V}$ .  $V_{\text{EN}} = V_{\text{IN}}$ ,  $R_{\text{ILIM}} = 33\text{ k}\Omega$ . Positive current into terminals. Typical value is at  $25^{\circ}\text{C}$ . All voltages are with respect to GND (unless otherwise noted).

| PARAMETER  |  | TEST CONDITIONS   | MIN  | TYP                | MAX  | UNIT          |
|--|--|---|--|--------------------|------|---------------|
| <b>POWER SWITCH</b>                                    |  |   |  |                    |      |               |
| $r_{\text{DS(on)}}$ IN - OUT resistance <sup>(1)</sup> |  | $2.5\text{ V} \leq V_{\text{IN}} \leq 5\text{ V}$ ,<br>$I_{\text{OUT}} = 2.5\text{ A}$  | $T_J = 25^{\circ}\text{C}$                               | 60                 | 70   | m $\Omega$    |
|  |  |   | $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$  | 60                 | 90   |               |
|  |  |   | $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$ | 60                 | 99   |               |
| <b>ENABLE INPUT EN</b>                                 |  |   |  |                    |      |               |
|  | EN terminal turnon threshold               | Input rising  |  |                    | 1.9  | V             |
|  | EN terminal turnoff threshold              | Input falling   | 0.6  |                    |      | V             |
|  | Hysteresis                                 |   |  | 330 <sup>(2)</sup> |      | mV            |
| $I_{\text{EN}}$  | Leakage current                            | $V_{\text{EN}} = 0\text{ V}$ or $5.5\text{ V}$  | -2   |                    | 2    | $\mu\text{A}$ |
| <b>DISCHARGE</b>                                       |  |   |  |                    |      |               |
| $R_{\text{DCHG}}$                                      | OUT discharge resistance                   | $V_{\text{OUT}} = 5\text{ V}$ , $V_{\text{EN}} = 0\text{ V}$  |  | 480                | 625  | $\Omega$      |
| <b>CURRENT LIMIT</b>                                   |  |   |  |                    |      |               |
| $I_{\text{OS}}$  | Current - limit, See <a href="#">图 7-4</a> | $R_{\text{ILIM}} = 33\text{ k}\Omega$   | 2773   | 2952               | 3127 | mA            |
|  |  | $R_{\text{ILIM}} = 40.2\text{ k}\Omega$   | 2270   | 2423               | 2570 |               |
|  |  | $R_{\text{ILIM}} = 56\text{ k}\Omega$   | 1620   | 1740               | 1860 |               |
|  |  | $R_{\text{ILIM}} = 80.6\text{ k}\Omega$   | 1110   | 1206               | 1300 |               |
|  |  | $R_{\text{ILIM}} = 150\text{ k}\Omega$  | 590  | 647                | 710  |               |
|  |  | $R_{\text{ILIM}} = 1100\text{ k}\Omega$   | 40   | 83                 | 130  |               |
| <b>OVERVOLTAGE LOCKOUT, IN</b>                         |  |   |  |                    |      |               |
| $V_{\text{(OVLO)}}$                                    | IN rising OVLO threshold voltage           | IN rising   | 6.8  | 7.6                | 8.45 | V             |
|  | Hysteresis                                 |   |  | 70 <sup>(2)</sup>  |      | mV            |
| <b>VOLTAGE CLAMP, OUT</b>                              |  |   |  |                    |      |               |
| $V_{\text{(OVC)}}$                                     | OUT clamp voltage threshold                | $C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$ , $V_{\text{IN}} = 6.5\text{ V}$   | 5.25   | 5.4                | 5.55 | V             |
| <b>SUPPLY CURRENT</b>                                  |  |   |  |                    |      |               |
| $I_{\text{IN(off)}}$                                   | Supply current, low-level output           | $V_{\text{EN}} = 0\text{ V}$ , $V_{\text{IN}} = 5\text{ V}$   |  | 0.8                | 5    | $\mu\text{A}$ |
|  |  | $V_{\text{EN}} = 0$ or $5\text{ V}$ , $V_{\text{IN}} = 20\text{ V}$   |  | 1000               | 1700 |               |
| $I_{\text{IN(on)}}$                                    | Supply current, high-level output          | $V_{\text{IN}} = 5\text{ V}$ ,<br>No load on OUT  | $R_{\text{ILIM}} = 33\text{ k}\Omega$                    | 143                | 200  | $\mu\text{A}$ |
|  |  |   | $R_{\text{ILIM}} = 150\text{ k}\Omega$                   | 134                | 190  |               |
| $I_{\text{REV}}$                                       | Reverse leakage current                    | $V_{\text{OUT}} = 6.5\text{ V}$ , $V_{\text{IN}} = V_{\text{EN}} = 0\text{ V}$ , $T_J = 25^{\circ}\text{C}$ ,<br>measure $I_{\text{OUT}}$ |  | 3                  | 5    | $\mu\text{A}$ |
| <b>UNDERVOLTAGE LOCKOUT, IN</b>                        |  |   |  |                    |      |               |
| $V_{\text{UVLO}}$                                      | IN rising UVLO threshold voltage           | IN rising   |  | 2.35               | 2.45 | V             |
|  | Hysteresis                                 |   |  | 30 <sup>(2)</sup>  |      | mV            |
| <b>FAULT FLAG</b>                                      |  |   |  |                    |      |               |
| $V_{\text{OL}}$  | Output low voltage, FAULT                  | $I_{\text{FAULT}} = 1\text{ mA}$  |  | 50                 | 180  | mV            |
|  | Off-state leakage                          | $V_{\text{FAULT}} = 6.5\text{ V}$   |  |                    | 1    | $\mu\text{A}$ |
| <b>THERMAL SHUTDOWN</b>                                |  |   |  |                    |      |               |

Conditions are  $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$  and  $2.5\text{ V} \leq V_{\text{IN}} \leq 6.5\text{ V}$ .  $V_{\text{EN}} = V_{\text{IN}}$ ,  $R_{\text{ILIM}} = 33\text{ k}\Omega$ . Positive current into terminals. Typical value is at  $25^{\circ}\text{C}$ . All voltages are with respect to GND (unless otherwise noted).

| PARAMETER   | TEST CONDITIONS | MIN               | TYP | MAX | UNIT |
|---|-----------------|-------------------|-----|-----|------|
| Thermal shutdown threshold, OTSD2                       |                 | 155               |     |     | °C   |
| Thermal shutdown threshold only in current-limit, OTSD1 |                 | 135               |     |     |      |
| Hysteresis  |                 | 20 <sup>(2)</sup> |     |     |      |

- (1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
- (2) These parameters are provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

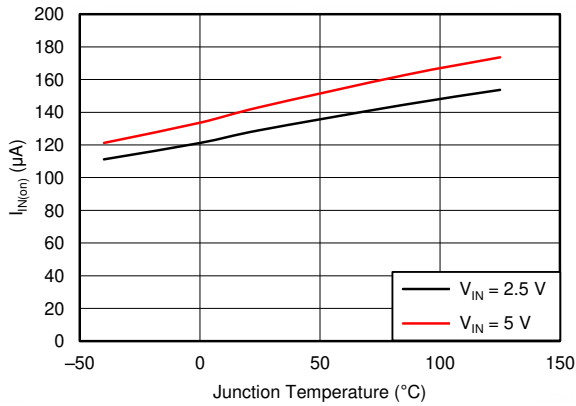
## 6.6 Timing Requirements

Conditions are  $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$  and  $2.5\text{ V} \leq V_{\text{IN}} \leq 6.5\text{ V}$ .  $V_{\text{EN}} = V_{\text{IN}}$ ,  $R_{\text{ILIM}} = 33\text{ k}\Omega$ . Positive current are into terminals. Typical value is at  $25^{\circ}\text{C}$ . All voltages are with respect to GND (unless otherwise noted)

|                                 |                             | TEST CONDITIONS   | MIN | TYP                | MAX | UNIT          |    |
|---------------------------------|-----------------------------|---|-----|--------------------|-----|---------------|----|
| <b>POWER SWITCH</b>             |                             |   |     |                    |     |               |    |
| $t_r$                           | OUT voltage rise time       | $C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$ , (see <a href="#">图 7-2</a> )   |     | 2.05               | 3.2 | ms            |    |
| $t_f$                           | OUT voltage fall time       |   |     | 0.18               | 0.2 |               |    |
| <b>ENABLE INPUT EN</b>          |                             |   |     |                    |     |               |    |
| $t_{\text{on}}$                 | Turnon time                 | $2.5\text{ V} \leq V_{\text{IN}} \leq 5\text{ V}$ , $C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$ , (see <a href="#">图 7-2</a> ) |     | 5.12               | 7.3 | ms            |    |
| $t_{\text{off}}$                | Turnoff time                |   |     | 0.22               | 0.3 | ms            |    |
| <b>CURRENT LIMIT</b>            |                             |   |     |                    |     |               |    |
| $t_{(\text{IOS})}$              | Short-circuit response time | $V_{\text{IN}} = 5\text{ V}$ (see <a href="#">图 7-4</a> )   |     | 3.5 <sup>(1)</sup> |     | $\mu\text{s}$ |    |
| <b>OVERVOLTAGE LOCKOUT, IN</b>  |                             |   |     |                    |     |               |    |
| $t_{(\text{OVLO\_off\_delay})}$ | Turnoff delay for OVLO      | $V_{\text{IN}}$ 5 V to 10 V with 1-V/ $\mu\text{s}$ ramp up rate, $V_{\text{OUT}}$ with 100- $\Omega$ load                                  |     | 0.6 <sup>(1)</sup> |     | $\mu\text{s}$ |    |
| <b>FAULT FLAG</b>               |                             |   |     |                    |     |               |    |
|                                 | FAULT deglitch              | FAULT assertion or de-assertion due to overcurrent condition  |     | 5                  | 8   | 12            | ms |

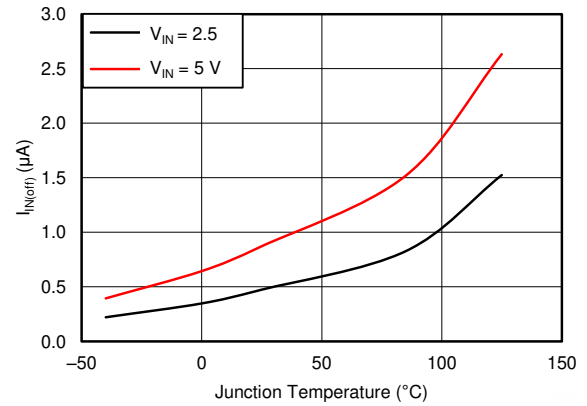
- (1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

## 6.7 Typical Characteristics



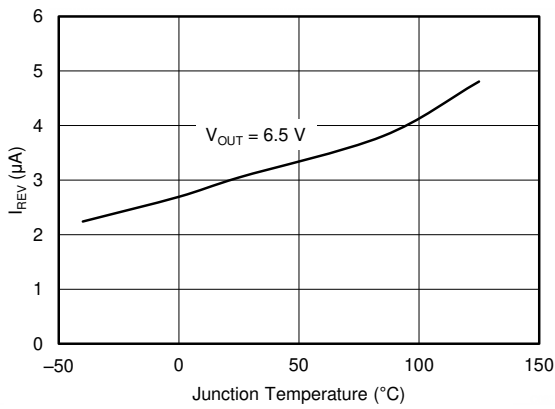
$R_{ILIM} = 33\text{ K}\Omega$

图 6-1.  $I_{IN(on)}$  vs Junction Temperature



$R_{ILIM} = 33\text{ K}\Omega$

图 6-2.  $I_{IN(off)}$  vs Junction Temperature



$V_{EN} = V_{IN} = 0\text{ V}$

图 6-3.  $I_{REV}$  vs Junction Temperature

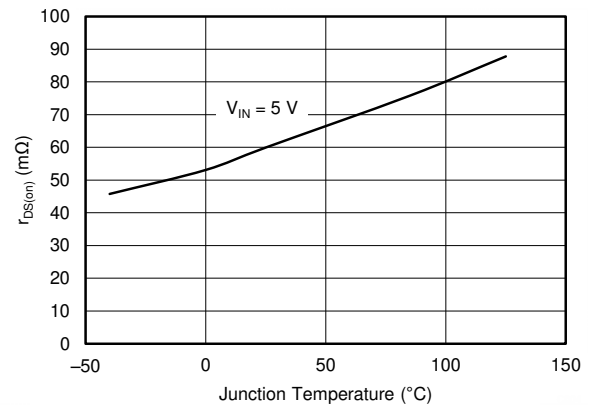
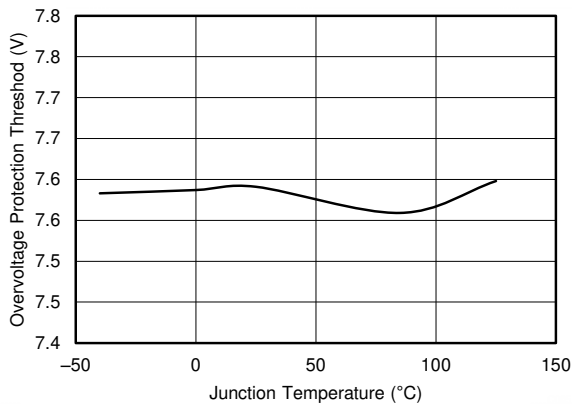


图 6-4.  $r_{DS(ON)}$  vs Junction Temperature



$V_{EN} = V_{IN} = 0\text{ V}$

图 6-5.  $V_{(OVLO)}$  vs Junction Temperature

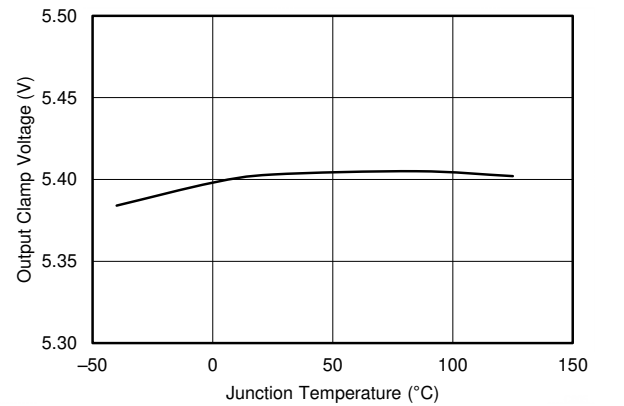
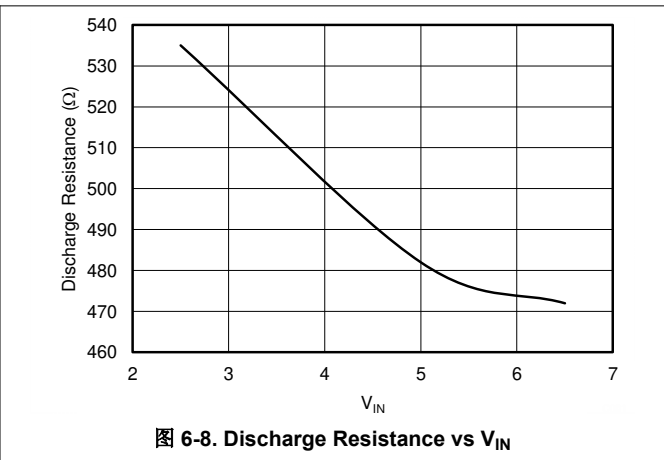
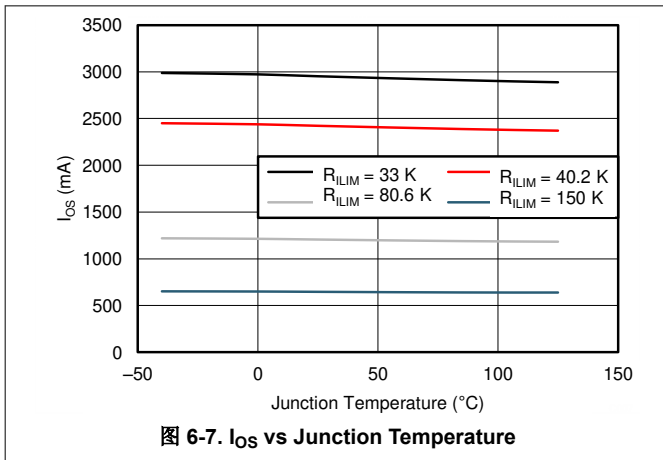


图 6-6.  $V_{O(VC)}$  vs Junction Temperature  
 $C_L = 1\ \mu\text{F}$      $R_L = 100\ \Omega$      $V_{IN} = 6.5\text{ V}$

### 6.7 Typical Characteristics (continued)





## 7 Parameter Measurement Information

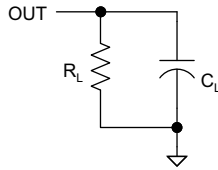


图 7-1. Output Rise-Fall Test Load

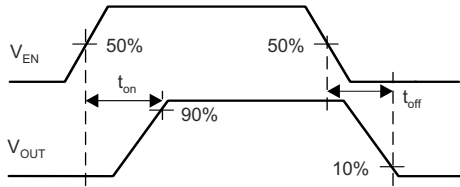


图 7-3. Enable Timing, Active High Enable

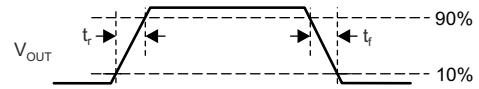


图 7-2. Power-On and Off Timing

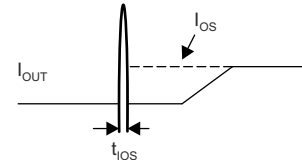


图 7-4. Output Short Circuit Parameters

## 8 Detailed Description

### 8.1 Overview

The TPS25200 is an intelligent low voltage switch or e-Fuse with robust overcurrent and overvoltage protection which are suitable for a variety of applications.

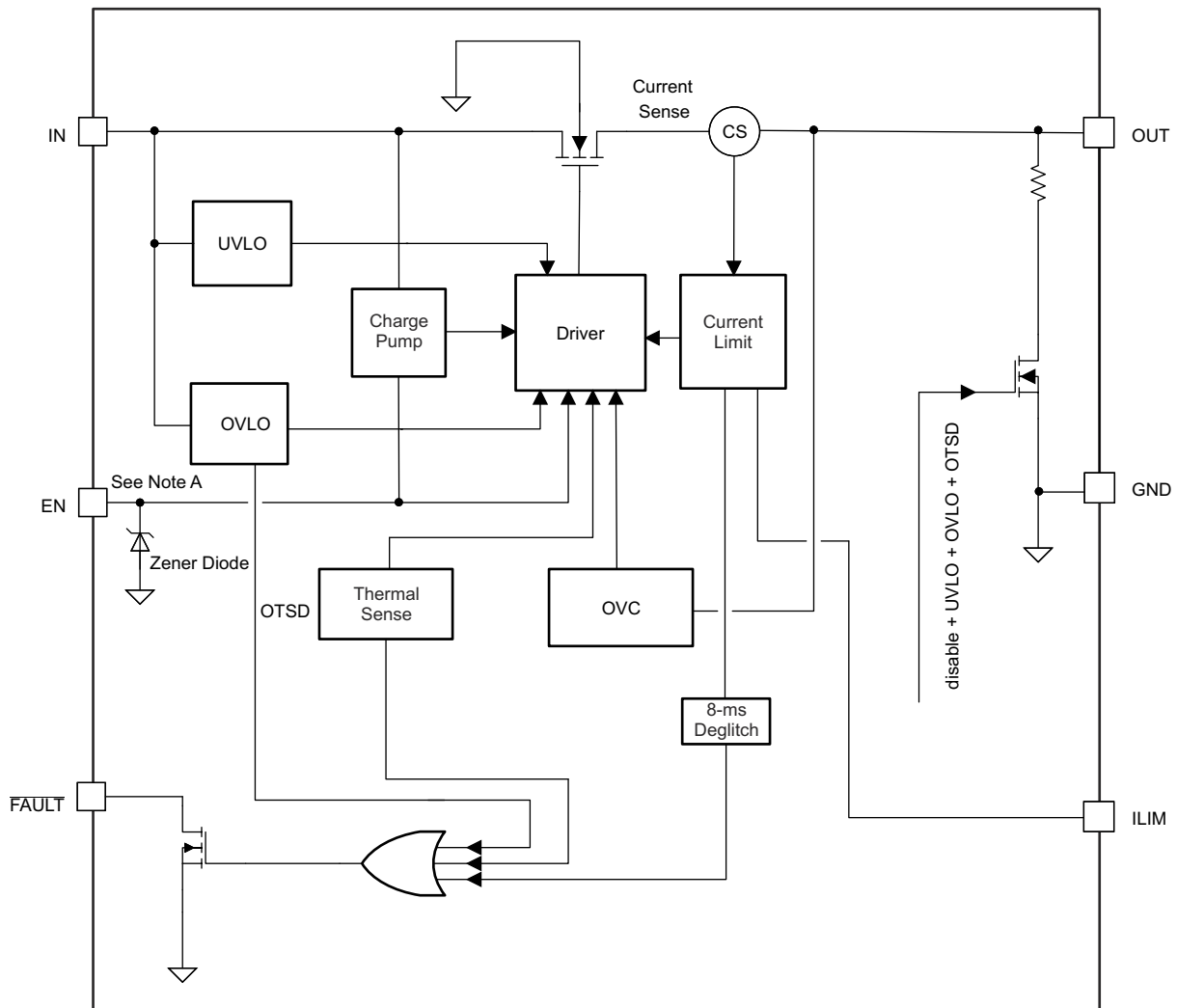
The TPS25200 current limited power switch uses N-channel MOSFETs in applications requiring up to 2.5 A of continuous load current. The device allows the user to program the current-limit threshold between 85 mA and 2.9 A (typical) via an external resistor. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS25200 Input can withstand 20-V DC voltage, but clamps  $V_{OUT}$  to a precision regulated 5.4 V and shuts down in the event  $V_{IN}$  exceeds 7.6 V. The device also integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply while the fast response short circuit protection isolates the load when a short circuit is detected.

The additional features include:

- Enable the device can be put into a sleep mode for portable applications.
- Overtemperature protection to safely shutdown in the event of an overcurrent event or a slight overvoltage event where the  $V_{OUT}$  clamp is engaged over an extended period of time.
- Deglitched fault reporting to filter the Fault signal to ensure the TPS25200 do not provide false fault alerts.
- Output discharge pull-down to help ensure a load is in fact off and not in some undefined operational state.
- Reverse blocking when disabled to prevent back-drive from an active load inadvertently causing undetermined behavior in the application.

## 8.2 Functional Block Diagram



A. 6.4-V Typical Clamp Voltage

## 8.3 Feature Description

### 8.3.1 Enable

This logic enable input controls the power switch and device supply current. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

EN can be tied to  $V_{IN}$  with a pull up resistor, and is protected with an integrated zener diode. Use a sufficiently large (300-k $\Omega$ ) pull up resistor to ensure that the  $V_{(EN)}$  is limited below the absolute maximum rating.

### 8.3.2 Thermal Sense

The TPS25200 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS25200 device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (minimum) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS25200 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (minimum) regardless of whether the power switch is in current limit and turns on the power switch after the device has cooled approximately 20°C. The TPS25200 continues to cycle off and on until the fault is removed.

### 8.3.3 Overcurrent Protection

The TPS25200 thermally protects itself by thermal cycling during an extended overcurrent condition. The device turns off when the junction temperature exceeds 135°C (typical) while in current limit. The device remains off until the junction temperature cools 20°C (typical) and then restarts. The TPS25200 cycles on/off until the overload is removed (see [Figure 9-13](#) and [Figure 9-16](#)).

The TPS25200 responds to an overcurrent condition by limiting their output current to the  $I_{OS}$  levels shown in [Figure 7-4](#). When an overcurrent condition is detected, the device maintains a constant output current and the output voltage is reduced accordingly. During an over current event, two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS25200 ramps the output current to  $I_{OS}$ . The TPS25200 devices limit the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time  $t_{IOS}$  (see [Figure 7-4](#)). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to  $I_{OS}$ . Similar to the previous case, the TPS25200 limits the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

### 8.3.4 FAULT Response

The  $\overline{\text{FAULT}}$  open-drain output is asserted (active low) during an overcurrent, overtemperature or overvoltage condition. The TPS25200 asserts the  $\overline{\text{FAULT}}$  signal until the fault condition is removed and the device resumes normal operation. The TPS25200 is designed to eliminate false  $\overline{\text{FAULT}}$  reporting by using an internal delay "deglitch" circuit for overcurrent (8-ms typical) conditions without the need for external circuitry. This ensures that  $\overline{\text{FAULT}}$  is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions.

The  $\overline{\text{FAULT}}$  signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents  $\overline{\text{FAULT}}$  oscillation during an overtemperature event.

The  $\overline{\text{FAULT}}$  signal is not deglitched when the MOSFET is disabled into OVLO or out of OVLO. The TPS25200 does not assert the  $\overline{\text{FAULT}}$  during output voltage clamp mode.

Connect  $\overline{\text{FAULT}}$  with a pull up resistor to a low voltage I/O rail.

### 8.3.5 Output Discharge

A 480- $\Omega$  (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS25200 is in UVLO, disabled or OVLO. The pull down capability decreases as  $V_{IN}$  decreases ([Figure 6-8](#)).

## 8.4 Device Functional Modes

The TPS25200  $V_{IN}$  can withstand up to 20 V. Within 0 V to 20 V range, it can be divided to four modes as shown in 图 8-1.

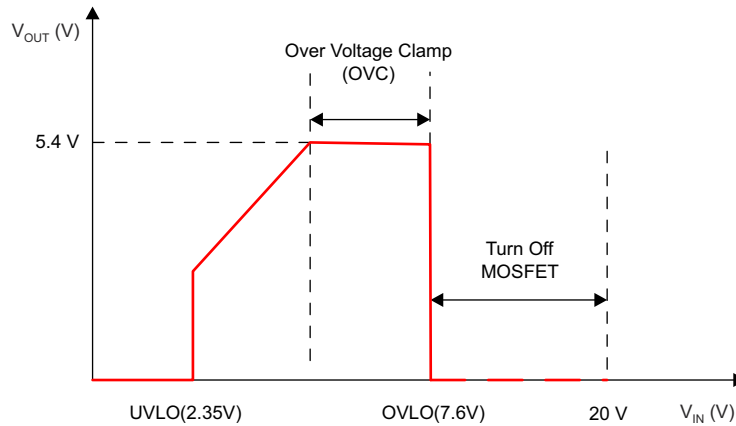


图 8-1. Output vs Input Voltage

### 8.4.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on and off cycling due to input voltage droop during turnon.

### 8.4.2 Overcurrent Protection (OCP)

When  $2.35\text{ V} < V_{IN} < 5.4\text{ V}$ , the TPS25200 is a traditional power switch, providing overcurrent protection.

### 8.4.3 Overvoltage Clamp (OVC)

When  $5.4\text{ V} < V_{IN} < 7.6\text{ V}$ , the overvoltage clamp (OVC) circuit clamps the output voltage to 5.4 V. Within this  $V_{IN}$  range, the overcurrent protection remains active.

### 8.4.4 Overvoltage Lockout (OVLO)

When  $V_{IN}$  exceeds 7.6 V, the overvoltage lockout (OVLO) circuit turns off the protected power switch.

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The TPS25200 is a 5-V eFuse with precision current limit and over-voltage clamp. When a slave device such as a mobile data-card device is hot plugged into a USB port as shown in 图 9-1, an input transient voltage could damage the slave device due to the cable inductance. Placing the TPS25200 at the input of mobile device as over-voltage and overcurrent protector can safeguard these slave devices. Input transients also occur when the current through the cable parasitic inductance changes abruptly. This can occur when the TPS25200 turns off the internal MOSFET in response to an overvoltage or overcurrent event. The TPS25200 can withstand the transient without a bypass bulk capacitor, or other external overvoltage protection components at input side. The TPS25200 also can be used at host side as a traditional power switch pin-to-pin compatible with the TPS2553.

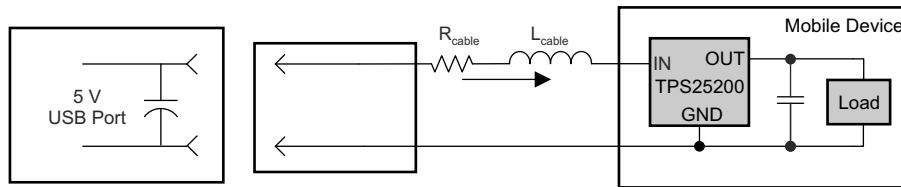


图 9-1. Hot Plug Into 5V USB port with Parasitic Cable Resistance and Inductance

### 9.2 Typical Application

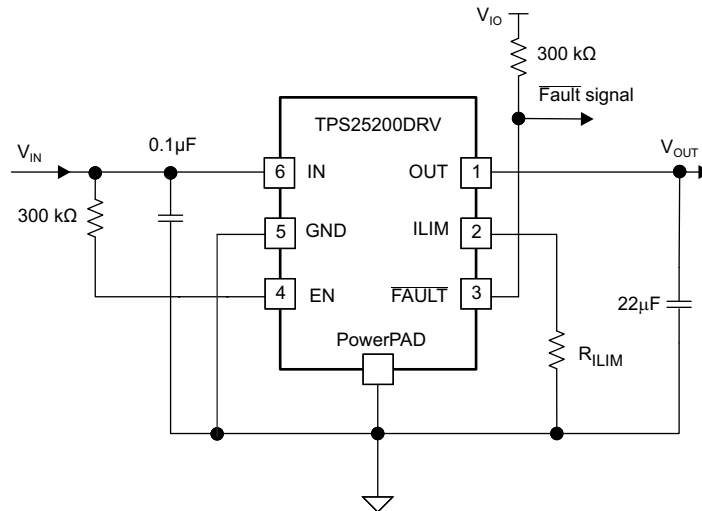


图 9-2. Overvoltage and Overcurrent Protector—Typical Application Schematic

Use the  $I_{OS}$  in the [Electrical Characteristics](#) table or  $I_{OS}$  in [方程式 1](#) to select the  $R_{ILIM}$ .

## 9.2.1 Design Requirements

For this design example, use the design parameters in 表 9-1 as the input parameters.

表 9-1. Design Parameters

| DESIGN PARAMETERS              | EXAMPLE VALUE |
|--------------------------------|---------------|
| Normal input operation voltage | 5 V           |
| Output transient voltage       | 6.5 V         |
| Minimum current limit          | 2.1 A         |
| Maximum currnt limit           | 2.9 A         |

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Step by Step Design Produce

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Output transient voltage
- Minimum Current Limit
- Maximum Current Limit

### 9.2.2.2 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, a 0.1- $\mu$ F or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

When  $V_{IN}$  ramp up exceed 7.6 V,  $V_{OUT}$  follows  $V_{IN}$  until the TPS25200 turns off the internal MOSFET after  $t_{(OVLO\_off\_delay)}$ . Since  $t_{(OVLO\_off\_delay)}$  largely depends on the  $V_{IN}$  ramp rate,  $V_{OUT}$  sees some peak voltage. Increasing the output capacitance can lower the output peak voltage as shown in 图 9-3.

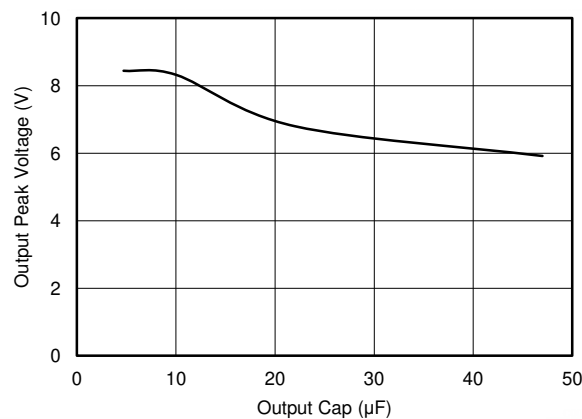


图 9-3.  $V_{OUT}$  Peak Voltage vs  $C_{OUT}$  ( $V_{IN}$  Step From 5 V to 15 V with 1-V/ $\mu$ s Ramp Up Rate)

### 9.2.2.3 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS25200 uses an internal regulation loop to provide a regulated voltage on the ILIM terminal. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for  $R_{ILIM}$  is  $33\text{ k}\Omega \leq R_{ILIM} \leq 1100\text{ k}\Omega$  to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for  $R_{ILIM}$ . The current-limit threshold equations (IOS) in 方程式 1 approximate the resulting overcurrent threshold for a given external resistor value  $R_{ILIM}$ . See the [Electrical Characteristics](#) table for specific current limit settings. The traces routing the  $R_{ILIM}$  resistor to the TPS25200 must be as short as possible to reduce parasitic effects on the current-limit accuracy.

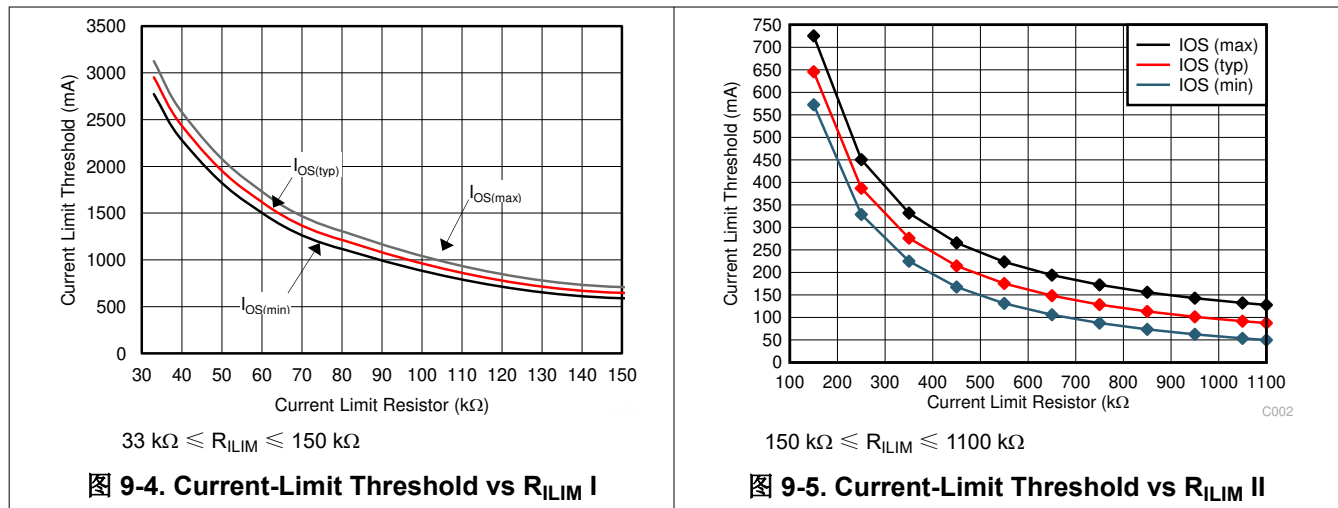
$R_{ILIM}$  can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of  $R_{ILIM}$  and the maximum desired load current on the  $I_{OS(min)}$  curve and choose a value of  $R_{ILIM}$  below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of  $R_{ILIM}$  and the  $I_{OS(max)}$  curve.

To design below a maximum current-limit threshold, find the intersection of  $R_{ILIM}$  and the maximum desired load current on the  $I_{OS(max)}$  curve and choose a value of  $R_{ILIM}$  above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of  $R_{ILIM}$  and the  $I_{OS(min)}$  curve. See [Figure 9-4](#) and [Figure 9-5](#).

$$\begin{aligned}
 I_{OSmax}(mA) &= \frac{96754V}{R_{ILIM} \cdot 0.985k\Omega} + 30 \\
 I_{OSnom}(mA) &= \frac{98322V}{R_{ILIM} \cdot 1.003k\Omega} \\
 I_{OSmin}(mA) &= \frac{97399}{R_{ILIM} \cdot 1.015k\Omega} - 30
 \end{aligned} \tag{1}$$

Where  $33\text{ k}\Omega \leq R_{ILIM} \leq 1100\text{ k}\Omega$ .



#### 9.2.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2.1 A must be delivered to the load so that the minimum desired current-limit threshold is 2100 mA. Use the  $I_{OS}$  equations ([方程式 1](#)) and [Figure 9-4](#) to select  $R_{ILIM}$  as shown in [方程式 2](#).

$$\begin{aligned}
 I_{OSmin}(mA) &= 2100\text{ mA} \\
 I_{OSmin}(mA) &= \frac{97399V}{R_{ILIM} \cdot 1.015k\Omega} - 30 \\
 R_{ILIM}(k\Omega) &= \left( \frac{97399}{I_{OS(min)} + 30} \right)^{1.015} = \left( \frac{97399}{2100 + 30} \right)^{1.015} = 43.22\text{ k}\Omega
 \end{aligned} \tag{2}$$



Select the closest 1% resistor less than the calculated value:  $R_{ILIM} = 42.2 \text{ k}\Omega$ . This sets the minimum current-limit threshold at 2130 mA as shown in [方程式 3](#).

$$I_{OSmin}(\text{mA}) = \frac{97399\text{V}}{R_{ILIM}^{1.015} \text{k}\Omega} - 30 = \frac{97399}{(42.2 \times 1.01)^{1.015}} - 30 = 2130\text{mA} \quad (3)$$

Use the  $I_{OS}$  equations ([方程式 1](#)), [Figure 9-4](#), and the previously calculated value for  $R_{ILIM}$  to calculate the maximum resulting current-limit threshold as shown in [方程式 4](#).

$$I_{OSmax}(\text{mA}) = \frac{96754}{R_{ILIM}^{0.985}} + 30$$

$$I_{OSmax}(\text{mA}) = \frac{96754}{(42.2 \times 0.99)^{0.985}} + 30 = 2479 \text{ mA} \quad (4)$$

The resulting current-limit threshold minimum is 2130 mA and maximum is 2479 mA with  $R_{ILIM} = 42.2\text{k}\Omega \pm 1\%$ .

### 9.2.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 2.9 A must be delivered to the load so that the minimum desired current-limit threshold is 2900 mA. Use the  $I_{OS}$  equations ([方程式 1](#)) and [Figure 9-5](#) to select  $R_{ILIM}$  as shown in [方程式 5](#).

$$I_{OSmax}(\text{mA}) = 2900\text{mA}$$

$$I_{OSmax}(\text{mA}) = \frac{96754}{R_{ILIM}^{0.985} \text{k}\Omega} + 30$$

$$R_{ILIM}(\text{k}\Omega) = \left( \frac{96754}{I_{OS(max)} - 30} \right)^{\frac{1}{0.985}} = \left( \frac{96754}{2900 - 30} \right)^{\frac{1}{0.985}} = 35.57 \text{ k}\Omega \quad (5)$$

Select the closest 1% resistor greater than the calculated value:  $R_{ILIM} = 36 \text{ k}\Omega$ . This sets the maximum current-limit threshold at 2894 mA as shown in [方程式 6](#).

$$I_{OSmax}(\text{mA}) = \frac{96754\text{V}}{R_{ILIM}^{0.985} \text{k}\Omega} + 30 = \frac{96754}{(36 \times 0.99)^{0.985}} + 30 = 2894\text{mA} \quad (6)$$

Use the  $I_{OS}$  equations, [Figure 9-5](#), and the previously calculated value for  $R_{ILIM}$  to calculate the minimum resulting current-limit threshold as shown in [方程式 7](#).

$$I_{OSmin}(\text{mA}) = \frac{97399}{R_{ILIM}^{1.015}} - 30$$

$$I_{OSmin}(\text{mA}) = \frac{97399}{(36 \times 1.01)^{1.015}} - 30 = 2508\text{mA} \quad (7)$$

The resulting minimum current-limit threshold minimum is 2508 mA and maximum is 2894 mA with  $R_{ILIM} = 36 \text{ k}\Omega \pm 1\%$ .

### 9.2.2.6 Power Dissipation and Junction Temperature

The low on-resistance of the internal N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from the typical characteristics graph. When  $V_{IN}$  is lower than  $V_{(OVC)}$ , the TPS2500 is a traditional power switch. Using this value, the power dissipation can be calculated by using [方程式 8](#).

$$P_D = r_{DS(on)} \times I_{OUT}^2 \quad (8)$$

When  $V_{IN}$  exceed  $V_{(OVC)}$ , but lower than  $V_{(OVL0)}$ , the TPS25200 clamp output to fixed  $V_{(OVC)}$ , the power dissipation can be calculated by using [方程式 9](#).

$$P_D = (V_{IN} - V_{(OVC)}) \times I_{OUT} \quad (9)$$

where

- $P_D$  = Total power dissipation (W)
- $r_{DS(on)}$  = Power switch on-resistance ( $\Omega$ )
- $V_{(OVC)}$  = Overvoltage clamp voltage (V)
- $I_{OUT}$  = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature using [方程式 10](#).

$$T_J = P_D \times \theta_{JA} + T_A \quad (10)$$

where

- $T_A$  = Ambient temperature ( $^{\circ}\text{C}$ )
- $\theta_{JA}$  = Thermal resistance ( $^{\circ}\text{C}/\text{W}$ )
- $P_D$  = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined"  $r_{DS(on)}$  from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance  $\theta_{JA}$ , and thermal resistance is highly dependent on the individual package and board layout.

### 9.2.3 Application Curves

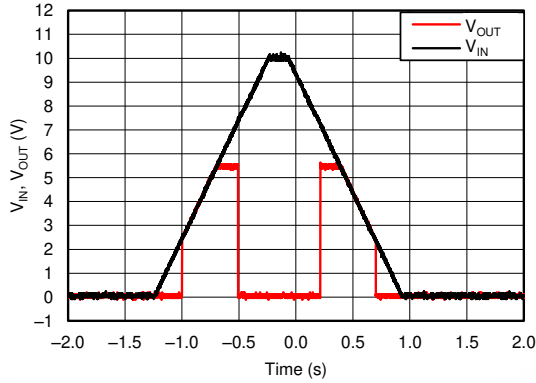


图 9-6.  $V_{OUT}$  vs  $V_{IN}$  (0 V to 10 V)

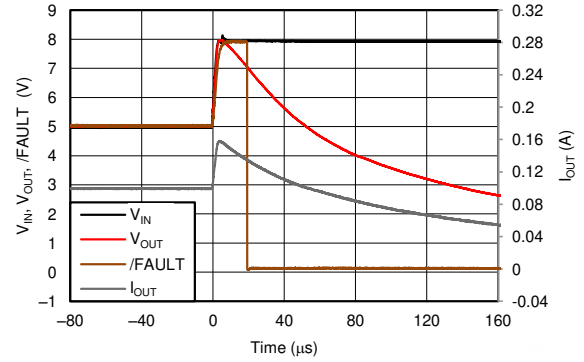


图 9-7.  $V_{IN}$  Step 5 V to 8 V with  $4.7 \mu F // 100 \Omega$

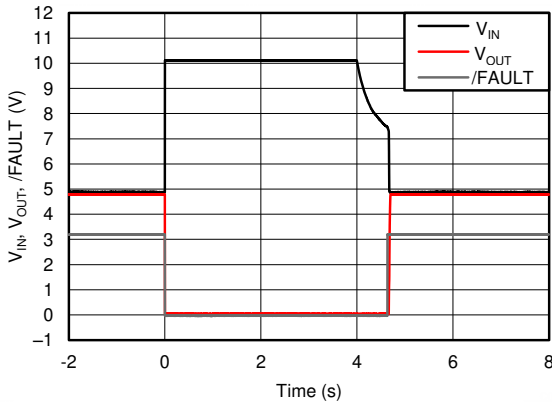


图 9-8. Pulse Overvoltage with  $100 \Omega$

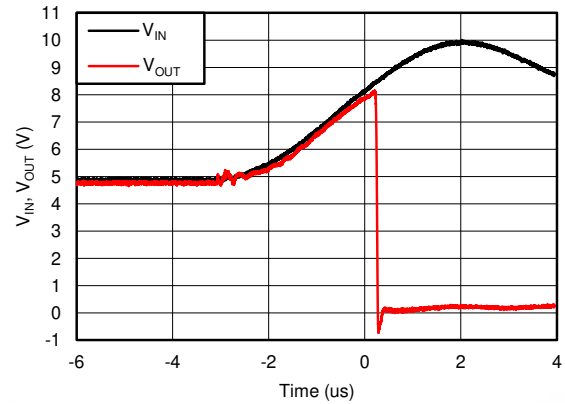


图 9-9. 5-V to 10-V OVLO Response Time

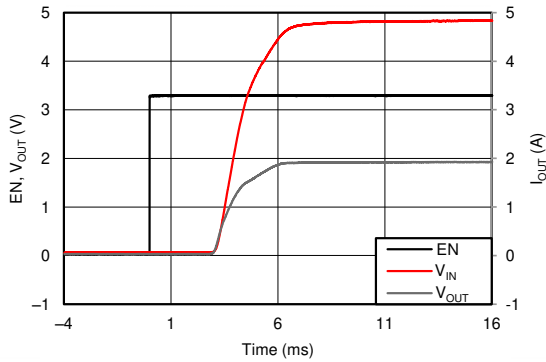


图 9-10. Turnon Delay and Rise Time  $150 \mu F // 2.5 \Omega$

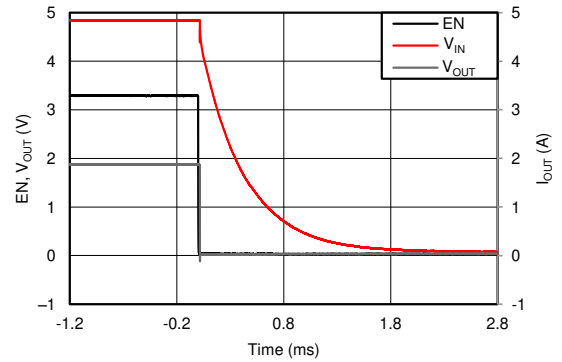


图 9-11. Turnoff Delay and Fall Time  $150 \mu F // 2.5 \Omega$

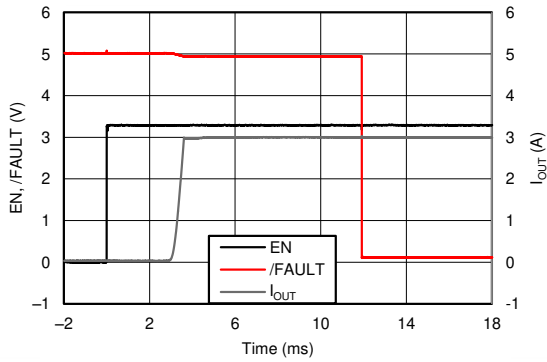


图 9-12. Enable into Output Short

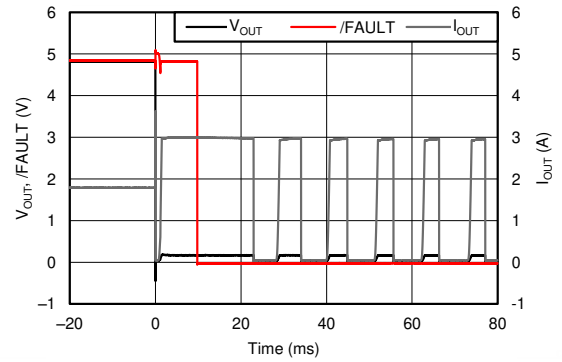


图 9-13. 2.5 Ω to Output Short Transient Response

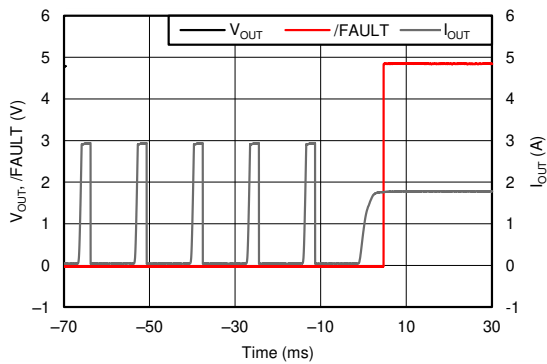


图 9-14. Output Short to 2.5-Ω Load Recovery Response

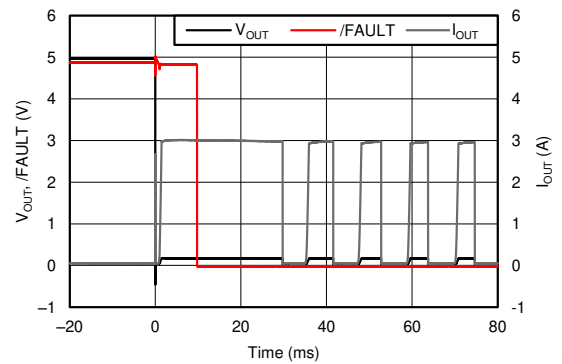


图 9-15. No Load to Output Short Transient Response

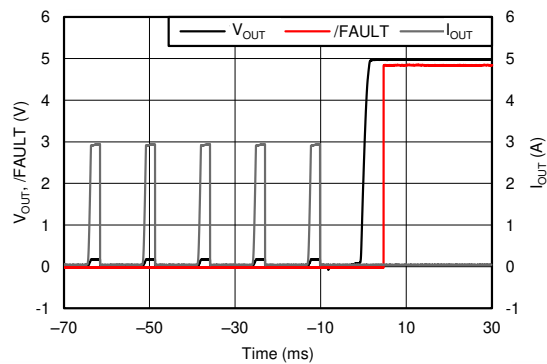


图 9-16. Output Short to No Load Recovery Response

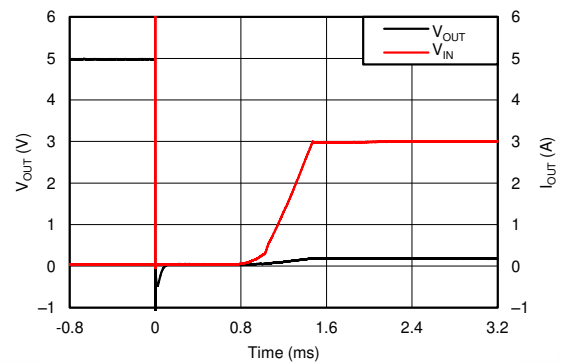


图 9-17. Hot-Short With 50 mΩ

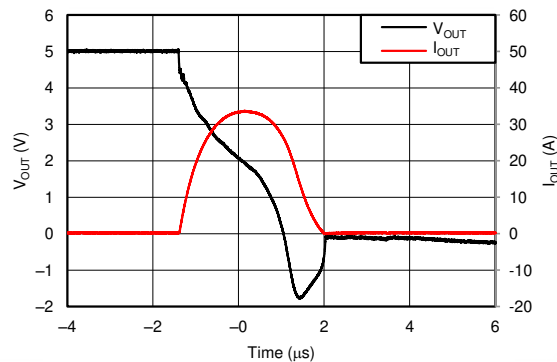


图 9-18. 50-mΩ Hot-Short Response Time

## 10 Power Supply Recommendations

The TPS25200 is designed for  $2.7\text{ V} < V_{IN} < 5\text{ V}$  (typical) voltage rails. While there is a  $V_{OUT}$  clamp, it is not intended to be used to regulate  $V_{OUT}$  at approximately 5.4 V with  $6\text{ V} < V_{IN} < 7\text{ V}$ . This is a protection feature only.

## 11 Layout

### 11.1 Layout Guidelines

- For all applications, a 0.1- $\mu\text{F}$  or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.
- For output capacitance, refer to [Figure 9-3](#), low ESR ceramic cap is recommended.
- The traces routing the  $R_{LIM}$  resistor to the device must be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

### 11.2 Layout Example

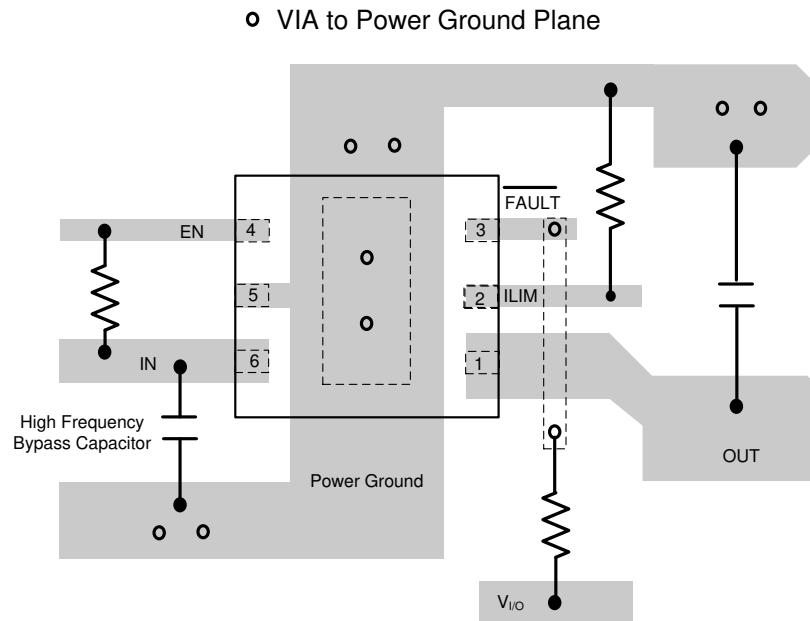


图 11-1. TPS25200 Board Layout

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

[TPS25200 EVM User's Guide](#)

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS25200DRVR     | ACTIVE        | WSON         | DRV             | 6    | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | SKB                     | <a href="#">Samples</a> |
| TPS25200DRV/T    | ACTIVE        | WSON         | DRV             | 6    | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | SKB                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS25200 :**

- Automotive : [TPS25200-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS25200DRVR | WSON         | DRV             | 6    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS25200DRVT | WSON         | DRV             | 6    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS25200DRVT | WSON         | DRV             | 6    | 250  | 178.0              | 8.4                | 2.25    | 2.25    | 1.0     | 4.0     | 8.0    | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS25200DRVR | WSON         | DRV             | 6    | 3000 | 210.0       | 185.0      | 35.0        |
| TPS25200DRVT | WSON         | DRV             | 6    | 250  | 210.0       | 185.0      | 35.0        |
| TPS25200DRVT | WSON         | DRV             | 6    | 250  | 205.0       | 200.0      | 33.0        |

## GENERIC PACKAGE VIEW

DRV 6

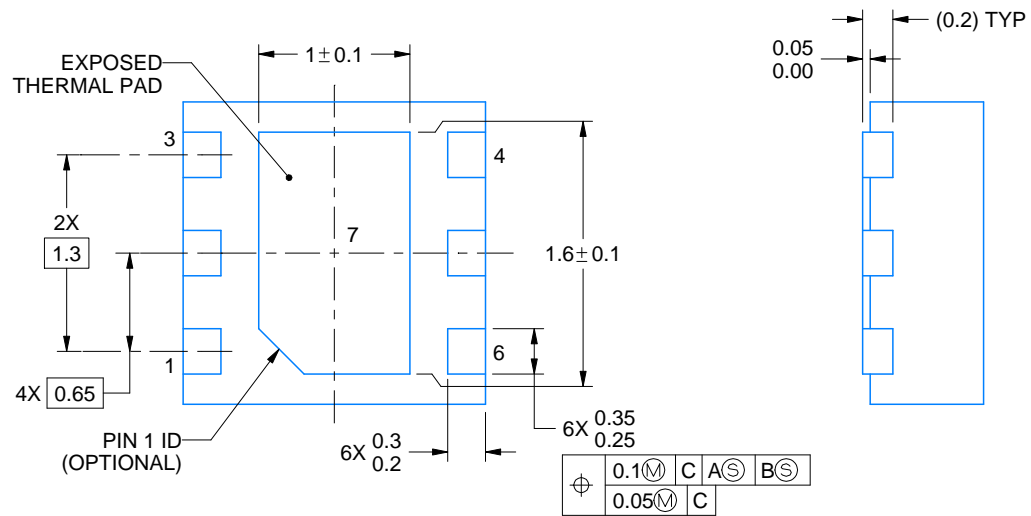
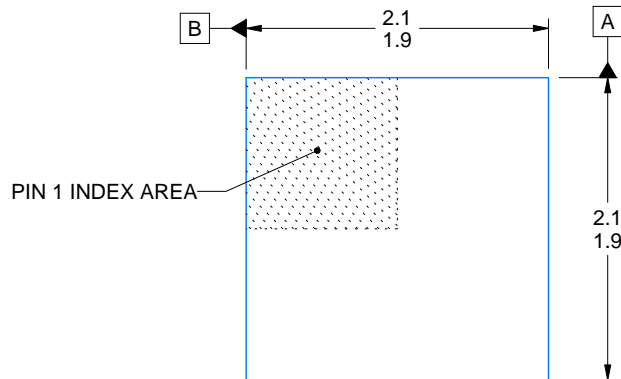
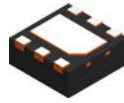
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

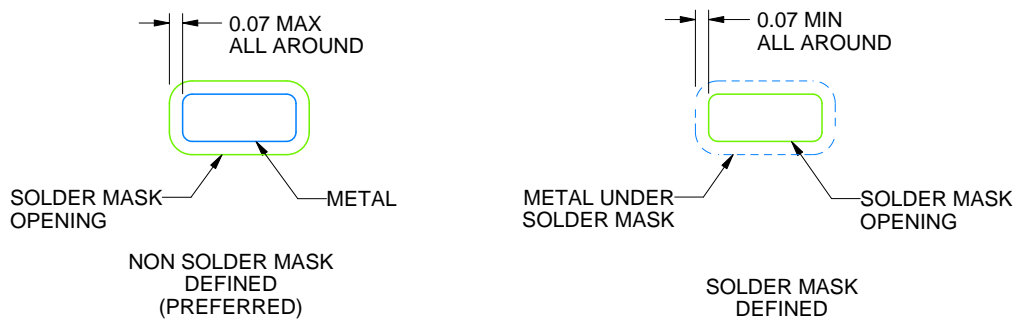
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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