# TPS2559-Q1 高精度可调式限流配电开关

## 1 特性

- 适用于汽车电子 应用 具有符合 AEC-Q100 标准的下列结果：
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C5
- 2.5V 至 6.5V 工作电压范围
- 1.2 至 4.7A 的可调节电流 $I_{(LIMIT)}$（4.7A 时的限流精度为 ±4.7%）
- 3.5µs 短路关断响应时间（典型值）
- 13mΩ 高侧金属氧化物半导体场效应晶体管 (MOSFET)
- 2µA 最大待机电源电流
- 内置软启动
- 禁用时提供反向电流阻断
- 8kV/15kV 系统级静电放电 (ESD) 能力
- 具有可湿性侧面的 10 引脚小外形尺寸无引线 (3mm × 3mm) 封装

## 2 应用

- 汽车类 USB 端口/集线器
- 汽车类内部负载开关

## 3 说明

TPS2559-Q1 配电开关专门用于 需要低电阻、高精度限流开关或使用高容性负载 的应用。TPS2559-Q1 最高可提供 5.5A 的持续负载电流，通过单个接地电阻即可实现精确限流。当输出负载超出限流阈值时，可通过切换至恒流模式使输出电流保持在一个安全的级别。过载事件期间，输出电流被限制在由 $R_{(ILIM)}$ 设定的级别。如果出现持续过载，TPS2559-Q1 将进入热关断模式，从而避免自身发生损坏。

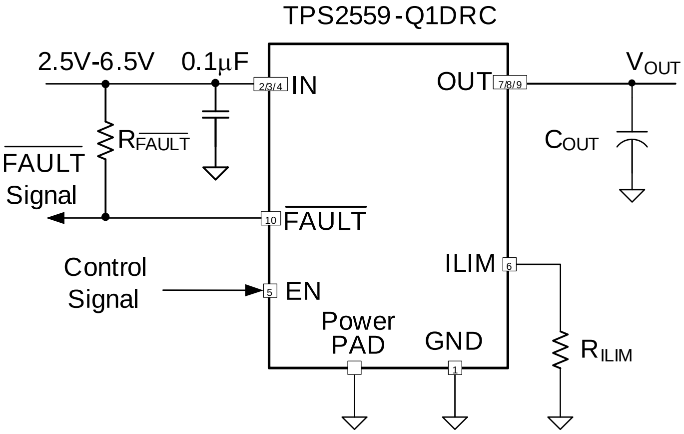
对电源开关的上升和下降次数进行控制以最大程度降低接通或关断期间的电流冲击。在过流或过热情况下，$\overline{\text{FAULT}}$ 逻辑输出被置为低电平。

器件信息[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS2559-Q1 | 超薄小外形尺寸无引线 (VSON) (10) | 3.00mm x 3.00mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

LP38690 的



# 目录

## 4 修订历史记录

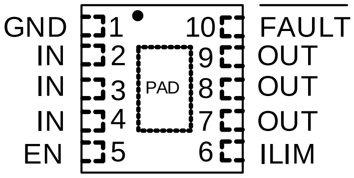
| 日期 | 修订版本 | 注释 |
|---|---|---|
| 2015 年 12 月 | * | 首次发布。 |

# 5 Device Comparison Table

| Device | Operation Range (V) | OCP Mode | ICONT. Adj. Range (A) | $R_{DS(on)}$ (mΩ) | $I_{OS}$ tolerance | Package |
|---|---|---|---|---|---|---|
| TPS2559-Q1 | 2.5 - 6.5 | Auto Retry | 5.5 | 13 | ±4.7% at 4.7 A | DRC (SON-10) |
| TPS2553-Q1 | 2.5 - 6.5 | Auto Retry | 1.2 | 85 (DBV) | ±6.8% at 1.3 A | DBV (SOT-23) |
| TPS2556/7-Q1 | 2.5 - 6.5 | Auto Retry | 5 | 22 | ±6.3% at 4.5 A | DRB (SON-8) |
| TPS2561A-Q1<br>(Dual Channels) | 2.5 - 6.5 | Auto Retry | 2.5 | 44 | 2.1 A to 2.5 A | DRC (SON-10) |
| TPS25200-Q1<br>(With OVP protection) | 2.5 - 6.5<br>(Withstand up to 20V) | Auto Retry | 2.5 | 60 | ±6.3% at 2.7 A | DRV (SON-6) |

# 6 Pin Configuration and Functions

**DRC Package**
**SON-10 (10 Pins)**
**Top View**



**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 1 | | Ground connection, connect externally to PowerPAD |
| IN | 2,3,4 | I | Input voltage, connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible |
| EN | 5 | I | Enable input, logic high turns on power switch. |
| ILIM | 6 | O | External resistor used to set current-limit threshold; recommended. 24.9 kΩ ≤ $R_{(ILIM)}$ ≤ 100 kΩ. |
| OUT | 7,8,9 | O | Power-switch output |
| $\overline{\text{FAULT}}$ | 10 | O | Active-low open-drain output, asserted during over-current or overtemperature conditions. |
| PowerPAD™ | PAD | | Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range | IN, OUT, EN, ILIM, $\overline{\text{FAULT}}$ | –0.3 | 7 | V |
| | IN to OUT | –7 | 7 | V |
| Continuous output current, $I_{OUT}$ | OUT | Internally Limited | | mA |
| Continuous $\overline{\text{FAULT}}$ sink current | | | 20 | mA |
| ILIM source current | | Internally Limited | | mA |
| Maximum junction temperature, $T_J$ | | –40 | to OTSD2 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge (1) | Human body model (HBM), ESD stress voltage, all pins (2) | | ±2000 | V |
| | | Charged device model (CDM), ESD stress voltage, all pins (3) | | ±750 | |
| | | System Level (4) | Contact discharge | ±8000 | |
| | | | Air discharge | ±15000 | |

(1) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by assembly-line electrostatic discharges into the device.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5.
(4) Surges per EN61000-4-2, 1999 applied between USB and output ground of the TPS2559EVM (SLUUB15) evaluation module (documentation available on the Web.) These were the test levels, not the failure threshold.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage, IN | 2.5 | 6.5 | V |
| $V_{EN}$ | Input voltage, EN | 0 | 6.5 | V |
| $I_{OUT}$ | Continuous output current of OUT | | 5.5 | A |
| | Continuous $\overline{\text{FAULT}}$ sink current | | 10 | mA |
| $R_{(ILIM)}$ | Recommended resistor limit range (1) | 24.9 | 100 | kΩ |
| $T_J$ | Operating junction temperature | -40 | 125 | °C |

(1) $R_{(ILIM)}$ is the resistor from ILIM pin to GND and ILIM pin can be shorted to GND.

## 7.4 Thermal Information

| THERMAL METRIC (1) | | TPS2559-Q1 | UNIT |
|---|---|---|---|
| | | DRC (10 PINS) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 40.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 45.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 15.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 15.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

Conditions are –40°C ≤ $T_J$ ≤ 125°C, 2.5 V ≤ $V_{IN}$ ≤ 6.5 V, $V_{(EN)} = V_{IN}$, $R_{(ILIM)}$ = 49.9 kΩ. Positive current are into pins. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | Input - Output Resistance[1] | $T_J$ = 25°C | | 13 | 16 | mΩ |
| | | -40°C ≤ $T_J$ ≤ 125°C | | | 21 | |
| **ENABLE INPUT EN** | | | | | | |
| | EN turn on/off threshold | | 0.66 | | 1.1 | V |
| | Hysteresis | | | 55[2] | | mV |
| $I_{(EN)}$ | Input current | $V_{(EN)}$ = 0 V or $V_{(EN)}$ = 6.5 V | –1 | | 1 | µA |
| **CURRENT LIMIT** | | | | | | |
| $I_{OS}$ | OUT short circuit current limit | $R_{(ILIM)}$ = 24.9 kΩ | 4490 | 4730 | 4931 | mA |
| | | $R_{(ILIM)}$ = 44.2kΩ | 2505 | 2660 | 2805 | |
| | | $R_{(ILIM)}$ = 49.9kΩ | 2215 | 2360 | 2490 | |
| | | $R_{(ILIM)}$ = 61.9 kΩ | 1780 | 1900 | 2015 | |
| | | $R_{(ILIM)}$ = 100 kΩ | 1080 | 1180 | 1265 | |
| | | ILIM pin short to GND ($R_{(ILIM)}$ = 0) | 5860 | 6700 | 7460 | |
| **SUPPLY CURRENT** | | | | | | |
| $I_{(IN\_OFF)}$ | Disabled, IN supply current | $V_{(EN)}$ = 0 V, No load on OUT | | 0.1 | 2 | µA |
| $I_{(IN\_ON)}$ | Enabled, IN supply current | $R_{(ILIM)}$ = 100 kΩ, no load on OUT | | 97 | 125 | µA |
| | | $R_{(ILIM)}$ = 24.9 kΩ, no load on OUT | | 107 | 135 | |
| $I_{(REV)}$ | Reverse leakage current | $V_{OUT}$ = 6.5 V, $V_{IN}$ = 0 V, $T_J$ = 25°C, Measure $I_{OUT}$ | | 0.01 | 1 | µA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | |
| $V_{UVLO}$ | IN rising UVLO threshold voltage | | | 2.36 | 2.45 | V |
| | Hysteresis | | | 35[2] | | mV |
| **$\overline{\text{FAULT}}$** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{\overline{FAULT}}$ = 1 mA | | | 180 | mV |
| | Off-state leakage | $V_{\overline{FAULT}}$ = 6.5 V | | | 1 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| OTSD2 | Thermal shutdown threshold | | 155 | | | °C |
| OTSD1 | Thermal shutdown threshold in current-limit | | 135 | | | |
| | Hysteresis | | | 20[2] | | |

---

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately

(2) These parameters are provided for reference only, and don't constitute part of TI's published device specifications for purposes of TI's product warranty.

## 7.6 Timing Requirements

Conditions are –40°C ≤ $T_J$ = ≤ 125°C, 2.5 V ≤ $V_{IN}$ ≤ 6.5 V, $V_{(EN)}$ = $V_{IN}$, $R_{(ILIM)}$ = 49.9 kΩ. Positive current are into pins. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | |
| $t_r$ | OUT voltage rise time | $V_{IN}$ = 6.5 V | $C_L$ = 1 µF, $R_L$ = 100 Ω, See Figure 13 | 2.6 | 3.44 | 5.2 | ms |
| | | $V_{IN}$ = 2.5 V | | 1.3 | 2.01 | 3.9 | |
| $t_f$ | OUT voltage fall time | $V_{IN}$ = 6.5 V | | 0.7 | 0.89 | 1.3 | |
| | | $V_{IN}$ = 2.5 V | | 0.42 | 0.58 | 1.04 | |
| **ENABLE INPUT EN** | | | | | | | |
| $t_{on}$ | OUT voltage turn-on time | $C_L$ = 1 µF, $R_L$ = 100 Ω, See Figure 14 | | | | 15 | ms |
| $t_{off}$ | OUT voltage turn-off time | | | | | 8 | |
| **CURRENT LIMIT** | | | | | | | |
| $t_{IOS}$ | Short-circuit response time(1) | $V_{IN}$ = 5 V, $R_{SHORT}$ = 50 mΩ, See Figure 15 | | | 3.5(1) | | µs |
| **$\overline{\text{FAULT}}$** | | | | | | | |
| | $\overline{\text{FAULT}}$ deglitch | $\overline{\text{FAULT}}$ assertion or de-assertion due to overcurrent condition | | 6 | 9 | 13 | ms |

(1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty

## 7.7 Typical Characteristics

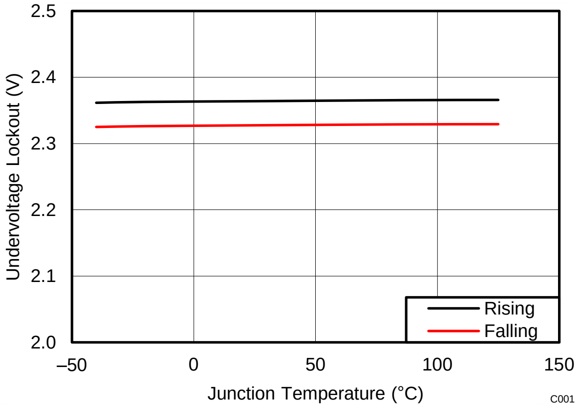
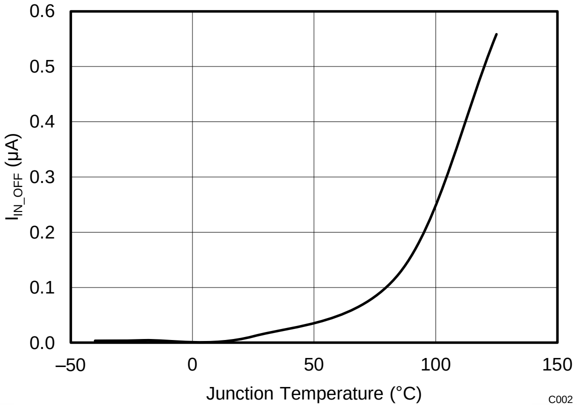
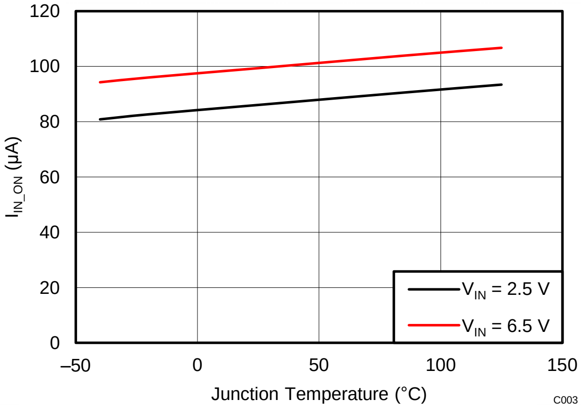


**Figure 1. Under-voltage Lockout (UVLO) vs Temperature**



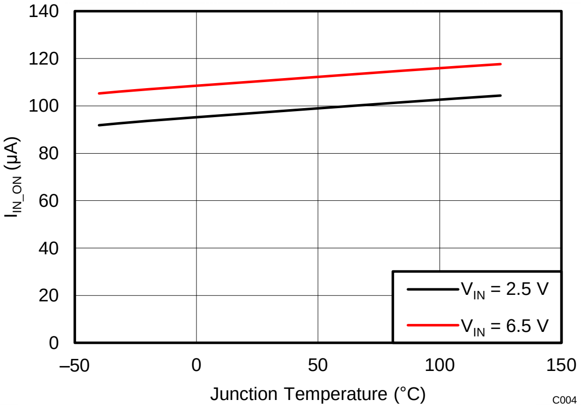
$V_{IN}$ = 6.5 V

**Figure 2. Supply Current, Output Disabled ($I_{IN\_OFF}$) vs Temperature**



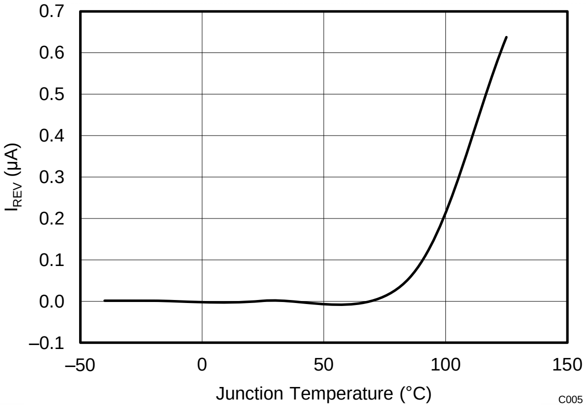
$R_{(ILIM)}$ = 100 KΩ

**Figure 3. Supply Current, Output Enabled ($I_{IN\_ON}$) vs Temperature**



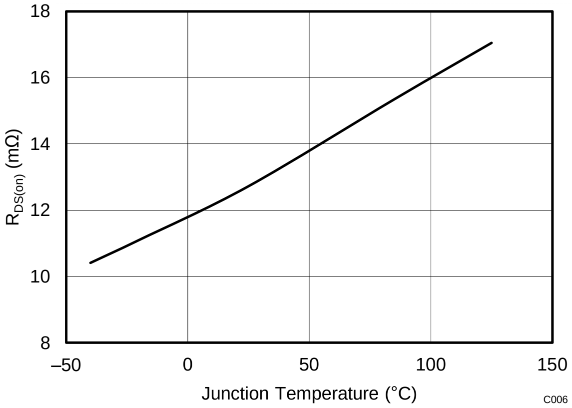
$R_{(ILIM)}$ = 24.9 KΩ

**Figure 4. Supply Current, Output Enabled ($I_{IN\_ON}$) vs Temperature**



$V_{OUT}$ = 6.5 V

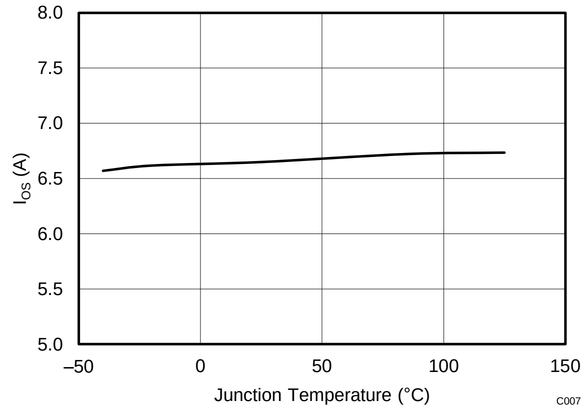
**Figure 5. Reverse Leakage Current ($I_{REV}$) v. Temperature**



$V_{IN}$ = 5 V

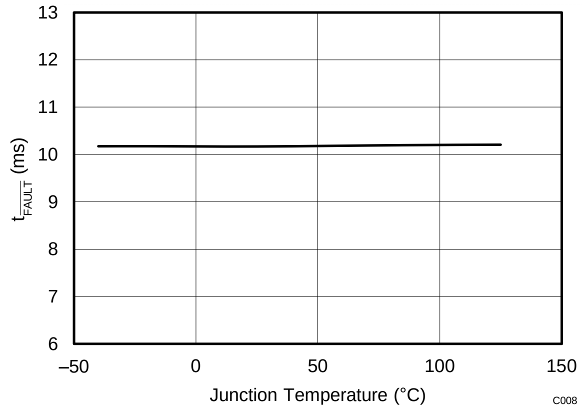
**Figure 6. Input-Output Resistance ($R_{DS(on)}$) vs Temperature**

## Typical Characteristics (continued)



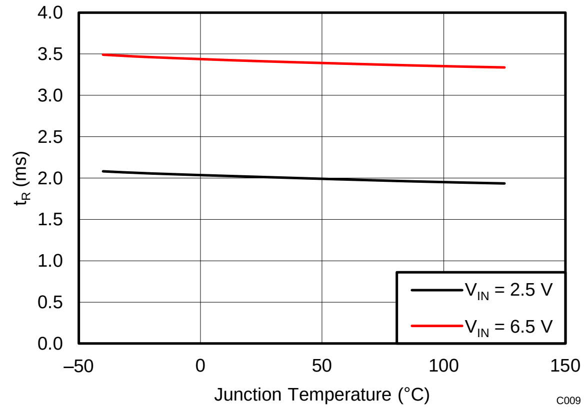
$V_{IN}$ = 6.5 V ILIM pin short to GND

**Figure 7. Short Circuit Current ($I_{OS}$) vs Temperature**



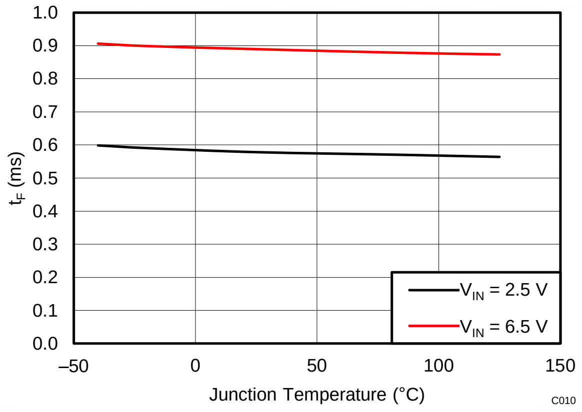
$V_{(\overline{FAULT})}$ = 2.5 V

**Figure 8. Deglitch Time ($t_{\overline{FAULT}}$) vs Temperature**



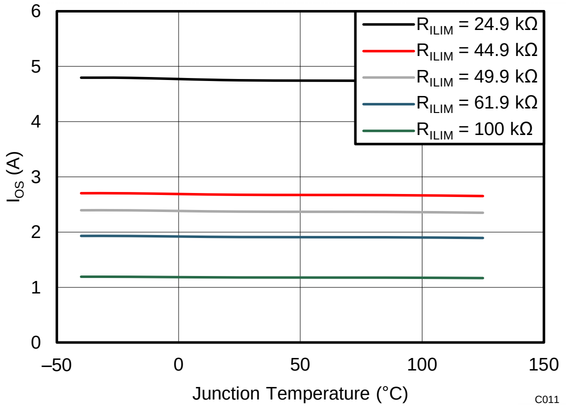
$C_{OUT}$ = 1 µF $R_{(LOAD)}$ = 100 Ω

**Figure 9. Output Rise Time ($t_R$) vs Temperature**



$C_{OUT}$ = 1 µF $R_{(LOAD)}$ = 100 Ω

**Figure 10. Output Fall Time ($t_F$) vs Temperature**



$V_{IN}$ = 6.5 V

**Figure 11. Short Circuit Current ($I_{OS}$) vs Temperature**

# 8 Parameter Measurement Information

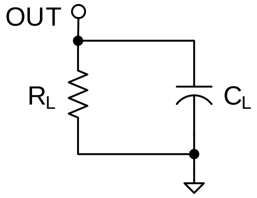


Figure 12. Output Rise/Fall time Test Load

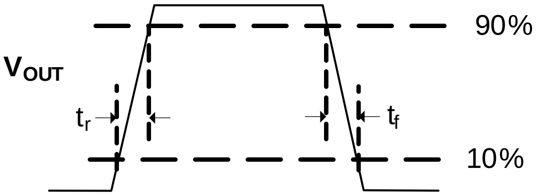


Figure 13. Power-On and Off Timing

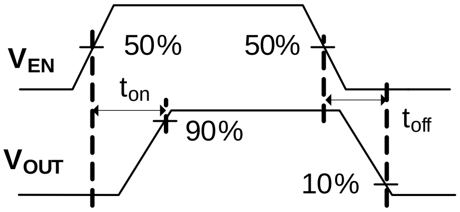


Figure 14. Enable Timing, Active High Enable

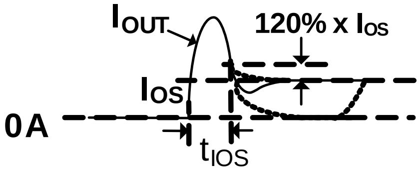


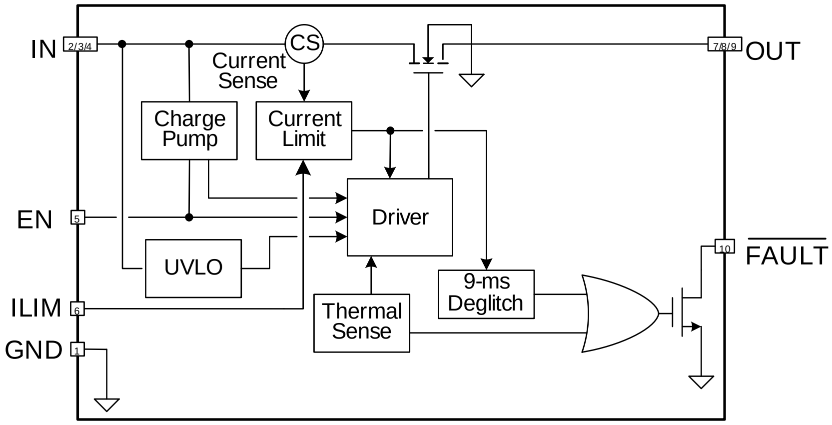
Figure 15. Output Short Circuit Parameters

# 9 Detailed Description

## 9.1 Overview

The TPS2559-Q1 is a current-limited, power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered. This device allows the user to program the current-limit via an external resistor and the maximum continuous output current up to 5.5 A. This device incorporates an internal charge pump and the gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. The TPS2559-Q1 limits the output current to the programmed current-limit threshold $I_{OS}$ during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to $I_{OS}$ reduces the output voltage at OUT because N-channel MOSFET is no longer fully enhanced.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Thermal Sense

The TPS2559-Q1 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS2559-Q1 device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an over-current condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS2559-Q1 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 20°C. The TPS2559-Q1 continues to cycle off and on until the fault is removed.

## Feature Description (continued)

### 9.3.2 Overcurrent Protection

The TPS2559-Q1 responds to overcurrent conditions by limiting their output current to IOS. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by ($I_{OS}$ × $R_{LOAD}$). Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2559-Q1 ramps the output current to $I_{OS}$. The TPS2559-Q1 limits the current to $I_{OS}$ until the overload condition is removed or the device begins to thermal cycle (see Figure 24).

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time $t_{IOS}$ (see Figure 15). The response speed and shape will vary with the overload level, input circuit, and rate of application. The current-limit response will vary between simply settling to $I_{OS}$, or turnoff and controlled return to IOS. Similar to the previous case, the TPS2559-Q1 limits the current to $I_{OS}$ until the overload condition is removed or the device begins to thermal cycle.

The TPS2559-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS2559-Q1 cycles on/off until the overload is removed (see Figure 25).

### 9.3.3 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an over-current or over-temperature condition. The TPS2559-Q1 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS2559-Q1 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for over-current (9-ms typ.) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions. The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an over-temperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an over-temperature event.

## 9.4 Device Functional Modes

### 9.4.1 Operation with $V_{IN}$ Undervoltage Lockout (UVLO) Control

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

### 9.4.2 Operation with EN Control

The logic enable controls the power switch and device supply current. The supply current is reduced to less than 2-μA when a logic low is present on EN. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The TPS2559-Q1 current limited power switch uses N-channel MOSFETs in applications requiring up to 5.5 A of continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

The TPS2559-Q1 power switch is used to protect the up-stream power supply when the output is overloaded.

## 10.2 Typical Application

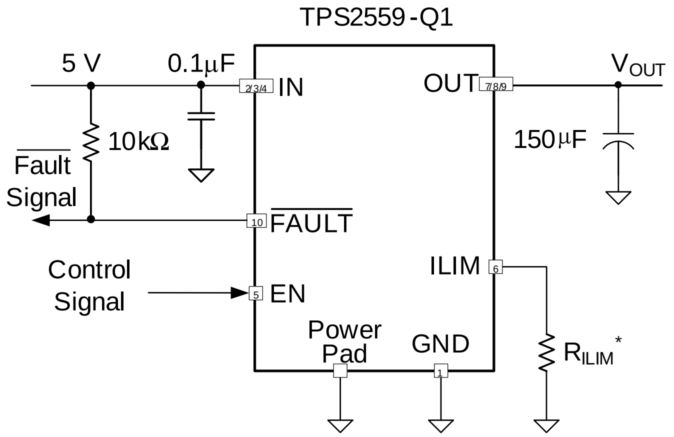


Figure 16. Typical TPS2559-Q1 Power Switch

Use the $I_{OS}$ in the *Electrical Characteristics* table or $I_{OS}$ in Equation 1 to select the $R_{ILIM}$.

### 10.2.1 Design Requirements

For this design example, use the following as the input parameters.

| DESIGN PARAMETERS | EXAMPLE VALUE |
|---|---|
| Input Operation Voltage | 5 V |
| Rating Current | 3A or 4.5A |
| Minimum Current Limit | 3A |
| Maximum Current Limit | 5A |

When choose power switch, there are some several general steps:

1. What is the power rail, 3.3 V or 5 V, and then choose the operation range of power switch can cover the power rail.
2. What is the normal operation current, for example, the maximum allowable current drawn by portable equipment for USB 2.0 port is 500mA, so the normal operation current is 500mA and the minimum current limit of power switch must exceed 500 mA to avoid false trigger during normal operation.
3. What is the maximum allowable current provided by up-stream power, and then decide the maximum current limit of power switch that must lower it to ensure power switch can protect the up-stream power when overload is encountered at the output of power switch.

---

**NOTE**

Choosing power switch with tighter current limit tolerance can loosen the up-stream power supply design.

---

## 10.2.2 Detailed Design Procedure

### *10.2.2.1 Step by Step Design Procedure*

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Rating Current
- Minimum Current Limit
- Maximum Current Limit

### *10.2.2.2 Input and Output Capacitance*

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage undershoot from exceeding the UVLO of other load share one power rail with TPS2559-Q1 or overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output to reduce the undershoot, which caused by the inductance of the output power bus just after a short has occurred and the TPS2559-Q1 has abruptly reduced OUT current. Energy stored in the inductance will drive the OUT voltage down and potentially negative as it discharges.

### *10.2.2.3 Programming the Current-Limit Threshold*

The overcurrent threshold is user programmable via an external resistor. The TPS2559-Q1 uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for $R_{(ILIM)}$ is 24.9 kΩ ≤ $R_{(ILIM)}$ ≤ 100 kΩ to ensure stability of the internal regulation loop.

When ILIM pin short to GND (single point failure), maximum current limit is less than 8 A over temperature and process variation.

Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for $R_{(ILIM)}$. The equations and the graph below can be used to estimate the minimum and maximum variation of the current-limit threshold for a predefined resistor value within $R_{(ILIM)}$ is 24.9 kΩ ≤ $R_{(ILIM)}$ ≤ 100 kΩ. This variation is an approximation only and does not take into account, for example, the resistor tolerance. For examples of more-precise variation of $I_{OS}$ refer to the current-limit section of the *Electrical Characteristics* table.

$$\begin{aligned} I_{OS\,max}(mA) &= \frac{118848\ V}{R_{(ILIM)}{}^{0.9918} k\Omega} + 30 \\ I_{OSnom}(mA) &= \frac{118079\ V}{R_{(ILIM)}{}^{1.0008} k\Omega} \\ I_{OS\,min}(mA) &= \frac{113325\ V}{R_{(ILIM)}{}^{1.0010} k\Omega} - 47 \end{aligned} \quad (1)$$

24.9 kΩ ≤ $R_{(ILIM)}$ ≤ 100 kΩ

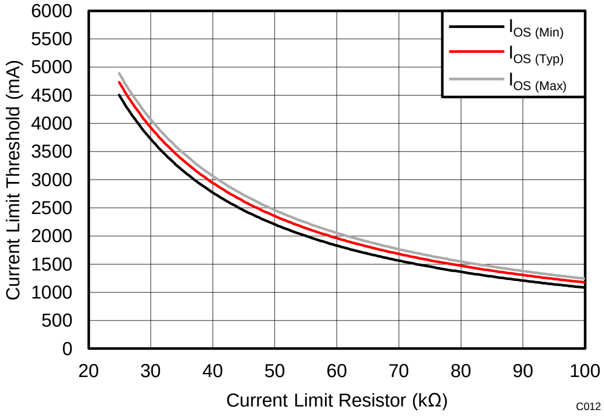


Figure 17. Current-Limit vs $R_{(ILIM)}$

### 10.2.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 3 A must be delivered to the load so that the minimum desired current-limit threshold is 3000 mA. Use the $I_{OS}$ equations and Figure 17 to select $R_{(ILIM)}$.

$$I_{OS\,min}(mA) = 3000\ mA$$

$$I_{OS\,min}(mA) = \frac{113325\ V}{R_{(ILIM)}{}^{1.0010}k\Omega} - 47$$

$$R_{(ILIM)}(k\Omega) = \left(\frac{113325}{I_{OS(min)} + 47}\right)^{\frac{1}{1.0010}} = \left(\frac{113325}{3000 + 47}\right)^{\frac{1}{1.0010}} = 37.06\ k\Omega \tag{2}$$

Select the closest 1% resistor less than the calculated value: $R_{(ILIM)}$ = 36.5 kΩ. This sets the minimum current-limit threshold at 3016 A.

$$I_{OS\,min}(mA) = \frac{113325\ V}{R_{(ILIM)}{}^{1.0010}k\Omega} - 47 = \frac{113325}{(36.5 \times 1.01)^{1.0010}} - 47 = 3016\ mA \tag{3}$$

Use the $I_{OS}$ equations, Figure 17, and the previously calculated value for $R_{(ILIM)}$ to calculate the maximum resulting current-limit threshold.

$$I_{OS\,max}(mA) = \frac{118848}{R_{(ILIM)}{}^{0.9918}} + 30 = \frac{118848}{(36.5 \times 0.99)^{0.9918}} + 30 = 3417\ mA \tag{4}$$

The resulting maximum current-limit threshold minimum is 3016 mA and maximum is 3417 mA with a 36.5 kΩ ± 1%.

### 10.2.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 5A must be delivered to the load so that the minimum desired current-limit threshold is 5000 mA. Use the $I_{OS}$ equations and Figure 17 to select $R_{(ILIM)}$.

$$I_{OS\,max}(mA) = 5000\ mA$$

$$I_{OS\,max}(mA) = \frac{118848}{R_{(ILIM)}{}^{0.9918}k\Omega} + 30$$

$$R_{(ILIM)}(k\Omega) = \left(\frac{118848}{I_{OS(max)} - 30}\right)^{\frac{1}{0.9918}} = \left(\frac{118848}{5000 - 30}\right)^{\frac{1}{0.9918}} = 24.55\ k\Omega \tag{5}$$

Select the closest 1% resistor less than the calculated value: $R_{ILIM}$ = 24.9 kΩ. This sets the maximum current-limit threshold at 4950 A.

$$I_{OS\,max}(mA) = \frac{118848}{R_{(ILIM)}^{0.9918} k\Omega} + 30 = \frac{118848}{(24.9 \times 0.99)^{0.9918}} + 30 = 4980\ mA \tag{6}$$

Use the $I_{OS}$ equations, Figure 17, and the previously calculated value for $R_{(ILIM)}$ to calculate the minimum resulting current-limit threshold.

$$I_{OS\,min}(mA) = \frac{113325}{R_{(ILIM)}^{1.0010}} - 47 = \frac{113325}{(24.9 \times 1.01)^{1.0010}} - 47 = 4445\ mA \tag{7}$$

The resulting minimum current-limit threshold minimum is 4445 mA and maximum is 4980 mA with a 24.9 kΩ ± 1%.

#### *10.2.2.6 Accounting for Resistor Tolerance*

The previous sections described the selection of $R_{(ILIM)}$ given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2559-Q1 is bounded by an upper and lower tolerance centered on a nominal resistance. The additional $R_{ILIM}$ resistance tolerance directly affects the current-limit threshold accuracy at a system level. Table 1 shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values.

Step one follows the selection process outlined in the application examples above.

Step two determines the upper and lower resistance bounds of the selected resistor.

Step three uses the upper and lower resistor bounds in the IOS equations to calculate the threshold limits.

It is important to use tighter tolerance resistors, that is, 0.5% or 0.1%, when precision current limiting is desired.

**Table 1. Common $R_{(ILIM)}$ Resistor Selections**

| DESIRED NOMINAL CURRENT LIMIT (mA) | IDEAL RESISTOR (kΩ) | CLOSEST 1% RESISTOR (kΩ) | RESISTOR TOLERANCE | | ACTUAL LIMITS | | |
|---|---|---|---|---|---|---|---|
| | | | 1% LOW (kΩ) | 1% HIGH (kΩ) | $I_{OS}$ MIN (mA) | $I_{OS}$ NOM (mA) | $I_{OS}$ MAX (mA) |
| 1250 | 94.1 | 93.1 | 92.2 | 94 | 1152.7 | 1263.7 | 1368.2 |
| 1500 | 78.4 | 78.7 | 77.9 | 79.5 | 1372.5 | 1495.1 | 1610.9 |
| 1750 | 67.2 | 66.5 | 65.8 | 67.2 | 1633.2 | 1769.7 | 1893.3 |
| 2000 | 58.8 | 59 | 58.4 | 59.6 | 1847 | 1994.8 | 2133.7 |
| 2250 | 52.3 | 52.3 | 51.8 | 52.8 | 2089.9 | 2550.6 | 2400.9 |
| 2500 | 47.1 | 47.5 | 47 | 48 | 2306 | 2478.2 | 2638.4 |
| 2750 | 42.8 | 43.2 | 42.8 | 43.6 | 2540.5 | 2725.1 | 2895.8 |
| 3000 | 39.2 | 39.2 | 38.8 | 39.6 | 2804.8 | 3003.4 | 3185.7 |
| 3250 | 36.2 | 36.5 | 36.1 | 36.9 | 3016 | 3225.7 | 3417.2 |
| 3500 | 33.6 | 34 | 33.7 | 34.3 | 3241.4 | 3463.1 | 3664.1 |
| 3750 | 31.4 | 31.6 | 31.3 | 31.9 | 3491.5 | 3726.4 | 3937.8 |
| 4000 | 29.4 | 29.4 | 29.1 | 29.7 | 3756.5 | 4005.4 | 4227.7 |
| 4250 | 27.7 | 28 | 27.7 | 28.3 | 3946.9 | 4205.9 | 4435.8 |
| 4500 | 26.2 | 26.1 | 25.8 | 26.4 | 4237.9 | 4512.3 | 4753.9 |
| 4750 | 24.8 | 24.9 | 24.7 | 25.1 | 4444.6 | 4729.9 | 4979.6 |

### 10.2.2.7 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated using Equation 8:

$$P_D = r_{DS(on)} \times I_{OUT}^2 \tag{8}$$

Where:

$P_D$ = Total power dissipation (W)
$r_{DS(on)}$ = Power switch on-resistance (Ω)
$I_{OUT}$ = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A \tag{9}$$

Where:

$T_A$ = Ambient temperature (°C)
$\theta_{JA}$ = Thermal resistance (°C/W)
$P_D$ = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $\theta_{JA}$ and thermal resistance is highly dependent on the individual package and board layout.

### 10.2.2.8 Auto-Retry

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{\text{FAULT}}$ pulls low EN. The part is disabled when EN is pulled below the turn-off threshold, and $\overline{\text{FAULT}}$ goes high impedance allowing $C_{(RETRY)}$ to begin charging. The part re-enables when the voltage on EN reaches the turn-on threshold. The part will continue to cycle in this manner until the fault condition is removed. The auto-retry cycling time is determined by the resistor/capacitor time constant, TPS2559-Q1 turn on time and $\overline{\text{FAULT}}$ deglitch time (see Figure 28).

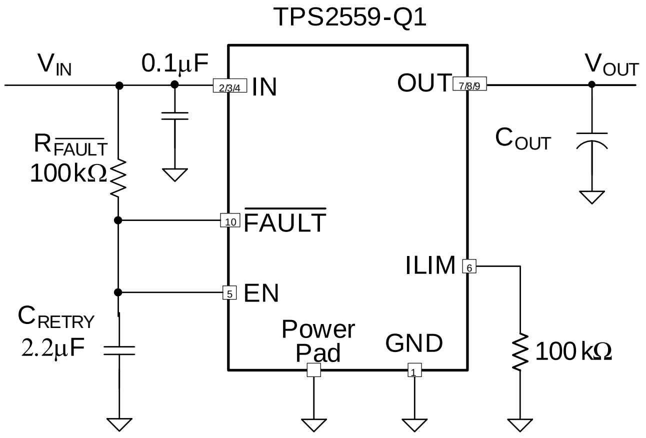


Figure 18. Auto-Retry Circuit

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. Figure 19 shows how an external logic signal can drive EN through $R_{(\overline{FAULT})}$ and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

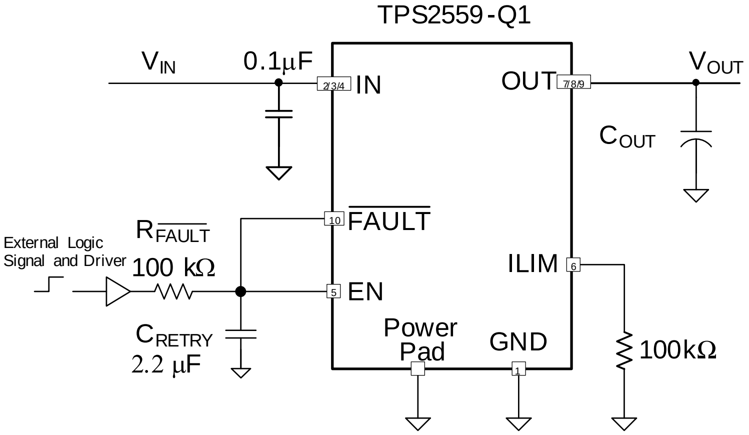


**Figure 19. Auto-Retry Circuit with External EN Signal**

If need to implement latch-off, refer to application report (SLVA282A).

### 10.2.2.9 Two-level Current-limit

Some applications require different current-limit thresholds depending on external system conditions. Figure 20 shows an implementation for an externally-controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see previously discussed *Programming the Current-Limit Threshold* section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND (see Figure 29 and Figure 30). Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

---

**NOTE**

ILIM should never be driven directly with an external signal.

---

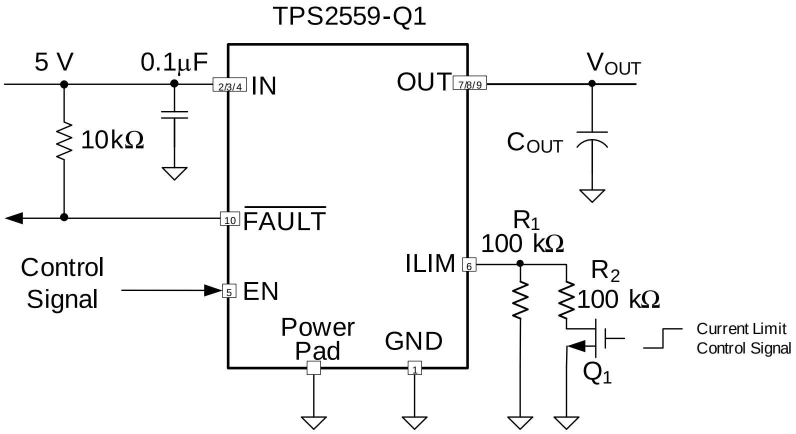


**Figure 20. Two-Level Current-Limit Circuit**

### 10.2.3 Application Curves

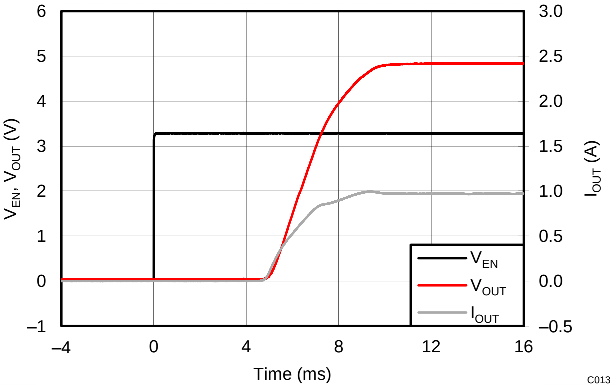


Figure 21. Output Rise with 150µF // 5Ω

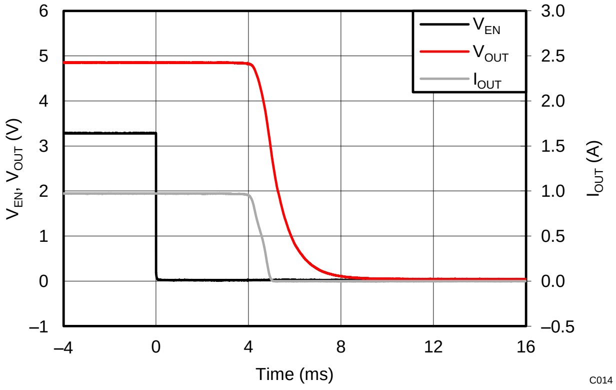


Figure 22. Output Fall with 150µF // 5Ω

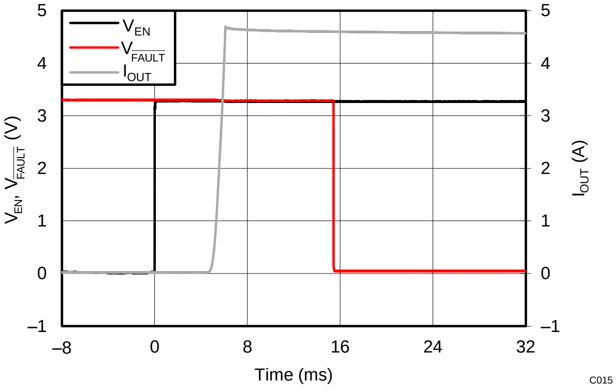


Figure 23. Enable into Output Short

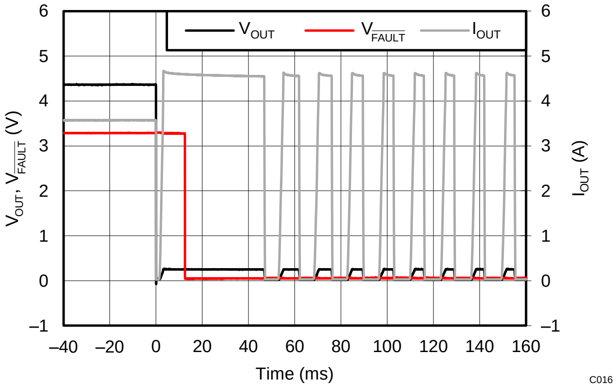


Figure 24. Full Load to Output Short Transient Response

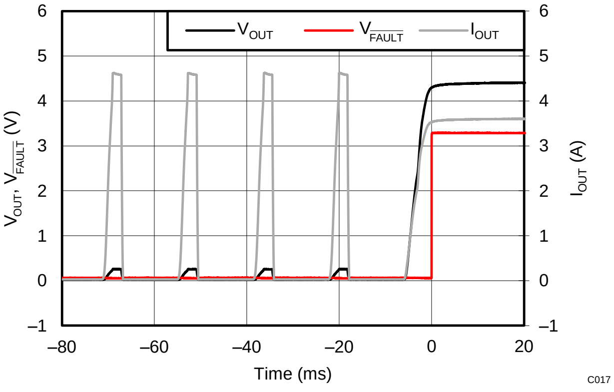


Figure 25. Output Short to Full Load Recovery Response

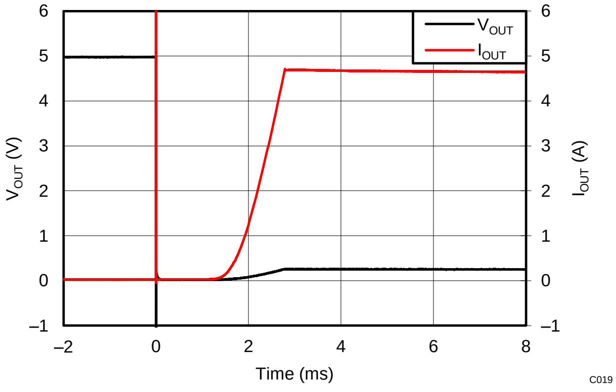


Figure 26. 50mΩ Hot-Short

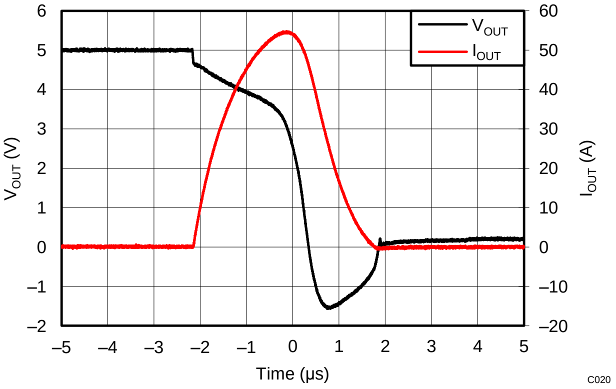


Figure 27. 50mΩ Hot-Short Response Time

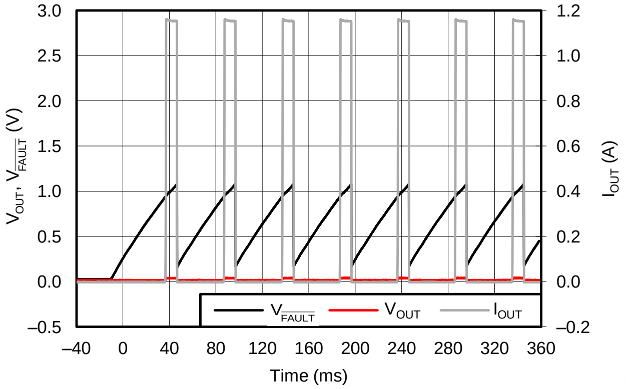


Figure 28. Auto-Retry Cycle

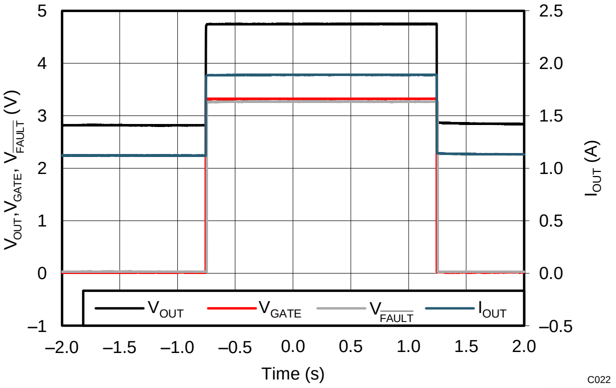


Figure 29. Two Level Current Limit with $R_{LOAD}$ = 2.5 Ω

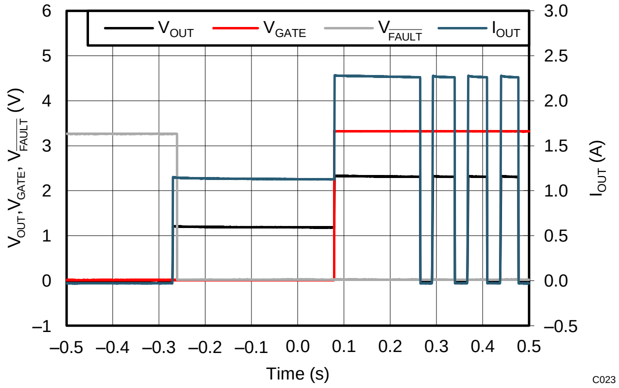


Figure 30. Two Level Current Limit with $R_{LOAD}$ = 1Ω

## 11 Power Supply Recommendations

Design of the devices is for operation from an input voltage supply range of 2.5 V to 6.5 V. The current capability of the power supply should exceed the maximum current limit of the power switch.

# 12 Layout

## 12.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- Placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output.
- The traces routing the $R_{ILIM}$ resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD should be directly connected to PCB ground plane using wide and short copper trace.

## 12.2 Layout Example

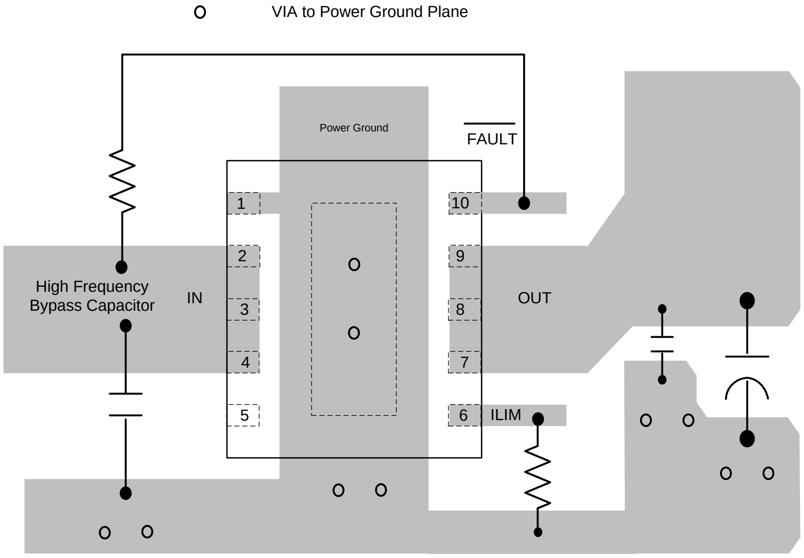


Figure 31. TPS2559-Q1 Board Layout

# 13 器件和文档支持

## 13.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.2 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS2559QWDRCRQ1 | Active | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 2559Q |
| TPS2559QWDRCRQ1.A | Active | Production | VSON (DRC) \| 10 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 2559Q |
| TPS2559QWDRCTQ1 | Active | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 2559Q |
| TPS2559QWDRCTQ1.A | Active | Production | VSON (DRC) \| 10 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 2559Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS2559-Q1 :**

- Catalog : TPS2559

NOTE: Qualified Version Definitions:

  - Catalog - TI's standard catalog product

# GENERIC PACKAGE VIEW

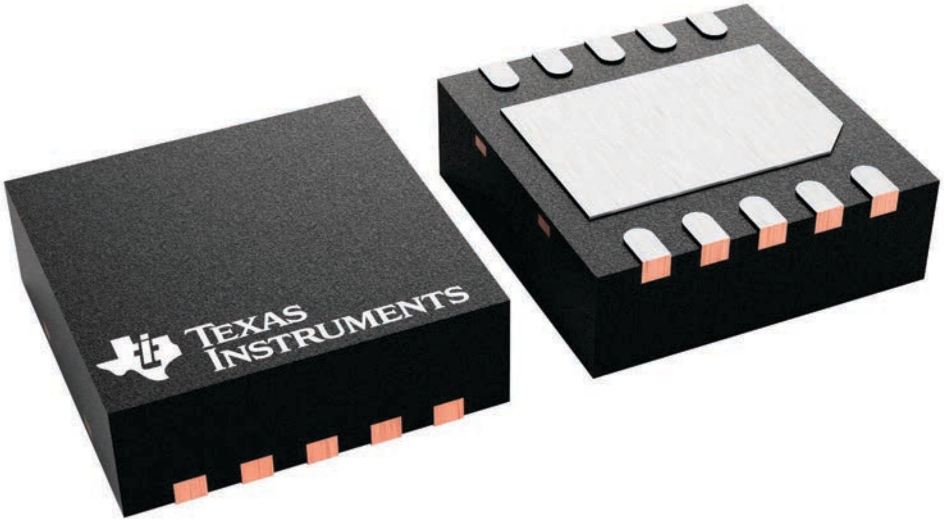
**DRC 10**

**VSON - 1 mm max height**

**3 x 3, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

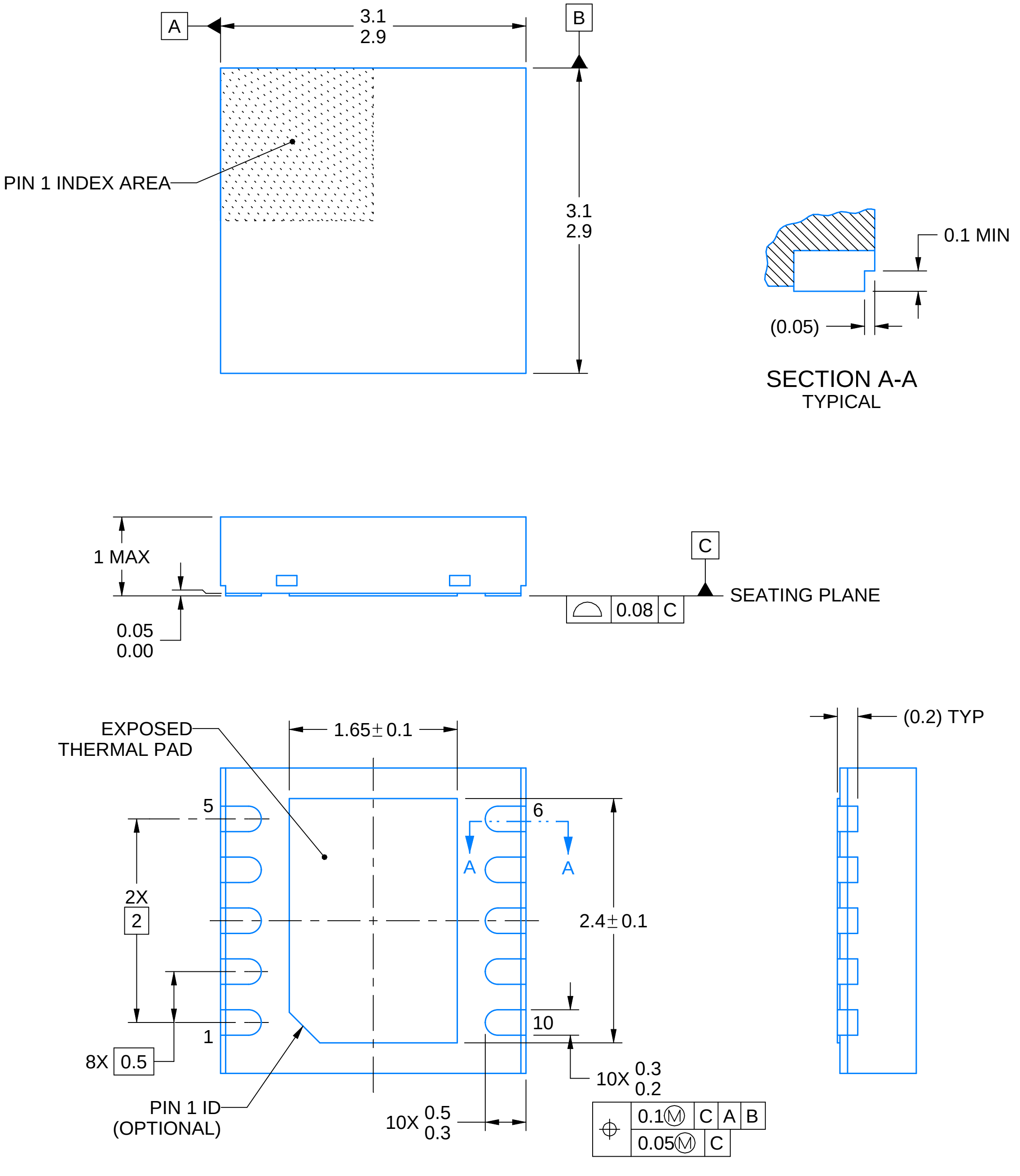


# PACKAGE OUTLINE

## DRC0010K

## VSON - 1 mm max height

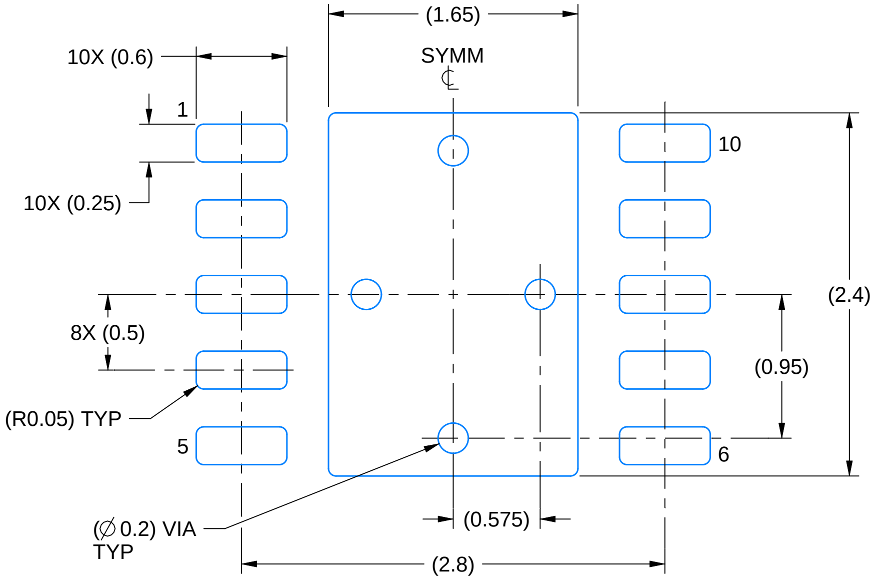
PLASTIC SMALL OUTLINE - NO LEAD



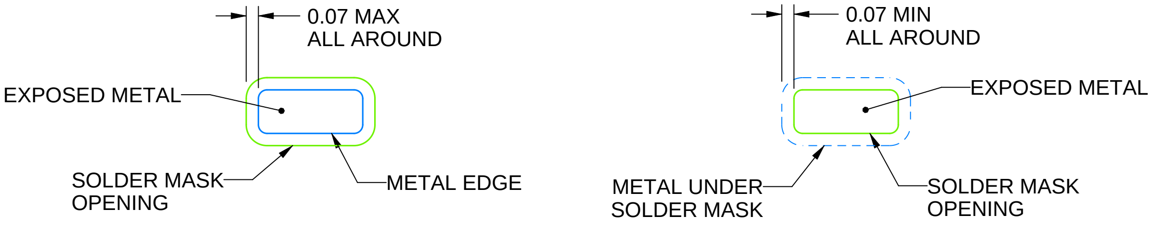
4222059/B 02/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



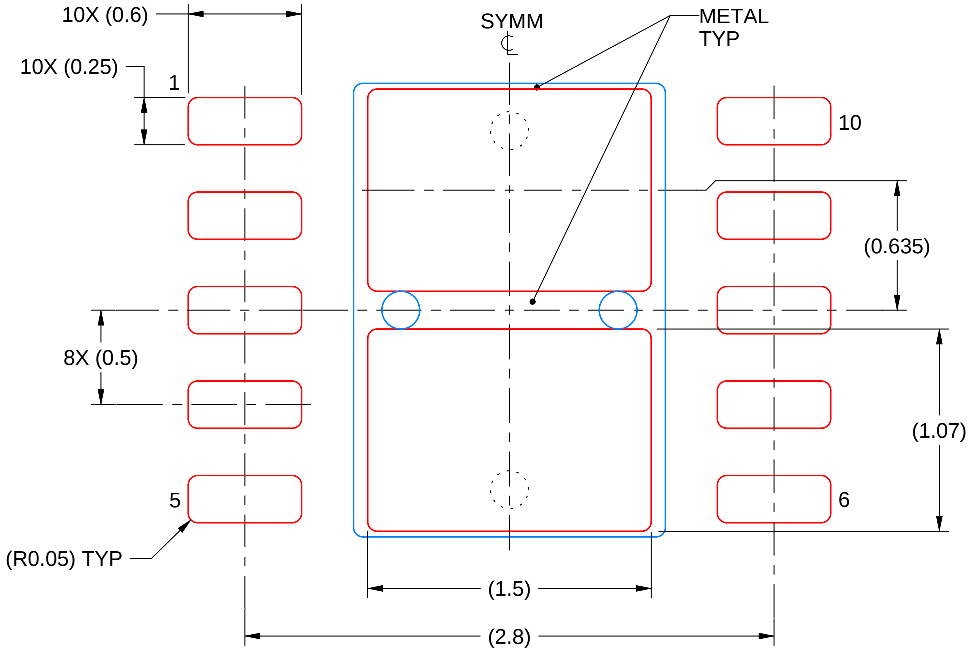
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要通知和免责声明

最后更新日期：2025 年 10 月