TPS25981x 具有瞬态过流消隐计时器的 2.7V 至 16V、10A、6mΩ 电子保险丝

1 特性

- 宽工作输入电压范围：2.7V 至 16V
  - 绝对最大值为 20V
- 具有低导通电阻的集成 FET：R_{ON} = 6mΩ（典型值）
- 快速过压保护
  - 可调节过压锁定 (OVLO)，响应时间为 1.2 µs（典型值）
- 过流保护，具有负载电流监测器输出 (ILM)
  - 断路器响应
  - 可调节阈值 (I_{LIM}) 1.5A - 11A
    - I_{LIM} > 5A 时精度为 ±10%
  - 可调瞬态消隐计时器 (ITIMER)，支持高达 2 × I_{LIM} 的峰值电流
  - 输出负载电流监控精度：±10% (I_{OUT} ≥ 3A)
- 通过快速跳变响应实现短路保护
  - 响应时间为 640 ns（典型值）
  - 可调节 (2 × I_{LIM}) 和固定阈值
- 具有可调节欠压锁定阈值 (UVLO) 的高电平有效使能输入
- 具有可调节欠压锁定阈值 (UVLO) 的低电平有效使能输入
- 可调节的输出压摆率控制 (dVdt)
- 可选择驱动外部 FET 以在禁用/关闭状态下实现反向电流阻断
- 过温保护
- 快速输出放电
- 数字输出
  - 电源正常 (PG) 和故障指示 ($\overline{FLT}$)
- UL2367 认证（正在申请中）
- IEC 62368 CB 认证（正在申请中）
- 小尺寸：QFN 2mm × 2mm，0.45mm 间距

2 应用

- 光学模块
- 服务器/PC 主板/附加卡
- 企业路由器/数据中心交换机
- 工业 PC
- UHDTV

3 说明

TPS25981xx 系列电子保险丝是采用小型封装的高度集成电路保护和电源管理解决方案。这些器件只需很少的外部元件即可提供多种保护模式，能够非常有效地抵御过载、短路、电压浪涌和过多浪涌电流。

可以使用单个外部电容器来调节输出压摆率和浪涌电流。通过在输入超过可调过压阈值时切断输出，可以保护负载免受输入过压情况的影响。此类器件通过主动限制电流（启动期间）或断开电路（稳态期间）来响应输出过载。用户可以调节过流保护阈值以及瞬态过流消隐计时器。电流限制控制引脚还用作模拟负载电流监测器。

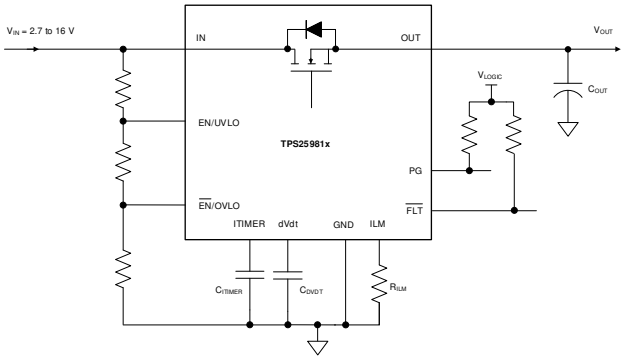
器件采用 2mm × 2mm 10 引脚 HotRod™ QFN 封装，旨在改善热性能并减小系统尺寸。

此类器件的额定工作结温范围为 –40°C 至 +125°C。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS25981	RPW（VQFN-HR，10）	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (July 2022) to Revision B (June 2023)	Page
• 添加了“为反向电流驱动外部 FET 的选项”	1
• Added variants TPS259813ARPW and TPS259813LRPW	3
• Updated the description of the DVDT pin	4
• Updated image formatting	11
• Updated image	19
• Updated 图 8-7	27
• Added 节 8.3.9	29

Changes from Revision * (April 2022) to Revision A (July 2022)	Page
• 将状态从“预告信息”更改为“量产数据”	1

5 Device Comparison Table

Part Number	Overvoltage Response	Overcurrent Response	Reverse Current Blocking FET driver	Response to Fault
TPS259814ARPW	Adjustable OVLO	Circuit-Breaker	No	Auto-Retry
TPS259814LRPW				Latch-Off
TPS259813ARPW			Yes	Auto-Retry
TPS259813LRPW				Latch-Off

6 Pin Configuration and Functions

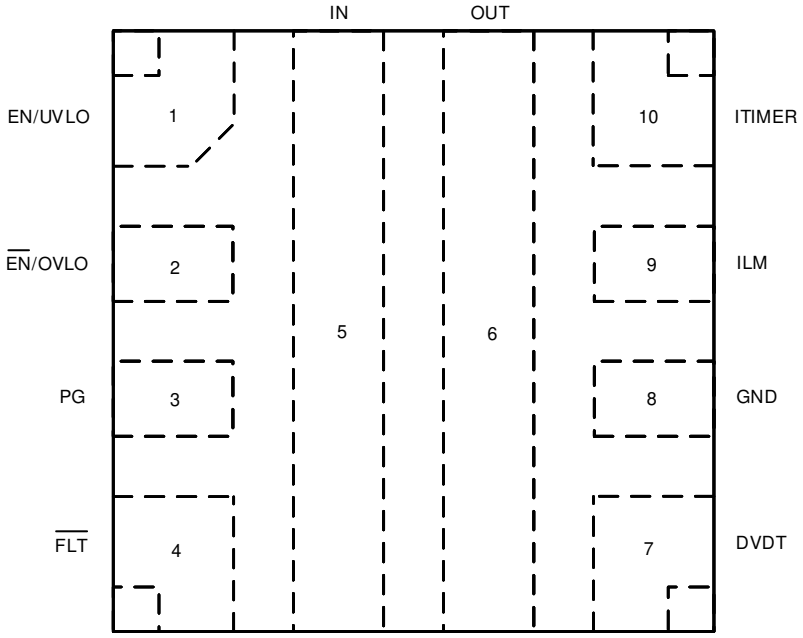


图 6-1. TPS25981xx RPW Package 10-Pin QFN Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active high enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the undervoltage lockout threshold. *Do not leave floating.* Refer to *Undervoltage Lockout (UVLO and UVP)* for details.
$\overline{EN}$/OVLO	2	Analog Input	A resistor divider on this pin from supply to GND can be used to adjust the overvoltage lockout threshold. This pin can also be used as an Active low enable for the device. *Do not leave floating.* Refer to *Overvoltage Lockout (OVLO)* for details.
PG	3	Digital Output	Power Good indication. This pin is an open-drain signal which is asserted high when the power FET has fully turned ON and is ready to deliver power. Refer to *Power Good (PG)* for more details.
$\overline{FLT}$	4	Digital Output	Active low fault event indicator. This pin is an open-drain signal which is pulled low when a fault is detected. Refer to *Fault Response and Indication ($\overline{FLT}$)* for more details.
IN	5	Power	Power input
OUT	6	Power	Power output
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn-on slew rate. Refer to *Slew Rate (dVdt) and Inrush Current Control* for details. Only for TPS259813x variants, this pin can also be used to drive an external FET to implement reverse current blocking. Please refer to *Reverse Current Blocking FET Driver* for more details.
GND	8	Ground	This pin is the ground reference for all internal circuits and must be connected to system GND.
ILM	9	Analog Output	This pin is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the overcurrent protection threshold during start-up as well as steady-state. The pin voltage can also be used as analog output load current monitor signal. *Do not leave floating.* Refer to *Circuit-Breaker During Steady-state* or *Active Current Limiting During Start-up* for more details.

表 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
ITIMER	10	Analog Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) during steady-state before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to *Circuit-Breaker During Steady-state* for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40℃ ≤ T_J ≤ 125℃	IN	–0.3	20	V
V_{OUT}	Maximum output voltage range, –40℃ ≤ T_J ≤ 125℃	OUT	–0.3	V_{IN} + 0.3	
$V_{OUT,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable pin voltage range	EN/UVLO	–0.3	6.5	V
V_{OV}	Maximum $\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	–0.3	6.5	V
V_{dVdT}	Maximum dVdT pin voltage range	dVdt	Internally limited		V
V_{ITIMER}	Maximum ITIMER pin voltage range	ITIMER	Internally limited		V
V_{PG}	Maximum PG pin voltage range	PG	–0.3	6.5	V
V_{FLTB}	Maximum $\overline{FLT}$ pin voltage range	$\overline{FLT}$	–0.3	6.5	V
V_{ILM}	Maximum ILM pin voltage range	ILM	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	16	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5(1)	V
V_{OV}	$\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	0.5	1.5	V
V_{dVdT}	dVdT pin capacitor voltage rating	dVdt	V_{IN} + 5 V		V
V_{FLTB}	$\overline{FLT}$ pin voltage range	$\overline{FLT}$		5	V
V_{PG}	PG pin voltage range	PG		5	V
V_{ITIMER}	ITIMER pin capacitor voltage rating	ITIMER	4		V
R_{ILM}	ILM pin resistance to GND	ILM	600	4400	Ω
I_{MAX}	Continuous switch current, T_J ≤ 125℃	IN to OUT		10	A

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V , it is recommended to use a resistor divider with minimum pull-up resistor value of 350 kΩ.

7.4 Thermal Information

THERMAL METRIC (1)		TPS25981xx RPW (QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7(2)	°C/W
		71.8(3)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1(2)	°C/W
	Junction-to-top characterization parameter	1.3(3)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23 (2)	°C/W
		14.5 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 611 Ω , dVdT = Open, ITIMER = Open, $\overline{FLT}$ = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current		417	610	µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		68	90	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		3	25	µA
$V_{UVP(R)}$	IN supply UVP rising threshold	2.44	2.53	2.64	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.35	2.42	2.55	V
OUTPUT LOAD CURRENT MONITOR (ILM)					
G_{IMON}	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 1.5 A, I_{OUT} < I_{LIM}	82.9	95.3	107.6	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 3 A, I_{OUT} < I_{LIM}	87	95.3	104.5	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 4.5 A, I_{OUT} < I_{LIM}	87.6	95.3	103.1	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 8 A, I_{OUT} < I_{LIM}	87.7	95.3	102.6	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 10 A, I_{OUT} < I_{LIM}	87.8	95.3	102.4	µA/A
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent threshold, R_{ILM} = 3320 Ω	1.72	1.99	2.26	A
	Overcurrent threshold, R_{ILM} = 2212 Ω	2.64	2.98	3.32	A
	Overcurrent threshold, R_{ILM} = 1102 kΩ	5.43	5.98	6.52	A
	Overcurrent threshold, R_{ILM} = 750 Ω	7.95	8.73	9.52	A
	Overcurrent threshold, R_{ILM} = 611 Ω	9.8	10.76	11.73	A
I_{SPFLT}	Circuit-Breaker threshold, ILM pin open (Single point failure)			0.1	A
I_{SPFLT}	Circuit-Breaker threshold, ILM pin shorted to GND (Single point failure)		2.24	3.3	A
I_{FT}	Fixed fast-trip current threshold		39.5		A
I_{SCGain}	Scalable fast-trip threshold (I_{SC}) : I_{LIM} ratio	170	193	242	%
V_{FB}	V_{OUT} threshold to exit current limit foldback	1.55	1.91	2.23	V
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} ≤ 4 V, I_{OUT} = 3 A, T_J = 25℃		6.07		mΩ
	4 < V_{IN} ≤ 16 V, I_{OUT} = 3 A, T_J = 25℃		5.81		mΩ
	2.7 ≤ V_{IN} ≤ 16 V, I_{OUT} = 3 A, –40℃ ≤ T_J ≤ 125℃			8.4	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.176	1.20	1.224	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.073	1.09	1.116	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.45	0.75		V
I_{ENLKG}	EN/UVLO pin leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT ($\overline{EN}$/OVLO)					
$V_{OV(R)}$	OVLO rising threshold	1.176	1.20	1.224	V
$V_{OV(F)}$	OVLO falling threshold	1.074	1.09	1.116	V
I_{OVLKG}	OVLO pin leakage current (0.5 V < V_{OVLO} < 1.5 V)	–0.1		0.1	µA
OVERCURRENT FAULT TIMER (ITIMER)					

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 611 Ω , dVdT = Open, ITIMER = Open, $\overline{FLT}$ = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
I_{ITIMER}	ITIMER pin internal discharge current, I_{OUT} > I_{LIM}	1.25	2	2.72	µA
R_{ITIMER}	ITIMER pin internal pullup resistance		15.4		kΩ
V_{INT}	ITIMER pin internal pullup voltage	2.1	2.57	2.74	V
$V_{ITIMER(F)}$	ITIMER comparator threshold, I_{OUT} > I_{LIM}	0.6	1.06	1.37	V
ΔV_{ITIMER}	ITIMER discharge differential voltage threshold, I_{OUT} > I_{LIM}	1.28	1.51	1.74	V
POWER GOOD INDICATION (PG)					
V_{PGD}	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pullup (I_{PG} = 26 µA)		0.66	0.80	V
	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pullup (I_{PG} = 242 µA)		0.78	0.90	V
	PG pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0	0.60	V
I_{PGLKG}	PG pin leakage current, PG asserted			3	µA
R_{FLTB}	$\overline{FLT}$ pin internal pulldown resistance		12.57		Ω
FAULT INDICATION ($\overline{FLT}$)					
I_{FLTLKG}	$\overline{FLT}$ pin leakage current	–1		1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J ↑		154		°C
TSD_{HYS}	Thermal Shutdown hysteresis, T_J ↓		10		°C
DVDT					
I_{dVdt}	dVdt pin internal charging current	1.4	3.45	5.7	µA
QUICK OUTPUT DISCHARGE (OUT)					
R_{QOD}	Quick Output Discharge Resistance, V_{EN} < $V_{UVLO(F)}$	455	488	530	Ω

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT} ↓		1.2		µs
t_{CB}	Circuit-Breaker response time	ITIMER = Open, I_{OUT} > I_{LIM} + 30% to V_{OUT} ↓		1.8		µs
t_{SC}	Short-circuit response time	I_{OUT} > 3 × I_{LIM} to output current cut off		640		ns
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT} ↓		640		ns
$t_{TSD,RST}$	Thermal Shutdown auto-retry Interval	Device enabled and T_J < TSD – TSD_{HYS}		105		ms
t_{PGA}	PG assertion de-glitch time			14		µs
t_{PGD}	PG de-assertion de-glitch time			14		µs

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it slows the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady-state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNITS
SR_{ON}	Output rising slew rate	2.7 V	8.19	1.30	0.78	V/ms
		5 V	11.28	1.42	0.84	
		12 V	19.71	1.68	0.98	
$t_{D,ON}$	Turn-on delay	2.7 V	0.14	0.46	0.70	ms
		5 V	0.14	0.60	0.96	
		12 V	0.14	0.93	1.57	
t_R	Rise time	2.7 V	0.26	1.66	2.77	ms
		5 V	0.36	2.82	4.78	
		12 V	0.49	5.74	9.84	
t_{ON}	Turn-on time	2.7 V	0.40	2.11	3.47	ms
		5 V	0.50	3.42	5.74	
		12 V	0.63	6.67	11.41	
$t_{D,OFF}$	Turn-off delay	2.7 V	24.90	24.90	24.90	µs
		5 V	21.10	21.10	21.10	
		12 V	18.80	18.80	18.80	

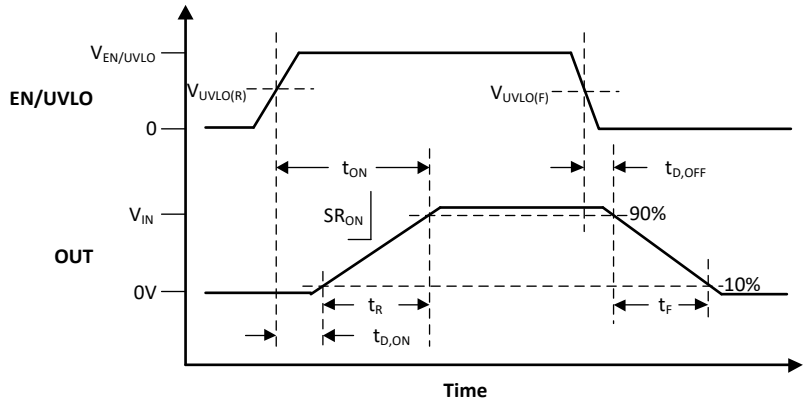


图 7-1. TPS25981xx Switching Times

7.8 Typical Characteristics

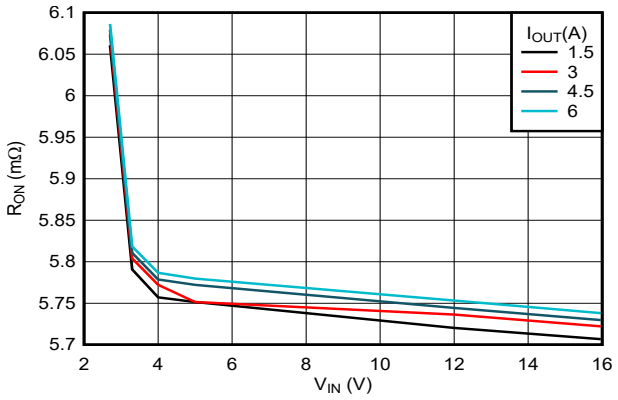


图 7-2. ON-Resistance vs Supply Voltage (T_A = 25°C)

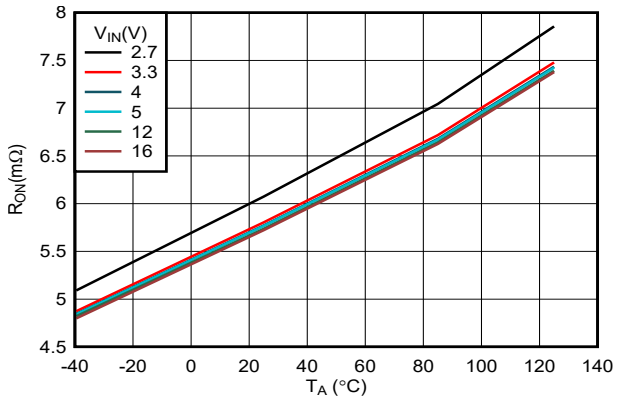


图 7-3. ON-Resistance vs Temperature (I_{OUT} = 3 A)

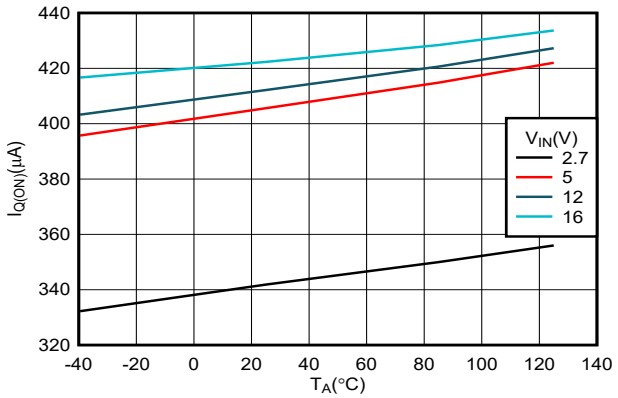


图 7-4. IN Quiescent Current vs Temperature

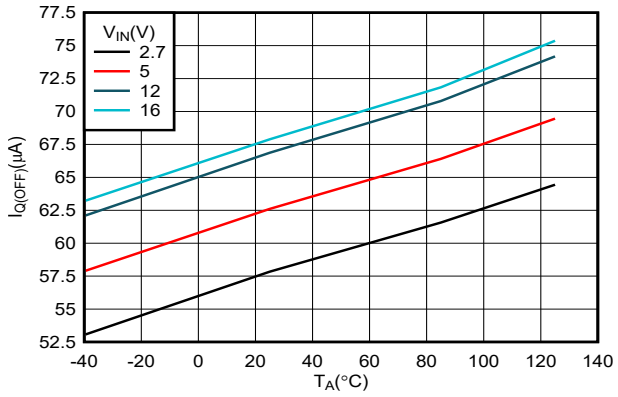


图 7-5. IN OFF State (UVLO) Current vs Temperature

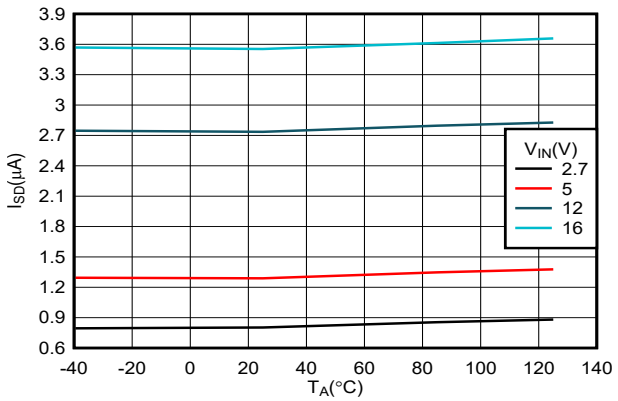


图 7-6. IN Shutdown Current vs Temperature

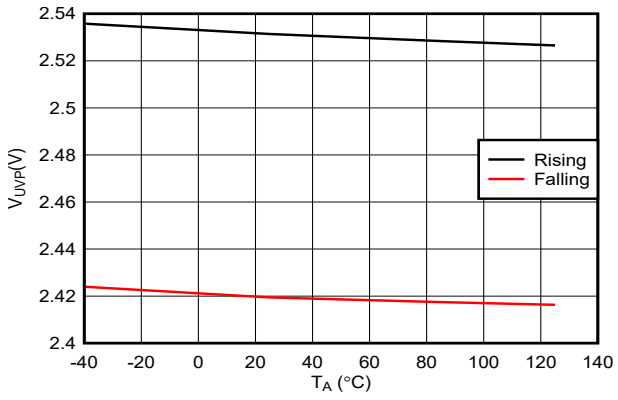


图 7-7. IN Undervoltage Threshold vs Temperature

7.8 Typical Characteristics (continued)

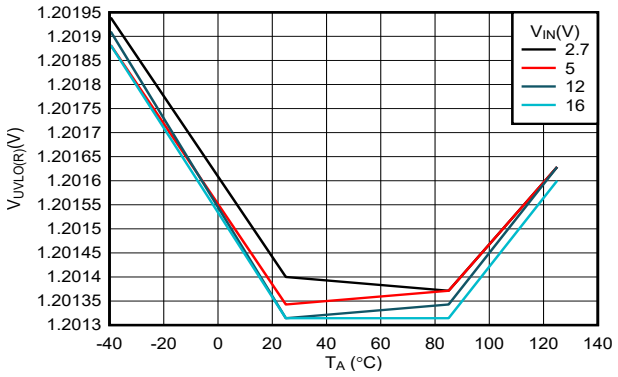


图 7-8. EN/UVLO Rising Threshold vs Temperature

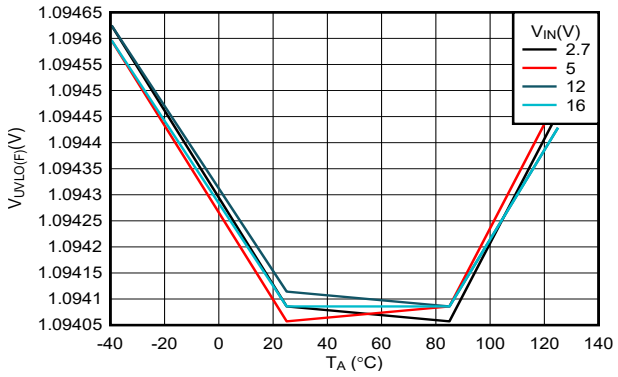


图 7-9. EN/UVLO Falling Threshold vs Temperature

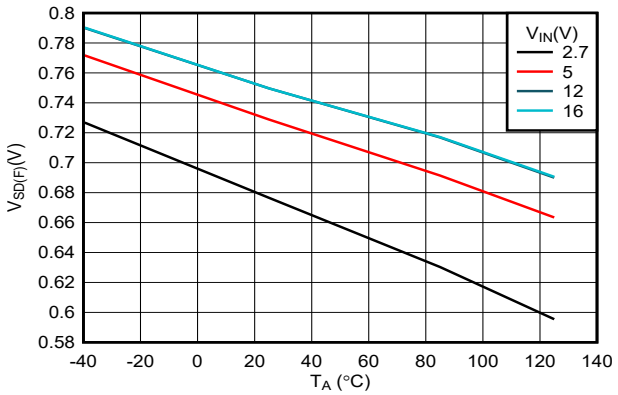


图 7-10. EN/UVLO Shutdown Falling Threshold vs Temperature

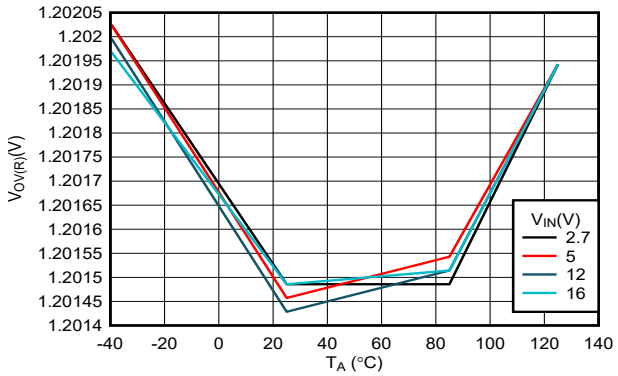


图 7-11. OVLO Rising Threshold vs Temperature

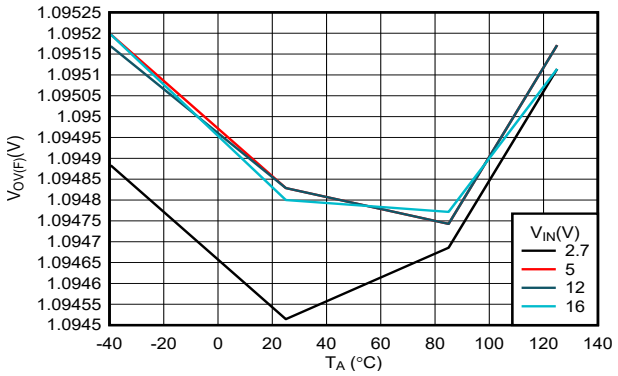


图 7-12. OVLO Falling Threshold vs Temperature

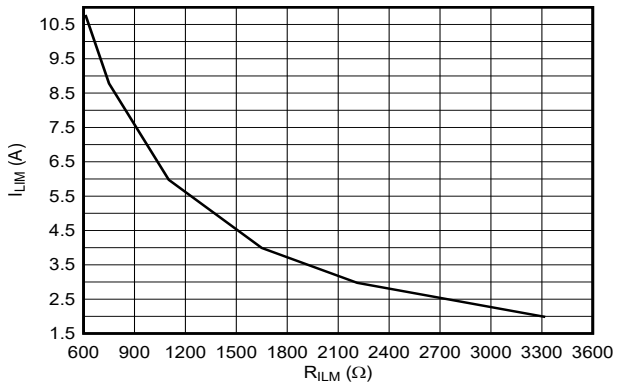


图 7-13. Overcurrent Threshold vs ILM Resistor

7.8 Typical Characteristics (continued)

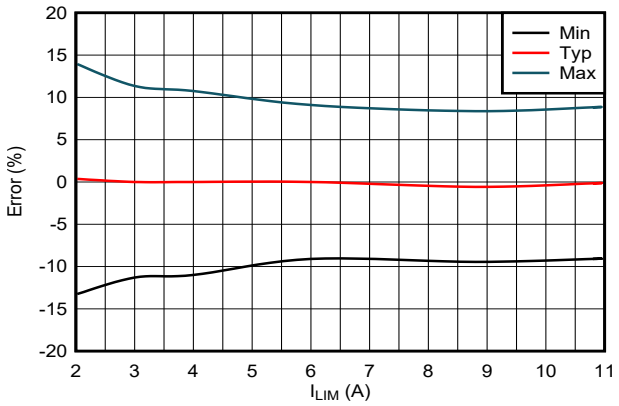


图 7-14. Overcurrent Threshold Accuracy (Across Process, Voltage and Temperature)

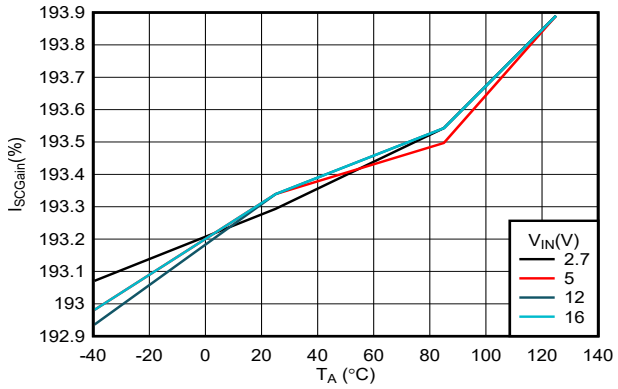


图 7-15. Scalable Fast-Trip Threshold: Current Limit Threshold (I_{LIM}) Ratio vs Temperature

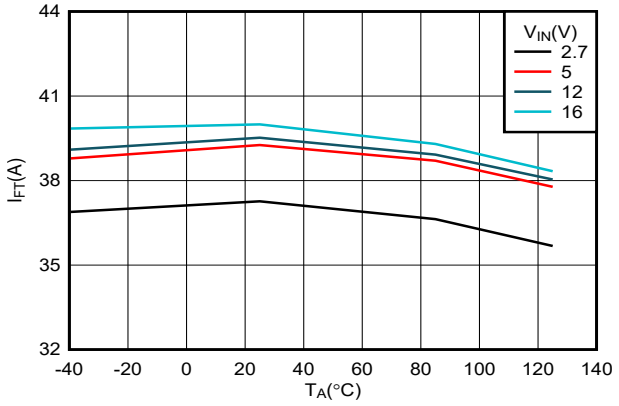


图 7-16. Fixed Fast-Trip Threshold vs Temperature

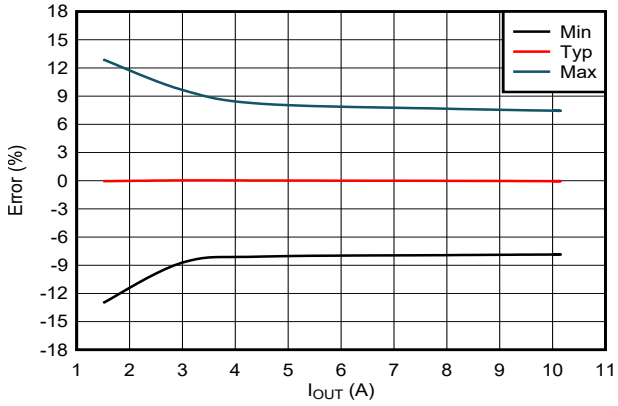


图 7-17. Analog Current Monitor Gain Accuracy

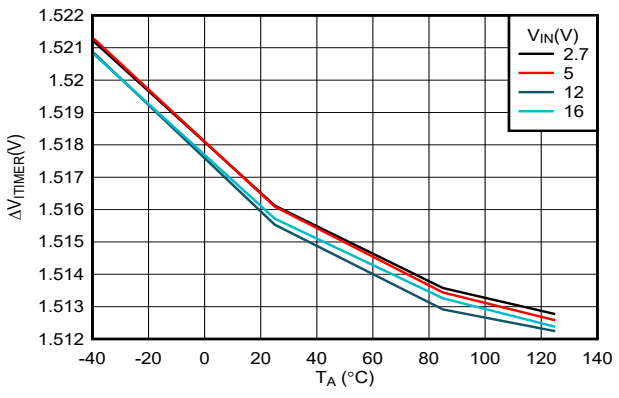


图 7-18. ITIMER Discharge Differential Voltage Threshold vs Temperature

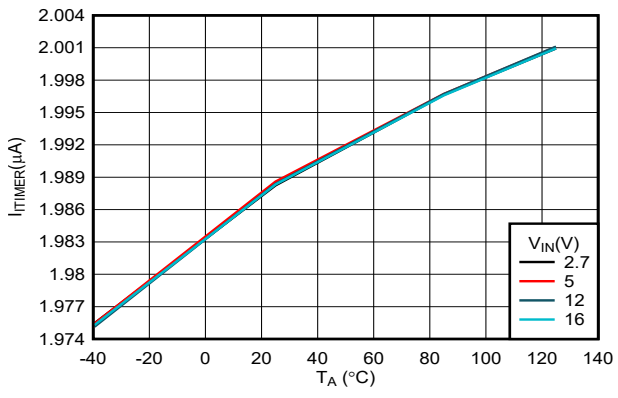


图 7-19. ITIMER Discharge Current vs Temperature

7.8 Typical Characteristics (continued)

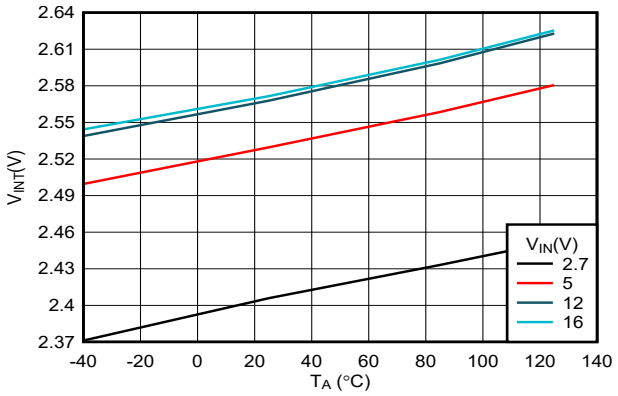


图 7-20. ITIMER Internal Pullup Voltage vs Temperature

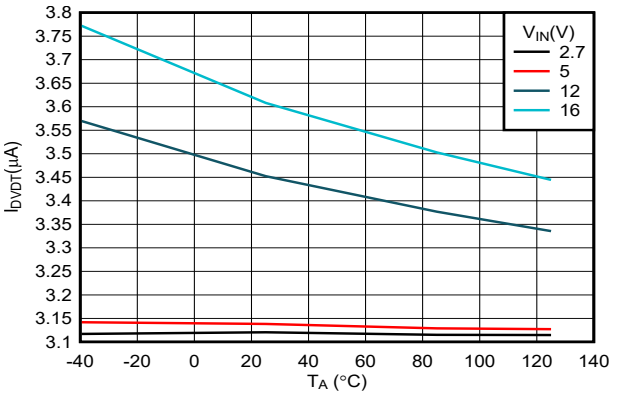


图 7-21. DVDT Charging Current vs Temperature

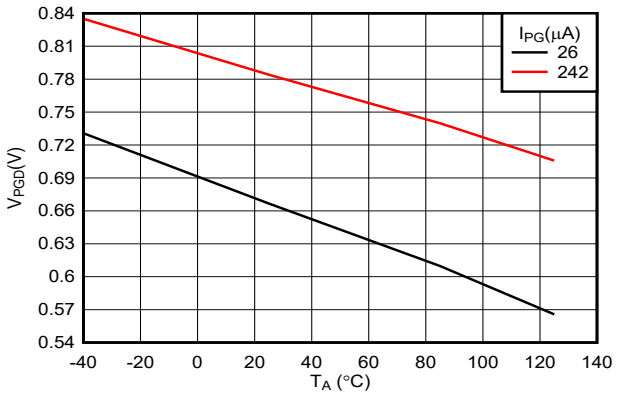


图 7-22. PG Pin Voltage vs Temperature (VIN = 0 V)

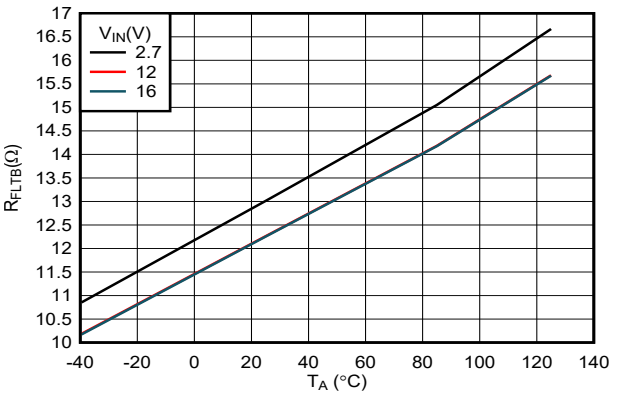


图 7-23. $\overline{\text{FLT}}$ Pin Pulldown Resistance vs Temperature

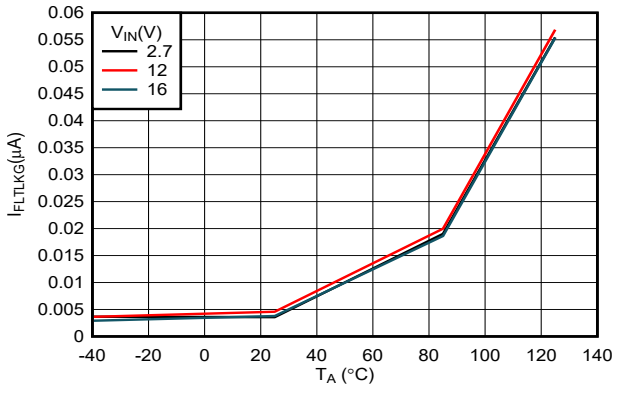


图 7-24. $\overline{\text{FLT}}$ Pin Leakage Current vs Temperature

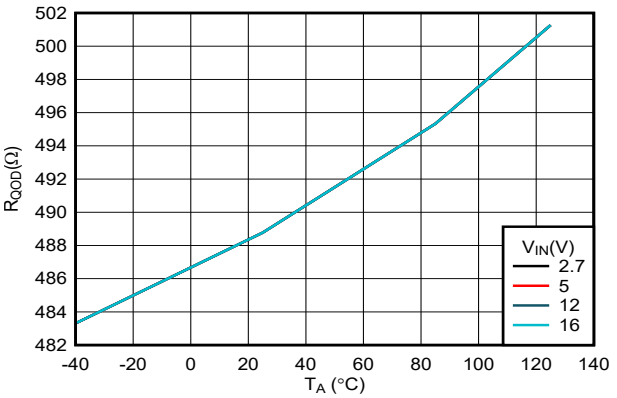


图 7-25. Quick Output Discharge Resistance vs Temperature

7.8 Typical Characteristics (continued)

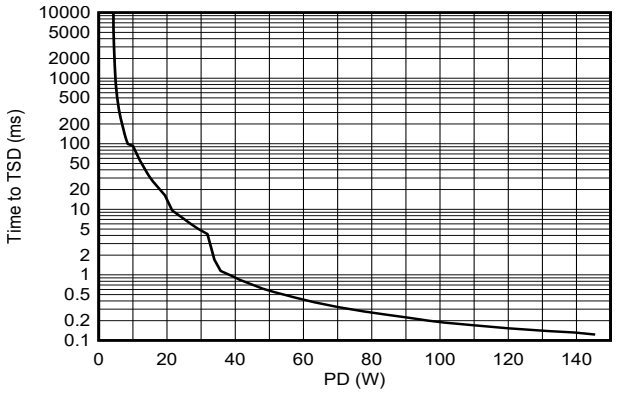


图 7-26. Time to Thermal Shutdown During Inrush State

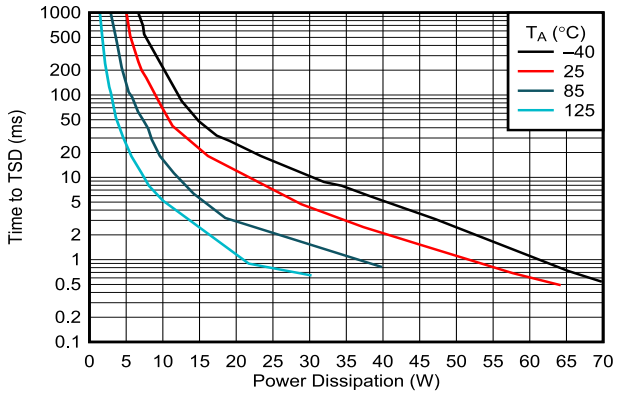
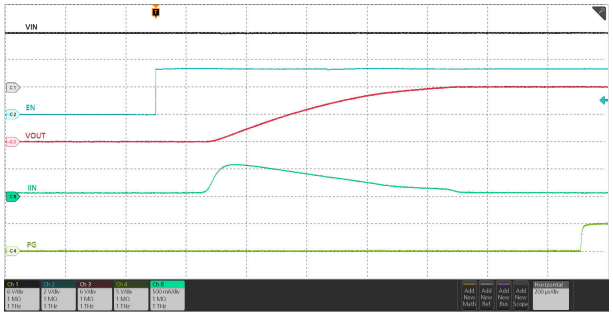
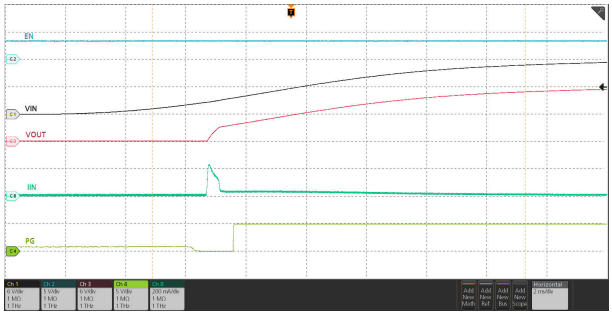


图 7-27. Time to Thermal Shutdown During Steady-State



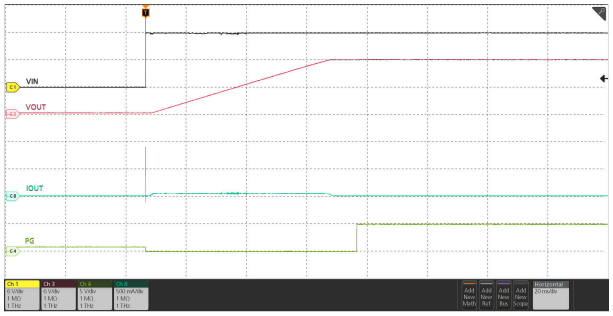
V_{IN} = 12 V, C_{OUT} = 10 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 3.3 V

图 7-28. Start-Up with Enable



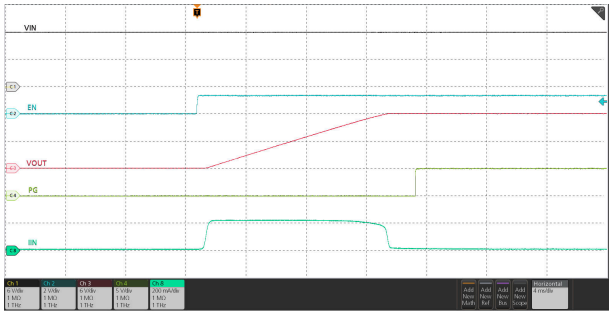
$V_{EN/UVLO}$ = 3.3 V, C_{OUT} = 10 µF, C_{dVdt} = Open, V_{IN} ramped up to 12 V

图 7-29. Start-Up with Supply



C_{OUT} = 220 µF, C_{dVdt} = 15 nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

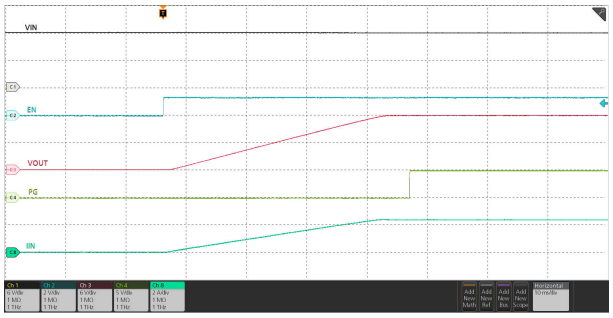
图 7-30. Input Hot-Plug



V_{IN} = 12 V, C_{OUT} = 220 µF, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

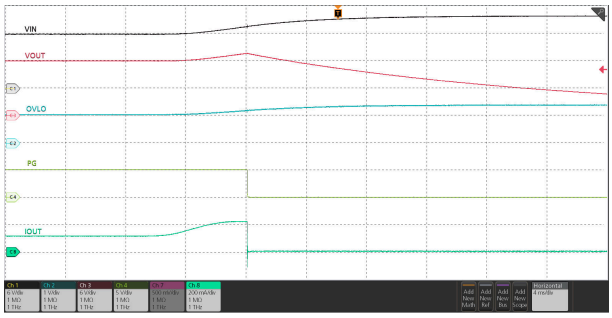
图 7-31. Inrush Current with Capacitive Load

7.8 Typical Characteristics (continued)



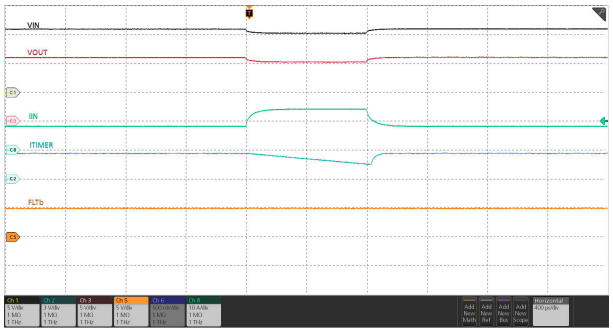
V_{IN} = 12 V, C_{OUT} = 220 µF, R_{OUT} = 5 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

图 7-32. Inrush Current with Resistive and Capacitive Load



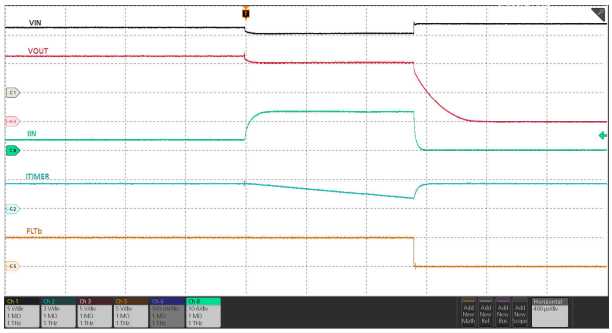
V_{IN} Overvoltage threshold set to 13.6 V using resistor ladder connected to OVLO pin, V_{IN} ramped up from 12 V to 16 V

图 7-33. Overvoltage Lockout Response



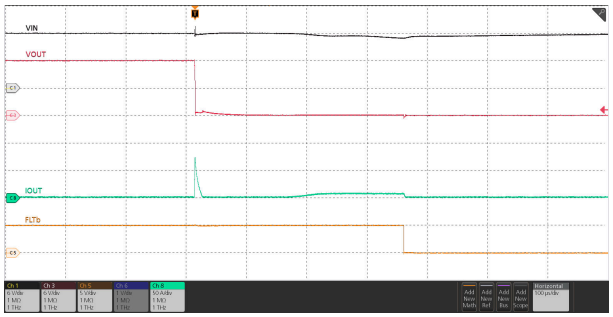
V_{IN} = 12 V, C_{ITIMER} = 1.5 nF, R_{ILM} = 649 Ω, I_{OUT} ramped from 8 A → 14 A→ 8 A within 1 ms

图 7-34. Transient Overcurrent Blanking Timer Response



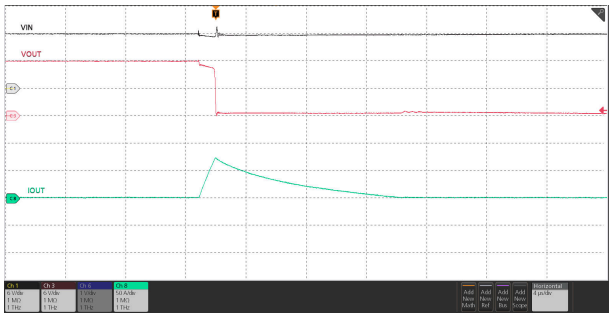
V_{IN} = 12 V, C_{ITIMER} = 1.5 nF, R_{ILM} = 649 Ω, I_{OUT} ramped from 4 A → 13 A

图 7-35. Circuit-Breaker Response



V_{IN} = 12 V, R_{ILM} = 649 Ω, OUT stepped from Open → Short-circuit to GND

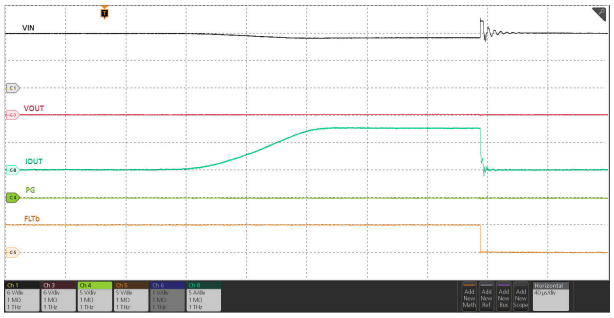
图 7-36. Output Short-Circuit During Steady-State



V_{IN} = 12 V, R_{ILM} = 649 Ω, OUT stepped from Open → Short-circuit to GND

图 7-37. Output Short-Circuit During Steady-State (Zoomed In)

7.8 Typical Characteristics (continued)



V_{IN} = 12 V, OUT short-circuit to GND, R_{ILM} = 649 Ω, $V_{EN/UVLO}$ stepped from 0 V to 3.3 V

图 7-38. Power Up into Short Circuit

8 Detailed Description

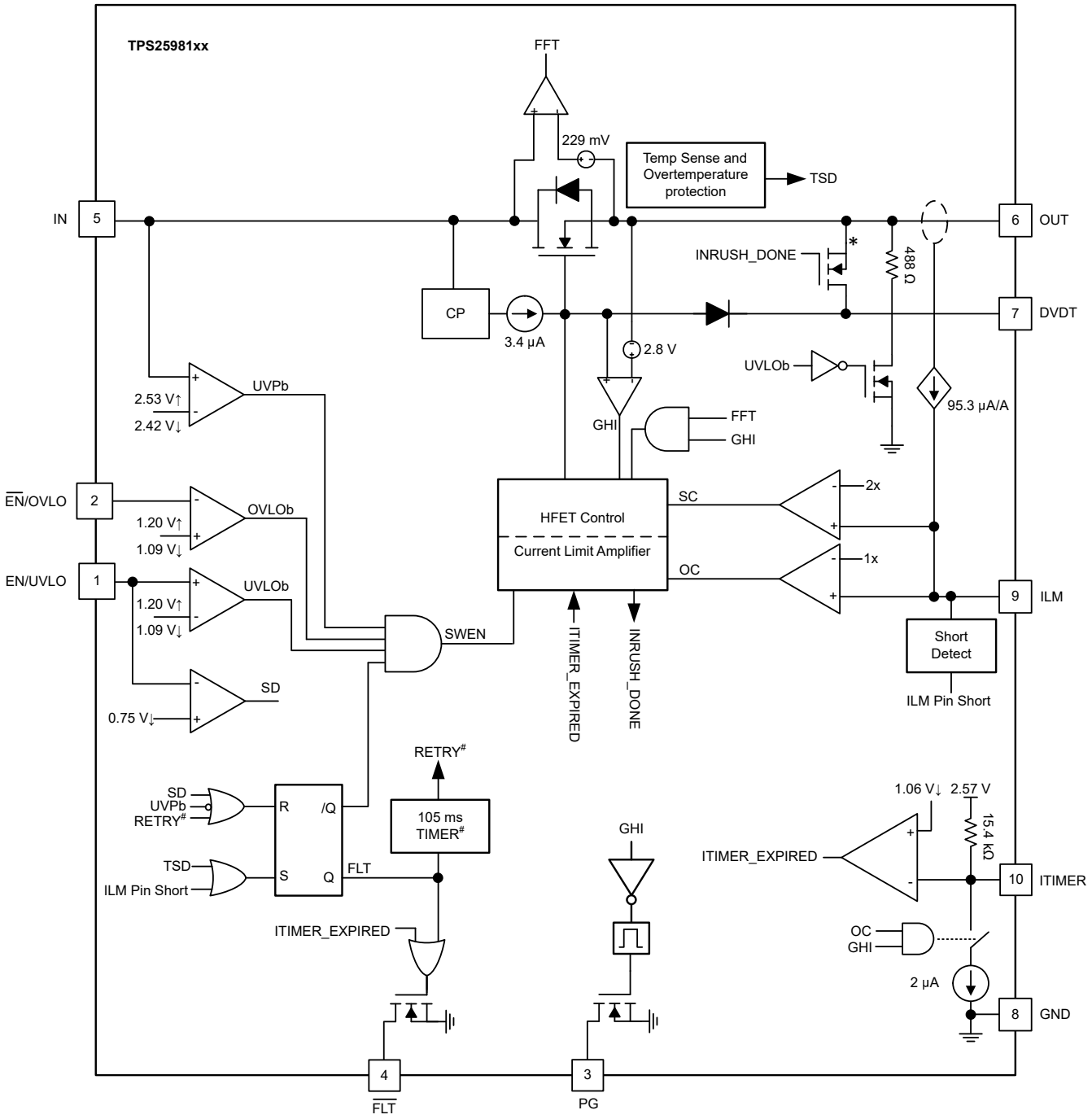
8.1 Overview

The TPS25981xx is an eFuse with integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the Undervoltage Protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the user adjustable overcurrent protection threshold (I_{LIM}) is not exceeded and overvoltage spikes are cut-off after they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). The device also provides fast protection against severe overcurrent during short-circuit events. This feature keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This feature ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

8.2 Functional Block Diagram



Not applicable to TPS25981xL (Latch-off) variants
* Not applicable for TPS259813x variants

8.3 Feature Description

The TPS25981xx eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS25981xx implements undervoltage protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. 图 8-1 and 方程式 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

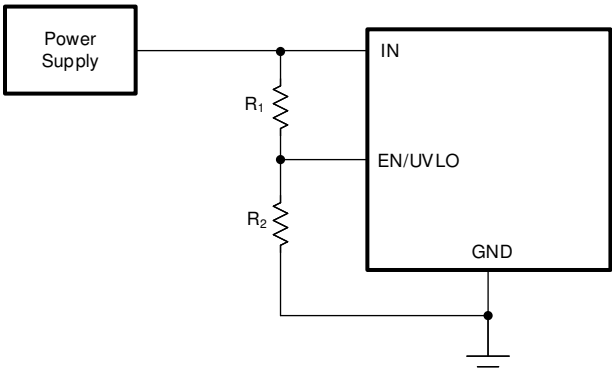


图 8-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

8.3.2 Overvoltage Lockout (OVLO)

The TPS259814x devices allow the user to implement overvoltage lockout to protect the load from input overvoltage conditions. The OVLO comparator on the $\overline{EN}$/OVLO pin allows the overvoltage protection threshold to be adjusted to a user defined value. After the voltage at the $\overline{EN}$/OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the $\overline{EN}$/OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysteresis. 图 8-2 and 方程式 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

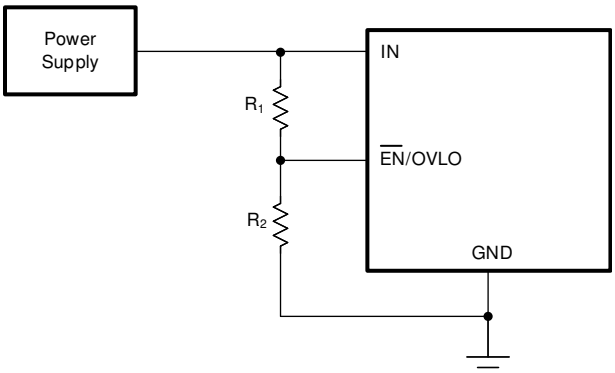


图 8-2. Adjustable Overvoltage Protection

$$V_{IN(OV)} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \quad (2)$$

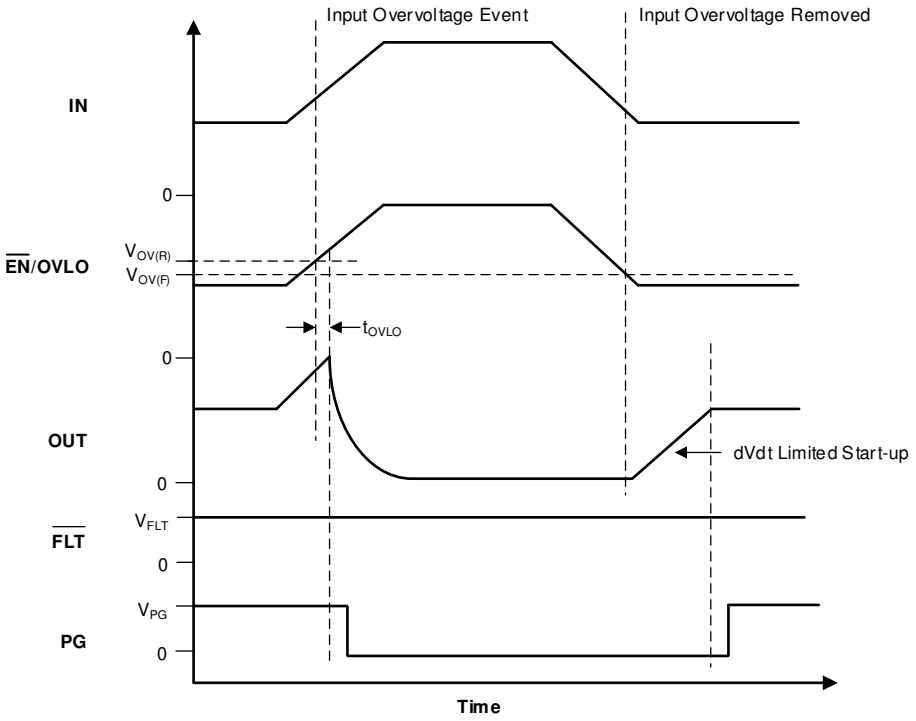


图 8-3. TPS259814x Overvoltage Lockout and Recovery

While recovering from a OVLO event, the TPS259814x variants start up with inrush control (dVdt).

8.3.3 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS25981xx incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
4. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short circuits during steady-state

8.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. 方程式 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{3}$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. Use 方程式 4 to calculate the required C_{dVdt} capacitance to produce a given slew rate.

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} \tag{4}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

备注

For C_{dVdt} > 10 nF, TI recommends to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

8.3.3.2 Circuit-Breaker During Steady-State

The TPS259814x (circuit-breaker) variants respond to output overcurrent conditions by turning off the output after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the fast-trip threshold (2 × I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal 2-µA pulldown current. If the load current drops below I_{LIM} before the ITIMER pin capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit-breaker action is not engaged. This action allows short load transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and after it discharges by ΔV_{ITIMER}, the circuit-breaker action turns off the FET immediately. At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This action ensures the full blanking timer interval is provided for every overcurrent event. 方程式 5 can be used to calculate the R_{ILM} value for a overcurrent threshold.

$$R_{ILM}\,(\Omega) = \frac{6585}{I_{LIM}\,(A)} \tag{5}$$

备注

1. Leaving the ILM pin open sets the current limit to nearly zero and results in the part breaking the circuit with the slightest amount of loading at the output.
2. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There is a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. Use 方程式 6 to calculate the C_{ITIMER} value needed to set the desired transient overcurrent blanking interval.

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms) \times I_{ITIMER}\,(\mu A)}{\Delta V_{ITIMER}\,(V)} \tag{6}$$

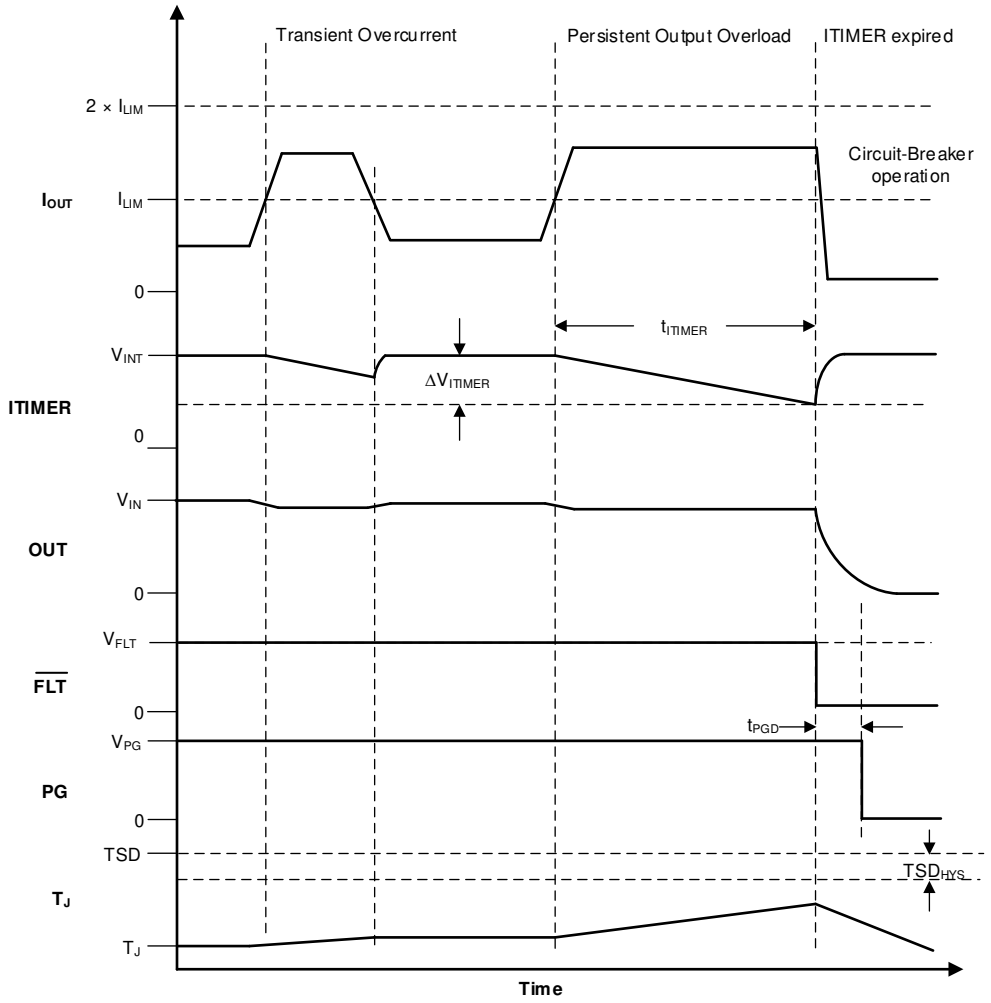


图 8-4. TPS259814x Overcurrent Response

备注

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This action is not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it takes lesser time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.
4. In low voltage applications, TI recommends adding a 30 kΩ resistor between the ITIMER pin and C_{ITIMER} for improved immunity to supply noise or fluctuations.

After the part shuts down due to a circuit-breaker fault, it either stays latched off (TPS259814L variant) or restarts automatically after a fixed delay (TPS259814A variant).

8.3.3.3 Active Current Limiting During Start-Up

The TPS259814x devices respond to output overcurrent conditions during start-up by actively limiting the current. If the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold (2 × I_{LIM}), the current limit loop starts regulating the FET to actively

limit the current to the set overcurrent threshold (I_{LIM}). 方程式 7 can be used to calculate the R_{ILM} value for a desired overcurrent threshold.

$$R_{ILM}\,(\Omega) = \frac{6585}{I_{LIM}\,(A)} \tag{7}$$

备注

1. Leaving the ILM pin open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
2. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the target steady-state overcurrent threshold (I_{LIM}).

During active current limit, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to TSD fault, it either stays latched off (TPS25981xL variants) or restarts automatically after a fixed delay (TPS25981xA variants). For more details on device response to overtemperature, see *Overtemperature Protection (OTP)*.

8.3.3.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the device triggers a fast-trip response to limit the current to a safe level. The internal fast-trip comparator employs a scalable threshold (I_{SC}) which is equal to 2 × I_{LIM}. This action enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short circuits during steady-state. The fixed fast-trip threshold is higher than the maximum recommended user adjustable scalable fast-trip threshold. After the current exceeds I_{SC} or I_{FT}, the FET is turned off completely within t_{FT}. Thereafter, the devices tries to turn the FET back on after a short de-glitch interval (30 µs) in a current limited manner instead of a dVdt limited manner. This action ensures that the FET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device stays in current limit causing the junction temperature to rise and eventually enter thermal shutdown. For details on the device response to overtemperature, see *Overtemperature Protection (OTP)*.

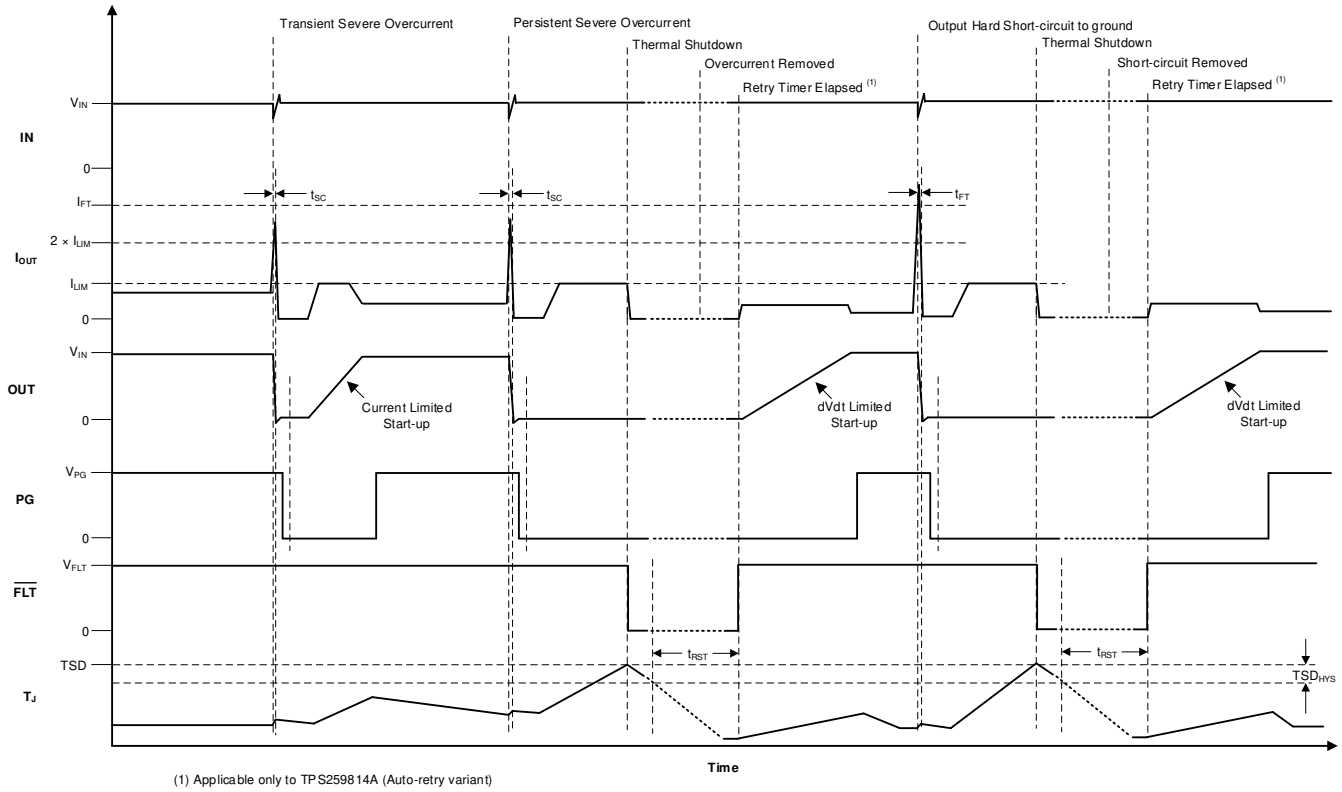


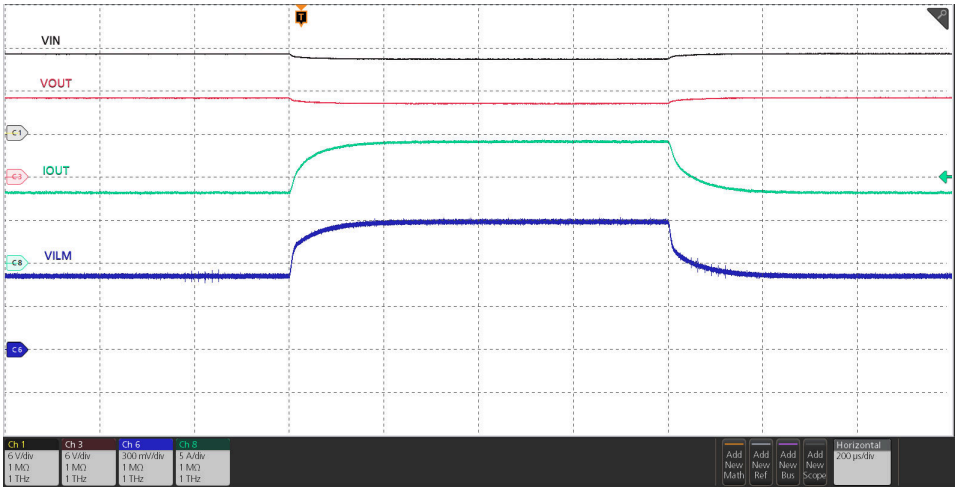
图 8-5. TPS25981xx Short-Circuit Response

8.3.4 Analog Load Current Monitor

The device allows the system to accurately monitor the output load current by providing an analog current sense output on the ILM pin which is proportional to the current through the FET. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$I_{LOAD}\,(A) = \frac{V_{ILM}\,(\mu V)}{G_{IMON}\,(\mu A/A) \times R_{ILM}\,(\Omega)} \tag{8}$$

The waveform below shows the ILM signal response to a load step at the output.



V_{IN} = 12 V, R_{ILM} = 649 Ω, I_{OUT} varied dynamically between 8 A and 14 A

图 8-6. Analog Load Current Monitor Response

备注

The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50 pF for stable operation.

8.3.5 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device does turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS25981xL (latch-off variant) detects thermal overload, it is shut down and remains latched-off until the device is power cycled or re-enabled. When the TPS25981xA (auto-retry variant) detects thermal overload, it remains off until it has cooled down by TSD_{HYS}. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

表 8-1. Thermal Shutdown

Device	Enter TSD	Exit TSD
TPS25981xL (latch-off)	$T_J \geq$ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ *or* EN/UVLO toggled below $V_{SD(F)}$
TPS25981xA (auto-retry)	$T_J \geq$ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ *or* EN/UVLO toggled below $V_{SD(F)}$ *or* t_{RST} timer expired

8.3.6 Fault Response and Indication ($\overline{FLT}$)

The following table summarizes the device response to various fault conditions. Additionally, an active low external fault indication ($\overline{FLT}$) pin is available.

表 8-2. Fault Summary

Event	Protection Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	$\overline{FLT}$ Assertion Delay
Overtemperature	Shutdown	Y	L	
Undervoltage (UVP or UVLO)	Shutdown	N	H	
Input overvoltage	Shutdown	N	H	
Transient overcurrent (I_{LIM} < I_{OUT} < 2 × I_{LIM})	None	N	N	
Persistent overcurrent	Circuit-breaker	Y	N/A	
Output short circuit to GND	Circuit-breaker followed by current limit	N	H	
ILM pin open (during steady-state)	Shutdown	N	L	t_{ITIMER}
ILM pin shorted to GND	Shutdown	Y	L	t_{ITIMER}

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}. This action also releases the $\overline{FLT}$ pin and resets the t_{RST} timer for the TPS25981xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This fact is true for both TPS25981xL (latch-off) and TPS25981xA (auto-retry) variants.

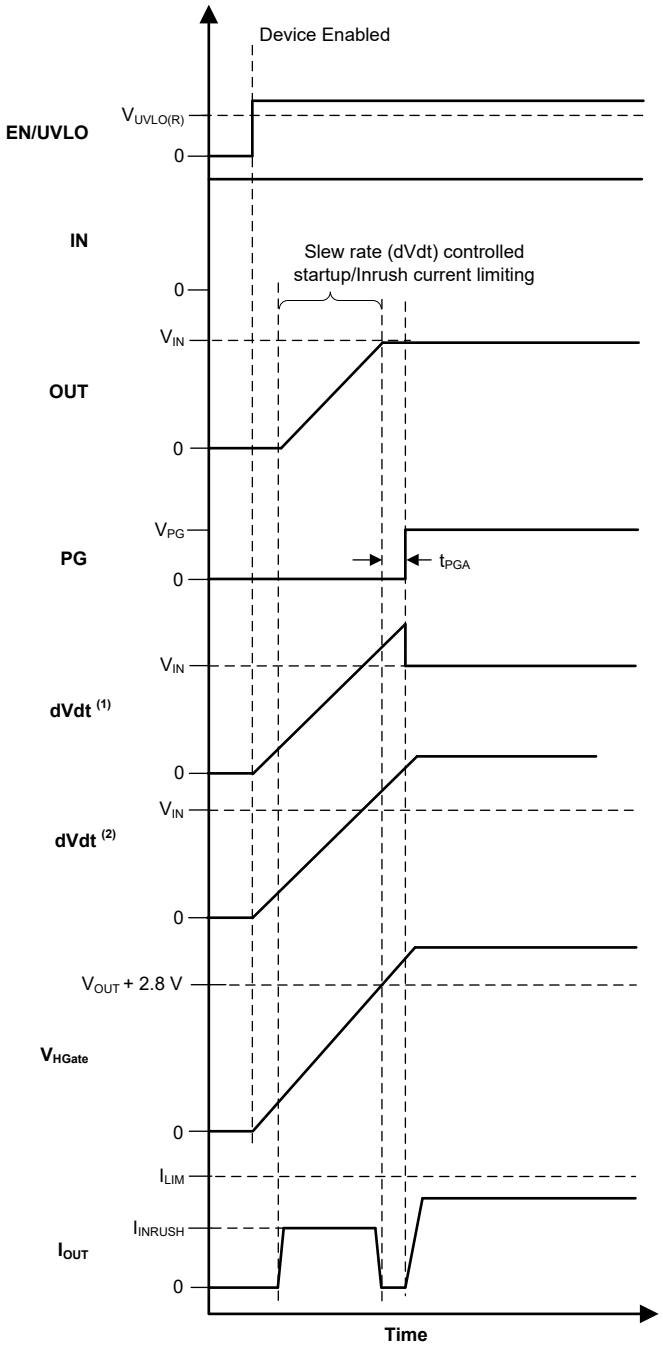
For TPS25981xA (auto-retry) variants, on expiry of the t_{RST}timer after a fault, the device restarts automatically and the $\overline{FLT}$ pin is de-asserted.

8.3.7 Power Good Indication (PG)

The TPS259814x provides an active high digital output (PG) which serves as a power good indication signal and is asserted high when the device is in steady-state and ready to deliver power. The PG is an open-drain pin and must be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the FET is turned on in a controlled manner. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time the FET is turned off. The PG de-assertion de-glitch time is t_{PGD}.



(1) Applicable only for TPS259814x variants
(2) Applicable only for TPS259813x variants

图 8-7. TPS25981xx PG Timing Diagram

表 8-3. TPS25981xx PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Overvoltage (OVLO)	Shutdown	L	t_{PGD}
Steady-state	NA	H	t_{PGA}
Transient overcurrent	NA	H	
Persistent overload	Circuit-breaker	L	t_{ITIMER} + t_{PGD}
Output short-circuit to GND	Fast-trip followed by current limit	L	t_{PGD}
ILM pin open	Shutdown	L	t_{ITIMER} + t_{PGD}
ILM pin shorted to GND	Shutdown	L	t_{PGD}
Overtemperature	Shutdown	L	t_{PGD}

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

8.3.8 Quick Output Discharge (QOD)

The TPS25981xx has an integrated output discharge function which can be helpful in quickly removing residual charge left on the large output capacitors and avoids bus floating at some undefined voltage. The internal QOD pulldown FET on the OUT pin is activated when the EN/UVLO is held low ($V_{EN} < V_{UVLO(F)}$). The output discharge function can result in excess power dissipation inside the device leading to increase in junction temperature. The output discharge is disabled if the junction temperature (T_J) crosses the thermal shutdown threshold (TSD) to avoid long term degradation of the part.

8.3.9 Reverse Current Blocking FET Driver

The TPS259813x variants provide an option to drive an external N-FET for implementing reverse current blocking function. The N-FET is connected in series with the eFuse in a common source configuration as shown in 图 8-8. The gate of the blocking FET is controlled by the DVDT pin of the eFuse. When the eFuse is turned ON and operating in steady-state, the DVDT pin is driven high which turns the external FET fully ON to provide a low impedance power path from input to output. When the eFuse turns OFF under any condition, the DVDT pin is pulled low and the blocking FET is turned OFF. This ensures there's no current path from the output to input in the OFF state.

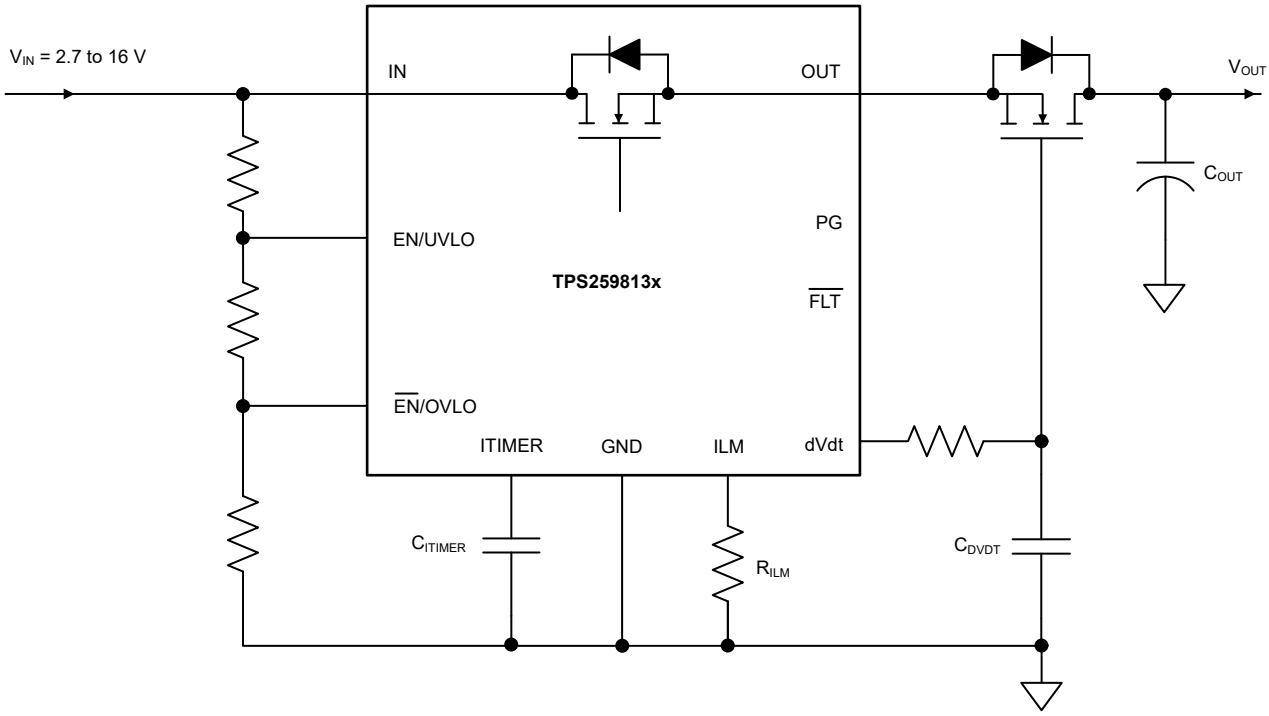


图 8-8. Reverse Current Blocking Using External FET

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25981xx is a 2.7-V to 16-V, 10-A eFuse that is typically used for power rail protection applications. The device operates from 2.7 V to 16 V with adjustable overvoltage and undervoltage protection. The device provides ability to control inrush current. The device can be used in a variety of systems such as server motherboard/add-on cards/NIC, optical modules, enterprise switches/routers, Industrial PC, UHDTV. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, *TPS25981xx Design Calculator*, is available in the web product folder.

9.1.1 Single Device, Self-Controlled

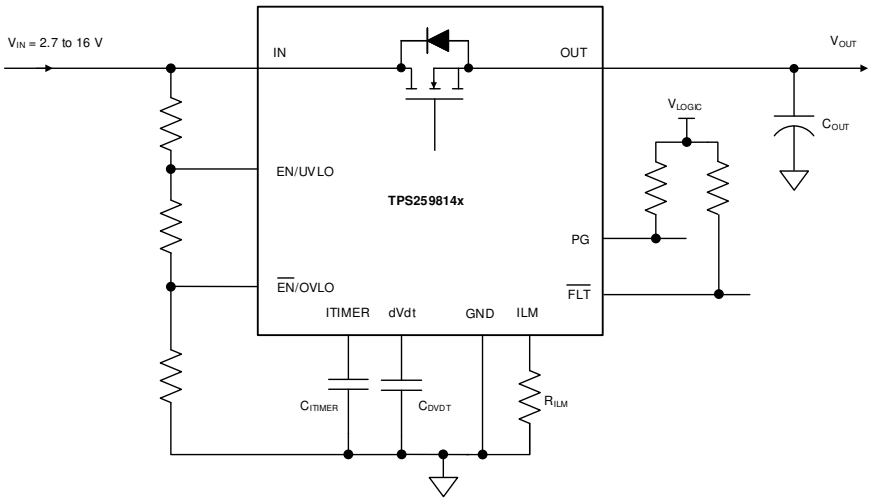


图 9-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

ILM pin can be connected to the MCU ADC input for current monitoring purpose.

备注

TI recommends to keep parasitic capacitance on the ILM pin below 50 pF to ensure stable operation.

9.1.2 Parallel Operation

Applications which need higher steady current can use two TPS25981xx devices connected in parallel as shown in 图 9-2 below. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low using the PG signal of the first device. After the inrush sequence is complete, the first device asserts its PG pin high and turns on the second device.

The second device asserts its PG signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady-state current.

Once in steady-state, both devices share current nearly equally. There can be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

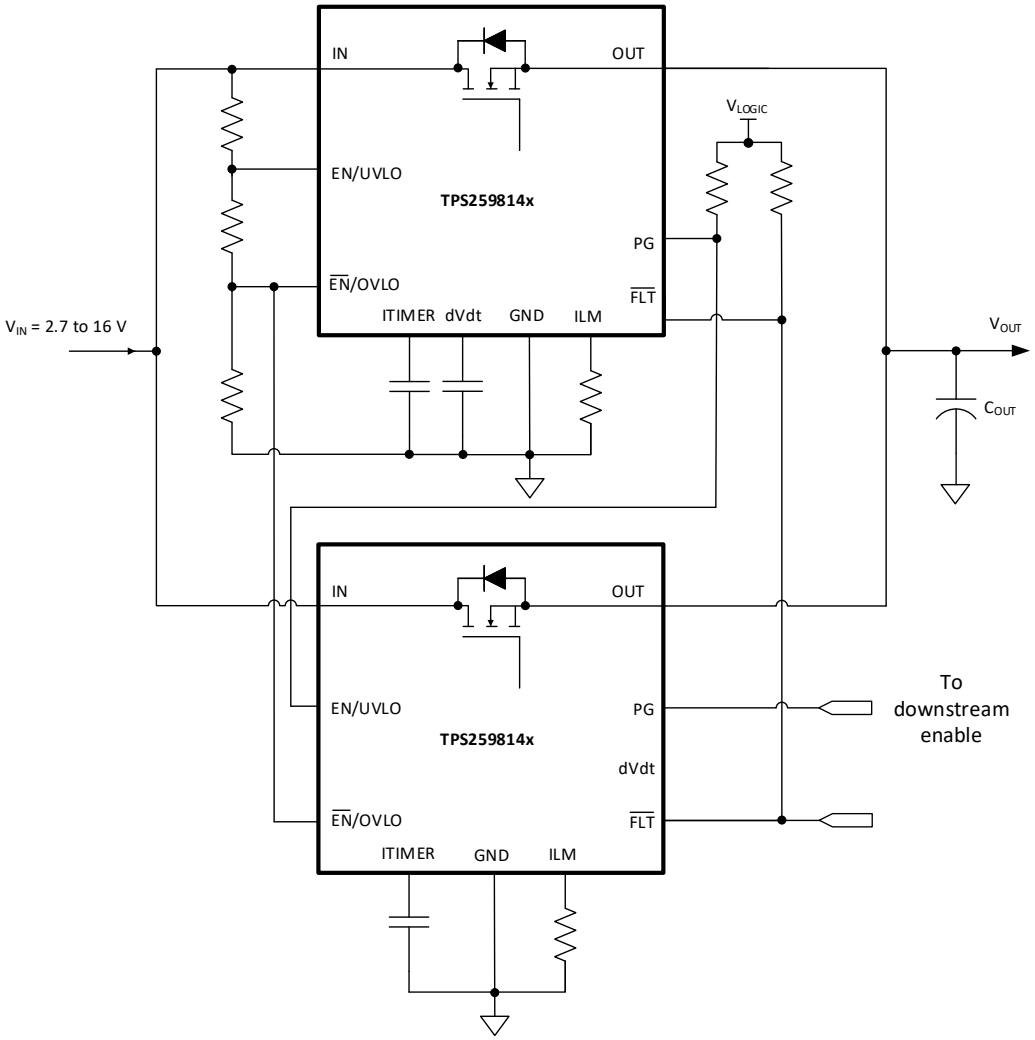


图 9-2. Two TPS259814x Devices Connected in Parallel for Higher Steady-State Current Capability

The waveforms below illustrate the behavior of the parallel configuration during start-up as well as during steady-state.

图 9-3. Parallel Devices Sequencing During Start-Up

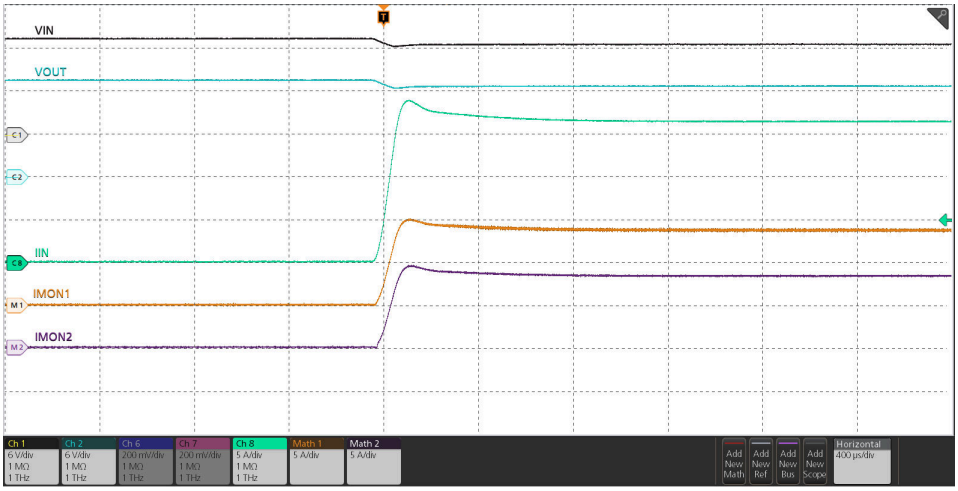


图 9-4. Parallel Devices Load Current During Steady-State

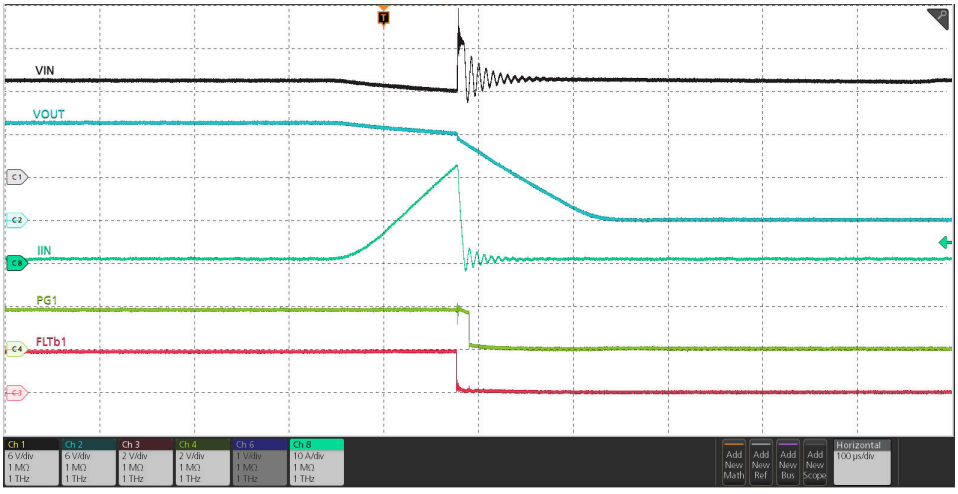


图 9-5. Parallel Devices Overcurrent Response

Another way to increase current handling capability of the eFuse in steady-state is by connecting a TPS25981xx eFuse in parallel with a TPS22811x load switch as shown in 图 9-6.

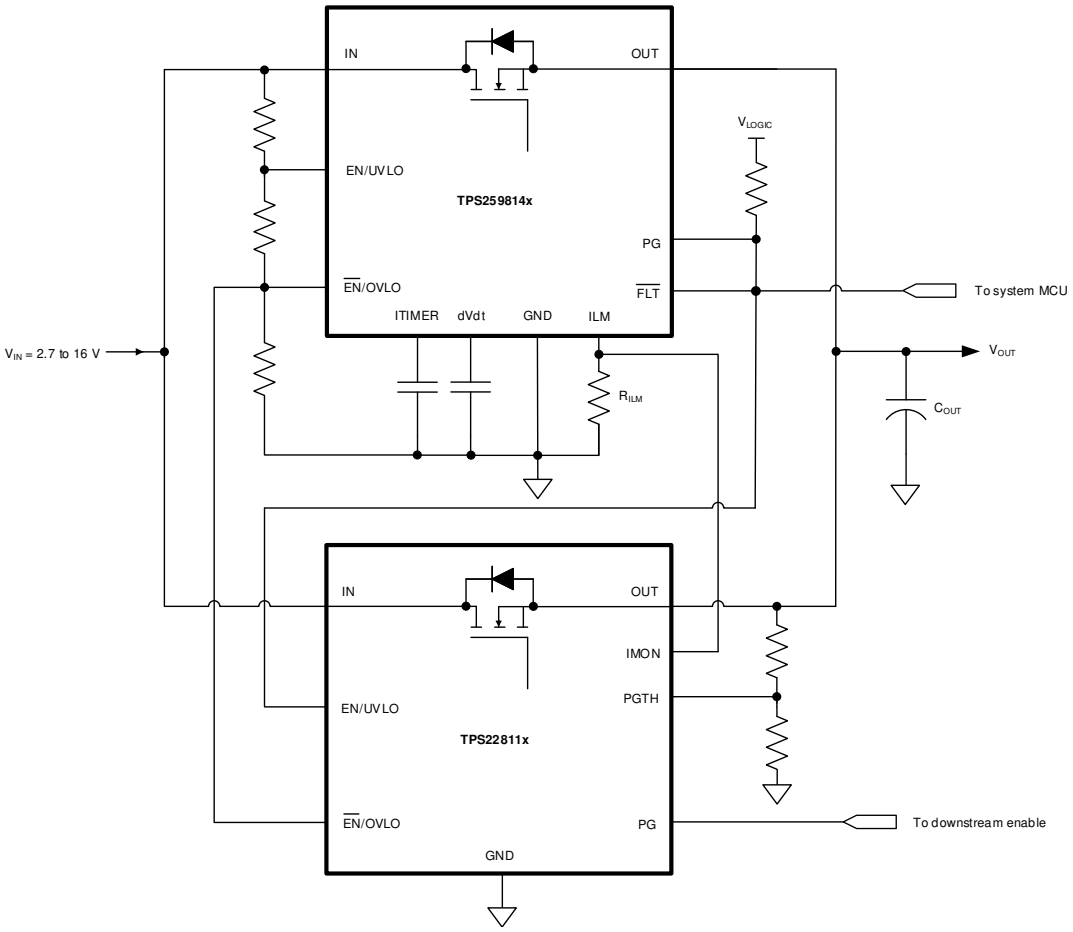


图 9-6. TPS259814x and TPS22811x Connected in Parallel for Higher Steady-State Current Capability

9.2 Typical Application

TPS259814x can be used for optical module power rail protection. Optical modules are commonly used in high-bandwidth data communication systems such as optical networking equipment, enterprise/data-center switches and routers. Several variants of optical modules are available in the market, which differ in the form-factor and the data speed support (Gbit/s). Of these, the popular variant double dense quad small form-factor pluggable (QSFP-DD) module supports speeds up to 400 Gbit/s. In addition to the system protection during hot-plug events, the other key requirement for optical module is the tight voltage regulation. The optical module uses 3.3-V supply and requires voltage regulation within ±5% for proper operation.

A typical power tree of such system is shown in 图 9-7. The optical line card consists of DC-DC converter, protection device (eFuse) and power supply filters. The DC-DC converter steps-down the 12 V to 3.3 V and maintains the 3.3-V rail within ±2 %. The power supply filtering network uses ‘LC’ components to reduce high frequency noise injection into the optical module. The DC resistance of the inductor ‘L’ causes voltage drop of around 1.5% which leaves us with a voltage drop budget of just 1.5% (3.3 V × 1.5% = 50 mV) across the protection device. Considering a maximum load current of 5.5 A per module, the maximum ON-resistance of the protection device must be less than 9 mΩ. TPS259814x eFuse offers a very low ON-resistance of 6 mΩ (typical), thereby meeting the target specification with additional margin to spare and simplifying the overall system design.

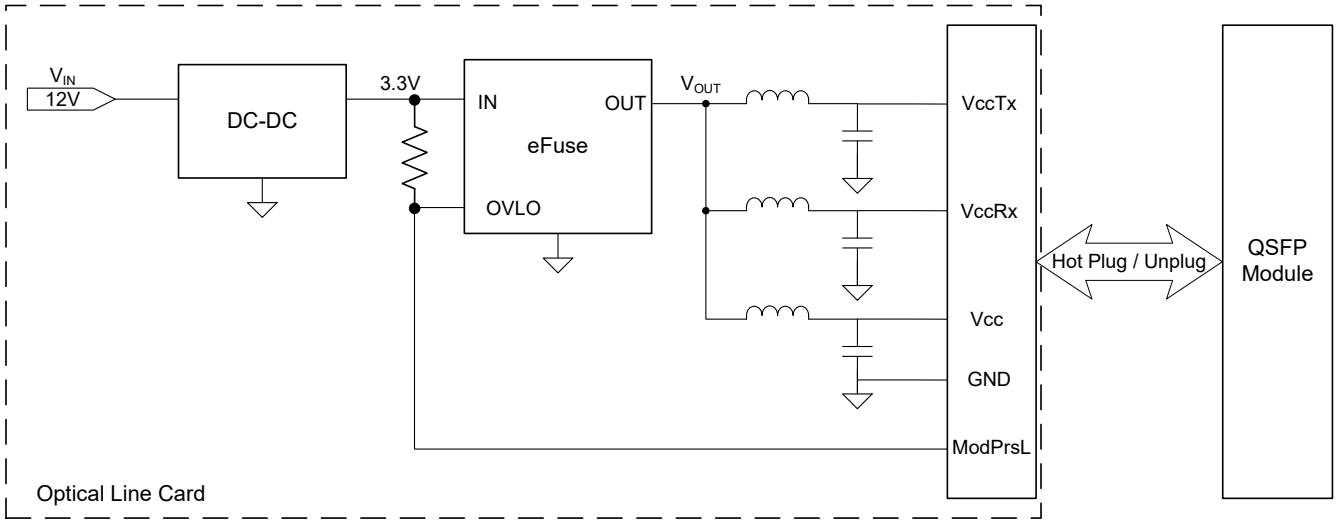
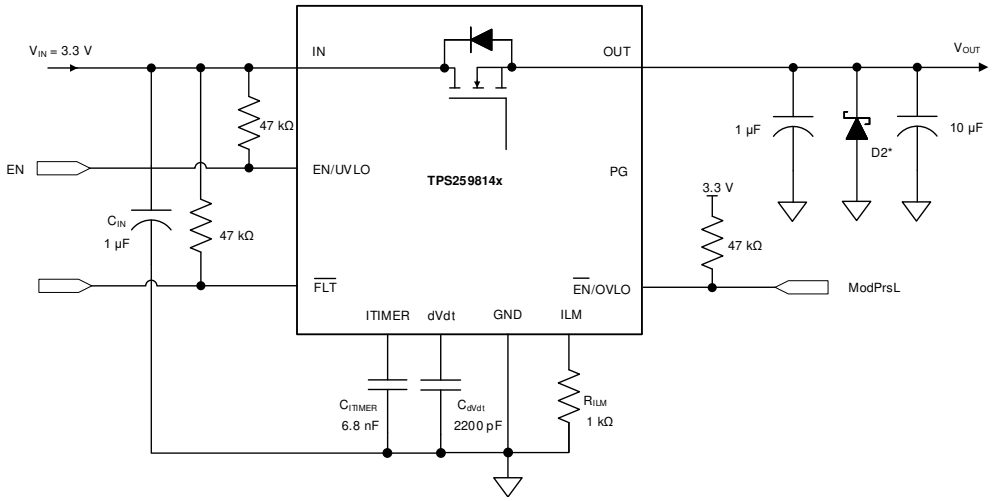


图 9-7. Power Tree Block Diagram of a Typical Optical Line Card

As shown in *图 9-7*, ModPrsL signal acts as a handshake signal between the line card and the optical module. ModPrsL is always pulled to ground inside the module. When the module is hot-plugged into the host "Optical Line Card" connector, the ModPrsL signal pulls down the OVLO pin and enables the TPS259814x eFuse to power the module. This action ensures that power is applied on the port only when a module is plugged in and disconnected when there is no module present.



* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

图 9-8. Optical Module Port Protection

9.2.1 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
Input supply voltage (V_{IN})	3.3 V
Maximum voltage drop in the path	± 5%
Maximum continuous current	5.5 A
Load transient blanking interval (t_{ITIMER})	5 ms

表 9-1. Design Parameters (continued)

PARAMETER	VALUE
Output capacitance (C_{OUT})	10 µF
Output rise time (t_R)	2.2 ms
Overcurrent threshold (I_{LIM})	6.5 A
Fault response	Auto-retry

9.2.2 Detailed Design Procedure

9.2.2.1 Device Selection

Because the application requires retry response after a fault, the TPS259814A variant is selected after referring to the *Device Comparison Table*.

9.2.2.2 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR\left(\frac{V}{ms}\right) = \frac{V_{IN}\,(V)}{t_R\,(ms)} = \frac{3.3\,V}{2.2\,ms} = 1.5\,\frac{V}{ms} \tag{9}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} = \frac{3300}{1.5\,\frac{V}{ms}} = 2200\,pF \tag{10}$$

Choose the nearest standard capacitor value as 2200 pF.

For this slew rate, the inrush current can be calculated as:

$$I_{INRUSH}\,(mA) = C_{OUT}\,(\mu F) \times SR\left(\frac{V}{ms}\right) = 10\,\mu F \times 1.5\,\frac{V}{ms} = 15\,mA \tag{11}$$

The average power dissipation inside the part during inrush can be calculated as:

$$PD_{INRUSH}\,(mW) = 0.5 \times V_{IN}\,(V) \times I_{INRUSH}\,(mA) = 0.5 \times 3.3\,V \times 15\,mA = 25\,mW \tag{12}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. 图 9-9 shows the thermal shutdown limit, for 0.025 W of power, the shutdown time is more than 10 s which is very large as compared to t_R = 2.2 ms. Therefore, it is safe to use 2.2 ms as the start-up time for this application.

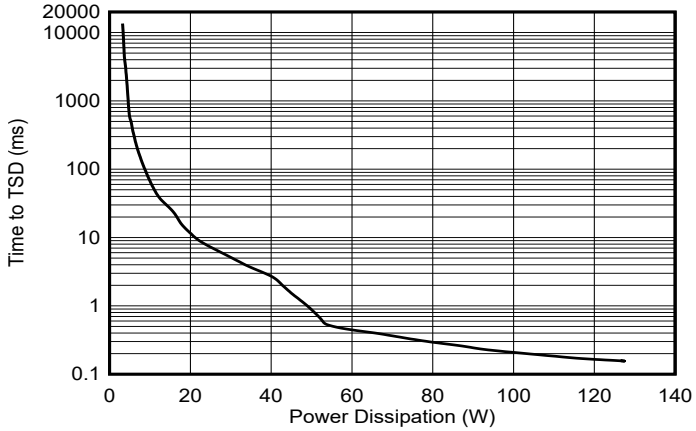


图 9-9. Thermal Shutdown Plot During Inrush

9.2.2.3 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection (circuit-breaker) threshold can be set using the R_{ILM} resistor whose value can be calculated as:

$$R_{ILM}\,(\Omega) = \frac{6585}{I_{LIM}\,(A)} = \frac{6585}{6.5\,A} = 1013\ \Omega \tag{13}$$

Choose the nearest 1% standard resistor value as 1 kΩ.

9.2.2.4 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms) \times I_{ITIMER}\,(\mu A)}{\Delta V_{ITIMER}\,(V)} = \frac{5\,ms \times 2\,\mu A}{1.51\,V} = 6.62\,nF \tag{14}$$

Choose the nearest standard capacitor value as 6.8 nF.

9.2.2.5 Voltage Drop

表 9-2 shows the power path voltage drop (%) due to the eFuse in QSFP modules of different power classes.

表 9-2. Voltage Drop Across TPS25981 on QSFP Module Power Rail

POWER CLASS	MAXIMUM POWER CONSUMPTION PER MODULE (W)	MAXIMUM LOAD CURRENT (A)	TYPICAL VOLTAGE DROP (%)
1	1.5	0.454	0.082
2	3.5	1.06	0.192
3	7	2.12	0.385
4	8	2.42	0.440
5	10	3.03	0.551
6	12	3.63	0.660
7	14	4.24	0.771
8	18	5.45	0.991

9.2.3 Application Curves

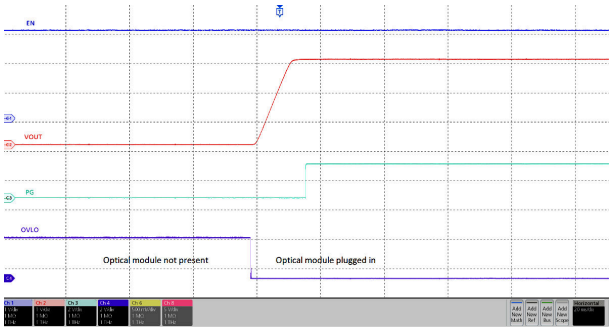


图 9-10. Output Voltage Profile When Optical Module is Inserted

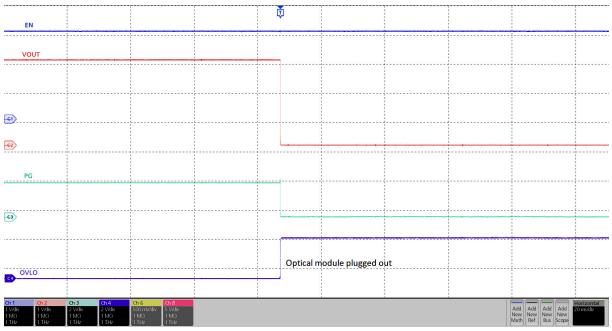


图 9-11. Output Voltage Profile When Optical Module is Plugged Out

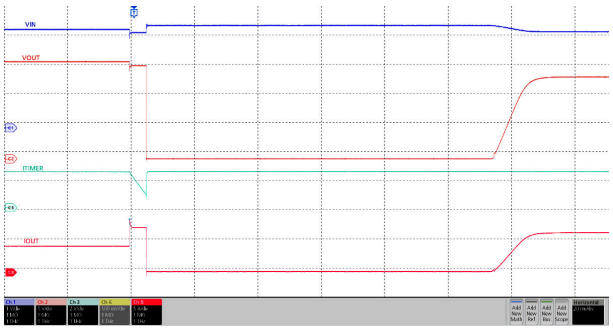


图 9-12. Circuit-Breaker with Transient Overcurrent Blanking Interval of 5 ms; Device Restarts in Current Limit Mode

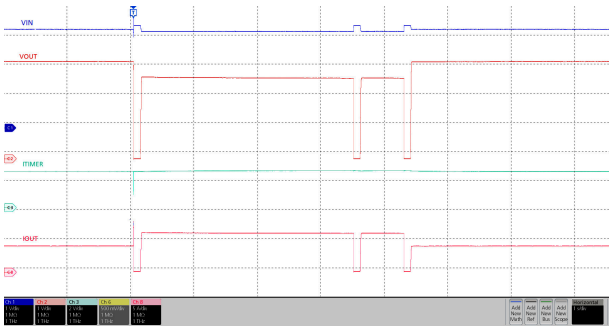


图 9-13. Overload Response and Recovery

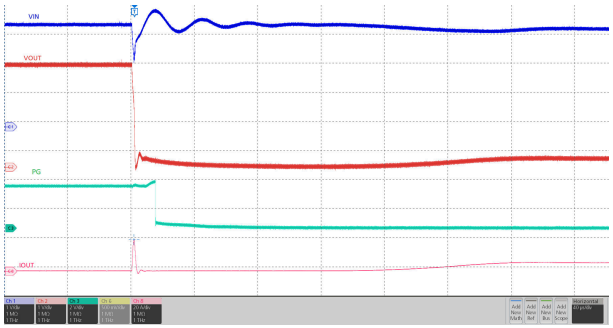


图 9-14. Output Hard Short Circuit While ON

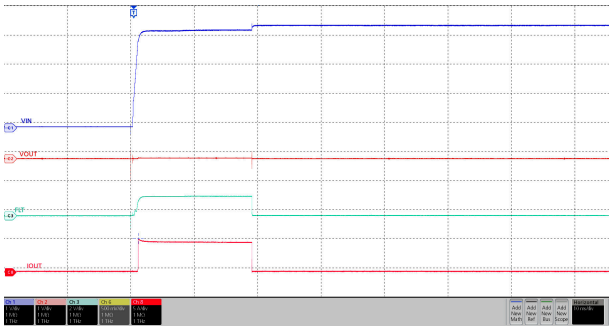


图 9-15. Power Up with Short Circuit on Output

10 Power Supply Recommendations

The TPS25981xx devices are designed for a supply voltage range of 2.7 V ⩽ V_{IN} ⩽ 16 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  Use 方程式 15 to estimate the approximate value of input capacitance:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (15)$$

  where

  - V_{IN} is the nominal supply voltage.
  - I_{LOAD} is the load current.
  - L_{IN} equals the effective inductance seen looking into the source.
  - C_{IN} is the capacitance present at the input.
- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

图 10-1 shows the circuit implementation with optional protection components.

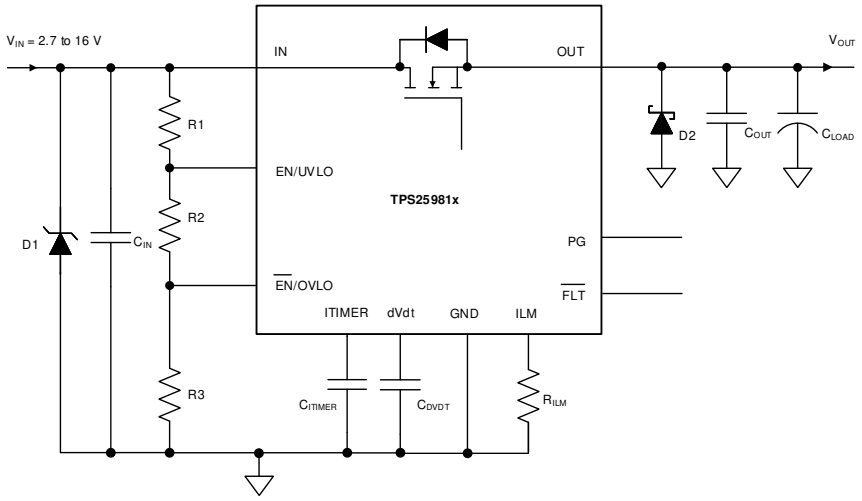


图 10-1. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

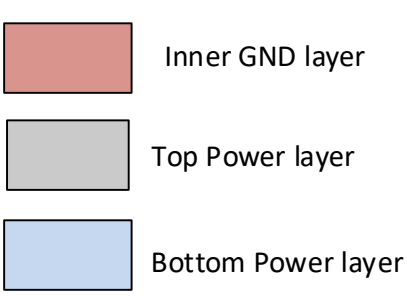
The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

11 Layout

11.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - C_{ITIMER}
  - Resistors for the EN/UVLO, $\overline{EN}$/OVLO pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit , overcurrent blanking interval and soft start timing. TI recommends to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation. These traces must not have any coupling to switching signals on the board.
- Because the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads. TI also recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode, bypass-capacitor connection, the OUT pin, and the GND terminal of the IC.

11.2 Layout Example



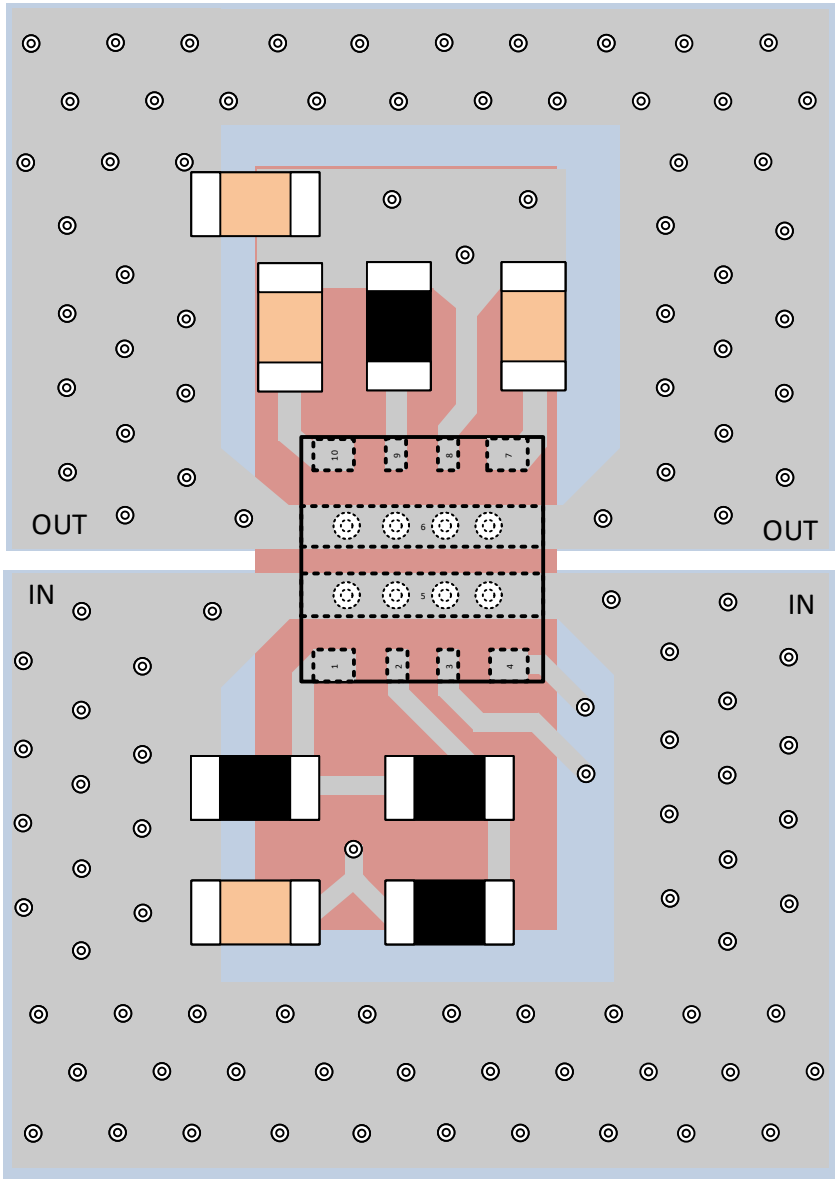


图 11-1. Layout Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS25981EVM eFuse Evaluation Board*
- Texas Instruments, *TPS25981xx Design Calculator*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

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12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259813ARPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	34NH	Samples
TPS259813LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	34OH	Samples
TPS259814ARPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2KWH	Samples
TPS259814LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2KXH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

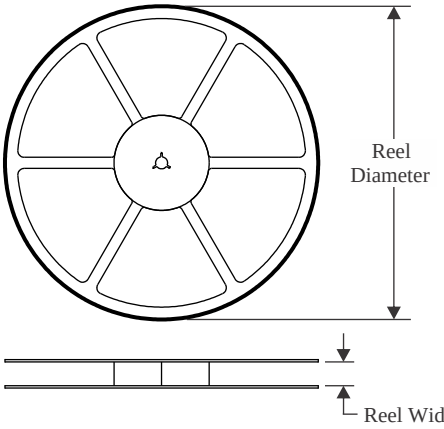
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

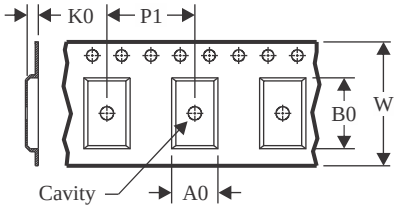
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

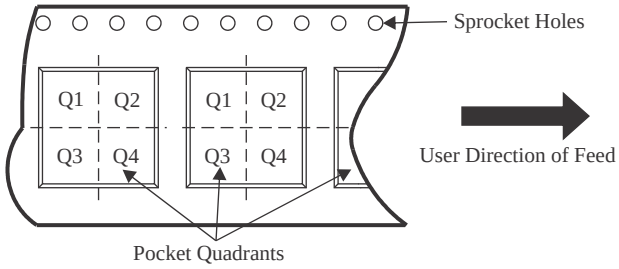


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

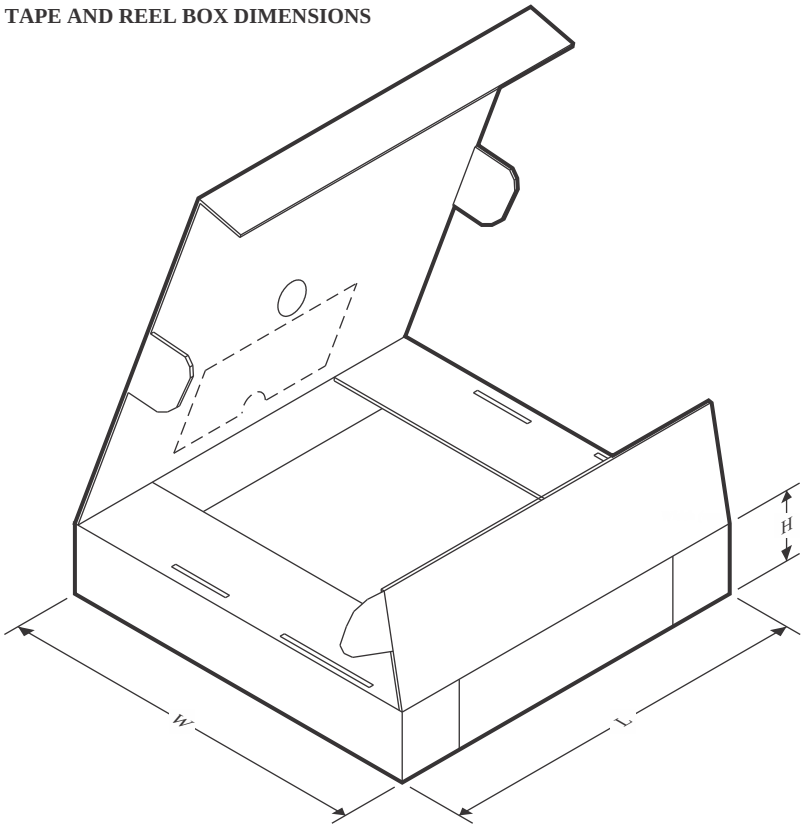
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259813ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259813LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259814ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259814LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

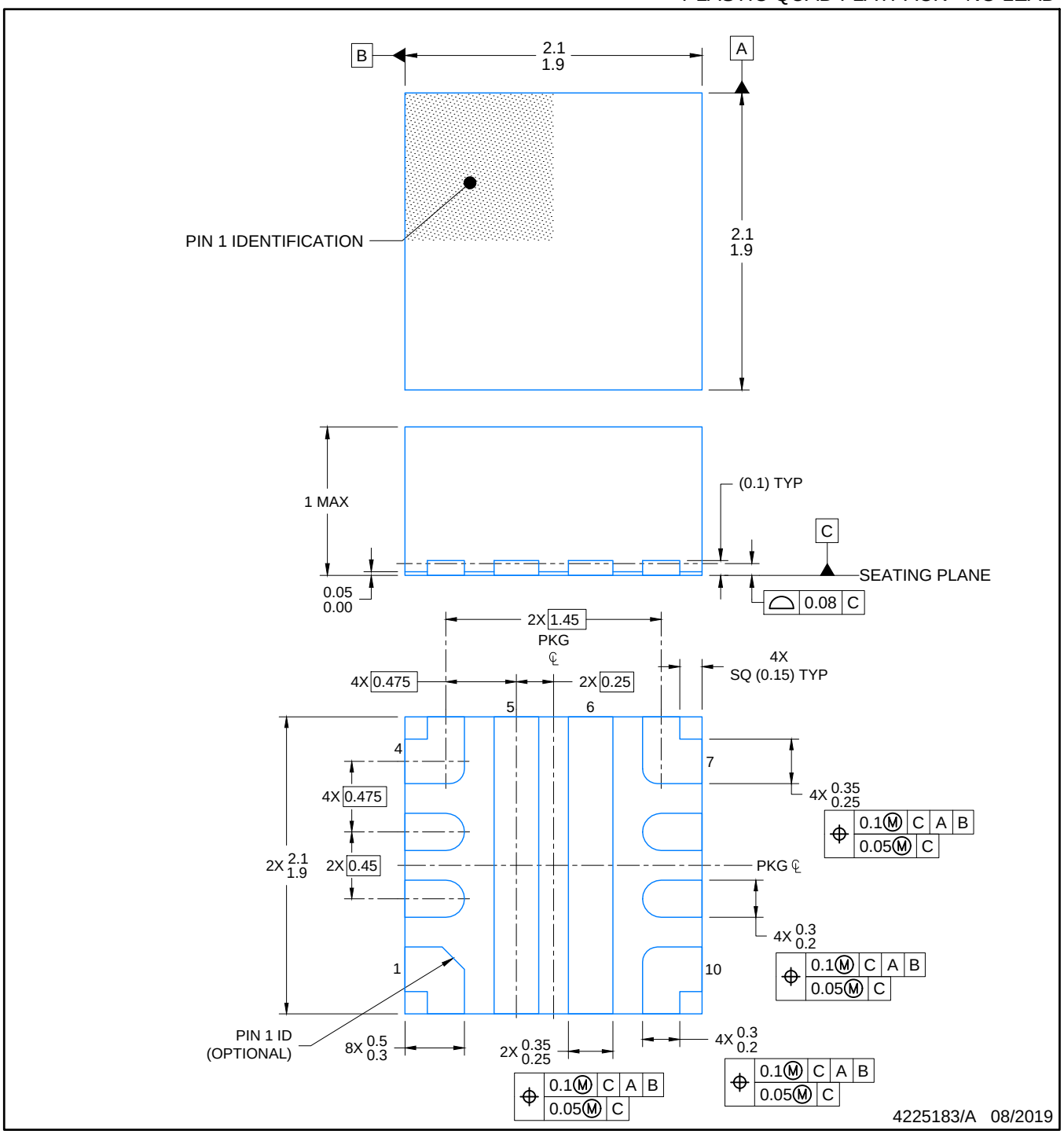
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259813ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259813LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259814ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259814LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPW0010A

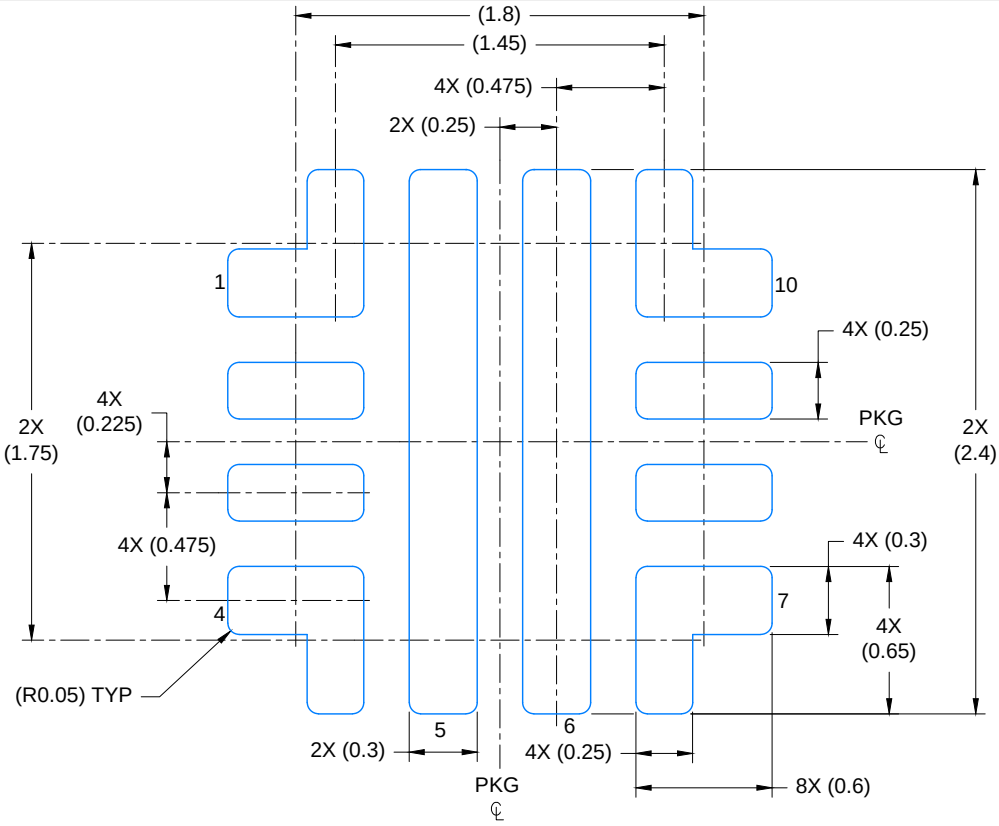
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



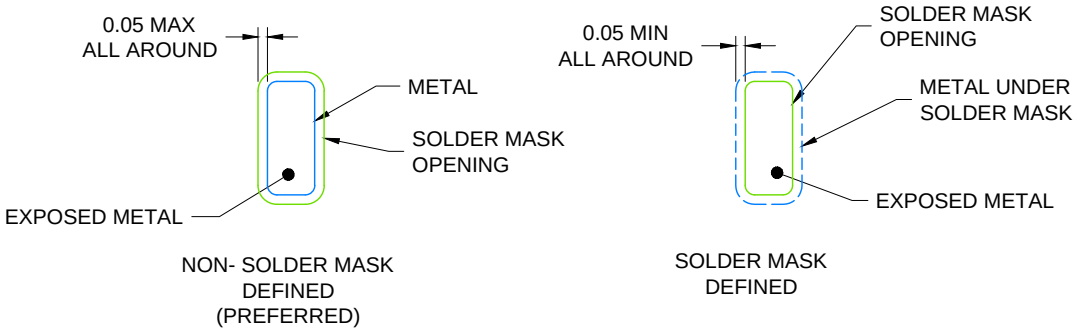
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



SOLDER MASK DETAILS

NOT TO SCALE

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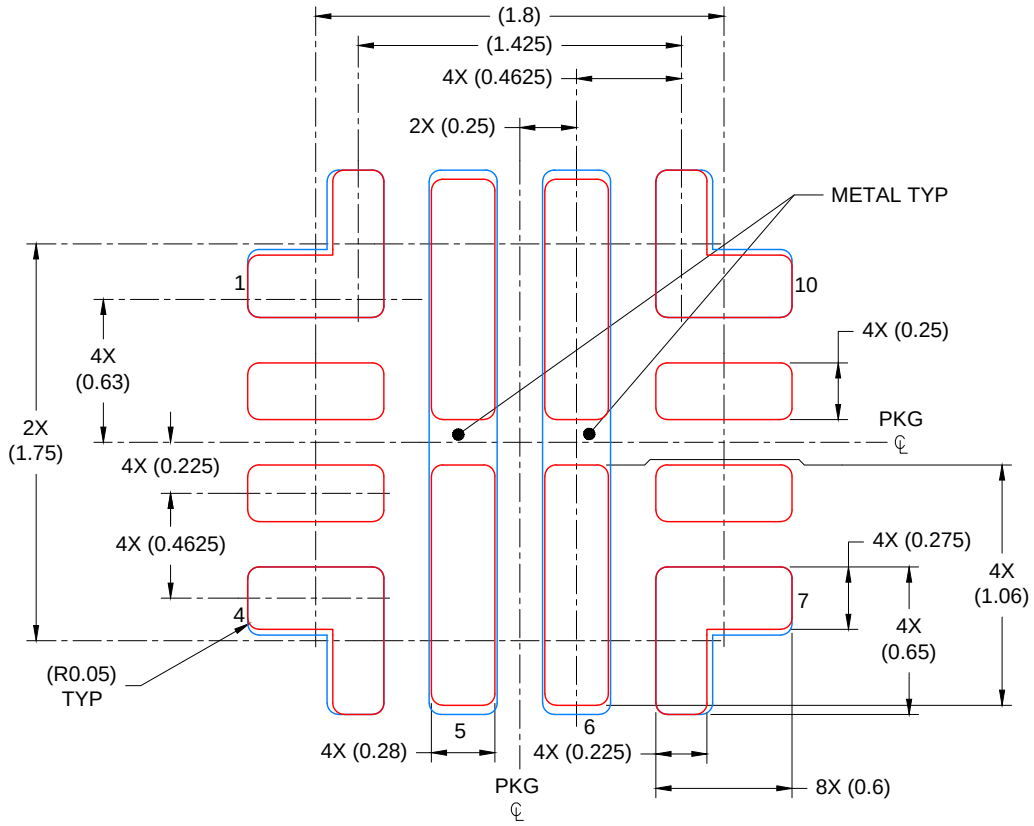
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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