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TPS4021x 4.5-V to 52-V Input Current Mode Boost Controller

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- For boost, flyback, SEPIC, LED drive apps
- Wide input operating voltage: 4.5 V to 52 V
- Adjustable oscillator frequency
- Fixed frequency current mode control
- Internal slope compensation
- Integrated low-side driver
- Programmable closed-loop soft start
- Overcurrent protection
- External synchronization capable
- Reference 700 mV (TPS40210), 260 mV (TPS40211)
- Low current disable function
- Create a custom design using the TPS4021x with the WEBENCH Power Designer

2 Applications

- LED lighting
- Industrial control systems
- Battery-powered systems

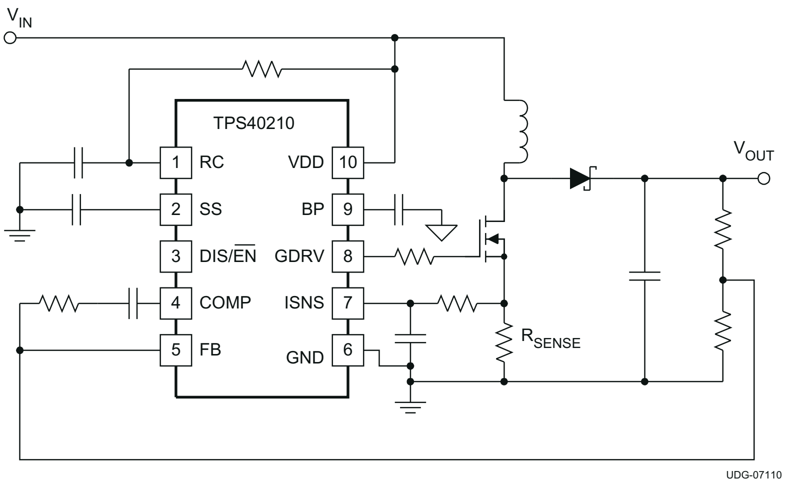
3 Description

The TPS40210 and TPS40211 are wide-input voltage (4.5 V to 52 V), nonsynchronous boost controllers. They are suitable for topologies which require a grounded source N-channel FET including boost, flyback, SEPIC, and various LED Driver applications. The device features include programmable soft start, overcurrent protection with automatic retry, and programmable oscillator frequency. Current mode control provides improved transient response and simplified loop compensation. The main difference between the two parts is the reference voltage to which the error amplifier regulates the FB pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40210	HVSSOP (10)	3.05 mm x 4.98 mm
TPS40211	VSON (10)	3.10 mm x 3.10 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2015) to Revision G (June 2020)	Page
• Added functional safety bullet to the *Section 1*	1

Changes from Revision E (October 2011) to Revision F (December 2014)	Page
• Added Updated Land Pattern	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision D (April 2010) to Revision E (October 2011)	Page
• Changed the Revision date from D, April 2010 to E, October 2011	1
• Added Q1 and Q3 to Figure 36 by illustrator	34

Changes from Revision C (October 2008) to Revision D (April 2010)	Page
• Changed C_{ISNS} to C_{IFLT}	19
• Changed C_{ISNS} to C_{IFLT}	20
• Changed equations 22 and 23	21
• Changed corrected equation 25	21
• Added "R1 is the high side feedback resistor in Ω" and " f_L is the desired loop crossover frequency, in Hz"	21
• Changed paragraph with new input	21
• Changed capacitor value from µF to F	21
• Changed 0.2 with 0.1 in MIN col in Design Example Specifications table	26
• Deleted text from Peak efficiency row	26
• Changed 10 V with 8 V in T_{OP} conditions column	26
• Changed 42.8% to 42.9% in eq 32	26
• Added (V_{FD}) and changed approximate duty cycle from 42.8% to 42.9%	26
• Changed equations 32, 34, 35, 36, 37, 38 and 39	27
• Changed equations 47, 48, 49, 50, 51 and 53	28
• Changed equations 58, 60, 61, 62	30

5 Pin Configuration and Functions

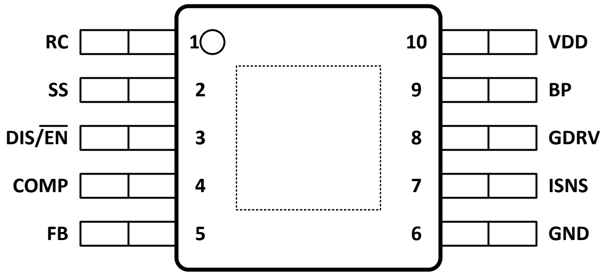


Figure 5-1. DGQ 10-Pin Top View

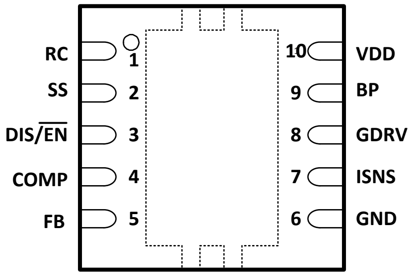


Figure 5-2. DRC 10-Pin Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BP	9	O	Regulator output pin. Connect a 1.0-µF bypass capacitor from this pin to GND.
COMP	4	O	Error amplifier output. Connect control loop compensation network between COMP pin and FB pin.
DIS/ $\overline{EN}$	3	I	Disable pin. Pulling this pin high places the part into a shutdown mode. Shutdown mode is characterized by a very low quiescent current. While in shutdown mode, the functionality of all blocks is disabled and the BP regulator is shut down. This pin has an internal 1 MΩ pulldown resistor to GND. Leaving this pin unconnected enables the device.
FB	5	I	Error amplifier inverting input. Connect a voltage divider from the output to this pin to set output voltage. Compensation network is connected between this pin and COMP.
GDRV	8	O	Connect the gate of the power N channel MOSFET to this pin.
GND	6	-	Device ground.
ISNS	7	I	Current sense pin. Connect an external current sensing resistor between this pin and GND. The voltage on this pin is used to provide current feedback in the control loop and detect an overcurrent condition. An overcurrent condition is declared when ISNS pin voltage exceeds the overcurrent threshold voltage, 150 mV typical.
RC	1	I	Switching frequency setting pin. Connect a resistor from RC pin to VDD of the IC power supply and a capacitor from RC to GND.
SS	2	I	Soft-start time programming pin. Connect capacitor from SS pin to GND to program converter soft-start time. This pin also functions as a timeout timer when the power supply is in an overcurrent condition.
VDD	10	I	System input voltage. Connect a local bypass capacitor from this pin to GND. Depending on the amount of required slope compensation, this pin can be connected to the converter output. See *Section 8.1* section for additional details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

			MIN	MAX	UNIT
	Input voltage	VDD	–0.3	52	V
		RC, SS, FB, DIS/ $\overline{\text{EN}}$	–0.3	10	
		ISNS	–0.3	8	
	Output voltage	COMP, BP, GDRV	–0.3	9	
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Input voltage	4.5	52	V
T_J	Operating Junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS40210	TPS40211	UNIT
		HVSSOP	VSON	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.2	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.5	74.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	22.2	
Ψ_{JT}	Junction-to-top characterization parameter	2.4	2.9	
Ψ_{JB}	Junction-to-board characterization parameter	40.7	22.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.6	8.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{DD}= 12V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE							
V_{FB}	Feedback voltage range	TPS40210	COMP = FB, 4.5 ≤ V_{DD} ≤ 52 V, T_J = 25°C	693	700	707	mV
		TPS40211	COMP=FB, 4.5 ≤ V_{DD} ≤ 52 V, T_J = 25°C	254	260	266	
		TPS40210	COMP = FB, 4.5 ≤ V_{DD} ≤ 52 V, -40°C ≤ T_J ≤ 125°C	686	700	714	
		TPS40211	COMP = FB, 4.5 ≤ V_{DD} ≤ 52 V, -40°C ≤ T_J ≤ 125°C	250	260	270	
INPUT SUPPLY							
V_{DD}	Input voltage range			4.5		52	V
I_{DD}	Operating current		4.5 ≤ V_{DD} ≤ 52 V, no switching, V_{DIS} < 0.8		1.5	2.5	mA
			2.5 ≤ V_{DIS} ≤ 7 V		10	20	µA
			V_{DD} < $V_{UVLO(on)}$, V_{DIS} < 0.8			530	µA
UNDERVOLTAGE LOCKOUT							
$V_{UVLO(on)}$	Turn on threshold voltage			4.00	4.25	4.50	V
$V_{UVLO(hyst)}$	UVLO hysteresis			140	195	240	mV
OSCILLATOR							
f_{OSC}	Oscillator frequency range(1)			35		1000	kHz
	Oscillator frequency		R_{RC} = 182 kΩ, C_{RC} = 330 pF	260	300	340	
	Frequency line regulation		4.5 ≤ V_{DD} ≤ 52 V	-20%		7%	
V_{SLP}	Slope compensation ramp			520	620	720	mV
PWM							
$t_{ON(min)}$	Minimum pulse width		V_{DD} = 12 V(1)		275	400	ns
			V_{DD} = 30 V		90	200	
$t_{OFF(min)}$	Minimum off time				170	200	
V_{VLY}	Valley voltage				1.2		V
SOFT-START							
$V_{SS(ofst)}$	Offset voltage from SS pin to error amplifier input				700		mV
$R_{SS(chg)}$	Soft-start charge resistance			320	430	600	kΩ
$R_{SS(dchg)}$	Soft-start discharge resistance			840	1200	1600	
ERROR AMPLIFIER							
GBWP	Unity gain bandwidth product(1)			1.5	3.0		MHz
A_{OL}	Open loop gain(1)			60	80		dB
$I_{IB(FB)}$	Input bias current (current out of FB pin)				100	300	nA
$I_{COMP(src)}$	Output source current		V_{FB} = 0.6 V, V_{COMP} = 1 V	100	250		µA
$I_{COMP(snk)}$	Output sink current		V_{FB} = 1.2 V, V_{COMP} = 1 V	1.2	2.5		mA
OVERCURRENT PROTECTION							
$V_{ISNS(oc)}$	Overcurrent detection threshold (at ISNS pin)		4.5 ≤ V_{DD} < 52 V, -40°C ≤ T_J ≤ 125°C	120	150	180	mV
D_{OC}	Overcurrent duty cycle(1)					2%	
$V_{SS(rst)}$	Overcurrent reset threshold voltage (at SS pin)			100	150	350	mV
T_{BLNK}	Leading edge blanking(1)				75		ns
CURRENT SENSE AMPLIFIER							
A_{CS}	Current sense amplifier gain			4..2	5.6	7.2	V/V

6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{DD}= 12V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{B(ISNS)}$	Input bias current			1	3	μA
DRIVER						
$I_{GDRV(src)}$	Gate driver source current	V_{GDRV} = 4 V, T_J = 25°C	375	400		mA
$I_{GDRV(snk)}$	Gate driver sink current	V_{GDRV} = 4 V, T_J = 25°C	330	400		
LINEAR REGULATOR						
V_{BP}	Bypass voltage output	0 mA < I_{BP} < 15 mA	7	8	9	V
DISABLE/ENABLE						
$V_{DIS(en)}$	Turn-on voltage		0.7		1.3	V
$V_{DIS(hys)}$	Hysteresis voltage		25	130	220	mV
R_{DIS}	DIS pin pulldown resistance		0.7	1.1	1.5	MΩ

(1) Ensured by design. Not production tested.

6.6 Typical Characteristics

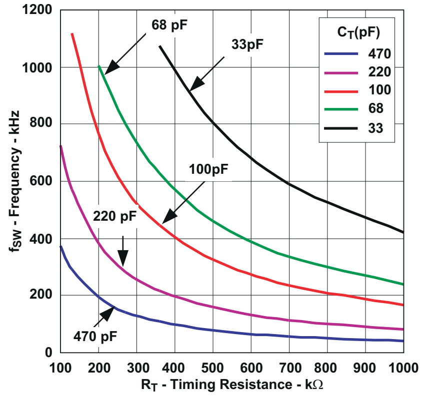


Figure 6-1. Frequency vs Timing Resistance

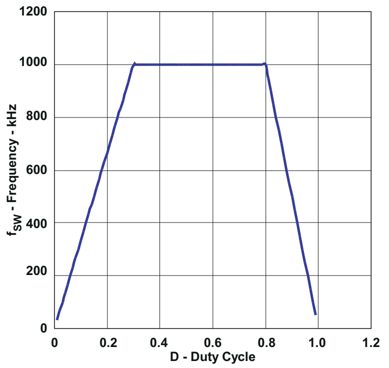


Figure 6-2. Switching Frequency vs Duty Cycle

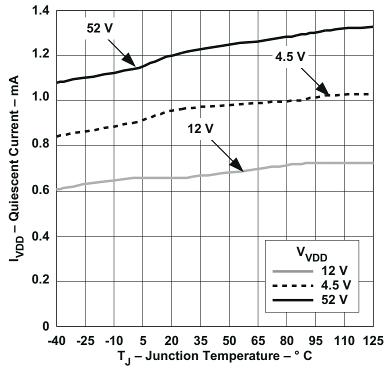


Figure 6-3. Quiescent Current vs Junction Temperature

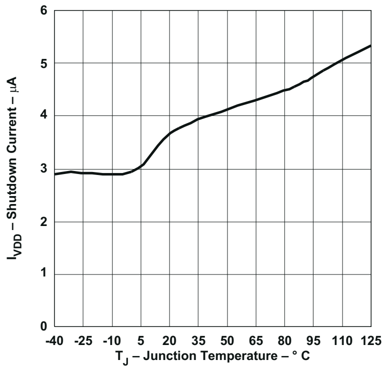


Figure 6-4. Shutdown Current vs Junction Temperature

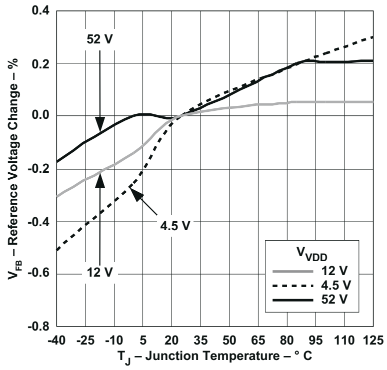


Figure 6-5. Reference Voltage Change vs Junction Temperature

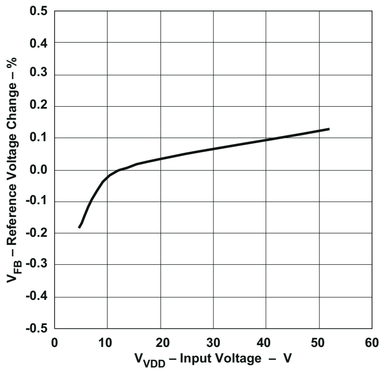


Figure 6-6. Reference Voltage Change vs Input Voltage

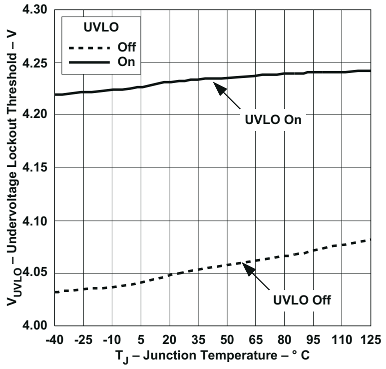


Figure 6-7. Undervoltage Lockout Threshold vs Junction Temperature

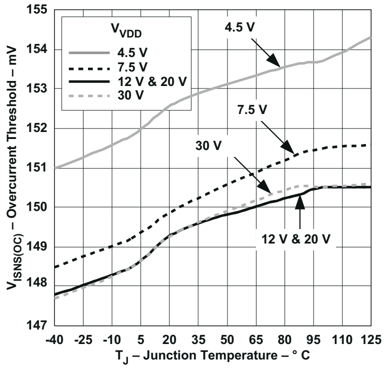


Figure 6-8. Overcurrent Threshold vs Junction Temperature

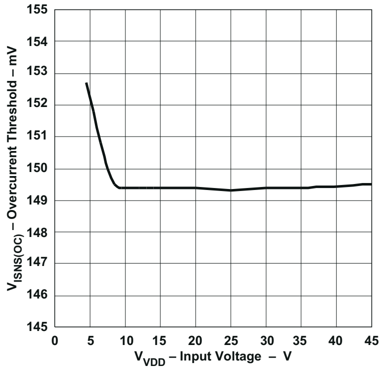


Figure 6-9. Overcurrent Threshold vs Input Voltage

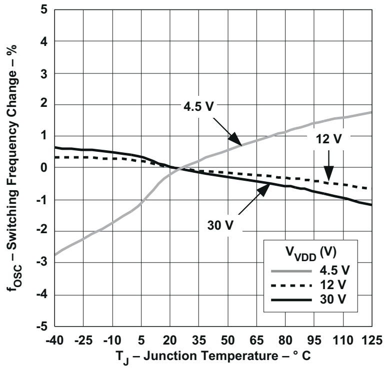


Figure 6-10. Switching Frequency Change vs Junction Temperature

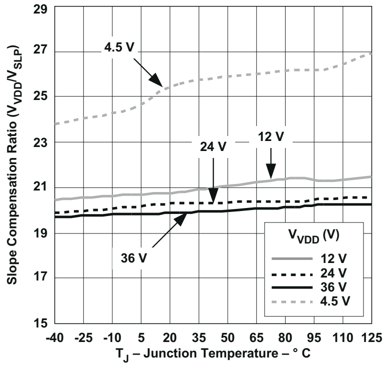


Figure 6-11. Oscillator Amplitude vs Junction Temperature

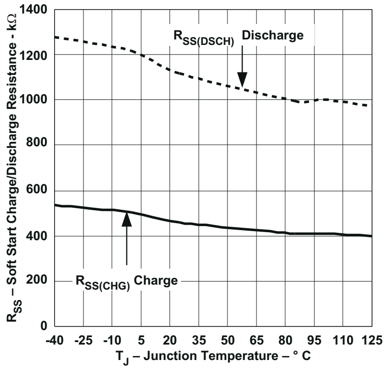


Figure 6-12. Soft Start Charge/Discharge Resistance vs Junction Temperature

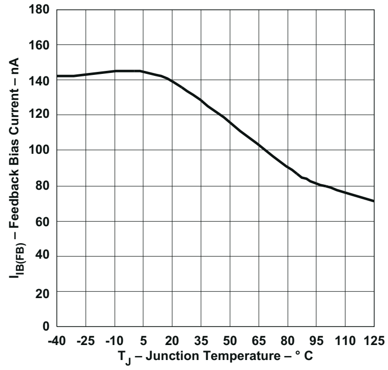


Figure 6-13. FB Bias Current vs Junction Temperature

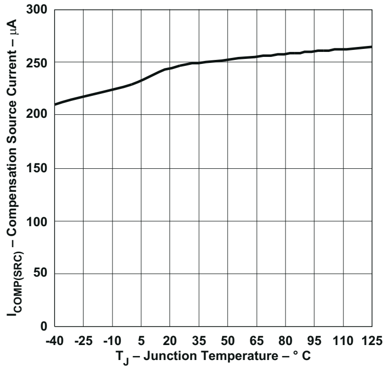


Figure 6-14. Compensation Source Current vs Junction Temperature

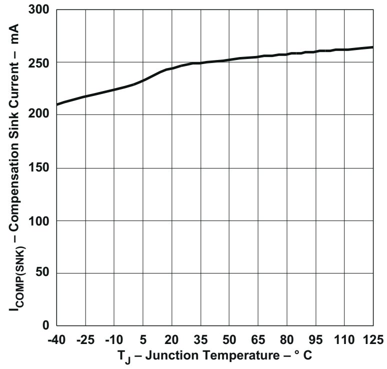


Figure 6-15. Compensation Sink Current vs Junction Temperature

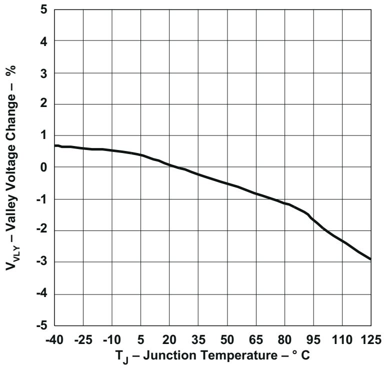


Figure 6-16. Valley Voltage Change vs Junction Temperature

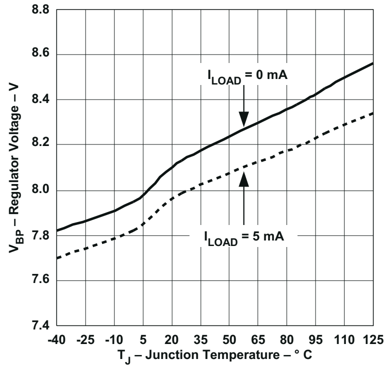


Figure 6-17. Regulator Voltage vs Junction Temperature

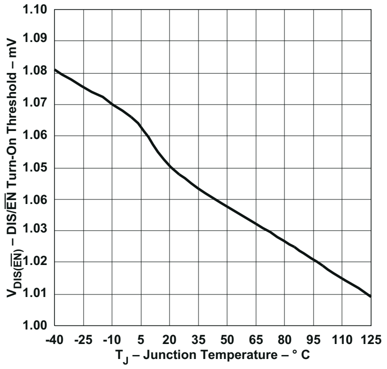


Figure 6-18. DIS/EN Turnon Threshold vs Junction Temperature

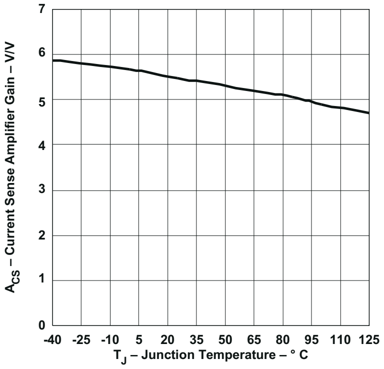


Figure 6-19. Current Sense Amplifier Gain vs Junction Temperature

7 Detailed Description

7.1 Overview

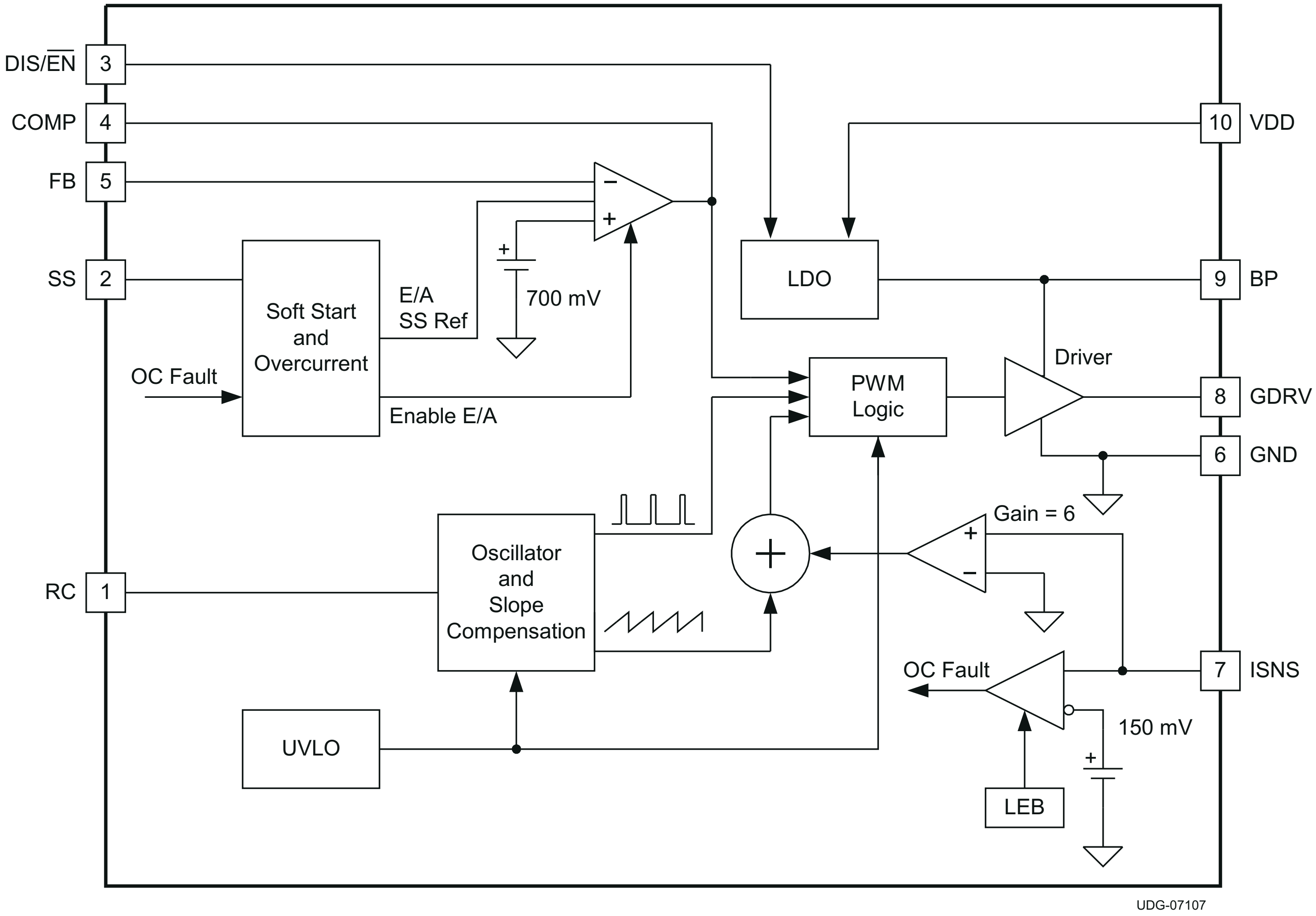
The TPS4021x is a peak current-mode control low-side controller with a built in 400-mA gate driver designed to drive n- channel MOSFETs at a fixed frequency. The frequency is adjustable from 35 kHz to 1000 kHz. Small size combined with complete functionality makes the part both versatile and easy to use.

The controller uses a low-value current-sensing resistor in series with the power MOSFET's source connection to detect switching current. When the voltage drop across this resistor exceeds 150 mV, the part enters an hiccup fault mode with a time period set by the external soft-start capacitor.

The TPS40210 uses voltage feedback to an error amplifier that is biased by a precision 700-mV reference. The TPS40211 has a lower 260-mV reference for higher efficiency in LED drive applications. Internal slope compensation eliminates the characteristic sub-harmonic instability of peak current mode control with duty cycles of 50% or greater.

The TPS4021x also incorporates a soft-start feature where the output follows a slowly rising soft-start voltage, preventing output-voltage overshoot. The DIS/ $\overline{\text{EN}}$ disables the TPS40210 putting it in a low quiescent current shutdown mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start

The soft-start feature of the TPS40210 and TPS40211 is a closed-loop soft start, meaning that the output voltage follows a linear ramp that is proportional to the ramp generated at the SS pin. This ramp is generated by an internal resistor connected from the BP pin to the SS pin and an external capacitor connected from the SS pin to GND. The SS pin voltage (V_{SS}) is level shifted down by approximately $V_{SS(ofst)}$ (approximately 700 mV) and sent to one of the “+” (the “+” input with the lowest voltage dominates) inputs of the error amplifier. When this level shifted voltage (V_{SSE}) starts to rise at time t_1 (see Figure 7-1), the output voltage the controller expects, rises as well. Since V_{SSE} starts at near 0 V, the controller attempts to regulate the output voltage from a starting point of zero volts. It cannot do this due to the converter architecture. The output voltage starts from the input voltage less the drop across the diode (V_{IN} - V_D) and rises from there. The point at which the output voltage starts to rise (t_2) is the point where the V_{SSE} ramp passes the point where it is commanding more output voltage than (V_{IN} - V_D). This voltage level is labeled $V_{SSE(1)}$. The time required for the output voltage to ramp from a theoretical zero to the final regulated value (from t_1 to t_3) is determined by the time it takes for the capacitor connected to the SS pin (C_{SS}) to rise through a 700-mV range, beginning at $V_{SS(ofst)}$ above GND.

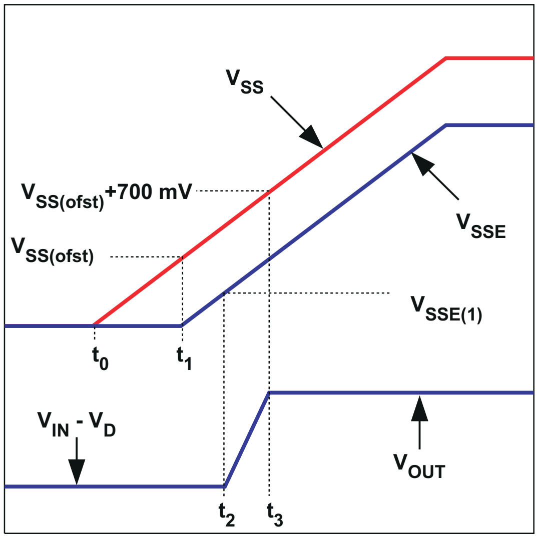


Figure 7-1. SS Pin Voltage and Output Voltage

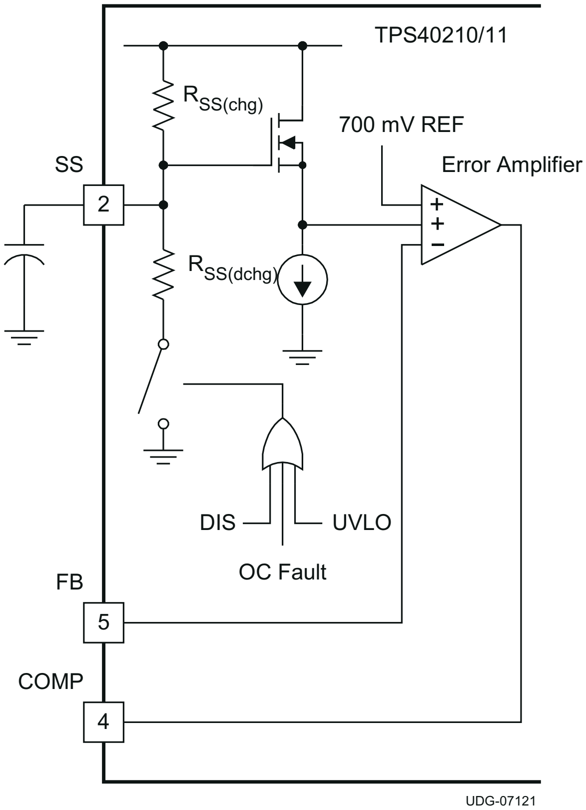


Figure 7-2. SS Pin Functional Circuit

The required capacitance for a given soft-start time $t_3 - t_1$ in Figure 7-1 is calculated in Equation 1.

$$C_{SS} = \frac{t_{SS}}{R_{SS} \times \ln\left(\frac{V_{BP} - V_{SS(ofst)}}{V_{BP} - \left(V_{SS(ofst)} + V_{FB}\right)}\right)} \tag{1}$$

where

- t_{SS} is the soft-start time, in seconds
- $R_{SS(chg)}$ is the SS charging resistance in Ω, typically 500 kΩ
- C_{SS} is the value of the capacitor on the SS pin, in F
- V_{BP} is the value of the voltage on the BP pin, in V
- $V_{SS(ofst)}$ is the approximate level shift from the SS pin to the error amplifier (~700 mV)
- V_{FB} is the error amplifier reference voltage, 700 mV typical

Note that t_{SS} is the time it takes for the output voltage to rise from 0 V to the final output voltage. Also note the tolerance on $R_{SS(chg)}$ given in the *Section 6.5*. This contributes to some variability in the output voltage rise time and margin must be applied to account for it in design.

Also take note of V_{BP}. Its value varies depending on input conditions. For example, a converter operating from a slowly rising input initializes V_{BP} at a fairly low value and increases during the entire startup sequence. If the controller has a voltage above 8 V at the input and the DIS pin is used to stop and then restart the converter, V_{BP} is approximately 8 V for the entire start-up sequence. The higher the voltage on BP, the shorter the start-up time is and conversely, the lower the voltage on BP, the longer the start-up time is.

The soft-start time (t_{SS}) must be chosen long enough so that the converter can start up without going into an overcurrent state. Since the over current state is triggered by sensing the peak voltage on the ISNS pin, that voltage must be kept below the overcurrent threshold voltage $V_{ISNS(oc)}$. The voltage on the ISNS pin is a function of the load current of the converter, the rate of rise of the output voltage and the output capacitance, and the current sensing resistor. The total output current that must be supported by the converter is the sum of the charging current required by the output capacitor and any external load that must be supplied during start-up. This current must be less than the $I_{OUT(oc)}$ value used in Equation 15 or Equation 16 (depending on the operating mode of the converter) to determine the current sense resistor value. In these equations, the actual input voltage at the time that the controller reaches the final output voltage is the important input voltage to use in the calculations. If the input voltage is slowly rising and is at less than the nominal input voltage when the start-up time ends, the output current limit is less than $I_{OUT(oc)}$ at the nominal input voltage. The output capacitor charging current must be reduced (decrease C_{OUT} or increase the t_{SS}) or $I_{OUT(oc)}$ must be increased and a new value for R_{ISNS} calculated.

$$I_{C(chg)} = \left(\frac{C_{OUT} \times V_{OUT}}{t_{SS}}\right) \tag{2}$$

$$t_{SS} > \left(\frac{C_{OUT} \times V_{OUT}}{\left(I_{OUT(oc)} - I_{EXT}\right)}\right) \tag{3}$$

where

- $I_{C(chg)}$ is the output capacitor charging current in A
- C_{OUT} is the total output capacitance in F
- V_{OUT} is the output voltage in V
- t_{SS} is the soft-start time from Equation 1
- $I_{OUT(oc)}$ is the desired over current trip point in A
- I_{EXT} is any external load current in A

The capacitor on the SS pin (C_{SS}) also plays a role in overcurrent functionality. It is used as the timer between restart attempts. The SS pin is connected to GND through a resistor, $R_{SS(dchg)}$, whenever the controller senses an overcurrent condition. Switching stops and nothing else happens until the SS pin discharges to the soft-start reset threshold, $V_{SS(rst)}$. At this point, the SS pin capacitor is allowed to charge again through the charging resistor $R_{SS(chg)}$, and the controller restarts from that point. The shortest time between restart attempts occurs when the SS pin discharges from $V_{SS(ofst)}$ (approximately 700 mV) to $V_{SS(rst)}$ (150 mV) and then back to $V_{SS(ofst)}$ and switching resumes. In actuality, this is a conservative estimate since switching does not resume until the V_{SSE} ramp rises to a point where it is commanding more output voltage than exists at the output of the controller. This occurs at some SS pin voltage greater than $V_{SS(ofst)}$ and depends on the voltage that remains on the output overvoltage the converter while switching has been halted. The fastest restart time can be calculated by using Equation 4, Equation 5, and Equation 6.

$$t_{DCHG} = R_{SS(dchg)} \times C_{SS} \times \ln\left(\frac{V_{SS(ofst)}}{V_{SS(rst)}}\right) \tag{4}$$

$$t_{CHG} = R_{SS(chg)} \times C_{SS} \times \ln\left(\frac{\left(V_{BP} - V_{SS(rst)}\right)}{\left(V_{BP} - V_{SS(ofst)}\right)}\right) \tag{5}$$

$$t_{RSTRT(min)} = t_{CHG} + t_{DCHG} \tag{6}$$

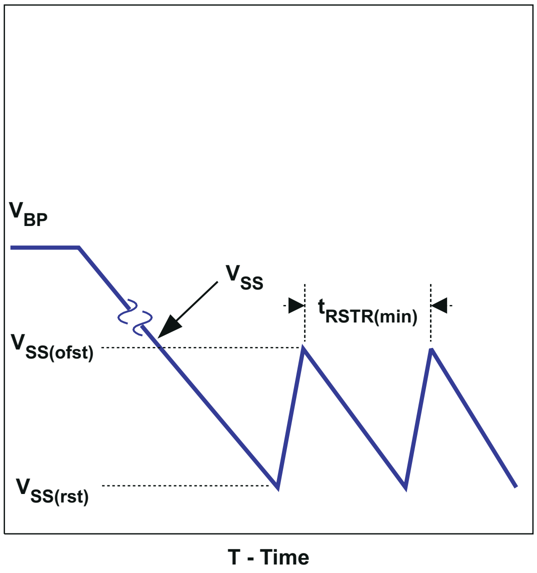


Figure 7-3. Soft Start during Overcurrent

7.3.2 BP Regulator

The TPS40210 and TPS40211 have an on-board linear regulator that supplies power to the internal circuitry of the controller, including the gate driver. This regulator has a nominal output voltage of 8 V and must be bypassed with a 1-µF capacitor. If the voltage at the VDD pin is less than 8 V, the voltage on the BP pin will also be less and the gate drive voltage to the external FET is reduced from the nominal 8 V. This should be considered when choosing a FET for the converter.

Connecting external loads to this regulator can be done, but care must be taken to ensure that the thermal rating of the device is observed since there is no thermal shutdown feature in this controller. Exceeding the thermal ratings causes out of specification behavior and can lead to reduced reliability. The controller dissipates more power when there is an external load on the BP pin and is tested for dropout voltage for up to 5-mA load. When the controller is in the disabled state, the BP pin regulator also shuts off so loads connected there power down as well. When the controller is disabled with the DIS/ $\overline{\text{EN}}$ pin, this regulator is turned off.

The total power dissipation in the controller can be calculated as follows. The total power is the sum of P_Q, P_G, and P_E.

$$P_Q = V_{VDD} \times I_{VDD(en)} \tag{7}$$

$$P_G = V_{VDD} \times Q_g \times f_{SW} \tag{8}$$

$$P_E = V_{VDD} \times I_{EXT} \tag{9}$$

where

- P_Q is the quiescent power of the device in W
- V_{DD} is the VDD pin voltage in V
- $I_{DD(en)}$ is the quiescent current of the controller when enabled but not switching in A
- P_G is the power dissipated by driving the gate of the FET in W
- Q_g is the total gate charge of the FET at the voltage on the BP pin in C
- f_{SW} is the switching frequency in Hz
- P_E is the dissipation caused be external loading of the BP pin in W
- I_{EXT} is the external load current in A

7.3.3 Shutdown (DIS/ $\overline{\text{EN}}$ Pin)

The DIS/ $\overline{\text{EN}}$ pin is an active high shutdown command for the controller. Pulling this pin above 1.2 V causes the controller to completely shut down and enter a low current consumption state. In this state, the regulator connected to the BP pin is turned off. There is an internal 1.1-MΩ pulldown resistor connected to this pin that keeps the pin at GND level when left floating. If this function is not used in an application, it is best to connect this pin to GND.

7.3.4 Minimum On-Time and Off-Time Considerations

The TPS40210 has a minimum off-time of approximately 200 ns and a minimum on-time of 300 ns. These two constraints place limitations on the operating frequency that can be used for a given input-to-output conversion ratio. See Figure 6-2 for the maximum frequency that can be used for a given duty cycle.

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in discontinuous conduction mode, the duty cycle varies with changes to the load much more than it does when running in continuous conduction mode.

In continuous conduction mode, the duty cycle is related primarily to the input and output voltages.

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{1}{1 - D} \tag{10}$$

$$D = \left(1 - \left(\frac{V_{IN}}{V_{OUT} + V_D}\right)\right) \tag{11}$$

In discontinuous mode, the duty cycle is a function of the load, input and output voltages, inductance, and switching frequency.

$$D = \frac{2 \times \left(V_{OUT} + V_D\right) \times I_{OUT} \times L \times f_{SW}}{\left(V_{IN}\right)^2} \tag{12}$$

All converters using a diode as the freewheeling or catch component have a load current level at which they transition from discontinuous conduction to continuous conduction. This is the point where the inductor current just falls to zero. At higher load currents, the inductor current does not fall to zero but remains flowing in a positive direction and assumes a trapezoidal wave shape as opposed to a triangular wave shape. This load boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as follows.

$$I_{OUT(crit)} = \frac{\left(V_{OUT} + V_D - V_{IN}\right) \times \left(V_{IN}\right)^2}{2 \times \left(V_{OUT} + V_D\right)^2 \times f_{SW} \times L} \tag{13}$$

For loads higher than the result of Equation 13, the duty cycle is given by Equation 11 and for loads less that the results of Equation 13, the duty cycle is given Equation 12. For Equations 1 through 4, the variable definitions are as follows.

- V_{OUT} is the output voltage of the converter in V
- V_D is the forward conduction voltage drop across the rectifier or catch diode in V
- V_{IN} is the input voltage to the converter in V
- I_{OUT} is the output current of the converter in A
- L is the inductor value in H
- f_{SW} is the switching frequency in Hz

7.3.5 Setting the Oscillator Frequency

The oscillator frequency is determined by a resistor and capacitor connected to the RC pin of the TPS40210. The capacitor is charged to a level of approximately $V_{DD}/20$ by current flowing through the resistor and is then discharged by a transistor internal to the TPS40210. The required resistor for a given oscillator frequency is found from either Figure 6-1 or Equation 14.

$$R_T = \frac{1}{5.8 \times 10^{-8} \times f_{SW} \times C_T + 8 \times 10^{-10} \times f_{SW}^2 + 1.4 \times 10^{-7} \times f_{SW} - 1.5 \times 10^{-4} + 1.7 \times 10^{-6} \times C_T - 4 \times 10^{-9} \times C_T^2} \tag{14}$$

where

- R_T is the timing resistance in kΩ
- f_{SW} is the switching frequency in kHz
- C_T is the timing capacitance in pF

For most applications, a capacitor in the range of 68 pF to 120 pF gives the best results. Resistor values should be limited to between 100 kΩ and 1 MΩ as well. If the resistor value falls below 100 kΩ, decrease the capacitor size and recalculate the resistor value for the desired frequency. As the capacitor size decreases below 47 pF, the accuracy of Equation 14 degrades and empirical means can be needed to fine tune the timing component values to achieve the desired switching frequency.

7.3.6 Synchronizing the Oscillator

The TPS40210 and TPS40211 can be synchronized to an external clock source. Figure 7-4 shows the functional diagram of the oscillator. When synchronizing the oscillator to an external clock, the RC pin must be pulled below 150 mV for 20 ns or more. The external clock frequency must be higher than the free running frequency of the converter as well. When synchronizing the controller, if the RC pin is held low for an excessive amount of time, erratic operation can occur. The maximum amount of time that the RC pin should be held low is 50% of a nominal output pulse, or 10% of the period of the synchronization frequency. If the external clock signal cannot operate with a low enough duty cycle to limit the amount of time the RC pin is held low, a resistor and capacitor can be added at the gate of the synchronization MOSFET. The capacitor should be added in series with the gate of the MOSFET to AC couple the rising edge of the synchronization signal. The resistor should be added from the gate of the MOSFET to ground to turn off the MOSFET. Typical values for the resistor and capacitor are 220 pF and 1 kΩ.

Under circumstances where the duty cycle is less than 50%, a Schottky diode connected from the RC pin to an external clock can be used to synchronize the oscillator. The cathode of the diode is connected to the RC pin. The trip point of the oscillator is set by an internal voltage divider to be 1/20 of the input voltage. The clock signal must have an amplitude higher than this trip point. When the clock goes low, it allows the reset current to restart the RC ramp, synchronizing the oscillator to the external clock. This provides a simple, single-component method for clock synchronization.

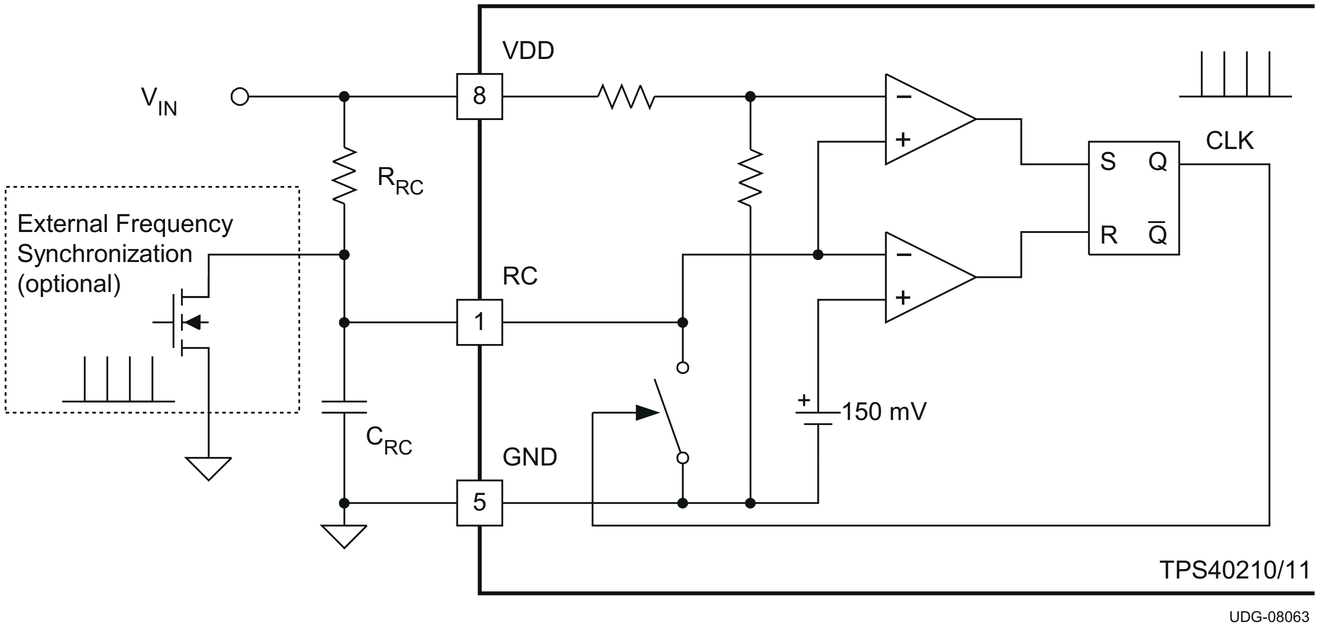


Figure 7-4. Oscillator Functional Diagram

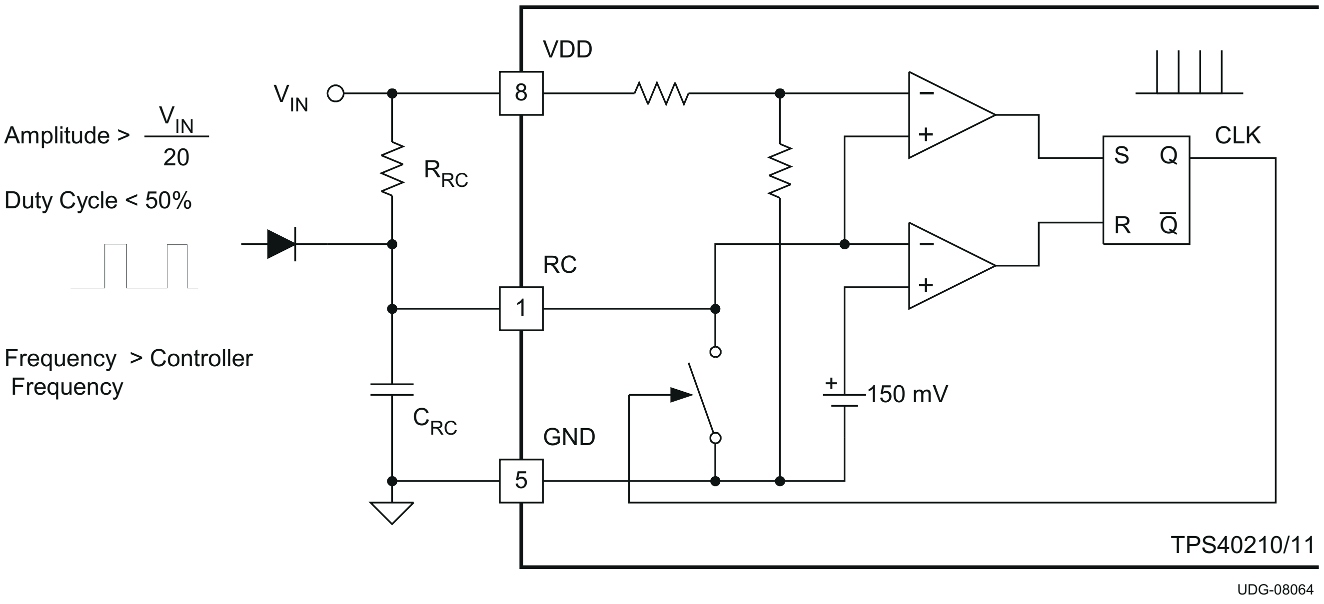


Figure 7-5. Diode Connected Synchronization

7.3.7 Current Sense and Overcurrent

The TPS4021x is a current mode controller that uses a resistor in series with the source terminal power FET to sense current for both the current mode control and overcurrent protection. The device enters a current limit state if the voltage on the ISNS pin exceeds the current limit threshold voltage $V_{ISNS(oc)}$ from the *Section 6.5*. When this happens, the controller discharges the SS capacitor through a relatively high impedance and then attempts to restart. The amount of output current that causes this to happen is dependent on several variables in the converter.

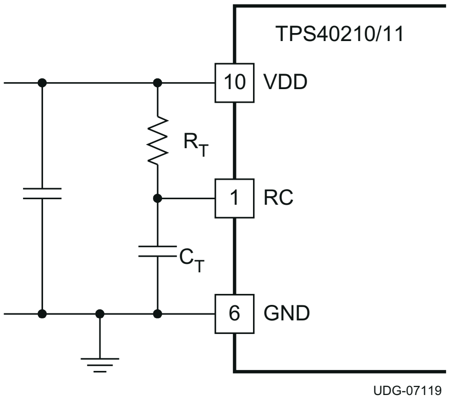


Figure 7-6. Oscillator Components

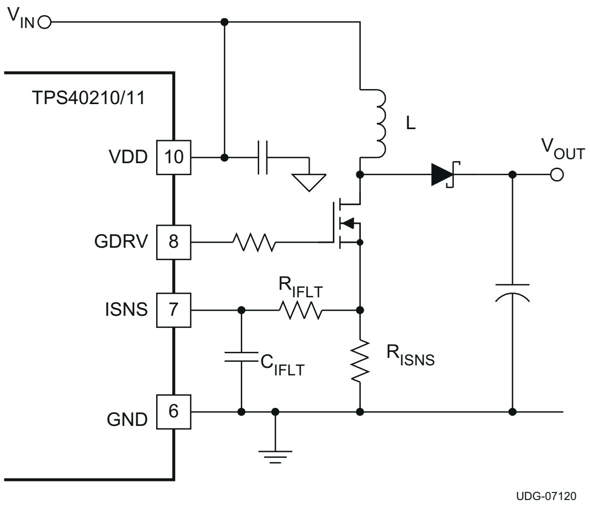


Figure 7-7. Current Sense Components

The load current overcurrent threshold is set by proper choice of R_{ISNS}. If the converter is operating in discontinuous mode, the current sense resistor is found in Equation 15.

$$R_{ISNS} = \frac{f_{SW} \times L \times V_{ISNS(oc)}}{\sqrt{2 \times L \times f_{SW} \times I_{OUT(oc)} \times \left(V_{OUT} + V_D - V_{IN}\right)}} \tag{15}$$

If the converter is operating in continuous conduction mode, R_{ISNS} can be found in Equation 16.

$$R_{ISNS} = \frac{V_{ISNS}}{\left(\frac{I_{OUT}}{1-D}\right) + \left(\frac{I_{RIPPLE}}{2}\right)} = \frac{V_{ISNS}}{\left(\frac{I_{OUT}}{(1-D)}\right) + \left(\frac{D \times V_{IN}}{2 \times f_{SW} \times L}\right)} \tag{16}$$

where

- R_{ISNS} is the value of the current sense resistor in Ω
- $V_{ISNS(oc)}$ is the overcurrent threshold voltage at the ISNS pin (from electrical specifications)
- D is the duty cycle (from Equation 11)
- f_{SW} is the switching frequency in Hz
- V_{IN} is the input voltage to the power stage in V (see text)
- L is the value of the inductor in H
- I_{OUT}(oc) is the desired overcurrent trip point in A
- V_D is the drop across the diode in Figure 7-7

The TPS40210 and TPS40211 have a fixed undervoltage lockout (UVLO) that allows the controller to start at a typical input voltage of 4.25 V. If the input voltage is slowly rising, the converter might have less than its designed nominal input voltage available when it has reached regulation. As a result, this can decrease the apparent current limit load current value and must be taken into consideration when selecting R_{ISNS}. The value of V_{IN} used to calculate R_{ISNS} must be the value at which the converter finishes start-up. The total converter output current at start-up is the sum of the external load current and the current required to charge the output capacitor or capacitors. See the *Section 7.3.1* section of this data sheet for information on calculating the required output capacitor charging current.

The topology of the standard boost converter has no method to limit current from the input to the output in the event of a short circuit fault on the output of the converter. If protection from this type of event is desired, it is necessary to use some secondary protection scheme, such as a fuse, or rely on the current limit of the upstream power source.

7.3.8 Current Sense and Subharmonic Instability

A characteristic of peak current mode control results in a condition where the current control loop can exhibit instability. This results in alternating long and short pulses from the pulse width modulator. The voltage loop maintains regulation and does not oscillate, but the output ripple voltage increases. The condition occurs only when the converter is operating in continuous conduction mode and the duty cycle is 50% or greater. The cause of this condition is described in the *Modeling, Analysis and Compensation of the Current-Mode Converter Application Report*. The remedy for this condition is to apply a compensating ramp from the oscillator to the signal going to the pulse width modulator. In the TPS40210 and TPS40211, the oscillator ramp is applied in a fixed amount to the pulse width modulator. The slope of the ramp is given in Equation 17.

$$s_e = f_{SW} \times \left(\frac{V_{VDD}}{20}\right) \tag{17}$$

To ensure that the converter does not enter into subharmonic instability, the slope of the compensating ramp signal must be at least half of the down slope of the current ramp signal. Since the compensating ramp is fixed in the TPS40210 and TPS40211, this places a constraint on the selection of the current sense resistor.

The down slope of the current sense wave form at the pulse width modulator is described in Equation 18.

$$m2 = \frac{A_{CS} \times R_{ISNS} \times \left(V_{OUT} + V_D - V_{IN}\right)}{L} \tag{18}$$

Since the slope compensation ramp must be at least half, and preferably equal to the down slope of the current sense waveform seen at the pulse width modulator, a maximum value is placed on the current sense resistor when operating in continuous mode at 50% duty cycle or greater. For design purposes, some margin should be applied to the actual value of the current sense resistor. As a starting point, the actual resistor chosen should be 80% or less that the value calculated in Equation 19. This equation calculates the resistor value that makes the slope compensation ramp equal to one half of the current ramp downslope. Values no more than 80% of this result would be acceptable.

$$R_{ISNS(max)} = \frac{V_{VDD} \times L \times f_{SW}}{60 \times \left(V_{OUT} + V_D - V_{IN}\right)} \tag{19}$$

where

- S_e is the slope of the voltage compensating ramp applied to the pulse width modulator in V/s
- f_{SW} is the switching frequency in Hz
- V_{DD} is the voltage at the VDD pin in V
- m2 is the down slope of the current sense waveform seen at the pulse width modulator in V/s
- R_{ISNS} is the value of the current sense resistor in Ω
- V_{OUT} is the converter output voltage V_{IN} is the converter power stage input voltage
- V_D is the drop across the diode in Figure 7-7

It is possible to increase the voltage compensation ramp slope by connecting the VDD pin to the output voltage of the converter instead of the input voltage as shown in Figure 7-7. This can help in situations where the converter design calls for a large ripple current value in relation to the desired output current limit setting.

Note

Connecting the VDD pin to the output voltage of the converter affects the start-up voltage of the converter since the controller undervoltage lockout (UVLO) circuit monitors the VDD pin and senses the input voltage less the diode drop before start-up. The effect is to increase the start-up voltage by the value of the diode voltage drop.

If an acceptable R_{ISNS} value is not available, the next higher value can be used and the signal from the resistor divided down to an acceptable level by placing another resistor in parallel with C_{IFLT}.

7.3.9 Current Sense Filtering

In most cases, a small filter placed on the ISNS pin improves performance of the converter. These are the components R_{IFLT} and C_{IFLT} in Figure 7-7. The time constant of this filter should be approximately 10% of the nominal pulse width of the converter. The pulse width can be found using Equation 20.

$$t_{ON} = \frac{D}{f_{SW}} \tag{20}$$

The suggested time constant is then

$$R_{IFLT} \times C_{IFLT} = 0.1 \times t_{ON} \tag{21}$$

The range of R_{IFLT} should be from about 1 kΩ to 5 kΩ for best results. Higher values can be used but this raises the impedance of the ISNS pin connection more than necessary and can lead to noise pickup issues in some layouts. C_{IFLT} should be located as close as possible to the ISNS pin as well to provide noise immunity.

7.3.10 Control Loop Considerations

There are two methods to design a suitable control loop for the TPS4021x. The first and preferred if equipment is available is to use a frequency response analyzer to measure the open loop modulator and power stage gain and to then design compensation to fit that. The usage of these tools for this purpose is well documented with the literature that accompanies the tool and is not be discussed here.

The second option is to make an initial guess at compensation, and then evaluate the transient response of the system to see if the compensation is acceptable to the application or not. For most systems, an adequate response can be obtained by simply placing a series resistor and capacitor (R_{FB} and C_{FB}) from the COMP pin to the FB pin as shown in Figure 7-8. The initial compensation selection can be done more accurately with aid of WEBENCH® to select the components or the average Spice model to simulate the open loop modulator and power stage gain.

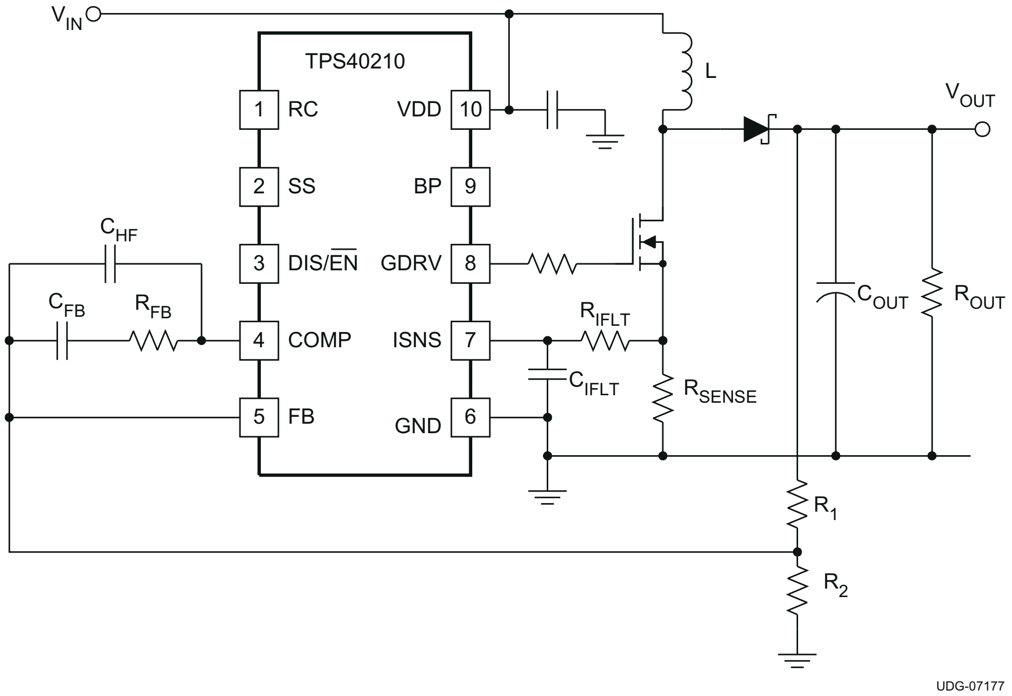


Figure 7-8. Basic Compensation Network

The natural phase characteristics of most capacitors used for boost outputs combined with the current mode control provide adequate phase margin when using this type of compensation. To determine an initial starting point for the compensation, the desired crossover frequency must be considered when estimating the control to output gain. The model used is a current source into the output capacitor and load.

When using these equations, the loop bandwidth should be no more than 20% of the switching frequency, f_{SW}. A more reasonable loop bandwidth would be 10% of the switching frequency. Be sure to evaluate the transient response of the converter over the expected load range to ensure acceptable operation.

$$\left|K_{CO}\right| = g_M \times \left|Z_{OUT}\left(f_{CO}\right)\right| \quad (22)$$

$$g_M = \frac{0.13 \times \sqrt{L \times \frac{f_{SW}}{R_{OUT}}}}{\left(R_{ISNS}\right)^2 \times \left(120 \times R_{ISNS} + L \times f_{SW}\right)} \quad (23)$$

$$\left|Z_{OUT}\right| = R_{OUT} \times \sqrt{\frac{\left(1+\left(2\pi \times f_L \times R_{ESR} \times C_{OUT}\right)^2\right)}{1+\left(\left(R_{OUT}\right)^2 + 2 \times R_{OUT} \times R_{ESR} + \left(R_{ESR}\right)^2\right) \times \left(2\pi \times f_L \times C_{OUT}\right)^2}} \quad (24)$$

where

- K_{CO} is the control to output gain of the converter, in V/V
- g_M is the transconductance of the power stage and modulator, in S
- R_{OUT} is the output load equivalent resistance, in Ω
- Z_{OUT} is the output impedance, including the output capacitor, in Ω
- R_{ISNS} is the value of the current sense resistor, in Ω
- L is the value of the inductor, in H
- C_{OUT} is the value of the output capacitance, in F
- R_{ESR} is the equivalent series resistance of C_{OUT}, in Ω
- f_{SW} is the switching frequency, in Hz
- f_L is the desired crossover frequency for the control loop, in Hz

These equations assume that the operation is discontinuous and that the load is purely resistive. The gain in continuous conduction can be found by evaluating Equation 23 at the resistance that gives the critical conduction current for the converter. Loads that are more like current sources give slightly higher gains than predicted here. To find the gain of the compensation network required for a control loop of bandwidth f_L, take the reciprocal of Equation 22.

$$K_{COMP} = \frac{1}{\left|K_{CO}\right|} \quad (25)$$

The GBWP of the error amplifier is only guaranteed to be at least 1.5MHz. If K_{COMP} multiplied by f_L is greater than 750 kHz, reduce the desired loop crossover frequency until this condition is satisfied. This ensures that the high-frequency pole from the error amplifier response with the compensation network in place does not cause excessive phase lag at f_L and decreased phase margin in the loop.

The RC network connected from COMP to FB places a zero in the compensation response. That zero should be approximately 1/10th of the desired crossover frequency, f_L. With that being the case, R_{FB} and C_{FB} can be found from Equation 26 and Equation 27.

$$R_{FB} = \frac{R1}{\left|K_{CO}\right|} = R1 \times K_{COMP} \quad (26)$$

$$C_{FB} = \frac{10}{2\pi \times f_L \times R_{FB}} \quad (27)$$

where

- R1 is the high side feedback resistor in Figure 7-8, in Ω
- f_L is the desired loop crossover frequency, in Hz

Thought not strictly necessary, it is recommended that a capacitor be added between COMP and FB to provide high-frequency noise attenuation in the control loop circuit. This capacitor introduces another pole in the compensation response. The allowable location of that pole frequency determines the capacitor value. As a starting point, the pole frequency should be 10 × f_L. The value of C_{HF} can be found from Equation 28.

$$C_{HF} = \frac{1}{20\pi \times f_L \times R_{FB}} \quad (28)$$

While the error amplifier GBWP will usually be higher, it can be as low as 1.5MHz. If 10 × K_{Comp} × f_L > 1.5MHz, the error amplifier gain-bandwidth product may limit the high-frequency response below that of the high-frequency capacitor. To maintain a consistent high-frequency gain roll-off, C_{HF} can be calculated by Equation 29.

$$C_{HF} = \frac{1}{2\pi \times 1.5 \times (10)^6 \times R_{FB}} \quad (29)$$

where

- C_{HF} is the high-frequency roll-off capacitor value in F
- R_{FB} is the mid band gain setting resistor value in Ω

7.3.11 Gate Drive Circuit

Some applications benefit from the addition of a resistor connected between the GDRV pin and the gate of the switching MOSFET. In applications that have particularly stringent load regulation (under 0.75%) requirements and operate from input voltages above 5 V, or are sensitive to pulse jitter in the discontinuous conduction region, this resistor is recommended. The recommended starting point for the value of this resistor can be calculated from Equation 30.

$$R_G = \frac{105}{Q_G} \quad (30)$$

where

- Q_G is the MOSFET total gate charge at 8 V, V_{GS} in nC
- R_G is the suggested starting point gate resistance in Ω

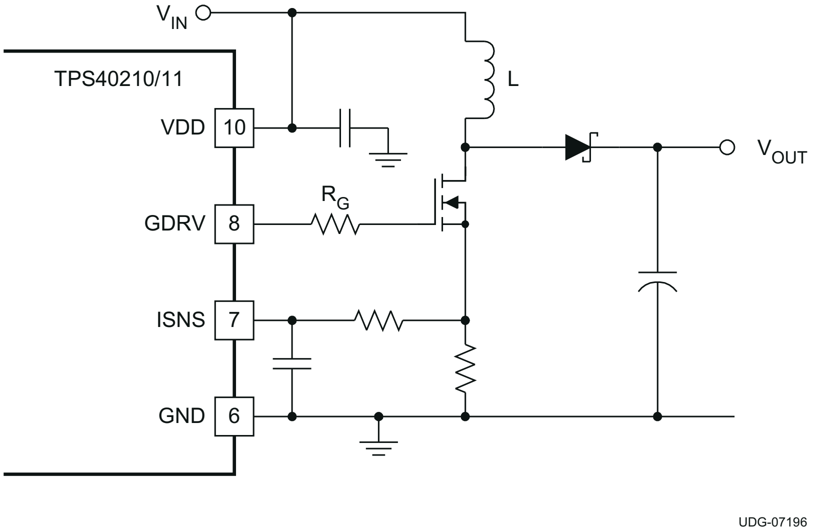


Figure 7-9. Gate Drive Resistor

7.3.12 TPS40211

The only difference between the TPS40210 and the TPS40211 is the reference voltage that the error amplifier uses to regulate the output voltage. The TPS40211 uses a 260-mV reference and is intended for applications where the output is actually a current instead of a regulated voltage. A typical example of an application of this type is an LED driver. An example schematic is shown in Figure 7-10.

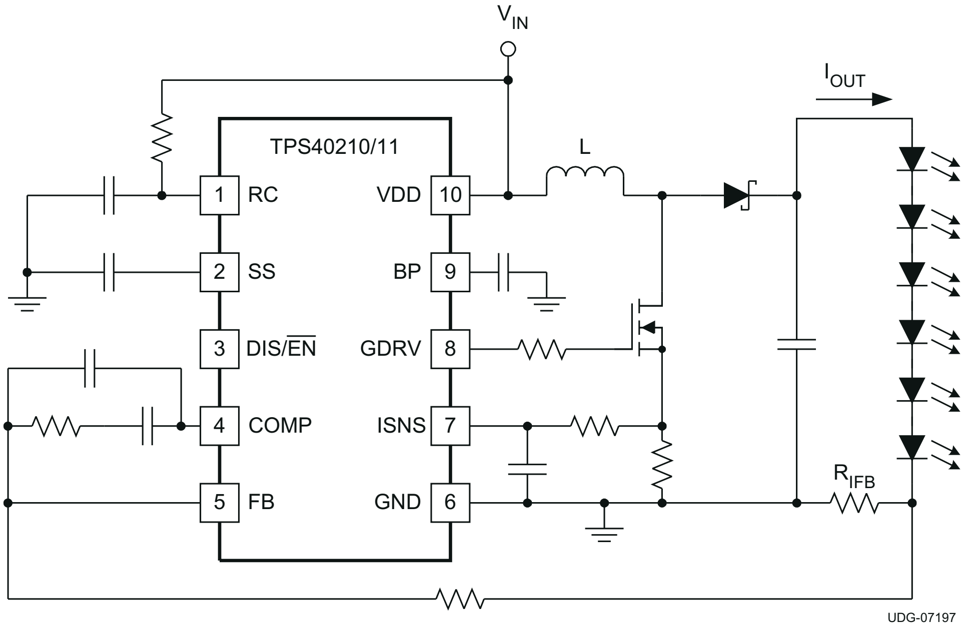


Figure 7-10. Typical LED Drive Schematic

The current in the LED string is set by the choice of the resistor R_{ISNS} as shown in Equation 31.

$$R_{IFB} = \frac{V_{FB}}{I_{OUT}} \tag{31}$$

where

- R_{IFB} is the value of the current sense resistor for the LED string in Ω
- V_{FB} is the reference voltage for the TPS40211 in V (0.260 V typ.)
- I_{OUT} is the desired DC current in the LED string in A

7.4 Device Functional Modes

7.4.1 Operation Near Minimum Input Voltage

The TPS4021x is designed to operate with input voltages above 4.5 V. The typical VDD UVLO threshold is 4.25 V and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device will not switch. When V_{VDD} passes the UVLO threshold the device will become active. Switching is enabled and the soft-start sequence is initiated. The TPS4021x will ramp up the output voltage at the rate determined by the external capacitor at the SS pin.

7.4.2 Operation With DIS/ $\overline{\text{EN}}$ Pin

The DIS/ $\overline{\text{EN}}$ pin has a 1.2-V typical threshold which can be used to disable the TPS4021x. With DIS/ $\overline{\text{EN}}$ forced above this threshold voltage, the device is disabled and switching is inhibited even if V_{VDD} is above its UVLO threshold. Hysteresis on the DIS/ $\overline{\text{EN}}$ pin threshold gives a typical turnon threshold of 1.05 V. If the DIS/ $\overline{\text{EN}}$ is left floating or is pulled below the 1.05-V threshold while V_{VDD} is above its UVLO threshold, the device becomes active. Switching is enabled and the soft-start sequence is initiated. The TPS4021x will ramp up the output voltage at the rate determined by the external capacitor at the soft-start pin.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS4021x is a 4.5-V to 52-V low-side controller with an integrated gate driver for a low-side N-channel MOSFET. This device is typically used in a boost topology to convert a lower DC voltage to a higher DC voltage with a peak current limit set by an external current sense resistor. It can also be configured in a SEPIC, Flyback and LED drive applications. In higher current applications, the maximum current can also be limited by the thermal performance of the external MOSFET and rectifying diode switch. Use the following design procedure to select external components for the TPS4021x. The design procedure illustrates the design of a typical boost regulator with the TPS40210. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

8.2 Typical Applications

8.2.1 12-V to 24-V Nonsynchronous Boost Regulator

The following example illustrates the design process and component selection for a 12-V to 24-V nonsynchronous boost regulator using the TPS40210 controller.

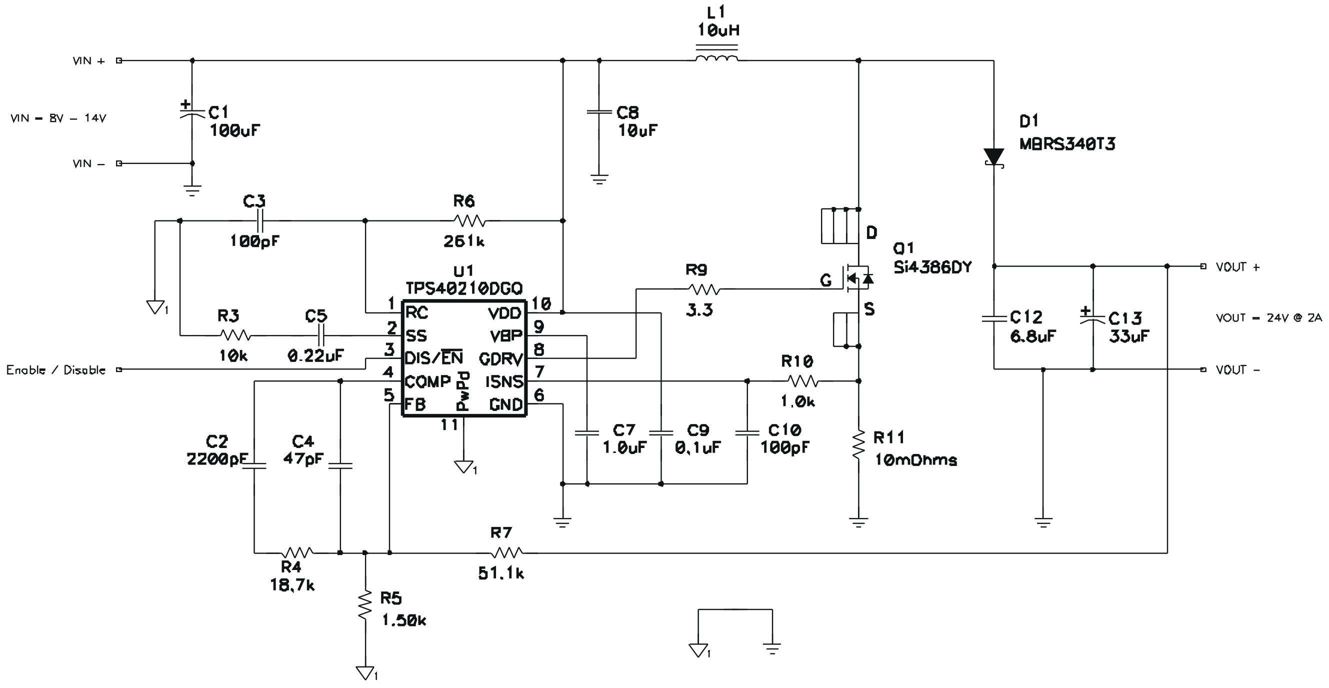


Figure 8-1. TPS40210 Design Example – 12 V to 24 V at 2 A

8.2.1.1 Design Requirements

Table 8-1. TPS40210 Design Example Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current			4.4		A
	No load input current				0.05	
$V_{IN(UVLO)}$	Input undervoltage lockout			4.5		V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage		23.5	24.0	24.5	V
	Line regulation				1%	
	Load regulation				1%	
$V_{OUT(ripple)}$	Output voltage ripple				500	mV_{PP}
I_{OUT}	Output current	8 V ≤ V_{IN} ≤ 14 V	0.1	1	2.0	A
I_{OCP}	Output overcurrent inception point		3.5			
	Transient response					
ΔI	Load step			1		A
	Load slew rate			1		A/µs
	Overshoot threshold voltage			500		mV
	Settling time			5		ms
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency			600		kHz
η_{PK}	Peak efficiency	V_{IN} = 12 V		95%		
η	Full load efficiency	V_{IN} = 12 V, I_{OUT} = 2 A		94%		
T_{OP}	Operating temperature range	8 V ≤ V_{IN} ≤ 14 V, I_{OUT} ≤ 2 A		25		°C
MECHANICAL DIMENSIONS						
W	Width			1.5		inch
L	Length			1.5		
h	Height			0.5		

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS40210 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.1.2.2 Duty Cycle Estimation

The duty cycle of the main switching MOSFET is estimated using Equation 32 and Equation 33.

$$D_{MIN} \approx \frac{V_{OUT} - V_{IN(max)} + V_{FD}}{V_{OUT} + V_{FD}} = \frac{24\,V - 14\,V + 0.5\,V}{24\,V + 0.5\,V} = 42.9\% \tag{32}$$

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN(min)} + V_{FD}}{V_{OUT} + V_{FD}} = \frac{24\,V - 8\,V + 0.5\,V}{24\,V + 0.5\,V} = 67.3\% \tag{33}$$

Using an estimated forward drop (V_{FD}) of 0.5 V for a schottky rectifier diode, the approximate duty cycle is 42.9% (minimum) to 67.3% (maximum).

8.2.1.2.3 Inductor Selection

The peak-to-peak ripple is chosen to be 30% of the maximum input current.

$$I_{RIPPLE(max)} = 0.3 \times \frac{I_{OUT(max)}}{1 - D_{MIN}} = 0.3 \times \frac{2}{1 - 0.429} = 1.05\,A \tag{34}$$

The minimum inductor size can be estimated using Equation 35.

$$L_{MIN} \approx \frac{V_{IN(max)}}{I_{RIPPLE(max)}} \times D_{MIN} \times \frac{1}{f_{SW}} = \frac{14\,V}{1.05\,A} \times 0.429 \times \frac{1}{600\,kHz} = 9.5\,\mu H \tag{35}$$

The next higher standard inductor value of 10 µH is selected. The ripple current for nominal and minimum V_{IN} is estimated by Equation 36 and Equation 37.

$$I_{RIPPLE(V_{in}typ)} \approx \frac{V_{IN}}{L} \times D \times \frac{1}{f_{SW}} = \frac{12\,V}{10\,\mu H} \times 0.50 \times \frac{1}{600\,kHz} = 1.02\,A \tag{36}$$

$$I_{RIPPLE(Vinmin)} \approx \frac{V_{IN}}{L} \times D \times \frac{1}{f_{SW}} = \frac{8\,V}{10\,\mu H} \times 0.673 \times \frac{1}{600\,kHz} = 0.90\,A \tag{37}$$

The worst case peak-to-peak ripple current occurs at 50% duty cycle (V_{IN} = 12.25 V) and is estimated as 1.02 A. Worst case RMS current through the inductor is approximated by Equation 38.

$$I_{Lrms} = \sqrt{\left(I_{L(avg)}\right)^2 + \left(\tfrac{1}{12} I_{RIPPLE}\right)^2} \approx \sqrt{\left(\frac{I_{OUT(max)}}{1 - D_{MAX}}\right)^2 + \left(\tfrac{1}{12} I_{RIPPLE(VINmin)}\right)^2} = \sqrt{\left(\frac{2}{1 - 0.673}\right)^2 + \left(\left(\tfrac{1}{12}\right) \times 0.90A\right)^2} = 6.13\,Arms \tag{38}$$

The worst case RMS inductor current is 6.13 Arms. The peak inductor current is estimated by Equation 39.

$$I_{Lpeak} \approx \frac{I_{OUT(max)}}{1 - D_{MAX}} + \left(\tfrac{1}{2}\right) I_{RIPPLE(Vinmin)} = \frac{2}{1 - 0.673} + \left(\tfrac{1}{2}\right) 0.90 = 6.57\,A \tag{39}$$

A 10-µH inductor with a minimum RMS current rating of 6.13 A and minimum saturation current rating of 6.57 A must be selected. A TDK RLF12560T-100M-7R5 7.5-A 10-µH inductor is selected.

This inductor power dissipation is estimated by Equation 40.

$$P_L \approx \left(I_{Lrms}\right)^2 \times DCR \tag{40}$$

The TDK RLF12560T-100M-7R5 12.4-mΩ DCR dissipates 466-mW of power.

8.2.1.2.4 Rectifier Diode Selection

A low forward voltage drop schottky diode is used as a rectifier diode to reduce its power dissipation and improve efficiency. Using 80% derating on V_{OUT} for ringing on the switch node, the rectifier diode minimum reverse break-down voltage is given by Equation 41.

$$V_{(BR)R(min)} \geq \frac{V_{OUT}}{0.8} = 1.25 \times V_{OUT} = 1.25 \times 24\,V = 30\,V \tag{41}$$

The diode must have reverse breakdown voltage greater than 30 V. The rectifier diode peak and average currents are estimated by Equation 42 and Equation 43.

$$I_{D(avg)} \approx I_{OUT(max)} = 2\,A \tag{42}$$

$$I_{D(peak)} = I_{L(peak)} = 6.57\,A \tag{43}$$

The power dissipation in the diode is estimated by Equation 44.

$$P_{D(max)} \approx V_{FD} \times I_{D(avg)} = 0.5\,V \times 2\,A = 1\,W \tag{44}$$

For this design, the maximum power dissipation is estimated as 1 W. Reviewing 30-V and 40-V schottky diodes, the MBRS340T3, 40-V, 3-A diode in an SMC package is selected. This diode has a forward voltage drop of 0.48 V at 6 A, so the conduction power dissipation is approximately 960 mW, less than half its rated power dissipation.

8.2.1.2.5 Output Capacitor Selection

Output capacitors must be selected to meet the required output ripple and transient specifications.

$$C_{OUT} = 8\frac{I_{OUT} \times D}{V_{OUT(ripple)}} \times \frac{1}{f_{SW}} = 8\left(\frac{2\,A \times 0.673}{500\,mV}\right) \times \frac{1}{600\,kHz} = 36\,\mu F \tag{45}$$

$$ESR = \frac{7}{8} \times \frac{V_{OUT(ripple)}}{I_{L(peak)} - I_{OUT}} = \frac{7}{8} \times \frac{500\,mV}{6.57\,A - 2\,A} = 96\,m\Omega \tag{46}$$

A Panasonic EEEFC1V330P 35-V 33-μF, 120-mΩ bulk capacitor and a 6.8-μF ceramic capacitor are selected to provide the required capacitance and ESR at the switching frequency. The combined capacitance of 39.8 μF and ESR of 60 mΩ are used in compensation calculations.

8.2.1.2.6 Input Capacitor Selection

Since a boost converter has continuous input current, the input capacitor senses only the inductor ripple current. The input capacitor value can be calculated by Equation 47 and Equation 48.

$$C_{IN} > \frac{I_{RIPPLE}}{4 \times V_{IN(ripple)} \times f_{SW}} = \frac{1.02\,A}{4 \times 60\,mV \times 600\,kHz} = 7.1\,\mu F \tag{47}$$

$$ESR < \frac{V_{IN(ripple)}}{2 \times I_{RIPPLE}} = \frac{60\,mV}{2 \times 1.02\,A} = 29\,m\Omega \tag{48}$$

For this design to meet a maximum input ripple of 60 mV (1/2% of V_{IN} nominal), a minimum 7.1-μF input capacitor with ESR less than 29 mΩ is needed. A 10-μF, X7R ceramic capacitor is selected.

8.2.1.2.7 Current Sense and Current Limit

The maximum allowable current sense resistor value is limited by both the current limit and sub-harmonic stability. These two limitations are given by Equation 49 and Equation 50.

$$R_{ISNS} < \frac{V_{ISNS(OC)MIN}}{1.1 \times \left(I_{L(peak)} + I_{Drive}\right)} = \frac{120\,\text{mV}}{1.1 \times (6.57\,\text{A} + 0.50\,\text{A})} = 15.4\,\text{m}\Omega \tag{49}$$

$$R_{ISNS} < \frac{V_{IN(MAX)} \times L \times f_{SW}}{60 \times (V_{OUT} + V_{FD} - V_{IN})} = \frac{14\,\text{V} \times 10\,\mu\text{H} \times 600\,\text{kHz}}{60 \times (24\,\text{V} + 0.48\,\text{V} - 14\,\text{V})} = 134\,\text{m}\Omega \tag{50}$$

With 10% margin on the current limit trip point (the 1.1 factor) and assuming a maximum gate drive current of 500 mA, the current limit requires a resistor less than 15.4 mΩ and stability requires a sense resistor less than 134 mΩ. A 10-mΩ resistor is selected. Approximately 2 mΩ of routing resistance is added in compensation calculations.

The power dissipation in R_{ISNS} is calculated by Equation 51.

$$P_{R_{ISNS}} = (I_{LRMS})^2 \cdot R_{ISNS} \cdot D \tag{51}$$

At maximum duty cycle, this is 0.253 W.

8.2.1.2.8 Current Sense Filter

To remove switching noise from the current sense, an RC filter is placed between the current sense resistor and the ISNS pin. A resistor with a value between 1 kΩ and 5 kΩ is selected and a capacitor value is calculated by Equation 52.

$$C_{IFLT} = \frac{0.1 \times D_{MIN}}{f_{SW} \times R_{IFLT}} = \frac{0.1 \times 0.429}{600\,\text{kHz} \times 1\text{k}\Omega} = 71\text{pF} \tag{52}$$

For a 1-kΩ filter resistor, 71 pF is calculated and a 100-pF capacitor is selected.

8.2.1.2.9 Switching MOSFET Selection

The TPS40210 drives a ground referenced N-channel FET. The $R_{DS(on)}$ and gate charge are estimated based on the desired efficiency target.

$$P_{DISS(total)} \approx P_{OUT} \times \left(\frac{1}{\eta} - 1\right) = V_{OUT} \times I_{OUT} \times \left(\frac{1}{\eta} - 1\right) = 24\,\text{V} \times 2\,\text{A} \times \left(\frac{1}{0.95} - 1\right) = 2.526\,\text{W} \tag{53}$$

For a target of 95% efficiency with a 24-V input voltage at 2 A, maximum power dissipation is limited to 2.526 W. The main power dissipating devices are the MOSFET, inductor, diode, current sense resistor and the integrated circuit, the TPS40210.

$$P_{FET} < P_{DISS(total)} - P_L - P_D - P_{Risns} - V_{IN(max)} \times I_{VDD(max)} \tag{54}$$

This leaves 812 mW of power dissipation for the MOSFET. This can likely cause an SO-8 MOSFET to get too hot, so power dissipation is limited to 500 mW. Allowing half for conduction and half for switching losses, we can determine a target $R_{DS(on)}$ and Q_{GS} for the MOSFET by Equation 55 and Equation 56.

$$Q_{GS} < \frac{3 \times P_{FET} \times I_{DRIVE}}{2 \times V_{OUT} \times I_{OUT} \times f_{SW}} = \frac{3 \times 0.50\,\text{W} \times 0.50\,\text{A}}{2 \times 24\,\text{V} \times 2\,\text{A} \times 600\,\text{kHz}} = 13.0\,\text{nC} \tag{55}$$

A target MOSFET gate-to-source charge of less than 13.0 nC is calculated to limit the switching losses to less than 250 mW.

$$R_{DS(on)} < \frac{P_{FET}}{2 \times (I_{RMS})^2 \times D} = \frac{0.50\,W}{2 \times 6.13^2 \times 0.673} = 9.9\,m\Omega \tag{56}$$

A target MOSFET $R_{DS(on)}$ of 9.9 mΩ is calculated to limit the conduction losses to less than 250 mW. Reviewing 30-V and 40-V MOSFETs, an Si4386DY 9-mΩ MOSFET is selected. A gate resistor was added per Equation 30. The maximum gate charge at V_{GS}= 8V for the Si4386DY is 33.2 nC, this implies R_G = 3.3 Ω.

8.2.1.2.10 Feedback Divider Resistors

The primary feedback divider resistor (R_{FB}) from V_{OUT} to FB should be selected between 10 kΩ and 100 kΩ to maintain a balance between power dissipation and noise sensitivity. For a 24-V output, a high feedback resistance is desirable to limit power dissipation so R_{FB} = 51.1 kΩ is selected.

$$R_{BIAS} = \frac{V_{FB} \times R_{FB}}{V_{OUT} - V_{FB}} = \frac{0.700\,V \times 51.1\,k\Omega}{24\,V - 0.700\,V} = 1.53\,k\Omega \tag{57}$$

R_{BIAS} = 1.50 kΩ is selected.

8.2.1.2.11 Error Amplifier Compensation

Compensation selection can be done with aid of WEBENCH to select compensation components or with the aid of the average Spice model to simulate the open loop modulator and power stage gain. Alternatively, the following procedure gives a good starting point.

While current mode control typically only requires Type II compensation, it is desirable to layout for Type III compensation to increase flexibility during design and development. Current mode control boost converters have higher gain with higher output impedance, so it is necessary to calculate the control loop gain at the maximum output impedance, estimated by Equation 58.

$$R_{OUT(max)} = \frac{V_{OUT}}{I_{OUT(min)}} = \frac{24\,V}{0.1\,A} = 240\,\Omega \tag{58}$$

The transconductance of the TPS40210 current mode control can be estimated by Equation 59.

$$g_M = \frac{0.13 \times \sqrt{L \times \frac{f_{SW}}{R_{OUT}}}}{(R_{ISNS})^2 \times (120 \times R_{ISNS} + L \times f_{SW})} = \frac{0.13 \times \sqrt{10\,\mu H \times \frac{600\,kHz}{240\,\Omega}}}{(12\,m\Omega)^2 \times (120 \times 12\,m\Omega + 10\,\mu H \times 600\,kHz)} = 19.2\,{}^{A}\!/_{V} \tag{59}$$

The maximum output impedance Z_{OUT}, can be estimated by Equation 60.

$$\left|Z_{OUT}(f)\right| = R_{OUT} \times \sqrt{\frac{\left(1 + (2\pi \times f \times R_{ESR} \times C_{OUT})^2\right)}{1 + \left((R_{OUT})^2 + 2 \times R_{OUT} \times R_{ESR} + (R_{ESR})^2\right) \times (2\pi \times f \times C_{OUT})^2}} \tag{60}$$

$$\left|Z_{OUT}(f_L)\right| = 240\,\Omega \times \sqrt{\frac{\left(1 + (2\pi \times 30\,kHz \times 60\,m\Omega \times 39.8\,\mu F)^2\right)}{1 + \left((240\,\Omega)^2 + 2 \times 240\,\Omega \times 60\,m\Omega + (60\,m\Omega)^2\right) \times (2\pi \times 30\,kHz \times 39.8\,\mu F)^2}} = 0.146\,\Omega \tag{61}$$

At the desired crossover frequency (f_L) of 30 kHz, Z_{OUT} becomes 0.146 Ω.

The modulator gain at the desired cross-over can be estimated by Equation 62.

$$\left|K_{CO}\right| = g_M \times \left|Z_{OUT}\left(f_{CO}\right)\right| = 19.2\,{}^{A}\!/\!{}_{V} \times 0.146\,\Omega = 2.80 \tag{62}$$

The feedback compensation network needs to be designed to provide an inverse gain at the cross-over frequency for unity loop gain. This sets the compensation mid-band gain at a value calculated in Equation 63.

$$K_{COMP} = \frac{1}{\left|K_{CO}\right|} = \frac{1}{2.80} = 0.357 \tag{63}$$

To set the mid-band gain of the error amplifier to K_{COMP}, use Equation 64.

$$R4 = R7 \times K_{COMP} = \frac{R7}{\left|K_{CO}\right|} = \frac{51.1\,k\Omega}{2.80} = 18.2\,k\Omega \tag{64}$$

R4 = 18.7 kΩ selected.

Place the zero at 1/10th of the desired cross-over frequency.

$$C2 = \frac{10}{2\pi \times f_L \times R4} = \frac{10}{2\pi \times 30\,kHz \times 18.7\,k\Omega} = 2837\,pF \tag{65}$$

C2 = 2200 pF selected.

Place a high-frequency pole at about five times the desired cross-over frequency and less than one-half the unity gain bandwidth of the error amplifier:

$$C4 \approx \frac{1}{10\pi \times f_L \times R4} = \frac{1}{10\pi \times 30\,kHz \times 18.7\,k\Omega} = 56.74\,pF \tag{66}$$

$$C4 > \frac{1}{\pi \times GBW \times R4} = \frac{1}{\pi \times 1.5\,MHz \times 18.7\,k\Omega} = 11.35\,pF \tag{67}$$

C4 = 47 pF selected.

8.2.1.2.12 RC Oscillator

The RC oscillator calculation is given as shown in Equation 14 in the data sheet, substituting 100 for C_T and 600 for f_{SW}. For a 600-kHz switching frequency, a 100pF capacitor is selected and a 262-kΩ resistor is calculated (261-kΩ selected).

8.2.1.2.13 Soft-Start Capacitor

Since VDD > 8 V, the soft-start capacitor is selected by using Equation 68 to calculate the value.

$$C_{SS} = 20 \times T_{SS} \times 10^{-6} \tag{68}$$

For T_{SS} = 12 ms, C_{SS} = 240 nF. A 220-nF capacitor is selected.

8.2.1.2.14 Regulator Bypass

A regulator bypass (BP) capacitor of 1.0 µF is selected per the datasheet recommendation.

8.2.1.2.15 Bill of Materials

Table 8-2. Bill of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SIZE	PART NUMBER	MANUFAC-TURER
C1	100 µF, aluminum capacitor, SM, ± 20%, 35 V	0.406 x 0.457	EEEFC1V101P	Panasonic
C2	2200 pF, ceramic capacitor, 25 V, X7R, 20%	0603	Std	Std
C3	100 pF, ceramic capacitor, 16 V, C0G, 10%	0603	Std	Std
C4	47 pF, ceramic capacitor, 16V, X7R, 20%	0603	Std	Std
C5	0.22 µF, ceramic capacitor, 16 V, X7R, 20%	0603	Std	Std
C7	1.0 µF, ceramic capacitor, 16 V, X5R, 20%	0603	Std	Std
C8	10 µF, ceramic capacitor, 25 V, X7R, 20%	0805	C3225X7R1E106M	TDK
C9	0.1 µF, ceramic capacitor, 50 V, X7R, 20%	0603	Std	Std
C10	100 pF, ceramic capacitor, 16 V, X7R, 20%	0603	Std	Std
D1	Schottky diode, 3 A, 40 V	SMC	MBRS340T3	On Semi
L1	10 µH, inductor, SMT, 7.5 A, 12.4 mΩ	0.325 x 0.318 inch	RLF12560T-100M-7R5	TDK
Q1	MOSFET, N-channel, 40 V, 14 A, 9mΩ	SO-8	Si4840DY	Vishay
R3	10 kΩ, chip resistor, 1/16 W, 5%	0603	Std	Std
R4	18.7 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R5	1.5 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R6	261 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R7	51.1 kΩ, chip resistor, 1/16 W, 1%	0603	Std	Std
R9	3.3 Ω, chip resistor, 1/16 W, 5%	0603	Std	Std
R10	1.0 kΩ, chip resistor, 1/16 W, 5%	0603	Std	Std
R11	10 mΩ, chip resistor, 1/2 W, 2%	1812	Std	Std
U1	IC, 4.5 V-52 V I/P, current mode boost controller	DGQ10	TPS40210DGQ	TI

8.2.1.3 Application Curves

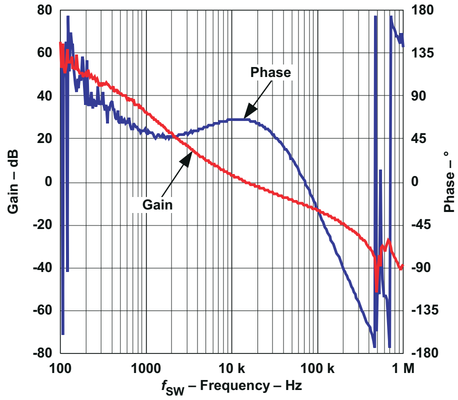


Figure 8-2. Gain and Phase vs Frequency

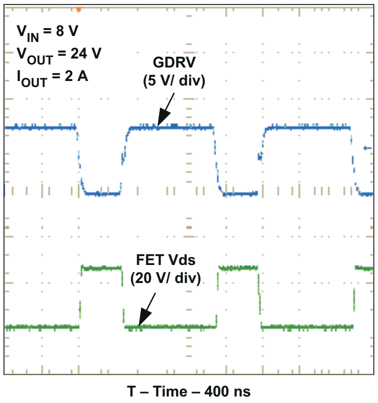


Figure 8-3. FET VDS and VGS Voltages vs Time

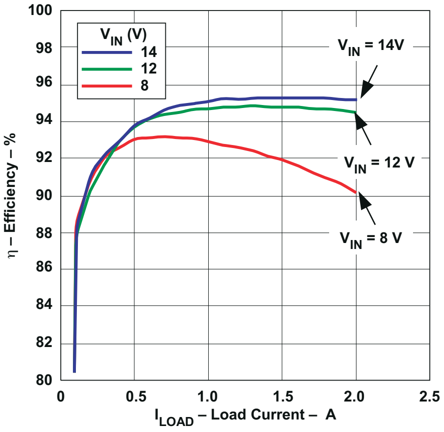


Figure 8-4. Efficiency vs Load Current

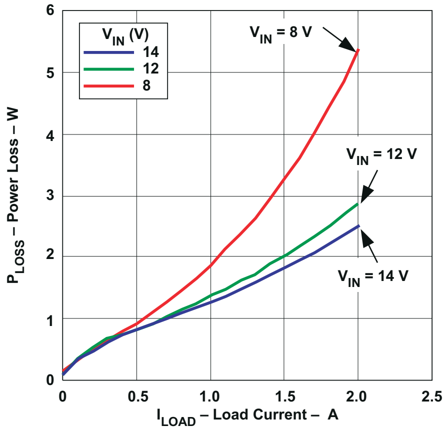


Figure 8-5. Power Loss vs Load Current

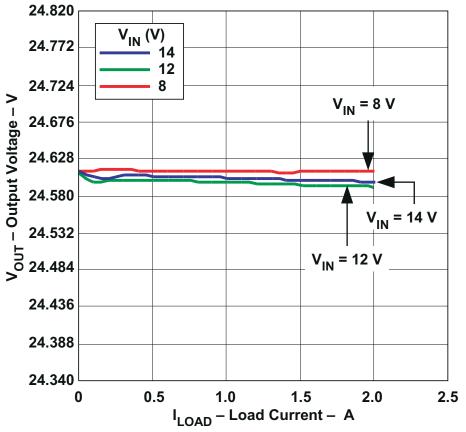


Figure 8-6. Output Voltage vs Load Current

8.2.2 12-V Input, 700-mA LED Driver, Up to 35-V LED String

This application uses the TPS40211 as a boost controller that drives a string of LED diodes. The feedback point for this circuit is a sense resistor in series with this string. The low 260-mV reference minimizes power wasted in this resistor, and maintains the LED current at a value given by 0.26/R6. As the input voltage is varied, the duty cycle changes to maintain the LED current at a constant value so that the light intensity does not change with large input voltage variations.

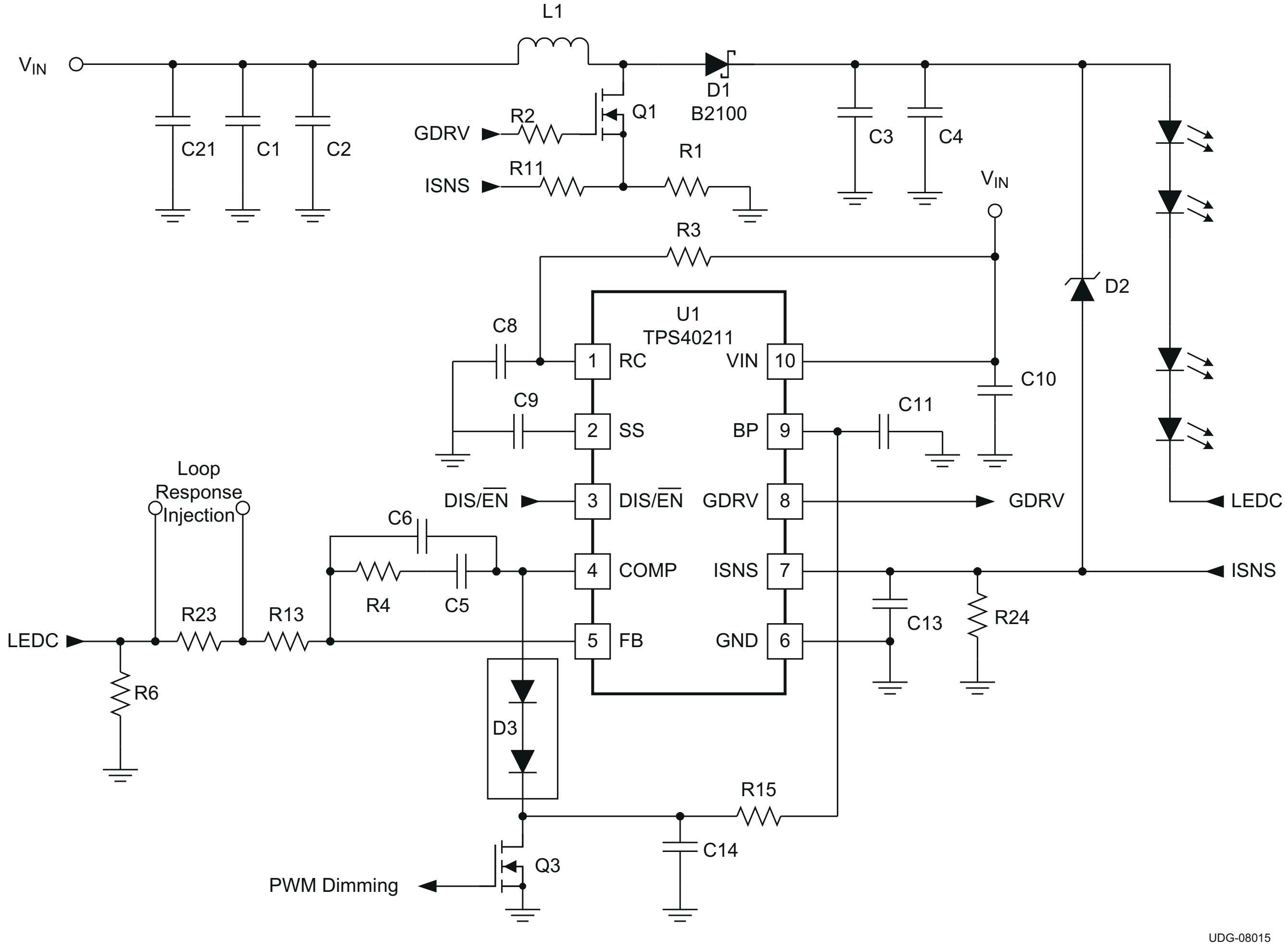


Figure 8-7. 12-V Input, 700-mA LED Driver, Up to 35-V LED String

8.2.2.1 Design Requirements

Table 8-3. TPS40211 Design Example Specifications

PARAMETER		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN}	Input voltage	8	12	20	V
OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage			35	V
I_{OUT}	Output current		0.7		A
SYSTEM CHARACTERISTICS					
f_{SW}	Switching frequency		400		kHz

8.2.2.2 Detailed Design Procedure

Table 8-4. TPS40211 LED Driver Bill of Materials

REFERENCE DESIGNATOR	TYPE	DESCRIPTION	SIZE
C1,C2	Capacitor	10 µF, 25 V	1206
C3, C4		2.2 µF, 100 V	1210
C5		1 nF, NPO	0603
C6		100 pF, NPO	0603
C8		100 pF	0603
C9		0.1 µF	0603
C10		0.1 µF, 25 V	0805
C11		1 µF, 25 V	1206
C13		220 pF	0603
C14		10 nF, X7R	0603
C21		330 µF, 25 V electrolytic	
D1	Diode	B2100, SHTKY, 100 V, 2 A	SMB
D2		BZT52C43	SOD-123
D3		MMBD7000	SOT-23
L1	Inductor	Wurth 7447709100, 10 µH, 6 A	12mm × 12mm × 10mm
Q1	MOSFET	Si7850DP, 60 V, 31 mΩ	SO-8
Q3		2N7002, 60 V, 0.1 A	SOT-23
R1	Resistor	15 mΩ	2512
R2		3.01 Ω	0805
R3		402 kΩ	0603
R4		14.3 kΩ	0603
R6		0.36 Ω	2512
R11		1 kΩ	0603
R13		30.1 kΩ	0603
R15		49.9 kΩ	0603
R24		10 kΩ	0603
R23		10 Ω	0603
U1	Integrated circuit	TPS40211	DRC-10

9 Power Supply Recommendations

The TPS4021x is designed to operate from an input voltage supply range between 4.5 V and 52 V. This input supply should remain within the input voltage range of the TPS4021x. If the input supply is located more than a few inches from the buck power stage controlled by the TPS4021x, additional bulk capacitance can be required in addition to ceramic-bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

10 Layout

10.1 Layout Guidelines

- For the maximum effectiveness from C9, place it near the VDD pin of the controller. Excessive high frequency noise on VDD during switching degrades overall regulation as the load increases.
- Keep the output loop (Q1-D1-C12-R11) as small as possible. A larger loop can degrade current limit accuracy and increase rediated emissions.
- For best current limit accuracy keep the ISNS filter components C10 and R10 near the ISNS and GND pins.
- Avoid connecting traces carrying large AC currents through a ground plane. Instead, use PCB traces on the top layer to conduct the AC current and use the ground plane as a noise shield.
- Split the ground plane as necessary to keep noise away from the TPS4021x and noise sensitive areas such as components connected to the RC pin, FB pin, COMP pin, and SS pin. Also keep these noise sensitive components close to the TPS4021x IC.
- Keep C7 near the BP and GND pins to provide good bypass for the BP regulator.
- The GDRV trace should be as close as possible to the power FET gate to minimize parisitic resistance and inductance in the trace. The parasitics should also be minimized in the return path from the source of the MOSFET, through the sense resistor and back to the GND pin.
- Keep the SW node as physically small as possible to minimize parasitic capacitance and radiated emissions.
- For good output voltage regulation, Kelvin connections should be brought from the load to the top FB resistor R7.

10.2 Layout Example

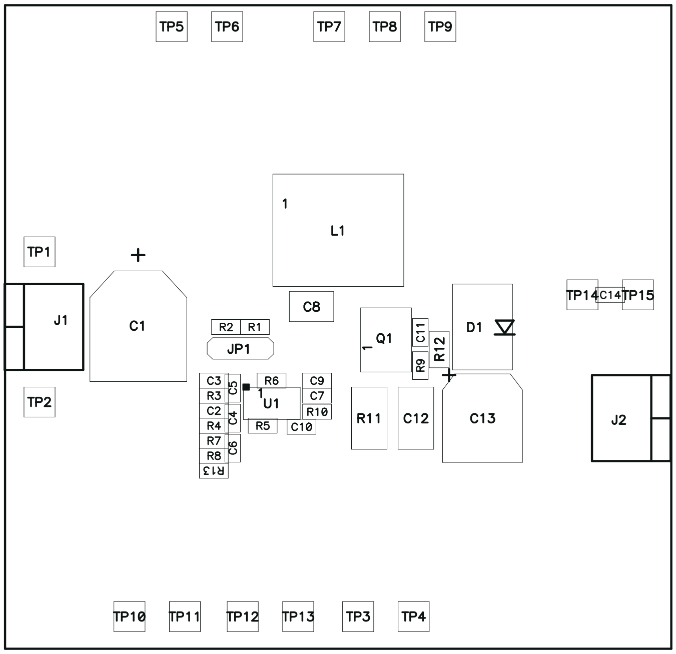


Figure 10-1. Component Placement

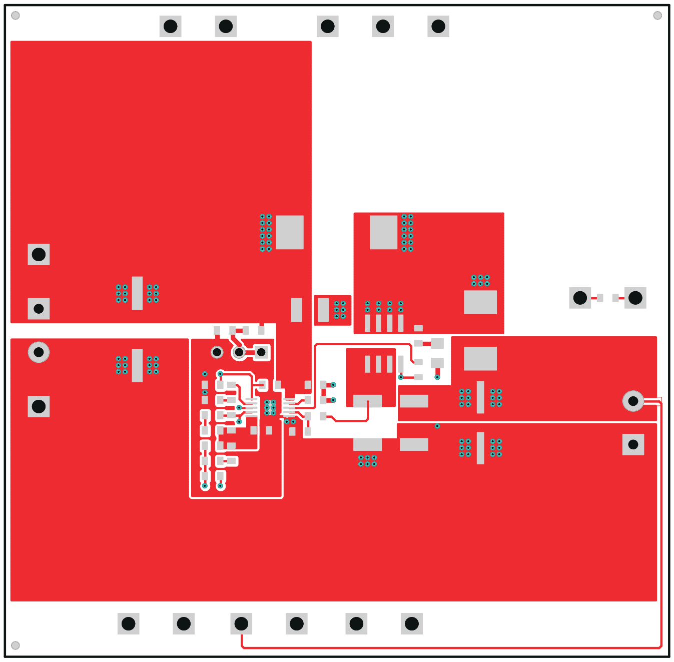


Figure 10-2. Top Copper

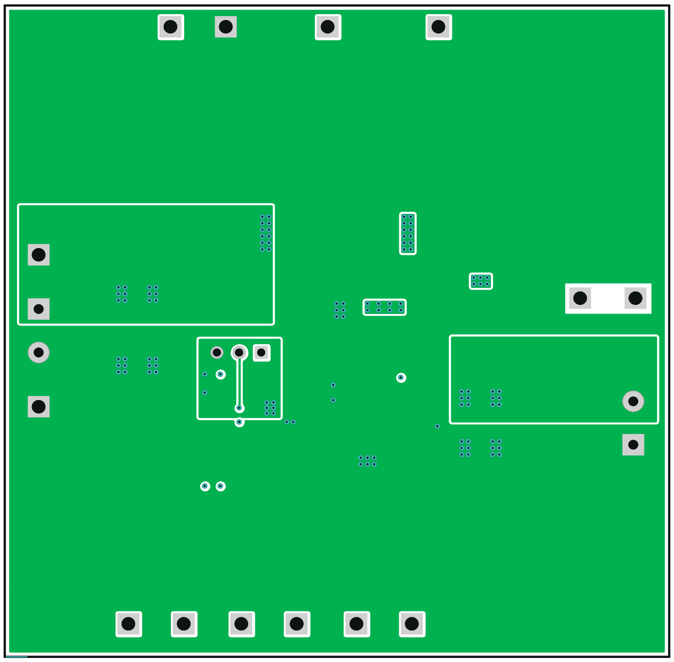


Figure 10-3. Bottom Copper Viewed From Top

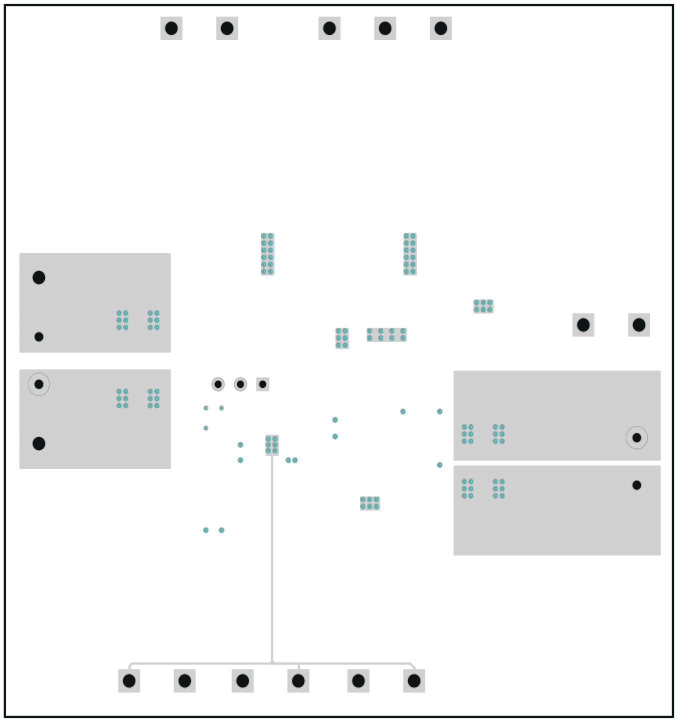


Figure 10-4. Internal 1 Copper Viewed From Top

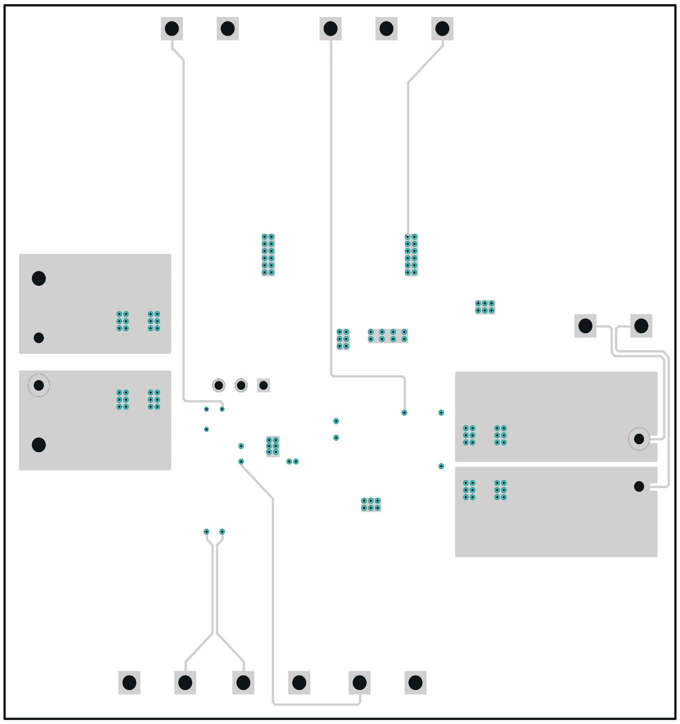


Figure 10-5. Internal 2 Copper Viewed From Top

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

- *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
- *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series

11.1.2 Related Devices

The following devices have characteristics similar to the TPS40210 and may be of interest.

Table 11-1. Related Parts

DEVICE	DESCRIPTION
TPS6100x	Single- and Dual-Cell Boost Converter with Start-up into Full Load
TPS6101x	High Efficiency 1-Cell and 2-Cell Boost Converters
TPS6300x	High Efficiency Single Inductor Buck-Boost Converter with 1.8A Switches

11.1.3 Development Support

11.1.3.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS40210 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

11.2 Documentation Support

11.2.1 Related Documentation

These references may be found on the web at www.power.ti.com under Technical Documents. Many design tools and links to additional references, may also be found at www.power.ti.com.

- *PowerPAD™ Thermally Enhanced Package*
- *PowerPAD™ Made Easy*
- *AC-DC Non-Isolated SMPS for Single-Phase Smart Meters Based on UCC28722*

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS40210	Click here	Click here	Click here	Click here	Click here

Table 11-2. Related Links (continued)

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS40211	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

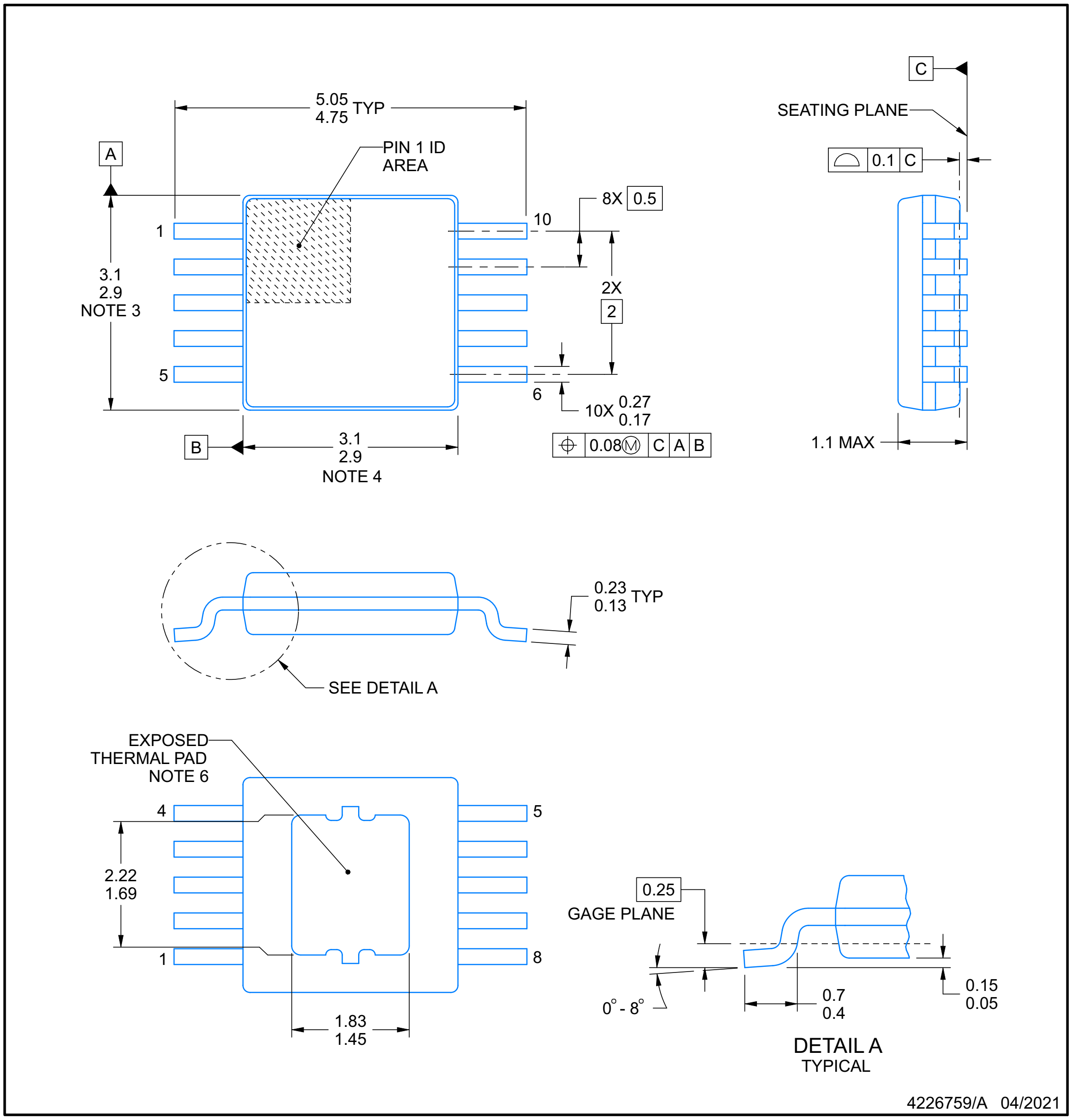
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DGQ0010D-C01

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

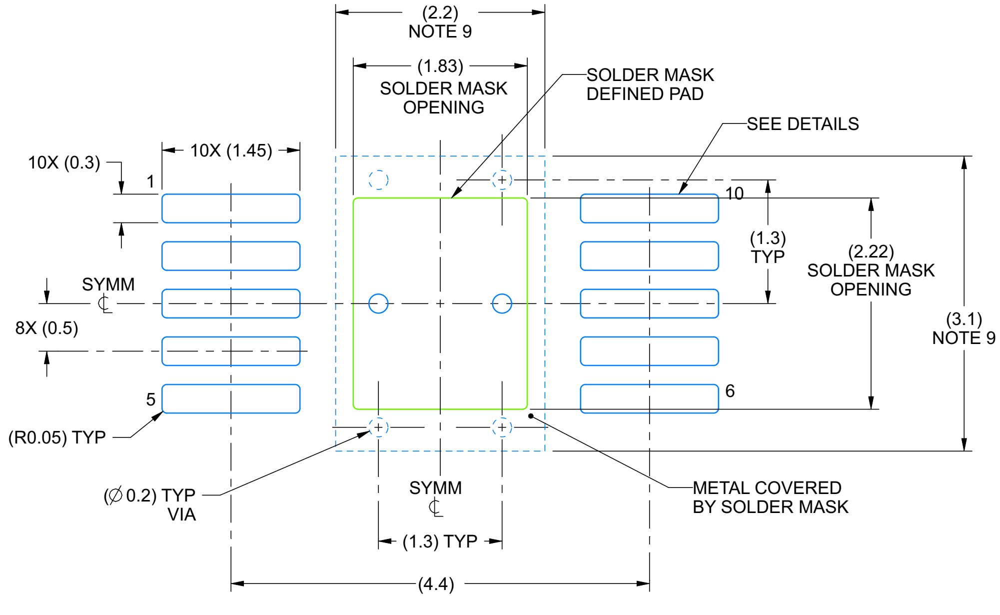
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
6. The thermal pad design could vary depending on manufacturing site.

TEXAS INSTRUMENTS
www.ti.com

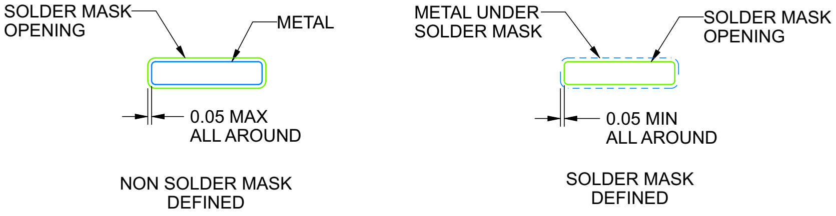
EXAMPLE BOARD LAYOUT

DGQ0010D-C01 **PowerPAD ™ - 1.1 mm max height**

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4226759/A 04/2021

NOTES: (continued)

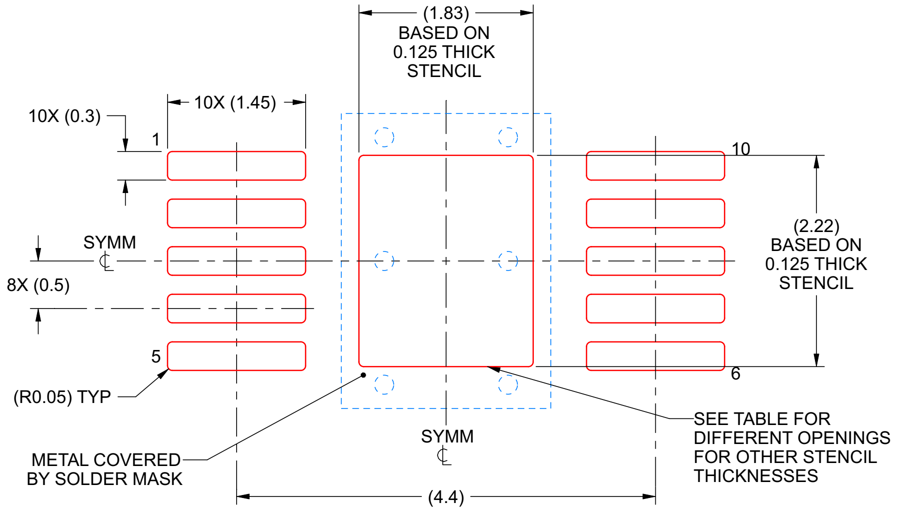
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.

www.ti.com

EXAMPLE STENCIL DESIGN

DGQ0010D-C01 **PowerPAD ™ - 1.1 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.48
0.125	1.83 X 2.22 (SHOWN)
0.150	1.67 X 2.03
0.175	1.55 X 1.88

4226759/A 04/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40210DGQ	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	40210	Samples
TPS40210DGQG4	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	40210	Samples
TPS40210DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	40210	Samples
TPS40210DGQRG4	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	40210	Samples
TPS40210DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4210	Samples
TPS40210DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4210	Samples
TPS40211DGQ	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	40211	Samples
TPS40211DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	40211	Samples
TPS40211DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4211	Samples
TPS40211DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4211	Samples
TPS40211DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4211	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS40210, TPS40211 :

- Automotive : TPS40210-Q1, TPS40211-Q1

- Enhanced Product : TPS40210-EP

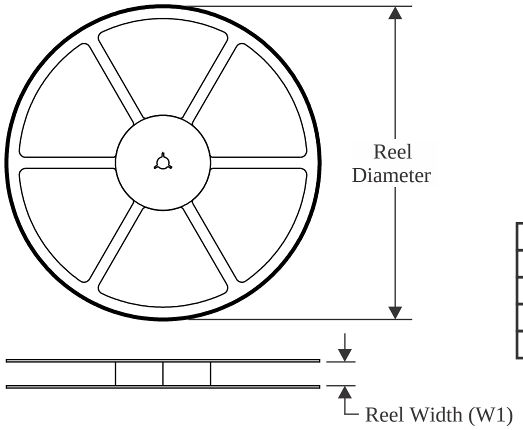
NOTE: Qualified Version Definitions:

  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

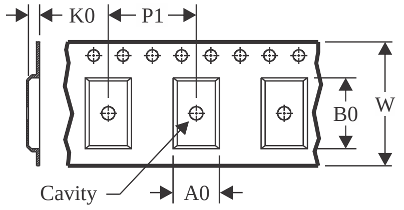
  - Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

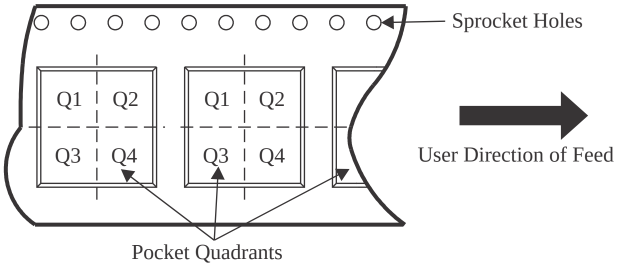


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

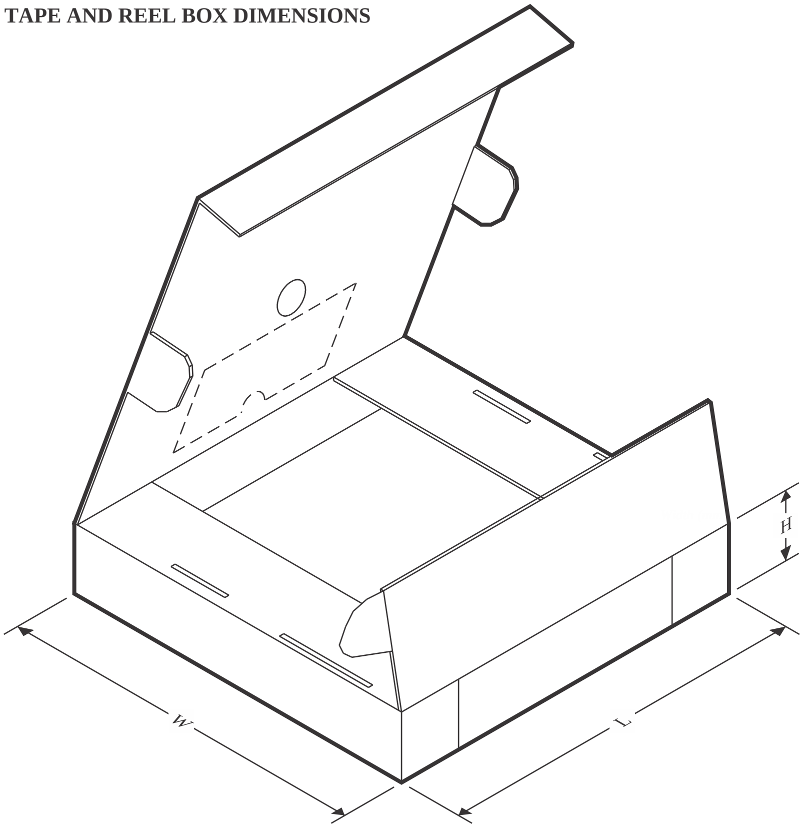
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40210DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TPS40210DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40210DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40211DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS40211DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40211DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

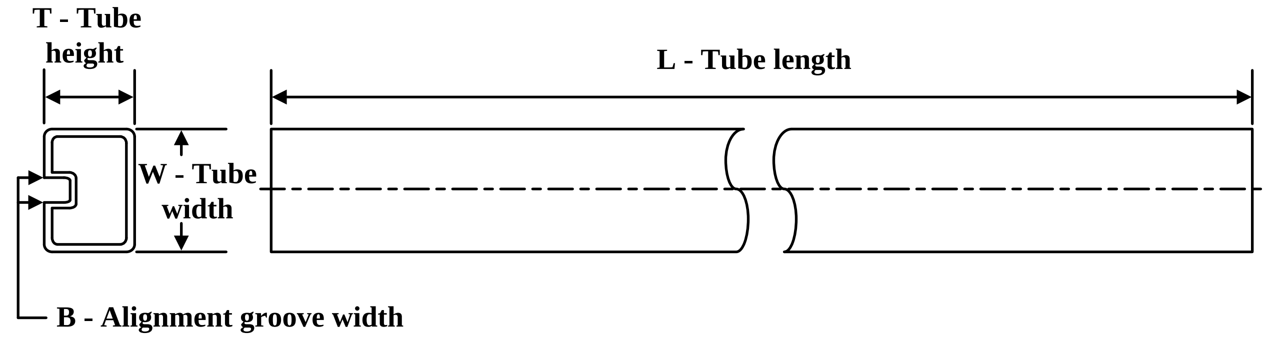
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40210DGQR	HVSSOP	DGQ	10	2500	366.0	364.0	50.0
TPS40210DRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TPS40210DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS40211DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
TPS40211DRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TPS40211DRCT	VSON	DRC	10	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS40210DGQ	DGQ	HVSSOP	10	80	330	6.55	500	2.88
TPS40210DGQ	DGQ	HVSSOP	10	80	322	6.55	1000	3.01
TPS40210DGQG4	DGQ	HVSSOP	10	80	322	6.55	1000	3.01
TPS40210DGQG4	DGQ	HVSSOP	10	80	330	6.55	500	2.88
TPS40211DGQ	DGQ	HVSSOP	10	80	330	6.55	500	2.88
TPS40211DGQ	DGQ	HVSSOP	10	80	322	6.55	1000	3.01

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