3.5V 至 28V 输入电压，1.7A 输出电流，带有集成金属氧化物半导体场效应晶体管 (MOSFET) 的非同步降压稳压器

查询样品: **TPS5402**

特性

- **3.5V** 至 **28V** 的宽输入电压范围
- 高达 **1.7A** 的最大持续输出负载电流
- 脉冲跳跃模式可在轻负载时实现高效率
- 高轻负载效率
- 频率展频以减少电磁干扰 **(EMI)**
- 由一个外部电阻器设定 **50kHz** 至 **1.1MHz** 的可调开关频率
（将引脚 **ROSC** 悬空。 将频率设定在 **120kHz** 并且接地连接至 **70kHz**）
- 频率展频以缓解 **EMI** 问题
- 峰值电流模式控制
- 逐周期过流保护
- 外部软启动
- 采用小外形集成电路 **(SOIC)8** 封装

应用范围

- **5V**，**9V**，**12V** 和 **24V** 分布式电源系统
- 消费类应用，诸如家用电器、机顶盒、**CPE** 设备、**LCD** 显示器、外设、和电池充电器
- 工业用和车载娱乐系统电源

说明

TPS5402 是一款具有宽运行输入电压范围（3.5V 至 28V）的单片非同步降压稳压器。此器件执行内部斜坡补偿的电流模式控制来减少组件数量。

TPS5402 还特有一个轻负载脉冲跳跃模式，此特性可在轻负载时减少为系统供电的输入电源的功率损失。

可使用一个外部电阻器将此转换器的开关频率设定在 50kHz 至 1.1MHz 之间。 引入了频率展频操作以减少 EMI。

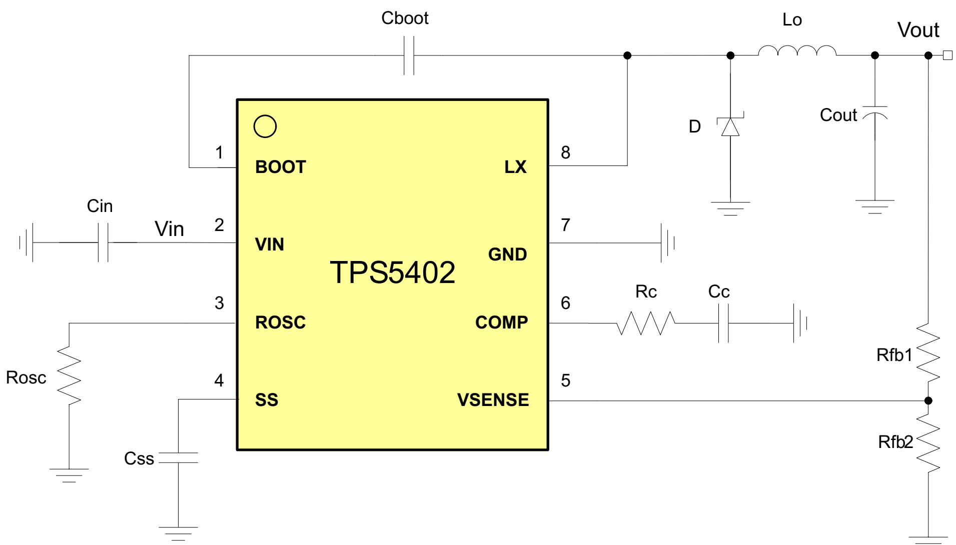
具有频率折返功能的逐周期电流限制在过载情况下保护集成电路 (IC)。

English Data Sheet: SLVSBK4

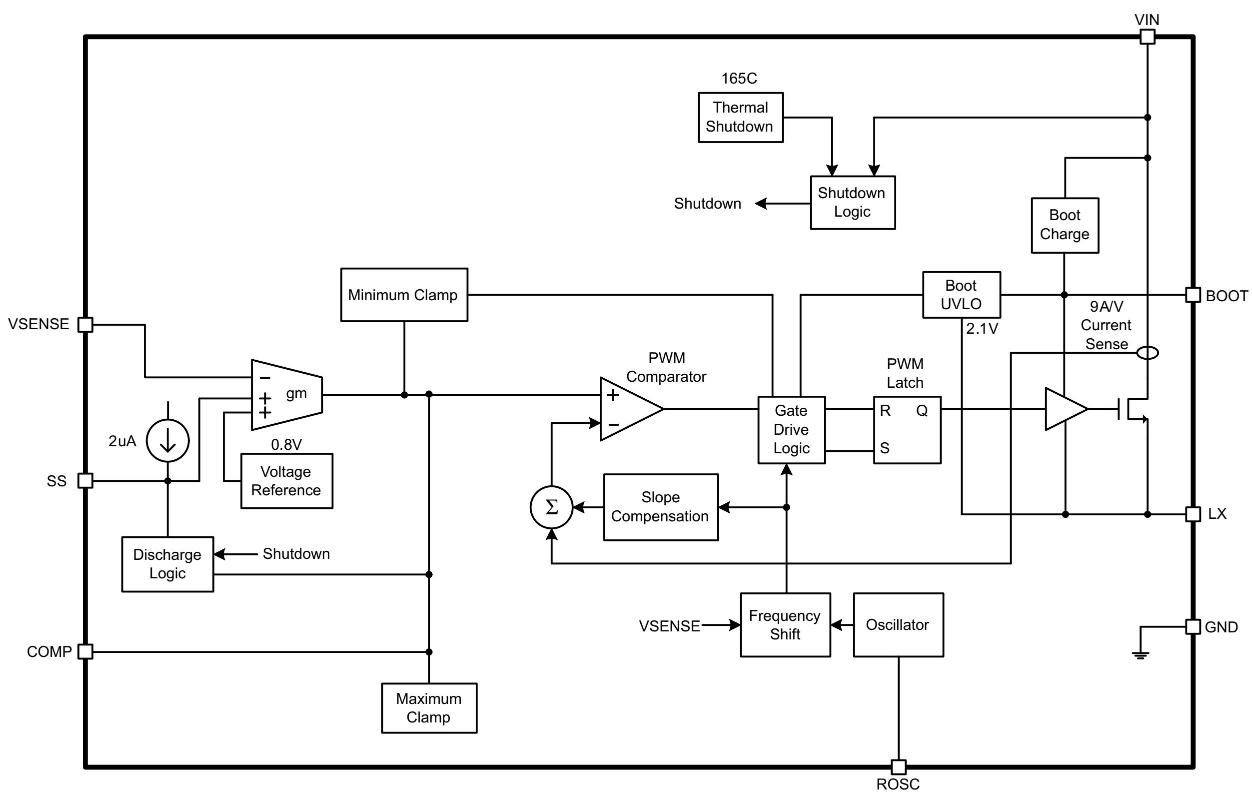
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

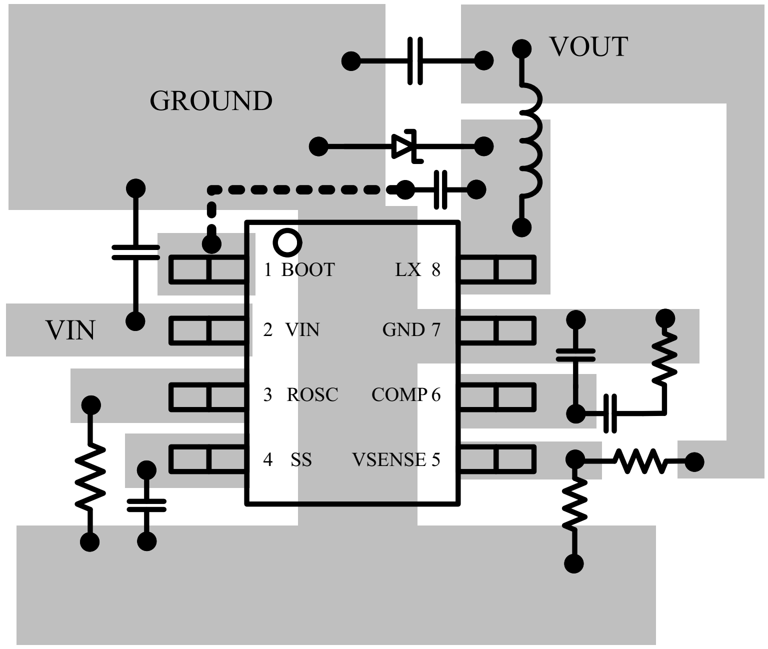
TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



PCB LAYOUT

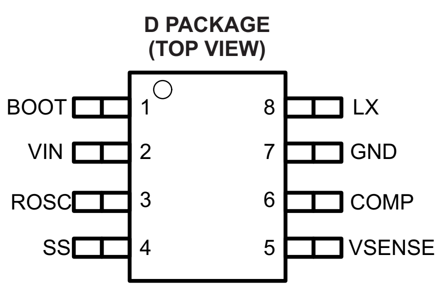


ORDERING INFORMATION[1]

T_A	PACKAGE[2]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	8-pin SOIC (D)	TPS5402DR	TPS5402

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN OUT



TERMINAL FUNCTIONS

NAME	NO.	DESCRIPTION
BOOT	1	A 0.1-µF bootstrap capacitor is required between BOOT and LX.
VIN	2	Input supply voltage, 3.5 V to 28 V
ROSC	3	Switching frequency program pin. Connect a resistor to this pin to set the switching frequency. Connect the pin to ground for a default 70-kHz switching frequency. Leave the pin open for 120-kHz switching frequency.
SS	4	Soft start pin. An external capacitor connected to this pin sets the output rise time.
VSENSE	5	Output voltage feedback pin
COMP	6	Error amplifier output and input to the PWM comparator. Connect frequency compensation components to this pin.
GND	7	Ground
LX	8	Switching node to external inductor

ABSOLUTE MAXIMUM RATINGS [1]

over operating free-air temperature range (unless otherwise noted)

	Voltage range at VIN, LX	–0.3 to 30	V
	Voltage range at LX (maximum withstand voltage transient < 20 ns)	–5 to 30	V
	Voltage from BOOT to LX	–0.3 to 7	V
	Voltage at VSENSE	–0.3 to 7	V
	Voltage at SS	–0.3 to 3	V
	Voltage at ROSC	–0.3 to 3	V
	Voltage at COMP	–0.3 to 3	V
	Voltage at GND	–0.3 to 0.3	V
T_J	Operating junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	3.5		28	V
T_A	Ambient temperature	–40		85	°C

THERMAL INFORMATION

THERMAL METRIC[1]		TPS5402 D 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	116.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	62.4	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	57.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	14.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	56.5	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	°C/W

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA} 。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input Voltage range		3.5		28	V
IDD_{Q_nsw}	Non switching quiescent power supply current	V_{SENSE} > 0.9 V		100		µA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}		3.5		V
		Hysteresis		200		mV
FEEDBACK AND ERROR AMPLIFIER						
V_{SENSE}	Regulated output voltage	V_{IN} = 12 V	0.776	0.8	0.824	V
G_{m_EA}	Error amplifier trans-conductance	-2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		92		µs
I_{gm}	Error amplifier source/sink current	V_{COMP} = 1 V, 100 mV overdrive		±7		µA
G_{m_SRC}	COMP voltage to inductor current Gm	V_{IN} = 12 V		9		A/V
PFM MODE AND SOFT-START						
I_{th}	Pulse skipping mode switch current threshold			300		mA
I_{SS}	Charge current			2		µA
OSCILLATOR						
f_{SW_BK}	Switching frequency range	Set by external resistor ROSC	50		1100	kHz
f_{SW}	Programmable frequency	ROSC = GND		70		kHz
		ROSC = OPEN		120		
		ROSC = 85.5 kΩ		300		
f_{jitter}	Frequency spread spectrum in percentage of f_{SW}	V_{IN} = 12 V		±6		%
f_{swing}	Jittering swing frequency in percentage of f_{SW}	V_{IN} = 12 V		1/512		
t_{min_on}	Minimum on time	V_{IN} = 12 V, T_A = 25°C		200		ns
D_{max}	Maximum duty ratio	V_{IN} = 12 V		93		%
CURRENT LIMIT						
I_{LIMIT}	Peak inductor current limit	V_{IN} = 12 V	2.2	2.5	3.1	A
MOSFET ON-RESISTANCE						
R_{dson_HS}	On resistance of high side FET	V_{IN} = 12 V		120	240	mΩ
THERMAL SHUTDOWN						
T_{TRIP}	Thermal protection trip point	Rising temperature		165		°C

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 120 kHz (unless otherwise noted)

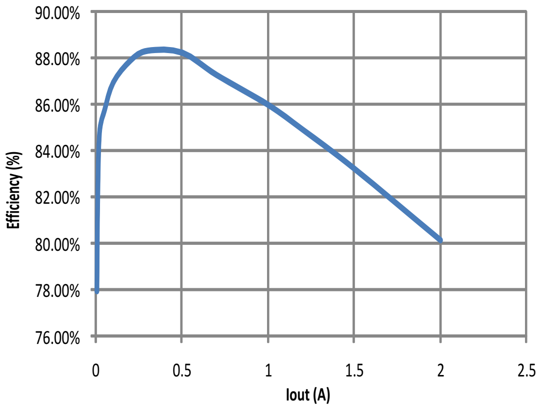


Figure 1. Efficiency
V_{IN} = 12 V, V_{OUT} = 3.3 V

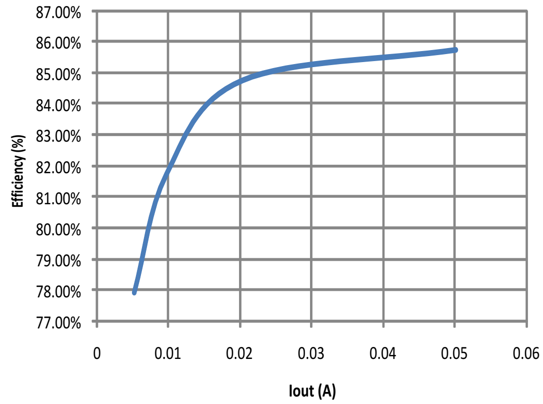


Figure 2. Efficiency
V_{IN} = 12 V, V_{OUT} = 3.3 V

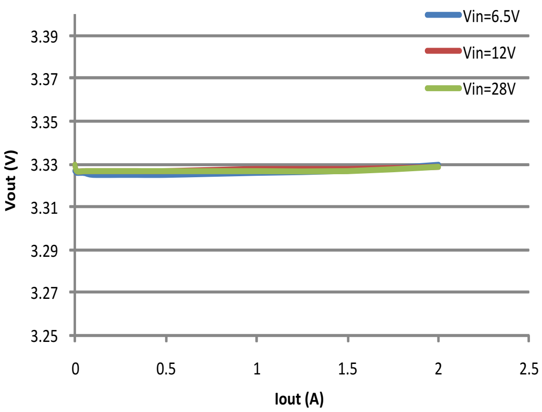


Figure 3. Load Regulation
V_{IN} = 12 V, V_{OUT} = 3.3 V

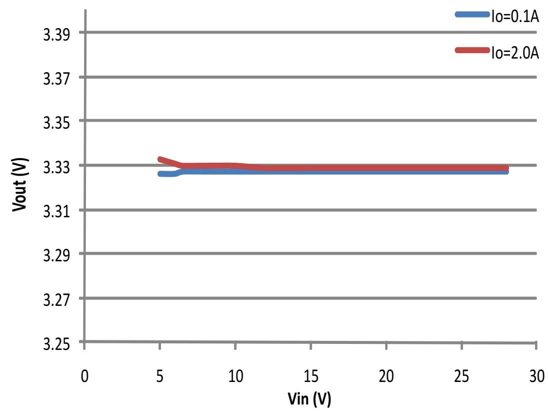


Figure 4. Line Regulation
V_{OUT} = 3.3 V

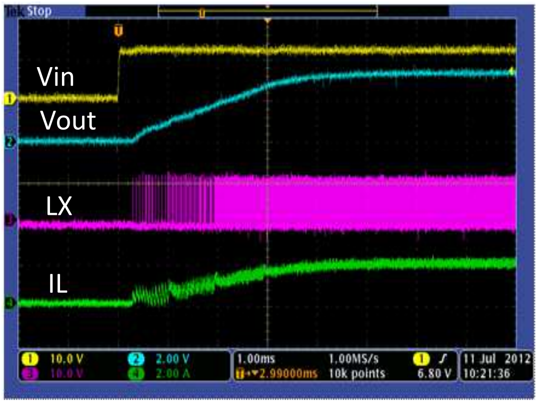


Figure 5. Startup
2-A Preset Loading

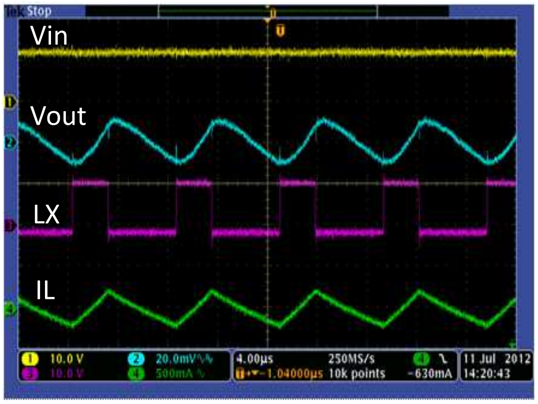


Figure 6. Steady State
I_O = 2 A

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 120 kHz (unless otherwise noted)

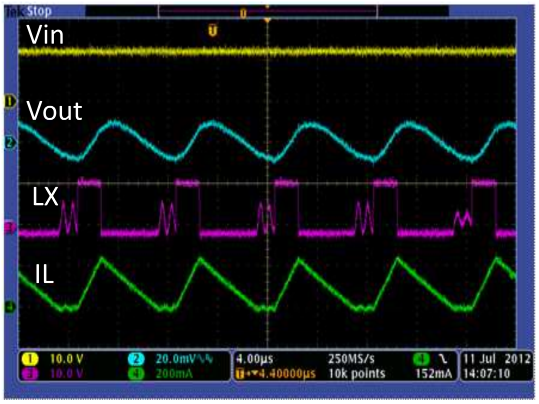


Figure 7. Steady State
I_O = 100 mA

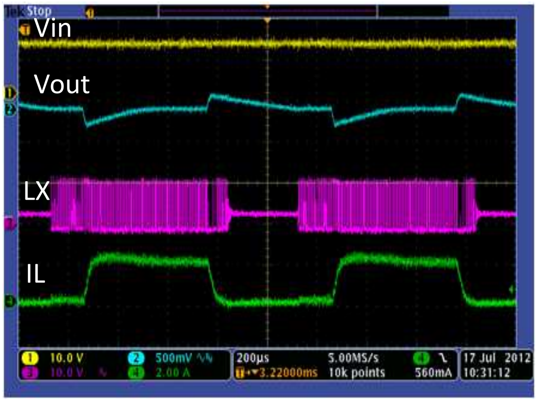


Figure 8. Load Transient
I_O = 0.1 A to 2 A

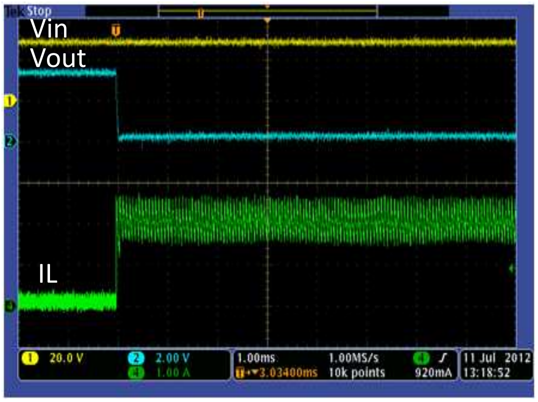


Figure 9. Short Circuit Protection

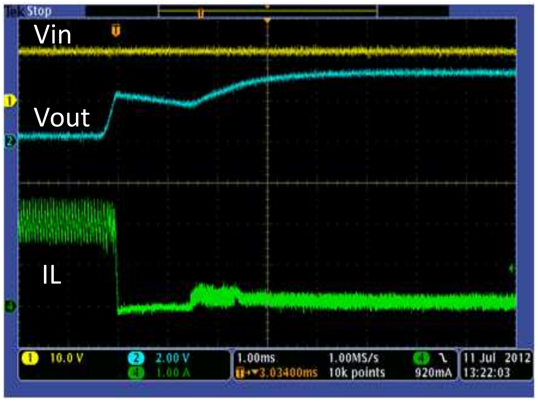


Figure 10. Short Circuit Recovery

OVERVIEW

The TPS5402 is a 28-V, 1.7-A, step-down (buck) converter with an integrated high-side N-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The TPS5402's switching frequency is adjustable with an external resistor or fixed by connecting the frequency program pin to GND or leaving it unconnected.

The TPS5402 starts switching at V_{IN} equal to 3.5 V. The operating current is 100 μA typically when not switching and under no load. When the device is disabled, the supply current is 1 μA typically.

The integrated 120-mΩ high-side MOSFET allows for high efficiency power supply designs with continuous output currents up to 1.7 A.

The TPS5402 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically.

By adding an external capacitor, the slow start time of the TPS5402 can be adjustable which enables flexible output filter selection. To improve the efficiency at light load conditions, the TPS5402 enters a special pulse skipping mode when the peak inductor current drops below 300 mA typically. The frequency foldback reduces the switching frequency during startup and over current conditions to help control the inductor current. The thermal shut down gives the additional protection under fault conditions.

DETAILED DESCRIPTION

Adjustable Frequency PWM Control

The TPS5402 uses an external resistor to adjust the switching frequency. Connecting the ROSC pin to ground fixes the switching frequency at 70 kHz, leaving it open gives 120-kHz switching frequency.

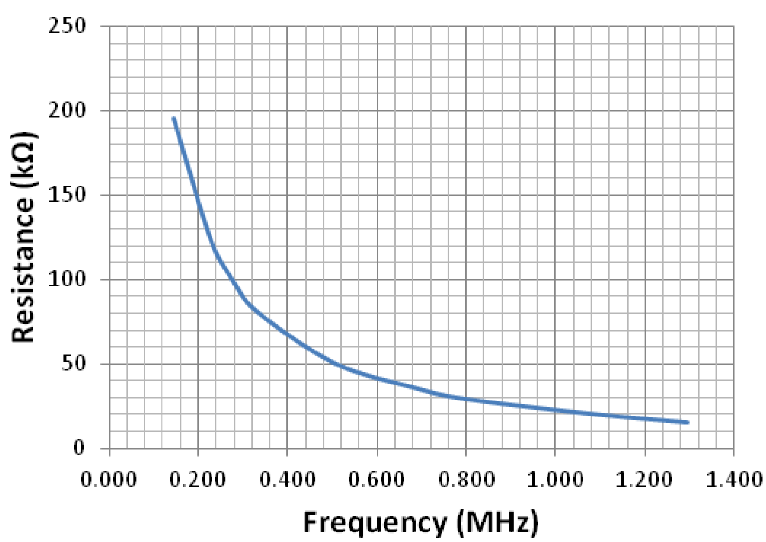


Figure 11. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 21.82 \cdot f_{SW}^{-1.167} \quad (1)$$

For operation at 300 kHz, an 85.5-kΩ resistor is required.

Pulse Skipping Mode

The TPS5402 is designed to operate in pulse skipping mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 300 mA typically, the COMP pin voltage falls to 0.5 V typically and the device enters pulse skipping mode. When the device is in pulse skipping mode, the COMP pin voltage is clamped at 0.5 V internally which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 300 mA for the COMP pin voltage to rise above 0.5 V and exit pulse skipping mode. Since the integrated current comparator catches the peak inductor current only, the average load current entering pulse skipping mode varies with the applications and external output filters.

Voltage Reference (V_{SENSE})

The voltage reference system produces a ±3% accuracy voltage reference by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8 V.

Bootstrap Voltage (BOOT)

The TPS5402 has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and LX pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS5402 is designed to operate at 100% duty cycle as long as the BOOT to LX pin voltage is greater than 2.1 V typically.

Programmable Slow Start Using SS Pin

It is recommended to program the slow start time externally because no slow start time is implemented internally. The TPS5402 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power supply's reference voltage fed into the error amplifier and will regulate the output accordingly. A capacitor (C_{SS}) on the SS pin to ground implements a slow start time. The TPS5402 has an internal pull-up current source of 2 µA that charges the external slow start capacitor. The equation for the slow start time (10% to 90%) is shown in Equation 2. The internal V_{ref} is 0.8 V and the I_{SS} current is 2 µA.

$$t_{ss}(ms) = \frac{C_{ss}(nF) \times V_{ref}(V)}{I_{ss}(\mu A)} \tag{2}$$

The slow start time should be set between 1 ms to 10 ms to ensure good start-up behavior. The slow start capacitor should be no more than 27 nF.

If during normal operation, the input voltage drops below the VIN UVLO threshold, or a thermal shutdown event occurs, the TPS5402 stops switching.

Error Amplifier

The TPS5402 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 µA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

Slope Compensation

To prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS5402 adds a built-in slope compensation which is a compensating ramp to the switch current signal.

Overcurrent Protection and Frequency Shift

The TPS5402 implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Every cycle the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limits the output current.

The TPS5402 provides robust protection during short circuits. There is potential for overcurrent runaway in the output inductor during a short circuit at the output. The TPS5402 solves this issue by increasing the off time during short circuit conditions by lowering the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on the VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is shown in Table 1.

Table 1. Switching Frequency Conditions

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
f_{SW}	$V_{SENSE} \geq 0.6$ V
$f_{SW}/2$	0.6 V > $V_{SENSE} \geq 0.4$ V
$f_{SW}/4$	0.4 V > $V_{SENSE} \geq 0.2$ V
$f_{SW}/8$	0.2 V > V_{SENSE}

Spread Spectrum

In order to reduce EMI, TPS5402 introduces frequency spread spectrum. The jittering span is ±6% of the switching frequency with 1/512 swing frequency.

Overvoltage Transient Protection

The TPS5402 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × V_{ref}, the high-side MOSFET will be forced off. When the VSENSE pin voltage falls below 107% × V_{ref}, the high-side MOSFET will be enabled again.

Inductor Selection

The higher operating frequency allows the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of switching loss and MOSFET gate charge losses. In addition to this basic trade-off, the effect of the inductor value on ripple current and low current operation must also be considered. The ripple current depends on the inductor value. The inductor ripple current (i_L) decreases with higher inductance or higher frequency and increases with higher input voltage (V_{IN}). Accepting larger values of i_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

To calculate the value of the output inductor, use Equation 3. LIR is a coefficient that represents inductor peak-to-peak ripple to DC load current. It is recommended to set LIR to 0.1 ~ 0.3 for most applications.

Actual core loss of the inductor is independent of core size for a fixed inductor value, but it is very dependent on the inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. It results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. It is important that the RMS current and saturation current ratings are not exceeding the inductor specification. The RMS and peak inductor current can be calculated from Equation 5 and Equation 6.

$$L = \frac{V_{IN} - V_{OUT}}{I_O \cdot LIR} \cdot \frac{V_{OUT}}{V_{IN} \cdot fsw} \quad (3)$$

$$\Delta i_L = \frac{V_{IN} - V_{OUT}}{I_O} \cdot \frac{V_{OUT}}{V_{IN} \cdot fsw} \quad (4)$$

$$i_{LRMS} = \sqrt{I_O^2 + \frac{\left(\frac{V_{OUT} \cdot (V_{INmax} - V_{OUT})}{V_{INmax} \cdot L \cdot fsw}\right)^2}{12}} \quad (5)$$

$$I_{Lpeak} = I_O + \frac{\Delta i_L}{2} \quad (6)$$

For this design example, use LIR = 0.3 and the inductor is calculated to be 5.40 µH with V_{IN} = 12 V. Choose 4.7 µH value for the standard inductor and the peak to peak inductor ripple is about 34% of 1-A DC load current.

Output Capacitor Selection

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

Equation 7 gives the minimum output capacitance to meet the transient specification. For this example, L = 4.7 µH, ΔI_{OUT} = 1 A – 0.0 A = 1 A and ΔV_{OUT} = 500 mV (10% of regulated 5 V). Using these numbers gives a minimum capacitance of 1 µF. A standard 22-µF ceramic is chosen in the design.

$$Co > \frac{\Delta I_{OUT}{}^2 \cdot L}{2 \cdot V_{OUT} \cdot \Delta V_{OUT}} \quad (7)$$

The selection of C_O is driven by the effective series resistance (ESR). Equation 8 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, ΔV_{OUT} is the maximum allowable output voltage ripple, and Δi_L is the inductor ripple current. In this case, the maximum output voltage ripple is 50 mV (1% of regulated 5 V). From Equation 4, the output current ripple is 1 A. From Equation 8, the minimum output capacitance meeting the output voltage ripple requirement is 2.5 µF with 3-mΩ ESR resistance.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{\Delta V_{OUT}}{\Delta i_L} - ESR} \quad (8)$$

After considering both requirements, for this example, one 22-µF, 6.3-V X7R ceramic capacitor with 3-mΩ ESR should be used.

Input Capacitor Selection

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in Equation 9. For this example, I_{OUT} = 1 A, V_{OUT} = 5 V, minimum V_{INmin} = 9.6 V, from Equation 9, the input capacitors must support a ripple current of 1-A RMS.

$$I_{INRMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{INmin}} \cdot \frac{(V_{INmin} - V_{OUT})}{V_{INmin}}} \quad (9)$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, I_{OUTmax} = 1 A, C_{IN} = 10 µF, f_{SW} = 300 kHz, yields an input voltage ripple of 83 mV.

$$\Delta V_{IN} = \frac{I_{OUTmax} \cdot 0.25}{C_{IN} \cdot f_{SW}} \quad (10)$$

To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 165°C, the device reinitiates the power up sequence.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5402DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T5402	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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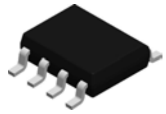
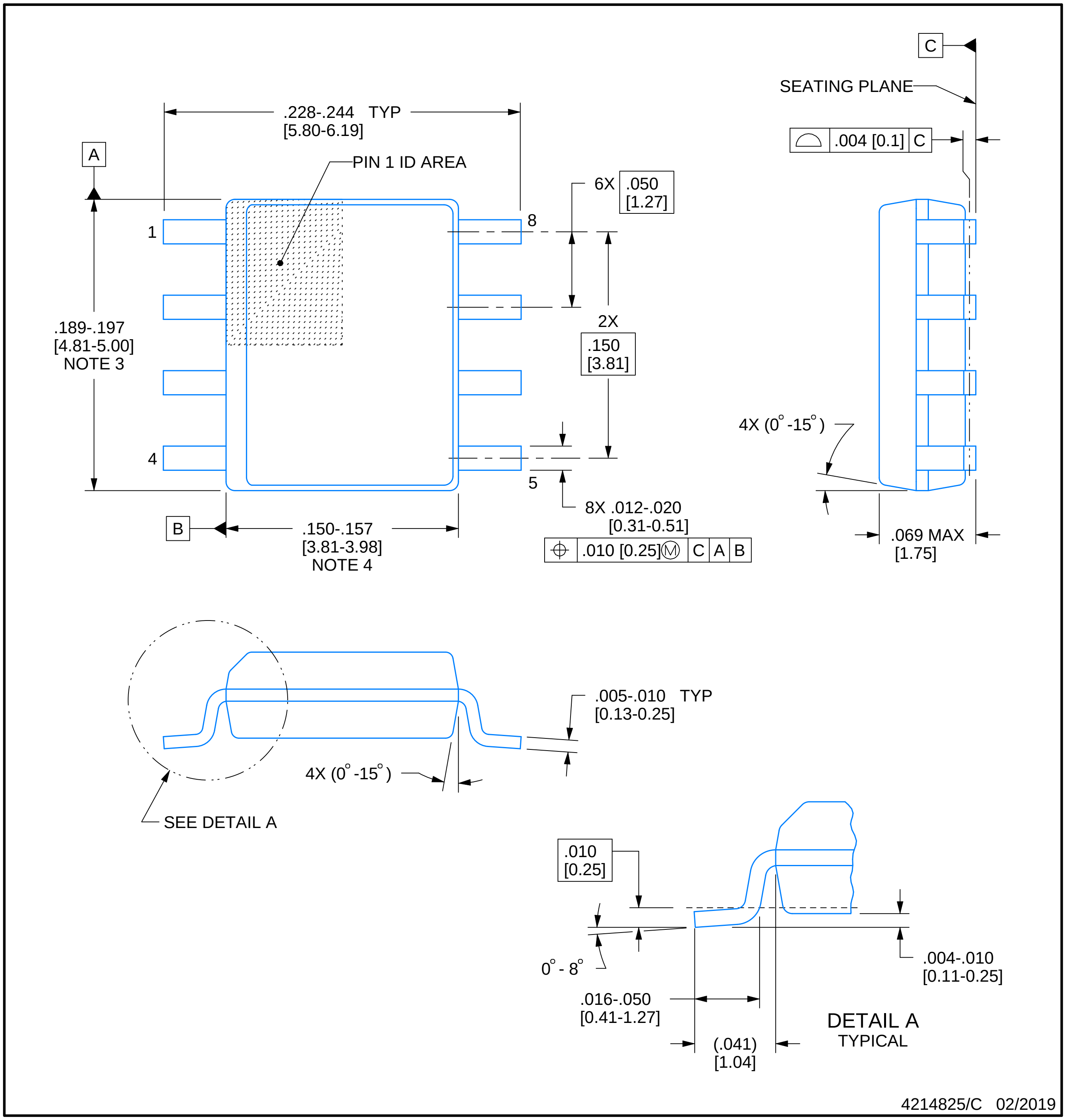


PACKAGE OUTLINE

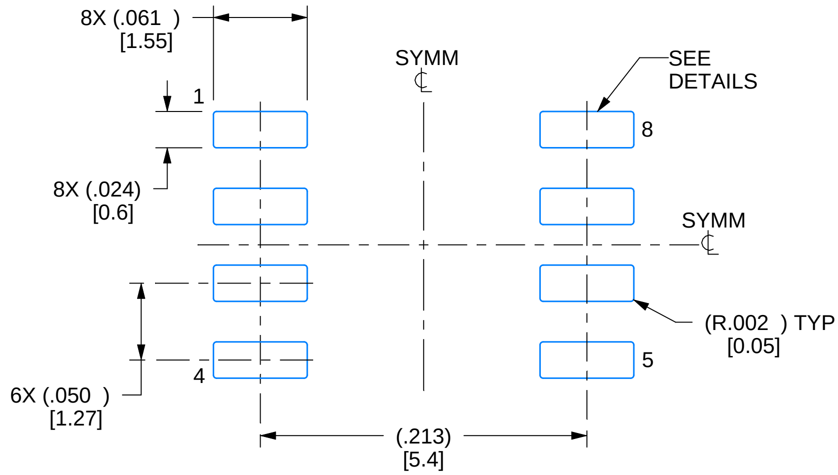
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

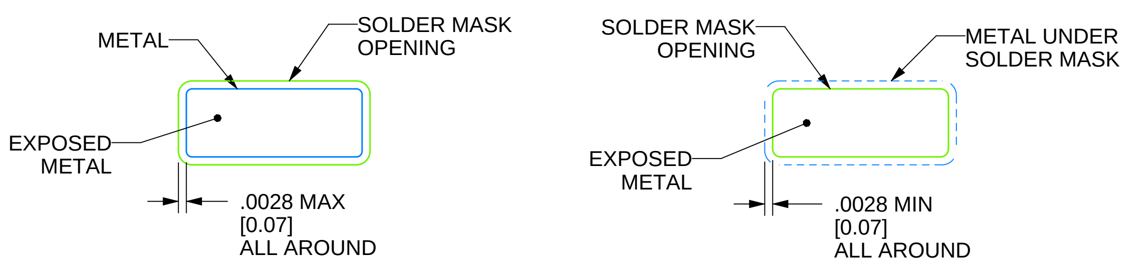


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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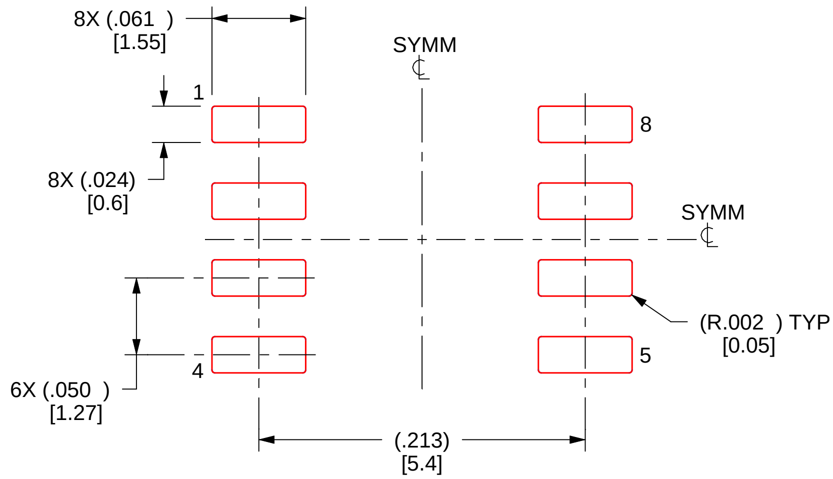
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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