具有集成场效应晶体管 (FET) 的 4.5V 至 18V 输入，4A 输出的单通道同步降压转换开关 (SWIFT™)

查询样品: **TPS54427**

特性

- **D-CAP2™** 模式支持快速瞬态响应
- 低输出纹波，支持陶瓷输出电容器
- 宽泛的 V_{IN}输入电压范围：**4.5V** 至 **18V**
- 输出电压范围：**0.76V** 至 **7.0V**
- 高效率集成型场效应晶体管 **(FET)** 针对较低占空比应用进行了优化 **-70mΩ**（高侧）与 **53mΩ**（低侧）
- 关断时的高效率，流耗不足 **10μA**
- 高初始带隙基准精度
- 可调软启动
- 预偏置软启动
- **650kHz** 开关频率 **(f_{SW})**
- 逐周期过流限制

应用范围

- 低电压系统的广泛应用
  - 数字电视电源
  - 高清 **Blu-ray Disc™** 播放器
  - 网络家庭终端设备
  - 数字机顶盒 **(STB)**

说明

TPS54427 是一款自适应接通时间 D-CAP2™ 模式同步降压转换器。 TPS54427 可帮助系统设计人员通过成本有效性、低组件数量、低待机电流解决方案来完成多种终端设备的电源总线调节器集。

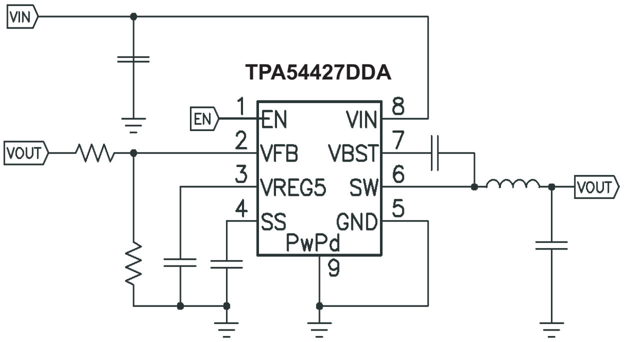
TPS54427 的主控制环路采用 D-CAP2™ 模式控制，无需外部补偿组件便可实现极快的瞬态响应。

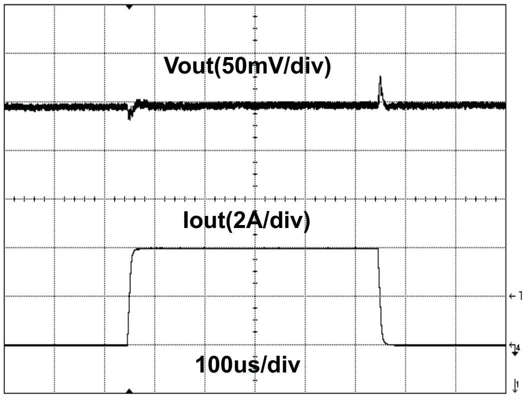
TPS54427 的专有电路还使该器件可采用诸如高分子有机半导体固体电容器 (POSCAP) 或高分子聚合物电容器 (SP-CAP) 等低等效串联电阻 (ESR) 输出电容器，以及超低 ESR 陶瓷电容器。

该器件的工作输入电压介于 4.5V 至 18V 之间。 可在 0.76V 至 7V 之间设定输出电压。

此器件还特有一个可调软启动时间。

TPS54427 采用 8 引脚 DDA 封装和 10 引脚 DRC 封装，被设计成在 –40°C 到 85°C 的温度范围内运行。





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Blu-ray Disc is a trademark of Blu-ray Disc Association.

English Data Sheet: SLVSB43

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA
–40°C to 85°C	DDA	TPS54427DDA	8	Tube
		TPS54427DDAR		Tape and Reel
	DRC	TPS54427DRCT	10	Tape and Reel
		TPS54427DRCR		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VIN, EN	–0.3	20	V
	VBST	–0.3	26	V
	VBST (10 ns transient)	–0.3	28	V
	VBST (vs SW)	–0.3	6.5	V
	VFB, SS	–0.3	6.5	V
	SW	–2	20	V
	SW (10 ns transient)	–3	22	V
Output voltage range	VREG5	–0.3	6.5	V
	GND	–0.3	0.3	V
Voltage from GND to thermal pad, V_{diff}		–0.2	0.2	V
Electrostatic discharge	Human Body Model (HBM)		2	kV
	Charged Device Model (CDM)		500	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54427		UNITS
		DDA (8 PINS)	DRC (10-PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	42.1	43.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	50.9	53.8	
θ_{JB}	Junction-to-board thermal resistance	31.8	18.2	
ψ_{JT}	Junction-to-top characterization parameter	5	0.6	
ψ_{JB}	Junction-to-board characterization parameter	13.5	18.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	7.1	4.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	18	V
V_I	Input voltage range	VBST	–0.1	24	V
		VBST (10 ns transient)	-0.1	27	
		VBST(vs SW)	–0.1	6	
		SS	–0.1	5.7	
		EN	–0.1	18	
		VFB	–0.1	5.5	
		SW	–1.8	18	
		SW (10 ns transient)	–3	21	
		GND	–0.1	0.1	
V_O	Output voltage range	VREG5	–0.1	5.7	V
I_O	Output Current range	I_{VREG5}	0	10	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		950	1400	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.0	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, continuous mode mode	757	765	773	mV
		T_A = –40°C to 85°C, V_O = 1.05 V, continuous mode mode(1)	751	765	779	
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6.0 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
V_{LN5}	Line regulation	6 V < V_{IN} < 18 V, I_{VREG5} = 5 mA			25	mV
V_{LD5}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	Output current	V_{IN} = 6 V, V_{REG5} = 4.0 V, T_A = 25°C		60		mA
MOSFET						
$R_{DS(on)h}$	High side switch resistance (DDA)	25°C, V_{BST} - SW = 5.5 V		70		mΩ
	High side switch resistance (DRC)			74		
$R_{DS(on)l}$	Low side switch resistance	25°C		53		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	L out = 1.5 µH (1)	4.6	5.3	6.8	A

(1) Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

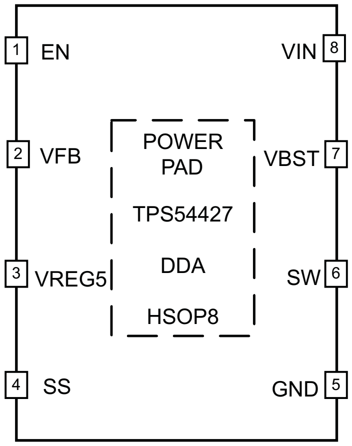
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(2)		170		°C
		Hysteresis(2)		35		
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260	310	ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 1 V	4.2	6.0	7.8	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
UVLO						
UVLO	UVLO threshold	Wake up V_{REG5} voltage	3.45	3.75	4.05	V
		Hysteresis V_{REG5} voltage	0.19	0.32	0.45	

(2) Not production tested.

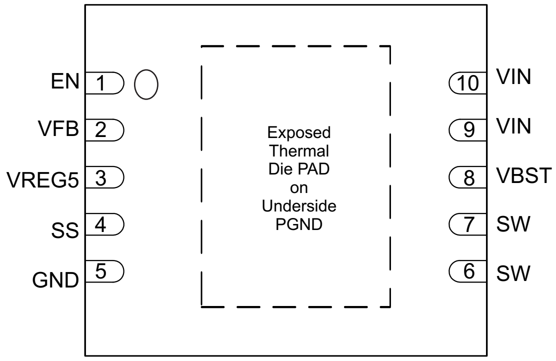
DEVICE INFORMATION

DEVICE INFORMATION

DDA PACKAGE
(TOP VIEW)



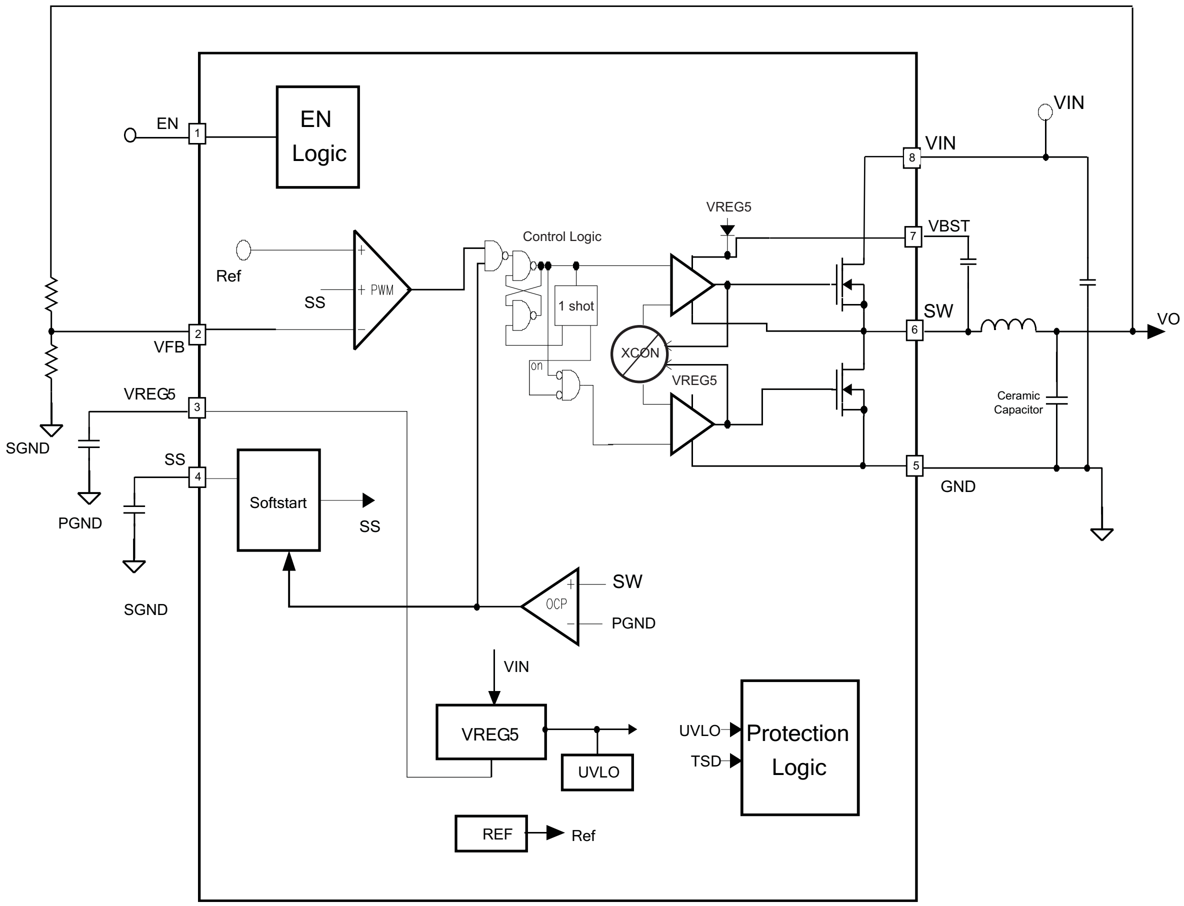
DRC PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN			DESCRIPTION
NAME	DDA	DRC	
EN	1	1	Enable input control. Active high and must be pulled up to enable the device.
VFB	2	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	3	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	6, 7	Switch node connection between high-side NFET and low-side NFET.
VBST	7	8	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	9, 10	Input voltage supply pin.
Exposed Thermal Pad	Back side		Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.
		Back side	Thermal pad of the package. PGND power ground return of internal low-side FET. Must be soldered to achieve appropriate dissipation.

FUNCTIONAL BLOCK DIAGRAM



OVERVIEW

The TPS54427 is a 4-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54427 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54427 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54427 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6-uA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 6-μA.

$$\mathrm{Tss(ms)} = \frac{\mathrm{C6(nF)} \times V f b \times 1.1}{\mathrm{Iss}(\mu \mathrm{A})} = \frac{\mathrm{C6(nF)} \times 0.765 \times 1.1}{6} \qquad (1)$$

The TPS54427 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. The TPS54427 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the over current condition is removed, the output voltage will return to the regulated value. This protection is non-latching.

UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54427 is shut off. This protection is non-latching.

Thermal Shutdown

TPS54427 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 170°C), the device is shut off. This is non-latch protection.

TYPICAL CHARACTERISTICS

VIN = 12 V, T_A = 25°C (unless otherwise noted)

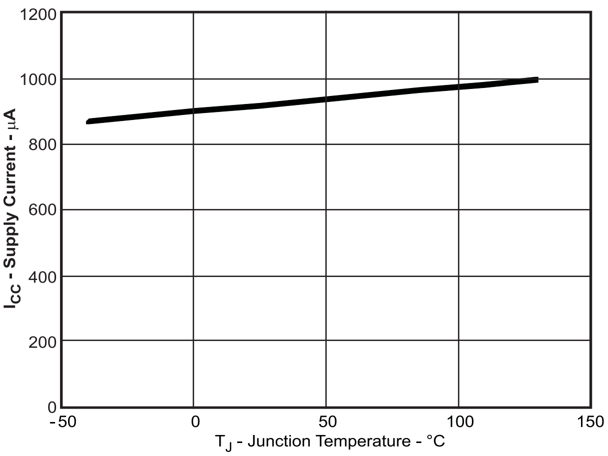


Figure 1. VIN CURRENT vs JUNCTION TEMPERATURE

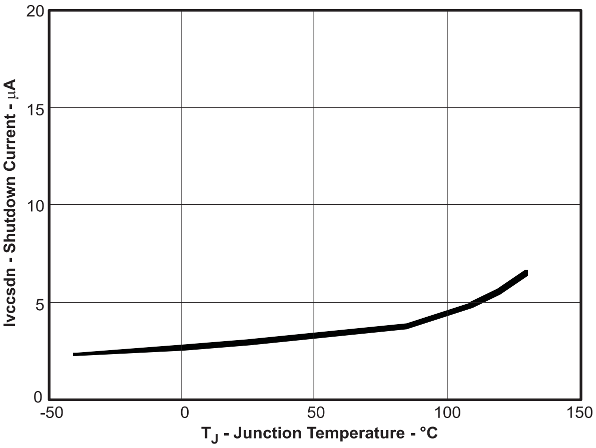


Figure 2. VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

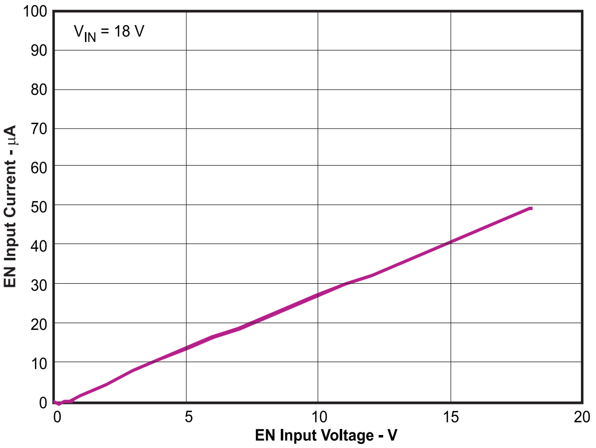


Figure 3. EN CURRENT vs EN VOLTAGE

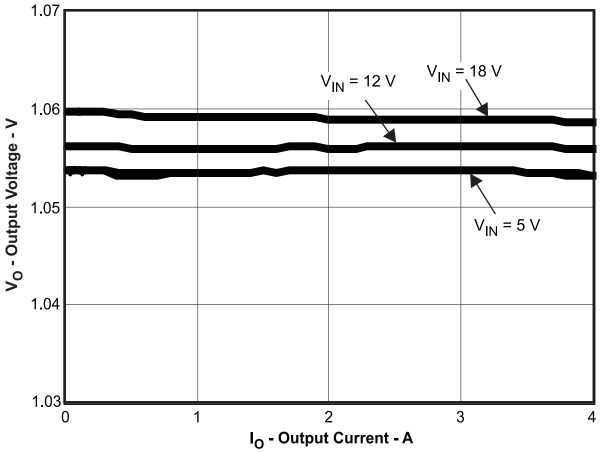


Figure 4. 1.05V OUTPUT VOLTAGE vs OUTPUT CURRENT

TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, T_A = 25°C (unless otherwise noted)

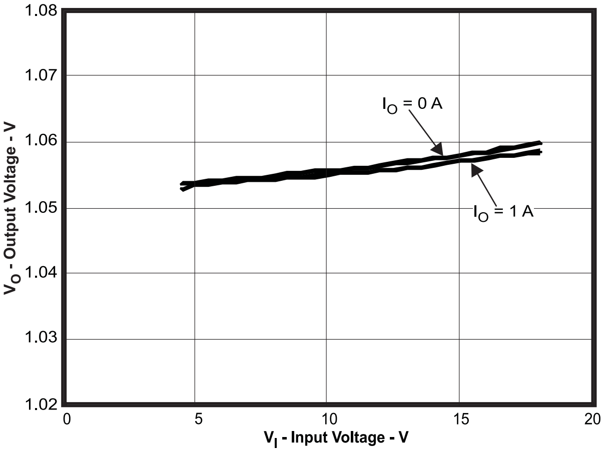


Figure 5. 1.05V OUTPUT VOLTAGE vs VIN VOLTAGE

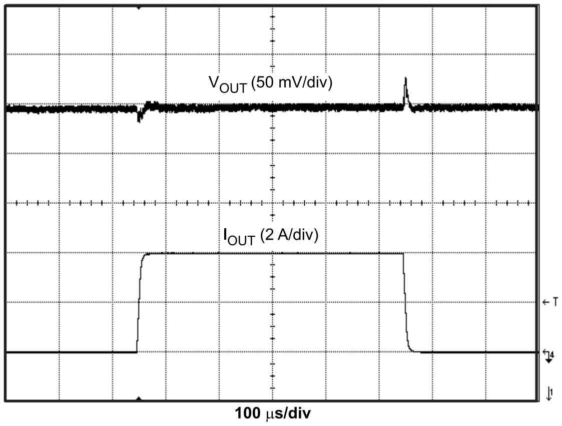


Figure 6. 1.05V 0A to 4-A LOAD TRANSIENT RESPONSE

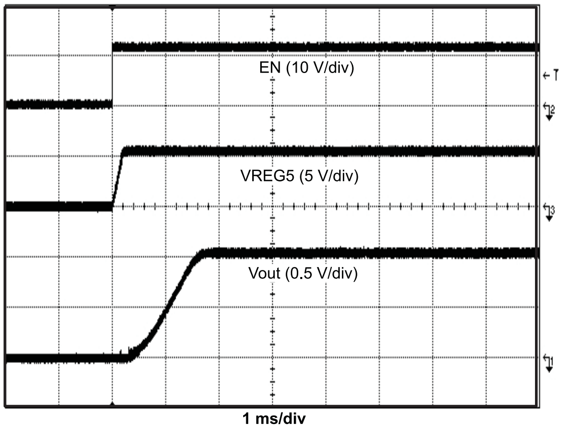


Figure 7. START UP WAVE FORM

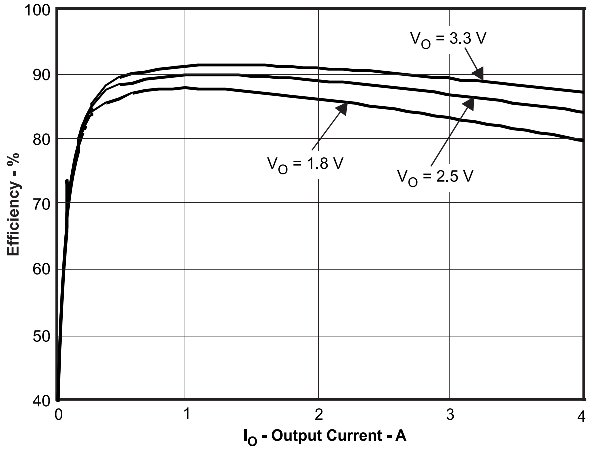


Figure 8. EFFICIENCY vs OUTPUT CURRENT

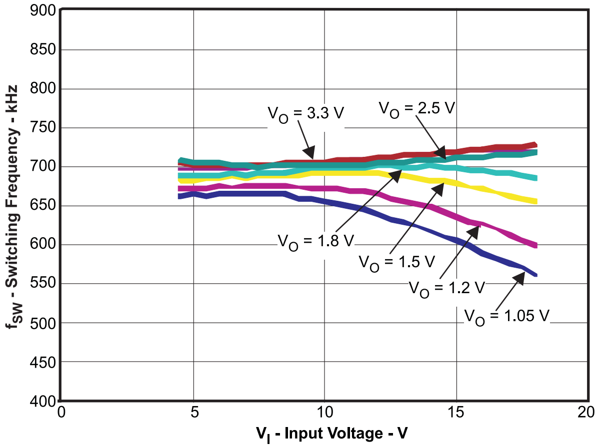


Figure 9. SWITCHING FREQUENCY vs INPUT VOLTAGE

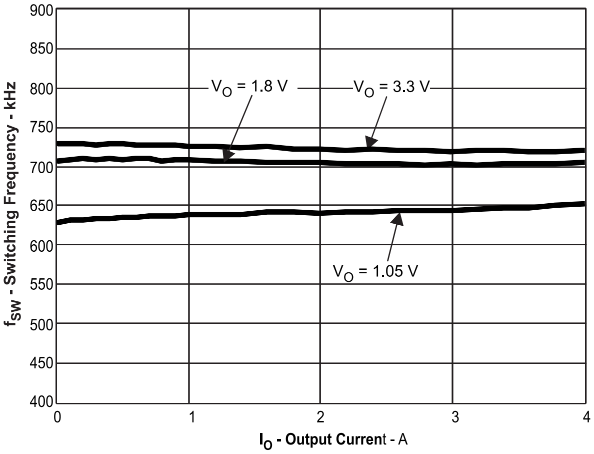


Figure 10. SWITCHING FREQUENCY vs OUTPUT CURRENT

TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, T_A = 25°C (unless otherwise noted)

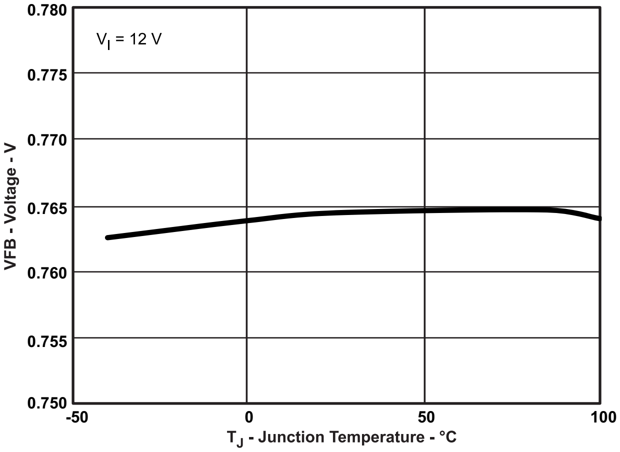


Figure 11. VFB VOLTAGE vs JUNCTION TEMPERATURE

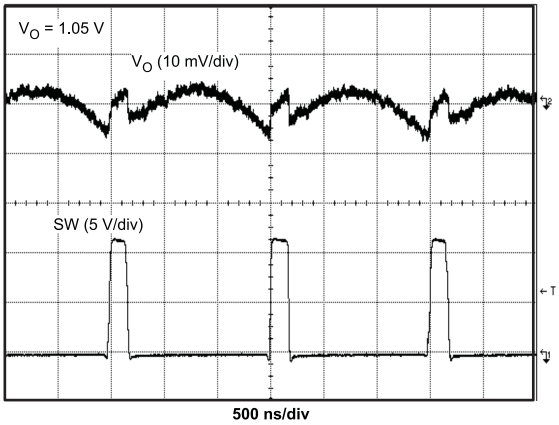


Figure 12. VOLTAGE RIPPLE AT OUTPUT (I_O = 4A)

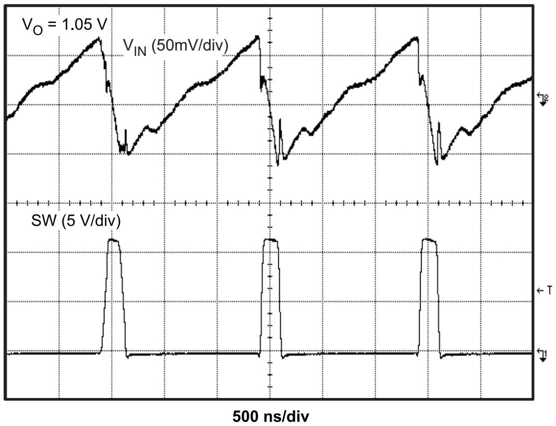


Figure 13. VOLTAGE RIPPLE AT INPUT (I_O = 4A)

DESIGN GUIDE

Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

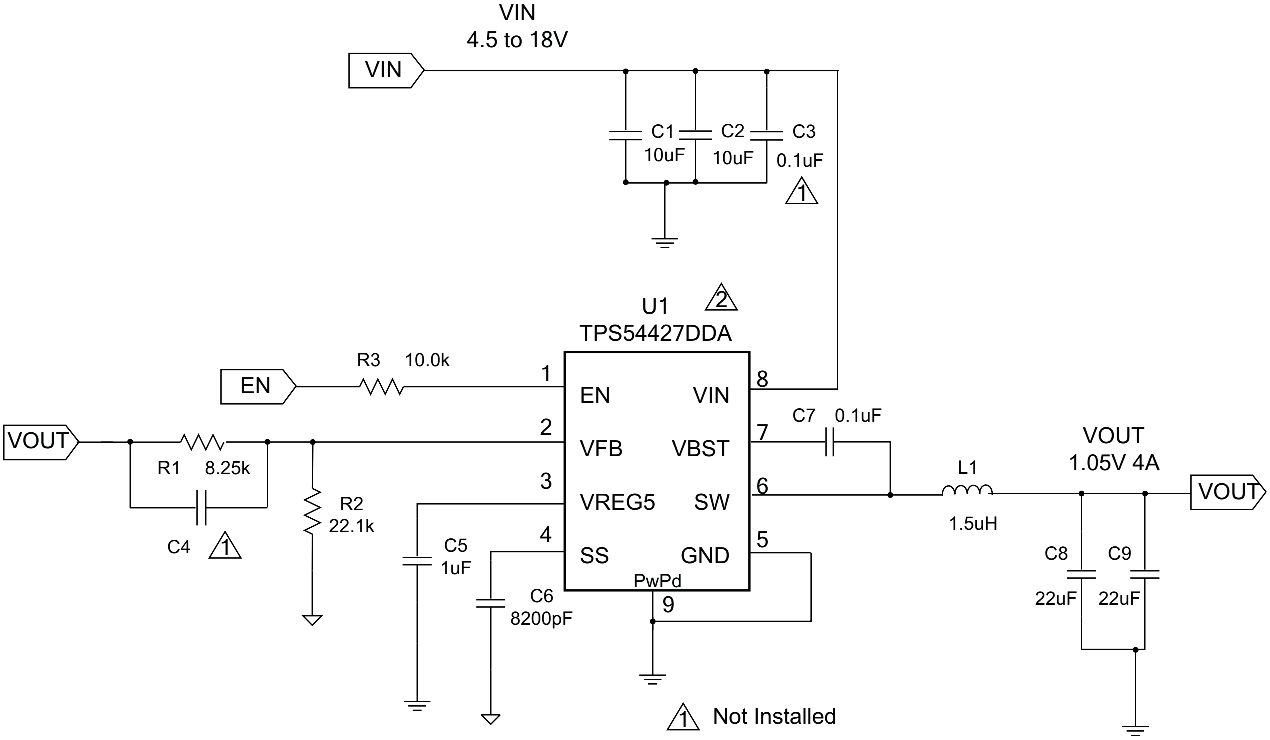


Figure 14. Shows the Schematic Diagram for this Design Example

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \times \left(1+\frac{R1}{R2}\right) \tag{2}$$

Output Filter Selection

The output filter used with the TPS54427 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54427. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.

Table 1. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L1 (µH)	C8 + C9 (µF)
1	6.81	22.1		1.5	22 - 68
1.05	8.25	22.1		1.5	22 - 68
1.2	12.7	22.1		1.5	22 - 68
1.5	21.5	22.1		1.5	22 - 68
1.8	30.1	22.1	5 - 22	2.2	22 - 68
2.5	49.9	22.1	5 - 22	2.2	22 - 68
3.3	73.2	22.1	5 - 22	2.2	22 - 68
5	124	22.1	5 - 22	3.3	22 - 68
6.5	165	22.1	5 - 22	3.3	22 - 68

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$Il_{P\text{-}P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$Il_{PEAK} = I_O + \frac{Il_{P\text{-}P}}{2} \tag{5}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Il_{P-P}^2} \tag{6}$$

For this design example, the calculated peak current is 4.51 A and the calculated RMS current is 4.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54427 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22µF to 68µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{7}$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

Input Capacitor Selection

The TPS54427 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C3) from pin 8 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

THERMAL INFORMATION

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

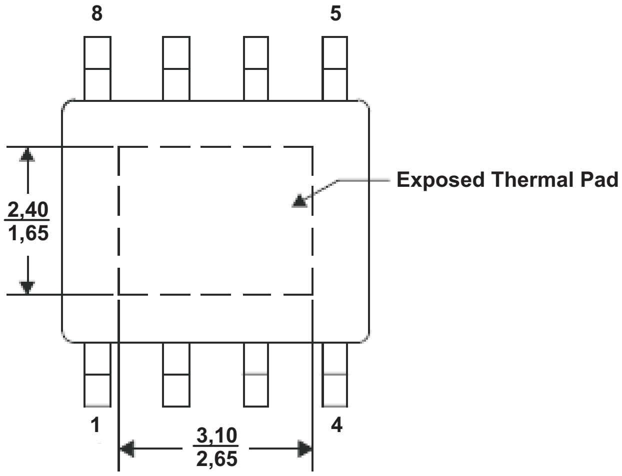


Figure 15. Thermal Pad Dimensions

LAYOUT CONSIDERATIONS

1. The TPS54427 can supply relatively large current up to 4A. So heat dissipation may be a concern. The top side area adjacent to the TPS54427 should be filled with ground as much as possible to dissipate heat.
2. The bottom side area directly below the IC should a dedicated ground area. It should be directed connected to the thermal pad of the using vias as shown. The ground area should be as large as practical. Additional internal layers can be dedicated as ground planes and connected to vias as well.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor should be placed near the device, and connected PGND.
11. Output capacitor should be connected to a broad pattern of the PGND.
12. Voltage feedback loop should be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
14. Providing sufficient via is preferable for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND should be as broad as possible.
16. VIN Capacitor should be placed as near as possible to the device.

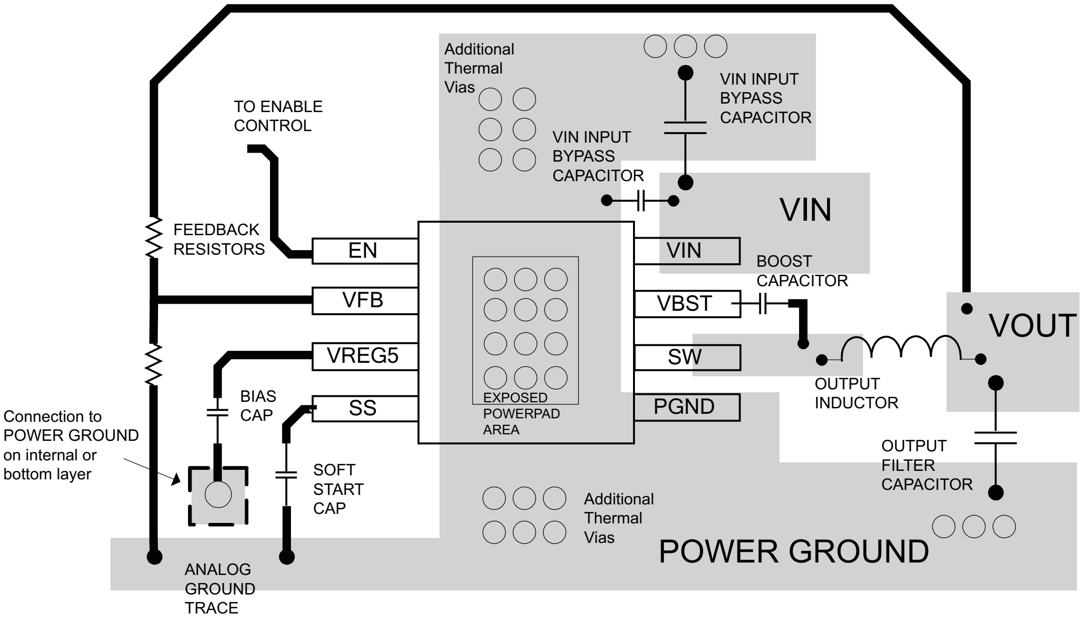


Figure 16. TPS54427 Layout

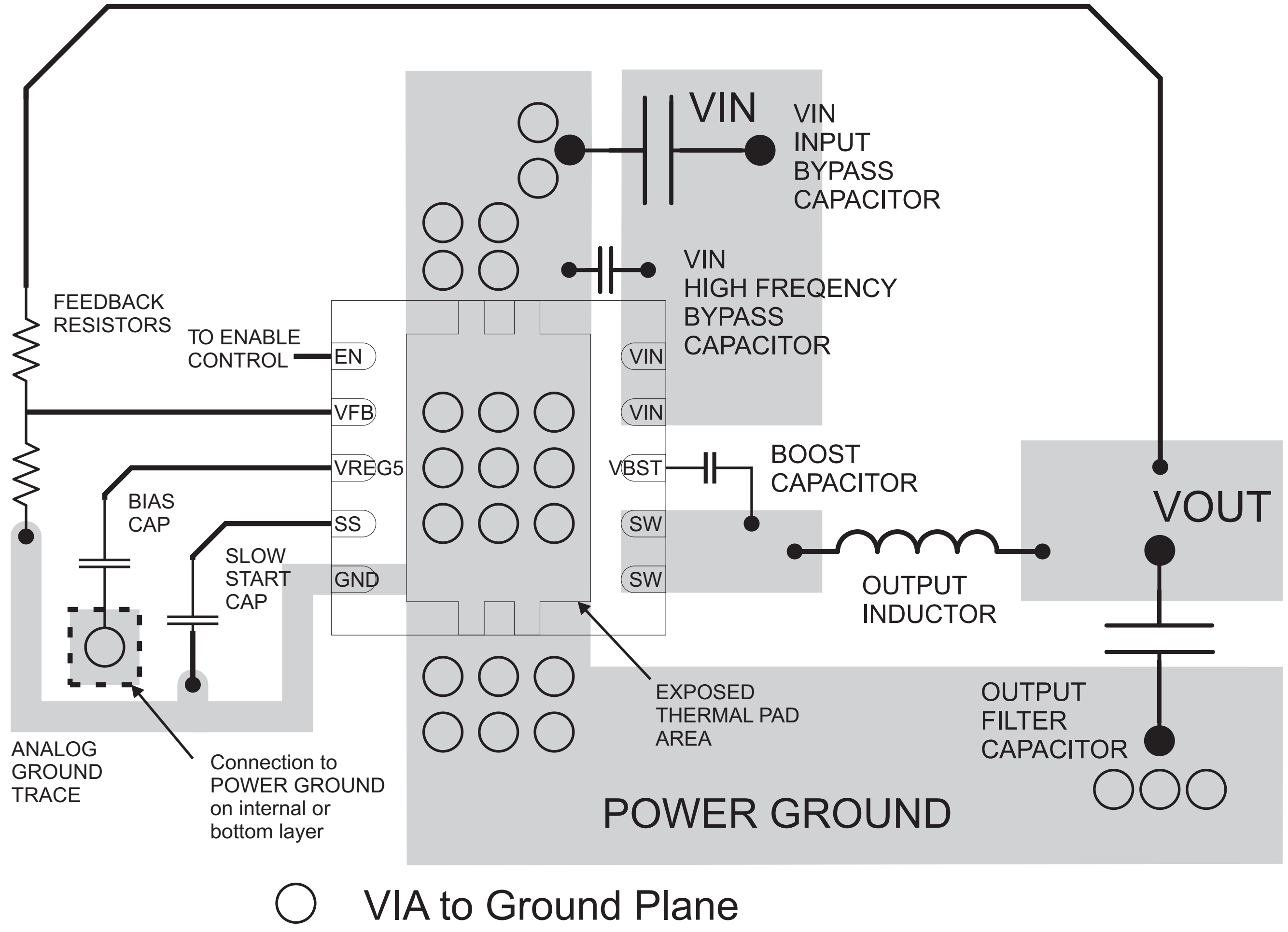


Figure 17. PCB Layout for the DRC Package

REVISION HISTORY

Changes from Original (November 2011) to Revision A	Page
• 在说明中添加了“以及 10 引脚 DRC 封装”	1
• Added the DRC-10 pin Package to the ORDERING INFORMATION table	2
• Changed the VBST(vs SW) MAX value From: 5.7V to 6V in the ROC table	3
• Changed V_{FB} input current MAX value From: ±0.15 µA To: ±0.1 µA	3
• Added High side switch resistance (DRC)	3
• Changed Figure 11	9
• Added Figure 13	10
• Added Figure 17	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54427DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	54427	Samples
TPS54427DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	54427	Samples
TPS54427DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54427	Samples
TPS54427DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54427	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

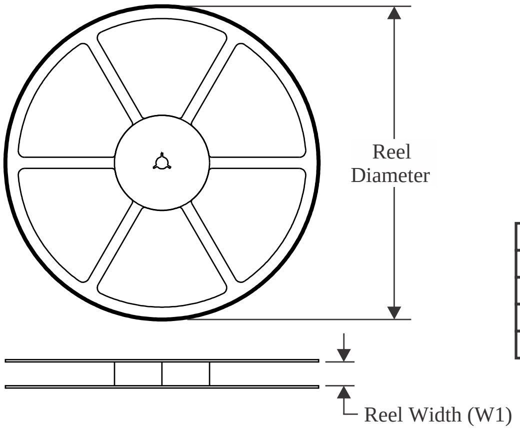
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

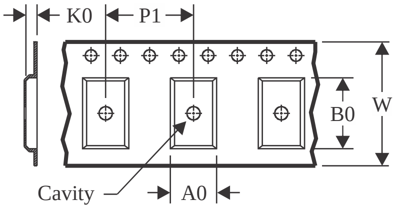
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

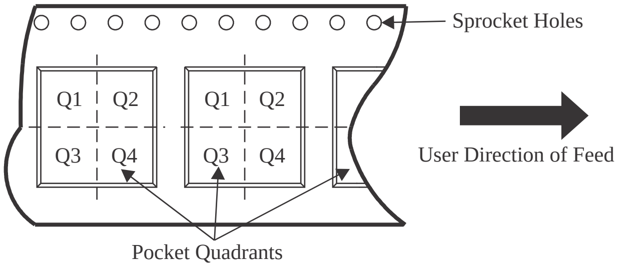


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

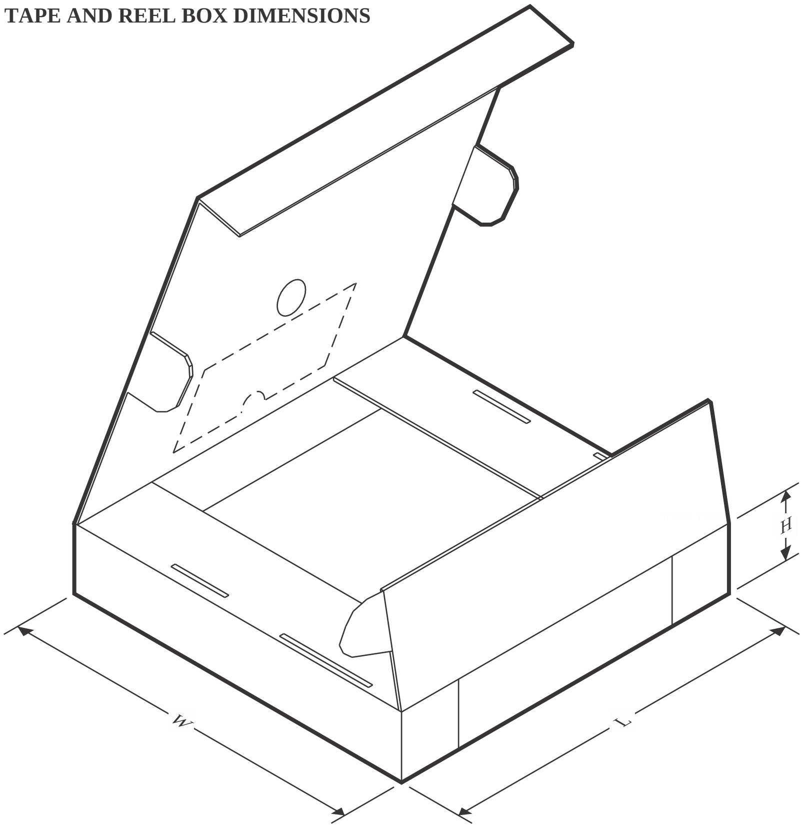
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54427DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54427DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

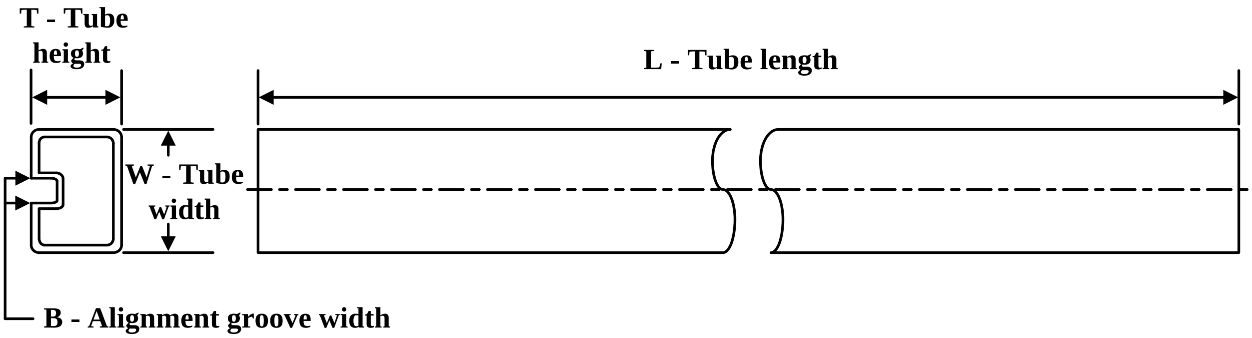
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54427DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS54427DRCT	VSON	DRC	10	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54427DDA	DDA	HSOIC	8	75	517	7.87	635	4.25

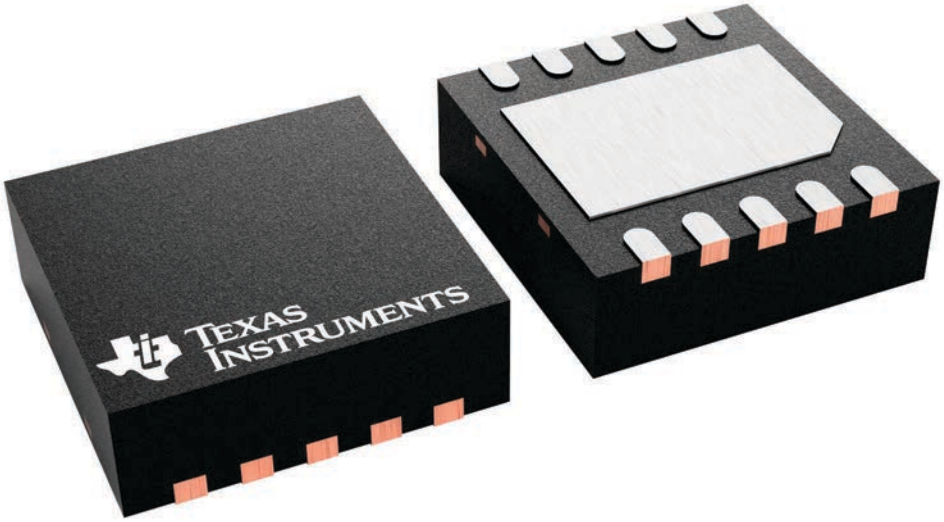
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

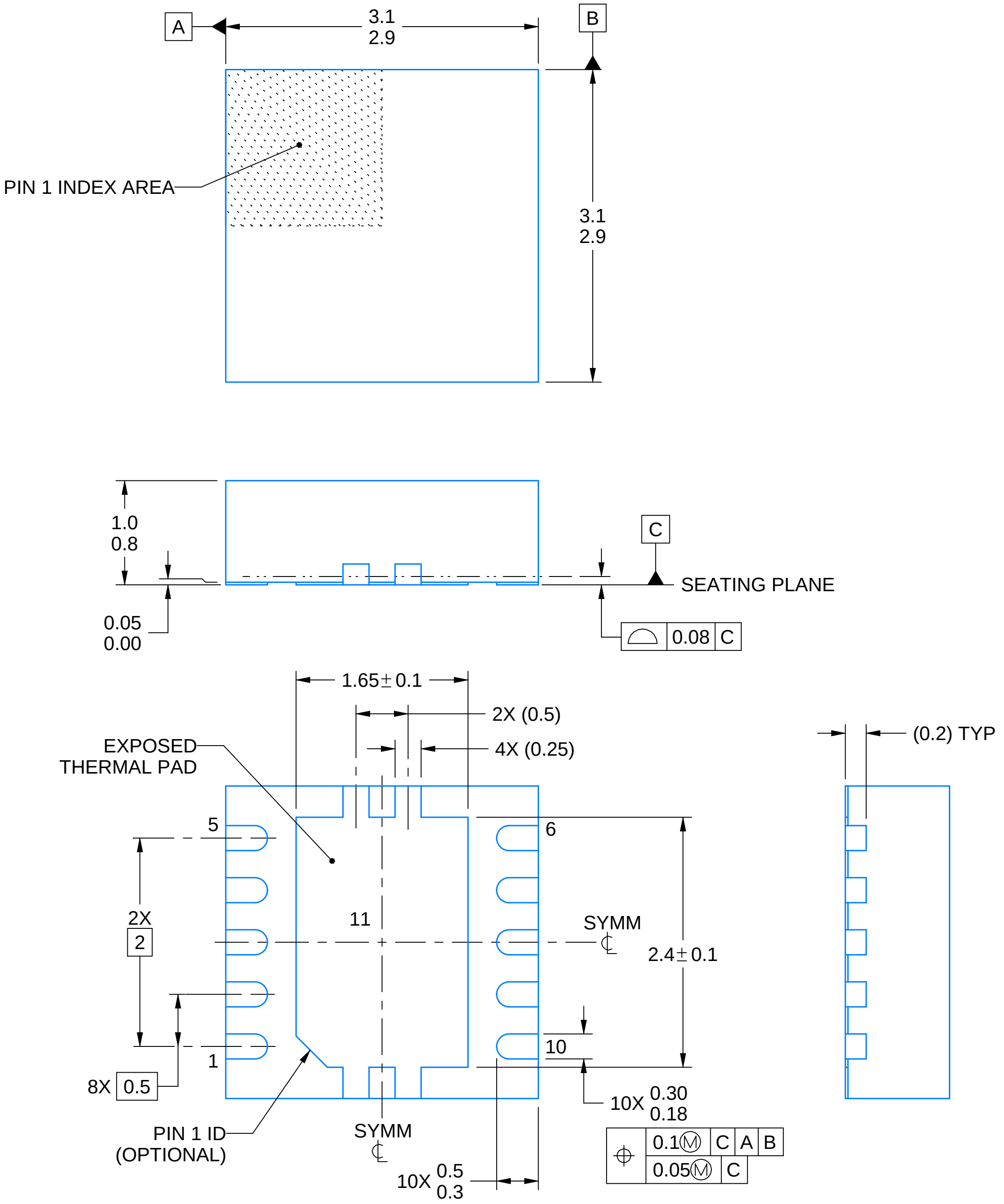
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

VSON - 1 mm max height

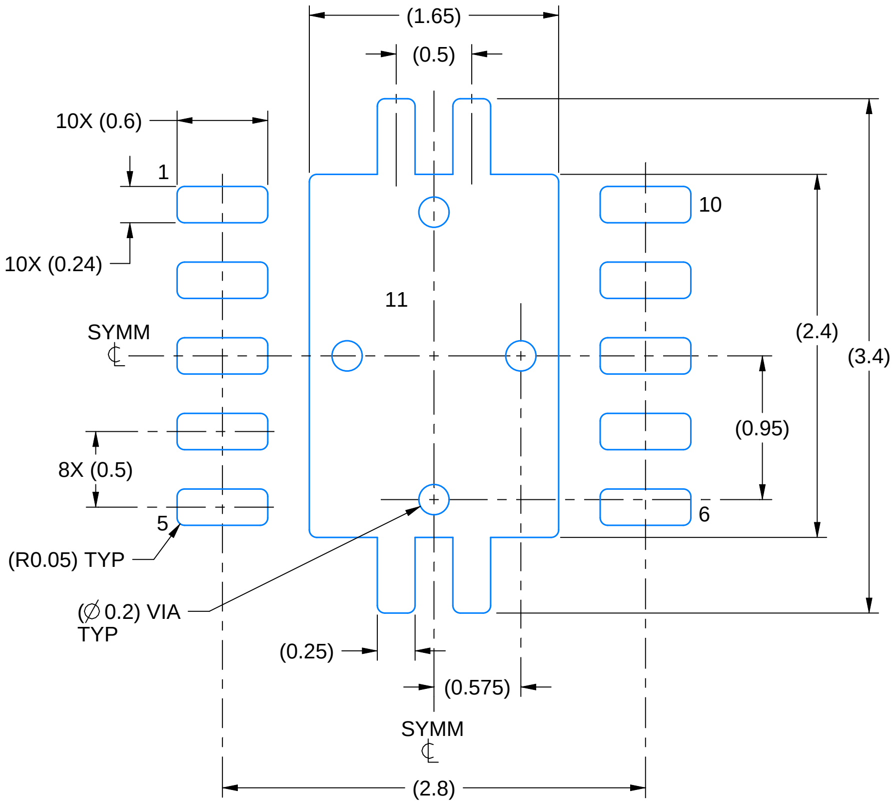
PLASTIC SMALL OUTLINE - NO LEAD



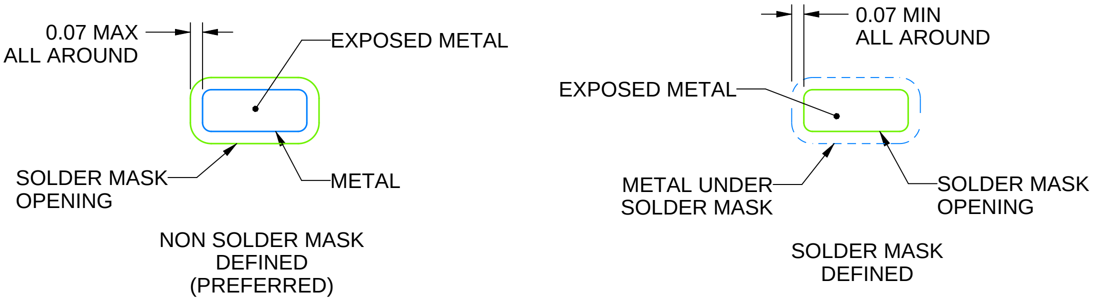
4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



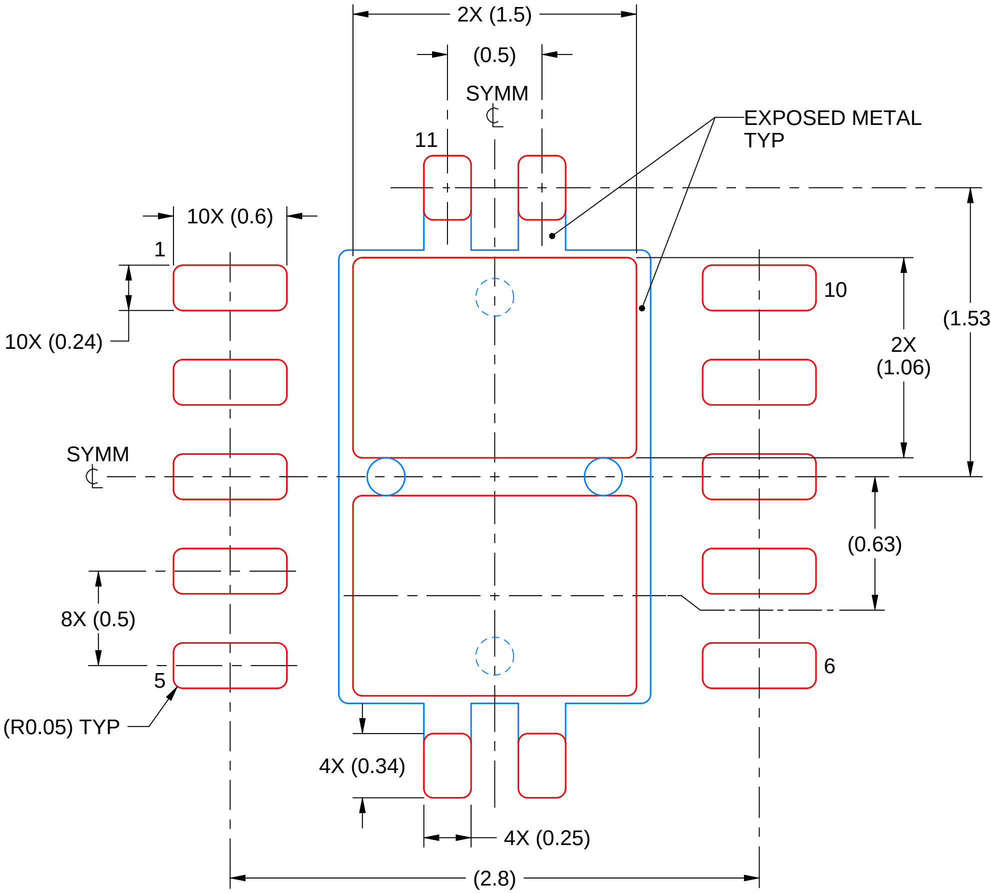
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

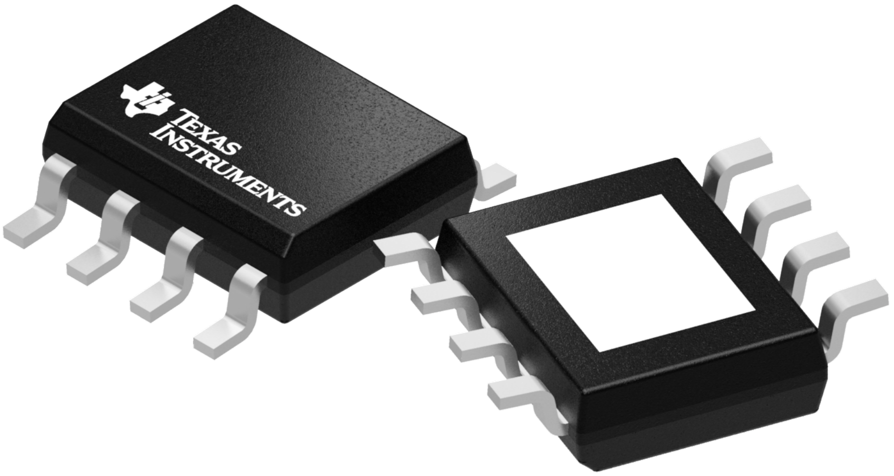
4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

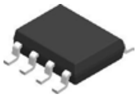
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

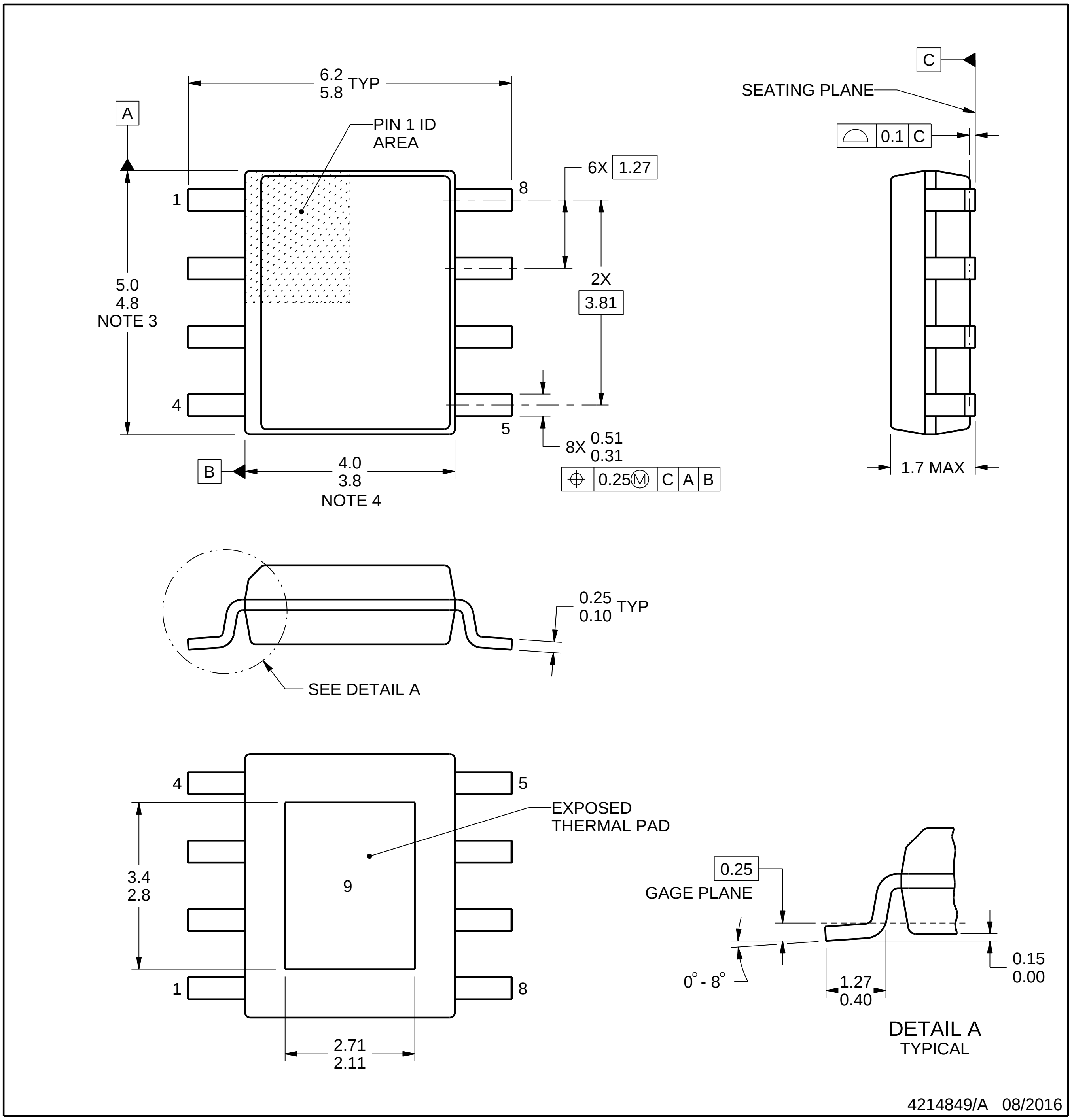
PACKAGE OUTLINE



DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

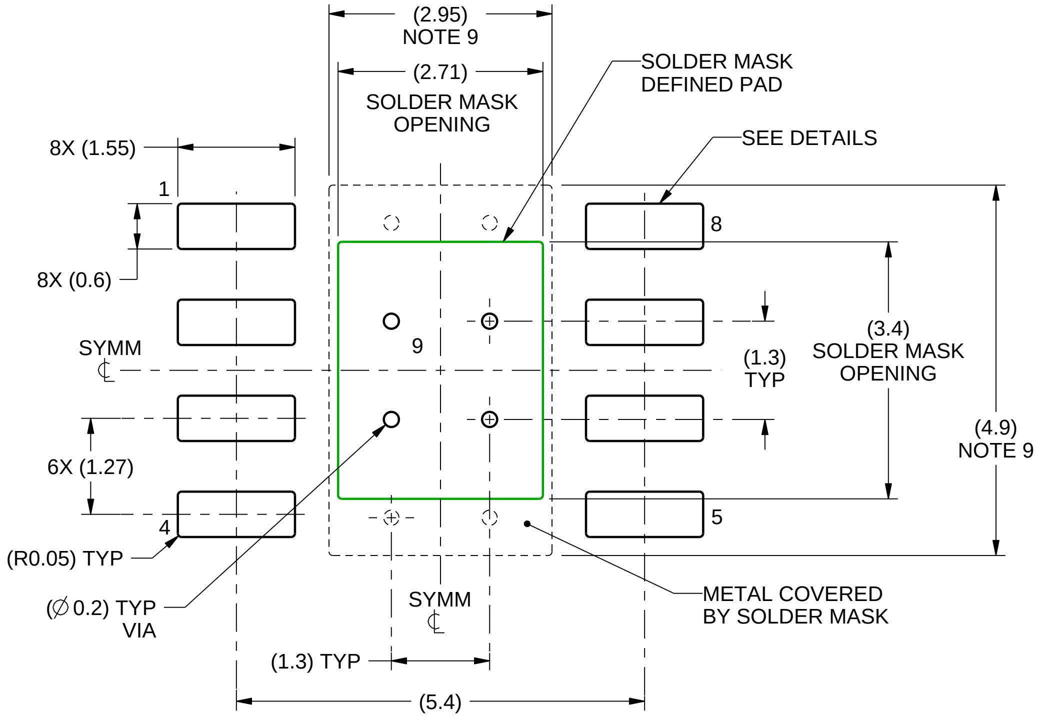
PLASTIC SMALL OUTLINE



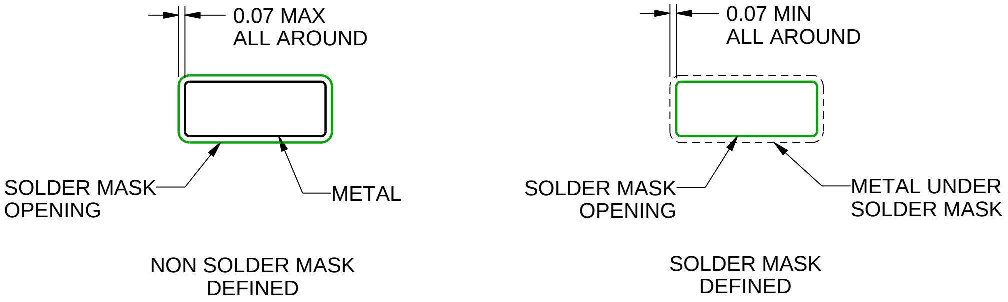
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



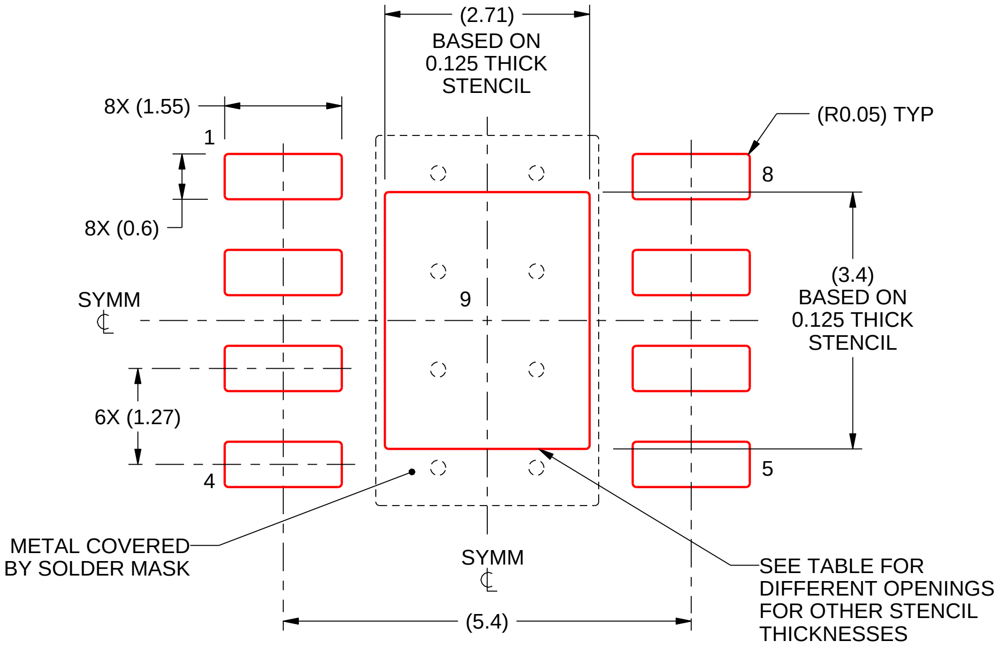
LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

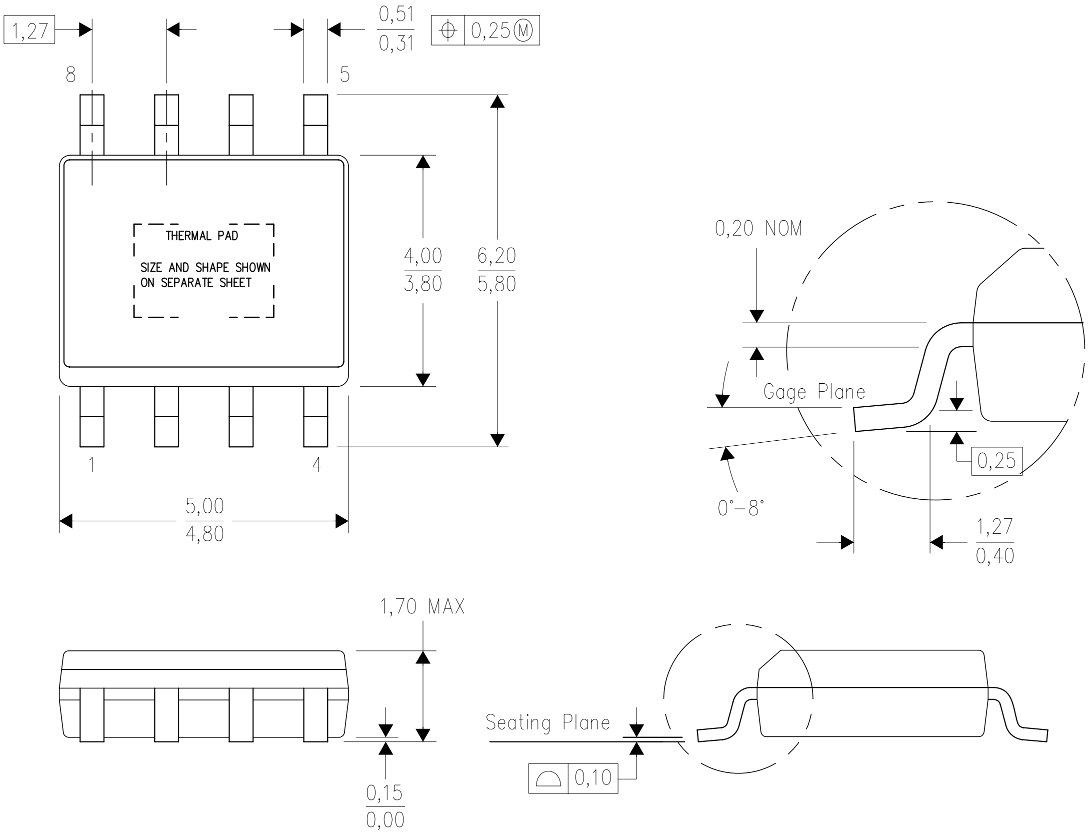
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. This package complies to JEDEC MS–012 variation BA

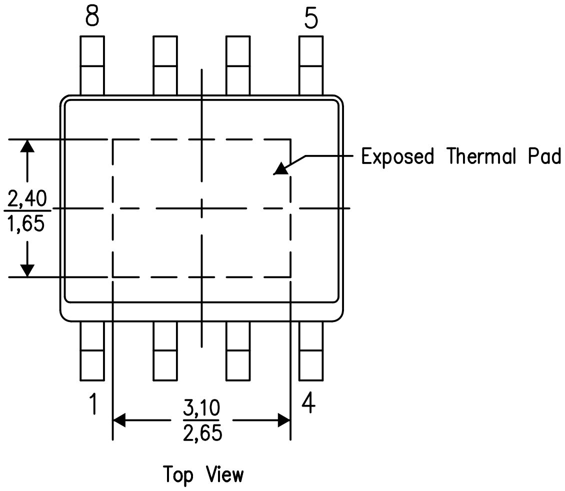
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



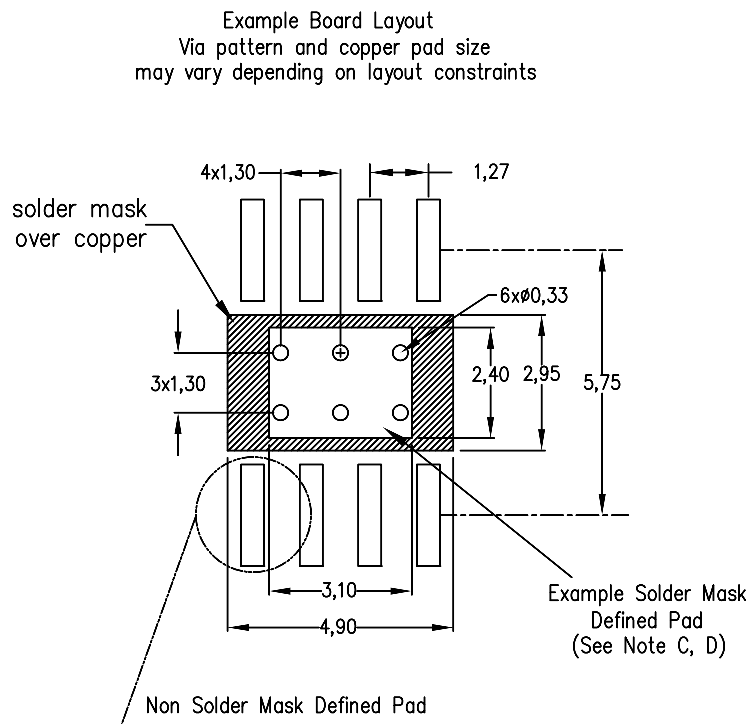
Exposed Thermal Pad Dimensions

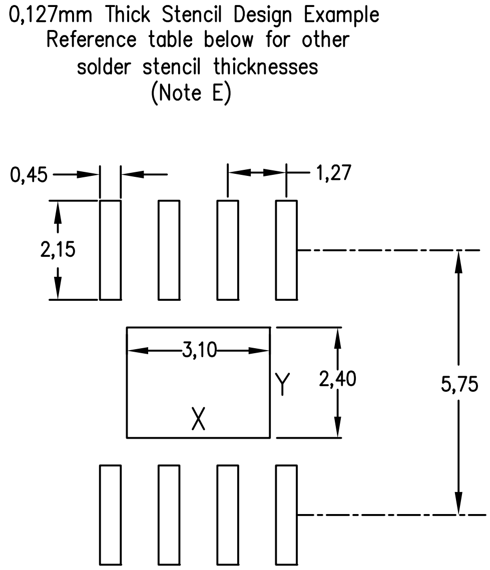
4206322-6/L 05/12

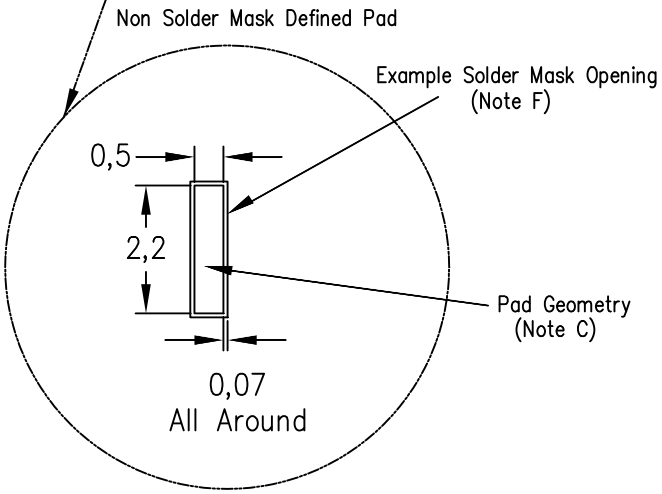
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE







Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951-6/D 04/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要通知和免责声明

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