TEXAS INSTRUMENTS

TPS54560-Q1

ZHCSBN7A –SEPTEMBER 2013–REVISED DECEMBER 2014

TPS54560-Q1 具有 Eco-Mode™ 的 4.5V 至 60V 输入、5A、降压 DC-DC 转换器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H1C
  - 器件组件充电模式 (CDM) ESD 分类等级 C3B
- 可在轻负载条件下实现高效率，使用脉冲跳跃 Eco-mode™
- 92mΩ 高侧金属氧化物半导体场效应晶体管 (MOSFET)
- 146μA 静态运行电流和 2μA 关断电流
- 100kHz 至 2.5MHz 可调开关频率
- 同步至外部时钟
- 轻负载条件下使用集成型引导 (BOOT) 再充电场效应晶体管 (FET) 实现的低压降
- 可调欠压闭锁 (UVLO) 电压和滞后
- 0.8V 1% 内部电压基准
- 8 引脚散热增强型小外形集成电路 (HSOIC) PowerPAD™封装
- -40°C 至 150°C T$_J$ 运行范围
- 由 WEBENCH®软件工具提供支持

2 应用范围

- 车辆附件：全球卫星定位 (GPS)（请参见 SLVA412），娱乐系统，高级驾驶员辅助系统 (ADAS)，紧急呼叫系统 (eCall)
- USB 专用充电端口和电池充电器（请参见 SLVA464）
- 工业自动化和电机控制
- 12V，24V 和 48V 工业、汽车和通信电源系统

3 说明

TPS54560-Q1 是一款 60V、5A 降压稳压器，此稳压器集成有一个高侧 MOSFET。按照 ISO 7637 标准，此器件能够耐受的抛负载脉冲高达 65V。电流模式控制提供了简单的外部补偿和灵活的组件选择。低纹波脉冲跳跃模式可将无负载电源电流降至 146μA。当使能引脚被拉至低电平时，关断电源电流会降至 2μA。

欠压闭锁在内部设定为 4.3V，但可用一个使能引脚上的外部电阻分压器将之提高。该器件可在内部控制输出电压启动斜坡，从而控制启动过程并消除过冲。

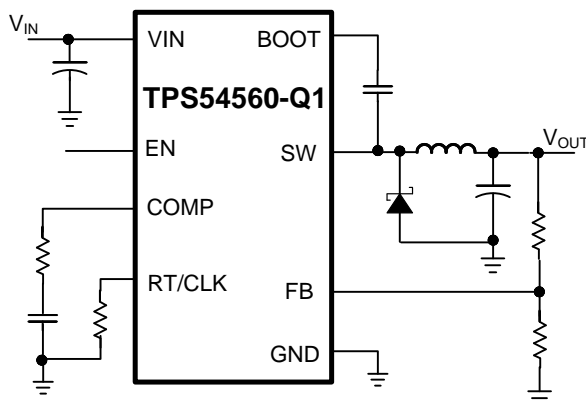宽开关频率范围可实现对效率或者外部组件尺寸进行的优化。输出电流是受限的逐周期电流。频率折返和热关断在过载条件下保护内部和外部组件。

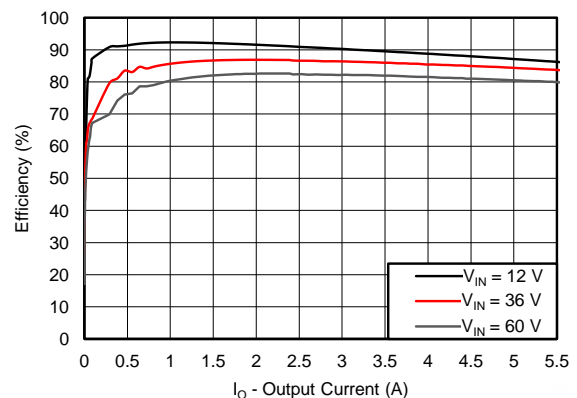TPS54560-Q1 采用 8 引脚散热增强型 HSOIC PowerPAD 封装。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TPS54560-Q1	SO PowerPAD (8)	3.90mm x 4.89mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图

效率与负载电流间的关系

目录

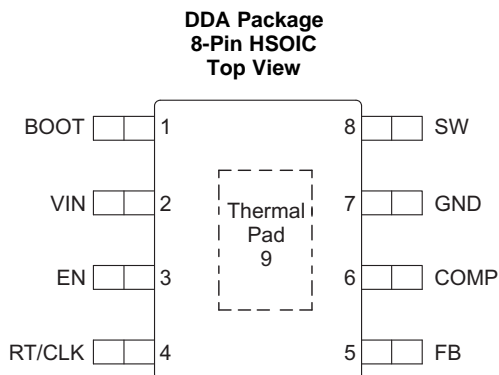## 4   修订历史记录

Changes from Original (September 2013) to Revision A   **Page**

- 已添加 ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。 1

5 Pin Configuration and Functions

DDA Package
8-Pin HSOIC
Top View

```
        BOOT ──┤ 1        8 ├── SW

         VIN ──┤ 2   ┌─────┐  7 ├── GND
                     │Thermal│
          EN ──┤ 3   │ Pad  │  6 ├── COMP
                     │  9   │
      RT/CLK ──┤ 4   └─────┘  5 ├── FB
```

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high-side MOSFET, the output is switched off until the capacitor is refreshed.
VIN	2	I	Input supply voltage with 4.5 V to 60 V operating range.
EN	3	I	Enable pin, with internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the *Enable and Adjusting Undervoltage Lockout* section.
RT/CLK	4	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
FB	5	I	Inverting input of the transconductance (gm) error amplifier.
COMP	6	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
GND	7	–	Ground
SW	8	I	The source of the internal high-side power MOSFET and switching node of the converter.
Thermal Pad	9	–	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	−0.3	65	V
	EN	−0.3	8.4	
	BOOT		73	
	FB	−0.3	3	
	COMP	−0.3	3	
	RT/CLK	−0.3	3.6	
Output voltage	BOOT-SW		8	V
	SW	−0.6	65	
	SW, 10-ns Transient	−2	65	
Operating junction temperature		−40	150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating Input Voltage on (VIN pin)	4.5	60	V
Operating junction temperature, T_J	−40	150	°C

6.4 Thermal Information

	THERMAL METRIC[1][2]	TPS54560-Q1 DDA 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	
ψ_{JT}	Junction-to-top characterization parameter	5.9	
ψ_{JB}	Junction-to-board characterization parameter	23.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Test boards conditions:
  (a) 3 inches x 3 inches, 2 layers, thickness: 0.062 inch
  (b) 2 oz. copper traces located on the top of the PCB
  (c) 2 oz. copper ground plane, bottom layer
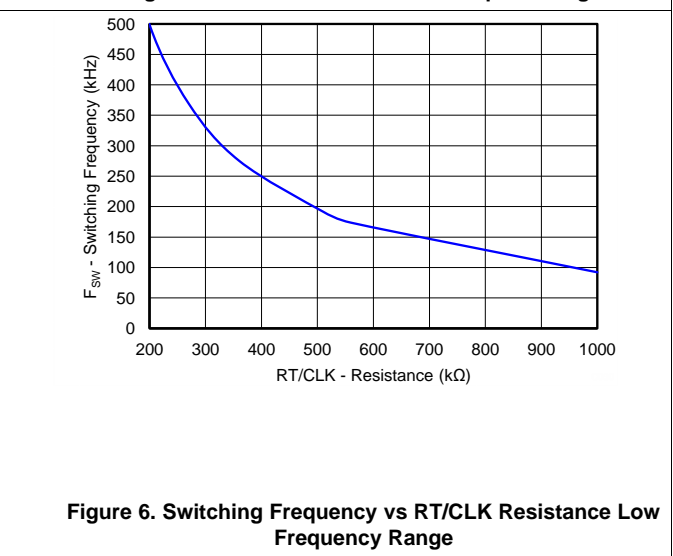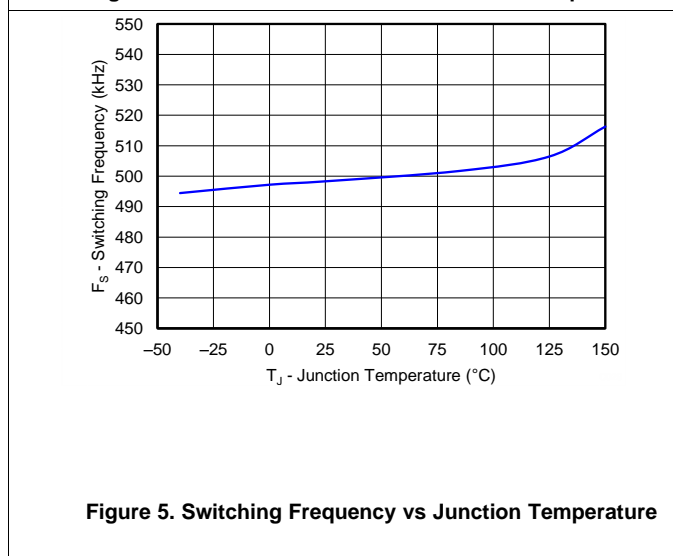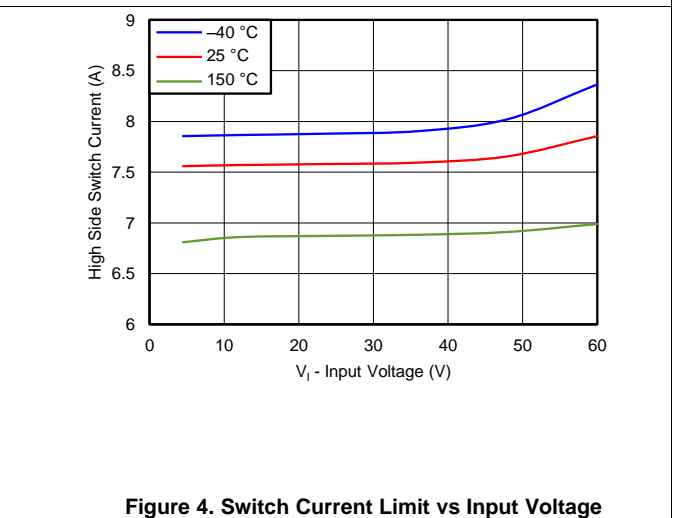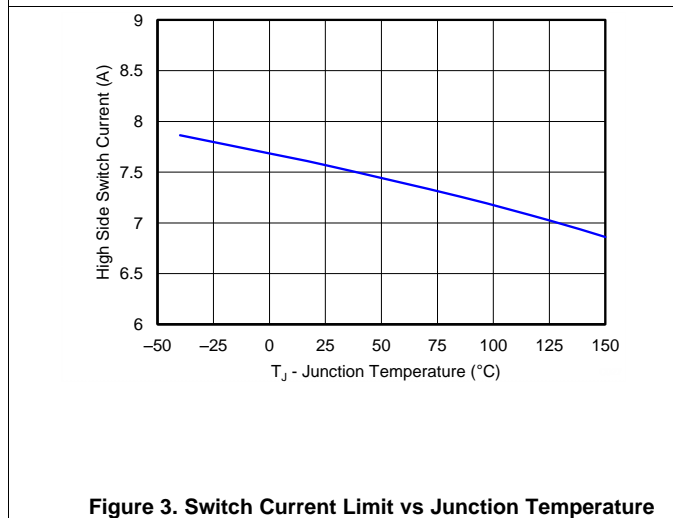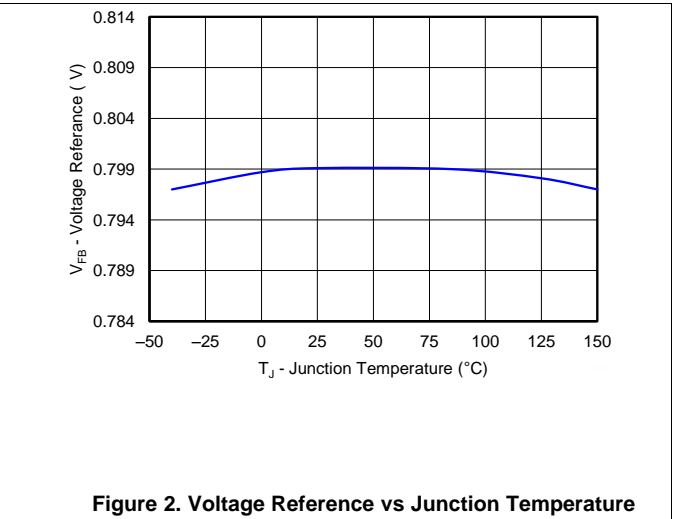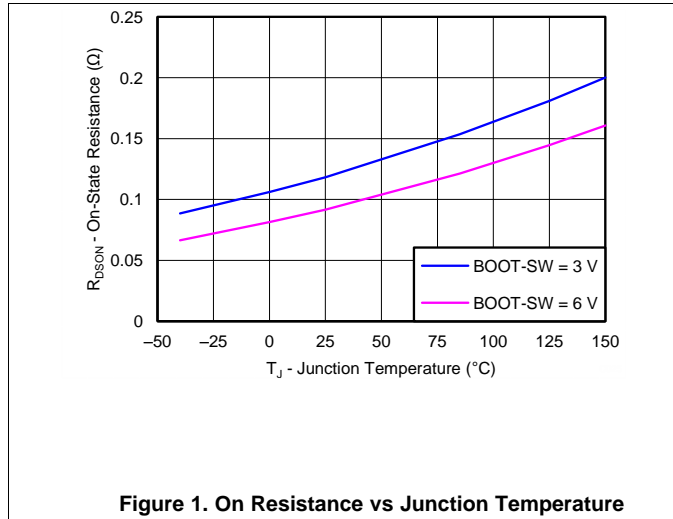 (d) 6 thermal vias (13mil) located under the device package

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 4.5 to 60V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
	Operating input voltage		4.5		60	V
	Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
	Internal undervoltage lockout threshold hysteresis			325		mV
	Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 60 V		2.25	4.5	μA
	Operating: nonswitching supply current	FB = 0.9 V, T_A = 25°C		146	175	
ENABLE AND UVLO (EN PIN)						
	Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
	Input current	Enable threshold +50 mV		–4.6		μA
		Enable threshold –50 mV	–0.58	–1.2	-1.8	
	Hysteresis current		–2.2	–3.4	-4.5	μA
	Enable to COMP active	V_{IN} = 12 V, T_A = 25°C		540		μs
INTERNAL SOFT-START TIME						
	Soft-Start Time	f_{SW} = 500 kHz, 10% to 90%		2.1		ms
	Soft-Start Time	f_{SW} = 2.5 MHz, 10% to 90%		0.42		ms
VOLTAGE REFERENCE						
	Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET						
	On-resistance	VIN = 12 V, BOOT-SW = 6 V		92	190	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
	Error amplifier transconductance (g_M)	–2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V		350		μMhos
	Error amplifier transconductance (g_M) during soft-start	–2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		μMhos
	Error amplifier dc gain	V_{FB} = 0.8 V		10,000		V/V
	Min unity gain bandwidth			2500		kHz
	Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±30		μA
	COMP to SW current transconductance			17		A/V
CURRENT LIMIT						
	Current limit threshold	All VIN and temperatures, Open-Loop[1]	6.3	7.5	8.8	A
		All temperatures, VIN = 12 V, Open-Loop[1]	6.3	7.5	8.3	
		VIN = 12 V, T_A = 25°C, Open-Loop[1]	7.1	7.5	7.9	
	Current limit threshold delay			60		ns
THERMAL SHUTDOWN						
	Thermal shutdown			176		°C
	Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	Minimum CLK input pulse width			15		ns
	RT/CLK high threshold			1.55	2	V
	RT/CLK low threshold		0.5	1.2		V
	RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with RT resistor in series		55		ns
	PLL lock in time	Measured at 500 kHz		78		μs

(1) Open-loop current limit measured directly at the SW pin and is independent of the inductor value and slope compensation.
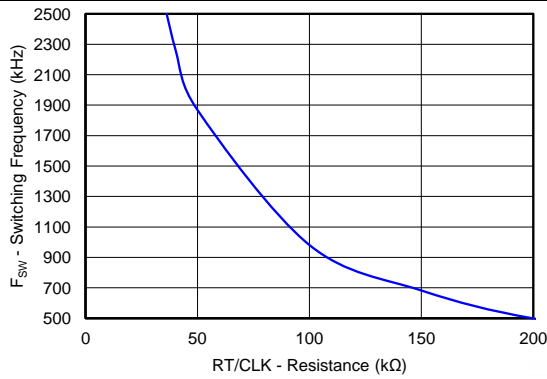
6.6 Typical Characteristics

Figure 1. On Resistance vs Junction Temperature

Figure 2. Voltage Reference vs Junction Temperature

Figure 3. Switch Current Limit vs Junction Temperature

Figure 4. Switch Current Limit vs Input Voltage

Figure 5. Switching Frequency vs Junction Temperature

Figure 6. Switching Frequency vs RT/CLK Resistance Low Frequency Range

Typical Characteristics (continued)

Figure 7. Switching Frequency vs RT/CLK Resistance High Frequency Range
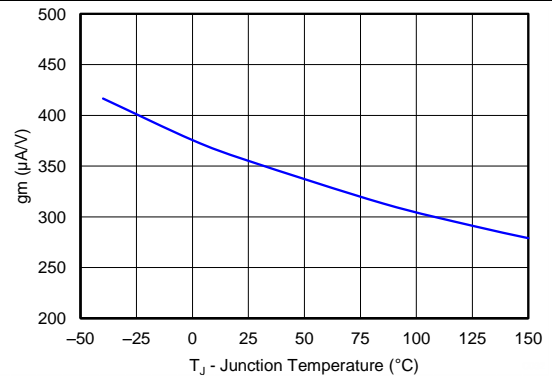

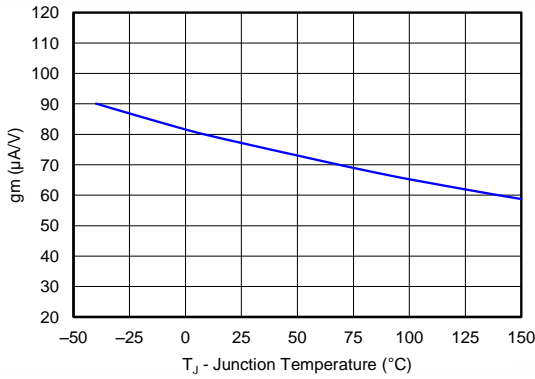**Figure 8. EA Transconductance vs Junction Temperature**

Figure 9. EA Transconductance During Soft-Start vs Junction Temperature
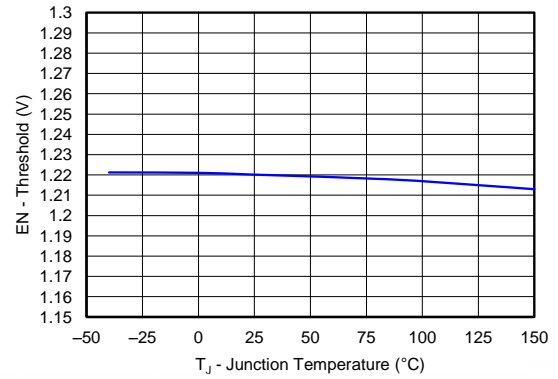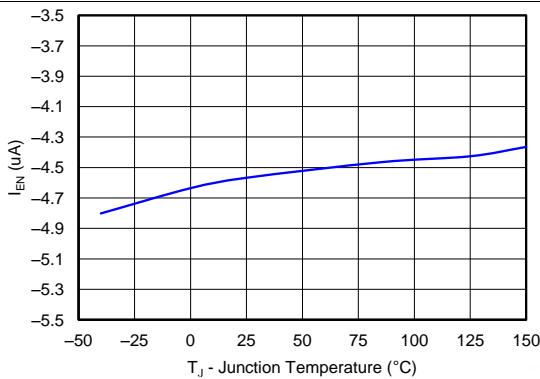

Figure 10. EN Pin Voltage vs Junction Temperature

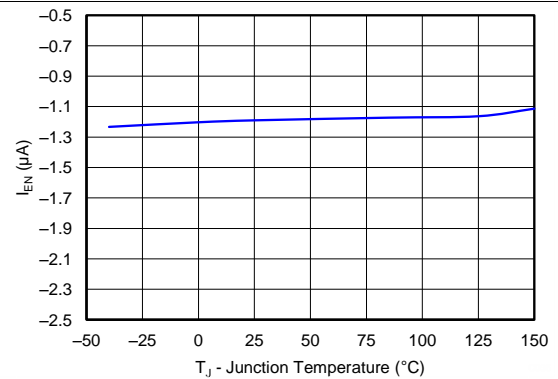**Figure 11. EN Pin Current vs Junction Temperature**

Figure 12. EN Pin Current vs Junction Temperature
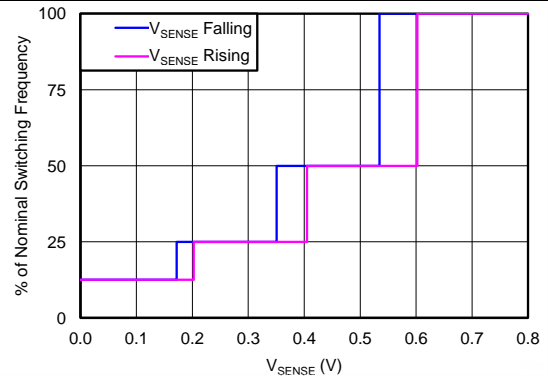
Typical Characteristics (continued)
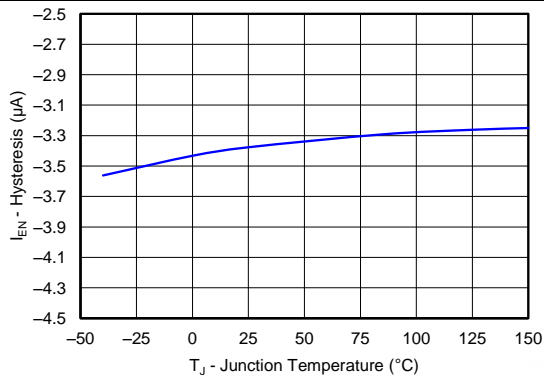
Figure 13. EN Pin Current Hysteresis vs Junction Temperature

Figure 14. Switching Frequency vs V_SENSE
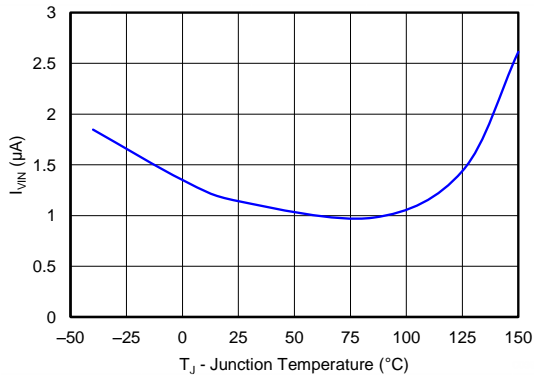
Figure 15. Shutdown Supply Current vs Junction Temperature
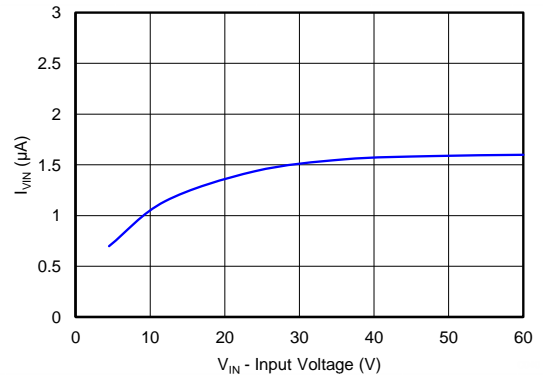
Figure 16. Shutdown Supply Current vs Input Voltage (V_IN)
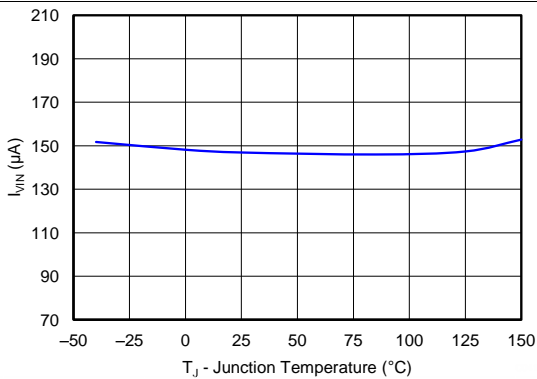
Figure 17. V_IN Supply Current vs Junction Temperature
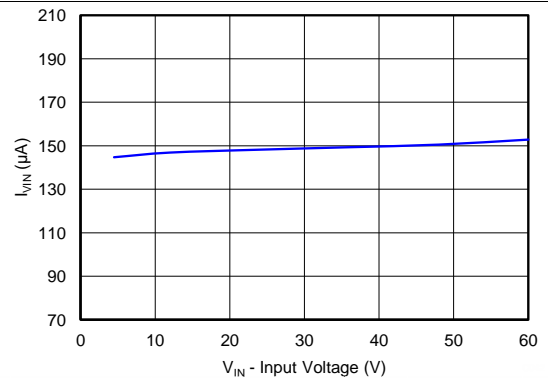
Figure 18. V_IN Supply Current vs Input Voltage

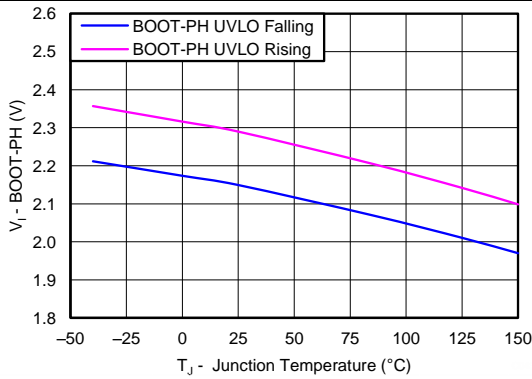## Typical Characteristics (continued)

Figure 19. BOOT-SW UVLO vs Junction Temperature
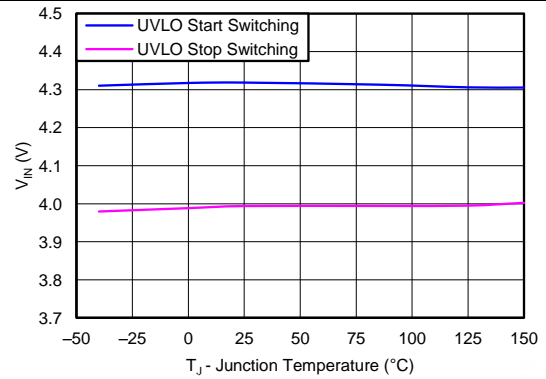

Figure 20. Input Voltage UVLO vs Junction Temperature
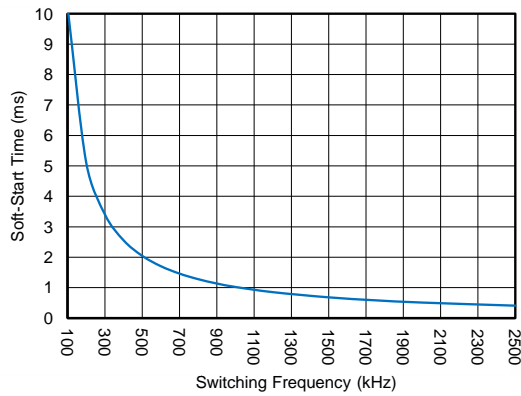

Figure 21. Soft-Start Time vs Switching Frequency
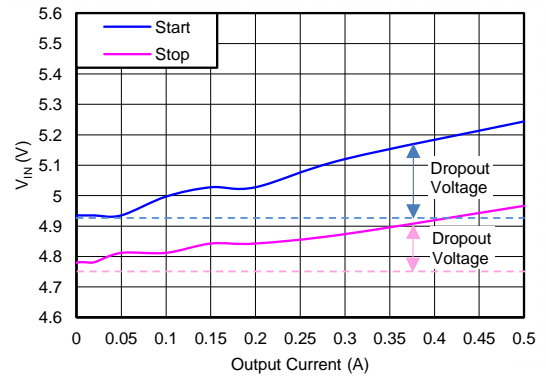

Figure 22. 5 V Start and Stop Voltage (see *Low Dropout Operation and Bootstrap Voltage (BOOT)*)

7 Detailed Description

7.1 Overview

The TPS54560-Q1 is a 60-V, 5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. The device implements constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2500 kHz allows either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK pin. The device has an internal phase-locked loop (PLL) connected to the RT/CLK pin that will synchronize the power switch turn on to a falling edge of an external clock signal.

The TPS54560-Q1 has a default input start-up voltage of approximately 4.3 V. The EN pin can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. An internal pull up current source enables operation when the EN pin is floating. The operating current is 146 μA under no load condition (not switching). When the device is disabled, the supply current is 2 μA.

The integrated 92-mΩ, high-side MOSFET supports high efficiency power supply designs capable of delivering 5 amperes of continuous current to a load. The gate drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW pins. The TPS54560-Q1 reduces the external component count by integrating the bootstrap recharge diode. The BOOT pin capacitor voltage is monitored by a UVLO circuit which turns off the high-side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54560-Q1 to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8-V feedback reference.

Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET is turned off and remains off until the output voltage is less than 106% of the desired output voltage.

The TPS54560-Q1 includes an internal soft-start circuit that slows the output rise time during start-up to reduce in-rush current and output voltage overshoot. Output overload conditions reset the soft-start timer. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help maintain control of the inductor current.

7.2 Functional Block Diagram
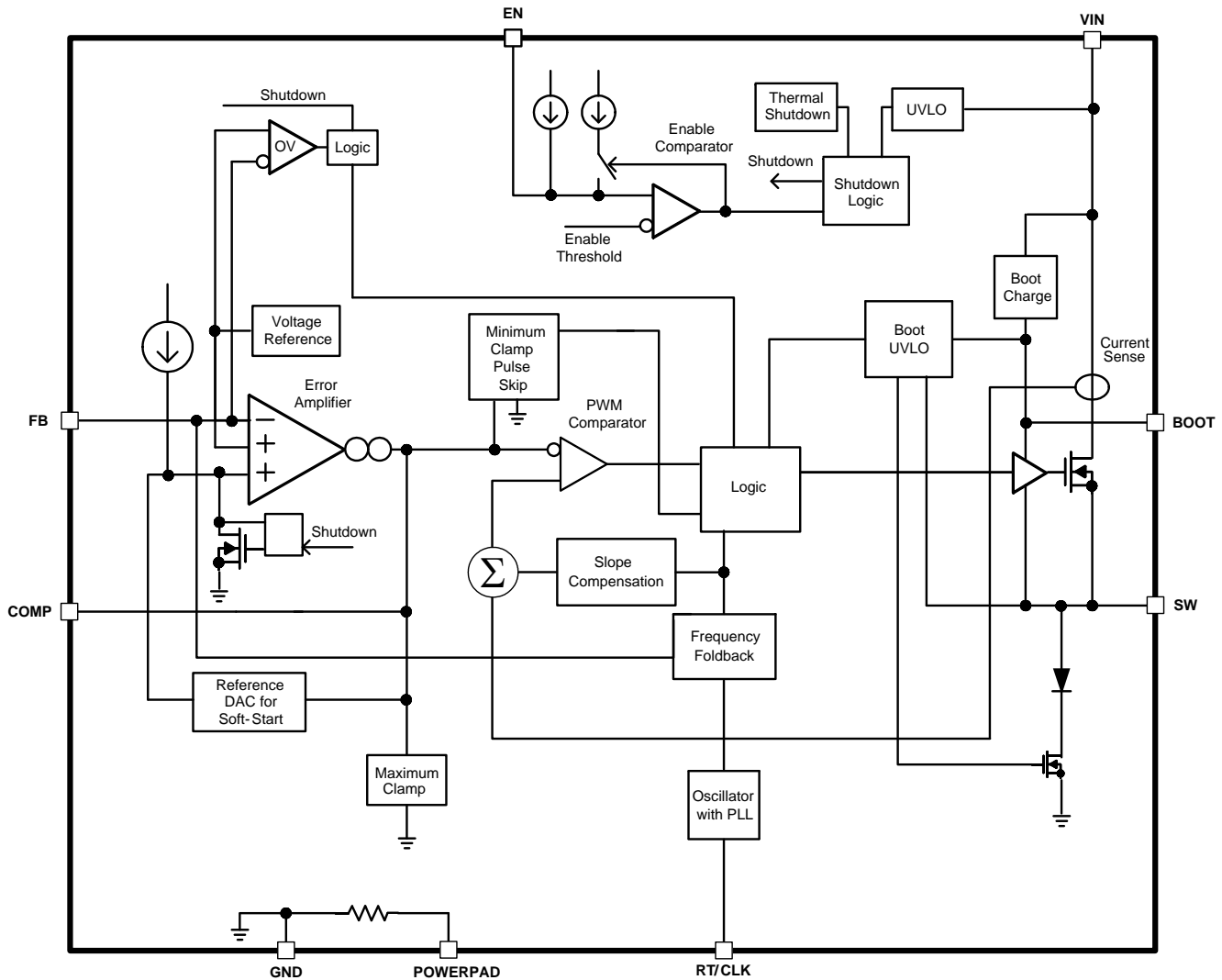
7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54560-Q1 uses fixed frequency, peak current mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output at the COMP pin controls the high-side power switch current. When the high-side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP pin voltage to a maximum level. The pulse-skipping Eco-Mode is implemented with a minimum voltage clamp on the COMP pin.

7.3.2 Slope Compensation Output Current

The TPS54560-Q1 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

Feature Description (continued)

7.3.3 Pulse Skip Eco-Mode

The TPS54560-Q1 operates in a pulse-skipping Eco-Mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse-skipping current threshold, the device enters Eco-Mode. The pulse-skipping current threshold is the peak switch current level corresponding to a nominal COMP voltage of 600 mV.

When in Eco-Mode, the COMP pin voltage is clamped at 600 mV and the high-side MOSFET is inhibited. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP pin voltage. The high-side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse-skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-Mode pulse-skipping threshold at which time the device again enters Eco-Mode. The internal PLL remains operational when in Eco-Mode. When operating at light load currents in Eco-Mode, the switching transitions occur synchronously with the external clock signal.

During Eco-Mode operation, the TPS54560-Q1 senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters Eco-Mode is dependent on the output inductor value. The circuit in Figure 36 enters Eco-Mode at about 25.3 mA output current. As the load current approaches zero, the device enters a pulse-skip mode during which it draws only 146 μA input quiescent current.

7.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54560-Q1 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the TPS54560-Q1 will operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V. When the voltage from BOOT to SW drops below 2.1 V, the high-side MOSFET is turned off and an integrated low-side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low-side MOSFET at high output voltages, it is disabled at 24 V output and re-enabled when the output reaches 21.5 V.

Since the gate drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode voltage and the printed circuit board resistance.

The start and stop voltage for a typical 5-V output application is shown in Figure 22 where the VIN voltage is plotted versus load current. The start voltage is defined as the input voltage needed to regulate the output within 1% of nominal. The stop voltage is defined as the input voltage at which the output drops by 5% or where switching stops.

During high duty cycle (low dropout) conditions, inductor current ripple increases when the BOOT capacitor is being recharged resulting in an increase in output voltage ripple. Increased ripple occurs when the off time required to recharge the BOOT capacitor is longer than the high-side off time associated with cycle-by-cycle PWM control.

At heavy loads, the minimum input voltage must be increased to insure a monotonic startup. Equation 1 can be used to calculate the minimum input voltage for this condition.

$$V_{OUT(max)} = D_{(max)} \times (V_{IN(min)} - I_{OUT(max)} \times R_{DS(on)} + VF) - VF + I_{OUT(max)} \times R_{L\,R}$$

(1)

Where:

Dmax ≥ 0.9
IB2SW = 100 μA
VF = Forward Drop of the Catch Diode
TSW = 1 / Fsw

Feature Description (continued)

VB2SW = VBOOT + VF

VBOOT = (1.41 x V_{IN} - 0.554 - VF / TSW - 1.847 x 10^3 x IB2SW) / (1.41 + 1 / Tsw)

$R_{DS(on)}$ = 1 / (-0.3 x $VB2SW^2$ + 3.577 x VB2SW - 4.246)

7.3.5 Error Amplifier

The TPS54560-Q1 voltage regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 350 μA/V during normal operation. During soft-start operation, the transconductance is reduced to 78 μA/V and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor and capacitor) are connected between the error amplifier output COMP pin and GND pin.

7.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8-V, ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap reference circuit. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. Select the low-side resistor R_{LS} for the desired divider current and use Equation 2 to calculate R_{HS}. To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{Vout - 0.8V}{0.8\ V} \right)$$

(2)

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54560-Q1 is enabled when the VIN pin voltage rises above 4.3 V and the EN pin voltage exceeds the enable threshold of 1.2 V. The TPS54560-Q1 is disabled when the VIN pin voltage falls below 4 V or when the EN pin voltage is below 1.2 V. The EN pin has an internal pull-up current source, I1, of 1.2 μA that enables operation of the TPS54560-Q1 when the EN pin floats.

If an application requires a higher undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 23 to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, an additional 3.4 μA of hysteresis current, I_{HYS}, is sourced out of the EN pin. When the EN pin is pulled below 1.2 V, the 3.4 μA Ihys current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use Equation 3 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use Equation 4 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (that is, from 4.5 V to 9 V) and withstand high input voltages (that is, from 40 V to 60 V), the EN pin may experience a voltage greater than the absolute maximum voltage of 8.4 V during the high input voltage condition. To avoid exceeding this voltage when using the EN resistors, the EN pin is clamped internally with a 5.8 V zener diode that will sink up to 150 μA.

Feature Description (continued)
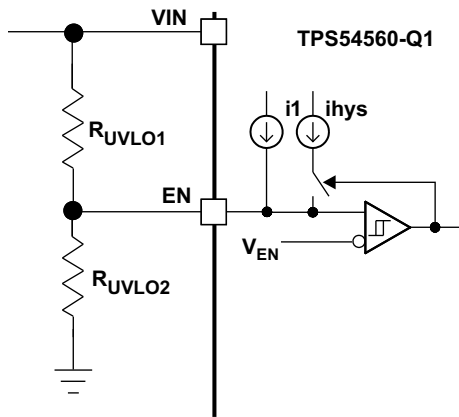
Figure 23. Adjustable Undervoltage Lockout (UVLO)

Figure 24. Internal EN Clamp

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}}$$

(3)

$$R_{UVLO2} = \frac{V_{ENA}}{\dfrac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1}$$

(4)

7.3.8 Internal Soft-Start

The TPS54560-Q1 has an internal digital soft-start that ramps the reference voltage from zero volts to its final value in 1024 switching cycles. The internal soft-start time (10% to 90%) is calculated using Equation 5

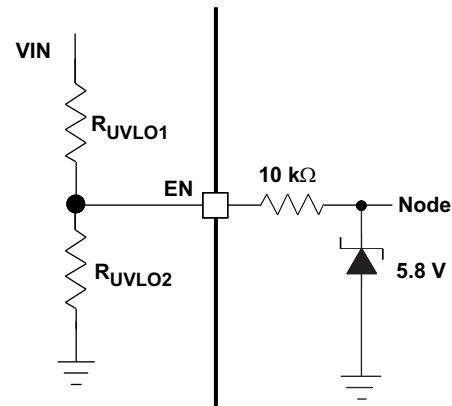$$t_{SS}(ms) = \frac{1024}{f_{SW}(kHz)}$$

(5)

If the EN pin is pulled below the stop threshold of 1.2 V, switching stops and the internal soft-start resets. The soft-start also resets in thermal shutdown.

7.3.9 Constant Switching Frequency and Timing Resistor (RT/CLK) Pin

The switching frequency of the TPS54560-Q1 is adjustable over a wide range from 100 kHz to 2500 kHz by placing a resistor between the RT/CLK pin and GND pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 6 or Equation 7 or the curves in Figure 5 and Figure 6. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 135 ns which limits the maximum operating frequency in applications with high input to output step down ratios. The maximum switching frequency is also limited by the frequency foldback circuit. A more detailed discussion of the maximum switching frequency is provided in the next section.

$$RT\ (k\Omega) = \frac{92417}{f_{SW}\ (kHz)^{0.991}}$$

(6)

$$f_{SW}\ (kHz) = \frac{101756}{RT\ (k\Omega)^{1.008}}$$

(7)

Feature Description (continued)

7.3.10 Accurate Current Limit Operation and Maximum Switching Frequency

The TPS54560-Q1 implements peak current mode control in which the COMP pin voltage controls the peak current of the high-side MOSFET. A signal proportional to the high-side switch current and the COMP pin voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP pin high. The error amplifier output is clamped internally at a level which sets the peak switch current limit. The TPS54560-Q1 provides an accurate current limit threshold with a typical current limit delay of 60 ns. With smaller inductor values, the delay will result in a higher peak inductor current. The relationship between the inductor value and the peak inductor current is shown in Figure 25.
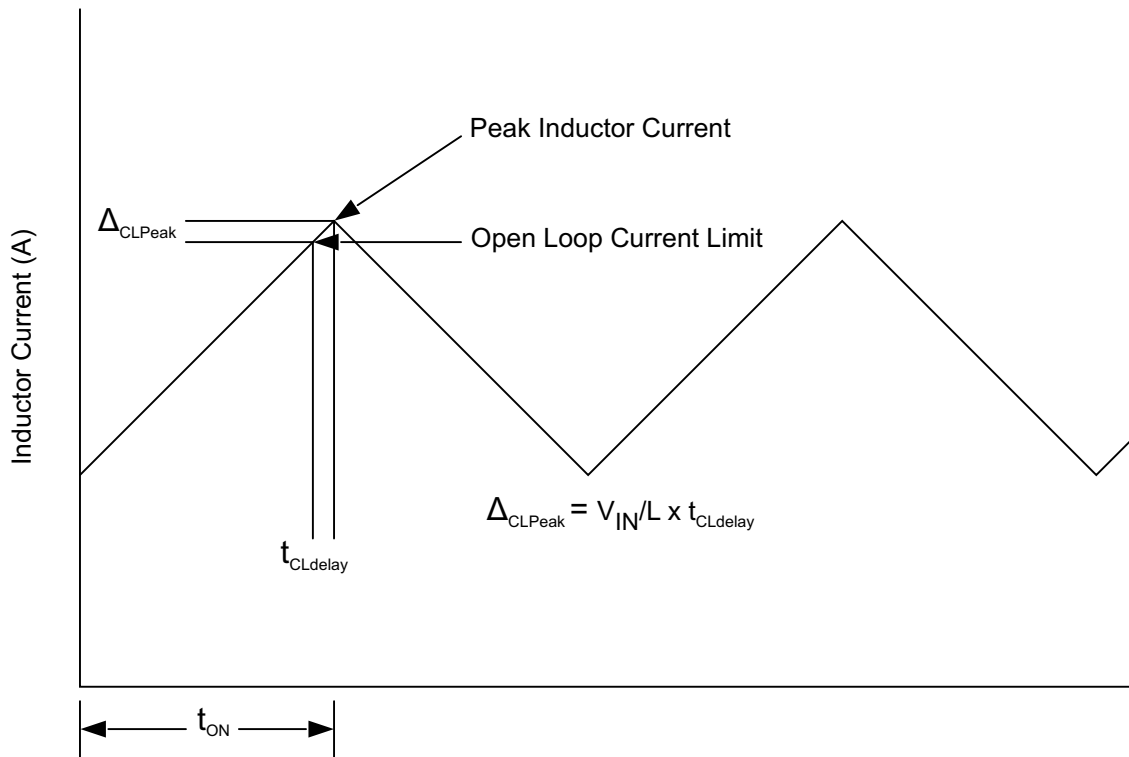

Figure 25. Current Limit Delay

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54560-Q1 implements a frequency foldback. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The TPS54560-Q1 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current can exceed the peak current limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. Equation 9 calculates the maximum switching frequency at which the inductor current will remain under control when V_{OUT} is forced to $V_{OUT(SC)}$. The selected operating frequency should not exceed the calculated value.

Equation 8 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required at maximum input voltage.

Feature Description (continued)

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right)$$

(8)

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right)$$

(9)

I_O	Output current
I_{CL}	Current limit
Rdc	inductor resistance
V_{IN}	maximum input voltage
V_{OUT}	output voltage
V_{OUTSC}	output voltage during short
Vd	diode voltage drop
$R_{DS(on)}$	switch on resistance
t_{ON}	controllable on time
f_{DIV}	frequency divide equals (1, 2, 4, or 8)

7.3.11 Synchronization to RT/CLK Pin

The RT/CLK pin can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature connect a square wave to the RT/CLK pin through either circuit network shown in Figure 26. The square wave applied to the RT/CLK pin must switch lower than 0.5 V and higher than 1.7 V and have a pulse-width greater than 15 ns. The synchronization frequency range is 160 kHz to 2300 kHz. The rising edge of the SW will be synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit should be designed such that the default frequency set resistor is connected from the RT/CLK pin to ground when the synchronization signal is off. When using a low impedance signal source, the frequency set resistor is connected in parallel with an ac coupling capacitor to a termination resistor (e.g., 50 Ω) as shown in Figure 26. The two resistors in series provide the default frequency setting resistance when the signal source is turned off. The sum of the resistance should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10 pF ceramic capacitor to RT/CLK pin.

The first time the RT/CLK is pulled above the PLL threshold the TPS54560-Q1 switches from the RT resistor free-running frequency mode to the PLL synchronized mode. The internal 0.5 V voltage source is removed and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and locks onto the external clock frequency within 78 microseconds. During the transition from the PLL mode to the resistor programmed mode, the switching frequency will fall to 150 kHz and then increase or decrease to the resistor programmed frequency when the 0.5 V bias voltage is reapplied to the RT/CLK resistor.

The switching frequency is divided by 8, 4, 2, and 1 as the FB pin voltage ramps from 0 to 0.8 volts. The device implements a digital frequency foldback to enable synchronizing to an external clock during normal start-up and fault conditions. Figure 27, Figure 28 and Figure 29 show the device synchronized to an external system clock in continuous conduction mode (CCM), discontinuous conduction (DCM), and pulse skip mode (Eco-Mode).
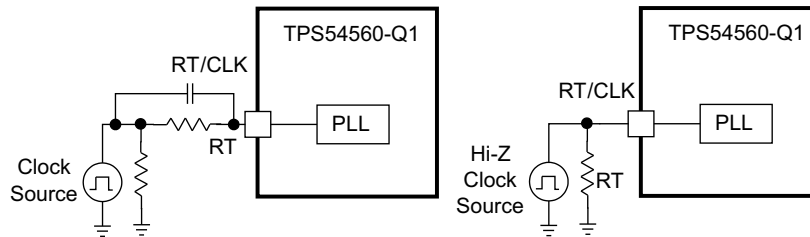
Feature Description (continued)

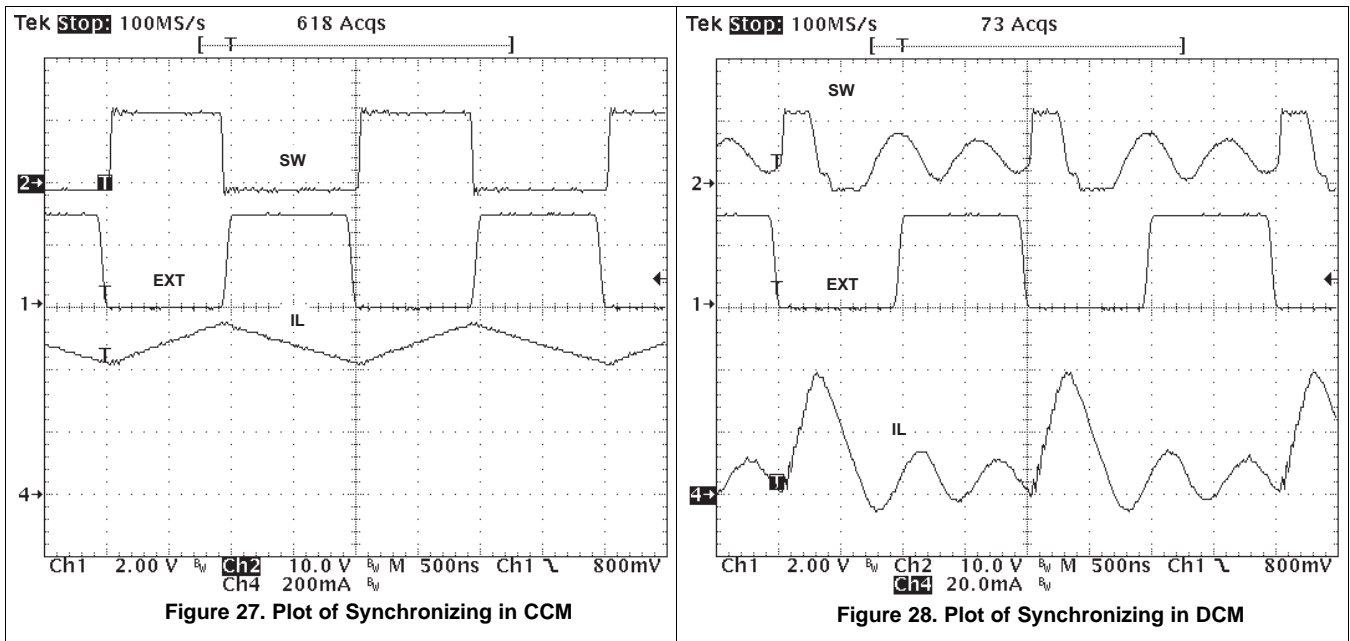**Figure 26. Synchronizing to a System Clock**

Figure 27. Plot of Synchronizing in CCM

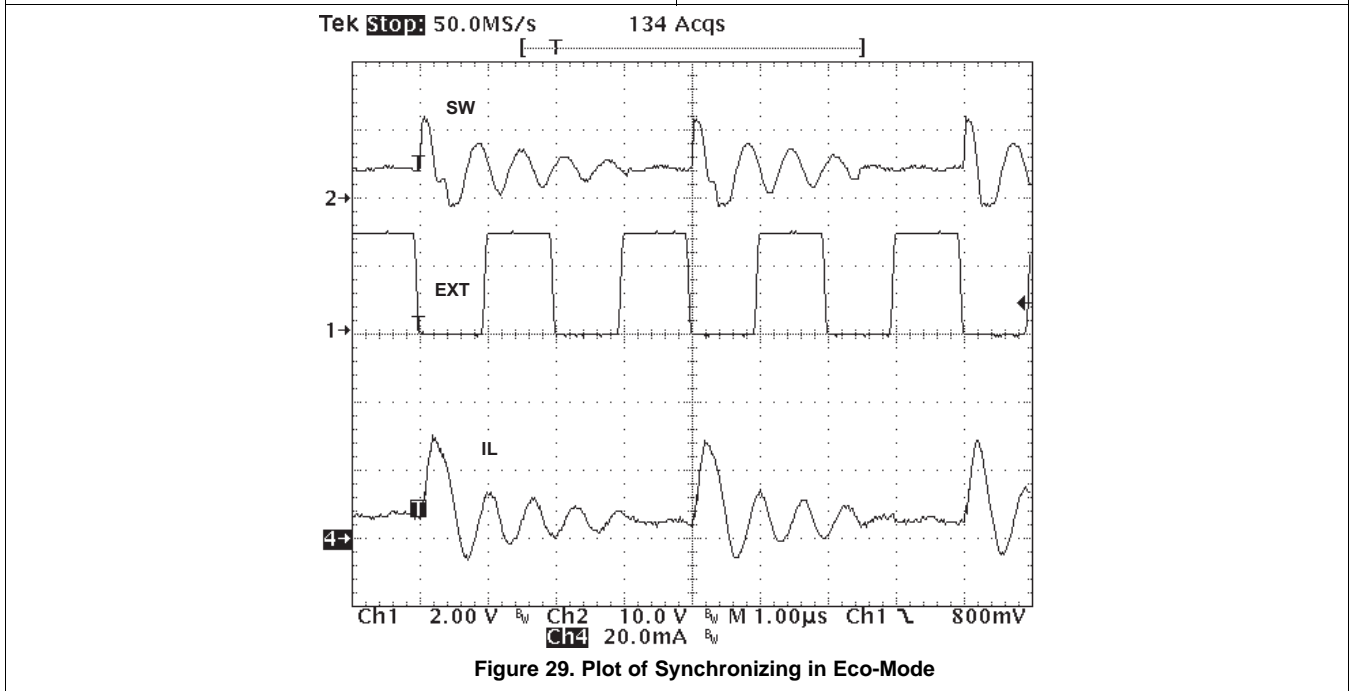

Figure 28. Plot of Synchronizing in DCM

Figure 29. Plot of Synchronizing in Eco-Mode

Feature Description (continued)

7.3.12 Overvoltage Protection

The TPS54560-Q1 incorporates an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will increase to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power supply output voltage can increase faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB pin voltage to the rising OVP threshold which is nominally 109% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high-side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high-side MOSFET resumes normal operation.

7.3.13 Thermal Shutdown

The TPS54560-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high-side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

7.3.14 Small Signal Model for Loop Response

Figure 30 shows an equivalent model for the TPS54560-Q1 control loop which can be simulated to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 350 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_o and capacitor C_o model the open-loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes A and B effectively breaks the control loop for the frequency response measurements. Plotting C/A provides the small signal response of the frequency compensation. Plotting A/B provides the small signal response of the overall loop. The dynamic loop response can be evaluated by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode (CCM) operation.
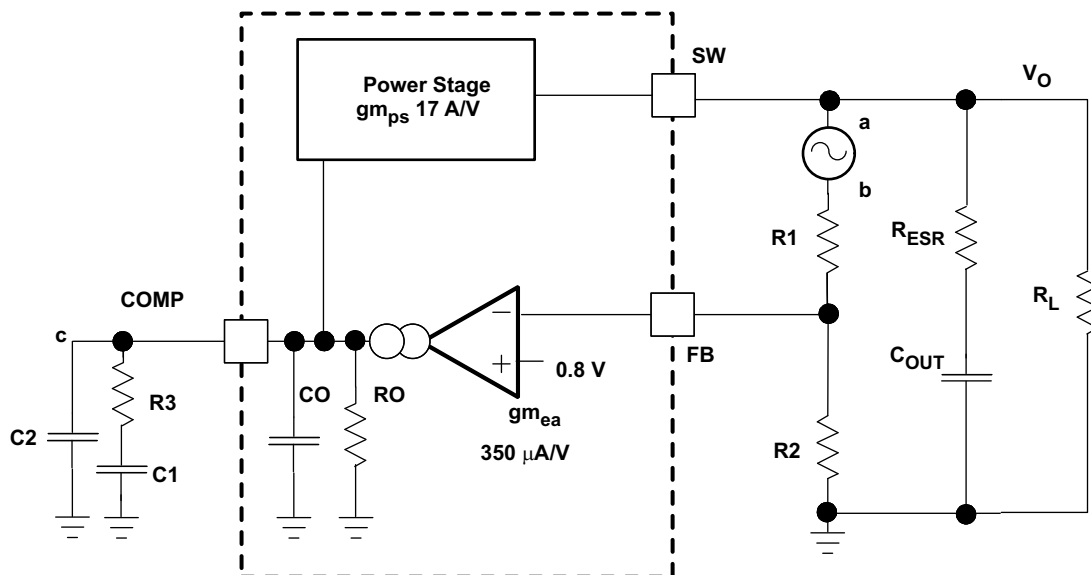

Figure 30. Small Signal Model for Loop Response

Feature Description (continued)

7.3.15 Simple Small Signal Model for Peak Current Mode Control

Figure 31 describes a simple small signal model that can be used to design the frequency compensation. The TPS54560-Q1 power stage can be approximated by a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 10 and consists of a DC gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node C in Figure 30) is the power stage transconductance, gm_{PS}. The gm_{PS} for the TPS54560-Q1 is 17 A/V. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 11.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 12). The combined effect is highlighted by the dashed line in the right half of Figure 31. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high-ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin is increased by the ESR zero of the output capacitor (see Equation 13).
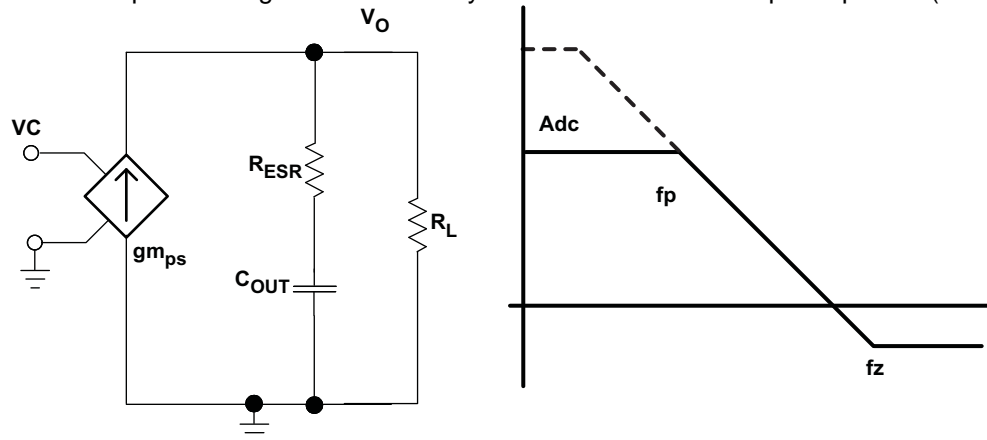
Figure 31. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \dfrac{s}{2\pi \times f_Z}\right)}{\left(1 + \dfrac{s}{2\pi \times f_P}\right)}$$

(10)

$$Adc = gm_{ps} \times R_L$$

(11)

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi}$$

(12)

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi}$$

(13)

7.3.16 Small Signal Model for Frequency Compensation

The TPS54560-Q1 uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 32. Type 2 circuits are typically implemented in high bandwidth power-supply designs using low-ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 14 and Equation 15 relate the frequency response of the amplifier to the small signal model in Figure 32. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 32. See the application section for a design example using a Type 2A network with a low ESR output capacitor.

Feature Description (continued)

Equation 14 through Equation 23 are provided as a reference. An alternative is to use WEBENCH software tools to create a design based on the power supply requirements.
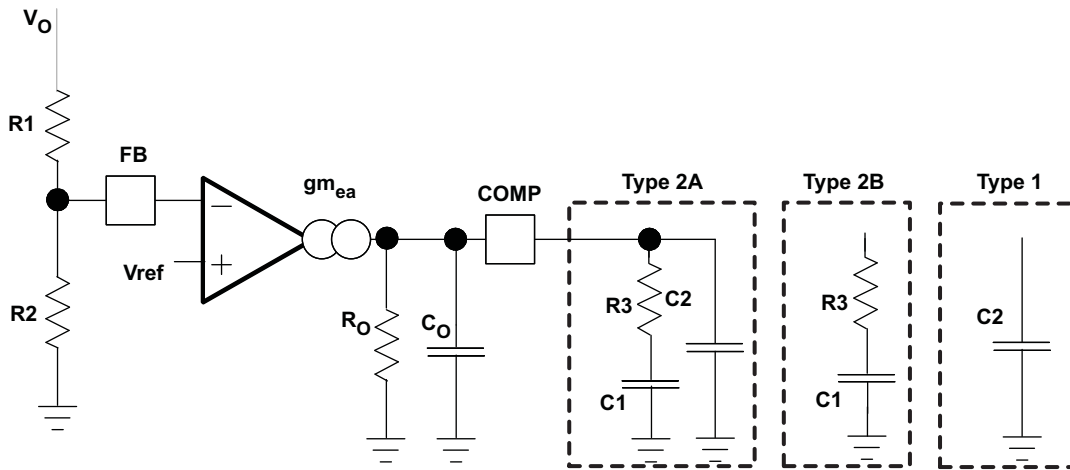
Figure 32. Types of Frequency Compensation
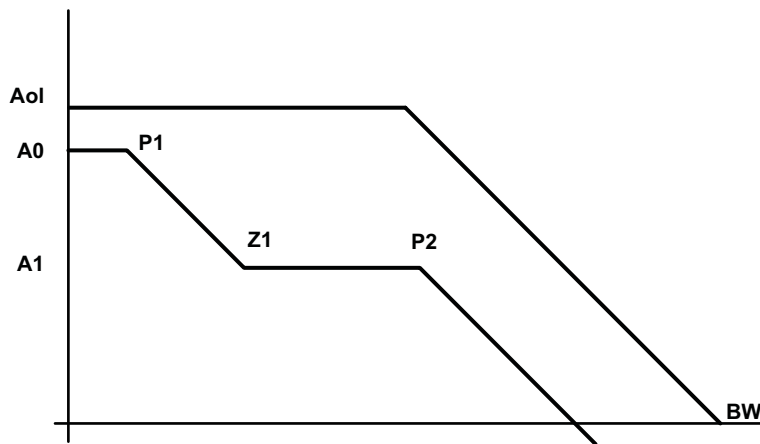
Figure 33. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$Ro = \frac{Aol(V/V)}{gm_{ea}}$$
(14)

$$C_O = \frac{gm_{ea}}{2\pi \times BW \text{ (Hz)}}$$
(15)

$$EA = A0 \times \frac{\left(1 + \dfrac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \dfrac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \dfrac{s}{2\pi \times f_{P2}}\right)}$$
(16)

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2}$$
(17)

$$A1 = gm_{ea} \times Ro||R3 \times \frac{R2}{R1 + R2}$$
(18)

Feature Description (continued)

$$P1 = \frac{1}{2\pi \times Ro \times C1}$$

(19)

$$Z1 = \frac{1}{2\pi \times R3 \times C1}$$

(20)

$$P2 = \frac{1}{2\pi \times R3 \,||\, R_O \times (C2 + C_O)} \text{ type 2a}$$

(21)

$$P2 = \frac{1}{2\pi \times R3 \,||\, R_O \times C_O} \text{ type 2b}$$

(22)

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{ type 1}$$

(23)

7.4 Device Functional Modes

7.4.1 Operation With V_I = 4.5 V (Minimum V_{DD})

TI recommends operating the TPS54561-Q1 device with input voltages above 4.5 V. The typical V_{DD} UVLO threshold is 4.3 V, and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If an external resistor divider pulls the EN pin up to V_{DD} or EN pin is floating, when V_{DD} passes the UVLO threshold the device becomes active. Switching begins, and the soft-start sequence initiates. The TPS54561-Q1 device starts at the soft-start time determined by the external capacitance on the SS/TR pin

7.4.2 Operation With EN Control

The enable threshold voltage is 1.2 V typical. With EN held below that voltage, the device shuts down and switching stops even if V_{DD} is above its UVLO threshold. The IC quiescent current decreases in this state. After increasing the EN pin voltage above the threshold while V_{DD} is above its UVLO threshold, the device becomes active. Switching resumes and the soft-start sequence begins. The TPS54561-Q1 device starts at the soft-start time determined by the external capacitance at the SS/TR pin.

7.4.3 Alternative Power-Supply Topologies

7.4.3.1 Inverting Power Supply

One use of the TPS54561-Q1 is to convert a positive input voltage to a negative output voltage. Ideal applications are amplifiers requiring a negative power supply. For a more-detailed example, see *Create an Inverting Power Supply From a Step-Down Regulator*, application report SLVA317.

Device Functional Modes (continued)
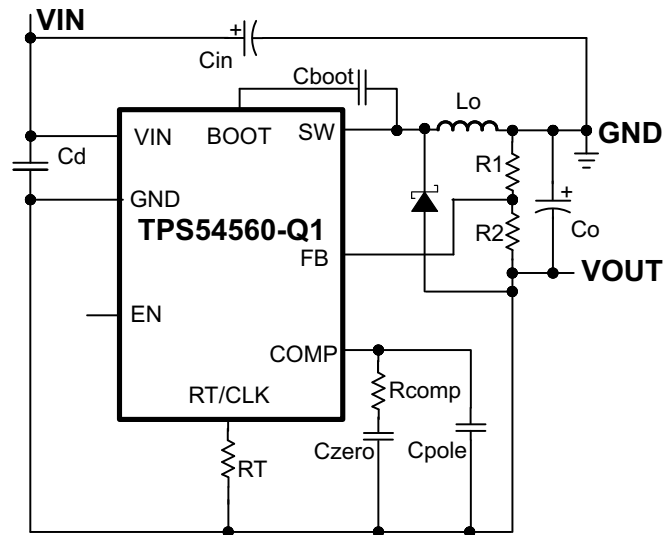
Figure 34. TPS54560-Q1 Inverting Power Supply from SLVA317 Application Note

7.4.3.2 Split-Rail Power Supply

Another use of the TPS54561-Q1 device is to convert a positive input voltage to a split-rail positive- and negative-output voltage by using a coupled inductor. Ideal applications are amplifiers requiring a split-rail positive- and negative-voltage power supply. For a more-detailed example, see *Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator*, application report SLVA369.
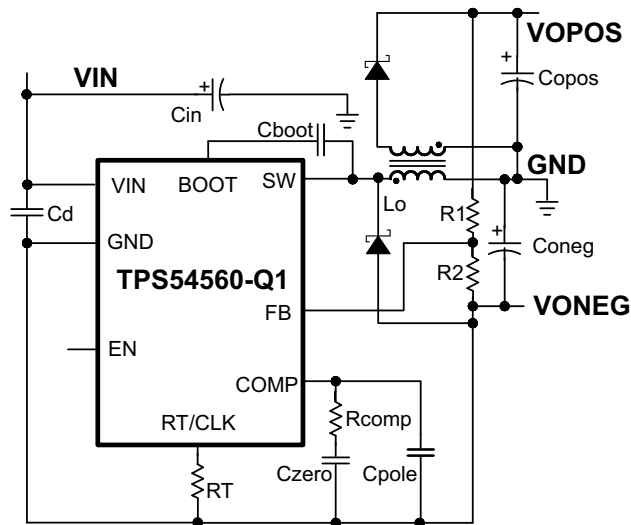
Figure 35. TPS54560-Q1 Split Rail Power Supply based on the SLVA369 Application Note

8 Applications and Implementation

> **NOTE**
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54560-Q1 device is a 60-V, 5-A, step-down regulator with an integrated high-side MOSFET. This device typically converts a higher DC voltage to a lower DC voltage with a maximum available output current of 5 A. Example applications are: 12-V, 24-V and 48-V industrial, automotive and communication power systems. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

8.2 Typical Application
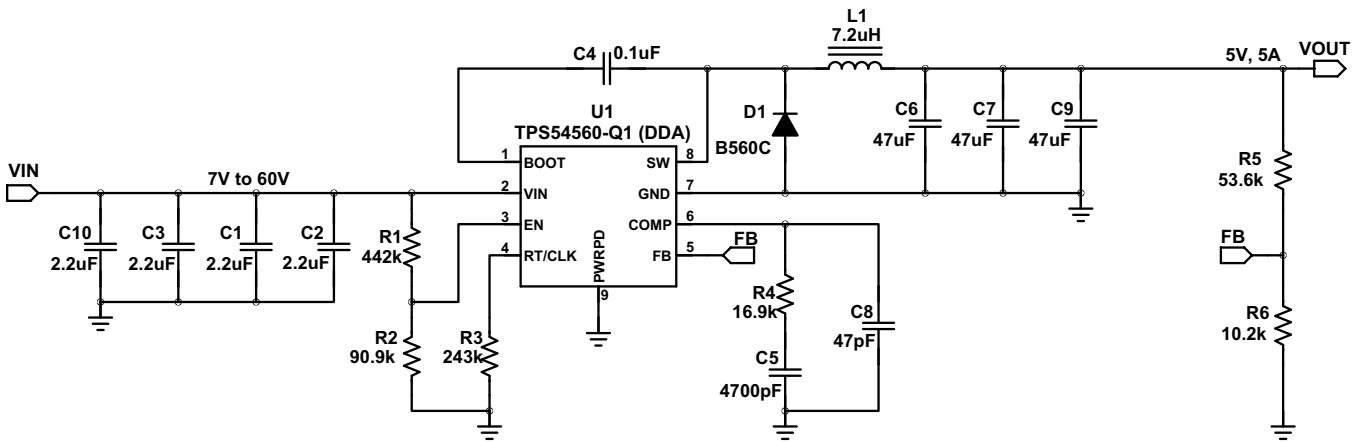
Figure 36. 5 V Output TPS54560-Q1 Design Example

8.2.1 Design Requirements

A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. Calculations can be done with the aid of WEBENCH or the excel spreadsheet (SLVC452) located on the product page. This example is designed to the following known parameters:

PARAMETER	UNIT
Output Voltage	5 V
Transient Response 1.25 A to 3.75 A load step	ΔV_{OUT} = 4 %
Maximum Output Current	5 A
Input Voltage	12 V nom. 7 V to 60 V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	6.5 V
Stop Input Voltage (falling VIN)	5 V

8.2.2 Detailed Design Procedure

Use the following design procedure to select component values for the TPS54560-Q1 device.

8.2.2.1 Selecting the Switching Frequency

The first step is to choose a switching frequency for the regulator. Typically, the designer uses the highest switching frequency possible since this produces the smallest solution size. High switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage and the frequency foldback protection.

Equation 8 and Equation 9 should be used to calculate the upper limit of the switching frequency for the regulator. Choose the lower value result from the two equations. Switching frequencies higher than these values results in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 135 ns for the TPS54560-Q1. For this example, the output voltage is 5 V and the maximum input voltage is 60 V, which allows for a maximum switch frequency up to 708 kHz to avoid pulse skipping from Equation 8. To ensure overcurrent runaway is not a concern during short circuits use Equation 9 to determine the maximum switching frequency for frequency foldback protection. With a maximum input voltage of 60 V, assuming a diode voltage of 0.7 V, inductor resistance of 11 mΩ, switch resistance of 92 mΩ, a current limit value of 6 A and short circuit output voltage of 0.1 V, the maximum switching frequency is 855 kHz.

For this design, a lower switching frequency of 400 kHz is chosen to operate comfortably below the calculated maximums. To determine the timing resistance for a given switching frequency, use Equation 6 or the curve in Figure 6. The switching frequency is set by resistor R_3 shown in Figure 36. For 400 kHz operation, the closest standard value resistor is 243 kΩ.

$$f_{SW(max\,skip)} = \frac{1}{135ns} \times \left(\frac{5\,A \times 11\,m\Omega + 5\,V + 0.7\,V}{60\,V - 5\,A \times 92\,m\Omega + 0.7\,V} \right) = 708\ kHz \tag{24}$$

$$f_{SW(shift)} = \frac{8}{135\ ns} \times \left(\frac{6\,A \times 11\,m\Omega + 0.1\,V + 0.7\,V}{60\,V - 6\,A \times 92\,m\Omega + 0.7\,V} \right) = 855\ kHz \tag{25}$$

$$RT\ (k\Omega) = \frac{92417}{400\ (kHz)^{0.991}} = 244\ k\Omega \tag{26}$$

8.2.2.2 Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 27.

K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be desirable. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Since the inductor ripple current is part of the current mode PWM control system, the inductor ripple current should always be greater than 150 mA for stable PWM operation. In a wide input voltage regulator, it is best to choose relatively large inductor ripple current. This provides sufficienct ripple current with the input voltage at the minimum.

For this design example, K_{IND} = 0.3 and the inductor value is calculated to be 7.6 μH. The nearest standard value is 7.2 μH. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from Equation 29 and Equation 30. For this design, the RMS inductor current is 5 A and the peak inductor current is 5.8 A. The chosen inductor is a WE 7447798720, which has a saturation current rating of 7.9 A and an RMS current rating of 6 A.

As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch current limit of the TPS54560-Q1 which is nominally 7.5 A.

$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} = \frac{60\text{ V} - 5\text{ V}}{5\text{ A} \times 0.3} \times \frac{5\text{ V}}{60\text{ V} \times 400\text{ kHz}} = 7.6\ \mu\text{H}$$

(27)

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} = \frac{5\text{ V} \times (60\text{ V} - 5\text{ V})}{60\text{ V} \times 7.2\ \mu\text{H} \times 400\text{ kHz}} = 1.591\text{ A}$$

(28)

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}}\right)^2} = \sqrt{(5\text{ A})^2 + \frac{1}{12} \times \left(\frac{5\text{ V} \times (60\text{ V} - 5\text{ V})}{60\text{ V} \times 7.2\ \mu\text{H} \times 400\text{ kHz}}\right)^2} = 5\text{ A}$$

(29)

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 5\text{ A} + \frac{1.591\text{ A}}{2} = 5.797\text{ A}$$

(30)

8.2.2.3 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for 2 clock cycles to maintain the output voltage within the specified range. Equation 31 shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, $f$sw is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 1.25 A to 3.75 A. Therefore, ΔI_{OUT} is 3.75 A - 1.25 A = 2.5 A and $\Delta V_{OUT} = 0.04 \times 5 = 0.2$ V. Using these numbers gives a minimum capacitance of 62.5 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be included in load step calculations.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator can not sink current so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. A typical load step response is shown in Figure 37. The excess energy absorbed in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 32 calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where L_O is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the peak output voltage, and Vi is the initial voltage. For this example, the worst case load step will be from 3.75 A to 1.25 A. The output voltage increases during this load transition and the stated maximum in our specification is 4 % of the output voltage. This makes $V_f = 1.04 \times 5 = 5.2$. Vi is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 32 yields a minimum capacitance of 44.1 µF.

Equation 33 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where $f$sw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. Equation 33 yields 19.9 µF.

Equation 34 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 34 indicates the ESR should be less than 15.7 mΩ.

The most stringent criteria for the output capacitor is 62.5 µF required to maintain the output voltage within regulation tolerance during a load transient.

Capacitance de-ratings for aging, temperature and dc bias increases this minimum value. For this example, 3 x 47 µF, 10 V ceramic capacitors with 5 mΩ of ESR will be used. The derated capacitance is 87.4 µF, well above the minimum required capacitance of 62.5 µF.

Capacitors are generally rated for a maximum ripple current that can be filtered without degrading capacitor reliability. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. Equation 35 can be used to calculate the RMS ripple current that the output capacitor must support. For this example, Equation 35 yields 459 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 2.5\ A}{400\ kHz \times 0.2\ V} = 62.5\ \mu F \tag{31}$$

$$C_{OUT} > L_O \ x \ \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_I)^2\right)} = 7.2\ \mu H \ x \ \frac{\left(3.75\ A^2 - 1.25\ A^2\right)}{\left(5.2\ V^2 - 5\ V^2\right)} = 44.1\ \mu F \tag{32}$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\dfrac{V_{ORIPPLE}}{I_{RIPPLE}}\right)} = \frac{1}{8 \times 400\ kHz} \ x \ \frac{1}{\left(\dfrac{25\ mV}{1.591\ A}\right)} = 19.9\ \mu F \tag{33}$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} = \frac{25\ mV}{1.591\ A} = 15.7\ m\Omega \tag{34}$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} = \frac{5\ V \times (60\ V - 5\ V)}{\sqrt{12} \times 60\ V \times 7.2\ \mu H \times 400\ kHz} = 459\ mA \tag{35}$$

8.2.2.4 Catch Diode

The TPS54560-Q1 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60 V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the TPS54560-Q1.

For the example design, the B560C-13-F Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the B560C-13-F is 0.70 volts at 5 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 36 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The B560C-13-F diode has a junction capacitance of 300 pF. Using Equation 36, the total loss in the diode at the maximum input voltage is 3.43 Watts.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times V\!fd}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times (V_{IN} + V\!fd)^2}{2} =$$

$$\frac{(60\ V\ -\ 5\ V) \times 5\ A \times 0.7\ V}{60\ V} + \frac{300\ pF \times 400\ kHz \times (60\ V\ +\ 0.7\ V)^2}{2} = 3.43\ W \tag{36}$$

8.2.2.5 Input Capacitor

The TPS54560-Q1 requires a high quality ceramic type X5R or X7R input decoupling capacitor with at least 3 µF of effective capacitance. Some applications will benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance due to dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54560-Q1. The input ripple current can be calculated using Equation 37.

The value of a ceramic capacitor varies significantly with temperature and the dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is more stable over temperature. X5R and X7R ceramic dielectrics are usually selected for switching regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with consideration for the dc bias. The effective value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 60 V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V. For this example, four 2.2 µF, 100 V capacitors in parallel are used. Table 1 shows several choices of high voltage capacitors.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 38. Using the design example values, I_{OUT} = 5 A, C_{IN} = 8.8 µF, $f$sw = 400 kHz, yields an input voltage ripple of 355 mV and a rms input ripple current of 2.26 A.

$$I_{CI(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 5\ A \sqrt{\frac{5\ V}{7\ V} \times \frac{(7\ V\ -\ 5\ V)}{7\ V}} = 2.26\ A \tag{37}$$

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} = \frac{5\ A \times 0.25}{8.8\ \mu F \times 400\ kHz} = 355\ mV \tag{38}$$

Table 1. Capacitor Types

VENDOR	VALUE (µF)	EIA Size	VOLTAGE	DIALECTRIC	COMMENTS
Murata	1 to 2.2	1210	100 V	X7R	GRM32 series
	1 to 4.7		50 V		
	1	1206	100 V		GRM31 series
	1 to 2.2		50 V		
Vishay	1 to 1.8	2220	50 V		VJ X7R series
	1 to 1.2		100 V		
	1 to 3.9	2225	50 V		
	1 to 1.8		100 V		
TDK	1 to 2.2	1812	100 V		C series C4532
	1.5 to 6.8		50 V		
	1 to 2.2	1210	100 V		C series C3225
	1 to 3.3		50 V		
AVX	1 to 4.7	1210	50 V		X7R dielectric series
	1		100 V		
	1 to 4.7	1812	50 V		
	1 to 2.2		100 V		

8.2.2.6 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10 V or higher voltage rating.

8.2.2.7 Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54560-Q1. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 6.5 V (UVLO start). After the regulator starts switching, it should continue to do so until the input voltage falls below 5 V (UVLO stop).

Programmable UVLO threshold voltages are set using the resistor divider of R_{UVLO1} and R_{UVLO2} between VIN and ground connected to the EN pin. Equation 3 and Equation 4 calculate the resistance values necessary. For the example application, a 442 kΩ between V_{IN} and EN (R_{UVLO1}) and a 90.9 kΩ between EN and ground (R_{UVLO2}) are required to produce the 6.5 V and 5 V start and stop voltages.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} = \frac{6.5\,V - 5\,V}{3.4\,\mu A} = 441\,k\Omega \tag{39}$$

$$R_{UVLO2} = \frac{V_{ENA}}{\dfrac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} = \frac{1.2\,V}{\dfrac{6.5\,V - 1.2\,V}{442\,k\Omega} + 1.2\,\mu A} = 90.9\,k\Omega \tag{40}$$

8.2.2.8 Output Voltage and Feedback Resistors Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, 10.2 kΩ was selected for R6. Using Equation 2, R5 is calculated as 53.5 kΩ. The nearest standard 1% resistor is 53.6 kΩ. Due to the input current of the FB pin, the current flowing through the feedback network should be greater than 1 µA to maintain the output voltage accuracy. This requirement is satisfied if the value of R6 is less than 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - 0.8\,V}{0.8\,V} = 10.2\,k\Omega \times \left(\frac{5\,V - 0.8\,V}{0.8\,V} \right) = 53.5\,k\Omega \tag{41}$$

8.2.2.9 Compensation

There are several methods to design compensation for DC-DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual crossover frequency will be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole.

To get started, the modulator pole, $f_{p(mod)}$, and the ESR zero, f_{z1} must be calculated using Equation 42 and Equation 43. For C_{OUT}, use a derated value of 87.4 µF. Use equations Equation 44 and Equation 45 to estimate a starting point for the crossover frequency, $f$co. For the example design, $f_{p(mod)}$ is 1821 Hz and $f_{z(mod)}$ is 1100 kHz. Equation 43 is the geometric mean of the modulator pole and the ESR zero and Equation 45 is the mean of modulator pole and half of the switching frequency. Equation 44 yields 44.6 kHz and Equation 45 gives 19.1 kHz. Use the geometric mean value of Equation 44 and Equation 45 for an initial crossover frequency. For this example, after lab measurement, the crossover frequency target was increased to 30 kHz for an improved transient response.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{5\,A}{2 \times \pi \times 5\,V \times 87.4\,\mu F} = 1821\,Hz \tag{42}$$

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2 \times \pi \times 1.67\,m\Omega \times 87.4\,\mu F} = 1100\,kHz \tag{43}$$

$$f_{co1} = \sqrt{f_{p(mod)} \times f_{z(mod)}} = \sqrt{1821\,Hz \times 1100\,kHz} = 44.6\,kHz \tag{44}$$

$$f_{co2} = \sqrt{f_{p(mod)} \times \frac{f_{SW}}{2}} = \sqrt{1821\,Hz \times \frac{400\,kHz}{2}} = 19.1\,kHz \tag{45}$$

To determine the compensation resistor, R4, use Equation 46. Assume the power stage transconductance, gmps, is 17 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 5 V, 0.8 V and 350 μA/V, respectively. R4 is calculated to be 16.8 kΩ and a standard value of 16.9 kΩ is selected. Use Equation 47 to set the compensation zero to the modulator pole frequency. Equation 47 yields 5172 pF for compensating capacitor C5. 4700 pF is used for this design.

$$R4 = \left(\frac{2 \times \pi \times f_{co} \times C_{OUT}}{gmps}\right) \times \left(\frac{V_{OUT}}{V_{REF} \times gmea}\right) = \left(\frac{2 \times \pi \times 29.2\,kHz \times 87.4\,\mu F}{17\,A/V}\right) \times \left(\frac{5V}{0.8\,V \times 350\,\mu A/V}\right) = 16.8\,k\Omega \tag{46}$$

$$C5 = \frac{1}{2 \times \pi \times R4 \times f_{p(mod)}} = \frac{1}{2 \times \pi \times 16.9\,k\Omega \times 1821\,Hz} = 5172\,pF \tag{47}$$

A compensation pole can be implemented if desired by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from Equation 48 and Equation 49 for C8 to set the compensation pole. The selected value of C8 is 47 pF for this design example.

$$C8 = \frac{C_{OUT} \times R_{ESR}}{R4} = \frac{87.4\,\mu F \times 1.67\,m\Omega}{16.9\,k\Omega} = 8.64\,pF \tag{48}$$
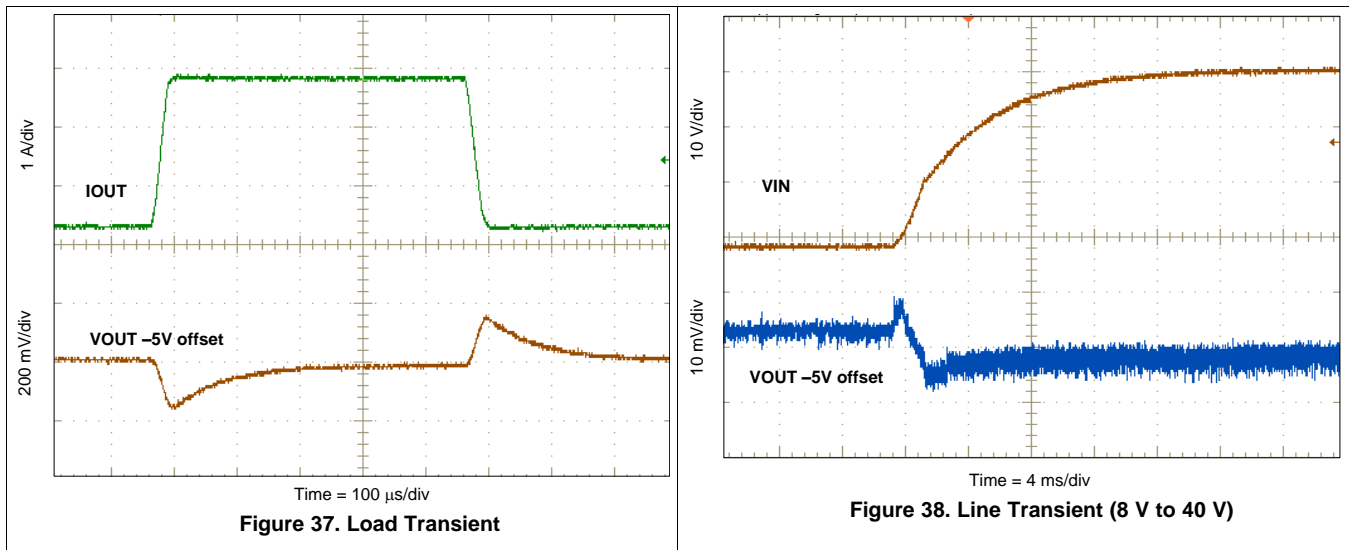
$$C8 = \frac{1}{R4 \times f_{sw} \times \pi} = \frac{1}{16.9\,k\Omega \times 400\,kHz \times \pi} = 47.1\,pF \tag{49}$$

8.2.2.10 Discontinuous Conduction Mode and Eco-Mode Boundary

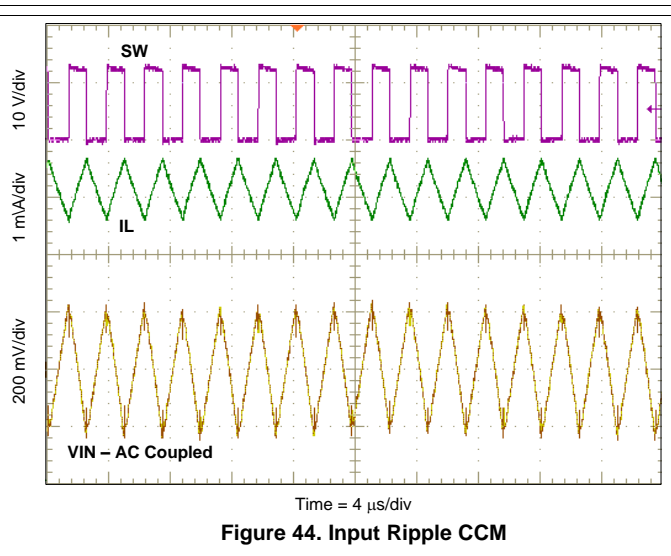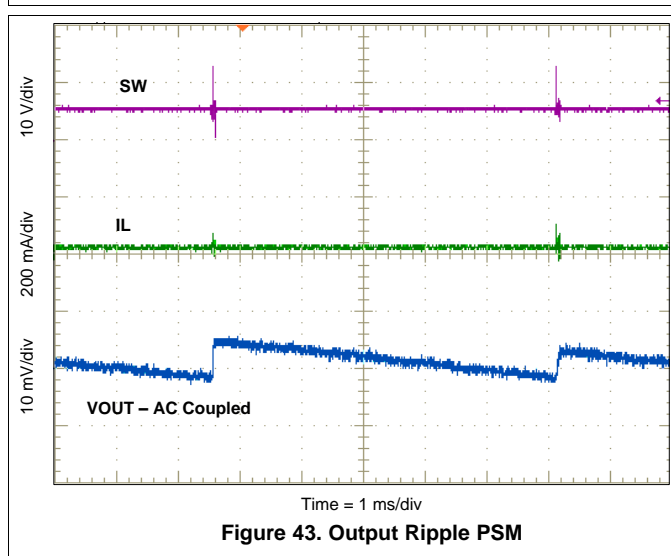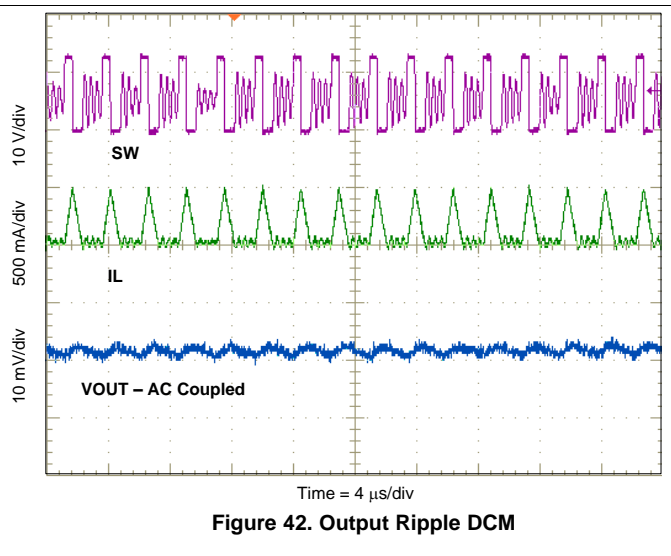With an input voltage of 12 V, the power supply enters discontinuous conduction mode when the output current is less than 408 mA. The power supply enters Eco-Mode when the output current is lower than 25.3 mA. The input current draw is 257 μA with no load.

8.2.3 Application Curves

Measurements are taken with standard EVM using a 12V input, 5V output, and 5A load unless otherwise noted.

Time = 100 μs/div

Figure 37. Load Transient

Time = 4 ms/div

Figure 38. Line Transient (8 V to 40 V)

Measurements are taken with standard EVM using a 12V input, 5V output, and 5A load unless otherwise noted.

Figure 39. Start-up With VIN

Time = 2 ms/div

Figure 40. Start-up With EN

Time = 2 ms/div

Figure 41. Output Ripple CCM

Time = 4 μs/div

Figure 42. Output Ripple DCM

Time = 4 μs/div

Figure 43. Output Ripple PSM

Time = 1 ms/div

Figure 44. Input Ripple CCM

Time = 4 μs/div
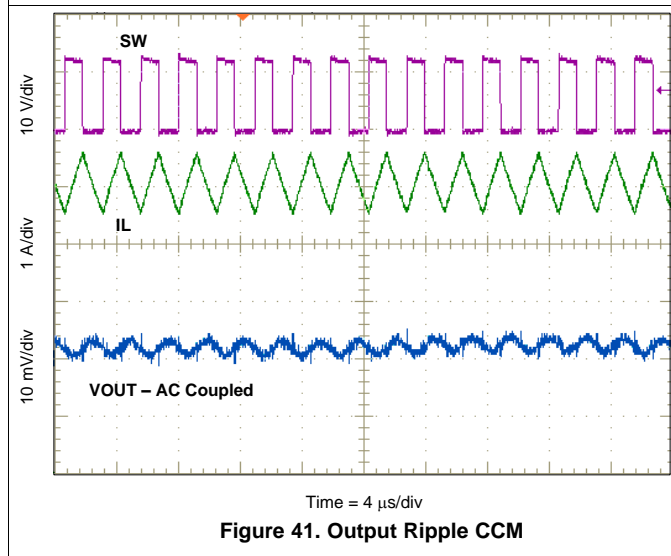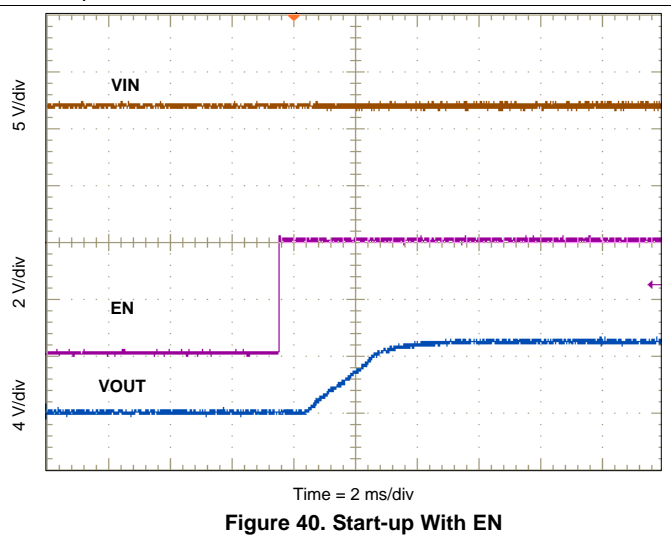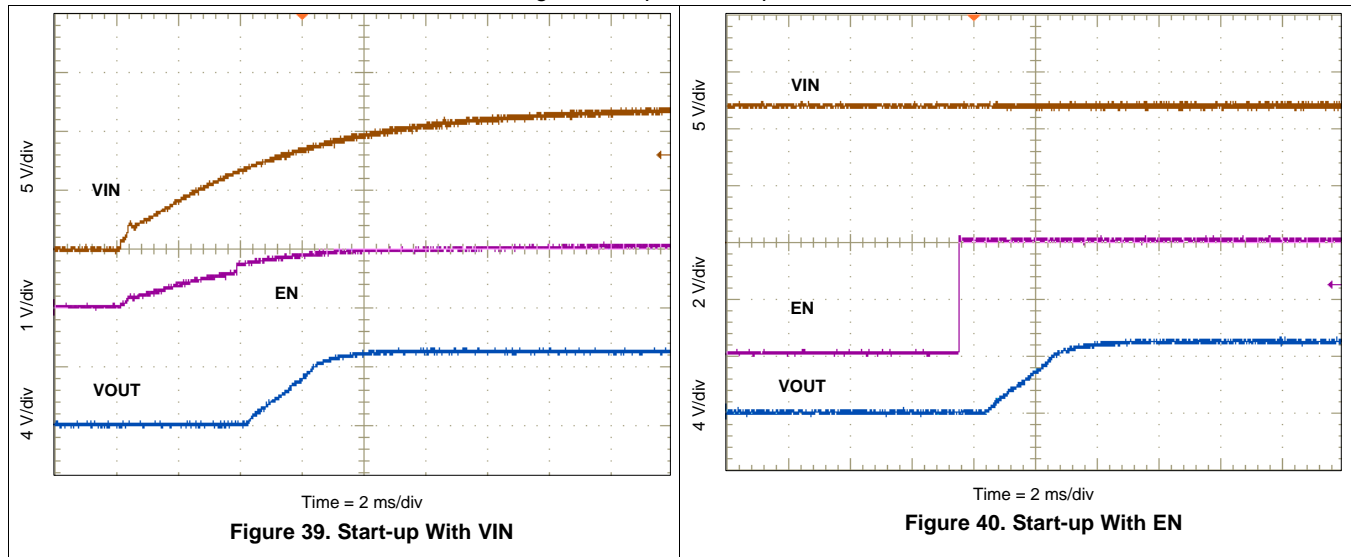
Measurements are taken with standard EVM using a 12V input, 5V output, and 5A load unless otherwise noted.

Figure 45. Input Ripple DCM

Figure 46. Low Dropout Operation
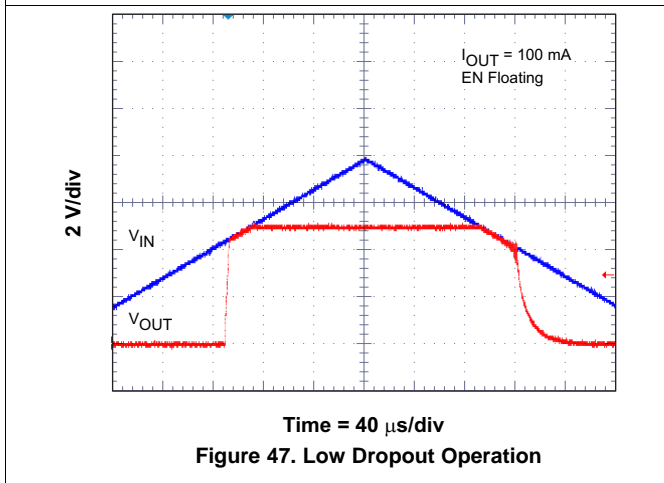
Figure 47. Low Dropout Operation
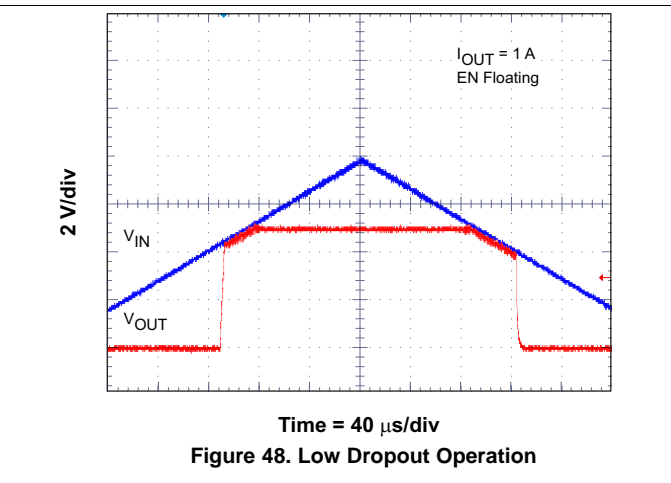
Figure 48. Low Dropout Operation
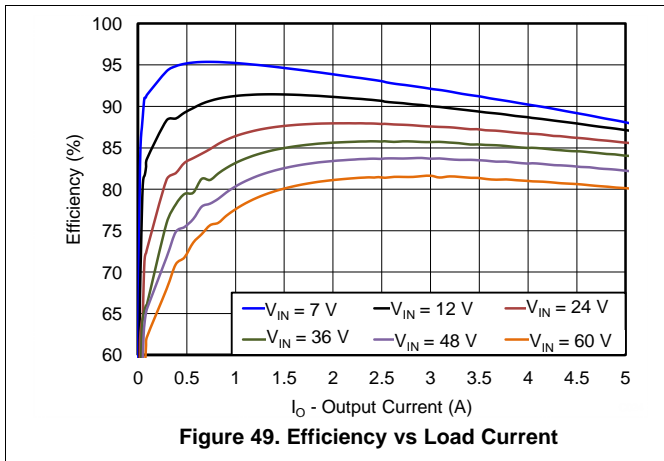
Figure 49. Efficiency vs Load Current
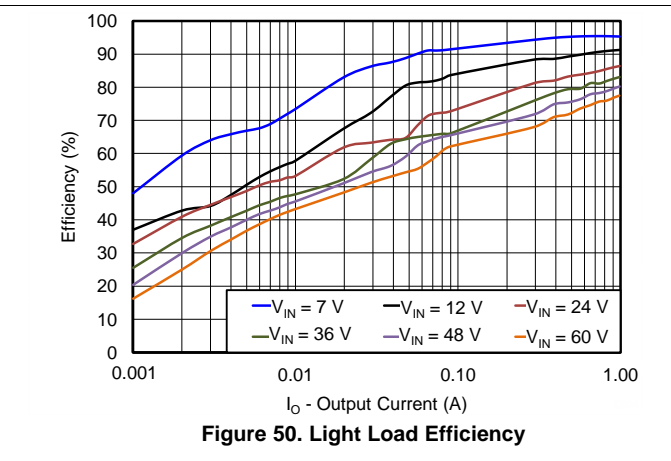
Figure 50. Light Load Efficiency

Measurements are taken with standard EVM using a 12V input, 5V output, and 5A load unless otherwise noted.
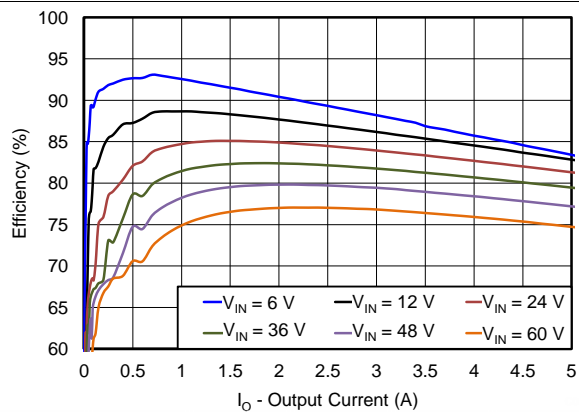
Figure 51. Efficiency vs Load Current
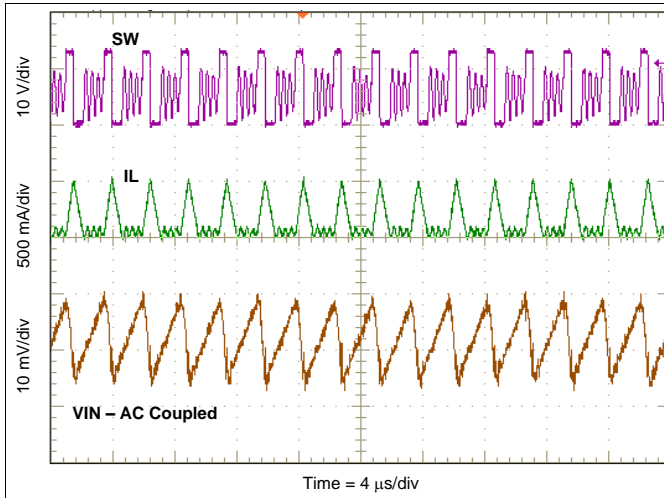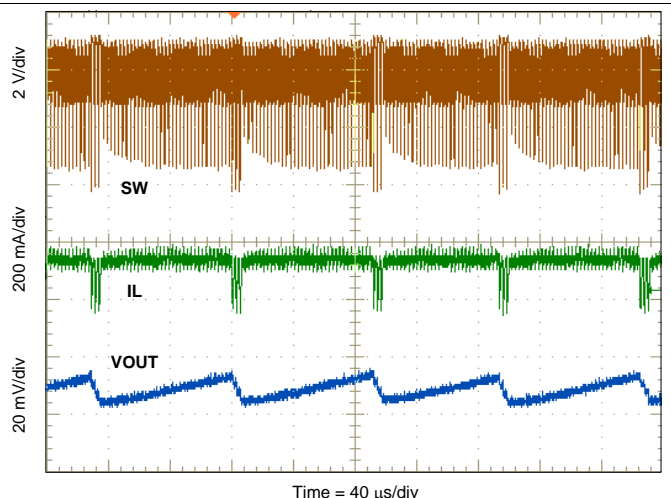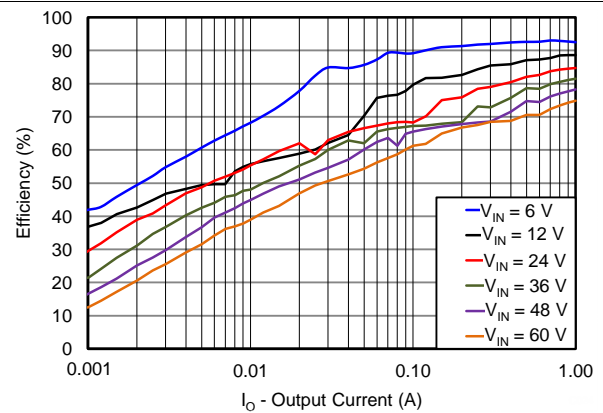

Figure 52. Light Load Efficiency
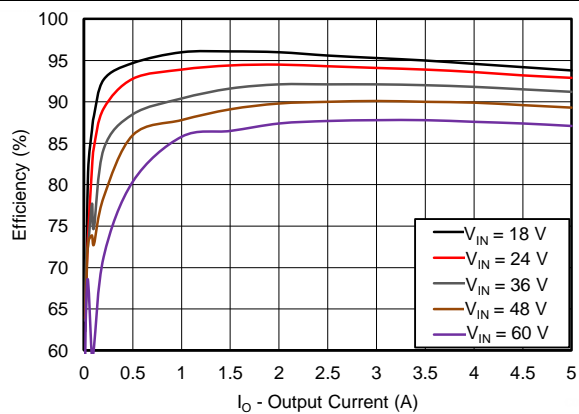
Figure 53. Efficiency vs Output Current
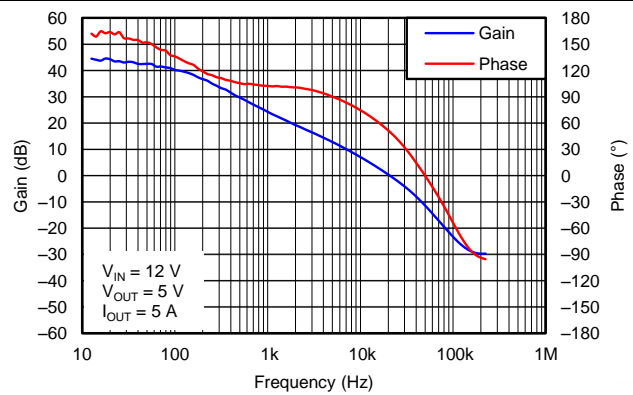
Figure 54. Overall Loop Frequency Response
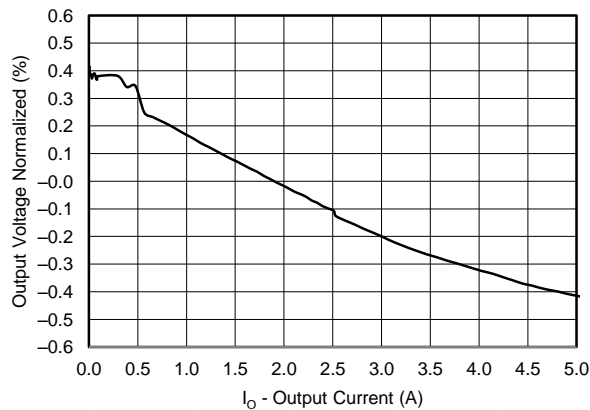
Figure 55. Regulation vs Load Current
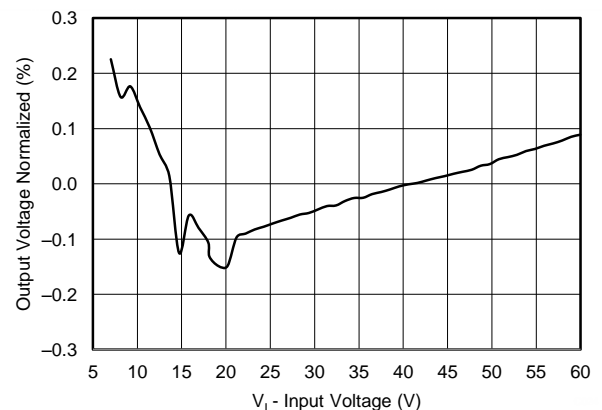
Figure 56. Regulation vs Input Voltage

9 Power Supply Recommendations

The design of the device is for operation from an input voltage supply range between 4.5 V and 60 V. Good regulation of this input supply is essential. If the input supply is more distant than a few inches from the TPS54560-Q1 converter, the circuit may require additional bulk capacitance besides the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice. Furthermore, if the supply voltage in the application is likely to reach negative voltage (for example, reverse battery) a forward diode must be placed at the input of the supply.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. To reduce parasitic effects, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the A node of the catch diode. See Figure 57 for a PCB layout example. The GND pin should be tied directly to the power pad under the IC and the power pad.

The power pad should be connected to internal PCB ground planes using multiple vias directly under the IC. The SW pin should be routed to the cathode of the catch diode and to the output inductor. Since the SW connection is the switching node, the catch diode and output inductor should be located close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

Figure 57. PCB Layout Example

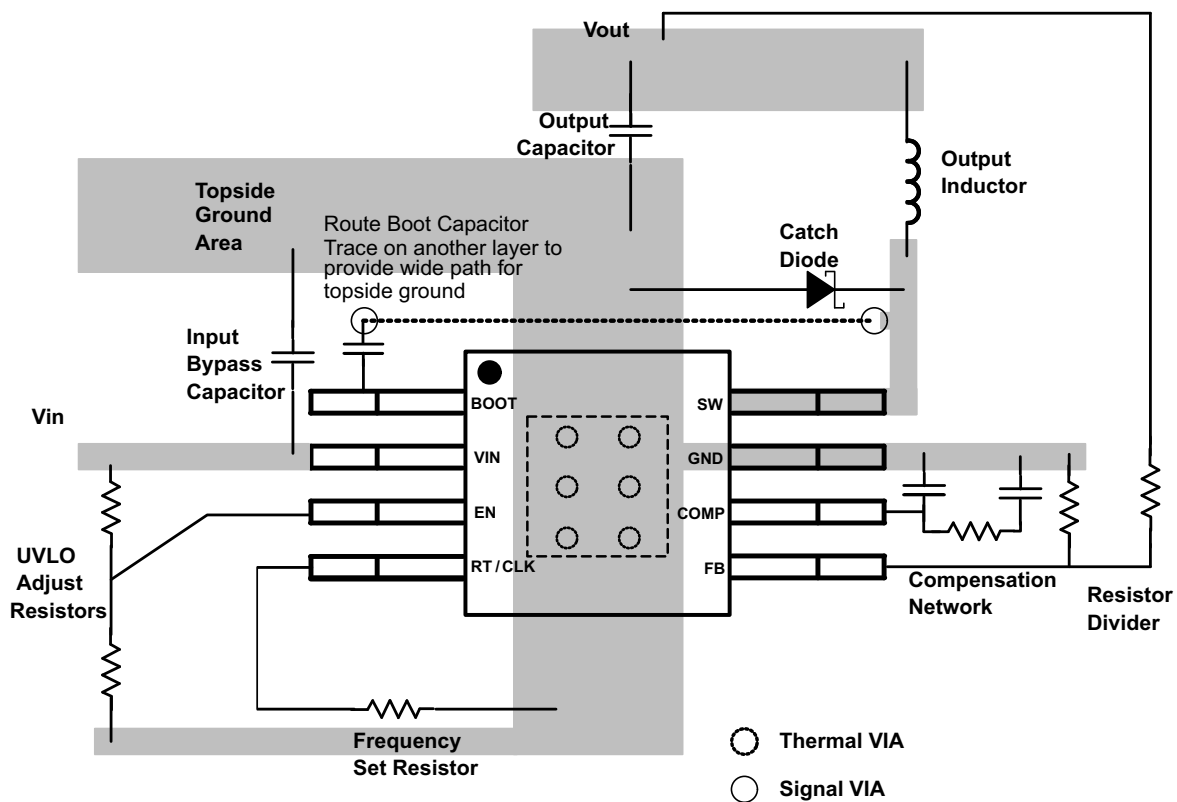## 10.3 Power Dissipation

The following formulas show how to estimate the TPS54560-Q1 power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is operating in discontinuous conduction mode (DCM).

Power Dissipation (continued)

The power dissipation of the IC includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}) and supply current (P_Q). Example calculations are shown with the 12 V typical input voltage of the design example.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}}\right) = 5\ A^2 \times 92\ m\Omega \times \frac{5\ V}{12\ V} = 0.958\ W \tag{50}$$

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times t_{rise} = 12\ V \times 400\ kHz \times 5\ A \times 4.9\ ns = 0.118\ W \tag{51}$$

$$P_{GD} = V_{IN} \times Q_G \times f_{SW} = 12\ V \times 3nC \times 400\ kHz = 0.014\ W \tag{52}$$

$$P_Q = V_{IN} \times I_Q = 12\ V \times 146\ \mu A = 0.0018\ W \tag{53}$$

Where:

I_{OUT} is the output current (A).
$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
V_{OUT} is the output voltage (V).
V_{IN} is the input voltage (V).
fsw is the switching frequency (Hz).
trise is the SW pin voltage rise time and can be estimated by trise = V_{IN} x 0.16 ns/V + 3 ns
Q_G is the total gate charge of the internal MOSFET
I_Q is the operating nonswitching supply current

Therefore,

$$P_{TOT} = P_{COND} + P_{SW} + P_{GD} + P_Q = 0.958\ W + 0.118\ W + 0.014\ W + 0.0018\ W = 1.092\ W \tag{54}$$

For given T_A,

$$T_J = T_A + R_{TH} \times P_{TOT} \tag{55}$$

For given T_{JMAX} = 150°C

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT} \tag{56}$$

Where:

Ptot is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
R_{TH} is the thermal resistance of the package (°C/W).
T_{JMAX} is maximum junction temperature (°C).
T_{AMAX} is maximum ambient temperature (°C).

There will be additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and PCB trace resistance impacting the overall efficiency of the regulator.

10.4 Safe Operating Area

The safe operating area (SOA) of the device is shown in Figure 58, through Figure 61 for 3.3 V, 5 V and 12 V outputs and varying amounts of forced air flow. The temperature derating curves represent the conditions at which the internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a double-sided PCB with 2 oz. copper, similar to the EVM. Careful attention must be paid to the other components chosen for the design, especially the catch diode.

Safe Operating Area (continued)
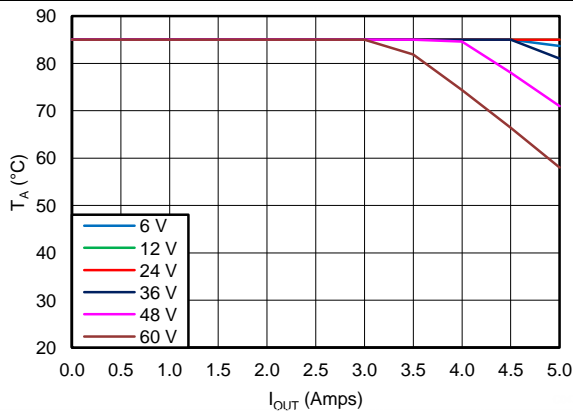
Figure 58. 3.3-V Outputs
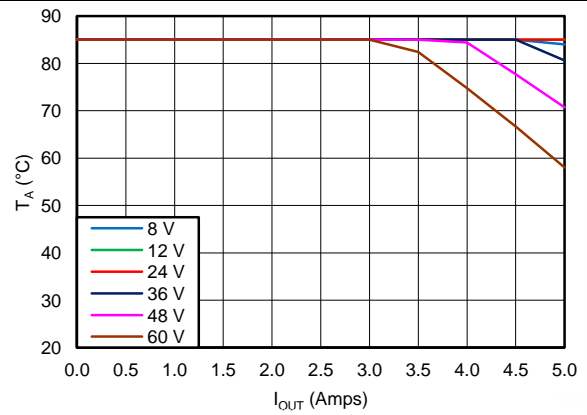
Figure 59. 5-V Outputs
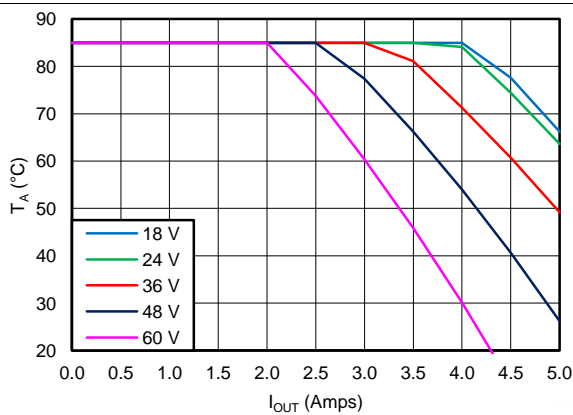
Figure 60. 12-V Outputs
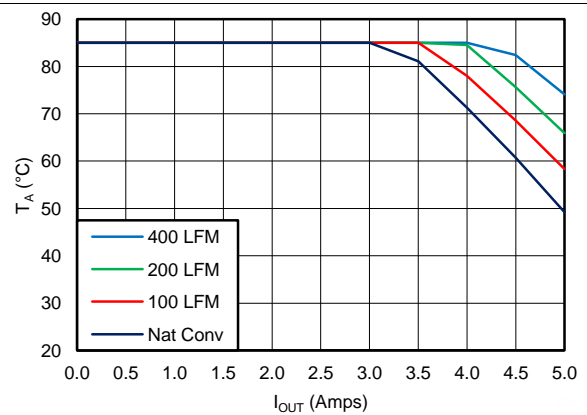
Figure 61. Air Flow Conditions
V_{IN} = 36 V, V_O = 12 V

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

- 《使用降压稳压器创建反向电源》，SLVA317
- 《使用宽范围输入电压降压稳压器创建分离轨电源》，SLVA369

11.2 商标

Eco-mode, PowerPAD are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — TI 术语表。
这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54560QDDAQ1	NRND	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	54560Q	
TPS54560QDDARQ1	NRND	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	54560Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54560QDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54560QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

PACKAGE MATERIALS INFORMATION

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54560QDDAQ1	DDA	HSOIC	8	75	517	7.87	635	4.25

DDA 8

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4202561/G

TEXAS
INSTRUMENTS

DDA (R−PDSO−G8) PowerPAD ™ PLASTIC SMALL−OUTLINE

THERMAL PAD

SIZE AND SHAPE SHOWN
ON SEPARATE SHEET

1,27

8

5

$\frac{0,51}{0,31}$ ⊕ 0,25 Ⓜ

$\frac{4,00}{3,80}$ $\frac{6,20}{5,80}$

1

4

$\frac{5,00}{4,80}$

1,70 MAX

$\frac{0,15}{0,00}$

0,20 NOM

Gage Plane

0°−8°

0,25

$\frac{1,27}{0,40}$

Seating Plane

0,10

4202561/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5−1994.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
      Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
      recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
   E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
   F. This package complies to JEDEC MS−012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R–PDSO–G8)   PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Top View

Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R−PDSO−G8)   PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

solder mask
over copper

4x1,30   1,27

6xØ0,33

2,40 2,95 5,75

3x1,30

3,10

4,90

Example Solder Mask
Defined Pad
(See Note C, D)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,5

2,2

Pad Geometry
(Note C)

0,07
All Around

0,127mm Thick Stencil Design Example
Reference table below for other
solder stencil thicknesses
(Note E)

0,45   1,27

2,15

3,10

Y 2,40

X

5,75

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951−6/D 04/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
            Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>. Publication IPC−7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
            metal load solder paste. Refer to IPC−7525 for other stencil recommendations.
        F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

重要声明和免责声明

TI"按原样"提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。