带有集成 FET 的 TPS54610 3V 至 6V 输入、6A 输出同步降压

1 特性

- 30mΩ、12A 峰值 MOSFET 开关，可在 6A 连续输出拉电流或灌电流下实现高效率
- 可调输出电压低至 0.9V，精度为 1.0%
- 宽泛的 PWM 频率：固定 350kHz、550kHz 或 280kHz 至 700kHz 可调
- 可同步到 700kHz
- 受峰值电流限制和热关断保护的负载
- 集成解决方案可减少电路板面积和组件数
- SWIFT 文档，操作说明书和设计软件，请见：www.ti.com.cn/swift

2 应用

- 低电压、高密度分布式电源系统
- 针对高性能 DSP、FPGA、ASIC 和微处理器的负载点调节
- 宽带、网络及光纤通信基础设施
- 便携式计算/笔记本电脑

3 说明

TPS54610 低输入电压、高输出电流、同步降压 PWM 转换器集成了所有必需的有源组件。除了所列的特性之外， 基板还包含一个真正的高性能电压误差放大器（可实现最高性能，并且可灵活选择输出滤波器 L 和 C 组件）；一个欠压锁定电路（用于防止在输入电压达到 3V 之前启动）；一个内部或外部设置的慢速启动电路（用于限制浪涌电流）；以及一个电源正常状态输出（用于处理器/逻辑复位、故障信令和电源定序）。

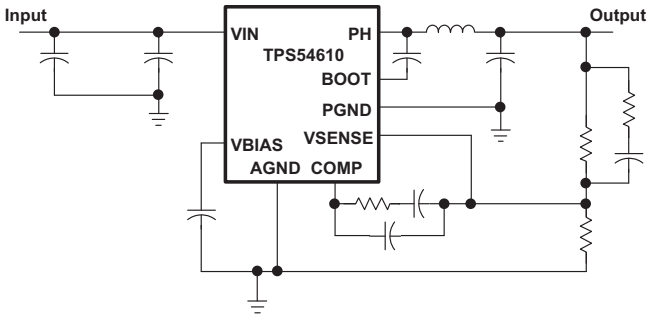
TPS54610 采用热增强型 28 引脚 HTSSOP (PWP) PowerPAD™封装，因而无需大型散热装置。TI 提供评估模块，有助于快速实现高性能电源设计，满足迫切的设备开发周期要求。

器件信息(1)

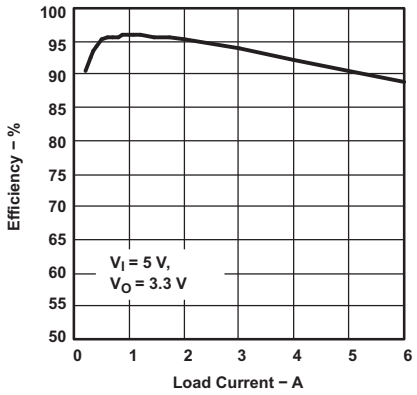
器件名称	封装	封装尺寸（标称值）
TPS54610	HTSSOP (28)	9.70mm x 6.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



在 350 kHz 时的效率



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (October 2015) to Revision H **Page**

- 仅有编辑更改；无技术性更改 ... 1

Changes from Revision F (April 2007) to Revision G **Page**

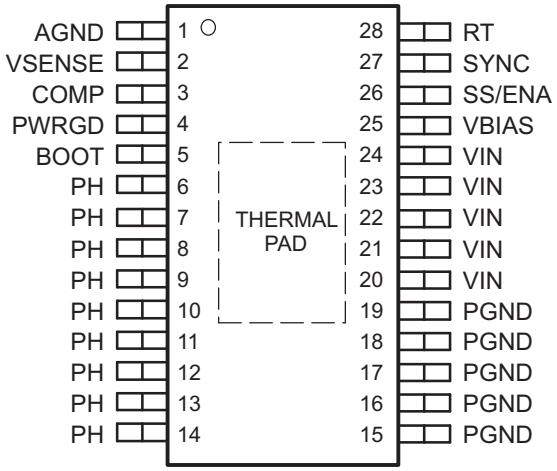
- 已添加 添加了*引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1

5 Device Comparison Table

DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE
TPS54611	0.9 V	TPS54614	1.8 V	TPS54672	DDR Memory/Adjustable
TPS54612	1.2 V	TPS54615	2.5 V	TPS54673	Pre-bias/Adjustable
TPS54613	1.5 V	TPS54616	3.3 V	TPS54680	Sequencing/Adjustable

6 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and SYNC pin. Connect PowerPAD™ to AGND.
BOOT	5	S	Bootstrap output. 0.022-μF to 0.1-μF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3		Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15-19	G	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative pins of the input and output capacitors. A single point connection to AGND is recommended.
PH	6-14	O	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PWRGD	4	O	Power good open drain output. High when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	I	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency. When using the SYNC pin, set the RT value for a frequency at or slightly lower than the external oscillator frequency.
SS/ENA	26	I/O	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	27	I/O	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	25	S	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-μF to 1.0-μF ceramic capacitor.

(1) I = Input, O = Output, S = Supply, G = Ground Return

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN	20-24	I	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low-ESR 10-μF ceramic capacitor.
VSENSE	2	I	Error amplifier inverting input. Connect to output voltage through compensation network/output divider.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

			MIN	MAX	UNIT
V_I	Input voltage	VIN, SS/ENA, SYNC	–0.3	7	V
		RT	–0.3	6	V
		VSENSE	–0.3	4	V
		BOOT	–0.3	17	V
V_O	Output voltage	VBIAS, COMP, PWRGD	–0.3	7	V
		PH	–0.6	10	V
		PH (transient < 10 ns)		–2	V
I_O	Source current	PH	Internally Limited		
		COMP, VBIAS		6	mA
I_S	Sink current	PH		12	A
		COMP		6	mA
		SS/ENA, PWRGD		10	mA
	Voltage differential	AGND to PGND	–0.3	0.3	V
T_J	Operating virtual junction temperature		–40	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I	3		6	V
Operating junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS54610 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
	Input voltage range, VIN		3		6	V
$I_{(Q)}$	Quiescent current	f_s = 350 kHz, SYNC ≤ 0.8 V, RT open, PH pin open	11		15.8	mA
		f_s = 550 kHz, SYNC ≥ 2.5 V, RT open, PH pin open	16		23.5	
		Shutdown, SS/ENA = 0 V		1	1.4	
UNDERVOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3.0	V
	Stop threshold voltage, UVLO		2.70	2.80		V
	Hysteresis voltage, UVLO		0.14	0.16		V
	Rising and falling edge deglitch, UVLO[1]			2.5		µs
BIAS VOLTAGE						
	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
	Output current, VBIAS [2]				100	µA
CUMULATIVE REFERENCE						
V_{ref}	Accuracy		0.882	0.891	0.900	V
REGULATION						
	Line regulation[2] [3]	I_L = 3 A, f_s = 350 kHz, T_J = 85°C			0.04	%/V
		I_L = 3 A, f_s = 550 kHz, T_J = 85°C			0.04	
	Load regulation[1] [3]	I_L = 0 A to 6 A, f_s = 350 kHz, T_J = 85°C			0.03	%/A
		I_L = 0 A to 6 A, f_s = 550 kHz, T_J = 85°C			0.03	
OSCILLATOR						
	Internally set—free running frequency	SYNC ≤ 0.8 V, RT open	280	350	420	kHz
		SYNC ≥ 2.5 V, RT open	440	550	660	
	Externally set—free running frequency range	RT = 180 kΩ (1% resistor to AGND)[1]	252	280	308	kHz
		RT = 100 kΩ (1% resistor to AGND)	460	500	540	
		RT = 68 kΩ (1% resistor to AGND)[1]	663	700	762	
	High level threshold, SYNC		2.5			V
	Low level threshold, SYNC				0.8	V
	Pulse duration, external synchronization, SYNC[1]		50			ns
	Frequency range, SYNC[1]		330		700	kHz

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10

Electrical Characteristics (continued)

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Ramp valley (1)			0.75		V
	Ramp amplitude (peak-to-peak)(1)			1		V
	Minimum controllable on time(1)				200	ns
	Maximum duty cycle		90%			
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND(1)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(1)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO(1)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP		1	1.4		V/μs
PWM COMPARATOR						
	PWM comparator propagation delay time,PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.20	1.40	V
	Enable hysteresis voltage, SS/ENA			0.03		V
	Falling edge deglitch, SS/ENA(1)			2.5		μs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	μA
	Discharge current, SS/ENA	SS/ENA = 1.2 V, V_I = 2.7 V	2	2.3	4	mA
POWER GOOD						
	Power good threshold voltage	VSENSE falling		90		%V_{ref}
	Power good hysteresis voltage(1)			3		%V_{ref}
	Power good falling edge deglitch(1)			35		μs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	V_I= 5.5 V			1	μA
CURRENT LIMIT						
	Current limit trip point	V_I = 3 V Output shorted(1)	7.2	10		A
		V_I= 6 V Output shorted(1)	10	12		
	Current limit leading edge blanking time(1)			100		ns
	Current limit total response time(1)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point(1)		135	150	165	°C
	Thermal shutdown hysteresis(1)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	V_I = 6 V(4)		26	47	mΩ
		V_I = 3 V(4)		36	65	

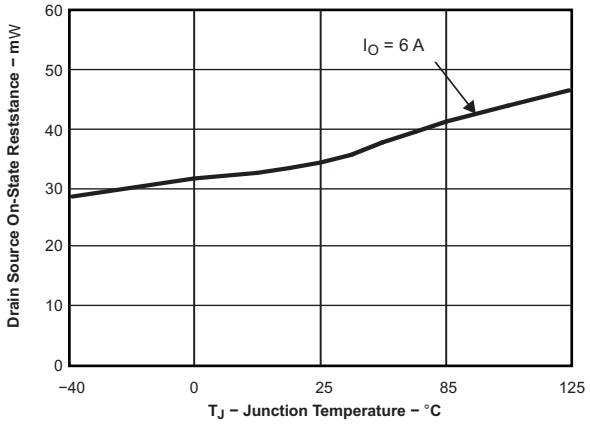
(4) Matched MOSFETs low-side $r_{DS(on)}$ production tested, high-side $r_{DS(on)}$ specified by design

7.6 Dissipation Ratings[1][2]

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
28 Pin PWP with solder	18.2 °C/W	5.49[3] W	3.02 W	2.20 W
28 Pin PWP without solder	40.5 °C/W	2.48 W	1.36 W	0.99 W

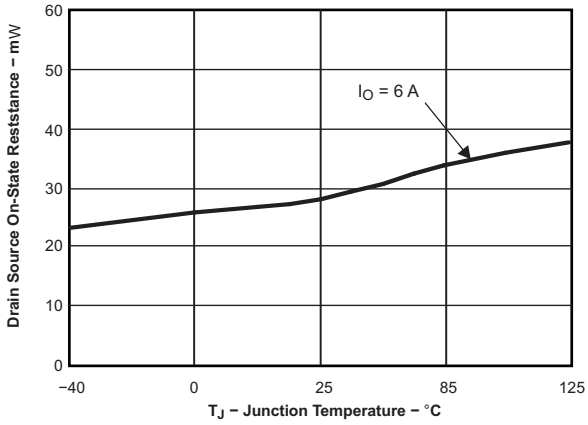
(1) Test board conditions:
  (a) 3 inch × 3 inch, 4 layers, thickness: 0.062 in
  (b) 1.5 oz. copper traces located on the top of the PCB
  (c) 1.5 oz. copper plane located on the bottom of the PCB
  (d) 0.5 oz. copper planes on the 2 inner layers
  (e) 12 thermal vias. See Figure 23
(2) Thermal metrics shown in *Thermal Information* refer to JEDEC High K board. Metrics in this table refer to the test board conditions listed below.
(3) Maximum power dissipation may be limited by overcurrent protection

7.7 Typical Characteristics



VIN = 3.3 V

Figure 1. Drain-Source On-State Resistance vs Junction Temperature



VIN = 5 V

Figure 2. Drain-Source On-State Resistance vs Junction Temperature

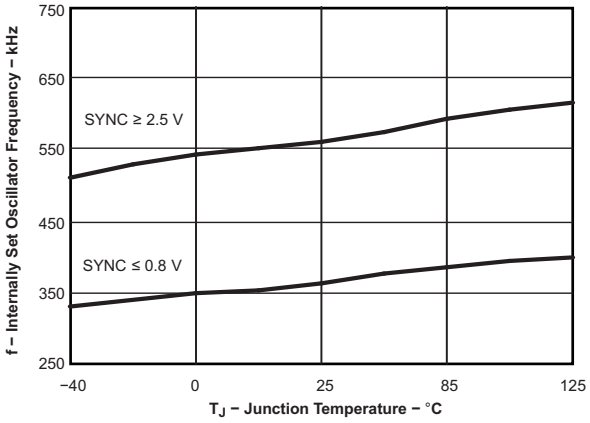


Figure 3. Internally Set Oscillator Frequency vs Junction Temperature

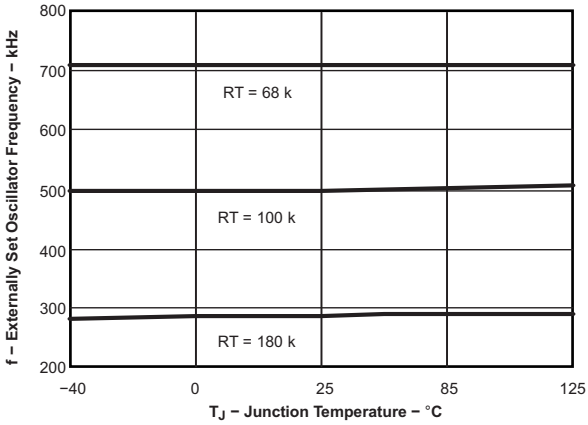


Figure 4. Externally Set Oscillator Frequency vs Junction Temperature

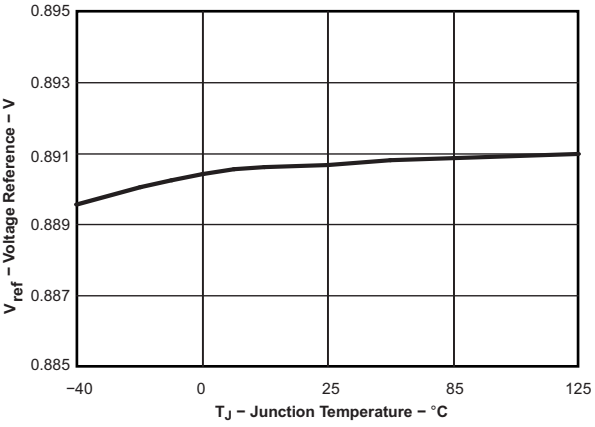
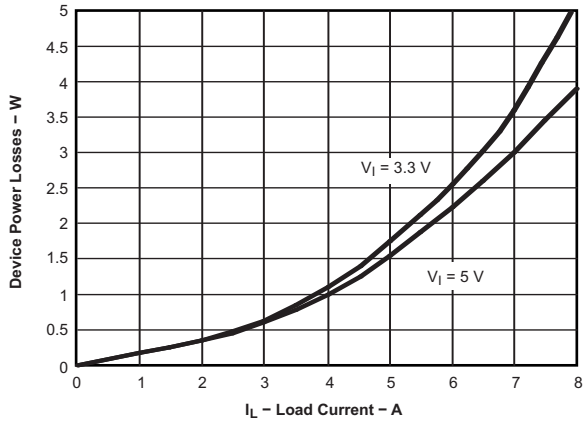


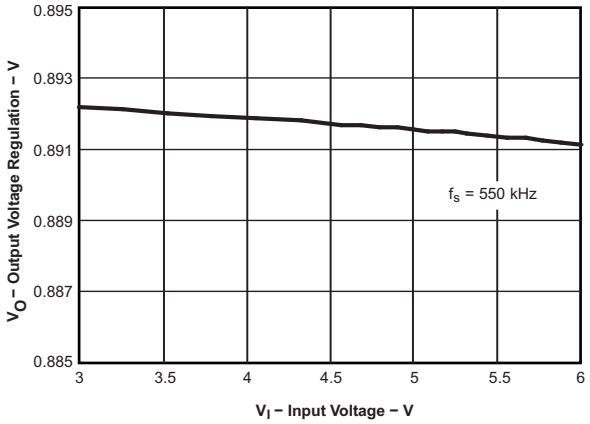
Figure 5. Voltage Reference vs Junction Temperature



T_J = 125°C f_s = 700 kHz

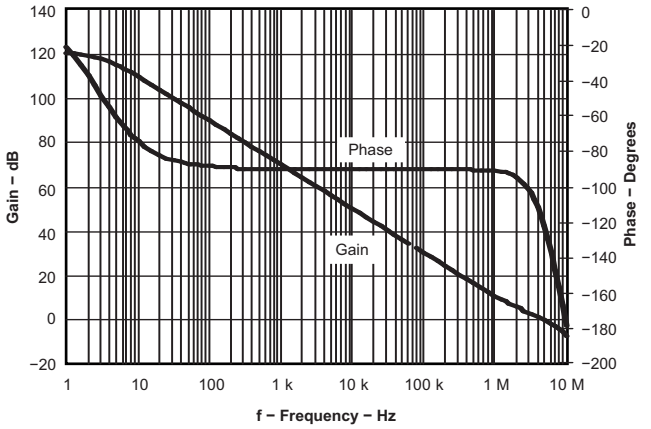
Figure 6. Device Power Losses at T_J = 125°C vs Load Current

Typical Characteristics (continued)



T_J = 85°C I_O = 3 A

Figure 7. Output Voltage Regulation vs Input Voltage



R_L= 10 kΩ C_L = 160 pF T_A = 25°C

Figure 8. Error Amplifier Open Loop Response

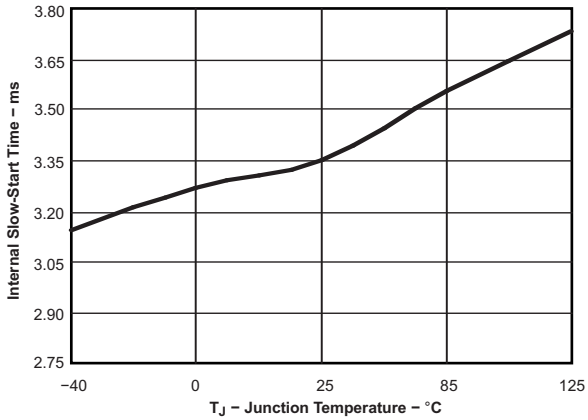


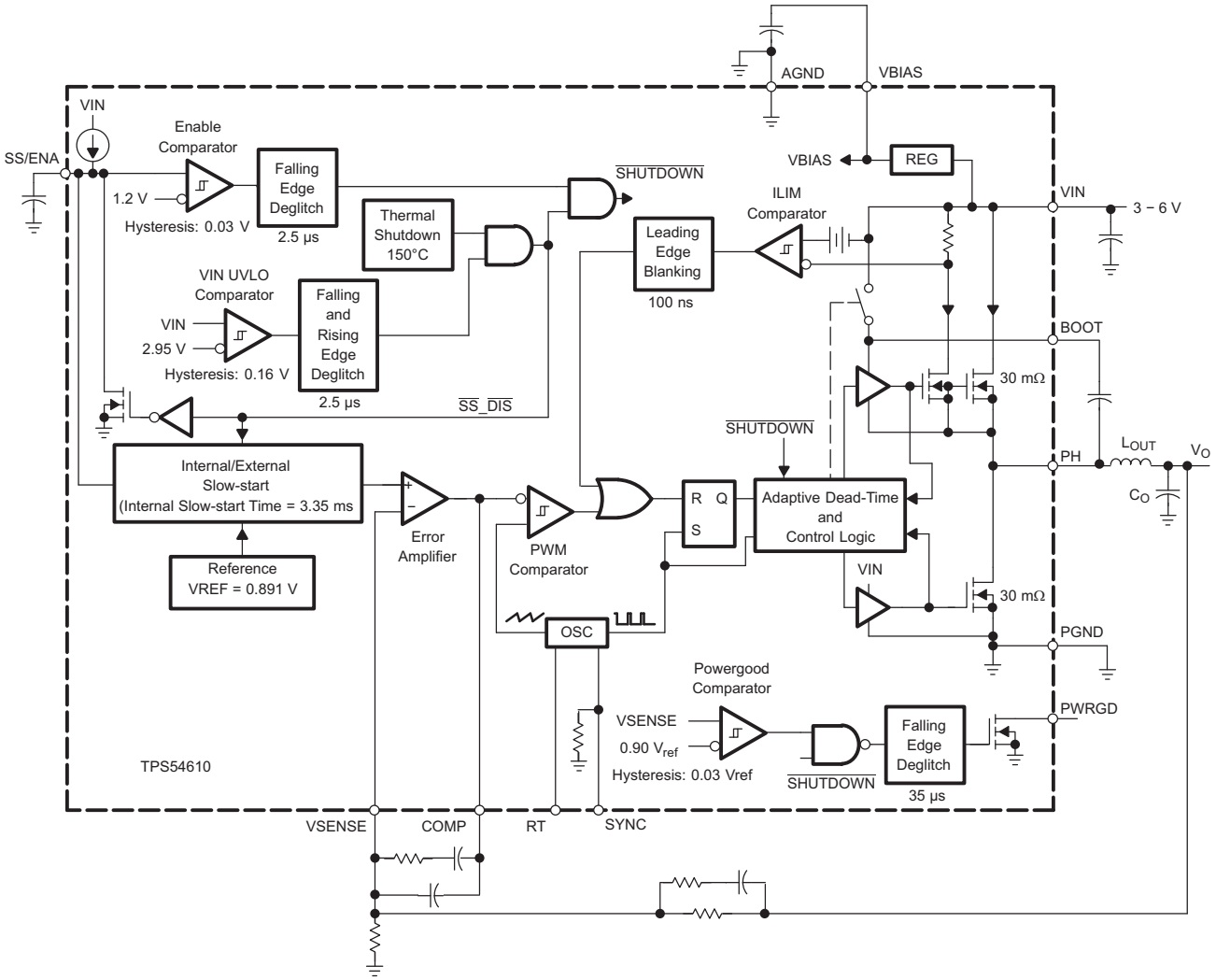
Figure 9. Internal Slow-Start Time vs Junction Temperature

8 Detailed Description

8.1 Overview

The TPS54610 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally or externally set slow-start circuit to limit inrush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The TPS54610 incorporates an UVLO to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-μs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

8.3.2 Slow Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-μs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (1)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (2)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

8.3.3 VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

8.3.4 Voltage Reference

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54610, since it cancels offset errors in the scale and error amplifier circuits.

8.3.5 Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin and AGND and floating the SYNC pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

Feature Description (continued)

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ [\text{kHz}] \quad (3)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose a resistor between the RT and AGND which sets the free running frequency to 80% of the synchronization signal. Table 1 summarizes the frequency selection configurations:

Table 1. Switching Frequency/Synchronization Configuration

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 700 kHz	Float	R = 180 kΩ to 68 kΩ
Externally synchronized frequency	Synchronization signal	R = RT value for 80% of external synchronization frequency

8.3.6 Error Amplifier

The high performance, wide bandwidth, voltage error amplifier sets the TPS54610 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

8.3.7 PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is reset, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54610 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

8.3.8 Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

8.3.9 Overcurrent Protection

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

8.3.10 Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

8.3.11 Power-Good (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low, or a thermal shutdown occurs. When VIN ≥ UVLO threshold, SS/ENA ≥ enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-μs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

8.4 Device Functional Modes

8.4.1 Continuous Conduction Mode

The TPS54610 devices operate in continuous conduction mode, that is, the low-side MOSFET runs fully complimentary to the high-side MOSFET regardless of output current.

8.4.2 Switching Frequency Selection/Synchronization

Depending on the configuration of the RT and SYNC pins, the TPS54610 can be configured to switch at 350 kHz, or 550 kHz without external components, or any frequency between 280 kHz and 700 kHz as configured by a resistor from the RT pin to ground. The TPS54610 can also be synchronized to an external clock using the SYNC pin. See Table 1 for more information.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS54610 is a 3 V to 6 V input, 6 A output synchronous buck PWM switcher. Ideal applications are: broadband, networking and optical communications infrastructure, and portable computing/notebook PCs.

9.2 Typical Applications

9.2.1 High Frequency Switching Regulator Using Ceramic Output Capacitors

Figure 10 shows the schematic diagram for a typical TPS54610 application. The TPS54610 (U1) can provide greater than 6 A of output current at a nominal output voltage of 3.3 V.

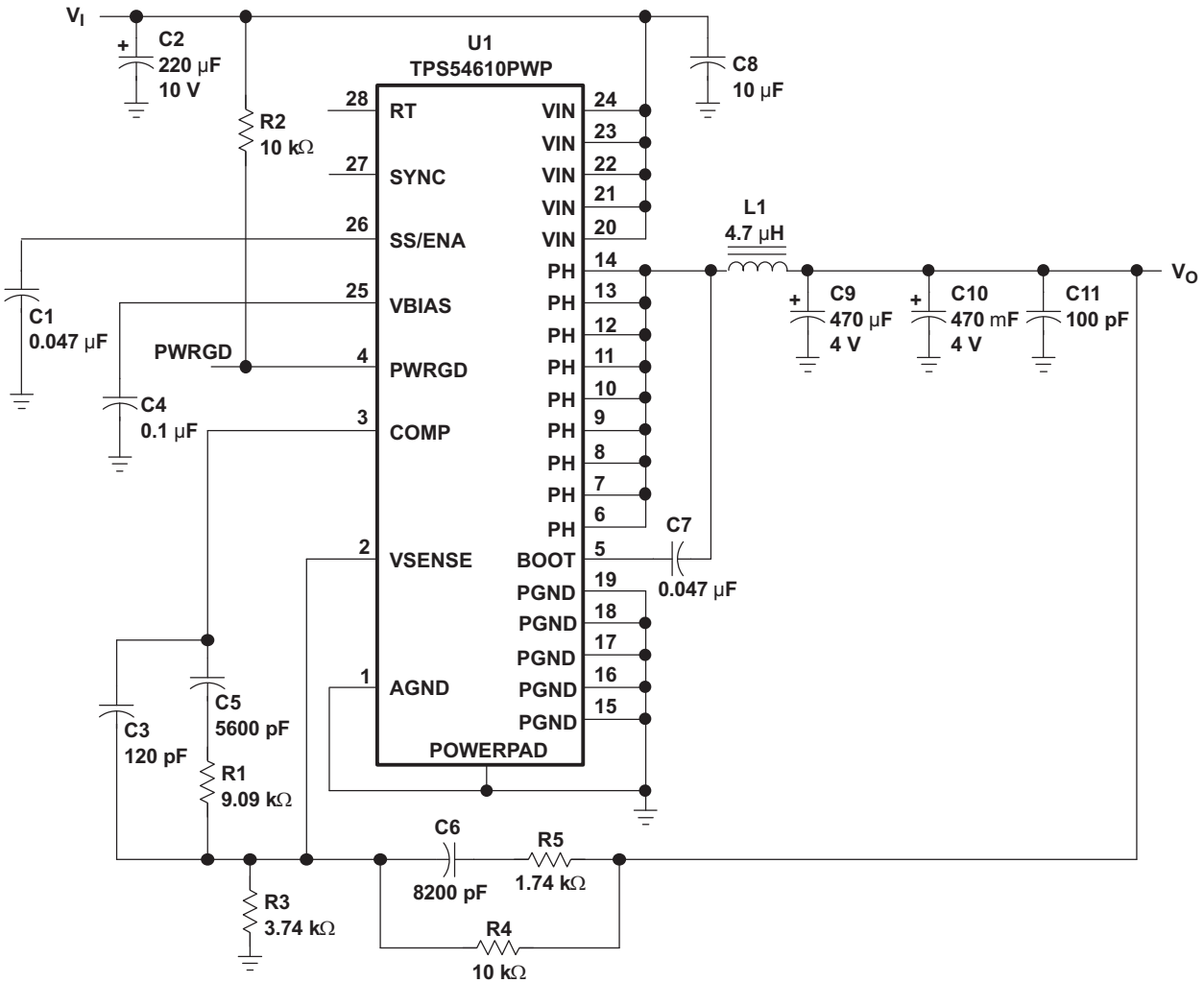


Figure 10. Application Circuit

Typical Applications (continued)

9.2.1.1 Design Requirements

This guide illustrates the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. For this example, start with the following known parameters:

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output Voltage	3.3 V
Maximum Output Current	6 A
Input Voltage	6 V

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Component Selection

The values for the components used in this design example were selected using the SWIFT designer software tool. SWIFT designer provides a complete design environment for developing dc-dc converters using the TPS54610.

9.2.1.2.2 Input Filter

The input to the circuit is a nominal 5 VDC. The input filter C2 is a 220-μF POSCAP capacitor, with a maximum allowable ripple current of 3 A. C8 provides high frequency decoupling of the TPS54610 from the input supply and must be located as close as possible to the device. Ripple current is carried in both C2 and C8, and the return path to PGND must avoid the current circulating in the output capacitors C9 and C10.

9.2.1.2.3 Feedback Circuit

The resistor divider network of R3 and R4 sets the output voltage for the circuit at 3.3 V. R4, along with R1, R5, C3, C5, and C6 form the loop compensation network for the circuit. For this design, a Type 3 topology is used.

9.2.1.2.4 Operating Frequency

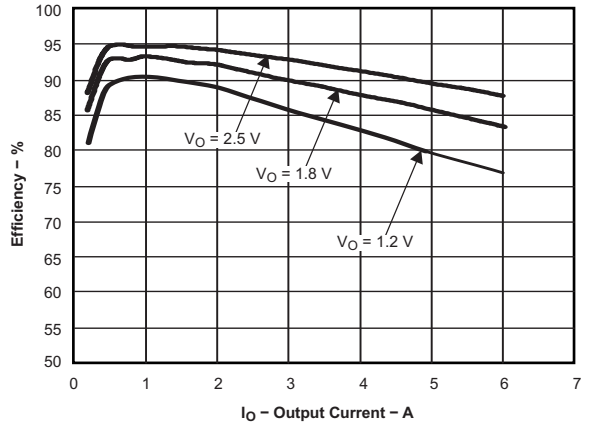
In the application circuit, the 350 kHz operation is selected by leaving RT and SYNC open. Connecting a 180 kΩ to 68 kΩ resistor between RT (pin 28) and analog ground can be used to set the switching frequency to 280 kHz to 700 kHz. To calculate the RT resistor, use the equation below:

$$R = \frac{500\,\text{kHz}}{\text{Switching Frequency}} \times 100\,[\text{k}\Omega] \quad (4)$$

9.2.1.2.5 Output Filter

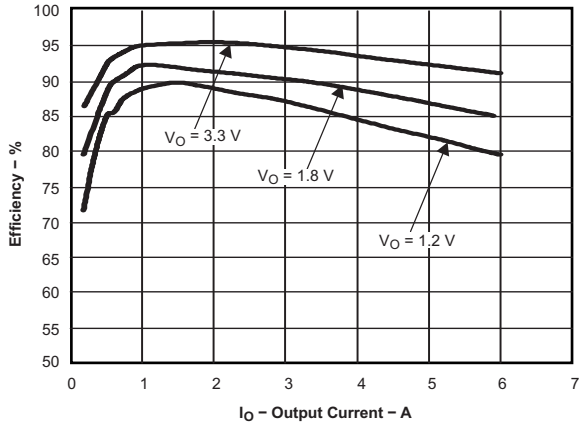
The output filter is composed of a 4.7-μH inductor and two 470-μF capacitors. The inductor is a low dc resistance (12 mΩ) type, Coiltronics UP3B-4R7. The capacitors used are 4-V POSCAP types with a maximum ESR of 0.040 Ω. The feedback loop is compensated so that the unity gain frequency is approximately 25 kHz.

9.2.1.3 Application Curves



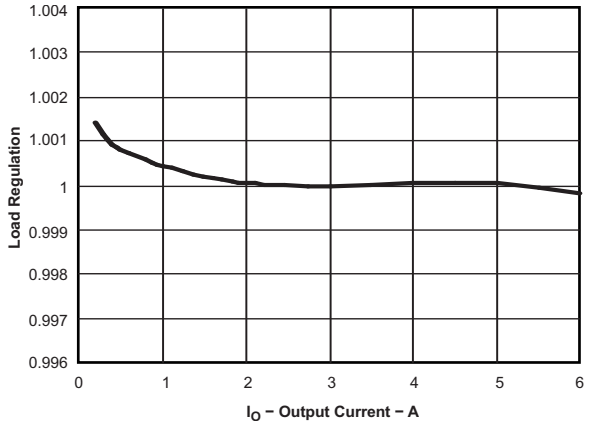
V_I = 3.3 V f = 550 kHz L = 4.7 µH
T_A = 25°C

Figure 11. Efficiency vs Output Current



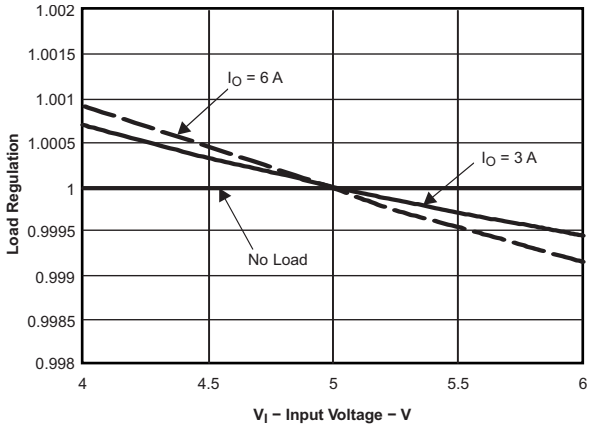
V_I = 5 V f = 550 kHz L = 4.7 µH
T_A = 25°C

Figure 12. Efficiency vs Output Current



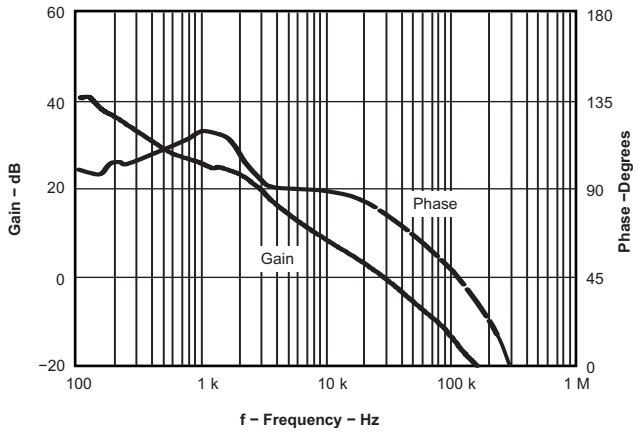
V_I = 5 V f = 550 kHz V_O = 3.3 V
T_A = 25°C

Figure 13. Load Regulation vs Output Current



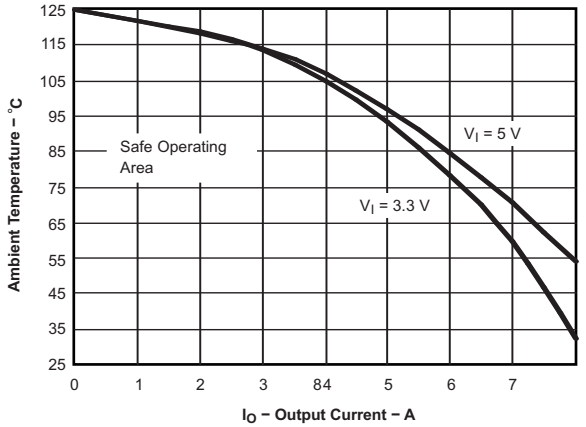
V_I = 5 V f = 550 kHz V_O = 3.3 V
T_A = 25°C

Figure 14. Line Regulation vs Input Voltage



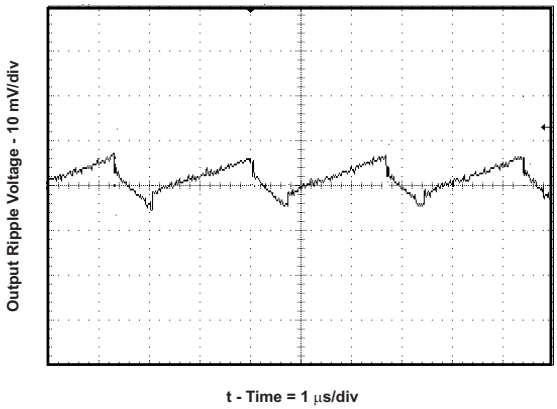
V_I = 5 V f = 550 kHz V_O = 3.3 V
T_A = 25°C I_O = 6A

Figure 15. Loop Response



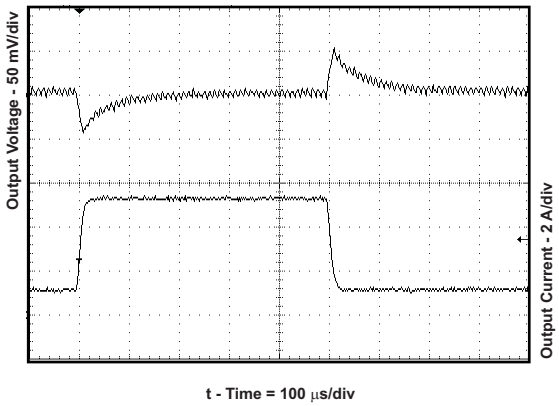
T_J = 125°C f_s = 700 kHz

Figure 16. Ambient Temperature vs Load Current



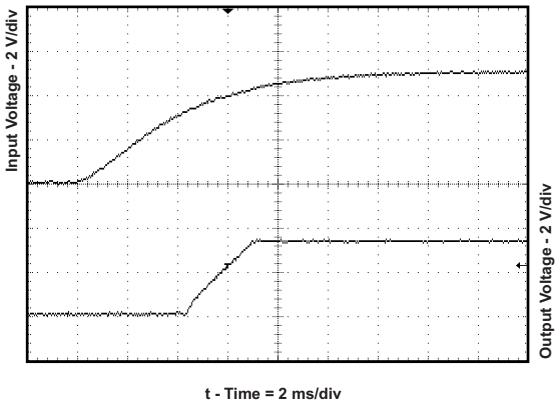
V_I = 5 V V_O = 3.3 V 6 A, 350 kHz

Figure 17. Output Ripple Voltage



V_I = 5 V 1 A to 5 A

Figure 18. Load Transient Response



V_I = 5 V No Slow-Start Cap

Figure 19. Slow-Start Timing

9.2.2 High Frequency Application

Figure 20 shows the schematic diagram for a reduced size, high frequency application using the TPS54610. The TPS54610 (U1) can provide up to 6 A of output current at a nominal outputvoltage of 1.8 V. A small size 0.56 uH inductor is used and the switching frequency is set to 680 kHz by R1. The compensation network is optimized for fast transient response as shown in Figure 20.

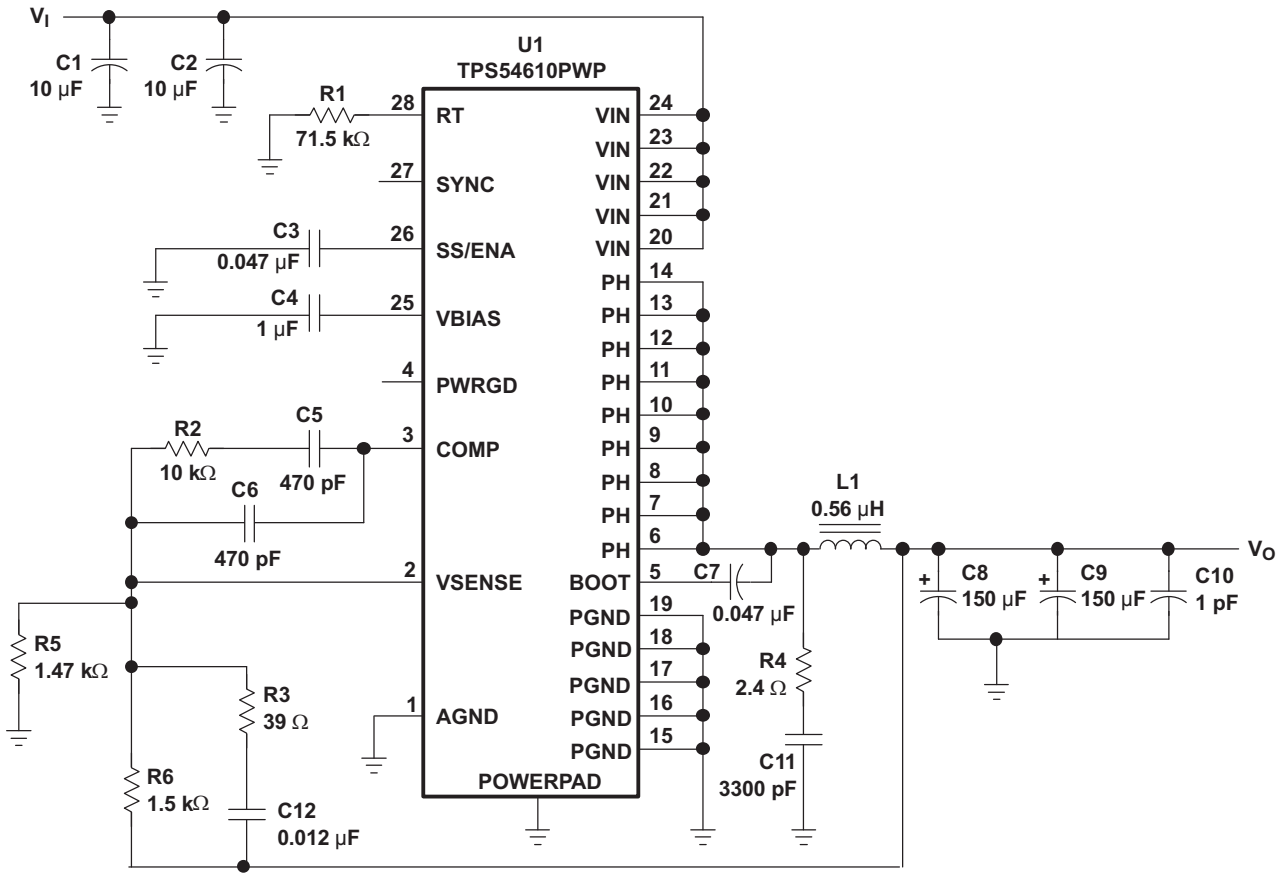


Figure 20. Small Size, High Frequency Design

9.2.2.1 Design Requirements

Refer to *Design Requirements* for the High Frequency Application Design Requirements.

9.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for the High Frequency Application Detailed Design Procedure.

9.2.2.3 Application Curve

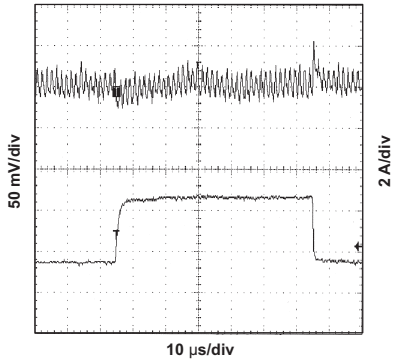


Figure 21. Transient Response, 1.5-A to 4.5-A Step

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3 V and 6 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS54610 converter additional bulk capacitance may be required.

11 Layout

11.1 Layout Guidelines

- For proper thermal performance, the exposed thermal PowerPAD underneath the integrated circuit package must be soldered to the printed-circuit board.
- For good thermal performance, the PowerPAD underneath the integrated circuit TPS54610 needs to be soldered well to the printed-circuit board.
- The VIN pins are connected together on the printed-circuit board (PCB) and bypassed with a low-ESR ceramic-bypass capacitor.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54610 ground pins.
- The minimum recommended bypass capacitance is 10-mF ceramic capacitor with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.
- The TPS54610 has two internal grounds (analog and power). Inside the TPS54610, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54610, particularly at higher output currents.
- However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. Therefore, separate analog and power ground traces are recommended.
- There is an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes.
- Additional vias are also used at the ground side of the input and output filter capacitors. The AGND and PGND pins are tied to the PCB ground by connecting them to the ground area under the device as shown.
- The only components that tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the TPS54610.
- Use a separate wide trace for the analog ground signal path. The analog ground is used for the voltage set point divider, timing resistor RT, slow-start capacitor and bias capacitor grounds. Connect this trace directly to AGND (Pin 1).
- Since the PH connection is the switching node, the inductor is located close to the PH pins. The area of theThe PH pins are tied together and routed to the output inductor. PCB conductor is minimized to prevent excessive capacitive coupling.
- Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor

Layout Guidelines (continued)

close to the IC and minimize the conductor trace lengths.

- Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, LOUT, COUT and PGND as small as practical.
- Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pin-out, they must be routed close, but maintain as much separation as possible while still keeping the layout compact.
- Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace.
- If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace.

11.2 Layout Example

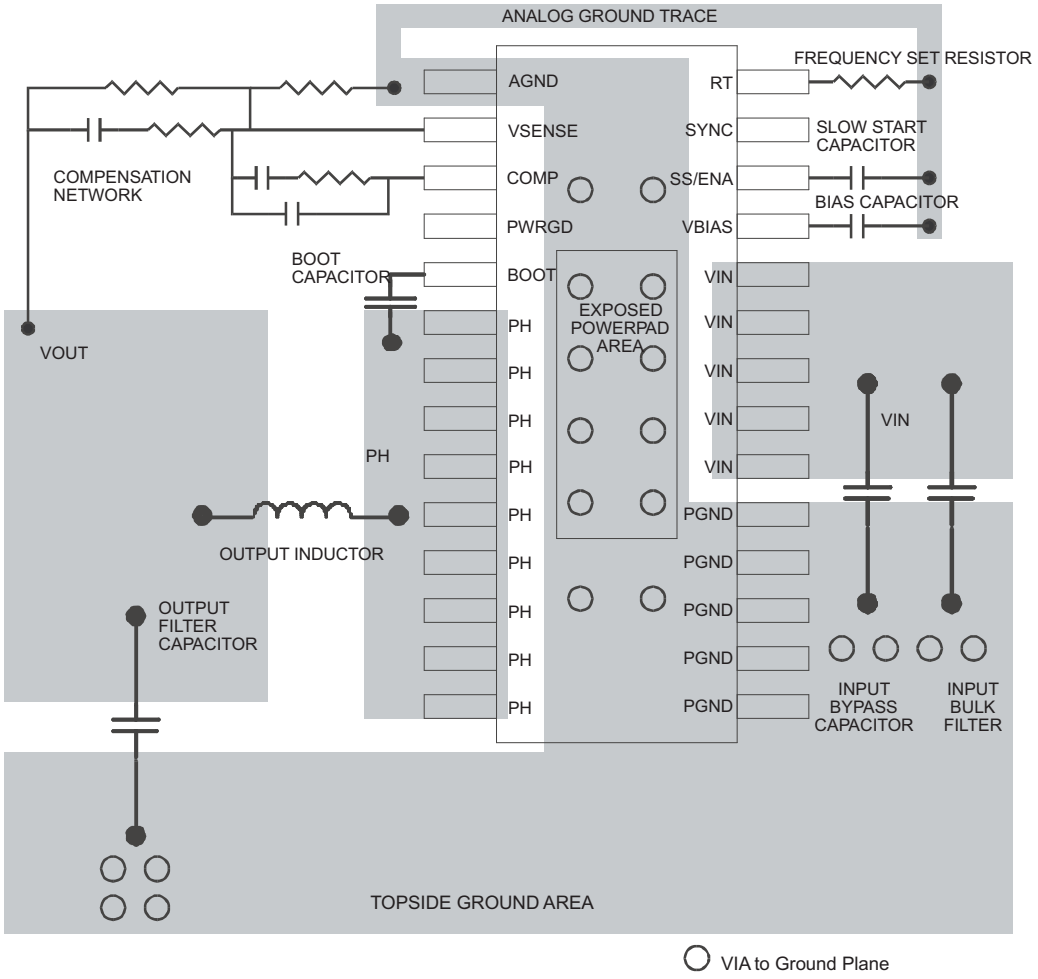


Figure 22. Recommended Land Pattern for 28-Pin PWP PowerPAD

11.3 Thermal Considerations

For operation at full rated load current, the analog ground plane must provide an adequate heat dissipating area. A 3-inch by 3-inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD™ must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD™ to the analog ground plane layer must be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.

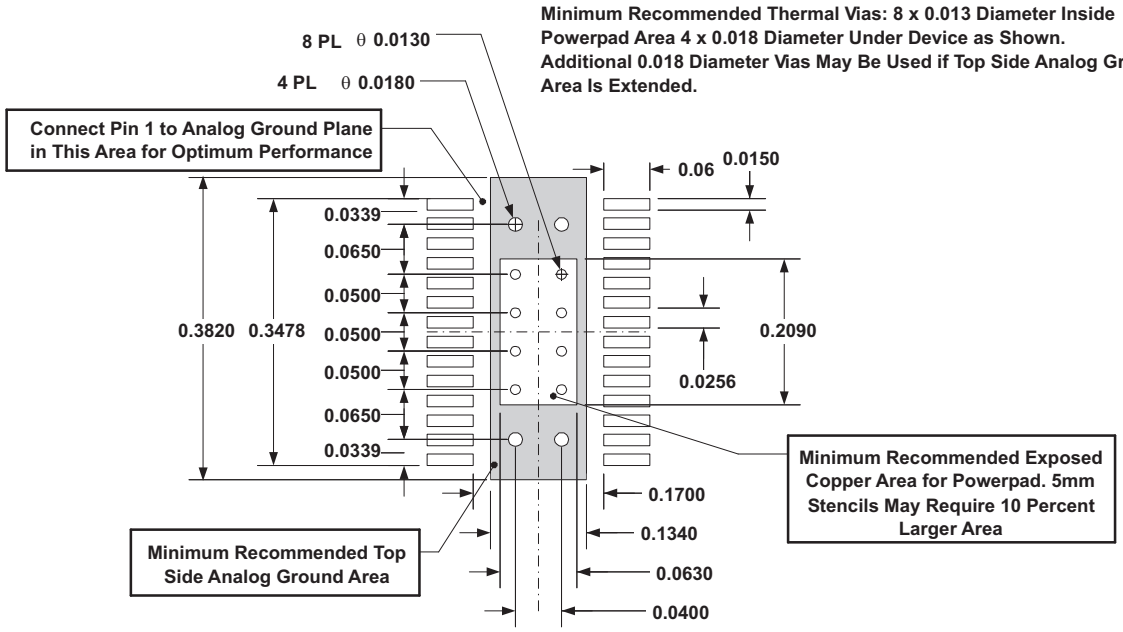


Figure 23. Recommended Land Pattern for 28-Pin PWP PowerPAD

12 器件和文档支持

12.1 器件支持

12.1.1 相关直流/直流产品

- TPS40000 - 直流/直流控制器
- TPS759xx - 7.5A 低压降稳压器
- PT6440 系列 - 6A 插件模块

应用信息可于 *"带有 Swift™ 系列同步降压稳压器的小型、高频率应用设计"*中找到。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54610PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54610	Samples
TPS54610PWPRG4	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS54610	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS54610 :

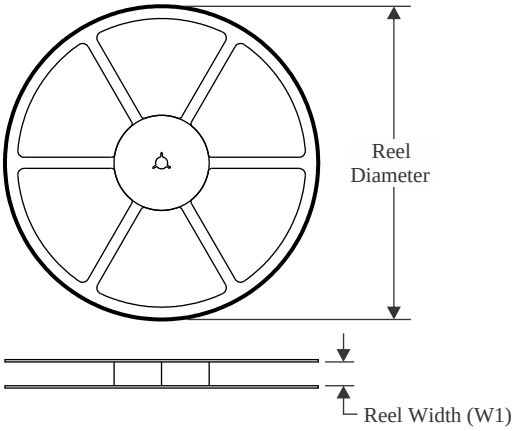
- Enhanced Product : TPS54610-EP

NOTE: Qualified Version Definitions:

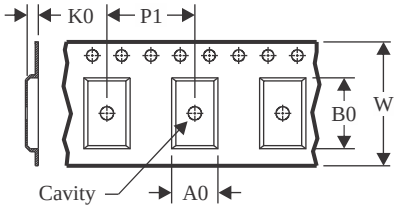
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

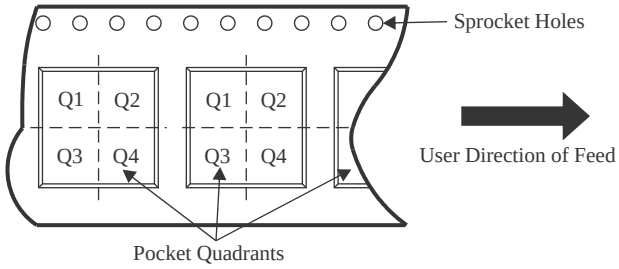


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

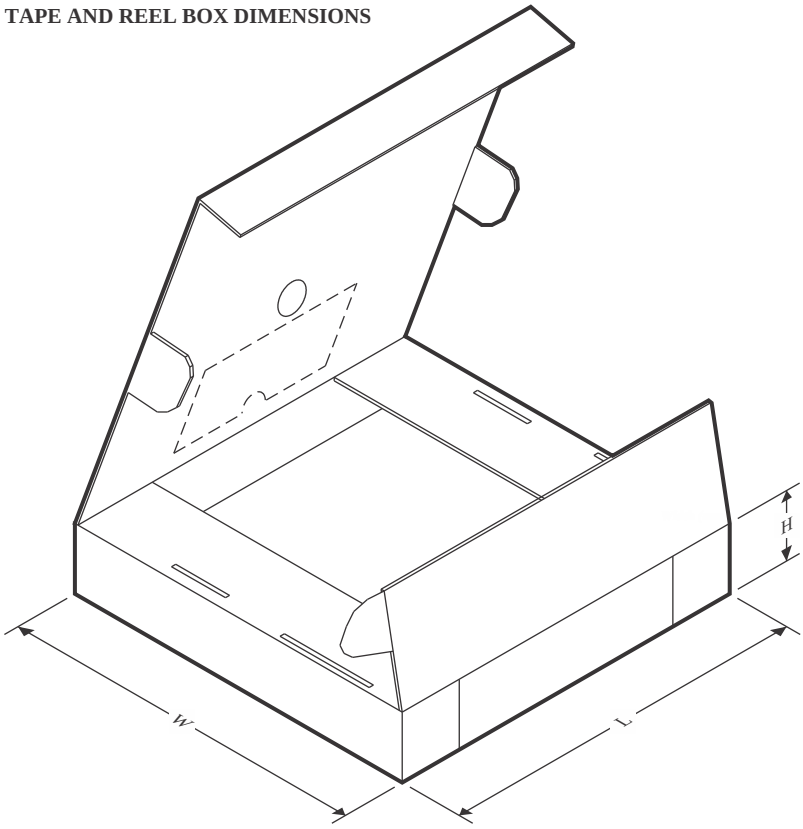
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54610PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS54610PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS54610PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54610PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS54610PWPR	HTSSOP	PWP	28	2000	356.0	356.0	35.0
TPS54610PWPR	HTSSOP	PWP	28	2000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

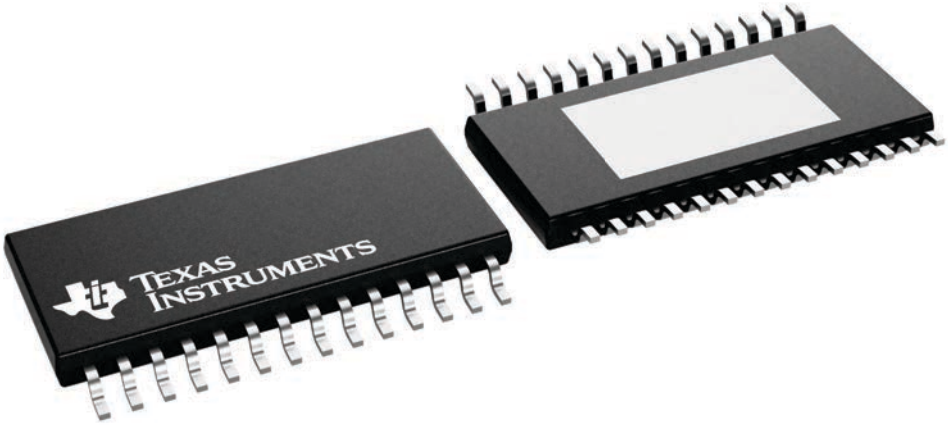
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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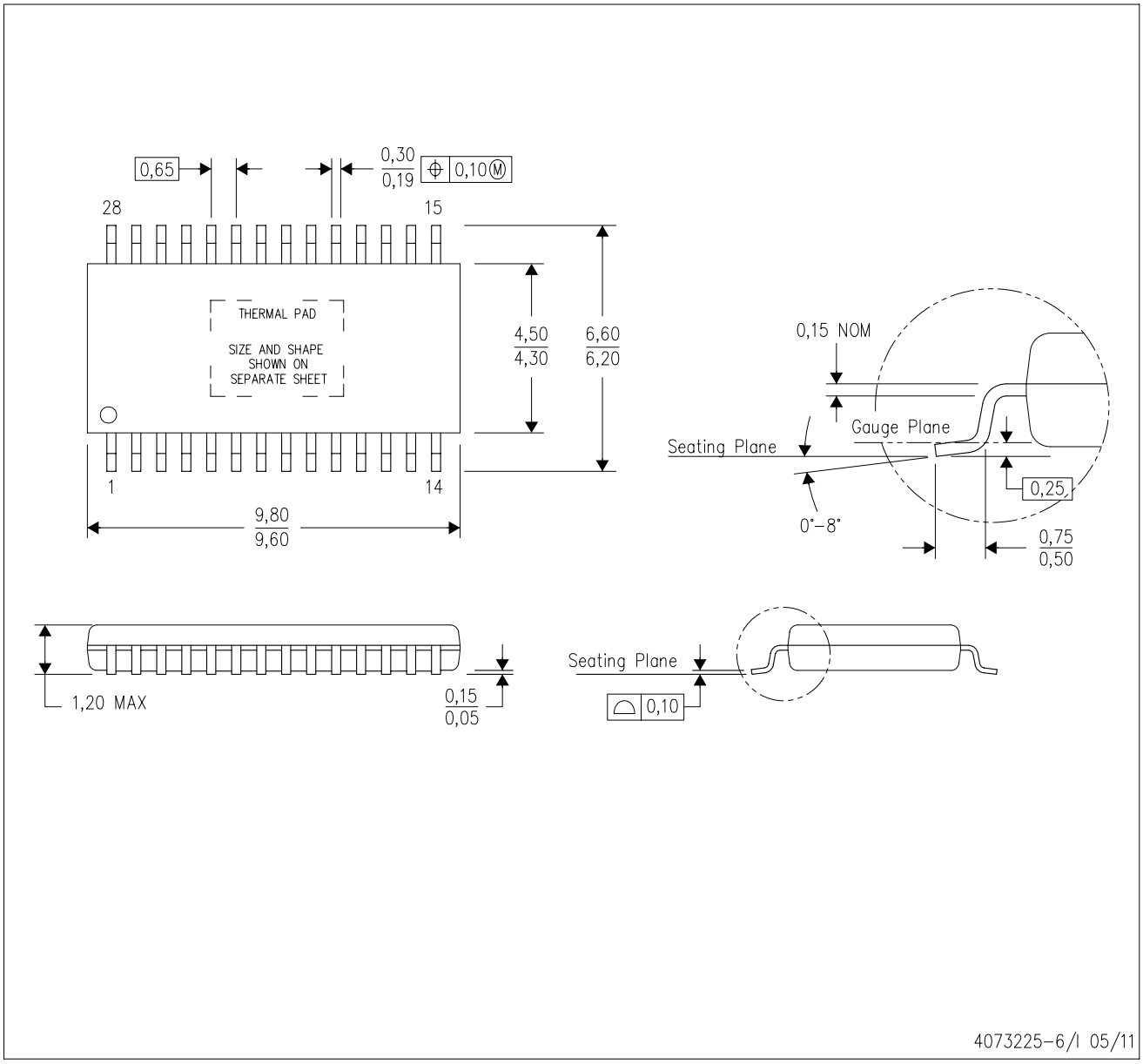
PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

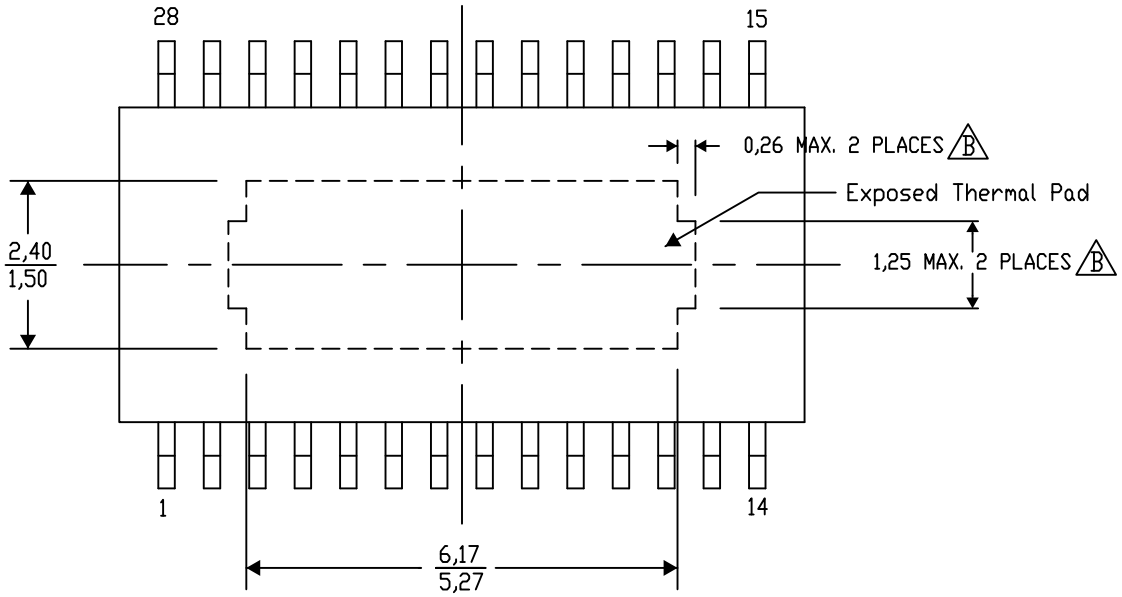
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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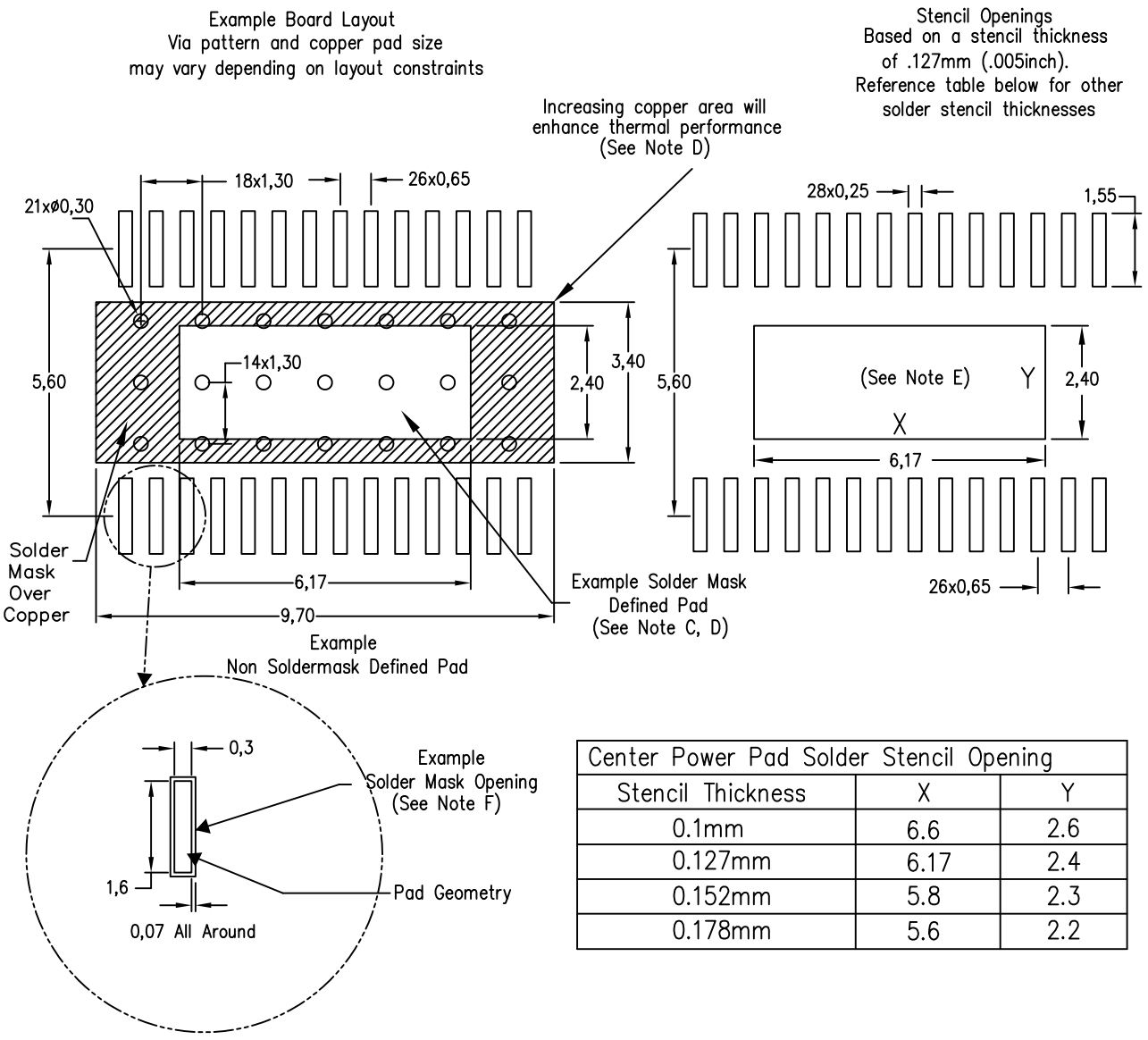
PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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