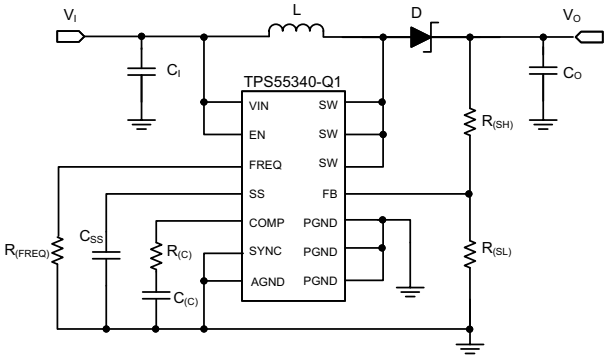
TPS55340-Q1 集成式、5A、宽输入范围升压、SEPIC 或反激式直流/直流转换器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 125°C
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 内部 5A，40V 低侧 MOSFET 开关
- 2.9 至 38V 输入电压范围
- ±0.7% 基准电压
- 0.5mA 静态工作电流
- 2.7μA 关断电源电流
- 固定频率电流模式脉宽调制 (PWM) 控制
- 频率在 100kHz 至 2.5MHz 之间可调（请参阅节 7.3.2）
- 同步外部时钟功能
- 软启动时间可调节
- 用于在轻负载时实现较高效率的脉冲跳跃模式
- 逐周期电流限制、热关断和 UVLO 保护
- 采用带有 PowerPad™ 的 WQFN-16 (3mm x 3mm) 封装
- 宽 T_J 运行范围：–40°C 至 +150°C
- 使用 TPS55340-Q1 并借助 WEBENCH Power Designer 创建定制设计方案

2 应用

- 升压、SEPIC 和反激式拓扑结构
- 支持启动/停止要求的汽车类预升压应用
- USB 电力输送
- 工业电源系统



典型升压应用

3 说明

TPS55340-Q1 器件是一款具有集成式 5A、40V 电源开关的单片非同步开关转换器。此器件可配置成多种标准开关稳压器拓扑，包括升压、SEPIC 和隔离反激式。此器件具有宽输入电压范围，可支持输入电压范围为 2.9V 至 38V 的应用。

TPS55340-Q1 器件使用电流模式 PWM（脉宽调制）控制来调节输出电压，并具有一个内部振荡器。PWM 的开关频率由一个外部电阻器设定或者通过与一个外部时钟信号同步来设置。用户可以在 100kHz 至 2.5MHz 之间对开关频率进行设定。

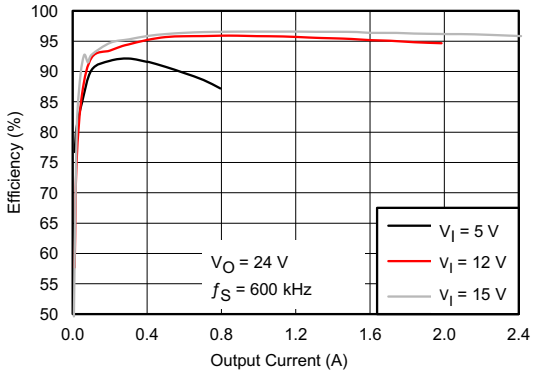
此器件具有可编程软启动功能，可限制启动期间的涌入电流，并且还具有其他内置保护特性，包括逐周期过流限制和热关断。

TPS55340-Q1 器件采用一个小型 3mm x 3mm 16 引脚 WQFN 封装，此封装带有 PowerPad 以增强散热性能。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS55340-Q1	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率与输出电流间的关系

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (January 2019) to Revision C (September 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision A (July 2016) to Revision B (January 2019)	Page
• 添加了 Webench 链接	1
• Added text note under pin configuration diagram.	3

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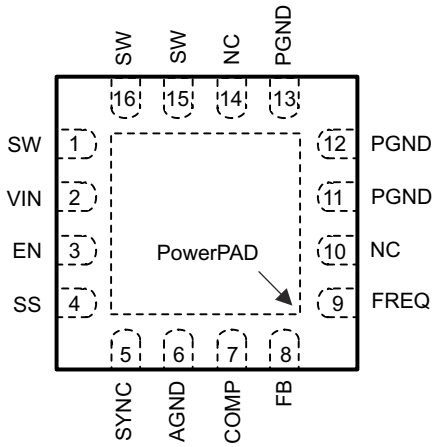
5 Pin Configuration and Functions



TI recommends connecting NC with AGND.

图 5-1. 16-Pin QFN With PowerPAD RTE Package (Top View)

表 5-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	6	Signal ground of the IC
COMP	7	Output of the transconductance error amplifier. An external RC network connected to this pin compensates the regulator feedback loop.
EN	3	Enable pin. When the voltage of this pin falls below the enable threshold for more than 1 ms, the IC turns off.
FB	8	Error amplifier input and feedback pin for positive voltage regulation. Connect the FB pin to the center tap of a resistor divider to program the output voltage.
FREQ	9	Switching frequency program pin. An external resistor connected between the FREQ pin and the AGND pin sets the switching frequency.
NC	10	This pin is reserved and must be connected to ground.
	14	
PGND	11	Power ground of the IC. The PGND pin is connected to the source of the internal power MOSFET switch.
	12	
	13	
SS	4	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start timing.
SW	1	SW is the drain of the internal power MOSFET. Connect the SW pin to the switched side of the boost or SEPIC inductor or the flyback transformer.
	15	
	16	
SYNC	5	Switching frequency synchronization pin. An external clock signal can set the switching frequency between 200 kHz and 1 MHz. If this pin is not used, it must be tied to AGND.
VIN	2	The input supply pin to the IC. Connect the VIN pin to a supply voltage between 2.9 V and 32 V. The voltage on the VIN pin can be different from the boost power stage input.
PowerPAD		The PowerPAD must be soldered to AGND. If possible, use thermal vias to connect the PowerPAD to PCB ground plane layers for improved power dissipation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN(2)	–0.3	40	V
	EN(2)	–0.3	40	V
	FB, FREQ, and COMP(2)	–0.3	3	V
	SS(2)	–0.3	5	V
	SYNC(2)	–0.3	7	V
Output voltage	SW(2)	–0.3	40	V
	SW (<10 ns transient)(2)	–5	40	V
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.9		38	V
V_O	Output voltage	V_I		38	V
$V_{(EN)}$	EN voltage	0		38	V
V_{SYN}	External switching-frequency logic input	0		5	V
T_A	Operating free-air temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS55340-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V_I = 5 V, T_J = –40°C to 150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.9		38	V
I_Q	Operating quiescent current into VIN	Device nonswitching, $V_{(FB)}$ = 2 V		0.5		mA
$I_{L(sd)}$	Shutdown current	EN = GND		2.7	10	µA
$V_{(UVLO)}$	Undervoltage lockout threshold	$V_{I(f)}$		2.5	2.7	V
V_{hys}	Undervoltage lockout hysteresis		120	140	160	mV
ENABLE AND REFERENCE CONTROL						
$V_{(EN)(r)}$	EN threshold voltage	EN rising input	0.9	1.08	1.3	V
$V_{(EN)(f)}$	EN threshold voltage	EN falling input	0.74	0.92	1.125	V
$V_{(EN)(hys)}$	EN threshold hysteresis			0.16		V
$R_{(EN)}$	EN pulldown resistor		400	950	1600	kΩ
t_{off}	Shutdown delay, SS discharge	EN high to low		1		ms
$V_{(SYNC)H}$	SYN logic high voltage		1.2			
$V_{(SYNC)L}$	SYN logic low voltage				0.4	V
VOLTAGE AND CURRENT CONTROL						
V_{ref}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
		T_A = 25°C	1.22	1.229	1.238	
$I_{IB(FB)}$	Voltage feedback input bias current	T_A = 25°C		1.6	20	nA
$I_{(COMP\_sink)}$	COMP pin sink current	$V_{(FB)} = V_{ref}$ + 200 mV, $V_{(COMP)}$ = 1 V		42		µA
$I_{S(COMP)}$	COMP pin source current	$V_{(FB)} = V_{ref}$ – 200 mV, $V_{(COMP)}$ = 1 V		42		µA
$V_{C(COMP)}$	COMP pin clamp voltage	High clamp, $V_{(FB)}$ = 1 V		3.1		V
		Low clamp, $V_{(FB)}$ = 1.5 V		0.75		
$V_{(COMP\_th)}$	COMP pin threshold	Duty cycle = 0%		1.04		V
$g_{m(ea)}$	Error amplifier transconductance		240	360	440	µmho
$R_{O(ea)}$	Error amplifier output resistance			10		MΩ
$f_{(ea)}$	Error amplifier crossover frequency			500		kHz
FREQUENCY						
f	Frequency	$R_{(FREQ)}$ = 480 kΩ	75	94	130	kHz
		$R_{(FREQ)}$ = 80 kΩ	460	577	740	
		$R_{(FREQ)}$ = 40 kΩ	920	1140	1480	
		$R_{(FREQ)}$ = 18 kΩ	2261	2549	2837	
D_{max}	Maximum duty cycle	$V_{(FB)}$ = 1 V, $R_{(FREQ)}$ = 80 kΩ	89%	96%		
$V_{(FREQ)}$	FREQ pin voltage			1.25		V
$t_{W(on)}$min	Minimum on pulse width	$R_{(FREQ)}$ = 80 kΩ		77	107	ns
POWER SWITCH						
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_I = 5 V		60	110	mΩ
		V_I = 3 V		70	120	
I_{LN_NFET}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C			2.1	µA
OCP AND SS						
I_{LIM}	N-channel MOSFET current limit	D = D_{max}	5.25	6.6	7.75	A
$I_{B(SS)}$	Soft-start bias current	$V_{(SS)}$ = 0 V		6		µA
THERMAL SHUTDOWN						
T_{sd}	Thermal shutdown threshold			165		°C

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V_I = 5 V, T_J = –40°C to 150°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{hys}	Thermal shutdown threshold hysteresis			15		°C

6.6 Typical Characteristics

V_I = 5 V, T_A = 25°C (unless otherwise noted)

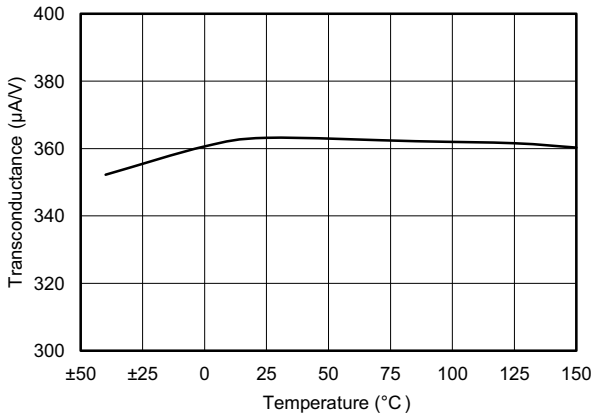

图 6-1. Error Amplifier Transconductance vs Temperature

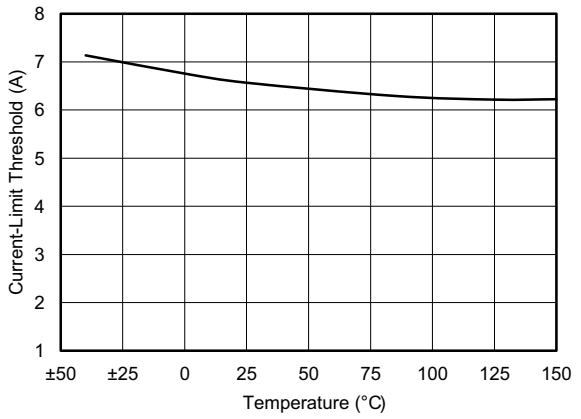

图 6-2. Switch Current Limit vs Temperature

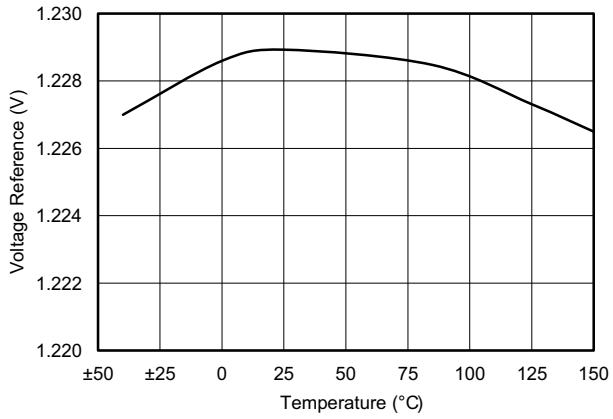

图 6-3. Feedback Voltage Reference vs Temperature

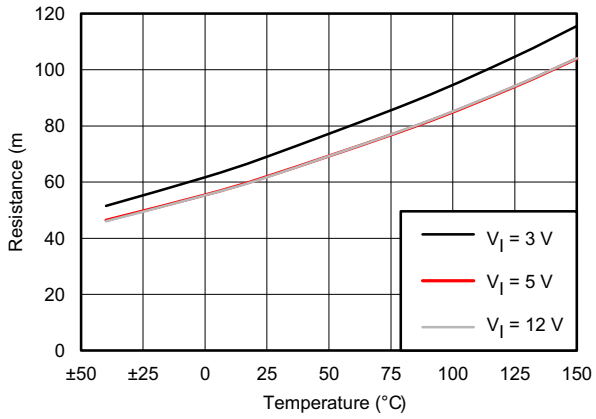

图 6-4. Static Drain Source On-State Resistance ($r_{DS(on)}$) vs Temperature

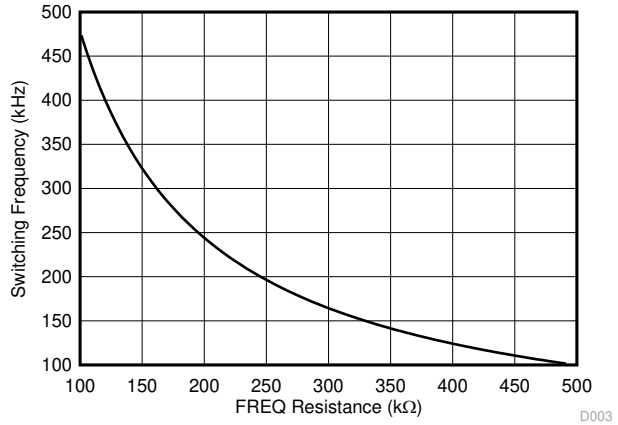

图 6-5. Frequency vs FREQ Resistance Low Frequency Range

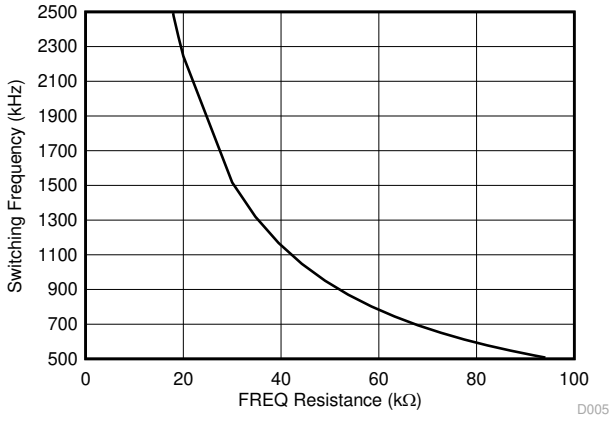

图 6-6. Frequency vs FREQ Resistance High Frequency Range

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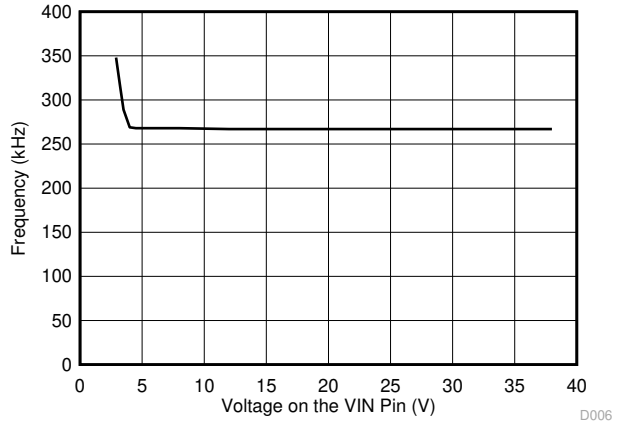
6.6 Typical Characteristics (continued)

V_I = 5 V, T_A = 25°C (unless otherwise noted)



T_A = 25°C

图 6-7. Minimum Switching Frequency for Quick Recovery from Frequency Foldback

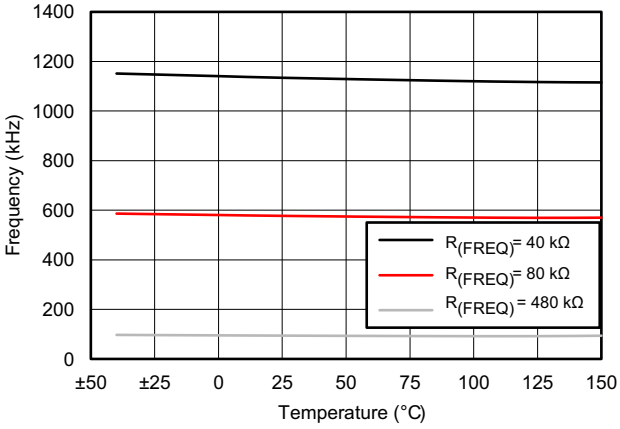
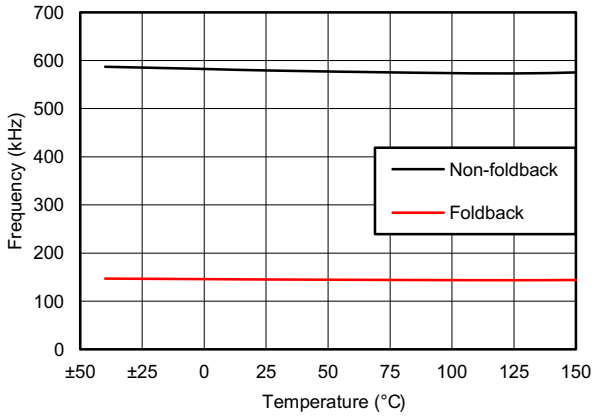


图 6-8. Frequency vs Temperature



$R_{(FREQ)}$ = 80 kΩ

图 6-9. Non-Foldback Frequency vs Foldback Frequency

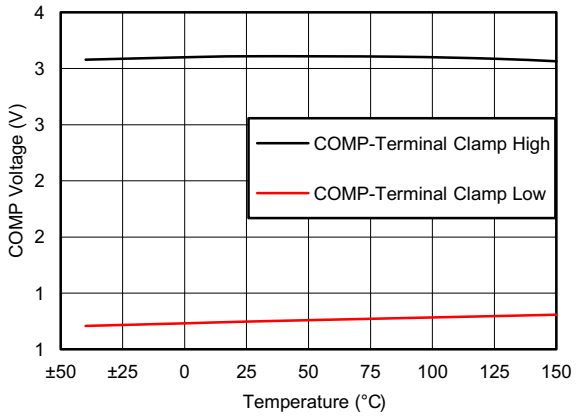


图 6-10. COMP Clamp Voltage vs Temperature

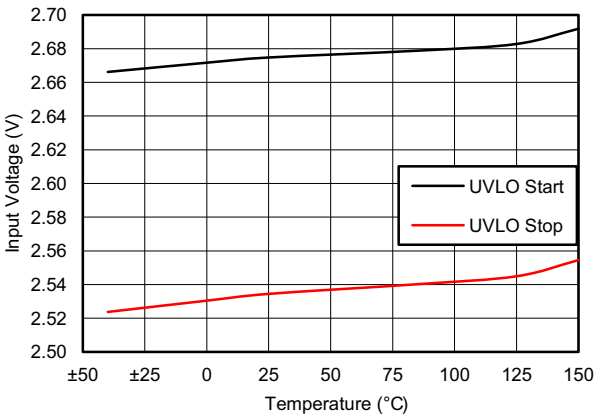


图 6-11. Input Voltage UVLO vs Temperature

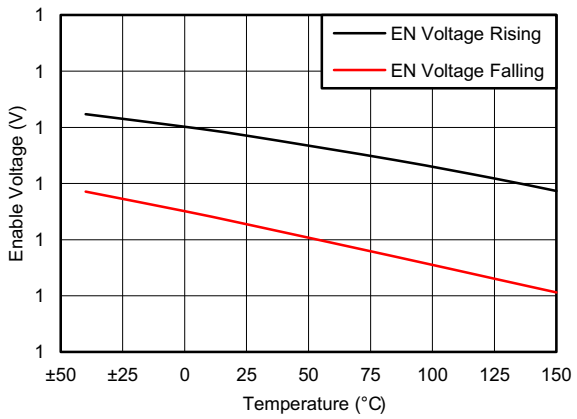


图 6-12. Enable Voltage vs Temperature

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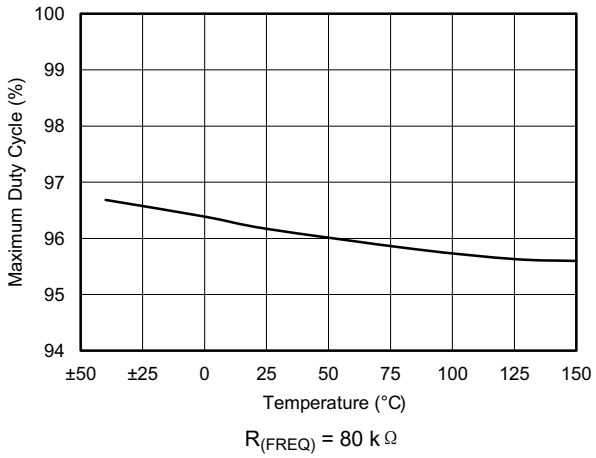
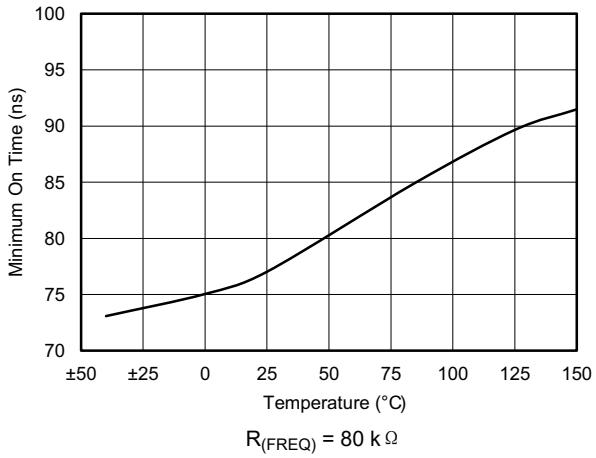
6.6 Typical Characteristics (continued)

V_I = 5 V, T_A = 25°C (unless otherwise noted)



$R_{(FREQ)}$ = 80 kΩ

图 6-13. Maximum Duty Cycle vs Temperature



$R_{(FREQ)}$ = 80 kΩ

图 6-14. Minimum On Time vs Temperature

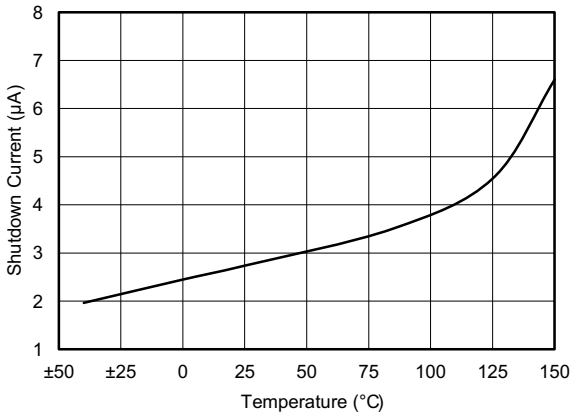


图 6-15. Shutdown Current vs Temperature

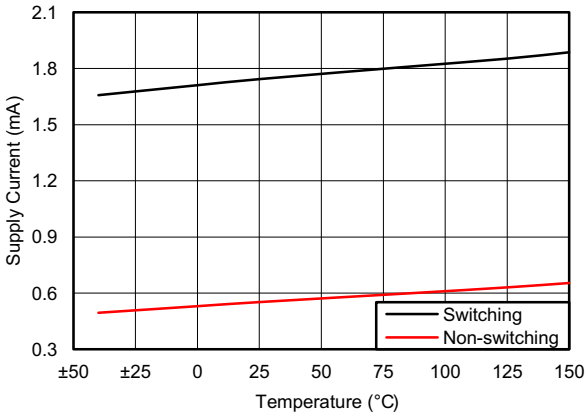


图 6-16. Supply Current vs Temperature

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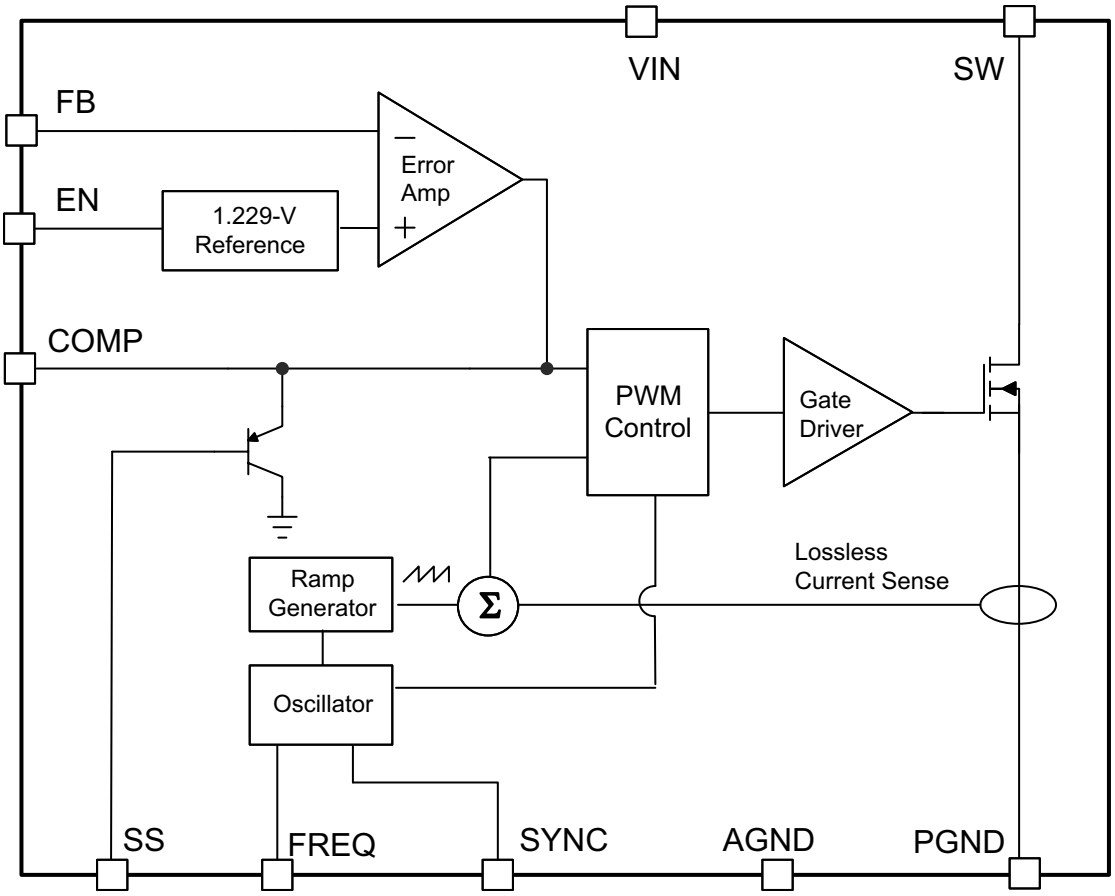
7 Detailed Description

7.1 Overview

The TPS55340-Q1 device is a monolithic non-synchronous switching converter with an integrated 5-A, 40-V power switch. The device can be configured in several standard switching regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multi-cell batteries or regulated 3.3-V, 5-V, 12-V, and 24-V power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation

If designed as a boost converter, the TPS55340-Q1 device regulates the output with current mode pulse-width-modulation (PWM) control. The PWM-control circuitry turns on the switch at the beginning of each oscillator clock cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current reaches a threshold level set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased to allow the inductor current to flow to the output. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The duty cycle of the converter is determined by the PWM-control comparator, which compares the error amplifier output and the current signal. The oscillator frequency is programmed by the external resistor or synchronized to an external clock signal.

A ramp signal from the oscillator is added to the inductor current ramp to provide slope compensation. Slope compensation is required to avoid subharmonic oscillation that is intrinsic to peak-current mode control at duty cycles higher than 50%. If the inductor value is too small, the internal slope compensation may not be adequate to maintain stability.

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The PWM control feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC-compensation network connected to the COMP pin is chosen for feedback loop stability and optimum transient response.

7.3.2 Switching Frequency

The switching frequency is set by a resistor ($R_{(FREQ)}$) connected to the FREQ pin of the TPS55340-Q1 device. The relationship between the resistance of $R_{(FREQ)}$ and frequency is shown in 图 6-5. Do not leave this pin open. A resistor must always be connected from the FREQ pin to ground for proper operation. Use 方程式 1 to calculate the resistor value required for a desired frequency.

$$R_{(FREQ)}\,(k\Omega) = 57500 \times f_S{}^{-1.03}\,(kHz) \tag{1}$$

For the given resistor value, use 方程式 2 to calculate the corresponding frequency.

$$f_S\,(kHz) = 41600 \times R_{(FREQ)}{}^{-0.97}\,(k\Omega) \tag{2}$$

The TPS55340-Q1 switching frequency can synchronized to an external clock signal that is applied to the SYNC pin. The required logic levels of the external clock are shown in 节 6.5. The recommended duty cycle of the clock is between 10% to 90%. A resistor must be connected from the FREQ pin to ground when the converter is synchronized to the external clock and the external clock frequency must be within ±20% of the corresponding frequency set by the resistor. For example, if the frequency programmed by the FREQ pin resistor is 600 kHz, the external clock signal must be in the range of 480 to 720 kHz.

With a switching frequency below 280 kHz (typical) after the TPS55340-Q1 enters frequency foldback as described in 节 7.3.3, if a load remains when the overcurrent condition is removed, the output may not recover to the set value. For the output to return to the set value, the load must be removed completely or the TPS55340-Q1 power cycled with the EN pin or VIN pin. Select a nominal switching frequency of 350 kHz for quicker recovery from frequency foldback.

When setting the switching frequency higher than 1.2 MHz, TI recommends using an external synchronous clock as the switching frequency to ensure that the pulse-skipping function works at a light load. When using the internal switching frequency above 1.2 MHz, the TPS55340-Q1 device might not pulse skip as described in 节 7.3.3.1. When the pulse-skipping function does not work at light loads, the TPS55340-Q1 device always operates in PWM mode with a minimum ON pulse width. This causes the output voltage to be higher than the set value with the resistor divider at the FB pin. This occurs in minimum duty cycle conditions such as when there is light output load or when the input voltage is close to the set output voltage in a boost topology. In the light load condition, a minimum output load will keep the output voltage at the set value in a boost topology. The required minimum load can be estimated with 方程式 3 or 方程式 4 using the maximum minimum on time of 107 ns and a parasitic $C_{(SW)}$ capacitance of 150 pF. For example, when boosting 5 V to 12 V with 2.5-MHz switching frequency and a 2-µH inductor, the worst case minimum output load is 36 mA.

$$I_O\,min = \frac{\left(V_I \times t_{W(on)}\,min + (V_O - V_I) \times \sqrt{L \times C_{SW}}\right)^2 \times fs}{2 \times L \times (V_O - V_I)} \quad \text{when } V_O - V_I < V_I \tag{3}$$

$$I_O\,min = \frac{\left(V_I \times t_{W(on)}\,min + V_I \times \sqrt{L \times C_{SW}}\right)^2 \times fs}{2 \times L \times (V_O - V_I)} \quad \text{when } V_O - V_I > V_I \tag{4}$$

7.3.3 Overcurrent Protection and Frequency Foldback

The TPS55340-Q1 device provides cycle-by-cycle overcurrent protection that turns off the power switch when the inductor current reaches the overcurrent limit threshold. The PWM circuitry resets at the beginning of the next switch cycle. During an overcurrent event, the output voltage begins to droop as a function of the load on the output. When the FB voltage through the feedback resistors, drops lower than 0.9 V, the switching frequency is automatically reduced to 1/4 of the normal value. 图 6-9 shows the non-foldback frequency with an 80-kΩ

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timing resistor and the corresponding foldback frequency. The switching frequency does not return to normal until the overcurrent condition is removed and the FB voltage increases above 0.9 V. The frequency foldback feature is disabled during soft start.

7.3.3.1 Minimum On Time and Pulse Skipping

The TPS55340-Q1 PWM control system has a minimum PWM pulse width of 77 ns (typical). This minimum on-time determines the minimum duty cycle of the PWM, for any set switching frequency. When the voltage regulation loop of the TPS55340-Q1 device requires a minimum on-time pulse width less than 77 ns, the IC enters pulse-skipping mode. In this mode, the device power switches off for several switching cycles to prevent the output voltage from rising above the desired regulated voltage. This operation typically occurs in light load conditions when the PWM operates in discontinuous conduction mode. Pulse skipping increases the output ripple as shown in 图 8-7.

7.3.4 Voltage Reference and Setting Output Voltage

An internal voltage reference provides a precise 1.229-V voltage reference at the error amplifier non-inverting input. To set the output voltage, select the FB pin resistor $R_{(SH)}$ and $R_{(SL)}$ as shown in 方程式 5.

$$V_O = 1.229\ V \times \left(\frac{R_{(SH)}}{R_{(SL)}} + 1 \right) \tag{5}$$

7.3.5 Soft Start

The TPS55340-Q1 device has a built-in soft-start circuit that significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current source (6 µA typical) charges a capacitor ($C_{(SS)}$) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the peak current and duty cycle of the PWM controller. Limiting the peak switch current during start-up with a slow ramp on the SS pin reduces in-rush current and output voltage overshoot. When the capacitor reaches 1.8 V, the soft-start cycle is complete and the soft-start voltage no longer clamps the error amplifier output. When the EN is pulled low for at least 1 ms, the IC enters Shutdown mode and the SS capacitor is discharged through a 5-kΩ resistor to prepare for the next soft-start sequence.

7.3.6 Slope Compensation

To prevent subharmonic oscillations, the TPS55340-Q1 device uses internal slope compensation. Use 方程式 6 to calculate the sensed current slope of boost converter.

$$S_{(n)} = \frac{V_I}{L} \times R_{(SENSE)} \tag{6}$$

Use 方程式 7 to calculate the slope compensation dv/dt.

$$S_{(e)} = \frac{\left(\frac{0.32\ V}{R_{(FREQ)}} \right)}{16 \times (1 - D) \times 6\ pF} + \frac{0.5\ \mu A}{6\ pF} \tag{7}$$

In a converter with current mode control, in addition to the output voltage feedback loop, the inner current loop including the inductor current sampling effect and the slope compensation on the small-signal response must be taken into account as calculated in 方程式 8.

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$$He\ (s) = \frac{1}{1 + \frac{s \times \left[\left(1 + \frac{S_{(e)}}{S_{(n)}}\right) \times (1 - D) - 0.5\right]}{f_S} + \frac{s^2}{\left(\pi \times f_S\right)^2}} \quad (8)$$

where

- $R_{(SENSE)}$ (15 mΩ) is the equivalent current-sense resistor.
- $R_{(FREQ)}$ is the timing resistor used to set frequency.
- D is the duty cycle.

Note

If $S_{(n)}$ << $S_{(e)}$, the converter operates in voltage mode control rather than operating current mode control and 方程式 8 is no longer valid.

7.3.7 Enable and Thermal Shutdown

The TPS55340-Q1 device enters shutdown when the EN voltage is less than 0.68 V (minimum) for more than 1 ms. In shutdown, the input supply current for the device is less than 10 µA (maximum). The EN pin has an internal 950-kΩ pulldown resistor to disable the device if the pin is floating.

An internal thermal shutdown turns off the device when the junction temperature exceeds 165°C (typical). The device restarts when the junction temperature drops by 15°C.

7.3.8 Undervoltage Lockout (UVLO)

An undervoltage-lockout circuit prevents misoperation of the device at input voltages below 2.5 V (typical). When the input voltage is below the UVLO threshold, the device remains off and the internal power MOSFET turns off. The UVLO threshold is set below the minimum operating voltage of 2.9 V to ensure that a transient VIN dip does not cause the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are *not* ensured.

7.3.9 Thermal Considerations

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. This restriction limits the power dissipation of the TPS55340-Q1 device. The TPS55340-Q1 device features a thermally enhanced QFN package. This package includes a PowerPad that improves the thermal capabilities of the package. The thermal resistance of the QFN package in any application greatly depends on the PCB layout and the PowerPad connection. The PowerPad must be soldered to the analog ground on the PCB. Use thermal vias underneath the PowerPad to achieve good thermal performance.

7.4 Device Functional Modes

7.4.1 Operation With V_I < 2.9 V (Minimum V_I)

The TPS55340-Q1 device operates with input voltages above 2.9 V. The typical UVLO voltage (turning off) is 2.5 V and the TPS55340-Q1 device remains off at input voltages lower than that point. For the input voltages between the UVLO threshold and 2.9 V, the device attempts to operate, but the electrical specifications are *not* ensured.

7.4.2 Operation With EN Control

The enable rising-edge threshold voltage is 1.08 V (typical) with 0.16-V hysteresis (typical). With the EN pin held below the turn-off voltage, the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When the input voltage is above the UVLO threshold and the EN pin voltage increases above the rising edge threshold, the device becomes active. Switching enables and the soft-start sequence initiates. The TPS55340-Q1 device starts at the soft-start time determined by the external soft-start capacitor.

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7.4.3 Operation at Light Loads

The device is designed to operate in high-efficiency pulse-skipping mode under light load conditions. Discontinuous conduction mode (DCM) operation initiates when the switch current falls to 0 A. During DCM operation, the catch diode stops conducting when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of Discontinuous conduction mode (DCM) operation as shown in 图 8-6. As the load decreases further and when the voltage-regulation loop of TPS55340-Q1 device requires an on-time pulse width less than the minimum PWM pulse width of 77 ns (typical), the IC enters Pulse-skipping mode. In this mode, the device holds the power switch off for several switching cycles to prevent the output voltage from rising too much above the desired regulated voltage.

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8 Application and Implementation

Note

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8.1 Application Information

The TPS55340-Q1 device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. For example, the device configured in boost topology is widely used to convert a lower DC voltage to a higher DC voltage with a maximum available switching current of 5.25 A. Use the following design procedure to select component values for a boost converter design or SEPIC design for the TPS55340-Q1 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Applications

The following section provides a step-by-step design approach for configuring the TPS55340-Q1 device as a voltage regulating boost converter, as shown in 图 8-1. When configured as SEPIC or flyback converter, a different design approach is required. A design example of a SEPIC converter is provided in 节 8.2.2.

8.2.1 TPS55340-Q1 Boost Converter

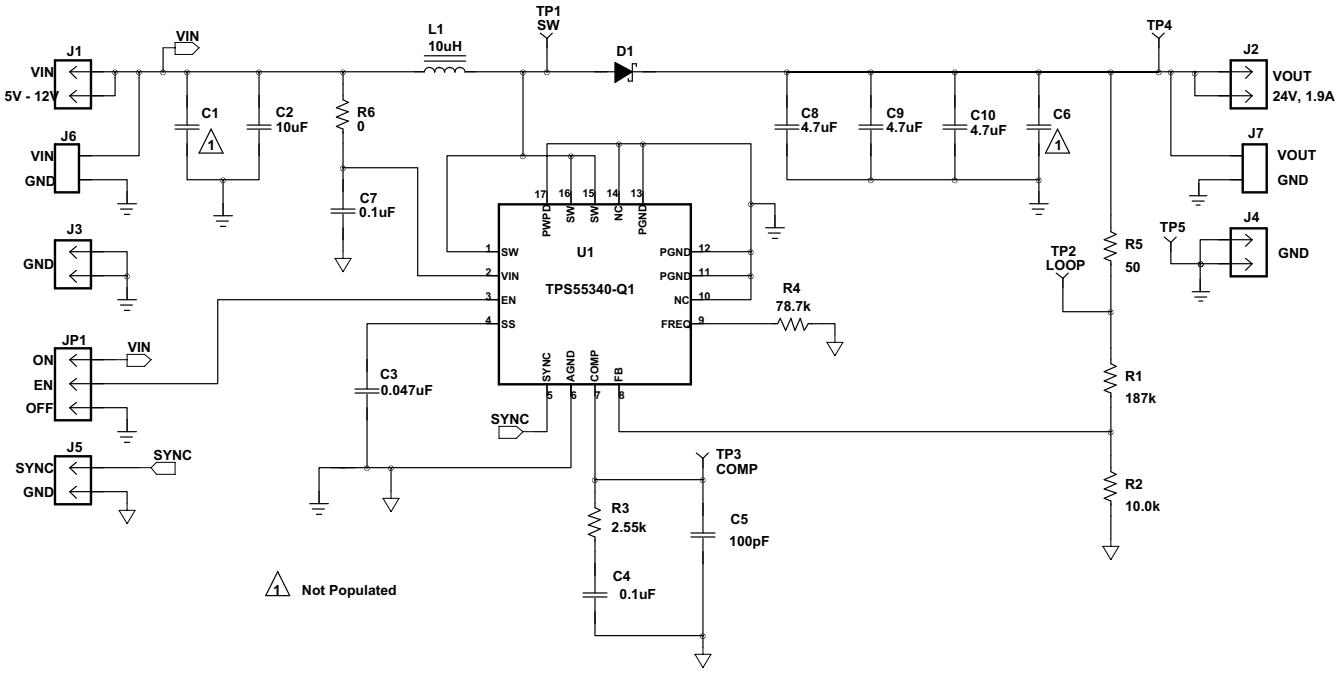

图 8-1. Boost Converter Application Schematic

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8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1. These parameters are typically determined at the system level.

表 8-1. Key Parameters of Boost Converter Example

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	24 V
Input voltage	5 V to 12 V
Maximum output current	800 mA
Transient response 50% load step (ΔV_O = 3%)	960 mV
Output voltage ripple (0.5% of V_O)	120 mV

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS55340-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Selecting the Switching Frequency (R4)

The first step of this design procedure is to determine the switching frequency of the regulator. Consider the trade-offs of a higher switching frequency versus a lower switching frequency. A higher switching frequency allows for the use of a lower-valued inductor and smaller output capacitors, which leads to the smallest solution size. A lower switching frequency results in a larger solution size, but better efficiency. In general, the selected switching frequency allows for the minimum tolerable efficiency to avoid excessively large external components.

A switching frequency of 600 kHz is a good trade-off between efficiency and solution size. The appropriate resistor value is selected based on the resistance versus frequency graph (see 图 6-5) or calculated using 方程式 1. The value of R4 is calculated to be 78.4 kΩ and the nearest standard value resistor of 78.7 kΩ is selected. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

8.2.1.2.3 Determining the Duty Cycle

The input-to-output voltage-conversion ratio of the TPS55340-Q1 device is limited by the worst-case maximum duty cycle of 89% and the minimum duty cycle, which is determined by the minimum on time of 77 ns and the switching frequency. Use 方程式 9 to calculate the minimum duty cycle. Selecting a 600-kHz switching frequency, the minimum duty cycle is calculated as 4%.

$$D_{(PS)} = t_{on}\text{min} \times f_S \quad (9)$$

The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in Discontinuous conduction mode (DCM) where the inductor current ramps to zero at the end of each cycle, the duty cycle varies with changes of the load much more than when running in

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Continuous conduction mode (CCM). In Continuous conduction mode where the inductor maintains a minimum DC current, the duty cycle is related primarily to the input and output voltages as calculated with 方程式 10. Assume a 0.5-V drop ($V_{(D)}$) across the Schottky rectifier. At the minimum input of 5 V, the duty cycle is 80%. At the maximum input of 12 V, the duty cycle is 51%.

$$D = \frac{V_O + V_{(D)} - V_I}{V_O + V_{(D)}} \tag{10}$$

At light loads, the converter operates in DCM. In this case, the duty cycle is a function of the following, as calculated in 方程式 11:

- Load
- Input voltage
- Output voltages
- Inductance
- Switching frequency

The light-load duty cycle can be calculated only after an inductance is selected (see 节 8.2.1.2.4). While operating in DCM with very-light load conditions, the duty cycle demand forces the TPS55340-Q1 device to operate with the minimum on time. The converter then begins pulse skipping, which can increase the output ripple.

$$D = \frac{\sqrt{2 \times (V_O + V_{(D)} - V_I) \times L \times I_O \times f_S}}{V_I} \tag{11}$$

All converters using a diode as the freewheeling or catch component have a load-current level at which the converters transition from DCM to CCM. The transit from DCM to CCM is the point when the inductor current falls to zero during the off time of the power switch. At higher load currents, the inductor current does not fall to zero and the diode and switch current assume a trapezoidal wave-shape as opposed to a triangular wave-shape. The load current boundary between discontinuous conduction and continuous conduction is calculated for a set of converter parameters as shown in 方程式 12.

$$I_{O(cr)} = \frac{\left(V_O + V_{(D)} - V_I\right) \times V_I^2}{2 \times \left(V_O + V_{(D)}\right)^2 \times f_S \times L} \tag{12}$$

where

- V_O is the output voltage of the converter in volts (V).
- $V_{(D)}$ is the forward conduction voltage drop across the rectifier or catch diode in volts (V).
- V_I is the input voltage to the converter in volts (V).
- I_O is the output current of the converter in amperes (A).
- L is the inductor value in henries (H).
- f_S is the switching frequency in hertz (Hz).

For loads higher than the result of the 方程式 12, the duty cycle is given by 方程式 10. For loads less than the results of 方程式 12, the duty cycle is given 方程式 11.

Unless otherwise stated, the design equations that follow assume that the converter is running in Continuous conduction mode, which typically results in a higher efficiency for the power levels of this converter.

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8.2.1.2.4 Selecting the Inductor (L1)

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. Because of these factors, the inductor is the most important component in the power regulator design. There are three important inductor specifications: inductor value, DC resistance, and saturation current. Considering inductor value alone is not enough. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, the effective inductance can fall to a fraction of the zero current value.

The minimum value of the inductor must meet the inductor current ripple (ΔI_L) requirement at worst case. In a boost converter, the maximum inductor-current ripple occurs at 50% duty cycle. For applications where duty cycle is always smaller or larger than 50%, use 方程式 14 to calculate the minimum inductance with the duty cycle as close to 50% as possible and the corresponding input voltage. For applications that must operate with 50% duty cycle when input voltage is somewhere between the minimum and the maximum input voltage, use 方程式 15. $K_{(IND)}$ is a coefficient that represents the amount of inductor ripple current relative to the maximum input current ($I_{(M\_DC)}$ = $I_L$avg). Use 方程式 13 to calculate the maximum input current with an estimated efficiency based on similar applications ($\eta_{(EST)}$). The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value ($K_{(IND)}$) is at the discretion of the designer. However, the following guidelines can be used to select the value for $K_{(IND)}$.

For CCM operation, TI recommends to use $K_{(IND)}$ values in the range of 0.2 to 0.4. Selecting a value for $K_{(IND)}$ that is closer to 0.2 results in a larger inductance value, maximizes the potential output current of the converter, and minimizes electromagnetic interference (EMI). Selecting a value for $K_{(IND)}$ that is closer to 0.4 results in a smaller inductance value, a physically smaller inductor, and improved transient response. However, a $K_{(IND)}$ value close to 0.4 can result in potentially worse EMI and lower efficiency. Using an inductor with a smaller inductance value can result in the converter operating in DCM. Operating in DCM reduces the maximum output current of the boost converter, causes larger input voltage and output voltage ripple, and reduces efficiency. For this design, a value of 0.3 for $K_{(IND)}$ was selected along with a conservative efficiency estimate of 85% with the minimum input voltage and maximum output current. Use 方程式 14 to calculate the minimum output inductance with the maximum input voltage because this equation corresponds to duty cycle closest to 50%. The maximum input current is estimated at 4.52 A and the minimum inductance is 7.53 µH. A standard value of 10 µH is selected.

$$I_{(M\_DC)} = \frac{V_O \times I_O}{\eta_{(EST)} \times V_I \min} \tag{13}$$

$$L_O \min \geq \frac{V_I}{I_{(M\_DC)} \times K_{(IND)}} \times \frac{D}{f_S},\ D \neq 50\%,\ V_I \text{ with D closest to } 50\% \tag{14}$$

$$L_O \min \geq \frac{\left(V_O + V_{(D)}\right)}{I_{(M\_DC)} \times K_{(IND)}} \times \frac{1}{4 \times f_S},\ D = 50\% \tag{15}$$

After selecting the inductance, the required current ratings can be calculated. Use 方程式 16 to calculate the ripple using the selected inductance. At a minimum input voltage, the inductor has the largest current ripple, therefore, the minimum V_I is used in 方程式 16. Use 方程式 17 and 方程式 18 to calculate the root mean square (RMS) and peak inductor current. For this design, the current ripple is 663 mA, the RMS inductor current is 4.52 A, and the peak inductor current is 4.85 A. TI recommends that the peak inductor current rating of the selected inductor be 20% higher to account for transients during power up, faults, or transient load conditions. The most conservative approach is to specify an inductor with a saturation current greater than the maximum peak current limit of the TPS55340-Q1 device. This approach helps to avoid saturation of the inductor. The selected inductor

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for this design was a Würth Elektronik 74437368100. This inductor has a saturation current rating of 12.5 A, RMS current rating of 5.2 A, and typical DCR of 27 mΩ.

$$\Delta I_L = \frac{V_I \text{min}}{L_O} \times \frac{D\text{max}}{f_S} \tag{16}$$

$$I_{L(RMS)} = \sqrt{\left(I_{I(DC)}\right)^2 + \left(\frac{\Delta I_L}{12}\right)^2} \tag{17}$$

$$I_{L(peak)} = I_{I(DC)} + \frac{\Delta I_L}{2} \tag{18}$$

The TPS55340-Q1 device has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too small, the slope compensation may not be adequate, and the loop can be unstable.

8.2.1.2.5 Computing the Maximum Output Current

The overcurrent limit for the integrated power MOSFET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power because of power conversion losses. Therefore, the following can all change the maximum current output ($I_O$max):

- Current-limit setting
- Input voltage
- Output voltage
- Efficiency

The current limit clamps the peak inductor current, therefore, the ripple must be subtracted to derive maximum DC current. Decreasing the $K_{(IND)}$ value or designing for a higher efficiency increases the maximum output current. Use the selected inductance or the selected $K_{(IND)}$ value to calculate the maximum output current. Use 方程式 19, the minimum input voltage, and minimum peak current limit ($I_{(LIM)}$) of 5.25 A to calculate the maximum output current.

$$I_O\text{max} = \frac{V_I \text{min} \times \left(I_{(LIM)} - \frac{\Delta I_L}{2}\right) \times \eta_{(EST)}}{V_O} = \frac{V_I \text{min} \times I_{(LIM)} \times \left(1 - \frac{K_{(IND)}}{2}\right) \times \eta_{(EST)}}{V_O} \tag{19}$$

For this design, with a 5-V input boosted to 24-V output, a 10-µH inductor with an assumed Schottky forward voltage of 0.5 V, and estimated efficiency of 85%, the maximum output current is calculated to be 871 mA. With a 12-V input and an increased estimated efficiency of 90%, the maximum output current calculated value increases to 2.13 A. This circuit was evaluated to the maximum output currents with both the minimum and maximum input voltage.

8.2.1.2.6 Selecting the Output Capacitor (C8 through C10)

At least 4.7 µF of ceramic type X5R or X7R capacitance is recommended at the output. This output capacitance was selected to meet the requirements for the output ripple (V_{rip}) and voltage change during a load transient. The loop is then compensated for the selected output capacitor. The output capacitance must be selected based on the most stringent of these criteria. The output ripple voltage is related to the capacitance and equivalent series resistance (ESR) of the output capacitor. Assuming a capacitor with zero ESR, use 方程式 20 to calculate the minimum capacitance required for a given ripple. Using high-ESR capacitors causes additional ripple. Use 方程式 21 to calculate the maximum ESR for a specified ripple. ESR ripple can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used. Use 方程式 22 to calculate the minimum ceramic output capacitance required to meet a load transient requirement. Use 方程式 23 to calculate the RMS current required by the output capacitor for support.

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$$C_O \geq \frac{Dmax \times I_O}{f_S \times V_{rip}} \quad (20)$$

$$ESR \leq \frac{\left(V_{rip} - \frac{Dmax \times I_O}{f_S \times C_O}\right)}{\Delta I_L} \quad (21)$$

$$C_O \geq \frac{\Delta I_{(TRAN)}}{2 \times \pi \times f_{BW} \times \Delta V_{(TRAN)}} \quad (22)$$

$$I_{CO(RMS)} = I_O \sqrt{\frac{Dmax}{(1 - Dmax)}} \quad (23)$$

Using 方程式 20 for this design, the minimum output capacitance for the specified 120-mV output ripple is 8.8 µF. For a maximum transient voltage change ($\Delta V_{(TRAN)}$) of 960 mV with a 400-mA load transient ($\Delta I_{(TRAN)}$), and a 6-kHz control loop bandwidth (f_{BW}) with 方程式 22, the minimum output capacitance is calculated as 11.1 µF. The most stringent criterion is the 11.1 µF for the required load transient. 方程式 23 calculates a 1.58-A RMS current in the output capacitor. The capacitor must also be properly rated for the desired output voltage.

Care must be taken when evaluating ceramic capacitors that derate under DC bias, aging, and AC signal conditions. For example, larger form factor capacitors (in 1206 size) have self-resonant frequencies in the range of the converter switching frequency. Self resonance significantly decreases the effective capacitance. The DC bias also significantly reduces capacitance. Ceramic capacitors can lose as much as 50% of the capacitance when operated at the rated voltage. Therefore, leave a margin when selecting the capacitor voltage rating to ensure adequate capacitance at the required output voltage. For this example, three 4.7-µF, 50-V 1210 X7R ceramic capacitors are used in parallel, leading to a negligible ESR. Selecting 50-V capacitors instead of 35-V capacitors reduces the effects of DC bias and allows this example circuit to be rated for the maximum output voltage range of the TPS55340-Q1 device.

8.2.1.2.7 Selecting the Input Capacitors (C2 and C7)

At least 4.7-µF of ceramic input capacitance is recommended. Additional input capacitance can be required to meet ripple requirements, transient requirements, or both. High-quality ceramic-type X5R or X7R capacitors are recommended to minimize capacitance variations over temperature. The capacitor must also have an RMS current rating greater than the maximum RMS input current of the TPS55340-Q1 device as calculated with 方程式 24. The input capacitor must also be rated greater than the maximum input voltage. Use 方程式 25 to calculate the input voltage ripple.

$$I_{CI(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad (24)$$

$$V_{I(rip)} = \frac{\Delta I_L}{4 \times f_S \times C_I} + \Delta I_L \times R_{(CI)} \quad (25)$$

In the design example, the input RMS current is calculated to be 191 mA. The selected input capacitor is a 10-µF, 35-V 1210 X7R with 3-mΩ ESR. Although a capacitor with a lower voltage rating can be used, a 35-V rated capacitor was selected to limit the effects of DC bias and to allow the circuit to be rated for the entire input range of the TPS55340-Q1 device. The input ripple is calculated to be 30 mV. An additional 0.1-µF, 50-V 0603 X5R is located close to the VIN pin and the GND pin for additional decoupling.

8.2.1.2.8 Setting the Output Voltage (R1 and R2)

To set the output voltage in either DCM or CCM, use 方程式 26 and 方程式 27 to calculate the values of R1 and R2.

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$$V_O = 1.229\ V \times \left(\frac{R1}{R2} + 1\right) \quad (26)$$

$$R1 = R2 \times \left(\frac{V_O}{1.229\ V} - 1\right) \quad (27)$$

Considering the leakage current through the resistor divider and noise decoupling into FB pin, an optimum value for R2 is around 10 kΩ. The output voltage tolerance depends on the $V_{(FB)}$ accuracy and the tolerance of R1 and R2. In this example, with a 24-V output, R1 is calculated to 185.3 kΩ using 方程式 27. The nearest standard value of 187 kΩ is used.

8.2.1.2.9 Setting the Soft-Start Time (C7)

Select the appropriate capacitor to set the soft-start time and avoid overshoot. Increasing the soft-start time reduces the overshoot during start-up. A 0.047-µF ceramic capacitor is used in this example.

8.2.1.2.10 Selecting the Schottky Diode (D1)

The high switching frequency of the TPS55340-Q1 device demands high-speed rectification for optimum efficiency. Ensure that the average current rating and peak current rating of the diode exceed the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the regulated output voltage. The diode must also be rated for the power dissipated, which is calculated using 方程式 28.

$$P_D = V_{(D)} \times I_O \quad (28)$$

In this conservative design example, the selected diode is rated for the maximum output current of 2.13 A. During normal operation with 800-mA output current and assuming a Schottky diode drop of 0.5 V, the diode must be capable of dissipating 400 mW. The recommended minimum ratings for this design are a 40-V, 3-A diode. However, to improve the flexibility of this design, a Diodes Inc. B540-13-F in an SMC package with voltage and current ratings of 40 V and 5 A was selected for this design.

8.2.1.2.11 Compensating the Control Loop (R3, C4, and C5)

The TPS55340-Q1 device requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor (R3) and ceramic capacitor (C4) are connected to the COMP pin to provide a pole and a zero as shown in the application circuit (see 图 8-1). This pole and zero, along with the inherent pole and zero of a boost converter, determine the closed loop frequency response, which is important for converter stability and transient response. Loop compensation must be designed for the minimum operating voltage.

The following equations summarize the loop equations for the TPS55340-Q1 device configured as a CCM boost converter. The equations include the power stage output pole (f_O) and the right-half-plane zero ($f_{(RHPZ)}$) of a boost converter calculated using 方程式 29 and 方程式 30, respectively. When calculating f_O, including the derating of ceramic output capacitors is important. In the example with an estimated 10.2-µF capacitance, these frequencies are calculated to be 980 kHz and 22.1 kHz, respectively. Use 方程式 29 to calculate the DC gain (A) of the power stage, which is 39.9 dB in this design. Use 方程式 32 and 方程式 33 to calculate the compensation pole ($f_{(P)}$) and zero ($f_{(Z)}$) generated by R3, C4, and the internal transconductance amplifier (respectively).

Most CCM boost converters have a stable control loop if $f_{(Z)}$ is set slightly above $f_{(P)}$ through proper sizing of R3 and C4. To start, select a value of 0.1 µF for C4 and a value of 2 kΩ for R3. Increasing R3 or reducing C4 increases the closed loop bandwidth, and therefore improves the transient response. Adjusting R3 and C4 in opposite directions increases the phase and gain margin of the loop, which improves loop stability. TI recommends to limit the bandwidth of the loop to the lower of either 1/5 of the switching frequency (f_S) or 1/3 the RHPZ frequency ($f_{(RHPZ)}$), which is calculated using 方程式 30. Use the spreadsheet tool located on the TPS55340-Q1 product page as an aid in compensation design.

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$$f_O \approx \frac{2}{2\pi \times R_O \times C_O} \quad (29)$$

where

- C_O is the equivalent output capacitor (C_O = C8 + C9 + C10).
- R_O is the equivalent load resistance (V_O / I_O).

$$f_{(RHPZ)} \approx \frac{R_O}{2\pi \times L} \times \left(\frac{V_I}{V_O}\right)^2 \quad (30)$$

$$A = \frac{1.229}{V_O} \times g_{M(ea)} \times 10\ M\Omega \times \frac{V_I}{V_O \times R_{(SENSE)}} \times R_O \times \frac{1}{2} \quad (31)$$

where

- g_{ea} is the error amplifier transconductance located in 节 6.5.
- $R_{(SENSE)}$ (15 mΩ, typical) is the sense resistor in the current control loop.

$$f_{(P)} = \frac{1}{2\pi \times 10\ M\Omega \times C4} \quad (32)$$

$$f_{(Z)} = \frac{1}{2\pi \times R3 \times C4} \quad (33)$$

$$f_{CO(1)} = \frac{f_S}{5} \quad (34)$$

where

- $f_{CO(1)}$ is possible bandwidth.

$$f_{CO(2)} = \frac{f_{(RHPZ)}}{3} \quad (35)$$

where

- $f_{CO(2)}$ is possible bandwidth.

An additional capacitor from the COMP pin to the GND pin (C5) can be used to place a high frequency pole in the control loop. Using this additional capacitor is not always required when using ceramic output capacitors. If a non-ceramic output capacitor is used, an additional zero ($f_{(ZESR)}$) is located in the control loop. Use 方程式 37 to calculate $f_{(ZESR)}$. Use 方程式 38 and 方程式 36 to calculate the value of C5 and the pole created by C5, respectively. Finally, if additional phase margin is required, add an additional zero ($f_{(ZFF)}$) by placing a capacitor ($C_{(FF)}$) in parallel with the top feedback resistor (R1). TI recommends to place the zero at the target cross-over frequency or higher. The feed forward capacitor also adds a pole at a higher frequency. Use 方程式 39 to calculate the recommended value of $C_{(FF)}$.

$$f_{(P2)} = \frac{1}{2\pi \times R3 \times C5} \quad (36)$$

$$f_{(ZESR)} \approx \frac{1}{2\pi \times R_{(ESR)} \times C_O} \quad (37)$$

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$$C5 = \frac{R_{(ESR)} \times C_O}{R3} \tag{38}$$

where

- $R_{(ESR)}$ is the ESR of the output capacitor

$$C_{(FF)} = \frac{1}{2\pi \times R1 \times f_{(ZFF)} \times \sqrt{\frac{V_{ref}}{V_O}}} \tag{39}$$

If a network measurement tool is available, the most accurate compensation design can be achieved following this procedure. The power stage frequency response is first measured using a network analyzer at the minimum 5-V input and maximum 800-mA load. 图 8-2 shows this measurement. In this design, only one pole and one zero are used, therefore, the maximum phase increase from the compensation is 180 degrees. For a 60 degree phase margin, the power stage phase must be –120 degrees at the lowest point. Based on the target 6-kHz bandwidth, the measured power stage gain, $K_{(PS)}$ (f_{BW}), is 24.84 dB and the phase is –110.3 degrees.

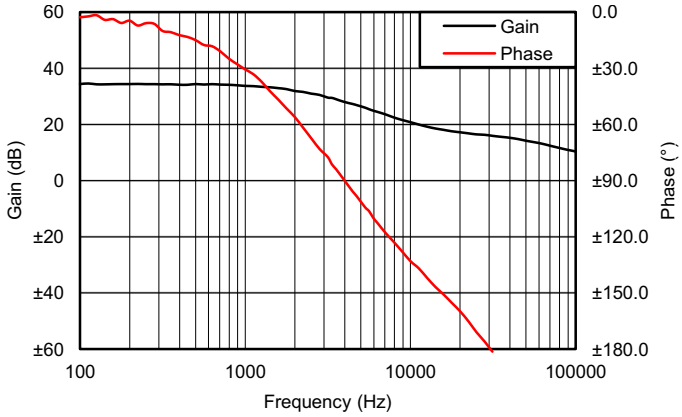

图 8-2. Power Stage Gain and Phase of the Boost Converter

The value of R3 is then selected to set the compensation gain as the reciprocal of the power stage gain at the target bandwidth using 方程式 40. The value of C4 is then selected to place a zero at 1/10 the target bandwidth using 方程式 41. In this case, R3 is calculated to be 2.56 kΩ, and the nearest standard value 2.55 kΩ is used. The value of C4 is calculated to be 0.104 µF and the nearest standard value of 0.100 µF is used. A 100-pF capacitor is selected for C5 to add a high frequency pole at a frequency 100 times the target bandwidth, however adding 100 pF for C5 is not necessary because this design uses all ceramic capacitors.

$$R3 = \frac{1}{\left(g_{M(ea)} \times \frac{R2}{(R1+R2)} \times 10^{\frac{K_{(PS)}(f_{BW})}{20}} \right)} \tag{40}$$

$$C4 = \frac{1}{2\pi \times R3 \times \frac{f_{BW}}{10}} \tag{41}$$

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8.2.1.3 Application Curves

The following application curves are characteristics of the boost converter.

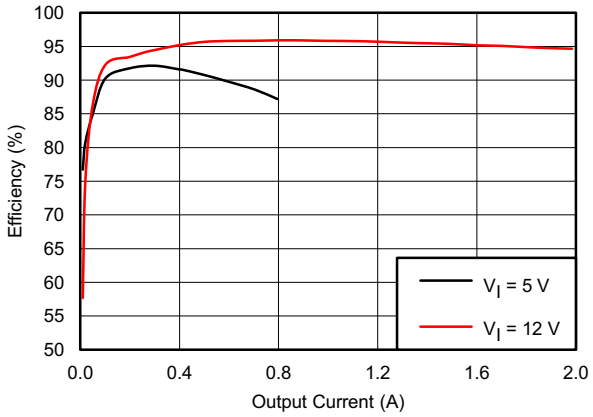

图 8-3. Efficiency Versus Output Current

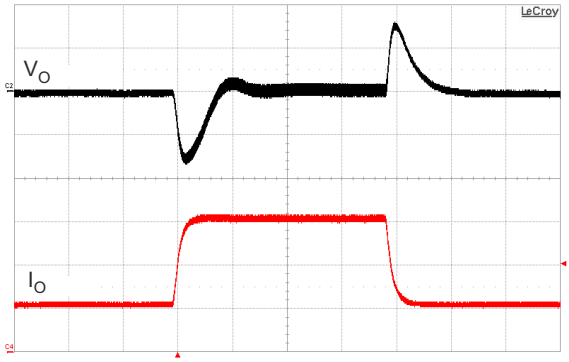

图 8-4. Load Transient Response

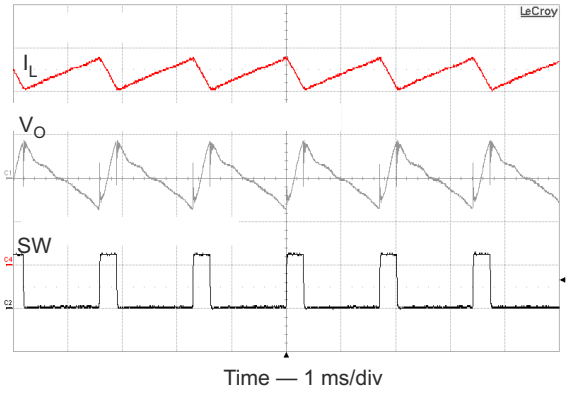

图 8-5. CCM PWM Operation

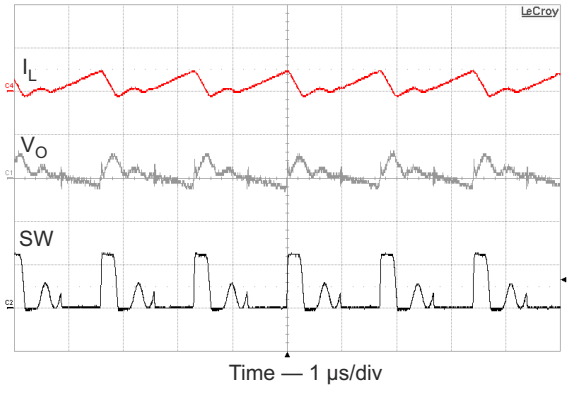

图 8-6. DCM PWM Operation

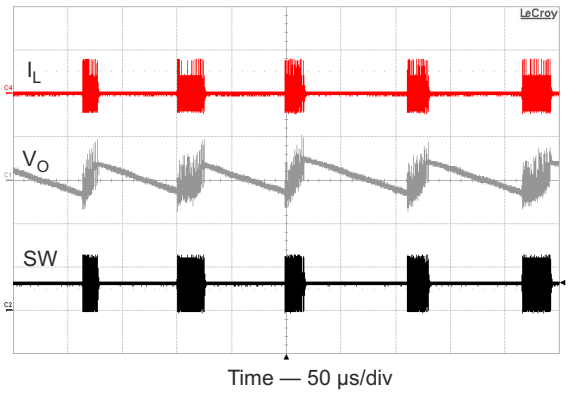

图 8-7. Pulse Skipping

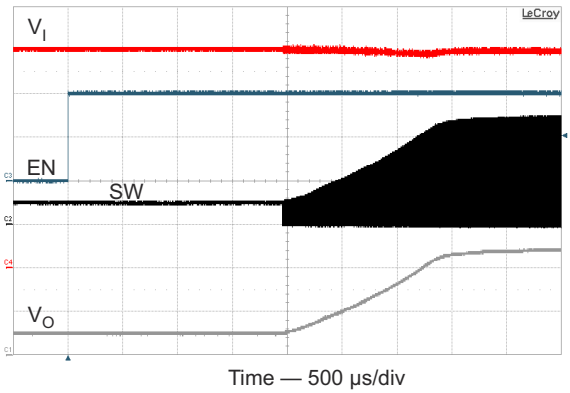

图 8-8. Start-Up

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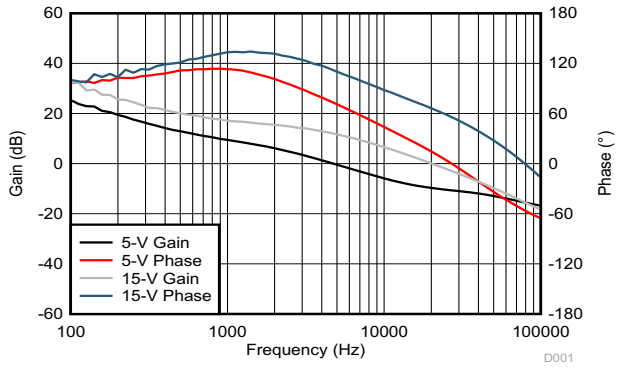

I_O = 800 mA

图 8-9. Closed Loop Gain and Phase of the Boost Converter

8.2.2 TPS55340-Q1 SEPIC Converter

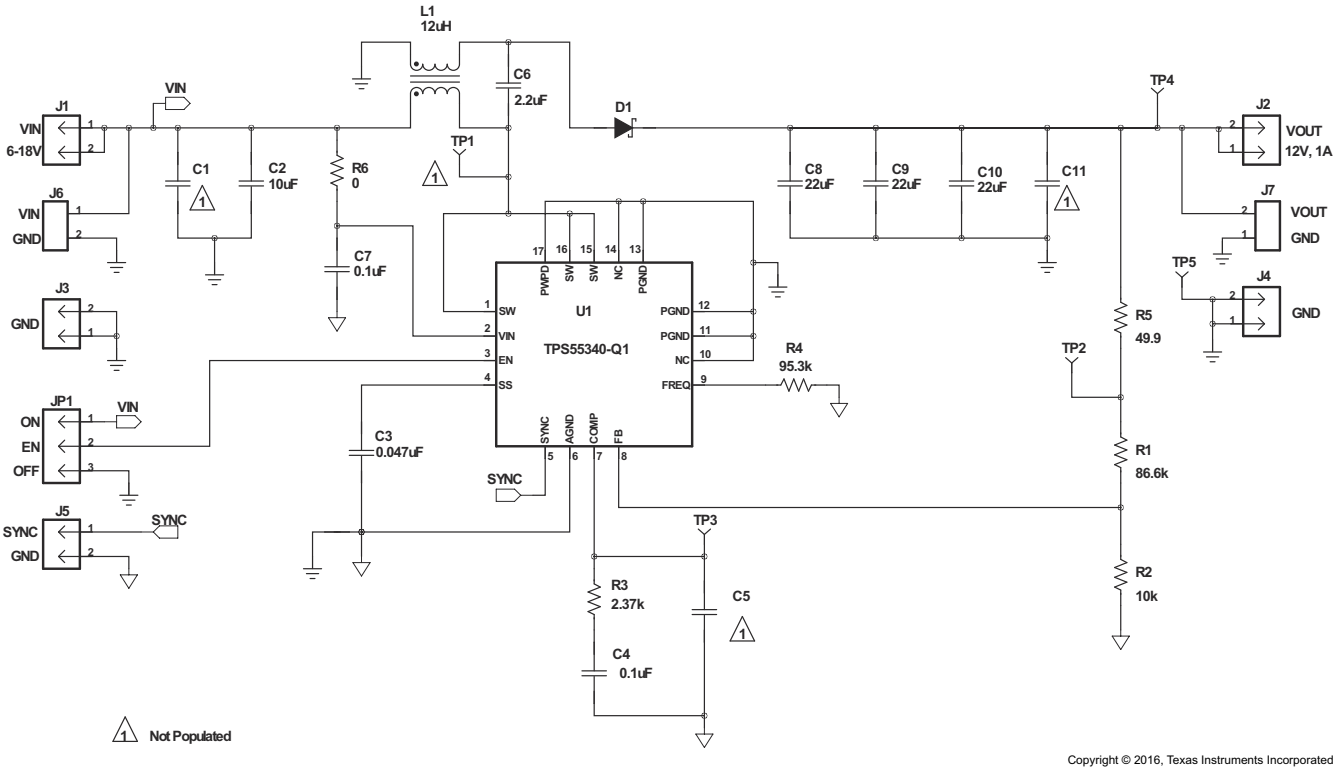

图 8-10. SEPIC-Converter Application Schematic

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8.2.2.1 Design Requirements

The parameters listed in 表 8-2 are used for a SEPIC converter design. These calculations are performed only for CCM operation. The use of a coupled inductor is assumed.

表 8-2. Key Parameters of SEPIC Converter Example

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	12 V
Input voltage	6 V to 18 V, 12 V nominal
Maximum output current	1 A
Transient response 50% load step (ΔV_O = 4%)	480 mV
Output voltage ripple (0.5% of V_O)	60 mV

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Selecting the Switching Frequency (R4)

A 500-kHz switching frequency (f_S) was selected for this design. Use 方程式 1 and the nearest standard value 95.3 kΩ to calculate the value of R4.

8.2.2.2.2 Duty Cycle

Use 方程式 42 to calculate the duty cycle of a SEPIC converter. When selecting the 6-V minimum input, the duty cycle is calculated as 68%. When selecting the 18-V maximum input voltage, the duty cycle is calculated as 41%.

$$D = \frac{V_O + V_{(D)}}{V_O + V_{(D)} + V_I} \tag{42}$$

8.2.2.2.3 Selecting the Inductor (L1)

With an estimated 85% efficiency, the input current is calculated to be 2.35 A using 方程式 11. The minimum inductance is calculated to be 10.5 µH using 方程式 43 with a $K_{(IND)}$ value of 0.3 and a maximum input value of 18 V. The nearest standard value of 12 µH is used. This equation assumes that a coupled inductor is used.

$$L \geq \frac{V_I\,\text{max} \times D\,\text{min}}{2 \times f_S \times I_{I(DC)} \times K_{(IND)}} \tag{43}$$

The inductor ripple current is recalculated to be 615 mA using 方程式 44. The peak current is calculated to be 3.69 A. For the saturation rating of the selected inductor, use the typical current limit. The RMS current for La is approximately the average input current 2.35 A. The RMS current for Lb is approximately the output current of 1 A. For this design, a CoilCraft MSD1260-123 was used with 6.86-A saturation, 74-mΩ DCR, and 3.12-A RMS current rating for one winding.

$$\Delta I_L = \frac{V_I\,\text{max} \times D\,\text{min}}{2 \times f_S \times L} \tag{44}$$

$$I_{L(peak)} = I_{L(a\_peak)} + I_{L(b\_peak)} = \left(I_{I(DC)} + \frac{\Delta I_L}{2}\right) + \left(I_O + \frac{\Delta I_L}{2}\right) \tag{45}$$

8.2.2.2.4 Calculating the Maximum Output Current

The maximum output current is calculated to be 1.47 A using 方程式 46 with the following:

- 6-V minimum input voltage
- 12-µH selected inductance

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- 5.25-A minimum current limit
- Estimated 85% efficiency

$$I_O\,max = \frac{\left(I_{(LIM)} - \Delta I_L\right)}{\left(\frac{V_O}{V_I\,min \times \eta_{(EST)}} + 1\right)} = \frac{\left(I_{(LIM)} - I_{I(DC)} \times K_{(IND)}\right)}{\left(\frac{V_O}{V_I\,min \times \eta_{(EST)}} + 1\right)} \quad (46)$$

8.2.2.2.5 Selecting the Output Capacitor (C8 Through C10)

To meet the 60-mV ripple specification, the minimum output capacitance is calculated to be 22.5 µF with 方程式 47. This design uses ceramic output capacitors and the effects of ESR are ignored. To meet the transient response of 500 mA with less than 480-mV voltage change and a 7-kHz control loop bandwidth, the minimum output capacitance is calculated to be 23.7 µF using 方程式 48. The RMS current is calculated to be 1.44 A using 方程式 24. The output capacitors used in this design are three 22-µF, 25-V X7R 1210 ceramic capacitors. With voltage derating, the effective total output capacitance is estimated to be 30.4 µF.

$$C_O \geq \frac{D\,max \times I_O}{f_S \times V_{rip}} \quad (47)$$

$$C_O \geq \frac{\Delta I_{(TRAN)}}{2\pi \times f_{BW} \times \Delta V_{(TRAN)}} \quad (48)$$

8.2.2.2.6 Selecting the Series Capacitor (C6)

The series capacitor is chosen to limit the ripple current to 5% of the maximum input voltage. Using 方程式 49, the minimum capacitance is 1.5 µF. Using 方程式 50, the RMS current is calculated to be 1.63 A. A 2.2-µF ceramic capacitor in a 1206 package was selected for this design.

$$C_{(P)} \geq \frac{I_O \times D\,max}{0.05 \times V_I\,max \times f_S} \quad (49)$$

$$I_{(CP\_RMS)} = I_{I(DC)} \times \sqrt{\frac{(1 - D\,max)}{D\,max}} \quad (50)$$

8.2.2.2.7 Selecting the Input Capacitor (C2 and C7)

Based on the minimum 4.7-µF ceramic recommended for the TPS55340-Q1 device, a 10-µF X7R input capacitor was used with an additional 0.1 µF placed close to the VIN pin and the GND pin. With an estimated 6-µF capacitance after voltage derating, the input ripple voltage is calculated to be 39.9 mV using 方程式 51. The RMS current of the input capacitance is calculated to be 0.177 A using 方程式 52.

$$V_{I(rip)} = \frac{\Delta I_L}{4 \times f_S \times C_I} \quad (51)$$

$$I_{(CI\_RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad (52)$$

8.2.2.2.8 Selecting the Schottky Diode (D1)

The selected diode must have a minimum breakdown voltage ($V_{(BR)}$). Use 方程式 53 to calculate $V_{(BR)}$ which is 30.5 V in this design. The average current rating is recommended to be greater than the maximum output current. With the maximum 18-V input, average current is calculated to be 2.6 A using 方程式 19. The package must also be capable of handling the power dissipation. With an estimated 0.5-V forward voltage, power

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dissipation is calculated with 方程式 28 to be 500 mW. Diodes Inc. B340B was chosen for this design with a 40-V, 3-A rating in a SMB package.

$$V_{(BR)} = V_O + V_I max + V_F \quad (53)$$

8.2.2.2.9 Setting the Output Voltage (R1 and R2)

With R2 fixed at 10 kΩ, use 方程式 27 to calculate the nearest standard value of 86.6 kΩ for R1.

8.2.2.2.10 Setting the Soft-Start Time (C3)

The recommended 0.047-µF soft-start capacitor is used for C3.

8.2.2.2.11 Mosfet Rating Considerations

In this design, with the maximum input voltage of 18 V and output voltage of 12 V, the FET receives approximately 30 V across drain and source. A 10% tolerance for the MOSFET V_{DS} rating is recommended to account for any ringing. The 40-V rating of the TPS55340-Q1 power MOSFET comfortably satisfies this requirement.

8.2.2.2.12 Compensating the Control Loop (R3 and C4)

This design was compensated by measuring the frequency response of the power stage at the lowest input voltage of 6 V and choosing the components for the desired bandwidth. The lowest right-half plane zero ($f_{(RHPZ)}$) is calculated with 方程式 54 to be 36.7 kHz. When using the recommendation of limiting the bandwidth to 1/3 of $f_{(RHPZ)}$ or less, the recommended maximum bandwidth is 12.2 kHz.

$$f_{(RHPZ)} = \frac{\frac{V_O}{I_O}}{2 \times \pi \times L \times \left(\frac{D}{(1-D)}\right)^2} \quad (54)$$

This design also uses only one pole and one zero. To achieve approximately 60 degrees of phase margin, the power stage phase must be no lower than approximately –120 degrees at the desired bandwidth. To ensure a stable design, R3 was initially set to 1 kΩ and C4 was set to 1 µF. 图 8-11 shows the measurement of the power stage. At 7 kHz, the power stage has a gain of 19.52 dB and phase of –118.1 degrees.

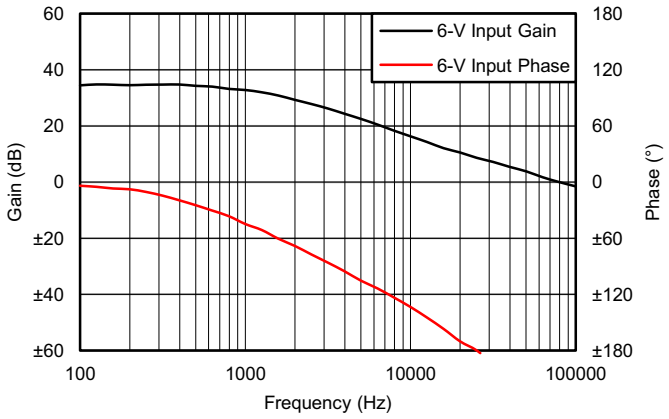

图 8-11. SEPIC Power Stage Gain and Phase

Because no changes occur in the transconductance amplifier, the equations used to calculate the external compensation components in a boost design can be used in the SEPIC design. Using the maximum $g_{m(ea)}$ from the electrical specification of 440 µmho, 方程式 40 calculates the nearest standard value of R3 to be 2.37 kΩ. Using 方程式 41, C4 is calculated to the nearest standard value of 0.1 µF.

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8.2.2.3 Application Curves

The following curves are characteristics of the SEPIC converter.

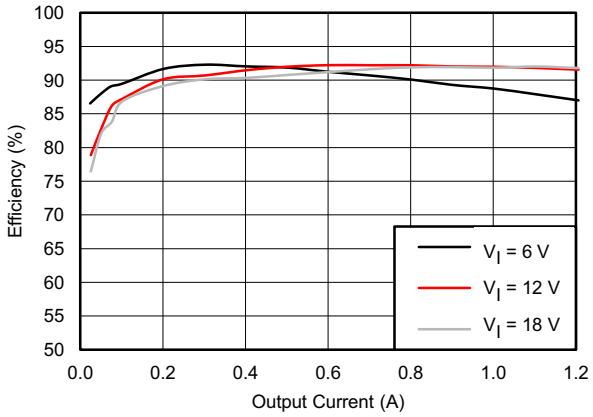
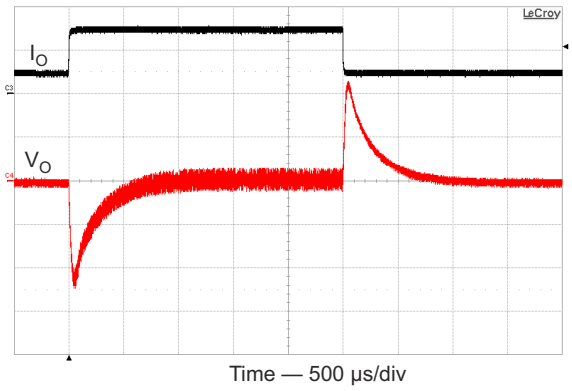
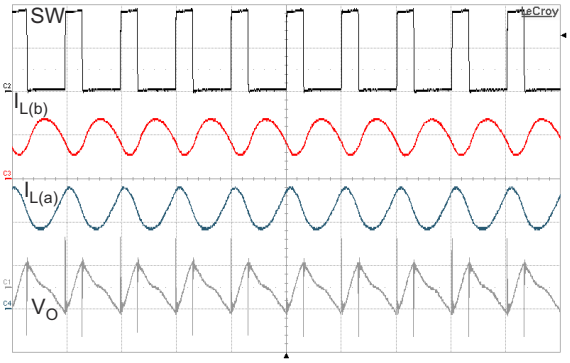


图 8-12. Efficiency vs Output Current



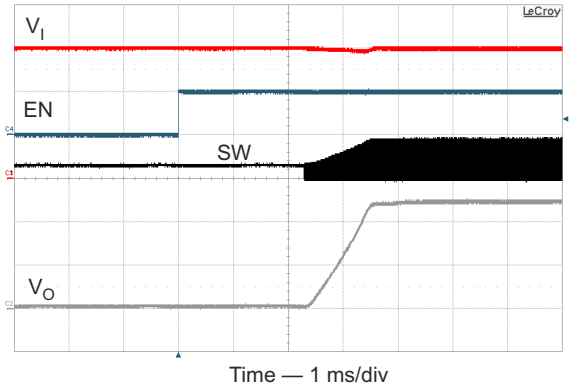
IO = 500 mA/div
VO (AC-coupled) = 200 mV/div

图 8-13. Load Transient Response



V(SW) = 10 V/div
VO (AC-coupled) = 50 mV/div
IL(b) = 1 A/div
IL(a) = 1 A/div

图 8-14. CCM PWM Operation



VI = 2 V/div
VO = 5 V/dvi
V(SW) = 20 V/div
V(EN) = 2 V/div

图 8-15. Output Voltage Soft Start

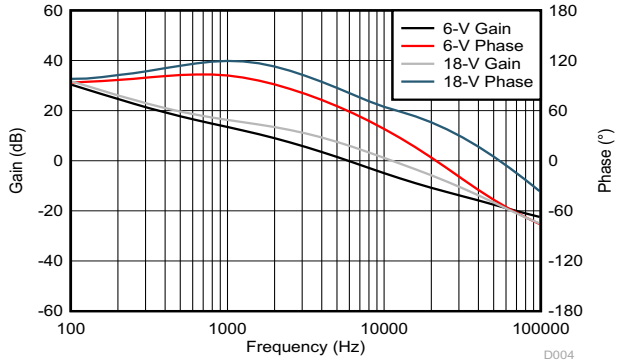


图 8-16. Closed Loop Gain and Phase of the SEPIC Converter

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.9 V and 32 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS55340-Q1 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

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10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those with high frequency and high switch current, printed circuit board (PCB) layout is an important design step. If the layout is not carefully designed, the regulator can suffer from instability as well as noise problems. The following guidelines are recommended for good PCB layout.

- To maximize efficiency, keep switch rise and fall times as short as possible.
- To prevent radiation of high frequency resonance problems, use proper layout of the high frequency switching path.
- Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.
- The high current path including the internal MOSFET switch, Schottky diode, and output capacitor, contains nanosecond rise times and fall times. Keep these rise times and fall times as short as possible.
- Place the input capacitor as close to the VIN pin and the AGND pin as possible to reduce the IC supply ripple.

10.2 Layout Example

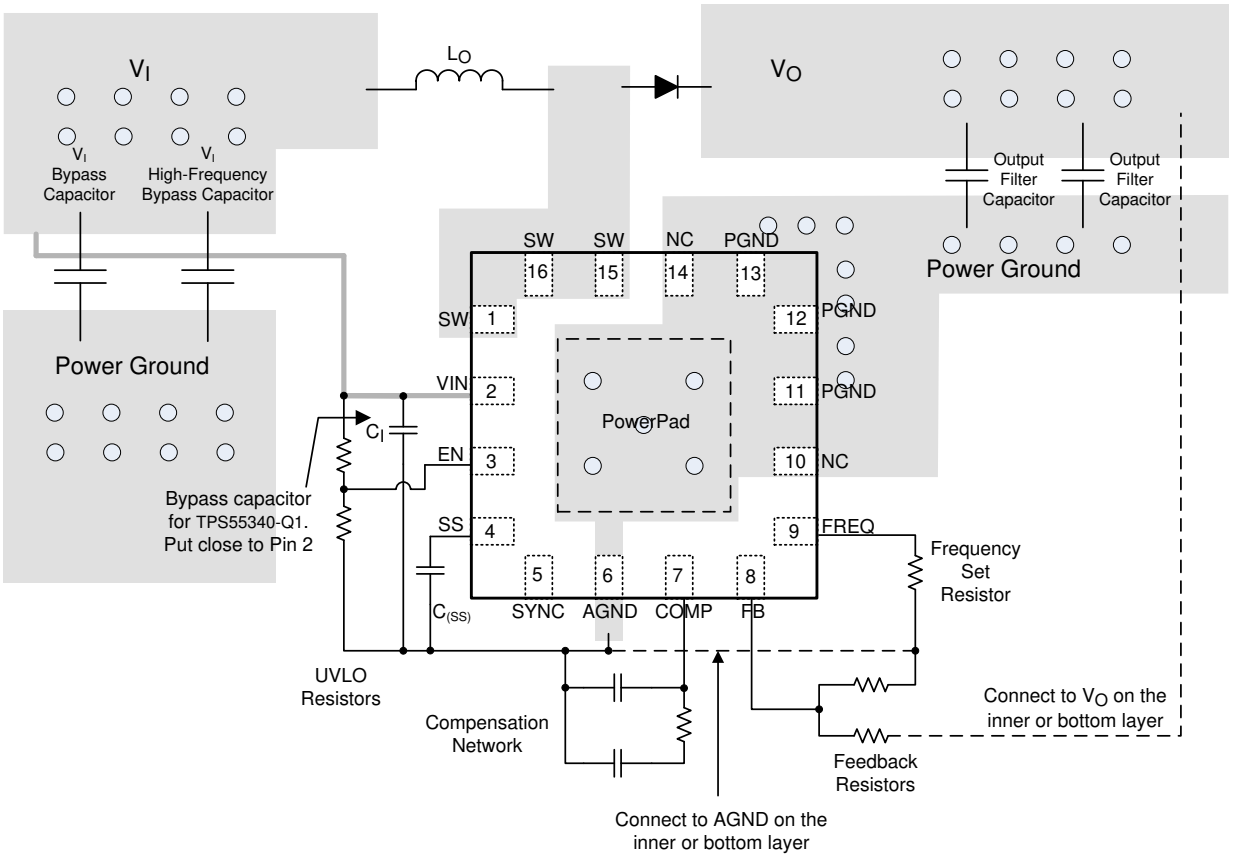

图 10-1. TPS55340-Q1 Example Board Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS55340-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 接收文档更新通知

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11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS55340QRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340Q	Samples
TPS55340QRTETQ1	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	55340Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS55340-Q1 :

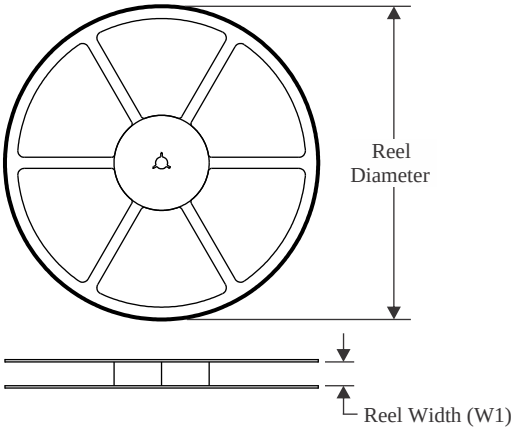
- Catalog : TPS55340
- Enhanced Product : TPS55340-EP

NOTE: Qualified Version Definitions:

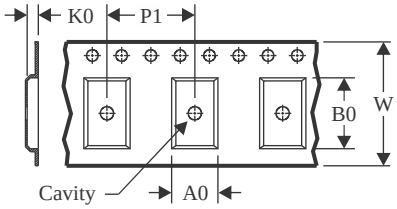
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

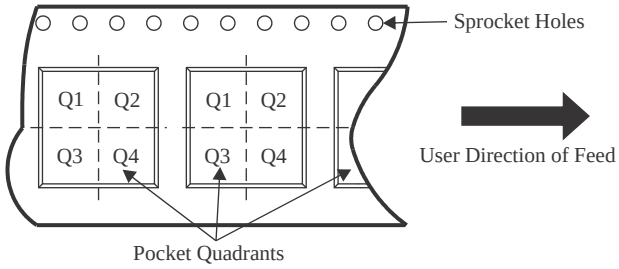


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

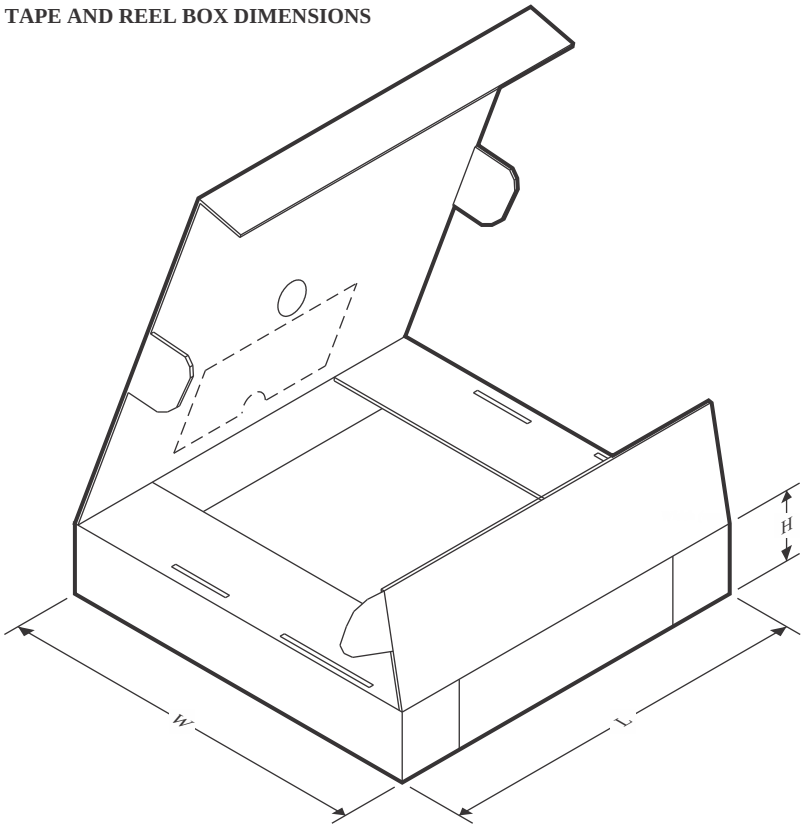
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55340QRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS55340QRTETQ1	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55340QRTERQ1	WQFN	RTE	16	3000	346.0	346.0	33.0
TPS55340QRTETQ1	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

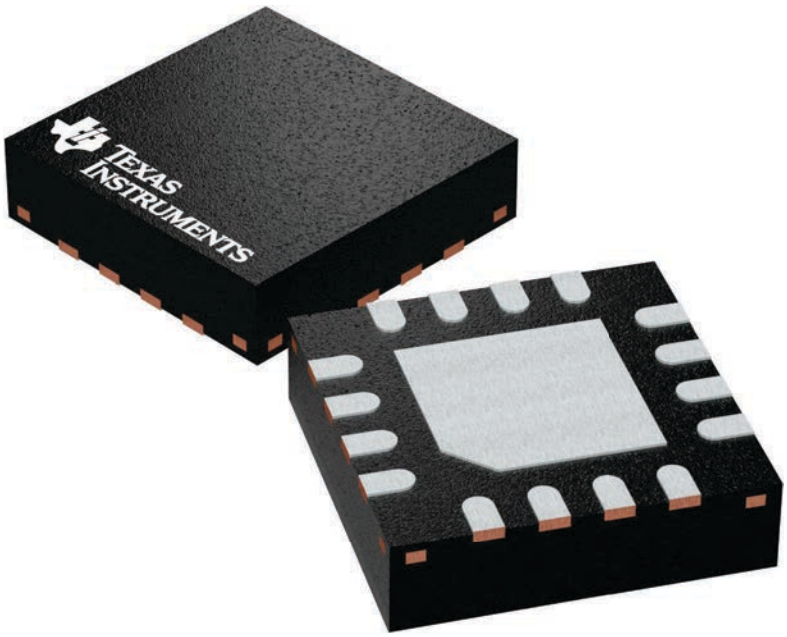
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

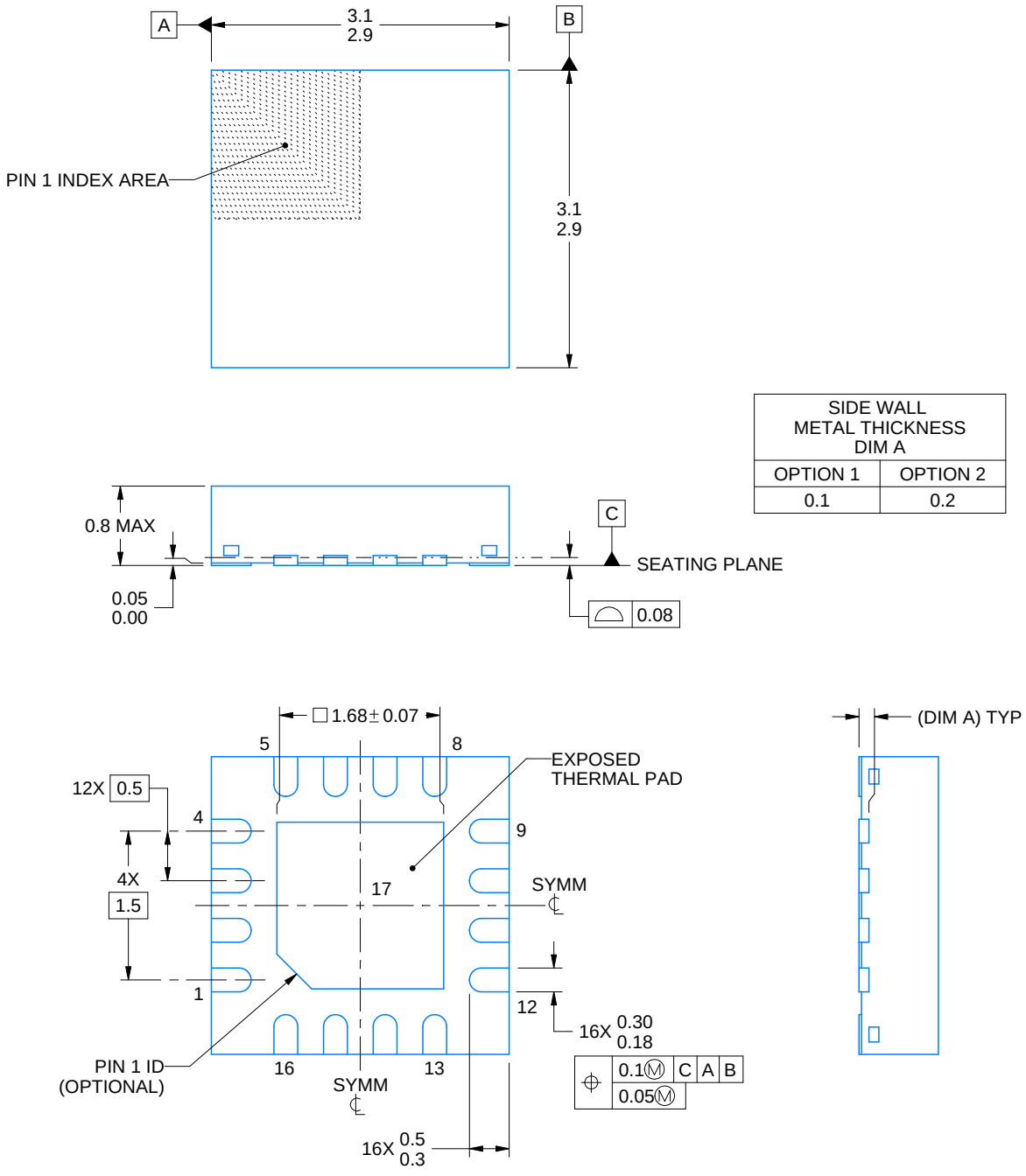


RTE0016C

PACKAGE OUTLINE

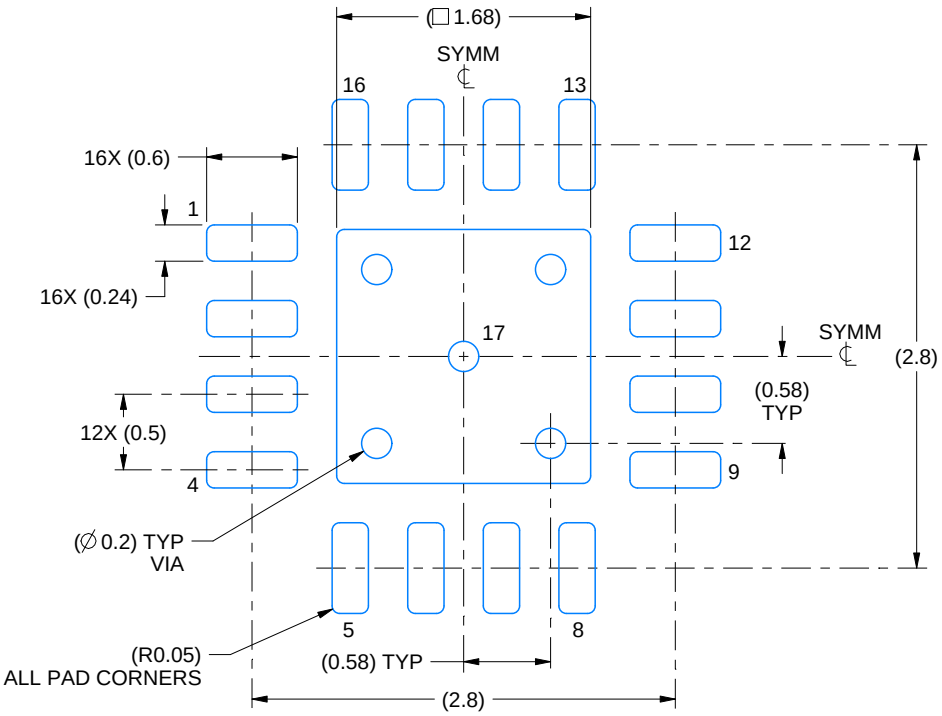
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

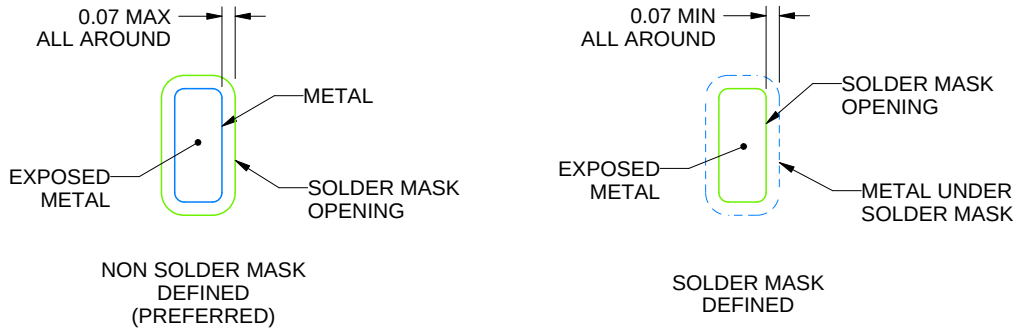


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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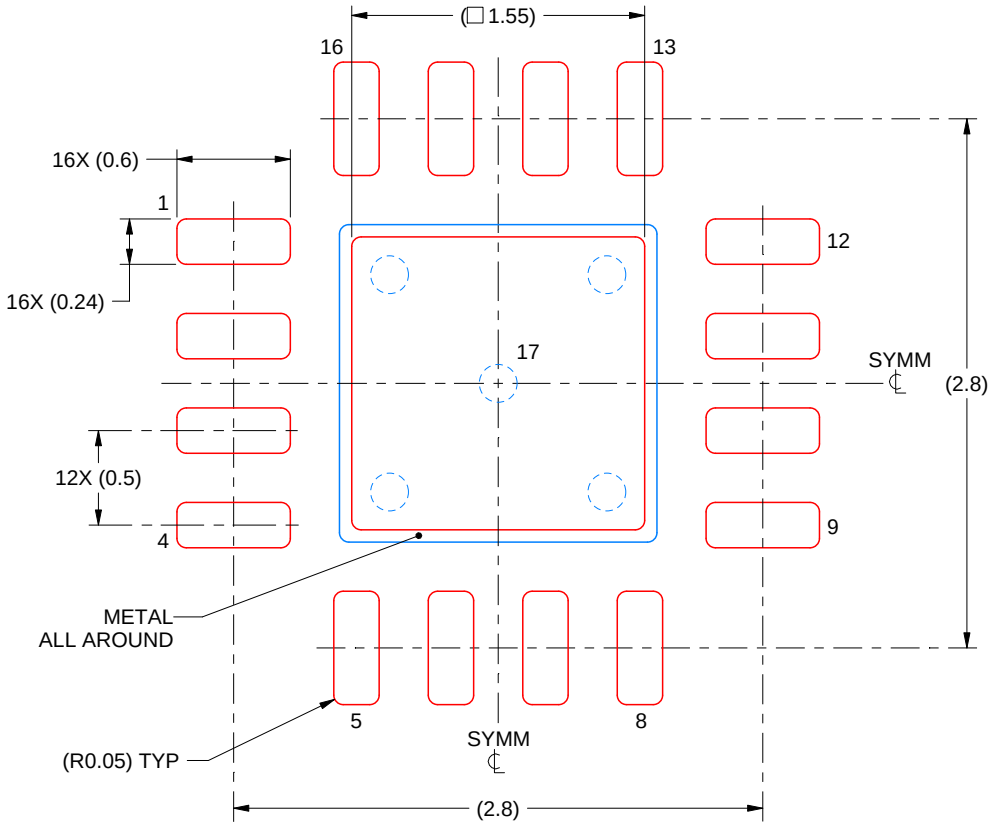
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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