

# TPS564208 采用 SOT-23 封装的 4.5V 至 17V 输入、4A 同步降压稳压器

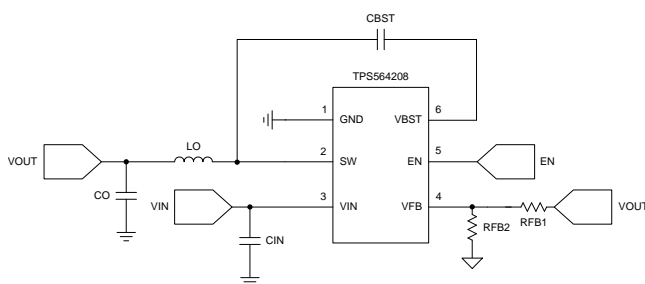
## 1 特性

- TPS564208 具有 50mΩ 和 22mΩ 集成场效应晶体管 (FET) 的 4A 转换器
- D-CAP2™ 模式控制，具有快速动态响应特性
- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.76V 至 7V
- 连续电流模式
- 560kHz 开关频率
- 低关断电流（小于 10μA）
- 1.6% 反馈电压精度 (25°C)
- 从预偏置输出电压中启动
- 逐周期过流限制
- 断续模式过流保护
- 非锁存欠压保护 (UVP) 和热关断 (TSD) 保护
- 固定软启动时间：1.0ms
- 结合使用 TPS564208 和 [WEBENCH® 电源设计器](#) 创建定制设计方案

## 2 应用

- 数字电视电源
- 高清 蓝光™ 光盘播放器
- 网络家庭终端设备
- 数字机顶盒 (STB)
- 安全监控

简化原理图



## 3 说明

TPS564208 是一款采用 SOT-23 封装的简单易用型 4A 同步降压转换器。

该器件经过优化，最大限度地减少了运行所需的外部组件并且可以实现低待机电流。

这些开关模式电源 (SMPS) 器件采用 D-CAP2 模式控制，能够提供快速瞬态响应，并且在无需外部补偿组件的情况下支持诸如高分子聚合物等低等效串联电阻 (ESR) 输出电容以及超低 ESR 陶瓷电容器。

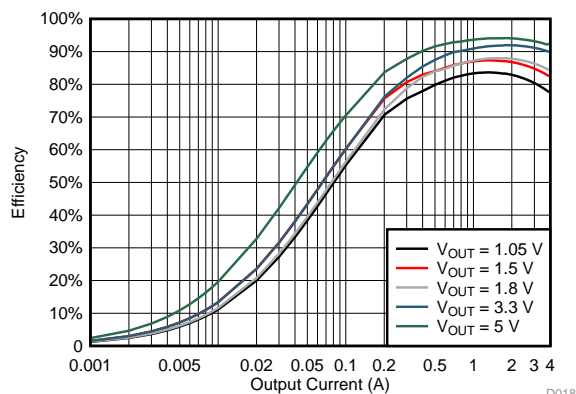
TPS564208 采用 6 引脚 1.6-mm × 2.9-mm SOT (DDC) 封装，额定结温范围为 -40°C 至 125°C。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TPS564208	DDC (6)	1.60mm x 2.90mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

TPS564208 效率



D018



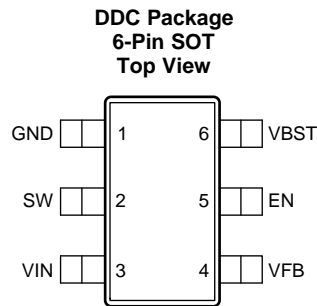
## 目录

<p><b>1</b> 特性 ..... 1</p> <p><b>2</b> 应用 ..... 1</p> <p><b>3</b> 说明 ..... 1</p> <p><b>4</b> 修订历史记录 ..... 2</p> <p><b>5</b> <b>Pin Configuration and Functions</b> ..... 3</p> <p><b>6</b> <b>Specifications</b> ..... 4</p> <p>    6.1 Absolute Maximum Ratings ..... 4</p> <p>    6.2 ESD Ratings ..... 4</p> <p>    6.3 Recommended Operating Conditions ..... 4</p> <p>    6.4 Thermal Information ..... 4</p> <p>    6.5 Electrical Characteristics ..... 5</p> <p>    6.6 Typical Characteristics ..... 6</p> <p><b>7</b> <b>Detailed Description</b> ..... 9</p> <p>    7.1 Overview ..... 9</p> <p>    7.2 Functional Block Diagram ..... 9</p> <p>    7.3 Feature Description ..... 10</p>	<p>    7.4 Device Functional Modes ..... 11</p> <p><b>8</b> <b>Application and Implementation</b> ..... 12</p> <p>    8.1 Application Information ..... 12</p> <p>    8.2 Typical Application ..... 12</p> <p><b>9</b> <b>Power Supply Recommendations</b> ..... 18</p> <p><b>10</b> <b>Layout</b> ..... 19</p> <p>    10.1 Layout Guidelines ..... 19</p> <p>    10.2 Layout Example ..... 19</p> <p><b>11</b> 器件和文档支持 ..... 20</p> <p>    11.1 开发支持 ..... 20</p> <p>    11.2 接收文档更新通知 ..... 20</p> <p>    11.3 社区资源 ..... 20</p> <p>    11.4 商标 ..... 20</p> <p>    11.5 静电放电警告 ..... 20</p> <p>    11.6 Glossary ..... 20</p> <p><b>12</b> 机械、封装和可订购信息 ..... 20</p>
---	--

## 4 修订历史记录

Changes from Revision A (October 2017) to Revision B	Page
<ul style="list-style-type: none"> <li>• Changed the <math>I_{VIN}</math> MAX value From: 780 <math>\mu</math>A To: 820 <math>\mu</math>A in the <i>Electrical Characteristics</i> ..... 5</li> </ul>	5
Changes from Original (March 2016) to Revision A	Page
<ul style="list-style-type: none"> <li>• 已添加 WEBENCH® 电源设计器链接 特性 ..... 1</li> <li>• Changed <math>V_{FBTH}</math> spec MIN from 739 to 745, TYP from 759 to 760, and MAX from 779 to 775 ..... 5</li> <li>• 已添加 <a href="#">使用 WEBENCH® 工具创建定制设计方案</a> ..... 20</li> </ul>	1 5 20

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 $\mu$ F capacitor between VBST and SW pins.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	VIN, EN	-0.3	19	V
	VBST	-0.3	25	V
	VBST (10 ns transient)	-0.3	27	V
	VBST (vs SW)	-0.3	6.5	V
	VFB	-0.3	6.5	V
	SW	-2	19	V
	SW (10 ns transient)	-3.5	21	V
Operating junction temperature, T <sub>J</sub>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Supply input voltage range	4.5		17	V
V <sub>I</sub>	Input voltage range	VBST		23	V
		VBST (10 ns transient)		26	
		VBST (vs SW)		6.0	
		EN	-0.1	17	
		VFB	-0.1	5.5	
		SW	-1.8	17	
		SW (10 ns transient)	-3.5	20	
T <sub>J</sub>	Operating junction temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS564208	UNIT
		DDC (SOT)	
		6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	86.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	39.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	13.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

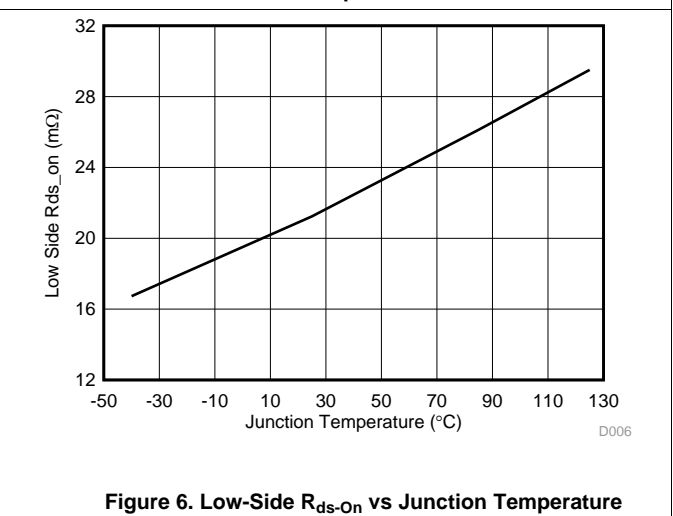
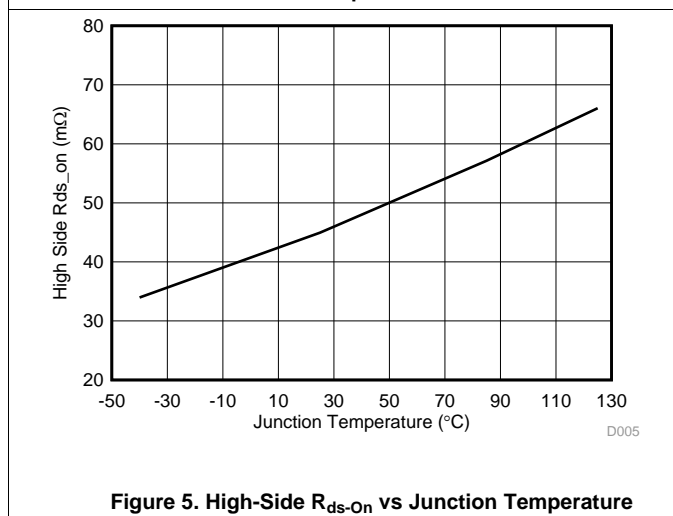
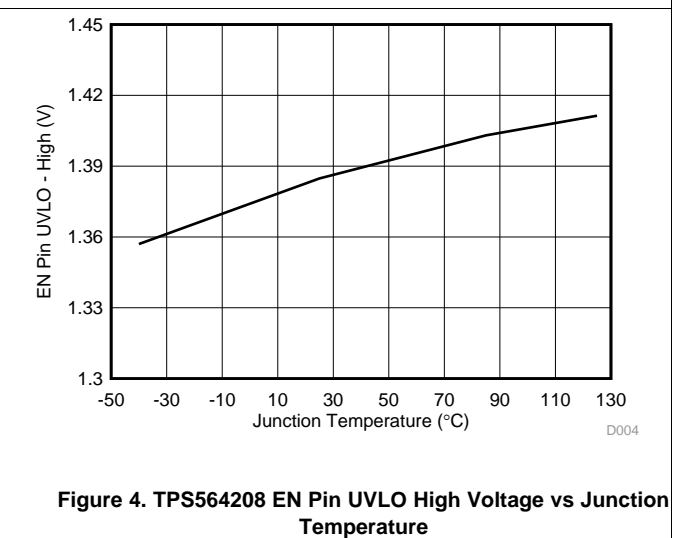
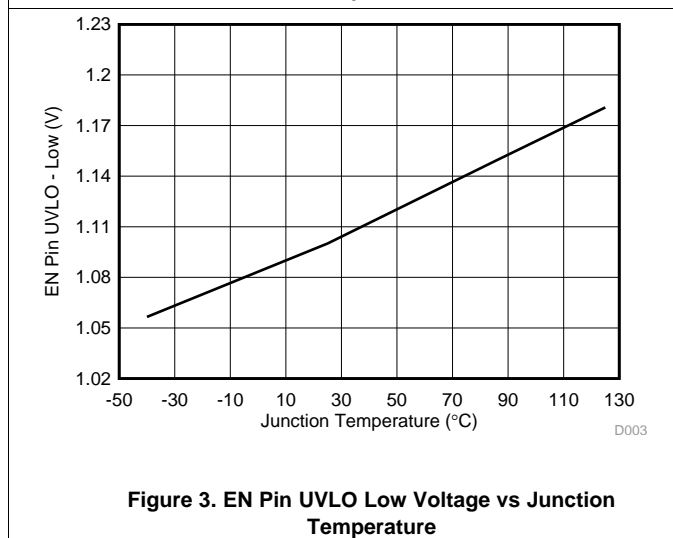
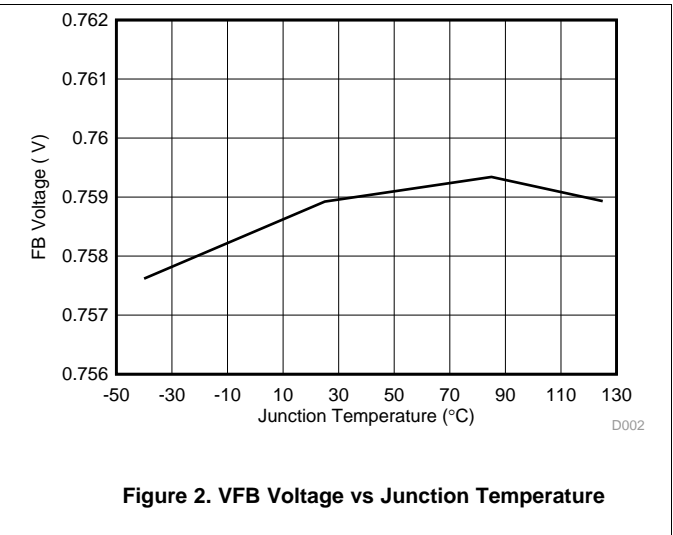
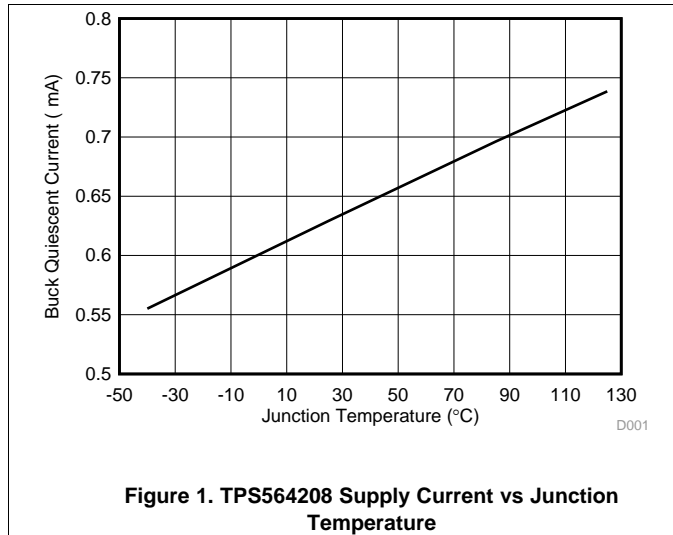
 $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 12\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$I_{VIN}$	Operating – non-switching supply current	$V_{IN}$ current, $EN = 5\text{ V}$ , $V_{FB} = 1\text{ V}$		640	820	$\mu\text{A}$
$I_{VINS\text{DN}}$	Shutdown supply current	$V_{IN}$ current, $EN = 0\text{ V}$		0.9	5	$\mu\text{A}$
<b>LOGIC THRESHOLD</b>						
$V_{ENH}$	EN high-level input voltage	EN	1.6			V
$V_{ENL}$	EN low-level input voltage	EN			0.8	V
$R_{EN}$	EN pin resistance to GND	$V_{EN} = 12\text{ V}$	225	425	900	$\text{k}\Omega$
<b><math>V_{FB}</math> VOLTAGE AND DISCHARGE RESISTANCE</b>						
$V_{FBTH}$	$V_{FB}$ threshold voltage	$V_O = 1.05\text{ V}$ , continuous mode operation	745	760	775	mV
$I_{VFB}$	$V_{FB}$ input current	$V_{FB} = 0.8\text{ V}$		0	$\pm 0.1$	$\mu\text{A}$
<b>MOSFET</b>						
$R_{DS(\text{on})h}$	High-side switch resistance	$T_A = 25^{\circ}\text{C}$ , $V_{BST} - SW = 5.5\text{ V}$		50		$\text{m}\Omega$
$R_{DS(\text{on})l}$	Low-side switch resistance	$T_A = 25^{\circ}\text{C}$		22		$\text{m}\Omega$
<b>CURRENT LIMIT</b>						
$I_{ocl}$	Current limit <sup>(1)</sup>	DC current, $V_{OUT} = 1.05\text{ V}$ , $L_1 = 1.5\text{ }\mu\text{H}$	4.2	6	7.7	A
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold <sup>(1)</sup>	Shutdown temperature		172		$^{\circ}\text{C}$
		Hysteresis		38		
<b>ON-TIME TIMER CONTROL</b>						
$t_{OFF(\text{MIN})}$	Minimum off time	$V_{FB} = 0.68\text{ V}$		220	280	ns
<b>SOFT START</b>						
$t_{SS}$	Soft-start time	Internal soft-start time		1		ms
<b>FREQUENCY</b>						
$F_{sw}$	Switching frequency	$V_{IN} = 12\text{ V}$ , $V_O = 1.05\text{ V}$ , FCCM mode		560		kHz
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>						
$V_{UVP}$	Output UVP threshold	Hiccup detect ( $H > L$ )		65%		
$T_{HICCUP\_WAIT}$	Hiccup on time			1.9		ms
$T_{HICCUP\_RE}$	Hiccup time before restart			15.5		ms
<b>UVLO</b>						
UVLO	UVLO threshold	Wake up VIN voltage		4	4.3	V
		Shutdown VIN voltage	3.3	3.6		
		Hysteresis VIN voltage <sup>(1)</sup>		0.4		

(1) Not production tested.

## 6.6 Typical Characteristics

$V_{IN} = 12\text{ V}$  (unless otherwise noted)



Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$  (unless otherwise noted)

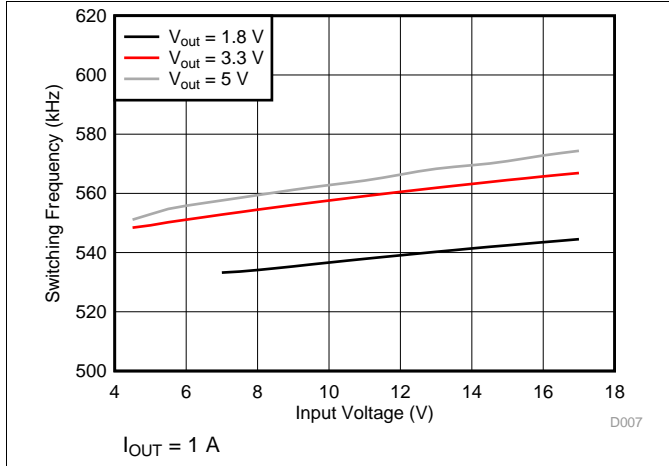


Figure 7. TPS564208 Switching Frequency vs Input Voltage

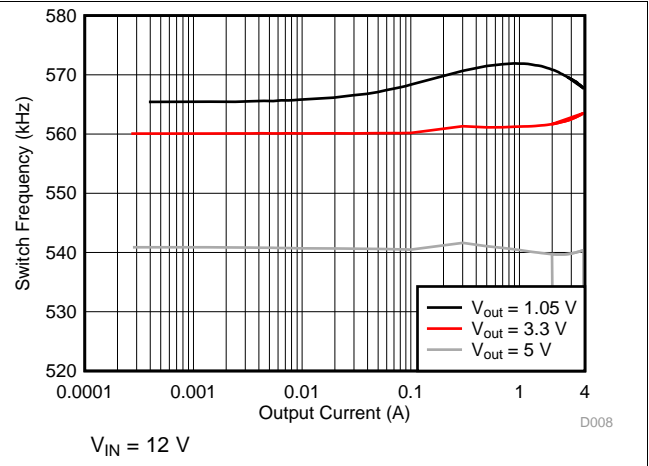


Figure 8. TPS564208 Switching Frequency vs Output Current

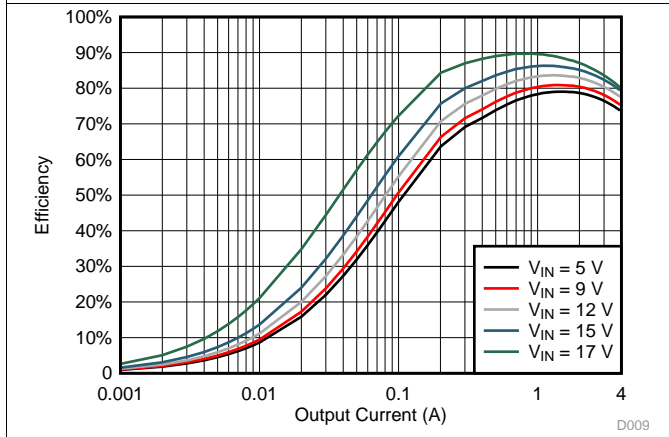


Figure 9. TPS564208  $V_{OUT} = 1.05\text{ V}$  Efficiency,  $L = 2.2\ \mu\text{H}$

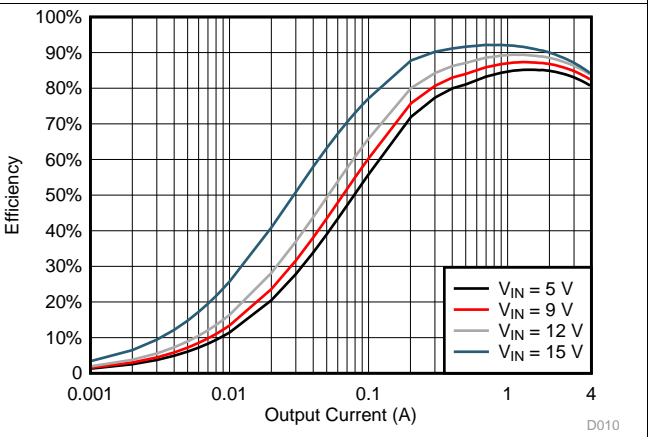


Figure 10. TPS564208  $V_{OUT} = 1.5\text{ V}$  Efficiency,  $L = 2.2\ \mu\text{H}$

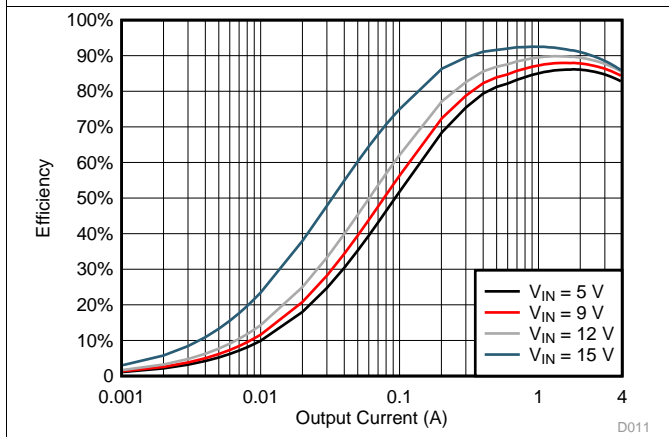


Figure 11. TPS564208  $V_{OUT} = 1.8\text{ V}$  Efficiency,  $L = 2.2\ \mu\text{H}$

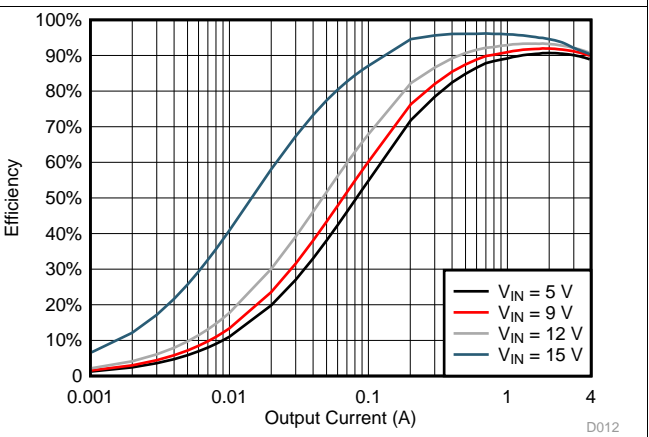
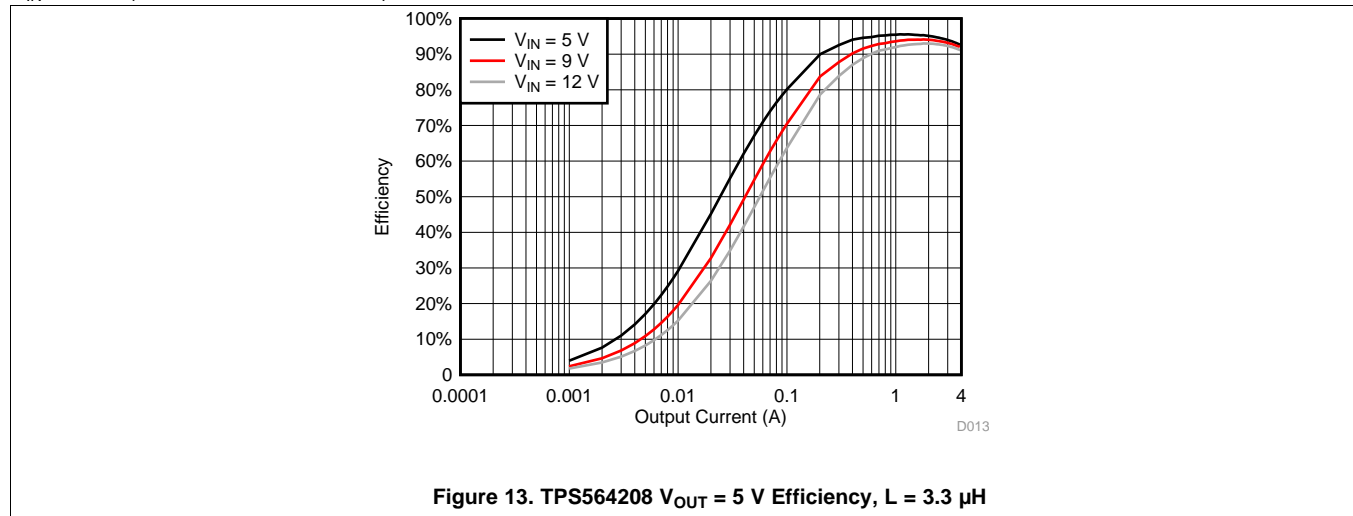


Figure 12. TPS564208  $V_{OUT} = 3.3\text{ V}$  Efficiency,  $L = 2.2\ \mu\text{H}$

**Typical Characteristics (continued)**

$V_{IN} = 12\text{ V}$  (unless otherwise noted)



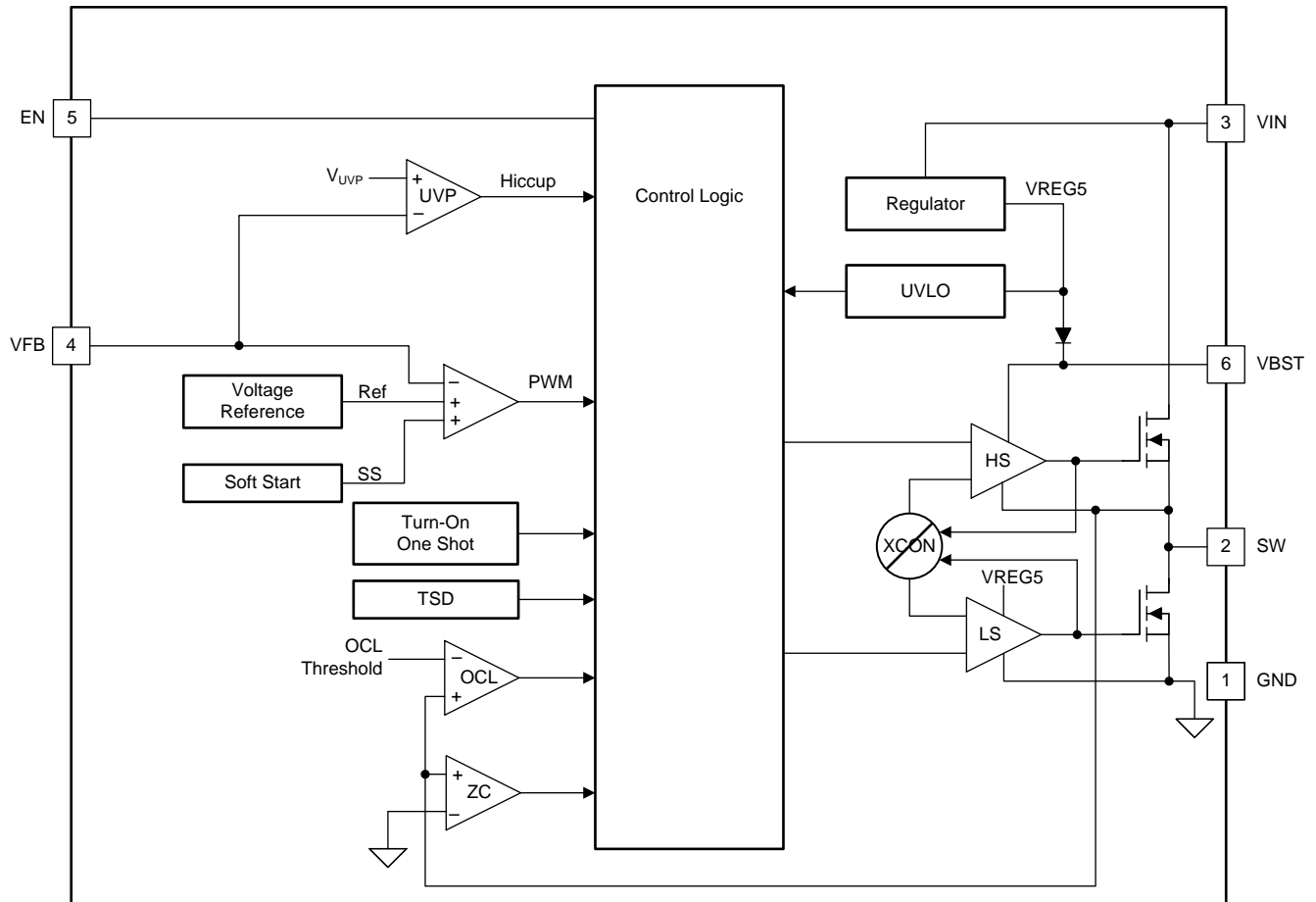


## 7 Detailed Description

### 7.1 Overview

The TPS564208 is a 4-A synchronous step-down converter. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

### 7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS564208 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot duration is set inversely proportional to the converter input voltage,  $V_{IN}$ , and proportional to the output voltage  $V_O$ , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### 7.3.2 Soft Start and Pre-Biased Soft Start

The TPS564208 has an internal 1.0-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage  $V_{FB}$ . This scheme ensures that the converter ramps up smoothly into regulation point.

## Feature Description (continued)

### 7.3.3 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by  $V_{IN}$ ,  $V_{OUT}$ , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current  $I_{out}$ . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device shuts down after the UVP delay time (typically 24  $\mu$ s) and re-starts after the hiccup time (typically 15.5 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

### 7.3.4 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

### 7.3.5 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS564208 operates in the normal switching mode. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS564208 operates at a quasi-fixed frequency of 560 kHz.

### 7.4.2 Standby Operation

When the TPS564208 is operating in normal CCM, it may be placed in standby by asserting the EN pin low.

## 8 Application and Implementation

### NOTE

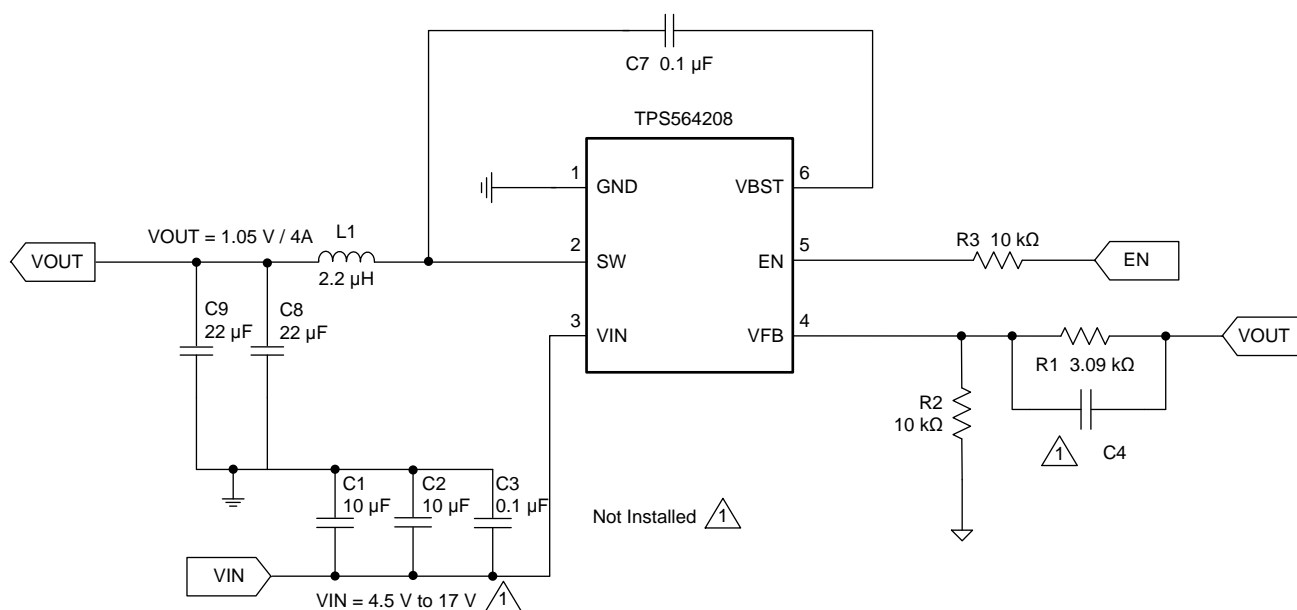
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The device is a typical step-down DC-DC converter for converting a higher dc voltage to a lower dc voltage with a maximum available output current of 4 A. The following design procedure can be used to select component values for the TPS564208. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

### 8.2 Typical Application

The application schematic in Figure 14 shows the TPS564208 4.5-V to 17-V input, 1.05-V output converter design meeting the requirements for 4-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.



Copyright © 2017, Texas Instruments Incorporated

Figure 14. TPS564208 1.05-V, 4-A Reference Design

## Typical Application (continued)

### 8.2.1 Design Requirements

Table 1 shows the design parameters for this application.

**Table 1. Design Parameters**

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	1.05 V
Transient response, 2-A load step	$\Delta V_{out} = \pm 5\%$
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	4 A
Operating frequency	560 kHz

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS564208 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

#### 8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using to calculate  $V_{OUT}$ .

To improve efficiency at very light loads consider using larger value resistors. However, using too high of resistance causes the circuit to be more susceptible to noise; and, voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.760 \times \left( 1 + \frac{R1}{R2} \right) \quad (1)$$

#### 8.2.2.3 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (2)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 2 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

**Table 2. Recommended Component Values**

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C8 + C9 (μF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 to 68
1.05	3.74	10.0	1.5	2.2	4.7	20 to 68
1.2	5.76	10.0	1.5	2.2	4.7	20 to 68
1.5	9.53	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.6	10.0	2.2	2.2	4.7	20 to 68
3.3	33.2	10.0	2.2	2.2	4.7	20 to 68
5	54.9	10.0	3.3	3.3	4.7	20 to 68
6.5	75	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 3, Equation 4, and Equation 5. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 560 kHz for  $f_{SW}$ . Make sure the chosen inductor is rated for the peak current of Equation 4 and the RMS current of Equation 6.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (3)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (4)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (5)$$

For this design example, the calculated peak current is 4.4 A and the calculated RMS current is 4 A. The inductor used is a WE 74431122 with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS564208 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 μF to 68 μF. Use Equation 6 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (6)$$

For this design two TDK C3216X5R0J226M 22-μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

#### 8.2.2.4 Input Capacitor Selection

The TPS564208 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 μF for the decoupling capacitor. An additional 0.1-μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

### **8.2.2.5 Bootstrap Capacitor Selection**

A 0.1- $\mu$ F ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.3 Application Curves

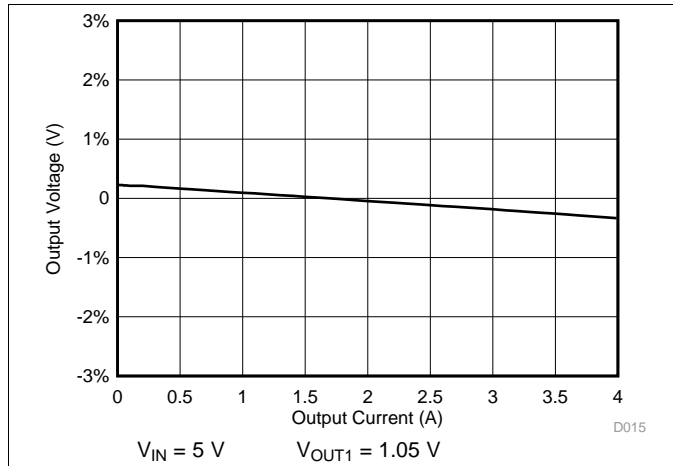


Figure 15. TPS564208 Load Regulation,  $V_{IN} = 5\text{ V}$

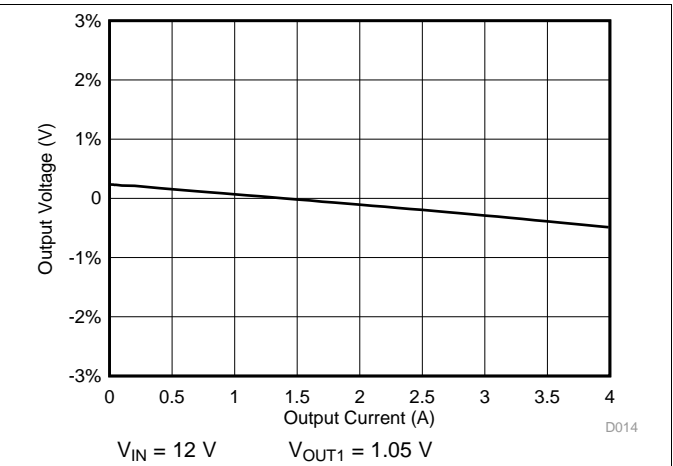


Figure 16. TPS564208 Load Regulation,  $V_{IN} = 12\text{ V}$

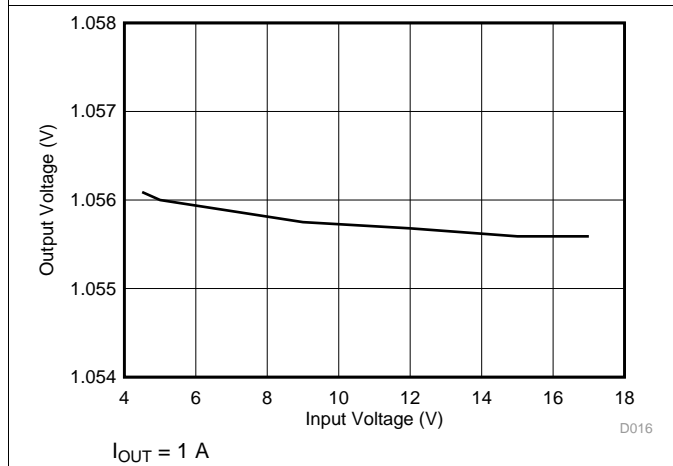


Figure 17. TPS564208 Line Regulation

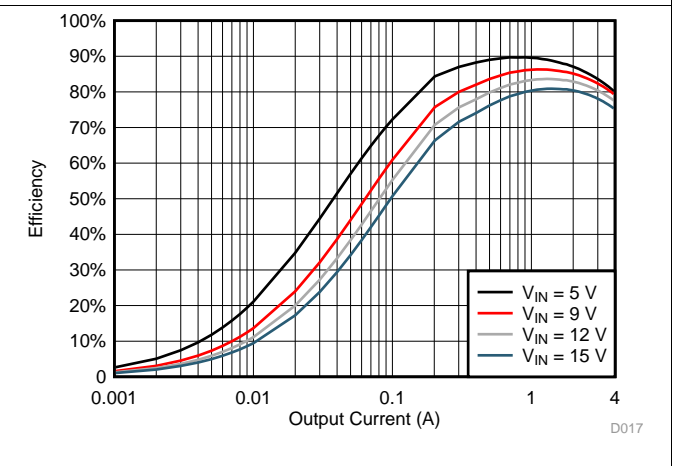


Figure 18. TPS564208 Efficiency,  $V_{out} = 1.05\text{ V}$

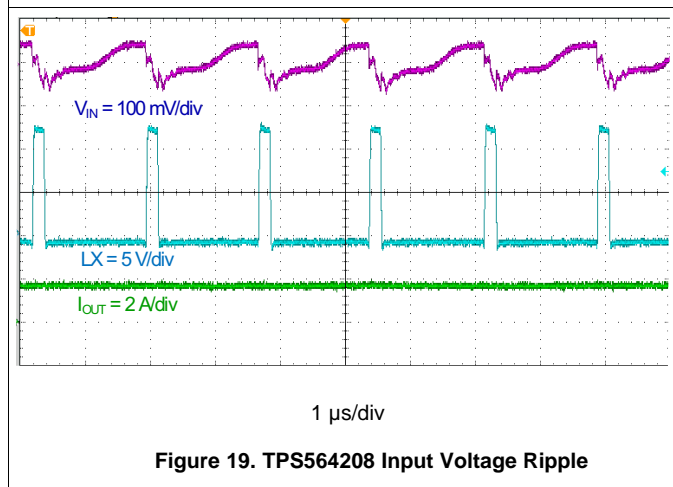


Figure 19. TPS564208 Input Voltage Ripple

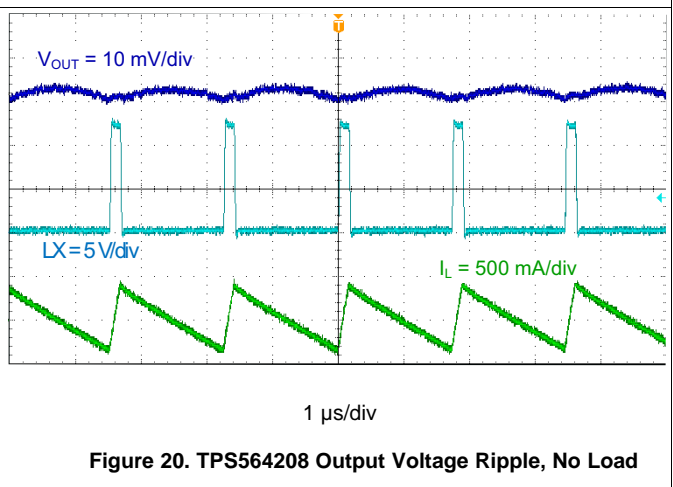
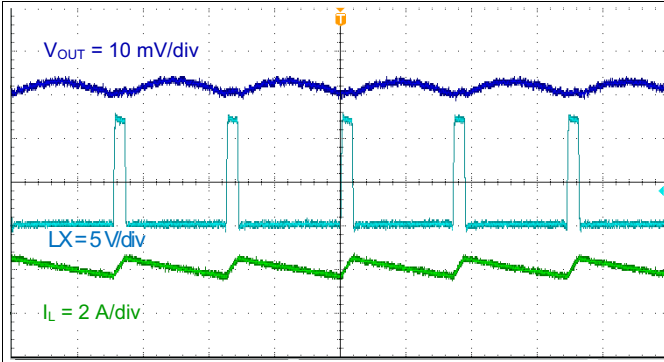


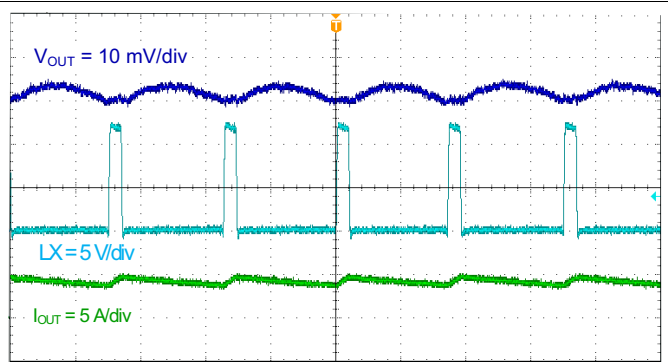
Figure 20. TPS564208 Output Voltage Ripple, No Load





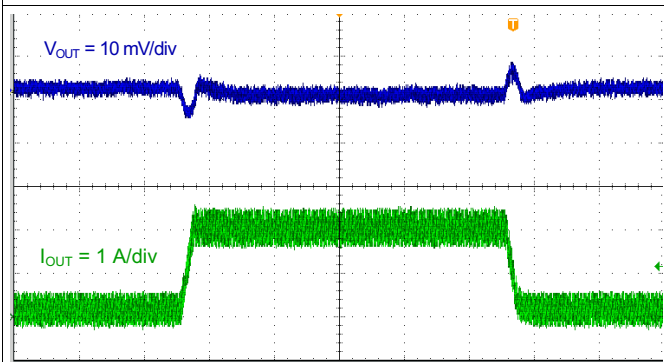
1 μs/div

Figure 21. TPS564208 Output Voltage Ripple, I<sub>OUT</sub> 2 A



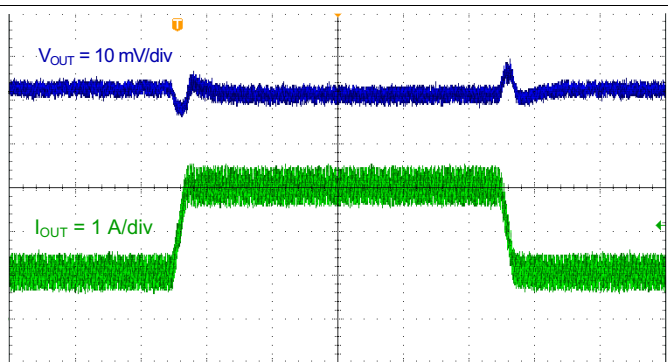
1 μs/div

Figure 22. TPS564208 Output Voltage Ripple, I<sub>OUT</sub> 4 A



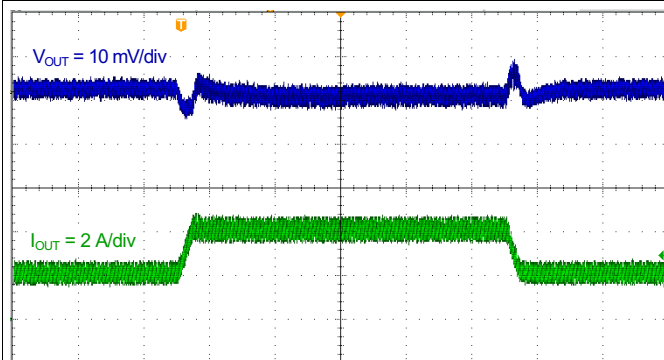
100 μs/div

Figure 23. TPS564208 Transient Response 0.1 to 2 A



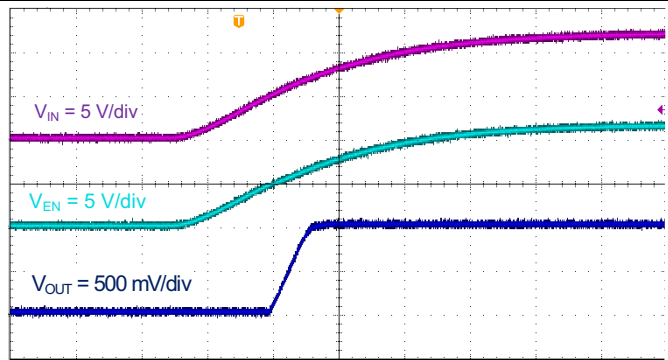
100 μs/div

Figure 24. TPS564208 Transient Response, 1 to 3 A



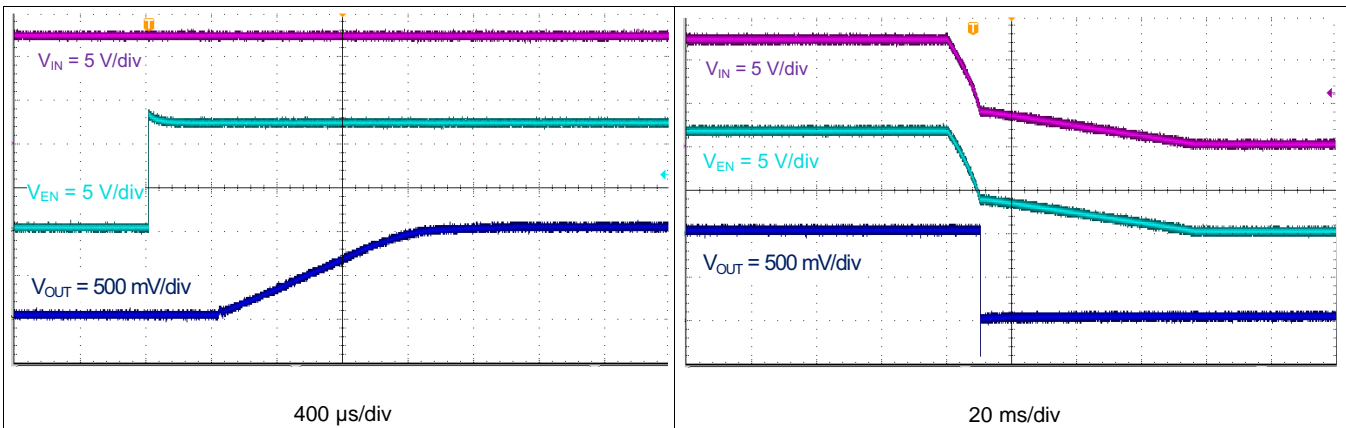
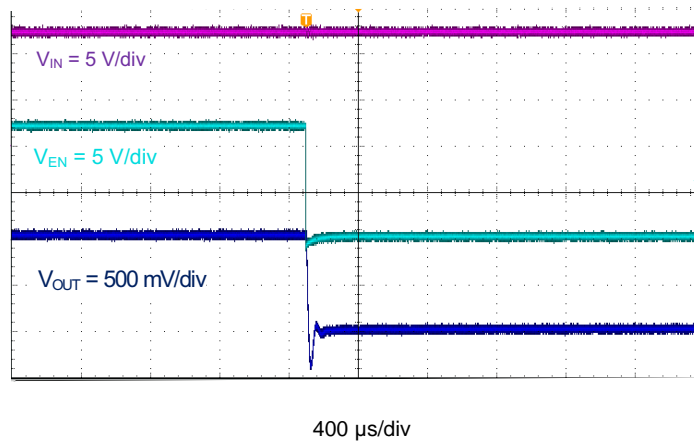
100 μs/div

Figure 25. TPS564208 Transient Response, 2 to 4 A



2 ms/div

Figure 26. TPS564208 Startup Relative to V<sub>IN</sub>


**Figure 27. TPS564208 Startup Relative to EN**
**Figure 28. TPS564208 Shutdown Relative to  $V_{IN}$** 

**Figure 29. TPS564208 Shutdown Relative to EN**

## 9 Power Supply Recommendations

The TPS564208 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is  $V_O / 0.75$ .

## 10 Layout

### 10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

### 10.2 Layout Example

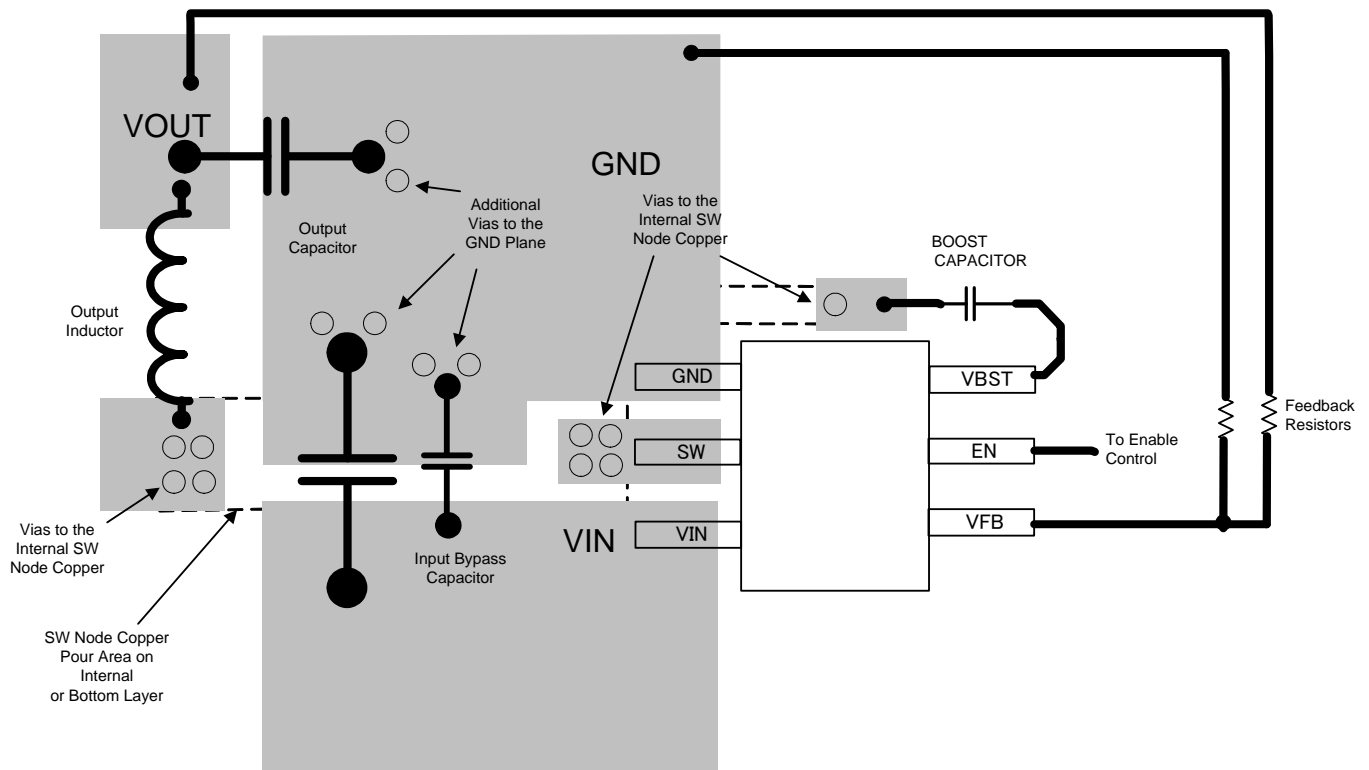


Figure 30. TPS564208 Layout Example

## 11 器件和文档支持

### 11.1 开发支持

#### 11.1.1 使用 WEBENCH® 工具创建定制设计方案

请单击[此处](#)，结合使用 TPS564208 器件和 WEBENCH® 电源设计器创建定制设计方案。

1. 首先键入输入电压 ( $V_{IN}$ )、输出电压 ( $V_{OUT}$ ) 和输出电流 ( $I_{OUT}$ ) 要求。
2. 使用优化器拨盘优化关键参数设计，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH)。

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.4 商标

D-CAP2, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

蓝光 is a trademark of Blu-ray Disc Association.

All other trademarks are the property of their respective owners.

### 11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS564208DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	4208	<a href="#">Samples</a>
TPS564208DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	4208	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS564208DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS564208DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS564208DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS564208DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0



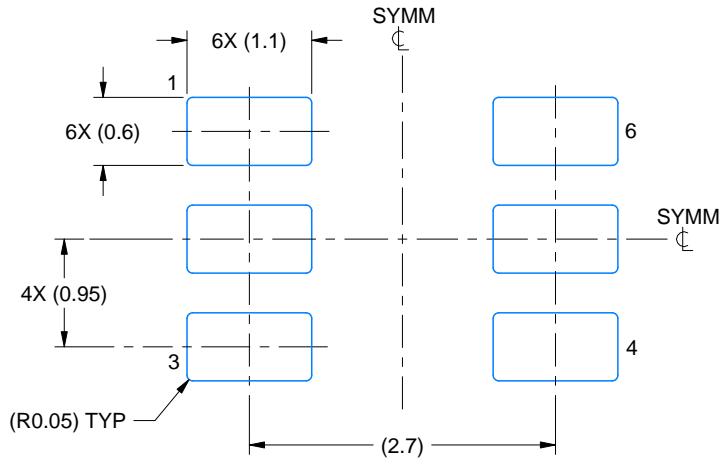


# EXAMPLE BOARD LAYOUT

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司