TPS57114-EP 2.95V 至 6V 输入、3.5A 输出、2MHz 同步降压 SWIFT ™ 转换器

1 特性

- 两个可在 3.5A 负载下获得高效率的 12mΩ（典型值）金属氧化物半导体场效应晶体管 (MOSFET)
- 200kHz 至 2MHz 开关频率
- （-55°C 至 125°C）温度范围内的电压基准为 0.8V ± 1%
- 同步至外部时钟
- 可调缓启动和排序
- 欠压 (UV) 和过压 (OV) 电源良好输出
- 耐热增强型 3mm x 3mm 16 引脚超薄型四方扁平无引线 (WQFN) 封装
- 支持国防、航天和医疗应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 支持军用（-55°C 至 125°C）温度范围
  - 延长的产品生命周期
  - 延长的产品变更通知
  - 产品可追溯性

2 应用范围

- 低压、高密度电源系统
- 针对高性能数字信号处理器 (DSP)，现场可编程门阵列 (FPGA)，特定用途集成电路 (ASIC) 和微处理器的负载点稳压
- 宽带、网络互联及光纤通信基础设施

3 说明

TPS57114-EP 器件是一款具有两个集成 MOSFET 的全功能 6V、
3.5A 同步降压电流模式转换器。

TPS57114-EP 通过集成 MOSFET、执行电流模式控制来减少外部组件数量、启用高达 2MHz 的开关频率来减小电感器尺寸，并借助小型 3mm × 3mm 耐热增强型 WQFN 封装尽量减小集成电路 (IC) 封装尺寸，从而实现小型设计。

TPS57114-EP 可在温度范围内为多种负载提供电压基准 (VREF) 精度达 ±1% 的准确调节。

集成型 12mΩ MOSFET 和 515μA 典型电源电流大大提高了效率。 通过使用使能引脚进入关断模式可以将关断电源电流减小至 5.5μA。

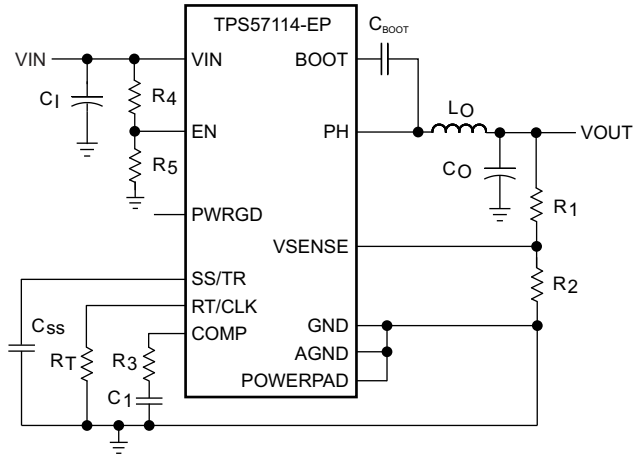
内部的欠压闭锁 (UVLO) 设定值为 2.45V，不过可以使用使能引脚上的电阻器网络编辑阈值来增大此电压值。缓启动引脚控制输出电压启动斜升。 一个开漏电源正常信号表示输出处于其标称电压值的 93% 至 107% 之内。

器件信息(1)

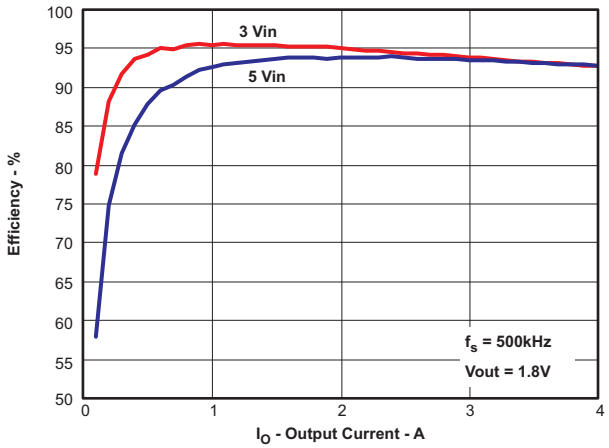
订货编号	封装	封装尺寸（标称值）
TPS57114MRTETEP	WQFN (16)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



效率与输出电流间的关系



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5 修订历史记录

日期	修订版本	注释
2014 年 7 月	*	最初发布。

6 说明（续）

频率折返和热关断功能负责在过流情况下保护器件。

此 SwitcherPro ™ 软件工具，可从www.ti.com/switcherpro内获得，并且支持 TPS57114-EP。

要获得更多 SWIFT ™ 文档，请参见 TI 网站 www.ti.com/swift。

TPS57114-EP 是一款电流模式控制器，可支持降压转换器配置等多种拓扑结构。

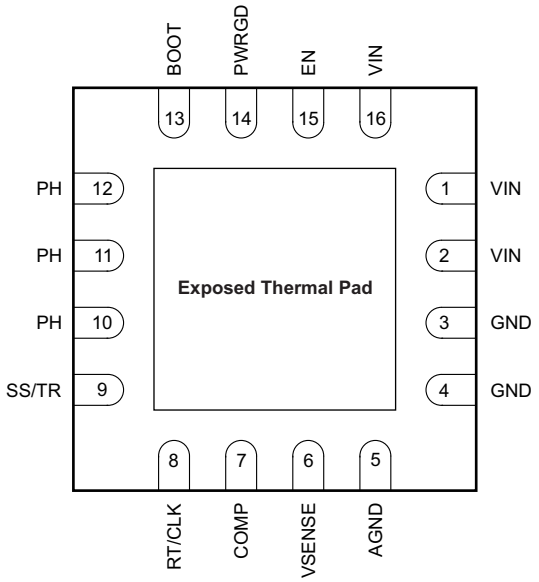
电流模式控制是一种双环路系统。 开关电源电感器隐藏在内部电流控制环路中。 这样可以简化外部电压控制环路的设计并通过多种方式改善电源性能，包括优化动态特性。 这种内部环路的目的是控制状态空间平均的电感器电流，但实际上，电感器瞬时峰值电流是控制的基础（通常检测开关电流，等效于导通期间的电感器电流）。 如果电感器纹波电流较小，电感器峰值电流控制则几乎等效于电感器平均电流控制。

电感器峰值电流控制方法的工作原理是，比较电感器电流（或开关电流）的上升斜率与外部环路设定的电流编程级别。 当瞬时电流达到所需级别时，比较器将关闭电源开关。 相比编程级别而言，电流斜坡通常较小，尤其是在 VIN 较低时。 因此，此方法极易受噪声干扰。 每次接通开关时，都会生成一个噪声尖峰。 控制电路中加上零点几伏的电压就可能导致开关立即关断，从而进入纹波电流更大的次谐波运行模式。 电路布局和旁路对于成功运行至关重要。

峰值电流模式控制方法本身在占空比超过 0.5 之后非常不稳定，可能导致次谐波振荡。 比较器输入端通常应用补偿斜坡（上升斜率等于电感器电流的下降斜率），以消除这种不稳定性。 必须将斜率补偿添加到检测电流波形中，或从控制电压中减去，以确保占空比超过 50% 时的稳定性。 比较器输入端通常应用补偿斜坡（上升斜率等于电感器电流的下降斜率），以消除这种不稳定性。 电流限值控制设计具备诸多优势：

- 电流模式控制提供开关峰值电流限制功能，即逐脉冲限流。
- 由于输出电感器已被推到更高频率，因此控制环路可简化为单极，这样便可以将一个双极系统变成两个实极点。 这样系统就可以降为一阶系统，从而简化控制。
- 可以并行连接多个转换器，并允许各个转换器之间共享等量的电流。
- 由于输入电压出现任何扰动都会反映在开关或电感器电流中，因此，开关内部提供输入电压前馈。 由于开关或电感器电流是直接控制输入，因此可以快速修复扰动问题。
- 误差放大器输出（外部控制环路）定义了一次电流（内部环路）调节脉冲持续时间和输出电压的级别。

7 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	5	Connect analog ground electrically to GND close to the device.
BOOT	13	The device requires a bootstrap capacitor between BOOT and PH. Having the voltage on this capacitor below the minimum required by the BOOT UVLO forces the output to switch off until the capacitor recharges.
COMP	7	Error amplifier output, and input to the output-switch current comparator. Connect frequency-compensation components to this pin.
EN	15	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. An alternative use of this pin can be to set the on-off threshold (adjust UVLO) with two additional resistors.
GND	3	Power ground. Electrically connect this pin directly to the thermal pad under the IC.
	4	
PH	10	The source of the internal high-side power MOSFET and the drain of the internal low-side (synchronous) rectifier MOSFET
	11	
	12	
PWRGD	14	An open-drain output; asserts low if output voltage is low due to thermal shutdown, overcurrent, overvoltage, undervoltage, or EN shutdown.
RT/CLK	8	Resistor-timing or external-clock input pin.
SS/TR	9	Slow start and tracking. An external capacitor connected to this pin sets the output-voltage rise time. Another use of this pin is for tracking.
VIN	1	Input supply voltage, 2.95 to 6 V
	2	
	16	
VSENSE	6	Inverting node of the transconductance (gm) error amplifier
Thermal pad	—	Connect the GND pin to the exposed thermal pad for proper operation. Connect this thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

8 Specifications

8.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7	V
	EN	–0.3	7	
	BOOT		PH + 7	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	7	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	7	
Output voltage	BOOT-PH		7	V
	PH	–0.6	7	
	PH 10-ns transient	–2	10	
Source current	EN		100	µA
	RT/CLK		100	µA
Sink current	COMP		100	µA
	PWRGD		10	mA
	SS/TR		100	µA
Temperature	T_J	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4000	4000	V
		Machine model (MM)	–200	200	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1500	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Input voltage	2.95		6	V
T_A	Operating ambient temperature	–55		125	°C
T_J	Operating junction temperature	–55		150	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS57114-EP RTE 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	44.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	46.1	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	16	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	16.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(7)	4.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

8.5 Electrical Characteristics

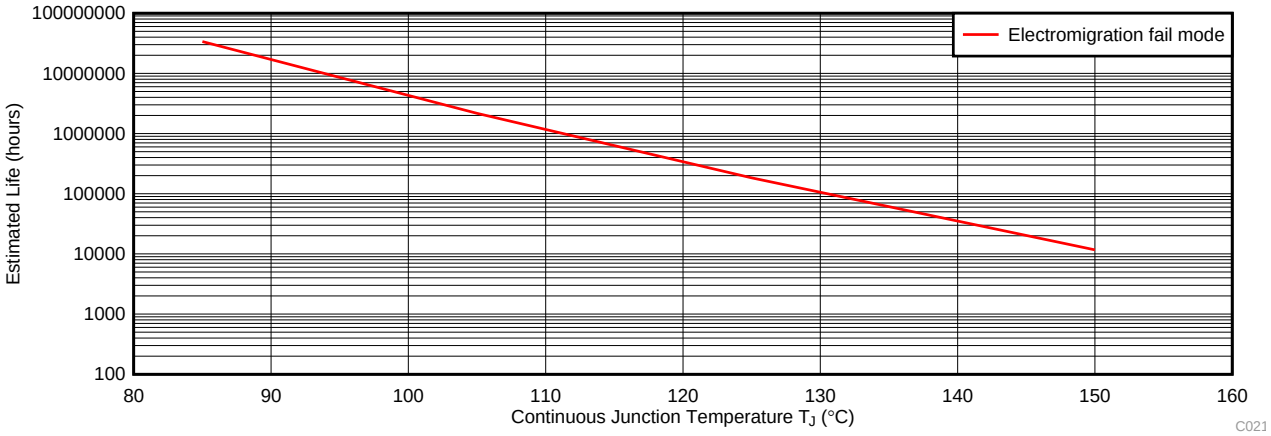
T_J = –55°C to 150°C, VIN = 2.95 to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage-lockout threshold	VIN UVLO START		2.28	2.5	V
	VIN UVLO STOP		2.45	2.6	V
Shutdown supply current	$V_{(EN)}$ = 0 V, 2.95 V ≤ $V_{(VIN)}$ ≤ 6 V		5.5	15	µA
Quiescent current – I_q	$V_{(VSENSE)}$ = 0.9 V, $V_{(VIN)}$ = 5 V, RT = 400 kΩ		515	750	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.25		V
	Falling		1.18		
Input current	Enable threshold + 50 mV		–3.2		µA
	Enable threshold – 50 mV		–1.65		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage reference	2.95 V ≤ $V_{(VIN)}$ ≤ 6 V, –55°C < T_J < 150°C	0.79	0.8	0.81	V
MOSFET					
High-side switch resistance	BOOT-PH = 5 V		12	30	mΩ
	BOOT-PH = 2.95 V		16	30	
Low-side switch resistance	$V_{(VIN)}$ = 5 V		13	30	mΩ
	$V_{(VIN)}$ = 2.95 V		17	30	
ERROR AMPLIFIER					
Input current			2		nA
Error-amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		245		µS
Error-amplifier transconductance (gm) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, $V_{(VSENSE)}$ = 0.4 V		79		µS
Error-amplifier source and sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±20		µA
COMP to Iswitch gm			25		S

Electrical Characteristics (continued)

T_J = –55°C to 150°C, VIN = 2.95 to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT					
Current-limit threshold	$V_{(VIN)}$ = 2.95 V, 25°C < T_J < 150°C	5	6.4		A
	T_J = –55°C	4			
	$V_{(VIN)}$ = 6 V, 25°C < T_J < 150°C	4.4	5.56		
	T_J = –55°C	4			
THERMAL SHUTDOWN					
Thermal shutdown			168		°C
Hysteresis			20		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching frequency range using RT mode		200		2000	kHz
Switching frequency	$R_{(RT/CLK)}$ = 400 kΩ	400	500	600	kHz
Switching frequency range using CLK mode		300		2000	kHz
Minimum CLK pulse duration		80			ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 400 kΩ		0.5		V
RT/CLK high threshold			1.6	2.5	V
RT/CLK low threshold		0.4	0.6		V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		90		ns
PLL lock in time	Measure at 500 kHz		42		µs
PH (PH PIN)					
Minimum on-time	Measured at 50% points on PH, I_{OUT} = 3.5 A		75		ns
	Measured at 50% points on PH, $V_{(VIN)}$ = 6 V, I_{OUT} = 0 A		120		
Minimum off-time	Prior to skipping off pulses, BOOT-PH = 2.95 V, I_{OUT} = 3.5 A		60		ns
Rise time	$V_{(VIN)}$ = 6 V, 3.5 A		2.25		V/ns
Fall time			2		
BOOT (BOOT PIN)					
BOOT charge resistance	$V_{(VIN)}$ = 5 V		16		Ω
BOOT-PH UVLO	$V_{(VIN)}$ = 2.95 V		2.1		V
SLOW START AND TRACKING (SS/TR PIN)					
Charge current	$V_{(SS/TR)}$ = 0.4 V		2		µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		54		mV
SS/TR to reference crossover	98% normal		1.1		V
SS/TR discharge voltage (overload)	$V_{(VSENSE)}$ = 0 V		60		mV
SS/TR discharge current (overload)	$V_{(VSENSE)}$ = 0 V, $V_{(SS/TR)}$ = 0.4 V		350		µA
SS discharge current (UVLO, EN, thermal fault)	$V_{(VIN)}$ = 5 V, $V_{(SS)}$ = 0.5 V		1.9		mA
POWER-GOOD (PWRGD PIN)					
VSENSE threshold	$V_{(VSENSE)}$ falling (fault)		91		%$V_{(VREF)}$
	$V_{(VSENSE)}$ rising (good)		93		
	$V_{(VSENSE)}$ rising (fault)		109		
	$V_{(VSENSE)}$ falling (good)		107		
Hysteresis	$V_{(VSENSE)}$ falling		2		%$V_{(VREF)}$
Output high leakage	$V_{(VSENSE)}$ = $V_{(VREF)}$, $V_{(PWRGD)}$ = 5.5 V		7		nA
On-resistance			56	100	Ω
Output low	$I_{(PWRGD)}$ = 3 mA		0.3		V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.650	1.5	V



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. TPS57114-EP Derating Chart

8.6 Typical Characteristics

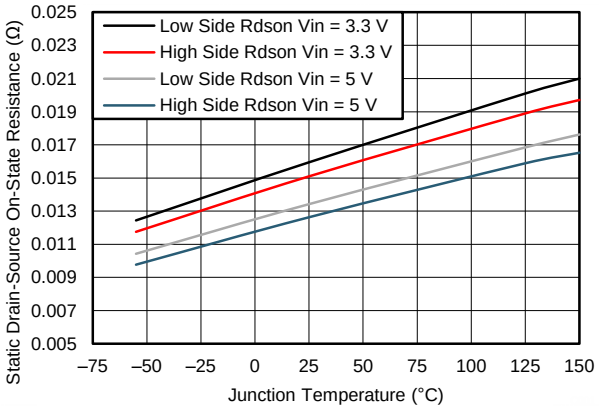


Figure 2. High-Side and Low-Side $r_{ds(on)}$ vs Temperature

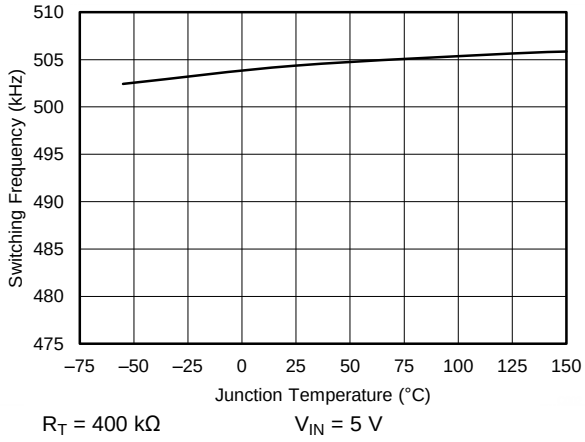


Figure 3. Frequency vs Temperature

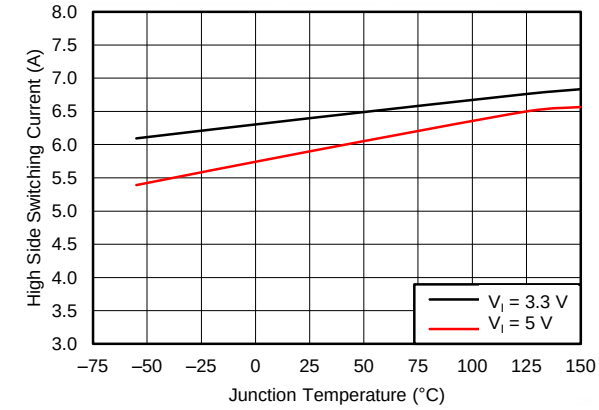


Figure 4. High-Side Current Limit vs Temperature

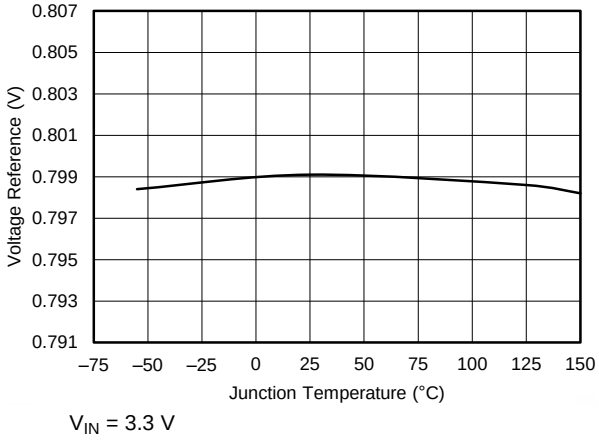


Figure 5. Voltage Reference vs Temperature

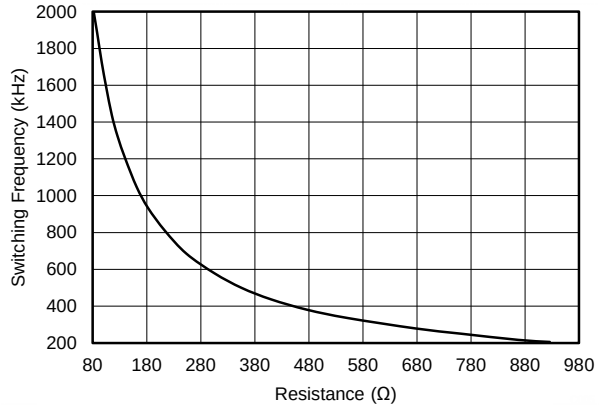


Figure 6. Switching Frequency vs RT Resistance, Low-Frequency Range

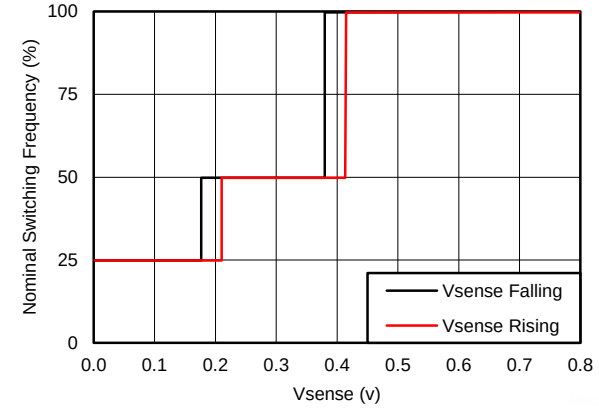


Figure 7. Switching Frequency vs VSENSE

Typical Characteristics (continued)

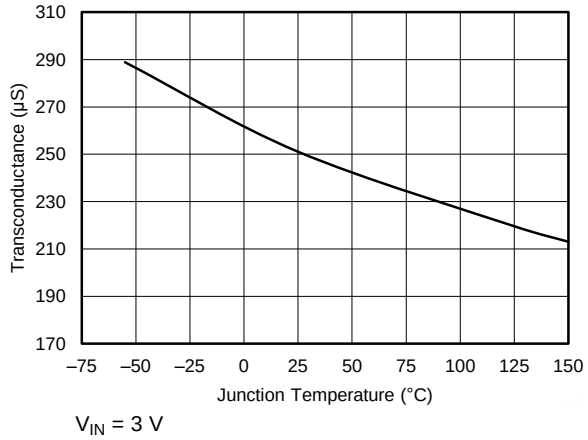


Figure 8. Transconductance vs Temperature

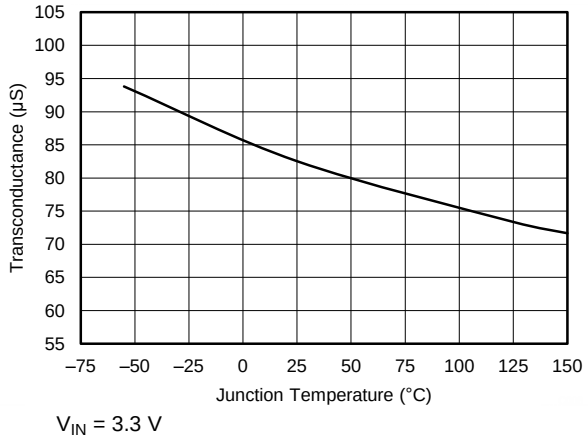


Figure 9. Transconductance (Slow Start) vs Junction Temperature

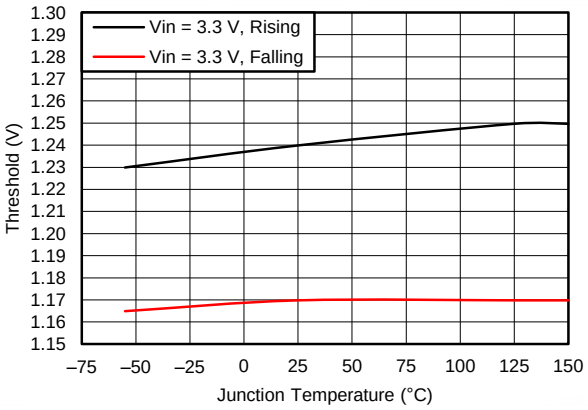


Figure 10. EN Pin Voltage vs Temperature

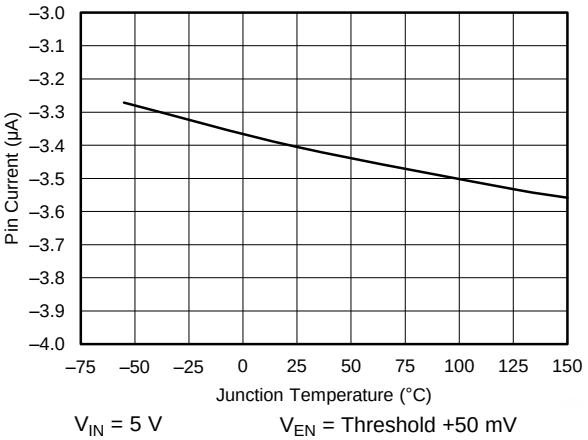


Figure 11. EN Pin Current vs Temperature

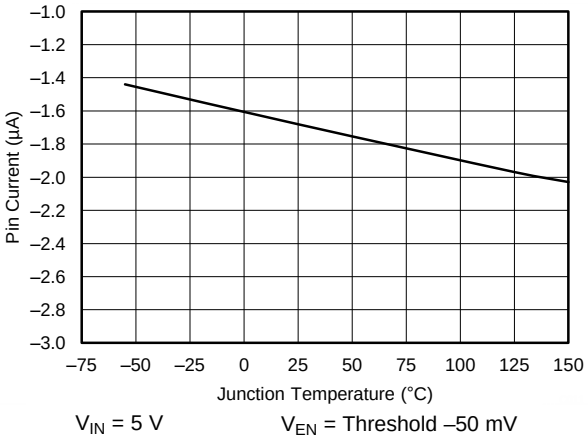


Figure 12. EN Pin Current vs Temperature

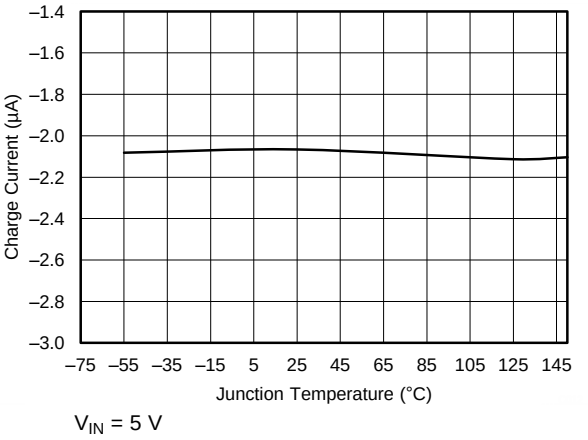


Figure 13. Charge Current vs Temperature

Typical Characteristics (continued)

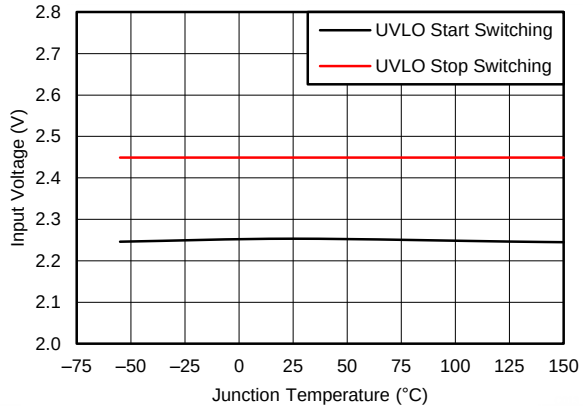


Figure 14. Input Voltage vs Temperature

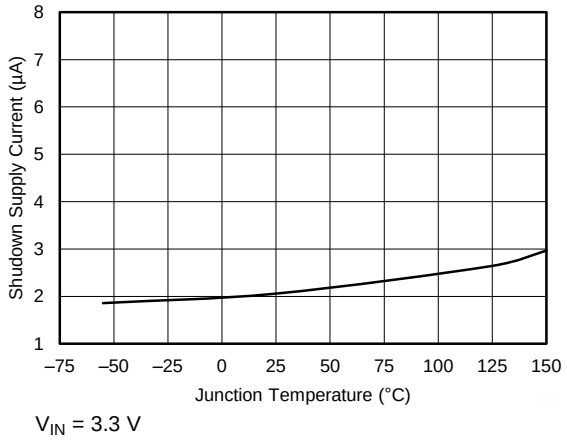


Figure 15. Shutdown Supply Current vs Temperature

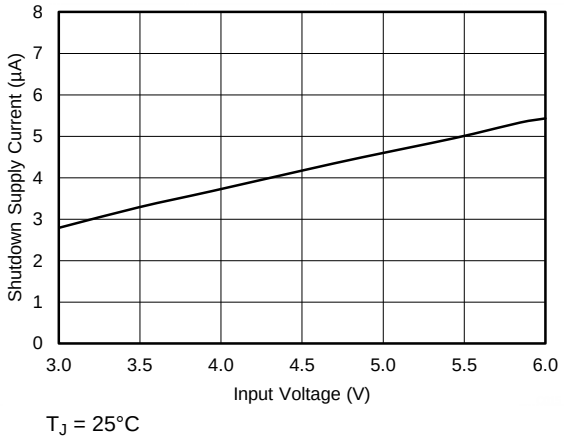


Figure 16. Shutdown Supply Current vs Input Voltage

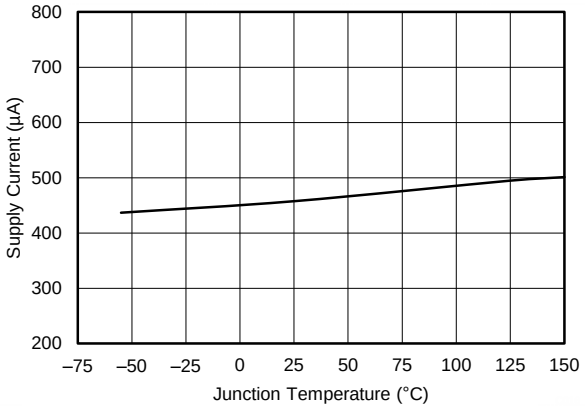


Figure 17. VIN Supply Current vs Junction Temperature

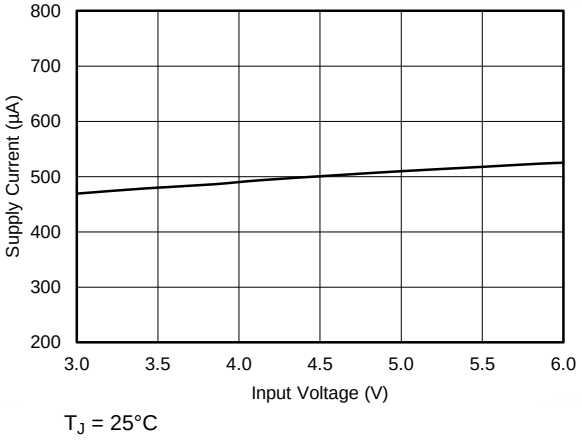


Figure 18. VIN Supply Current vs Input Voltage

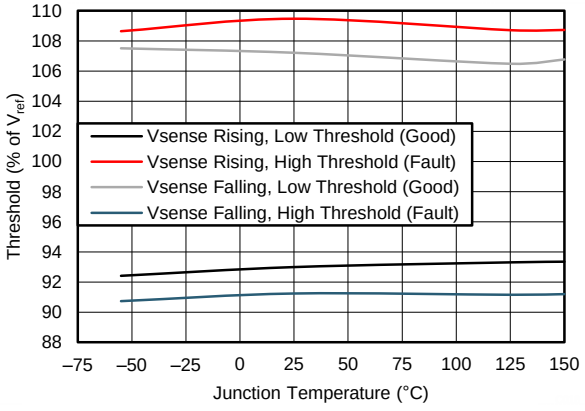


Figure 19. PWRGD Threshold vs Temperature

Typical Characteristics (continued)

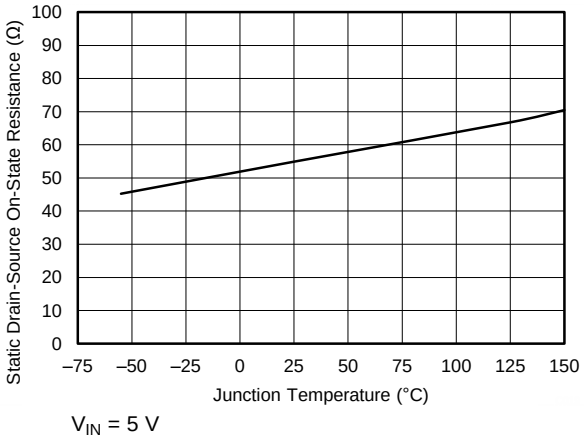


Figure 20. PWRGD On-Resistance vs Temperature

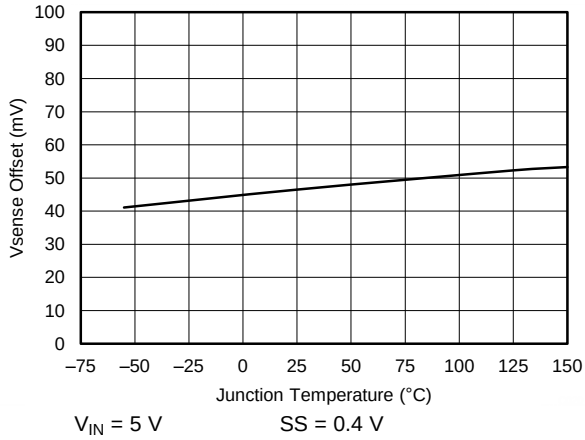


Figure 21. SS/TR to VSENSE Offset vs Temperature

9 Detailed Description

9.1 Overview

The TPS57114-EP is a 6-V, 3.5-A, synchronous step-down (buck) converter with two integrated N-channel MOSFETs. To improve performance during line and load transients, the device implements a constant-frequency, peak-current mode control which reduces output capacitance and simplifies external frequency-compensation design. The wide switching-frequency range of 200 to 2000 kHz allows for efficiency and size optimization when selecting the output-filter components. Adjust the switching frequency using a resistor to ground on the RT/CLK pin. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that synchronizes the power-switch turn-on to the falling edge of an external system clock.

The TPS57114-EP has a typical default start-up voltage of 2.45 V. The EN pin has an internal pullup current source; to adjust the input-voltage UVLO, use two external resistors on the EN pin. In addition, the pullup current provides a default condition, allowing the device to operate when the EN pin is floating. The total operating current for the TPS57114-EP is typically 515 µA when not switching and under no load. When the device is disabled, the supply current is less than 5.5 µA.

The integrated 12-mΩ MOSFETs allow for high-efficiency power-supply designs with continuous output currents up to 3.5 A.

The TPS57114-EP reduces the external component count by integrating the boot recharge diode. A capacitor between the BOOT and PH pins supplies the bias voltage for the integrated high-side MOSFET. A UVLO circuit, which monitors the boot-capacitor voltage, turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS57114-EP to operate approaching 100% duty cycle. The output voltage can be stepped down to as low as the 0.8-V reference.

The TPS57114-EP has a power-good comparator (PWRGD) with 2% hysteresis.

The TPS57114-EP minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. The regulated output voltage exceeding 109% of the nominal voltage activates the overvoltage comparator, which turns off the high-side MOSFET and masks it from turning on until the output voltage is lower than 107% of the nominal voltage.

The SS/TR (slow-start or tracking) pin minimizes inrush currents or provides power-supply sequencing during power-up. Connect a small-value capacitor to the pin for slow start. Discharging the SS/TR pin before the output powers up ensures a repeatable restart after an overtemperature fault, UVLO fault, or disabled condition.

The use of a frequency-foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help limit the inductor current.

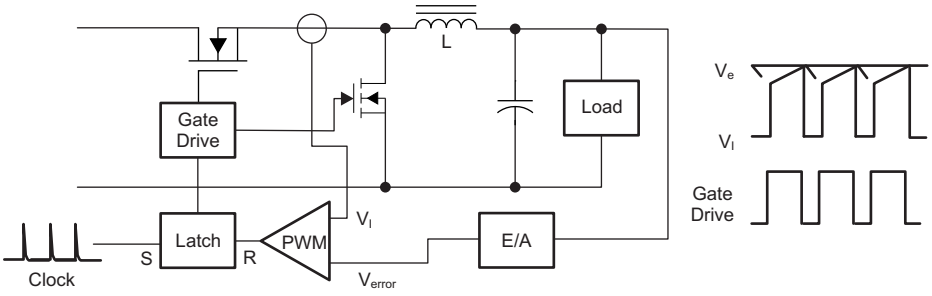
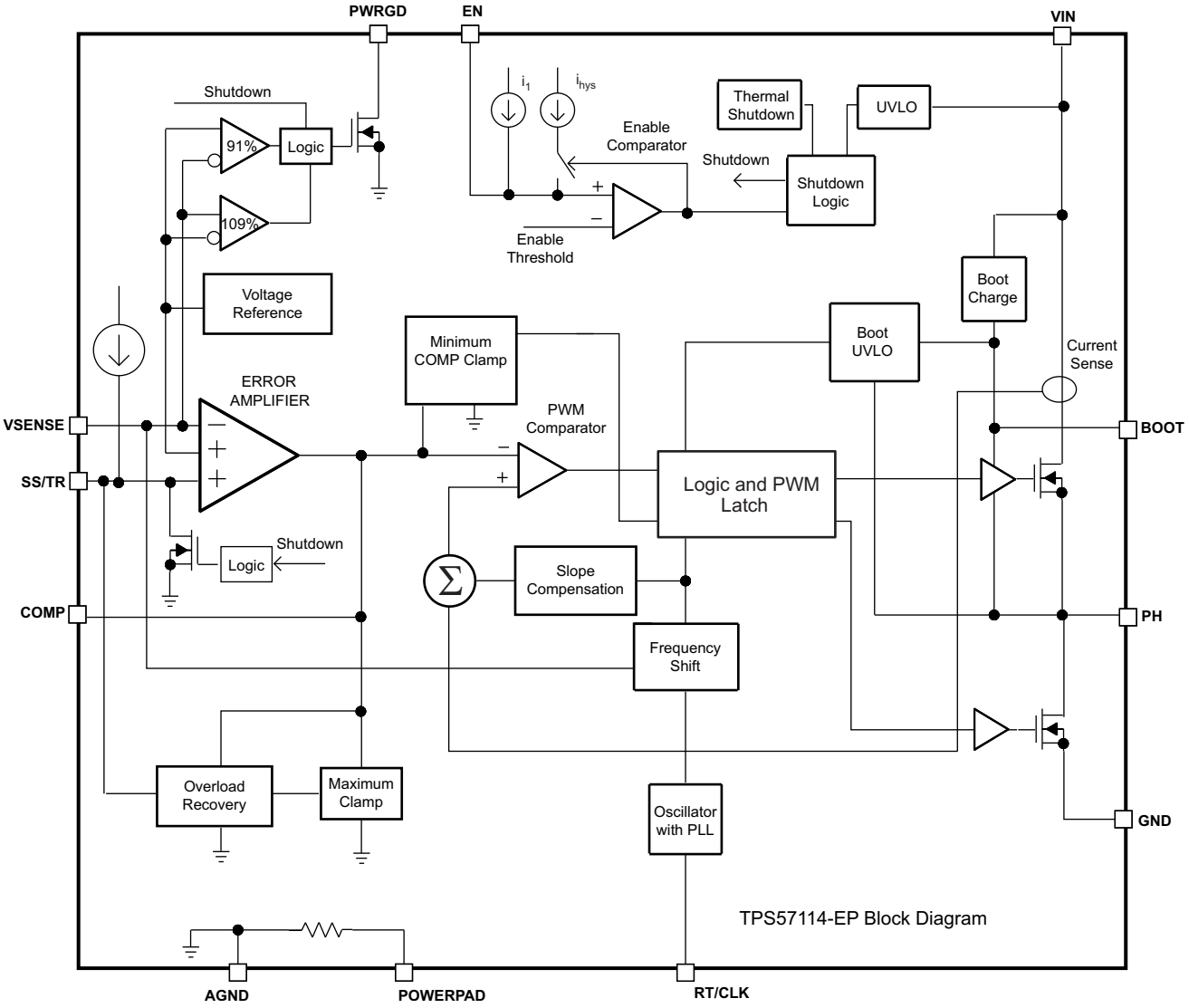


Figure 22. Peak Current Mode Control (See Application Note U-140)

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fixed-Frequency Pwm Control

The TPS57114-EP uses an adjustable fixed-frequency peak-current mode control. An error amplifier, which drives the COMP pin, compares the output voltage through external resistors on the VSENSE pin to an internal voltage reference. An internal oscillator initiates the turn-on of the high-side power switch. The device compares the error-amplifier output to the high-side power-switch current. When the power-switch current reaches the COMP voltage level, the high-side power switch turns off and the low-side power switch turns on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level, and also implements a minimum clamp for improved transient-response performance.

9.3.2 Slope Compensation and Output Current

The TPS57114-EP adds a compensating ramp to the switch-current signal. This slope compensation prevents subharmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

Feature Description (continued)

9.3.3 Bootstrap Voltage (Boot) and Low-Dropout Operation

The TPS57114-EP has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve dropout, the design of the TPS57114-EP is for operation at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.2 V. A UVLO circuit turns off the high-side MOSFET, allowing for the low-side MOSFET to conduct when the voltage from BOOT to PH drops below 2.2 V. Because the supply current sourced from the BOOT pin is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor; thus, the effective duty cycle of the switching regulator is high.

9.3.4 Error Amplifier

The TPS57114-EP has a transconductance amplifier which it uses as an error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance of the error amplifier is 245 µS during normal operation. When the voltage of the VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the gm is typically greater than 79 µS, but less than 245 µS.

9.3.5 Voltage Reference

The voltage-reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature-stable band-gap circuit. The band-gap and scaling circuits produce 0.8 V at the non-inverting input of the error amplifier.

9.3.6 Adjusting the Output Voltage

A resistor divider from the output node to the VSENSE pin sets the output voltage. TI recommends using divider resistors with 1% tolerance or better. Start with 100 kΩ for the R1 resistor and use Equation 1 to calculate R2. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.799\ V}{V_O - 0.799\ V} \right) \quad (1)$$

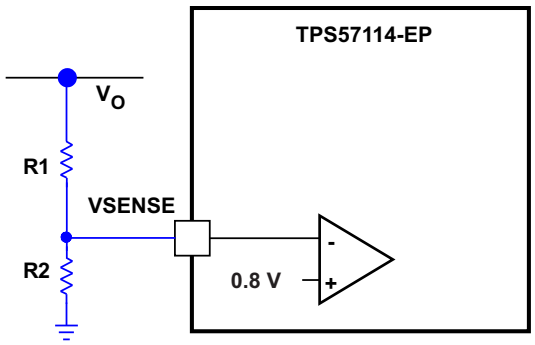


Figure 23. Voltage-Divider Circuit

Feature Description (continued)

9.3.7 Enable Functionality and Adjusting UVLO

The VIN pin voltage falling below 2.6 V disables the TPS57114-EP. If an application requires a higher UVLO, use the EN pin as shown in Figure 24 to adjust the input voltage UVLO by connecting two external resistors. TI recommends using the EN resistors to set the UVLO falling threshold (V_{STOP}) above 2.6 V. Set the rising threshold (V_{START}) to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pullup current source that provides the default condition of the TPS57114-EP operating when the EN pin floats. When the EN pin voltage exceeds 1.25 V, the circuitry adds an additional 1.6 µA of hysteresis. Pulling the EN pin below 1.18 V removes the 1.6 µA. This additional current facilitates input voltage hysteresis.

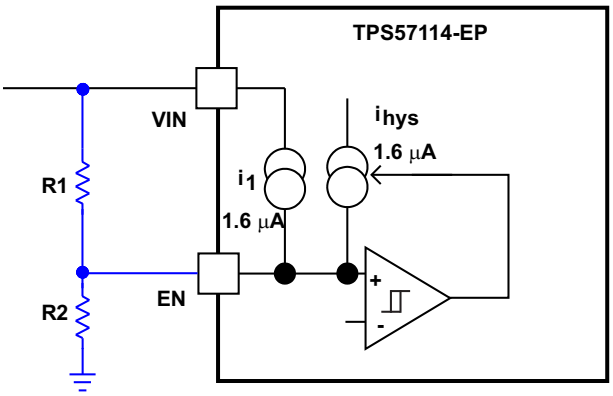


Figure 24. Adjustable UVLO

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_1\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_{hys}} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_1 + I_{hys})} \quad (3)$$

where

- I_{hys} = 1.6 µA
- I_1 = 1.6 µA
- $V_{ENRISING}$ = 1.25 V
- $V_{ENFALLING}$ = 1.18 V

9.3.8 Slow-Start or Tracking Pin

The TPS57114-EP regulates to the lower of the SS/TR pin and the internal reference voltage. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS57114-EP has an internal pullup current source of 2 µA which charges the external slow-start capacitor. Equation 4 calculates the required slow-start capacitor value.

$$Css(nF) = \frac{Tss(mS) \times Iss(\mu A)}{Vref(V)} \quad (4)$$

where

- Tss is the desired slow-start time in ms
- Iss is the internal slow-start charging current of 2 µA
- Vref is the internal voltage reference of 0.8 V

Feature Description (continued)

If during normal operation VIN goes below UVLO, the EN pin goes below 1.2 V, or a thermal shutdown event occurs, the TPS57114-EP stops switching. Upon VIN going above UVLO, the release or pulling high of EN, or the exit of a thermal shutdown, SS/TR discharges to below 60 mV before reinitiating a powering-up sequence. The VSENSE voltage follows the SS/TR pin voltage with a 54-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference.

9.3.9 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS57114-EP is adjustable over a wide range from 300 to 2000 kHz by placing a maximum of 700 kΩ or minimum of 85 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in Figure 6 or Equation 5.

$$RT\left(k\Omega\right) = \frac{235892}{f_{SW}\left(kHz\right)^{1.027}} \tag{5}$$

$$f_{SW}\left(kHz\right) = \frac{171032}{RT\left(k\Omega\right)^{0.974}} \tag{6}$$

To reduce the solution size, one would typically set the switching frequency as high as possible, but consider tradeoffs of the efficiency, maximum input voltage, and minimum controllable on-time.

The minimum controllable on-time is typically 65 ns at full-current load and 120 ns at no load and limits the maximum operating input voltage or output voltage.

9.3.10 Overcurrent Protection

The TPS57114-EP implements a cycle-by-cycle current limit. During each switching cycle, the device compares the high-side switch current to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. There is an internal clamp on the error-amplifier output. This clamp functions as a switch-current limit.

9.3.11 Frequency Shift

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS57114-EP implements a frequency shift. Without this frequency shift, during an overcurrent condition the low-side MOSFET may not turn off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, during an overcurrent condition there is a switching frequency reduction from 100% to 50%, then 25%, as the voltage decreases from 0.8 to 0 V on the VSENSE pin, to allow the low-side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 to 0.8 V. See Figure 7 for details.

9.3.12 Reverse Overcurrent Protection

The TPS57114-EP implements low-side current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 4.5 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into prebiased outputs.

Feature Description (continued)

9.3.13 Synchronize Using the RT/CLK Pin

The RT/CLK pin synchronizes the converter to an external system clock (see Figure 25). To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on-time of at least 75 ns. If the pin goes above the PLL upper threshold, a mode change occurs, and the pin becomes a synchronization input. The device disables the internal amplifier, and the pin is a high-impedance clock input to the internal PLL. If clocking edges stop, the device re-enables the internal amplifier and the mode returns to the frequency set by the resistor. The square-wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V, typically. The synchronization frequency range is 300 to 2000 kHz. The rising edge of PH synchronizes to the falling edge of the RT/CLK pin.

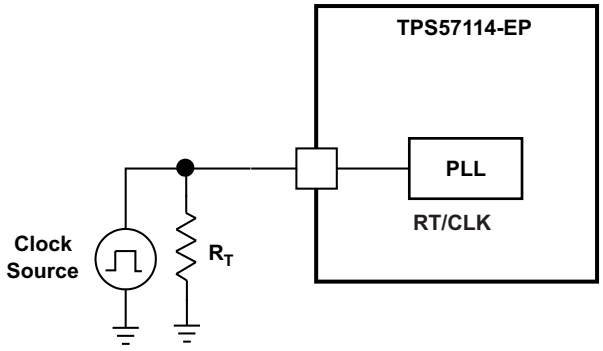


Figure 25. Synchronizing to a System Clock

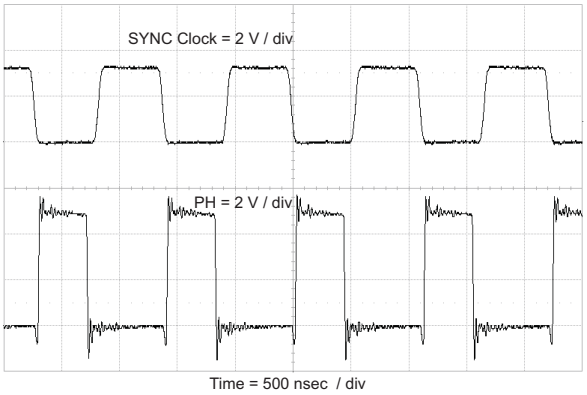


Figure 26. Plot of Synchronizing to System Clock

9.3.14 Power Good (PWRGD Pin)

The PWRGD pin output is an open-drain MOSFET. The output goes low when the VSENSE voltage enters the fault condition by falling below 91% or rising above 109% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 107% of the internal voltage reference, the PWRGD output MOSFET turns off. TI recommends to use a pullup resistor between 1 to 100 kΩ with a voltage source that is 6 V or less. PWRGD is in a valid state after the VIN input voltage is greater than 1.1 V.

9.3.15 Overvoltage Transient Protection (OVTP)

The TPS57114-EP incorporates an OVTP circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold, which is 109% of the internal voltage reference. The VSENSE pin voltage going greater than the OVTP threshold disables the high-side MOSFET, preventing current from flowing to the output and minimizing output overshoot. The VSENSE voltage dropping lower than the OVTP threshold allows the high-side MOSFET to turn on during the next clock cycle.

9.3.16 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 168°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the die temperature decreases below 148°C, the device reinitiates the power-up sequence by discharging the SS pin to below 60 mV. The thermal shutdown hysteresis is 20°C.

Feature Description (continued)

9.3.17 Small-Signal Model for Loop Response

Figure 27 shows an equivalent model for the TPS57114-EP control loop which the user can model in a circuit-simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm of 245 µS. The user can use an ideal voltage-controlled current source to model the error amplifier. Resistor R0 and capacitor C0 model the open-loop gain and frequency response of the amplifier. The 1-mV AC voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting a or c versus frequency shows the small-signal response of the frequency compensation. Plotting a or b versus frequency shows the small-signal response of the overall loop. The user can check the dynamic loop response by replacing R_L with a current source having the appropriate load-step amplitude and step rate in a time domain analysis.

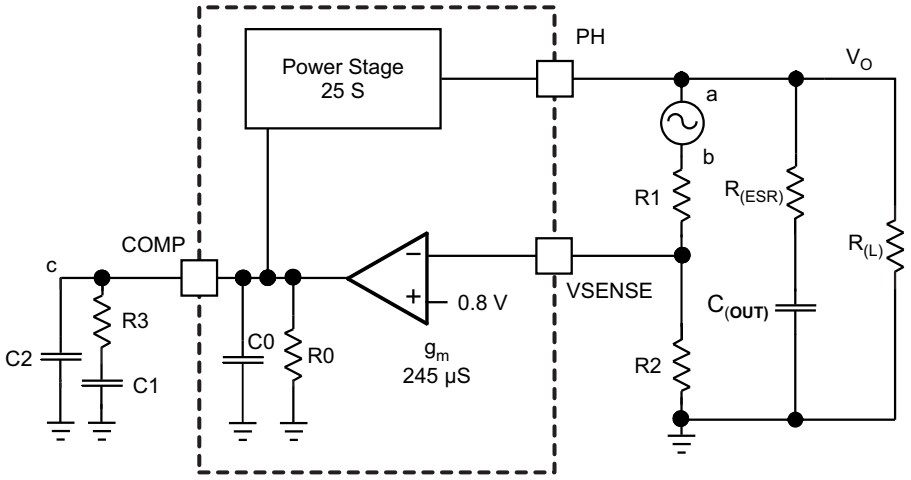


Figure 27. Small-Signal Model for Loop Response

9.3.18 Simple Small-Signal Model for Peak-Current Mode Control

Figure 27 is a simple small-signal model that the user can use to understand how to design the frequency compensation. An approximation of a voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor can approximate the TPS57114-EP power stage. The control-to-output transfer function, shown in Equation 7, consists of a DC gain, one dominant pole, and one ESR zero. The quotient of the change in switch current divided by the change in COMP pin voltage (node c in Figure 27) is the power-stage transconductance. The gm for the TPS57114-EP is 25 S. The low-frequency gain of the power-stage frequency response is the product of the transconductance and the load resistance, as shown in Equation 8. As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current (see Equation 9). The dashed line in the right half of Figure 28 highlights the combined effect. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation.

Feature Description (continued)

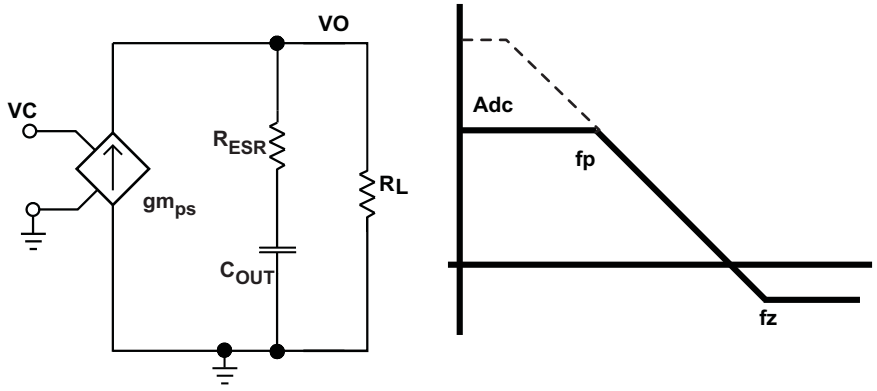


Figure 28. Simple Small-Signal Model and Frequency Response for Peak-Current Mode Control

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (7)$$

$$Adc = gm_{ps} \times R_L \quad (8)$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (9)$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (10)$$

9.3.19 Small-Signal Model for Frequency Compensation

The TPS57114-EP uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency-compensation circuits. Figure 29 shows the compensation circuits. High-bandwidth power-supply designs most likely implement Type 2 circuits using low-ESR output capacitors. In Type 2A, inclusion of one additional high-frequency pole attenuates high-frequency noise.

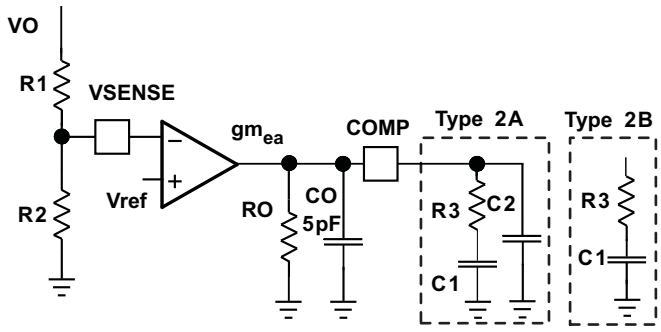


Figure 29. Types of Frequency Compensation

Feature Description (continued)

The design guidelines for TPS57114-EP loop compensation are as follows:

1. Calculate the modulator pole, $f$pmod, and the ESR zero, fz1, using Equation 11 and Equation 12. If the output voltage is a high percentage of the capacitor rating, it may be necessary to derate the output capacitor (C_{OUT}). Use the manufacturer information for the capacitor to derate the capacitor value. Use Equation 13 and Equation 14 to estimate a starting point for the crossover frequency, fc. Equation 13 is the geometric mean of the modulator pole and the ESR zero and Equation 14 is the mean of the modulator pole and the switching frequency. Use the lower value of Equation 13 or Equation 14 as the maximum crossover frequency.

$$f\text{p mod} = \frac{\text{Ioutmax}}{2\pi \times \text{Vout} \times \text{Cout}} \tag{11}$$

$$f\text{z mod} = \frac{1}{2\pi \times \text{Resr} \times \text{Cout}} \tag{12}$$

$$f_C = \sqrt{f\text{p mod} \times f\text{z mod}} \tag{13}$$

$$f_C = \sqrt{f\text{p mod} \times \frac{f\text{sw}}{2}} \tag{14}$$

2. Determine R3 with:

$$\text{R3} = \frac{2\pi \times f\text{c} \times \text{Vo} \times C_{OUT}}{gm_{ea} \times \text{Vref} \times gm_{ps}}$$

where

- gm_{ea} is the amplifier gain (245 µS)
- gm_{ps} is the power stage gain (25 S)

(15)

3. Place a compensation zero at the dominant pole $f\text{p} = \frac{1}{C_{OUT} \times R_L \times 2\pi}$. Determine C1 with:

$$\text{C1} = \frac{R_L \times C_{OUT}}{\text{R3}} \tag{16}$$

4. C2 is optional. Use it, if necessary, to cancel the 0 from the ESR of C_{OUT}.

$$\text{C2} = \frac{\text{Resr} \times C_{OUT}}{\text{R3}} \tag{17}$$

9.4 Device Functional Modes

9.4.1 RT (Resistor Timing) Mode

External resistor to ground can be connected to the RT/CLK pin, which enables the user to adjust the switching frequency. The device has an internal PLL on the RT/CLK pin that synchronizes the power-switch turn on to the falling edge of an external system clock. The frequency is adjustable from 200 to 2000 kHz by using external resistor maximum of 700 kΩ or minimum of 85 kΩ (see *Constant Switching Frequency and Timing Resistor (RT/CLK Pin)*).

Device Functional Modes (continued)

9.4.2 CLK (External Clock) Mode

The RT/CLK pin synchronizes the converter to an external system clock. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on-time of at least 75 ns. If the pin goes above the PLL upper threshold, a mode change occurs, and the pin becomes a synchronization input. The device disables the internal amplifier and the terminal is a high-impedance clock input to the internal PLL. If clocking edges stop, the device re-enables the internal amplifier and the mode returns to the frequency set by the resistor. The square-wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V, typically. The synchronization frequency range is 300 to 2000 kHz. The rising edge of PH synchronizes to the falling edge of the RT/CLK pin.

10 Application and Implementation

10.1 Application Information

10.1.1 Sequencing

The user can implement many of the common power-supply sequencing methods using the SS/TR, EN, and PWRGD pins. Implement the sequential method by using an open-drain or collector output of the power-on-reset pin of another device. Figure 30 shows the sequential method. Coupling power-good to the EN pin on the TPS57114-EP enables the second power supply after the primary supply reaches regulation.

The user can accomplish ratiometric start-up by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, double the pullup current source in Equation 4. Figure 32 shows the ratiometric method.

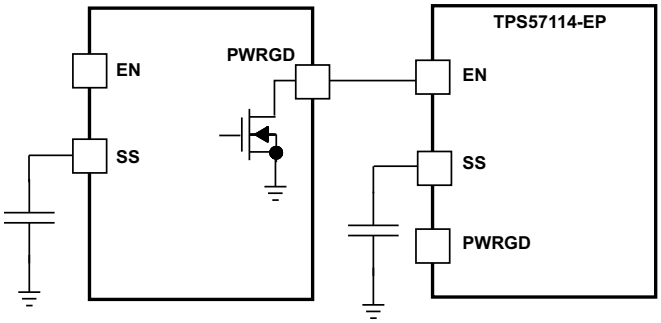


Figure 30. Sequential Start-Up Sequence

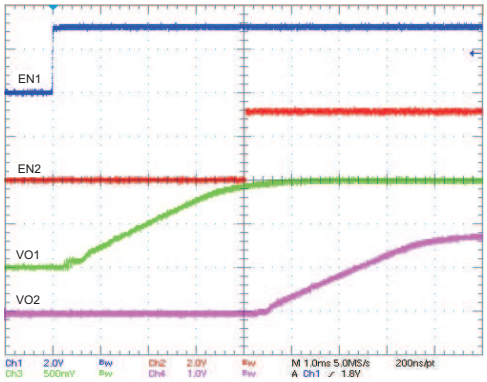


Figure 31. Sequential Start-Up Using EN and PWRGD

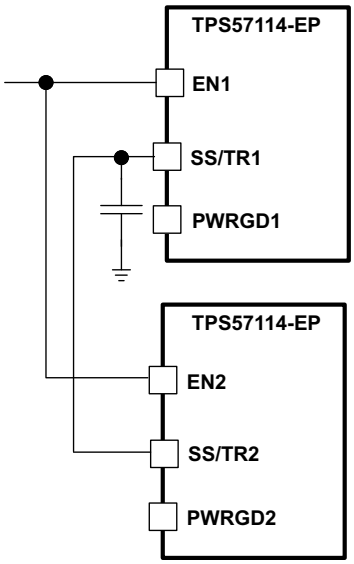


Figure 32. Schematic for Ratiometric Start-Up Sequence

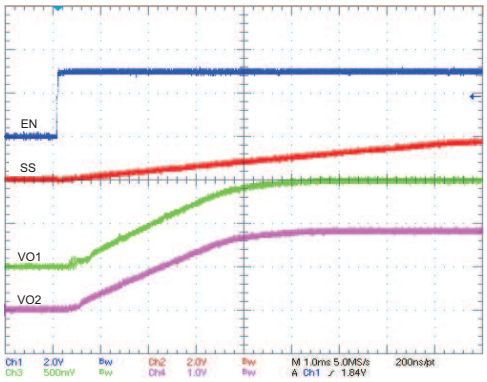


Figure 33. Ratiometric Start-Up With Vout1 Leading Vout2

Application Information (continued)

The user can implement ratiometric and simultaneous power-supply sequencing by connecting the resistor network of R1 and R2 shown in Figure 34 to the output of the power supply that requires tracking, or to another voltage reference source. Using Equation 18 and Equation 19 allows calculation of the tracking resistors to initiate the Vout2 slightly before, after, or at the same time as Vout1. Equation 20 is the voltage difference between Vout1 and Vout2. The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR-to-VSENSE offset (Vssoffset) in the slow-start circuit and the offset created by the pullup current source (Iss) and tracking resistors, the equations include Vssoffset and Iss as variables. To design a ratiometric start-up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 18 through Equation 20 for ΔV. Equation 20 results in a positive number for applications in which Vout2 is slightly lower than Vout1 when achieving Vout2 regulation. The requirement to pull the SS/TR pin below 60 mV before starting after an EN, UVLO, or thermal shutdown fault necessitates careful selection of the tracking resistors to ensure the device can restart after a fault. Make sure the calculated R1 value from Equation 18 is greater than the value calculated in Equation 21 to ensure the device can recover from a fault. As the SS/TR voltage becomes more than 85% of the nominal reference voltage, Vssoffset becomes larger as the slow-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.1 V for a complete handoff to the internal voltage reference, as shown in Figure 33.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \tag{18}$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \tag{19}$$

$$\Delta V = Vout1 - Vout2 \tag{20}$$

$$R1 > 2930 \times Vout1 - 145 \times \Delta V \tag{21}$$

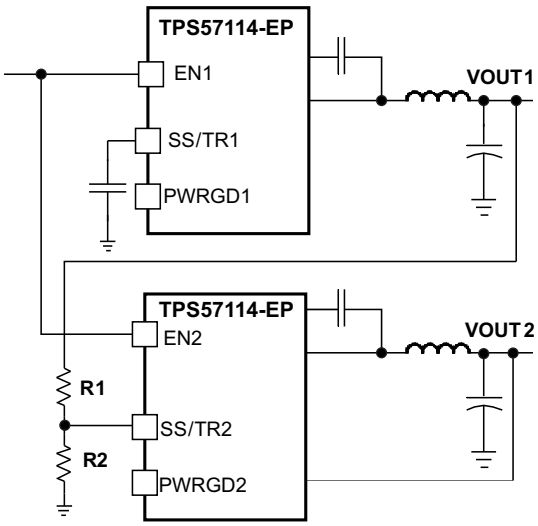


Figure 34. Ratiometric and Simultaneous Start-Up Sequence

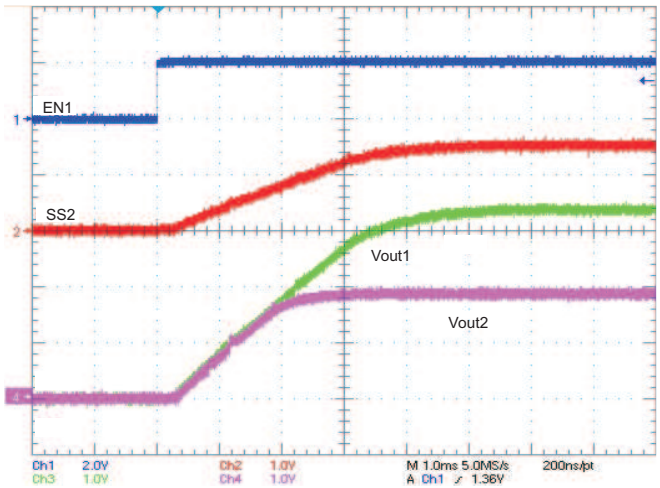


Figure 35. Ratiometric Start-Up Using Coupled SS/TR Pins

10.2 Typical Application

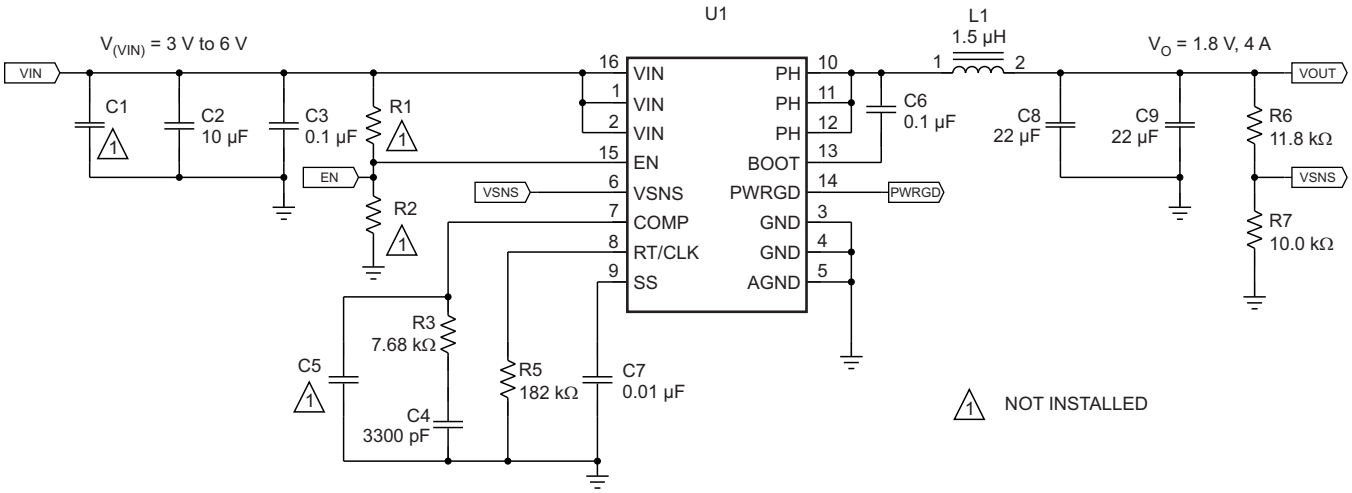


Figure 36. High-Frequency, 1.8-V Output Power-Supply Design With Adjusted UVLO

10.2.1 Design Requirements

This example details the design of a high-frequency switching regulator using ceramic output capacitors. This design is available as the HPA375 evaluation module (EVM). To start the design process, it is necessary to know a few parameters. Determination of these parameters typically occurs at the system level. For this example, start with the following known parameters:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	1.8 V
Transient response, 1- to 2-A load step	ΔVout = 5%
Maximum output current	3.5 A
Input voltage	5 V nominal, 3 to 5 V
Output-voltage ripple	<30 mVp-p
Switching frequency (f_{SW})	1000 kHz

10.2.2 Detailed Design Procedure

10.2.2.1 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user wants to choose the highest switching frequency possible, because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the performance of the converter. The converter is capable of running from 300 kHz to 2 MHz. Unless a small solution size is the ultimate goal, select a moderate switching frequency of 1 MHz to achieve both a small solution size and high-efficiency operation. Using Equation 5, calculate R5 to be 180 kΩ. Choose a standard 1% 182-kΩ value for the design.

10.2.2.2 Output Inductor Selection

The inductor selected works for the entire TPS57114-EP input-voltage range. To calculate the value of the output inductor, use Equation 22. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use K_{IND} = 0.3, which results in a calculated inductor value of 1.36 µH. For this design, choose the nearest standard value: 1.5 µH. For the output-filter inductor, it is important not to exceed the rms-current and saturation-current ratings. Find the rms and peak inductor current using Equation 24 and Equation 25.

For this design, the rms inductor current is 4 A and the peak inductor current is 4.6 A. The chosen inductor is a Coilcraft XLA4020-152ME_ or equivalent. It has a saturation current rating of 9.6 A and an rms current rating of 7.5 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor-current level calculated previously. In transient conditions, the inductor current can increase up to the switch-current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch-current limit rather than the peak inductor current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \tag{22}$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \tag{23}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \tag{24}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{25}$$

10.2.2.3 Output Capacitor

To select the value of the output capacitor, use three primary considerations. The output capacitor determines the modulator pole, the output-voltage ripple, and how the regulator responds to a large change in load current. Base the output-capacitance selection on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after removal of the input power. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load, such as transitioning from no load to a full load. The regulator usually requires two or more clock cycles for the control loop to detect the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor size must be capable of supplying the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 26 shows the minimum output capacitance necessary to accomplish this.

For this example, the transient load response is specified as a 5% change in Vout for a load step from 0 A (no load) to 1.5 A (50% load). For this example, ΔIout = 1.5 – 0 = 1.5 A and ΔVout= 0.05 × 1.8 = 0.09 V. Using these numbers gives a minimum capacitance of 33 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 27 calculates the minimum output capacitance needed to meet the output-voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 27 yields 2.3 µF.

$$Co > \frac{2 \times \Delta Iout}{fsw \times \Delta Vout}$$

where

- ΔIout is the change in output current
- $f$sw is the regulator switching frequency
- ΔVout is the allowable change in the output voltage

(26)

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}}$$

where

- $f$sw is the switching frequency
- Voripple is the maximum allowable output-voltage ripple
- Iripple is the inductor ripple current

(27)

Equation 28 calculates the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 28 indicates the ESR should be less than 55 mΩ. In this case, the ESR of the ceramic capacitor is much less than 55 mΩ.

Factoring in additional capacitance deratings for aging, temperature, and DC bias increases this minimum value. This example uses two 22-µF, 10-V X5R ceramic capacitors with 3 mΩ of ESR.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root-mean-square (rms) value of the maximum ripple current. Use Equation 29 to calculate the rms ripple current that the output capacitor must support. For this application, Equation 29 yields 333 mA.

$$Resr < \frac{Voripple}{Iripple} \quad (28)$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \quad (29)$$

10.2.2.4 Input Capacitor

The TPS57114-EP requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor with at least 4.7 µF of effective capacitance, and in some applications a bulk capacitance. The effective capacitance includes any DC-bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS57114-EP. Calculate the input ripple current using Equation 30.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. The dielectrics are usually selected for power regulator capacitors are X5R and X7R ceramic because they have a high capacitance-to-volume ratio and are fairly stable over temperature. Also select the output capacitor with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

This design example requires a ceramic capacitor with at least a 10-V voltage rating to support the maximum input voltage. The selections for this example are one 10-µF and one 0.1-µF 10-V capacitor in parallel. The input capacitance value determines the input ripple voltage of the regulator. Calculate the input voltage ripple using Equation 31. Using the design example values, Ioutmax = 4 A, Cin = 10 µF, and $f$sw = 1 MHz, yields an input-voltage ripple of 100 mV and an rms input-ripple current of 1.96 A.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \quad (30)$$

$$\Delta Vin = \frac{Ioutmax \times 0.25}{Cin \times fsw} \quad (31)$$

10.2.2.5 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. Slow start is useful if a load requires a controlled rate of voltage slew. Slow start is also used if the output capacitance is large and would require large amounts of current to charge the capacitor quickly to the output-voltage level. The large currents necessary to charge the capacitor may make the TPS57114-EP reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

Calculate the slow-start capacitor value using Equation 32. For the example circuit, the slow-start time is not too critical because the output capacitor value is 44 µF, which does not require much current to charge to 1.8 V. The example circuit has the slow-start time set to an arbitrary value of 4 ms, which requires a 10-nF capacitor. In TPS57114-EP, Iss is 2.2 µA and Vref is 0.8 V.

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \tag{32}$$

10.2.2.6 Bootstrap Capacitor Selection

Connect a 0.1-µF ceramic capacitor between the BOOT and PH pins for proper operation. TI recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 10-V, or higher, voltage rating.

10.2.2.7 Output-Voltage and Feedback-Resistor Selection

For the design example, the selection for R6 is 100 kΩ. Using Equation 33, calculate R7 as 80 kΩ. The nearest standard 1% resistor is 80.5 kΩ.

$$R7 = \frac{Vref}{Vo - Vref} R6 \tag{33}$$

Due to the internal design of the TPS57114-EP, a minimum output voltage limit exists for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, an output voltage limit may exist due to the minimum controllable on-time. In this case, Equation 34 gives the minimum output voltage.

$$Voutmin = Ontimemin \times Fsmax \times (Vinmax - Ioutmin \times 2 \times RDS) - Ioutmin \times (RL + RDS) \tag{34}$$

where

- Voutmin = Minimum achievable output voltage
- Ontimemin = Minimum controllable on-time (65 ns, typical; 120 ns, no load)
- Fsmax = Maximum switching frequency, including tolerance
- Vinmax = Maximum input voltage
- Ioutmin = Minimum load current
- RDS = Minimum high-side MOSFET on-resistance (15 to 19 mΩ)
- RL = Series resistance of output inductor

There is also a maximum achievable output voltage, which is limited by the minimum off-time. Equation 35 gives the maximum output voltage

$$Voutmax = (1 - Offtimemax \times Fsmax) \times (Vinmin - Ioutmax \times 2 \times RDS) - Ioutmax \times (RL + RDS) \tag{35}$$

where

- Voutmax = Maximum achievable output voltage
- Offtimeman = Maximum off-time (60 ns, typical)
- Fsmax = Maximum switching frequency, including tolerance
- Vinmin = Minimum input voltage
- Ioutmax = Maximum load current
- RDS = Maximum high-side MOSFET on-resistance (19 to 30 mΩ)
- RL = Series resistance of output inductor

10.2.2.8 Compensation

Several industry techniques are used to compensate DC-DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. The method presented here ignores the effects of the slope compensation that is internal to the TPS57114-EP. Because of ignoring the slope compensation, the actual crossover frequency is usually lower than the crossover frequency used in the calculations. Use SwitcherPro software for a more-accurate design.

To get started, calculate the modulator pole, $f$pmod, and the ESR zero, fz1, using Equation 36 and Equation 37. For Cout, derating the capacitor is not necessary, as the 1.8-V output is a small percentage of the 10-V capacitor rating. If the output is a high percentage of the capacitor rating, use the manufacturer information for the capacitor to derate the capacitor value. Use Equation 38 and Equation 39 to estimate a starting point for the crossover frequency, fc. For the example design, $f$pmod is 6.03 kHz and $f$zmod is 1210 kHz. Equation 38 is the geometric mean of the modulator pole and the ESR zero, and Equation 39 is the mean of the modulator pole and the switching frequency. Equation 38 yields 85.3 kHz and Equation 39 gives 54.9 kHz. Use the lower value of Equation 38 or Equation 39 as the approximate crossover frequency. For this example, fc is 56 kHz. Next, calculate the compensation components. Use a resistor in series with a capacitor to create a compensating zero. A capacitor in parallel with these two components forms the compensating pole (if needed).

$$f\text{p mod} = \frac{\text{Ioutmax}}{2\pi \times \text{Vout} \times \text{Cout}} \tag{36}$$

$$f\text{z mod} = \frac{1}{2\pi \times \text{Resr} \times \text{Cout}} \tag{37}$$

$$f_C = \sqrt{f\text{p mod} \times f\text{z mod}} \tag{38}$$

$$f_C = \sqrt{f\text{p mod} \times \frac{f\text{sw}}{2}} \tag{39}$$

The compensation design takes the following steps:

1. Set up the anticipated crossover frequency. Use Equation 40 to calculate the resistor value for the compensation network. In this example, the anticipated crossover frequency (fc) is 56 kHz. The power-stage gain (gm_{ps}) is 25 S, and the error-amplifier gain (gm_{ea}) is 245 µS.

$$\text{R3} = \frac{2\pi \times f\text{c} \times \text{Vo} \times \text{Co}}{\text{Gm} \times \text{Vref} \times \text{VI}_{gm}} \tag{40}$$

2. Place compensation zero at the pole formed by the load resistor and the output capacitor. Calculate the capacitor for the compensation network using Equation 41.

$$\text{C3} = \frac{\text{Ro} \times \text{Co}}{\text{R3}} \tag{41}$$

3. The user can add an additional pole to attenuate high-frequency noise. In this application, it is not necessary to add it.

From the preceding procedure, the compensation network includes a 7.68-kΩ resistor and a 3300-pF capacitor.

10.2.2.9 Power-Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous-conduction mode (CCM) operation. The power dissipation of the IC (Ptot) includes conduction loss (Pcon), dead-time loss (Pd), switching loss (Psw), gate-drive loss (Pgd), and supply-current loss (Pq).

$$\text{Pcon} = \text{Io}^2 \times r_{DS(on)\_Temp} \tag{42}$$

$$\text{Pd} = f_{sw} \times \text{Io} \times 0.7 \times 60 \times 10^{-9} \tag{43}$$

$$\text{Psw} = 1 / 2 \times V_{in} \times \text{Io} \times f_{sw} \times 8 \times 10^{-9} \tag{44}$$

$$\text{Pgd} = 2 \times V_{in} \times f_{sw} \times 2 \times 10^{-9} \tag{45}$$

$$\text{Pq} = V_{in} \times 515 \times 10^{-6} \tag{46}$$

where:

- I_O is the output current (A)
- $r_{DS(on)\_Temp}$ is the on-resistance of the high-side MOSFET at a given temperature (Ω)
- V_{in} is the input voltage (V)
- f_{sw} is the switching frequency (Hz)

So

$$Ptot = Pcon + Pd + Psw + Pgd + Pq \quad (47)$$

For a given T_A,

$$T_J = T_A + Rth \times Ptot \quad (48)$$

For a given T_JMAX = 150°C,

$$T_A MAX = T_J MAX - Rth \times Ptot \quad (49)$$

where:

- Ptot is the total device power dissipation (W)
- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- Rth is the thermal resistance of the package (°C/W)
- T_JMAX is maximum junction temperature (°C)
- T_AMAX is maximum ambient temperature (°C)

Additional power losses in the regulator circuit occur due to the inductor ac and dc losses and trace resistance that impact the overall efficiency of the regulator.

10.2.3 Application Curves

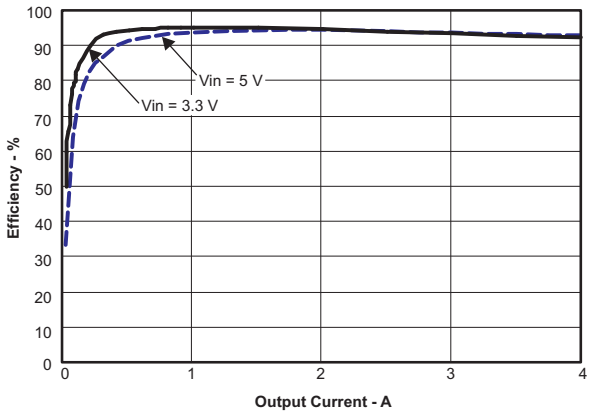


Figure 37. Efficiency vs Load Current

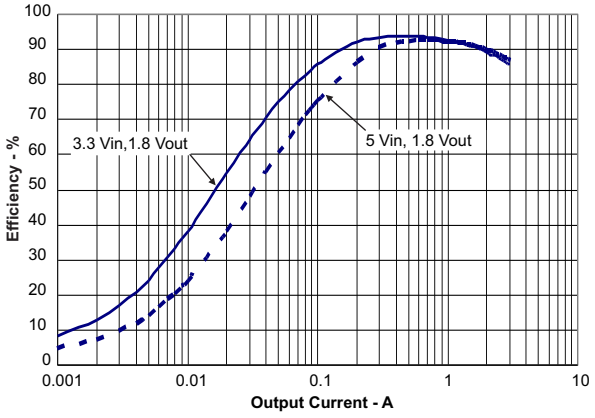


Figure 38. Efficiency vs Load Current

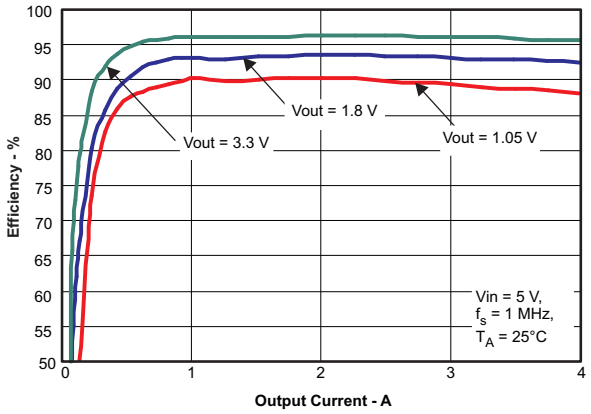


Figure 39. Efficiency vs Load Current

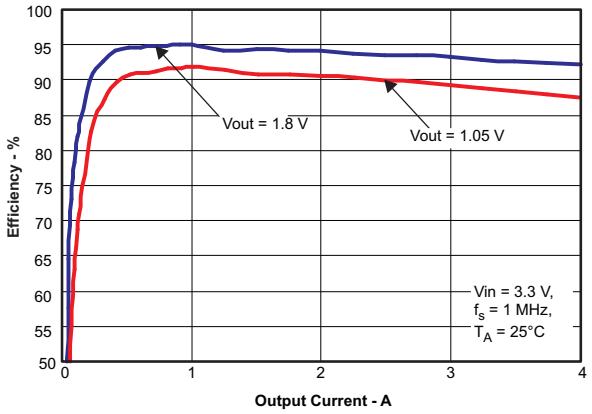


Figure 40. Efficiency vs Load Current

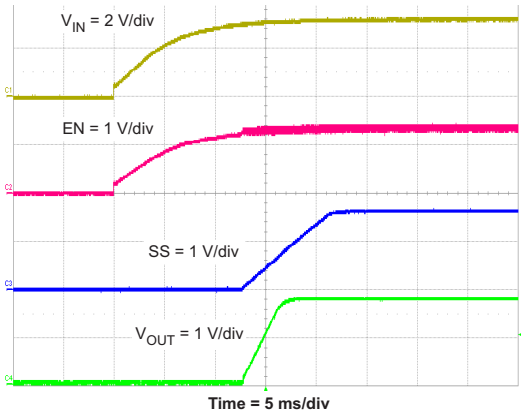


Figure 41. Power-Up VOUT, VIN

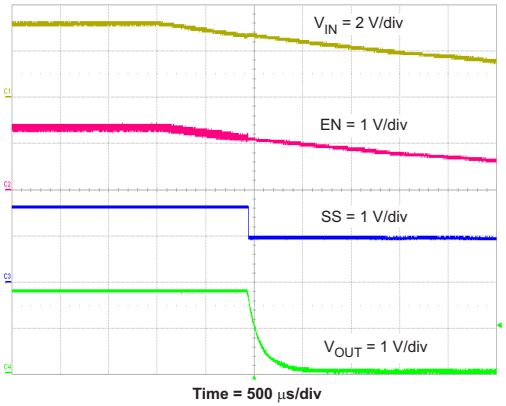


Figure 42. Power-Down VOUT, VIN

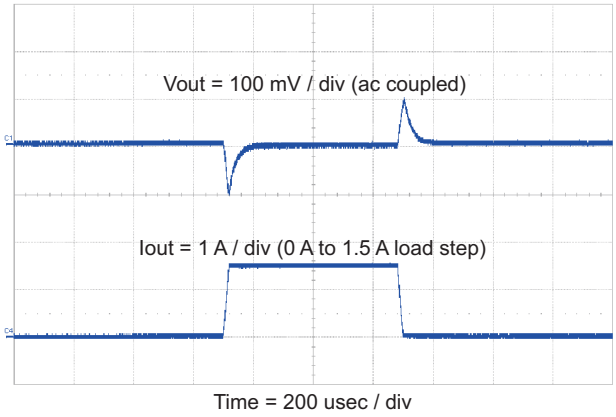


Figure 43. Transient Response, 1.5-A Step

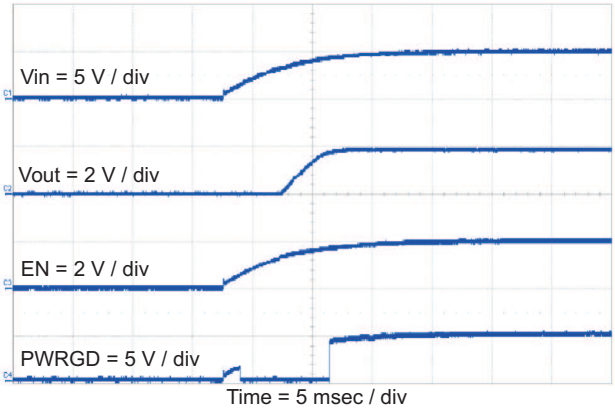


Figure 44. Power-Up VOUT, VIN

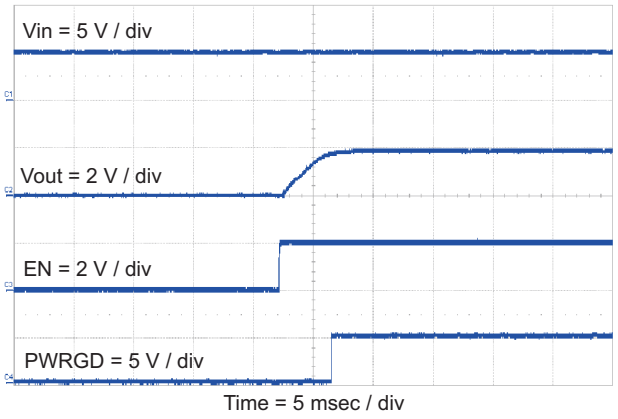


Figure 45. Power-Up VOUT, EN

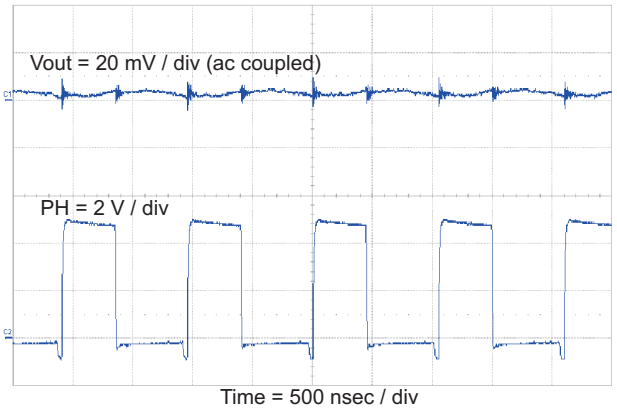


Figure 46. Output Ripple, 3.5 A

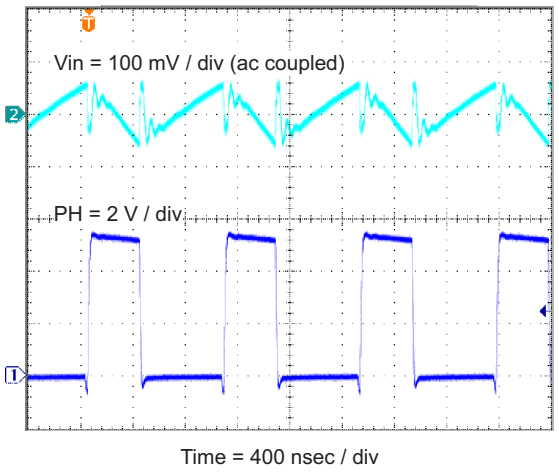


Figure 47. Input Ripple, 3.5 A

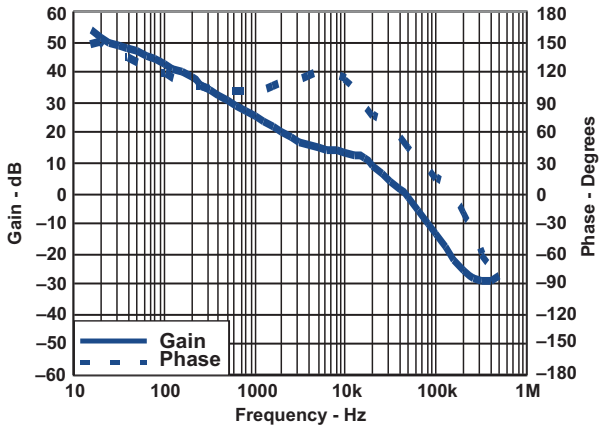


Figure 48. Closed-Loop Response, VIN (5 V), 3.5 A

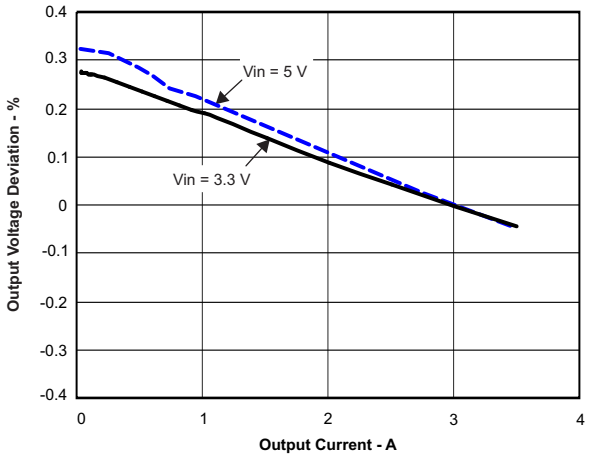


Figure 49. Load Regulation vs Load Current

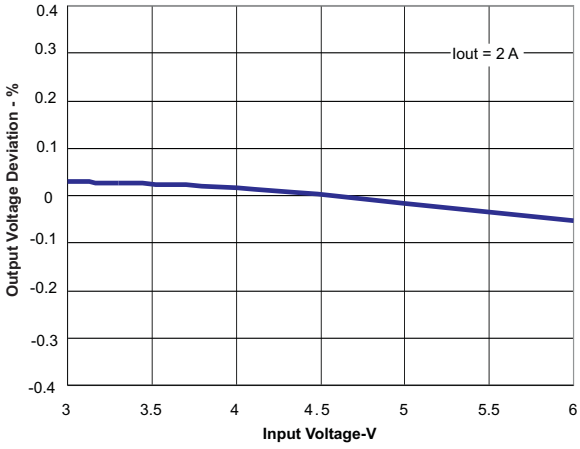


Figure 50. Regulation vs Input Voltage

11 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 2.95 and 6 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS57114-EP converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 47 µF is a typical choice; however, this may vary depending upon the output power being delivered.

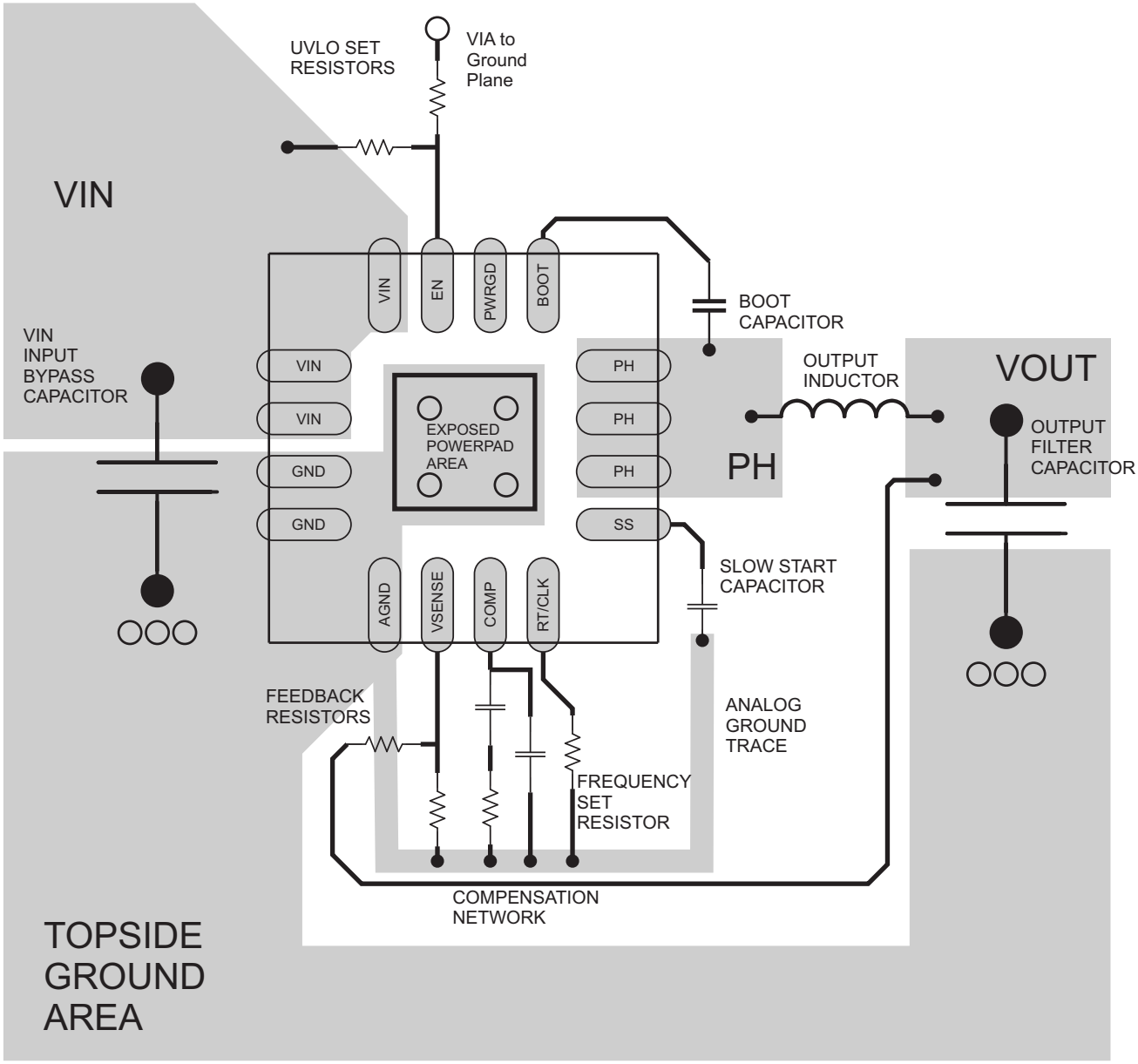
12 Layout

12.1 Layout Guidelines

Layout is a critical portion of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. Take care to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See *Layout Example* for a PCB layout example. Tie the GND pins and AGND pin directly to the thermal pad under the IC. Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC. Use additional vias to connect the top-side ground area to the internal planes near the input and output capacitors. For operation at full-rated load, the top-side ground area along with any additional internal ground planes must provide adequate heat dissipating area.

Locate the input bypass capacitor as close to the IC as possible. Route the PH pin to the output inductor. Because the PH connection is the switching node, locate the output inductor close to the PH pins and minimize the area of the PCB conductor to prevent excessive capacitive coupling. Also, locate the boot capacitor close to the device. Connect the sensitive analog ground connections for the feedback voltage divider, compensation components, slow-start capacitor, and frequency-set resistor to a separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise, so locate the RT resistor as close as possible to the IC and connect it with minimal lengths of trace. Place the additional external components approximately as shown. It may be possible to obtain acceptable performance with alternative PCB layout. However, this layout, meant as a guideline, produces good results.

12.2 Layout Example



13 器件和文档支持

13.1 Trademarks

SWIFT, SwitcherPro are trademarks of Texas Instruments.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS57114MRTETEP	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	7114M	Samples
V62/14612-01XE	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	7114M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

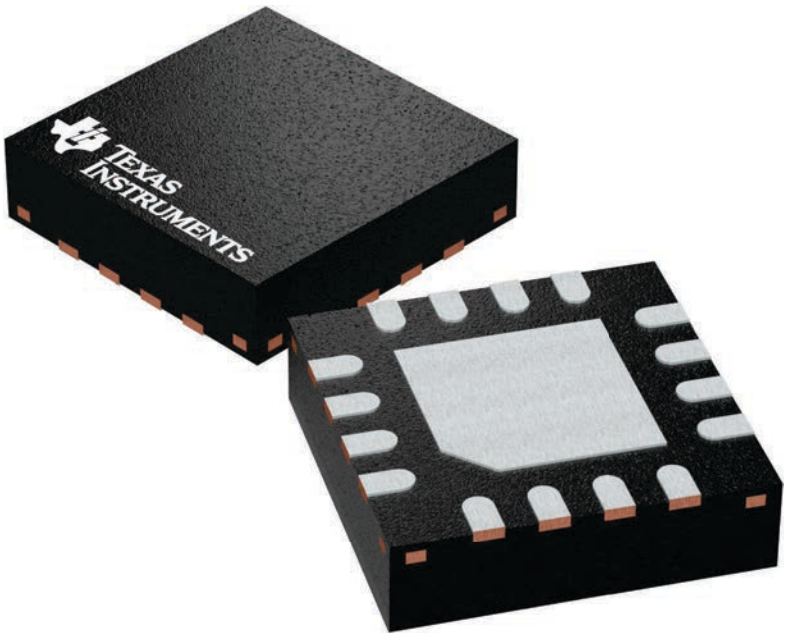
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

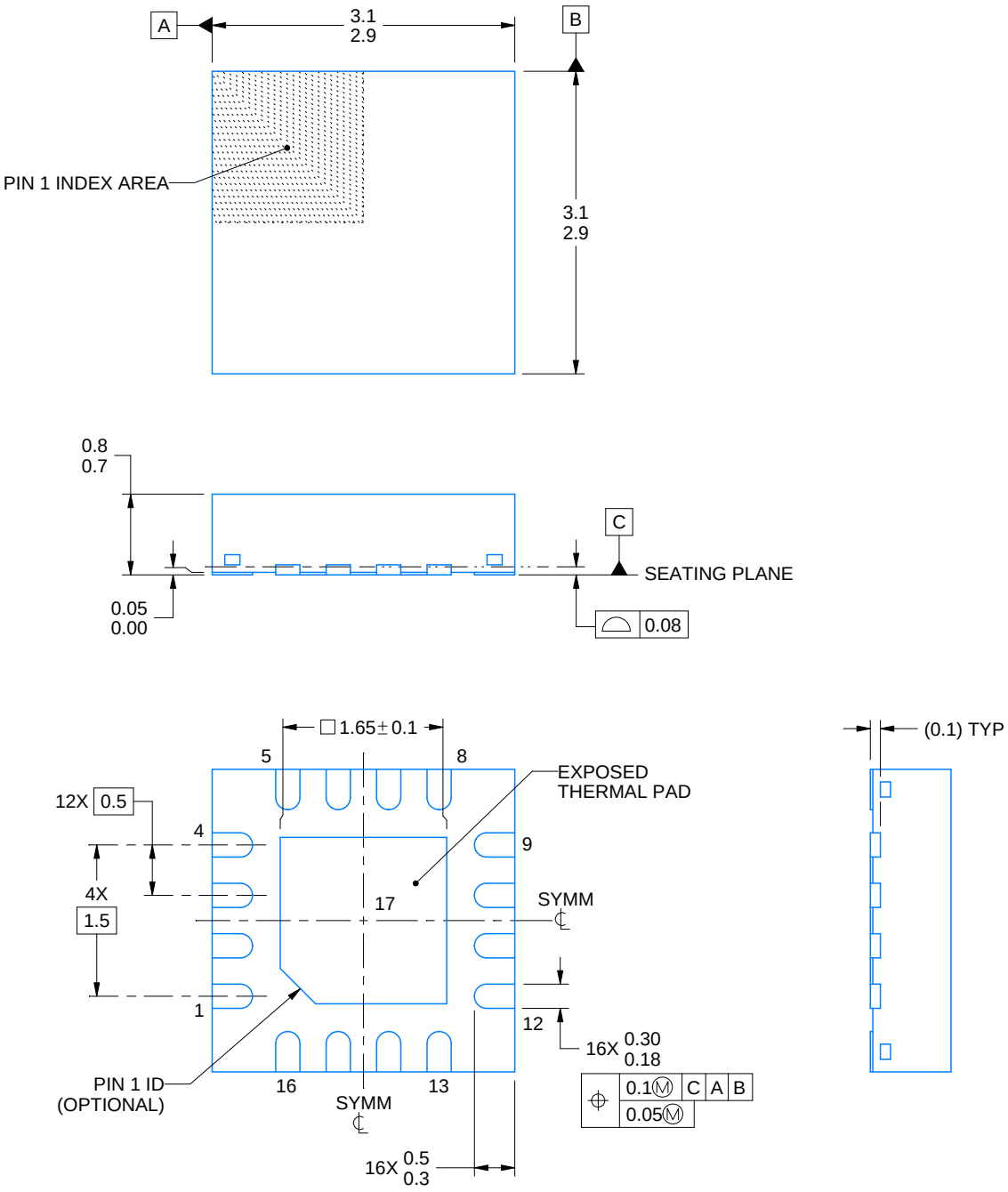


RTE0016F

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

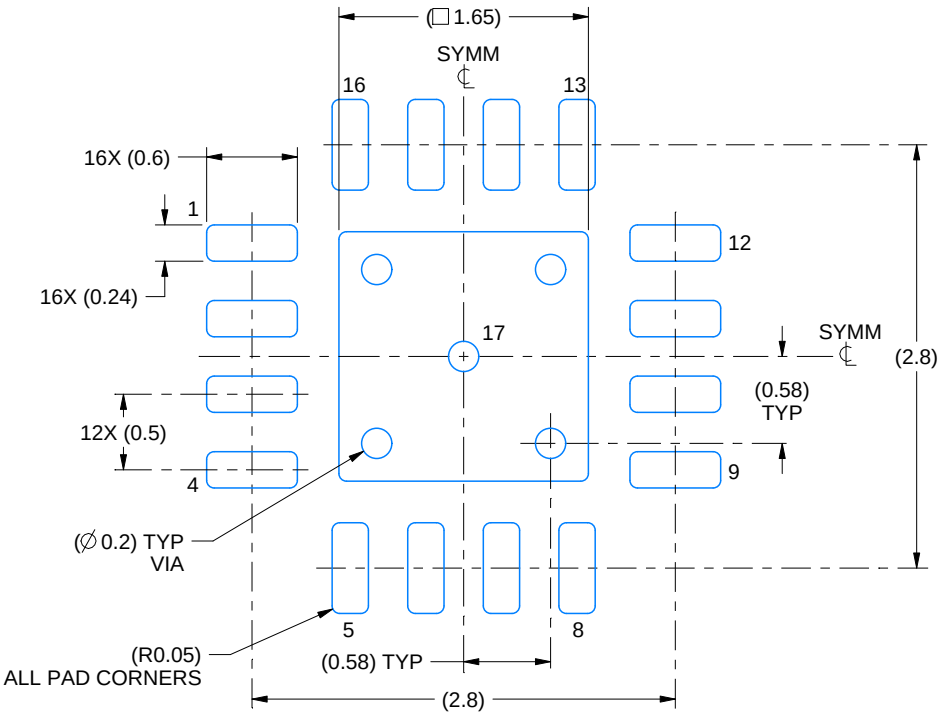
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

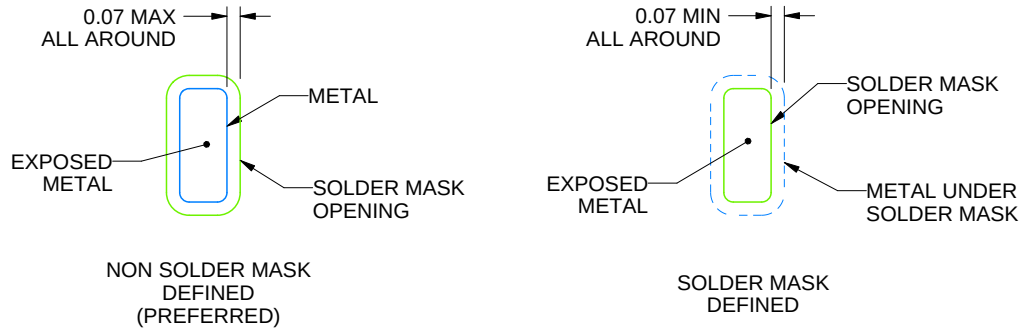
RTE0016F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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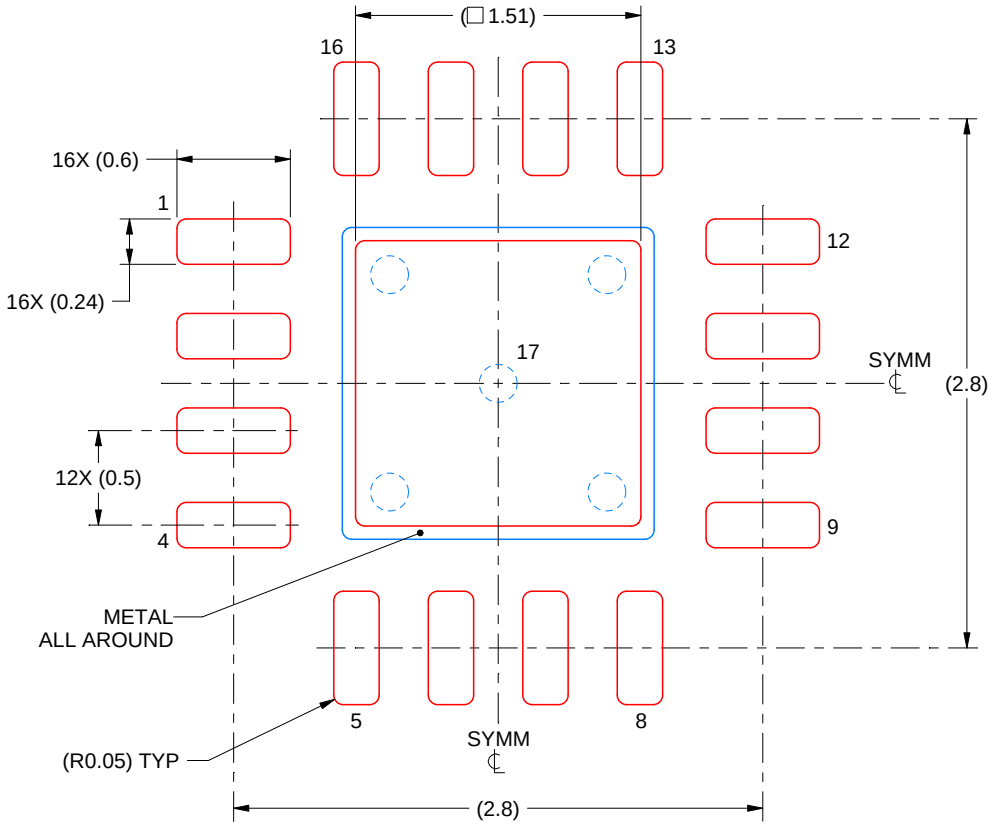
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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