TPS6014x Low Power DC-DC Converter Regulated 5-V, 100-mA Charge Pump Voltage Tripler

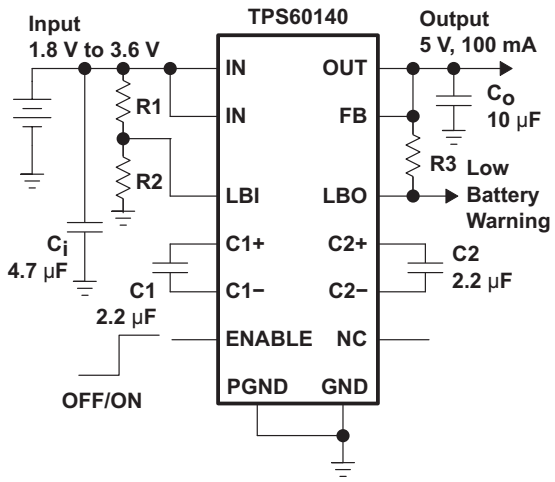
1 Features

- Regulated 5 V ±4% Output Voltage
- Up to 100-mA Output Current
- 1.8-V to 3.6-V Input Voltage Range
- 65-µA Quiescent Supply Current
- 0.05-µA Shutdown Current, Battery Is Isolated From Load in Shutdown
- Integrated Low-Battery or Power-Good Indicator
- Low-Output Voltage Ripple Over Complete Output Current Range
- Easy-to-Design With Low-EMI Power Supply Because No Inductors Are Required
- Evaluation Module Available (TPS60140EVM-144)
- Available in a 6.5-mm × 4.4-mm 20-Pin HTSSOP Package

2 Applications

- Replacement of DC-DC Converters With Inductors in Battery-Powered Applications:
  - Two Battery Cells to 5-V Conversions
  - Portable Instruments
  - Miniature Equipment
  - Backup-Battery Boost Converters
  - Medical Instruments
  - 5-V Smart Card Supplies

Typical Application Schematic



3 Description

The TPS6014x step-up, regulated charge pumps generate a 5-V ±4% output voltage from a 1.8-V to 3.6-V input voltage range. The devices are typically powered by two alkaline, NiCd, or NiMH battery cells and provide an output current of minimum 100 mA from a 2-V input. Only four external capacitors are needed to build a complete voltage tripler charge pump.

The devices regulate the output by using the pulse-skip topology. The controller is optimized for lowest output voltage ripple over the complete output current range. The output peak current and therefore the output voltage ripple are drastically reduced compared to a conventional pulse-skip topology by regulating the charge pump output resistance. At light loads the maximum output resistance is limited to assure a low quiescent current.

The TPS60140 includes a low-battery comparator that issues a warning if the battery voltage drops below a user-adjustable threshold voltage. The TPS60141 features a power-good output that goes active when the output voltage reaches 90% of its nominal value.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6014x	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Output Current

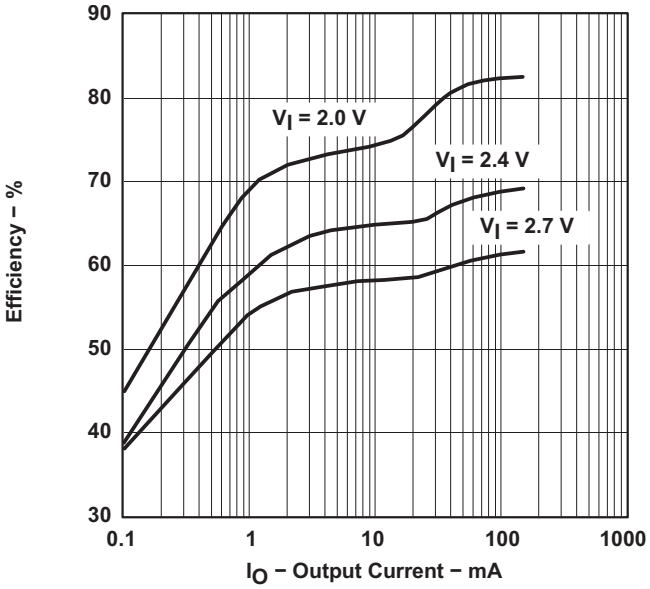


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2000) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Description (continued)

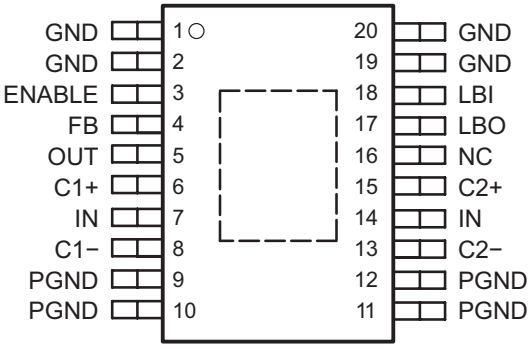
The logic shutdown function disables the converter, reduces the supply current to a maximum of 1 µA and disconnects the output from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This DC/DC converter requires no inductors, therefore, EMI is of little concern. The TPS6014x operates over a free-air temperature range of –40°C to 85°C. It is available in the small, thermally enhanced 20-pin HTSSOP package (PWP).

6 Device Comparison Table

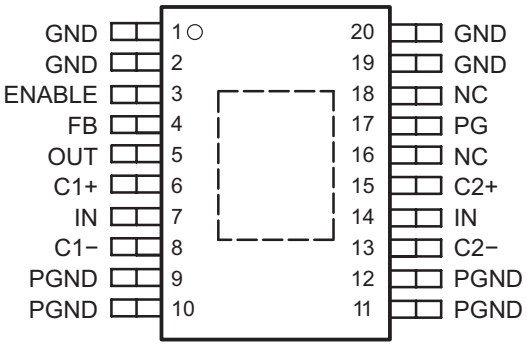
PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	DEVICE FEATURES	
TPS60140	20-pin thermally enhanced HTSSOP	PWP	2-cell to 5 V, 100 mA	Low-battery detector
TPS60141				Power-good detector

7 Pin Configuration and Functions

PWP Package (TPS60140)
20 Pin-HTSSOP
Top View



PWP Package (TPS60141)
20 Pin-HTSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	6	—	Positive terminal of the flying capacitor C1
C1−	8	—	Negative terminal of the flying capacitor C1
C2+	15	—	Positive terminal of the flying capacitor C2
C2−	13	—	Negative terminal of the flying capacitor C2
ENABLE	3	I	ENABLE input. Connect ENABLE to IN for normal operation. When ENABLE is a logic low, the device turns off and the supply current decreases to 0.05 µA. The output is disconnected from the input when the device is placed in shutdown.
FB	4	I	Feedback input. Connect FB to OUT as close to the load as possible to achieve best regulation. A resistive divider is on the chip to match the output voltage to the internal reference voltage of 1.21 V.
GND	1, 2, 19, 20	—	Ground. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7,14	I	Supply input. Bypass IN to PGND with capacitor C_{IN}. Connect both IN terminals through a short trace.
LBO/PG	17	O	Low battery detector output (TPS60140) or power good output (TPS60141). Open-drain output of the low-battery indicator or power-good comparator. It can sink 1 mA. TI recommends a 100-kΩ to 1-MΩ pullup. Leave the terminal unconnected if the low-battery or power-good detector function is not used.
LBI/NC	18	I	Low battery detector input (TPS60140 only). The voltage applied to this terminal is compared to the internal 1.21-V reference voltage. Connect the terminal to ground if the low-battery comparator is not used. On the TPS60141, this terminal is not connected to the chip and should remain unconnected.
NC	16	—	Not connected
OUT	5	O	Regulated 5-V power output. Bypass OUT to PGND with the output filter capacitor C_{OUT}.
PGND	9−12	—	Power ground. The charge-pump current flows through this terminal. Connect all PGND terminals together.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Supply voltage at IN to GND and PGND		−0.3	3.6	V
Voltage at OUT, ENABLE, LBI, LBO, PG, FB to GND and PGND		−0.3	5.4	V
Voltage at C1+ to GND		−0.3	V_{OUT} + 0.3	V
Voltage at C1– to GND		−0.3	V_{IN} + 0.3	V
Voltage at C2+ to GND		−0.3	V_{OUT} + 0.3	V
Voltage at C2– to GND		−0.3	V_{IN} + 0.3	V
Continuous output current			150	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $V_{(ENABLE)}$, $V_{(LBI)}$, $V_{(LBO)}$, and $V_{(PG)}$ can exceed V_{IN} up to the maximum rated voltage without increasing the leakage current drawn by these inputs.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.8		3.6	V
$I_O$max	Continuous output current			100	mA
T_J	Operating junction temperature			125	°C

8.4 Thermal Information

THERMAL METRIC (1)		TPS60140, TPS60141 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

C_{IN} = 4.7 µF, C1 = C2 = 2.2 µF, C_{OUT} = 10 µF(1) at T_C = −40°C to 85°C, V_{IN} = 2 V, FB = V_{OUT} and ENABLE = V_{IN} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(UVLO)}$	Undervoltage lockout threshold		T_C = 25°C		1.6	1.8	V
$I_O$max	Maximum continuous output current			100			mA
V_O	Output voltage		1.8 V < V_{IN} < 2 V, V_{OUT}, Start-up = 5 V, 0 < I_{OUT} < $I_O$max/2, T_C = 0°C to 70°C	4.8		5.2	V
			2 V < V_{IN} < 3.6 V, 0 < I_{OUT} < $I_O$max	4.8		5.2	
I_{lkg}(OUT)	Output leakage current		V_{IN}= 2.4 V, $V_{(ENABLE)}$ = GND			1	µA
I_Q	Quiescent current (no-load input current)		V_{IN}= 2.4 V		65	90	µA
$I_{(SD)}$	Shutdown current		V_{IN} = 2.4 V, $V_{(ENABLE)}$ = GND		0.05	1	µA
$f_{(OSC)}$	Oscillator frequency			210	320	450	kHz
V_{IL}	ENABLE input voltage low		V_{IN} = 1.8 V			0.3 × V_I	V
V_{IH}	ENABLE input voltage high		V_{IN} = 3.6 V	0.7 × V_I			V
$I_{lkg(ENABLE)}$	ENABLE input leakage current		$V_{(ENABLE)}$ = GND or V_{IN}		0.01	0.1	µA
	Output load regulation		V_{IN} = 2.4 V, 1 mA < I_{OUT} < I_{OUT}max, T_C = 25°C		0.003		%/mA
	Output line regulation		2 V < V_{IN} < 3.6 V, V_{OUT} = 5 V: I_{OUT} = 75 mA, T_C = 25°C		0.08		%/V
$I_{(SC)}$	Short-circuit current limit		V_{IN}< 2.4 V, V_{OUT} = 0 V, T_C = 25°C		100		mA
$V_{(TRIP,LBI)}$	LBI trip voltage	TPS60140	V_{IN} = 1.8 V to 2.2 V, Hysteresis 0.8% for rising LBI voltage, T_C = 0°C to 70°C	1.15	1.21	1.27	V
$I_{IN(LBI)}$	LBI input current	TPS60140	LBI = 1.3 V		20	100	nA
$V_{OUT(LBO)}$	LBO output voltage low(2)	TPS60140	$V_{(LBI)}$ = 0 V, $I_{(LBO,SINK)}$ = 1 mA			0.4	v
$I_{lkg(LBO)}$	LBO output leakage current	TPS60140	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 5 V		0.01	0.1	µA
$V_{(TRIP,PG)}$	Power-good trip voltage	TPS60141	T_C = 0°C to 70°C	0.86 × V_O	0.90 × V_O	0.94 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	TPS60141	V_{OUT} ramping down, T_C = 0°C to 70°C		0.80%		
$V_{OUT(PG)}$	Power-good output voltage low	TPS60141	V_{OUT}= 0 V, $I_{(PG,SINK)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	TPS60141	V_{OUT} = 5 V, $V_{(PG)}$ = 5 V		0.01	0.1	µA

(1) All capacitors are ceramic capacitors of the type X5R or X7R.
(2) During start-up the LBO signal is invalid for the first 500 µs.

8.6 Typical Characteristics

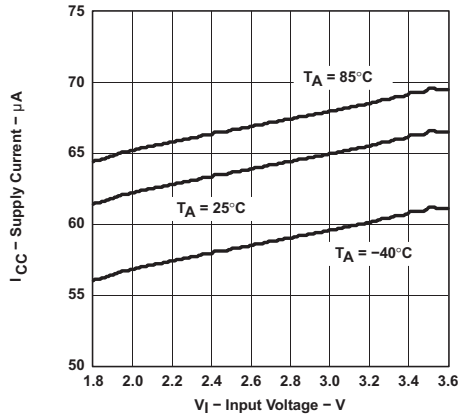


Figure 1. Quiescent Supply Current vs Input Voltage

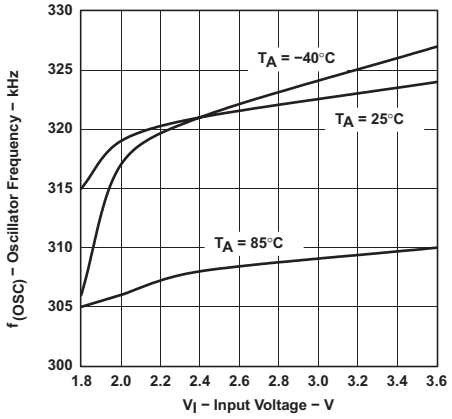


Figure 2. Oscillator Frequency vs Input Voltage

9 Detailed Description

9.1 Overview

The TPS6014x devices regulate the output voltage using an improved pulse-skip topology. In pulse-skip mode the error amplifier disables switching of the power stages when it detects an output voltage higher than 5 V. The oscillator halts and the controller skips switching cycles. The error amplifier reactivates the oscillator and starts switching of the power stages again when the output voltage drops below 5 V. The output resistance of the charge pump is controlled to improve the ripple performance. This limits the output current to the minimum that is necessary to sustain a regulated output voltage. The benefit is that the ripple performance is nearly as good as with a linear-regulation topology.

At light loads a conventional pulse-skip regulation mode is used, but the charge pump output resistance is held at a high level. The pulse-skip regulation minimizes the operating current because the charge pump does not switch continuously and hence the gate-charge losses of the MOSFETs are reduced. Additionally, all functions except voltage reference, error amplifier, and low-battery or power-good comparator are deactivated when the output is higher than 5 V. When switching is disabled by the error amplifier, the load is also isolated from the input. This improved pulse-skip control topology is also referred to as *active-cycle* control.

9.2 Functional Block Diagrams

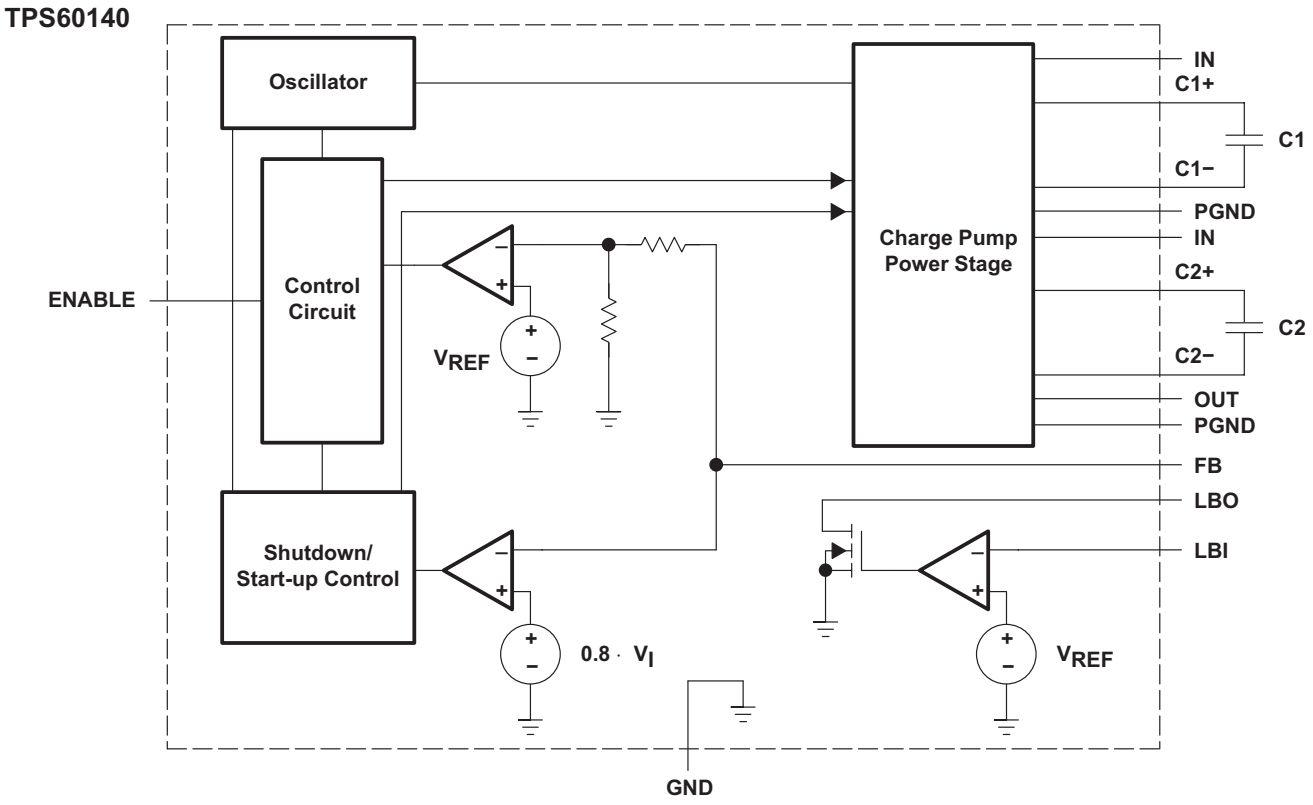


Figure 3. TPS60140 Functional Block Diagram

Functional Block Diagrams (continued)

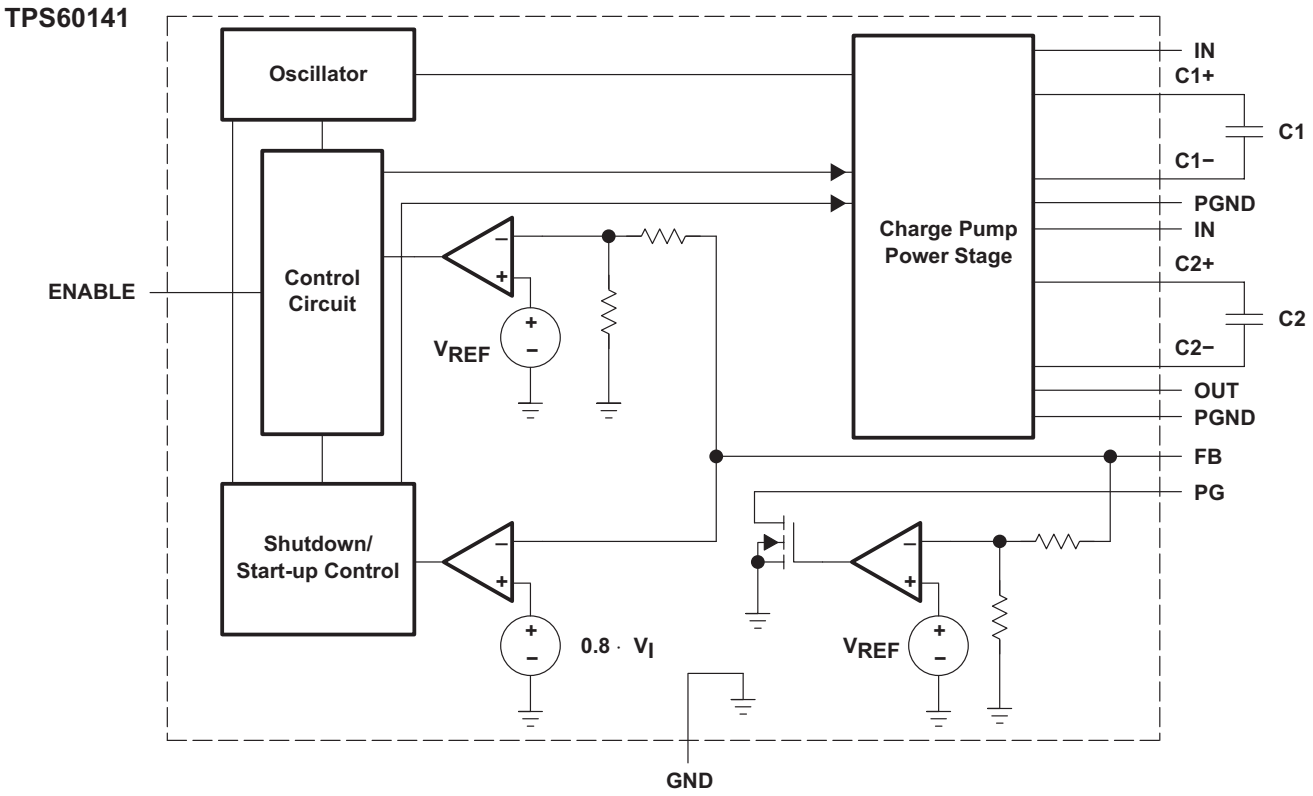


Figure 4. TPS60141 Functional Block Diagram

9.3 Feature Description

9.3.1 Undervoltage Lockout

The TPS6014x devices have an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below 1.6 V.

9.3.2 Low-Battery Detector (TPS60140 Only)

The internal low-battery comparator trips at 1.21 V ± 5% when the voltage on pin LBI ramps down. The voltage $V_{(TRIP)}$ at which the low battery warning is issued can be adjusted with a resistive divider as shown in Figure 5. TI recommends that the sum of resistors R1 and R2 to be in the 100-kΩ to 1-MΩ range. When choosing R1 and R2, be aware of the input leakage current into the LBI terminal.

LBO is an open-drain output. TI recommends an external pullup resistor to OUT, in the 100-kΩ to 1-MΩ range. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected.

Feature Description (continued)

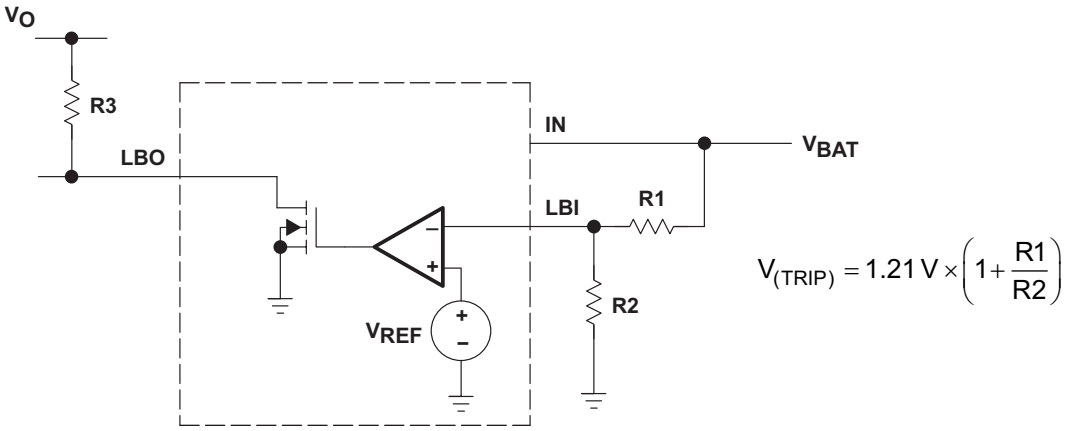


Figure 5. Programming of the Low-Battery Comparator Trip Voltage

A 100-nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low battery detection, with $V_{(LBI)}$ = 1.15 V to 1.27 V:

$$R2 = 1\,M\Omega \times \frac{V_{LBI}}{V_{BAT}} \quad (1)$$

$$R1 = 1\,M\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum trip voltage:

$$V_{trip(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \quad (3)$$

$$V_{trip(man)} = V_{LBI(man)} \times \frac{R1_{(man)} + R2_{(mix)}}{R2_{(mix)}} \quad (4)$$

Table 1. Recommended Values for the Resistive Divider From the E96 Series (±1%)

V_I/V	R1/kΩ	R2/kΩ	$V_{(TRIP)}$MIN/V	$V_{(TRIP)}$MAX/V
1.8	357	732	1.700	1.902
1.9	365	634	1.799	2.016
2	412	634	1.883	2.112
2.1	432	590	1.975	2.219
2.2	442	536	2.08	2.338

9.3.3 Power-Good Detector (TPS60141)

The power-good (PG) terminal is an open-drain output that is pulled low when the output is out of regulation. When the output rises to typically 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation an external pullup resistor must be connected between PG and OUT. The resistor should be in the 100-kΩ to 1-MΩ range. If the power-good function is not used, the PG terminal should remain unconnected.

9.4 Device Functional Modes

9.4.1 Start-Up Procedure and Shutdown

During start-up (that is, when ENABLE is set from logic low to logic high), the output capacitor is charged up with a limited current until the output voltage (V_O) reaches 0.8 × V_I. When the start-up comparator detects this voltage limit, the IC begins switching. This precharging of the output capacitor ensures a short start-up time. In addition, the inrush current into an empty output capacitor is limited because the current through the switches is limited before the charge pump starts switching.

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05 µA of supply current in this mode. Leakage current drawn from the output is as low as 1 µA (maximum). The device exits shutdown once ENABLE is set to a high level. When the device is in shutdown, the load is isolated from the input.

9.4.2 Short-Circuit Protection

The TPS6014x devices are also short-circuit protected. The output current is limited to typically 100 mA during a hard short-circuit condition at the output; that is, when V_{OUT} is GND. In this case, the condition to enter the start-up mode is met, the device stops switching and controls the on-resistance of the appropriate MOSFET switches to limit the current.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6014x charge pumps provide a regulated 5-V output from a 1.8-V to 3.6-V input voltage range. They can deliver a maximum continuous load current of at least 100 mA at V_I = 2 V minimum.

10.2 Typical Application

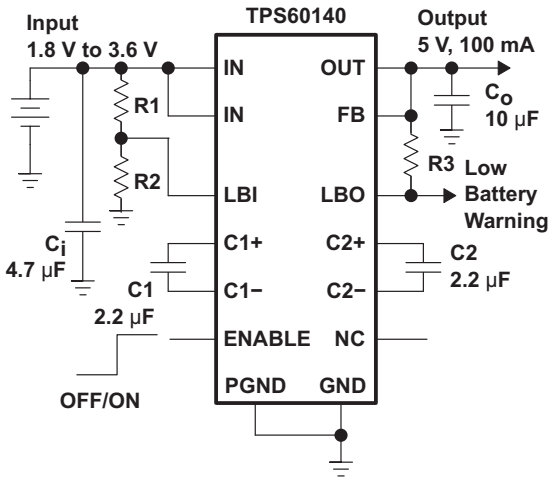


Figure 6. Typical Application Schematic

10.2.1 Design Requirements

Designed specifically for space-critical battery-powered applications, the complete charge pump circuit requires only four external capacitors. The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions*.

Table 2 shows the list of components for the *Application Curves*.

Table 2. Components for Application Curves

REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C2	2.2 µF	Ceramic flying capacitors	Taiyo Yuden	EMK316BJ225KL-T
C_{IN}	4.7 µF	Ceramic input capacitor	Taiyo Yuden	LMK316BJ475KL-T
C_{OUT}	10 µF	Ceramic output capacitor	Taiyo Yuden	JMK316BJ106ML-T
R1	357 kΩ	LBI input voltage adjustment		E96-Series
R2	619 kΩ	LBI input voltage adjustment		E96-Series
R3	1 MΩ	Pullup resistor for the open-drain output LBO		

10.2.2 Detailed Design Procedure

10.2.2.1 Capacitor Selection

The capacitance values of the TPS6014x external capacitors are closely linked to the output current and output ripple requirements. For lowest ripple, low ESR (< 0.1 Ω) capacitors should be used at the input and output of the charge pump.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. The input capacitor selection also depends on the output ripple requirements. C_{IN} is recommended to be about 2-times to 4-times as large as the flying capacitors. The lower the ESR of the input capacitor C_{IN}, the lower is the output ripple.

The output capacitor C_{OUT} can be selected from 2× to 50× larger than the flying capacitor, depending on the ripple tolerance. The larger C_{OUT} and the lower its ESR, the lower will be the output voltage ripple.

Generally, the flying capacitors will be the smallest. Only ceramic capacitors are recommended because of their low ESR and because they retain their capacitance at the switching frequency. Be aware that, depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U or Y5V-type capacitors will decrease in capacitance. Table 3 lists recommended capacitor values.

Table 3. Recommended Capacitor Values

I_{OUT} (mA)	C_{IN} (µF)	$C_{(xF)}$ (µF)	C_{OUT} (µF)	V_{PP}TYP (mV)
0 − 50	4.7	2.2	4.7	40
0 − 100	4.7	2.2	10	40
0 − 100	4.7	2.2	22	18

If the measured output voltage ripple is too high for the application, improvements can be made. The first step is to increase the capacitance at the output. If the ripple is still too high, the second step would be to increase the capacitance at the input. For lower output currents, lower value flying capacitors can be used. Table 3 and Table 4 lists the manufacturers of recommended capacitors.

Table 4. Recommended Capacitors (1)

MANUFACTURER	PART NUMBER	CAPACITANCE	CASE SIZE	TYPE
Taiyo Yuden	LMK212BJ105KG−T	1 µF	805	Ceramic
	EMK316BJ225KL−T	2.2 µF	1206	Ceramic
	LMK212BJ225MG−T	2.2 µF	805	Ceramic
	LMK316BJ475KL−T	4.7 µF	1206	Ceramic
	JMK316BJ106ML–T	10 µF	1206	Ceramic
	LMK325BJ106MN−T	10 µF	1210	Ceramic
	LMK432226MM−T	22 µF	1812	Ceramic
AVX	0805ZC105KAT2A	1 µF	805	Ceramic
	1206ZC225KAT2A	2.2 µF	1206	Ceramic

(1) Note: Case code compatibility with EIA 535BAAC and CECC30801 molded chips.

Table 5. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t−yuden.com/
AVX	X7R/X5R ceramic	http://www.avxcorp.com/

10.2.3 Application Curves

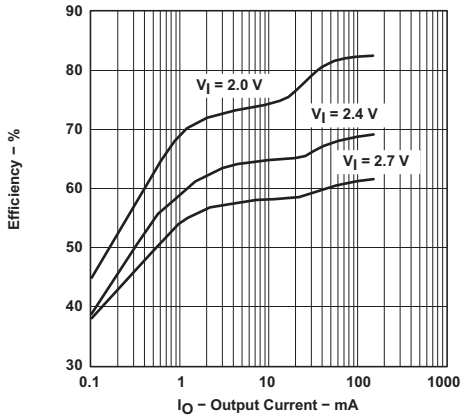


Figure 7. Efficiency vs Output Current

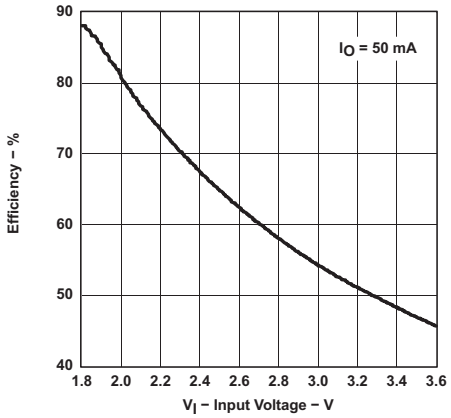


Figure 8. Efficiency vs Input Voltage

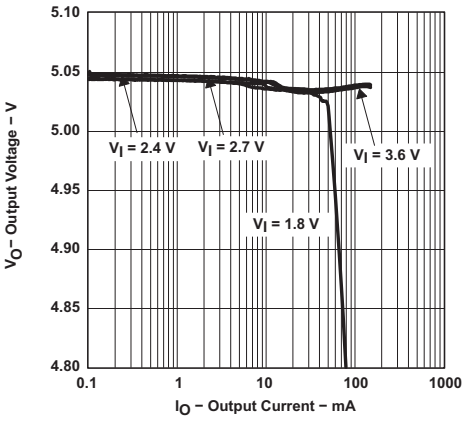


Figure 9. Output Voltage vs Output Current

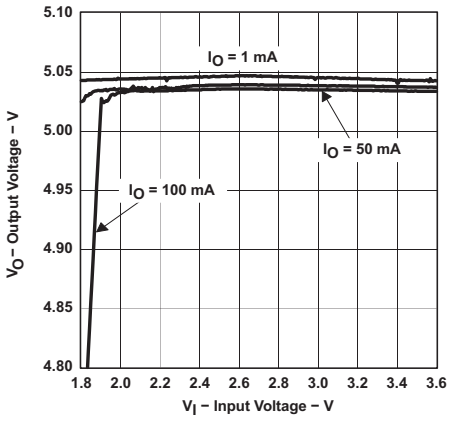


Figure 10. Output Voltage vs Input Voltage

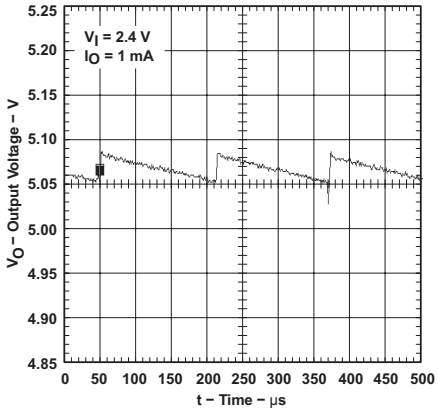


Figure 11. Output Voltage Ripple

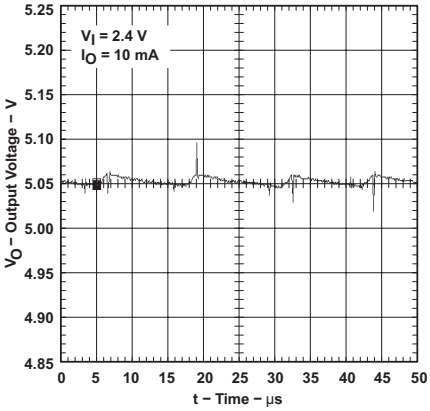


Figure 12. Output Voltage Ripple

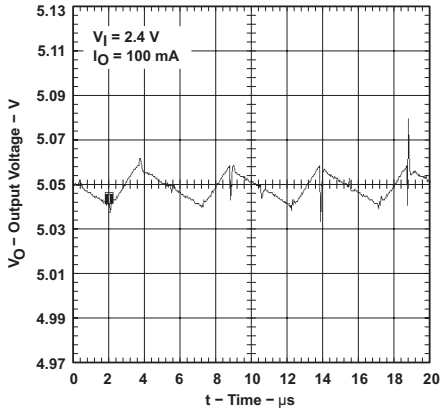


Figure 13. Output Voltage Ripple

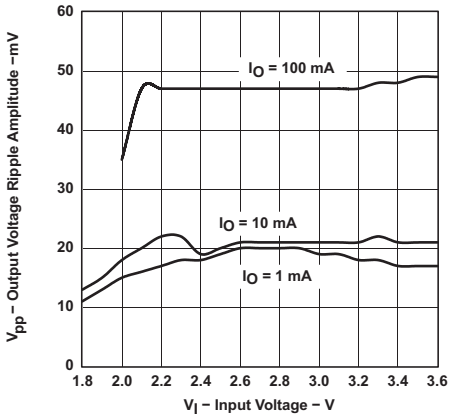


Figure 14. Output Voltage Ripple Amplitude vs Input Voltage

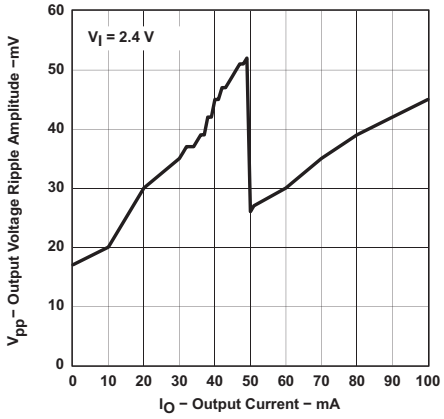


Figure 15. Output Voltage Ripple Amplitude vs Output Current

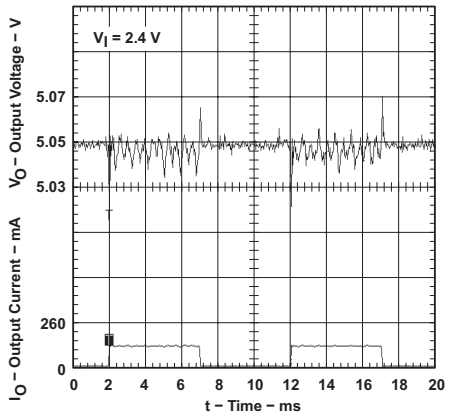


Figure 16. Load Transient Response

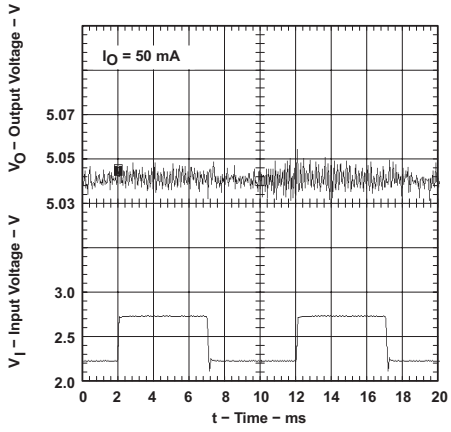


Figure 17. Line Transient Response

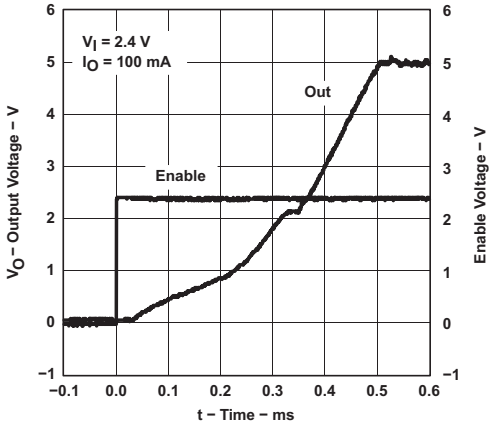


Figure 18. Output Voltage vs Time (Start-Up Timing)

11 Power Supply Recommendations

The TPS6014x devices have no special requirements for its input power supply. The input power supply's output current must be rated according to the supply voltage, output voltage and output current of the TPS6014x.

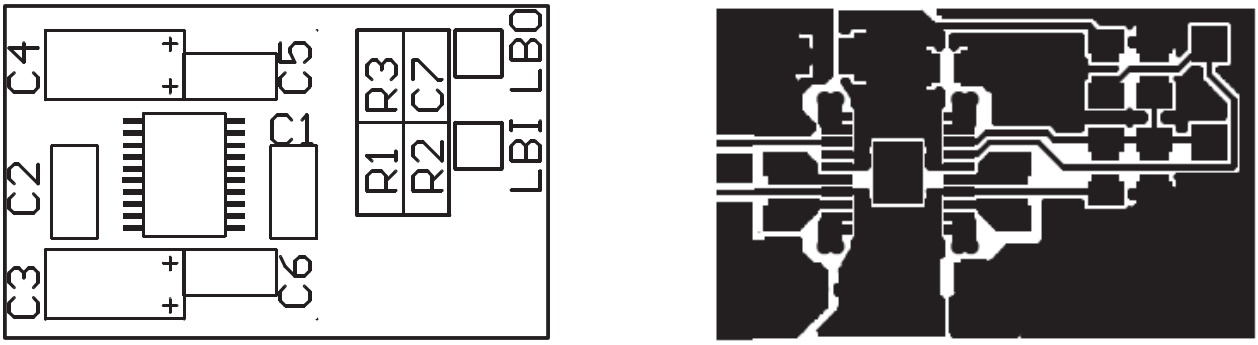
12 Layout

12.1 Layout Guidelines

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be soldered in close proximity to the IC. Connect ground and power ground terminals through a short, low-impedance trace. A PCB layout proposal for a two-layer board is given in Figure 19. The bottom layer of the board carries only ground potential for best performance. The layout also provides improved thermal performance as the exposed lead frame of the PowerPAD package is soldered to the PCB.

An evaluation module for the TPS60140 is available and can be ordered under product code TPS60140EVM−144. The EVM uses the layout shown in Figure 19.

12.2 Layout Example



NOTE: Actual size is 15 mm x 25 mm.

Figure 19. Recommended Component Placement and Board Layout

Table 6. Component Identification

IC1	TPS6014x
C1, C2	Flying capacitors
C3, C6	Input capacitors
C4, C5	Output capacitors
C7	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO

The best performance of the converter is achieved with additional bypass capacitors C5 and C6 at the input and output. Capacitor C7 should be included if the large line transients are expected. The capacitors are not required. They can be omitted in most applications.

12.3 Power Dissipation

The power dissipated in the TPS6014x depends mainly on input voltage and output current and is described by Equation 5:

$$P_{(DISS)} = I_O \times (3 \times V_I - V_O) \quad (5)$$

Power Dissipation (continued)

By observation of Equation 5, it can be seen that the power dissipation is worse for the highest input voltage V_I and the highest output current I_{OUT}. For an input voltage of 3.6 V and an output current of 100 mA, the calculated power dissipation $P_{(DISS)}$ is 580 mW. This is also the point where the charge pump operates with its lowest efficiency, which is only 45%, and hence with the highest power losses.

$P_{(DISS)}$ must be less than that allowed by the package rating. The thermal resistance junction to ambient of the thermally enhanced TSSOP is 178°C/W for an unsoldered package. The thermal resistance junction to case, with the exposed thermal pad soldered to an infinitive heat sink, is 3.5°C/W.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated using Equation 6.

$$R_{\theta JA}\,\text{max} = \frac{T_J\,\text{max} - T_A}{P_{(DISS)}\,\text{max}} = \frac{125°C - 85°C}{580\ \text{mW}} = 69°C / W \tag{6}$$

Using a board layout as described in the application information section, $R_{\theta JA}$ is typically 56°C/W for an unsoldered PowerPAD™ and 41°C/W for a soldered PowerPAD.

For more information, refer to the PowerPAD application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002).

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package*, SLMA002.
- *TPS6010x/TPS6011x Charge Pump*, SLVA070.

13.3 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS60140	Click here	Click here	Click here	Click here	Click here
TPS60141	Click here	Click here	Click here	Click here	Click here

13.4 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60140PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60140	Samples
TPS60140PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60140	Samples
TPS60140PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60140	Samples
TPS60141PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60141	Samples
TPS60141PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60141	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

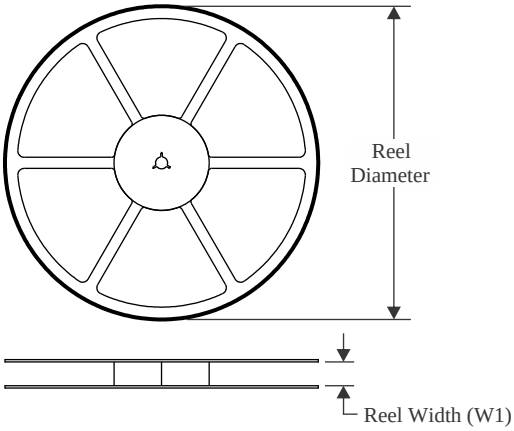
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

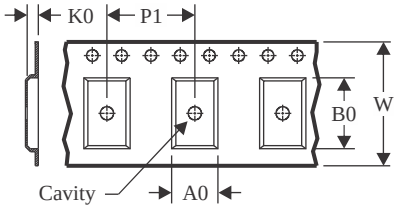
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

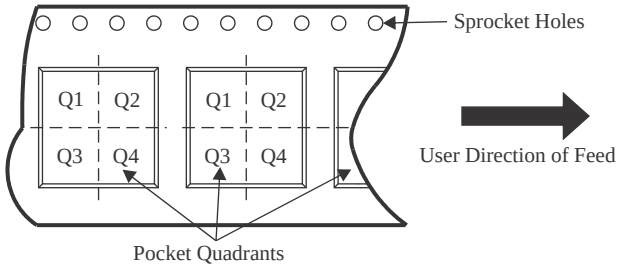


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

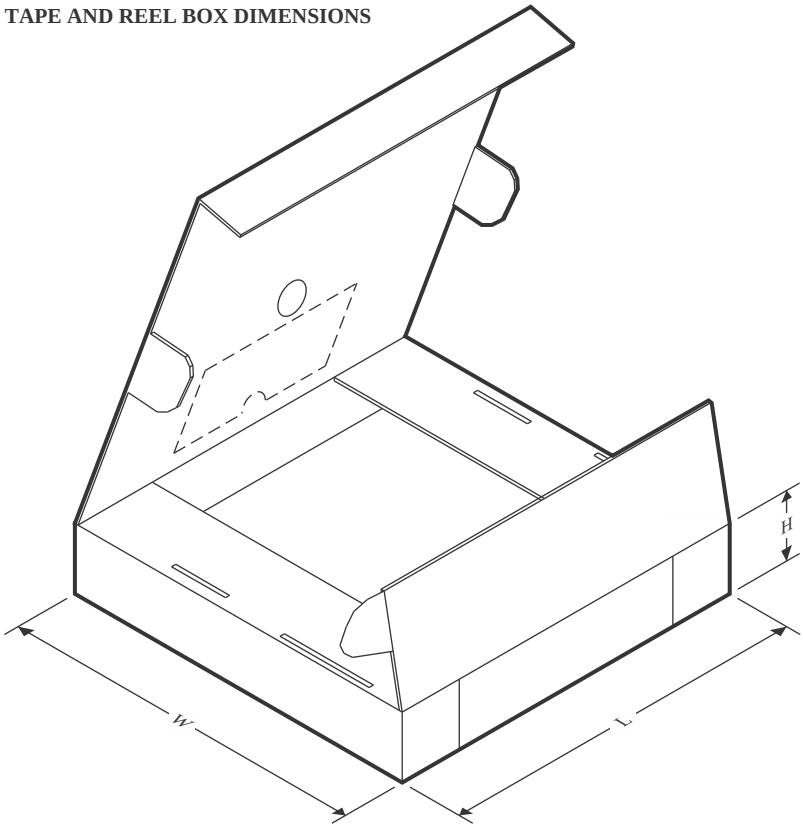
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60140PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS60141PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

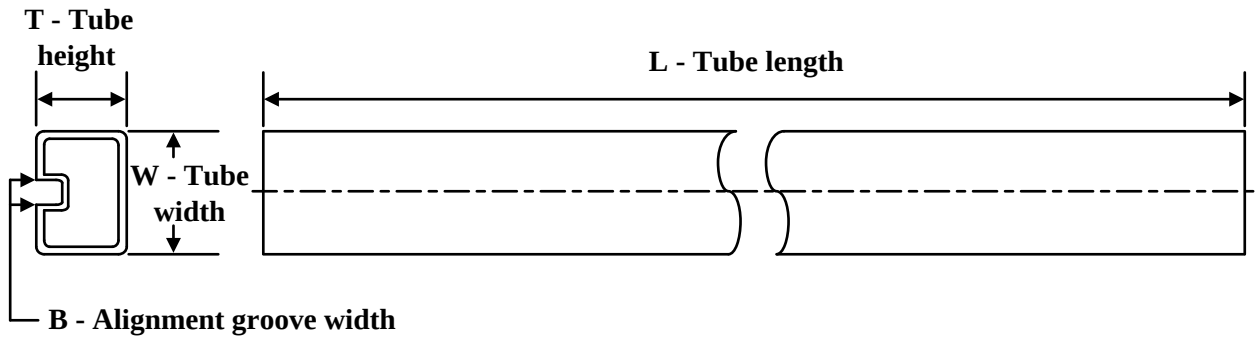
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60140PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS60141PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60140PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS60141PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

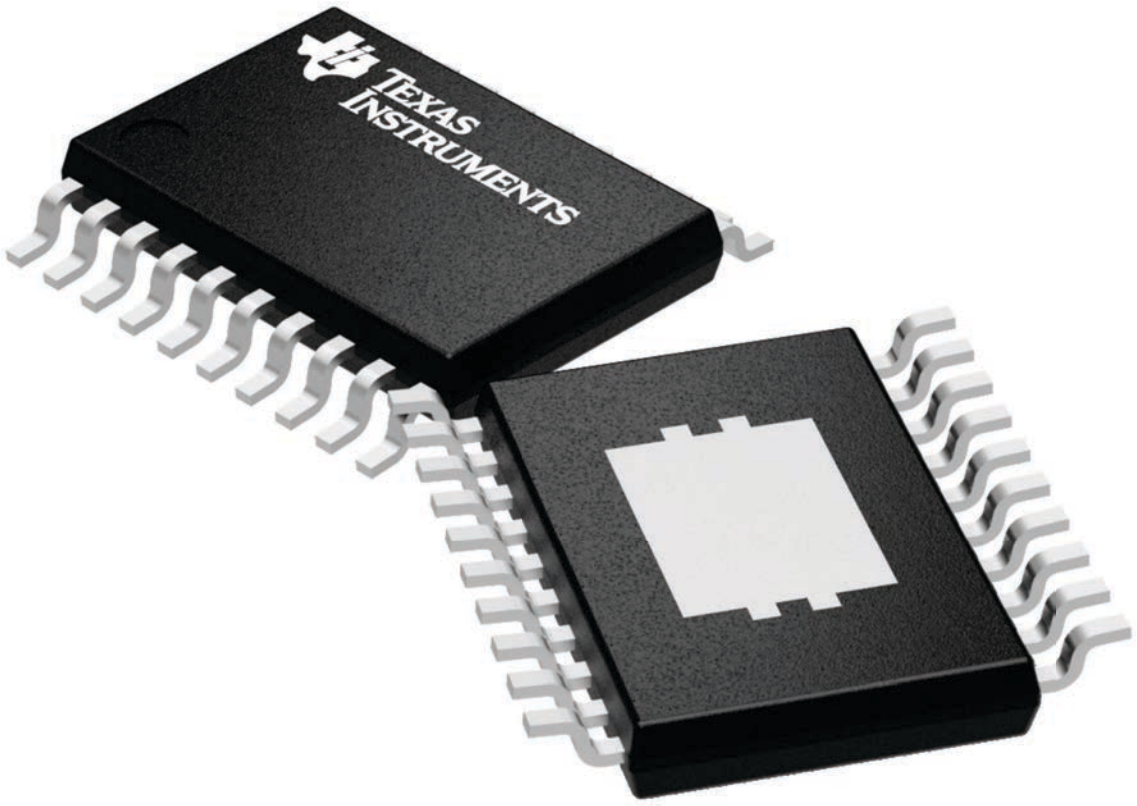
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

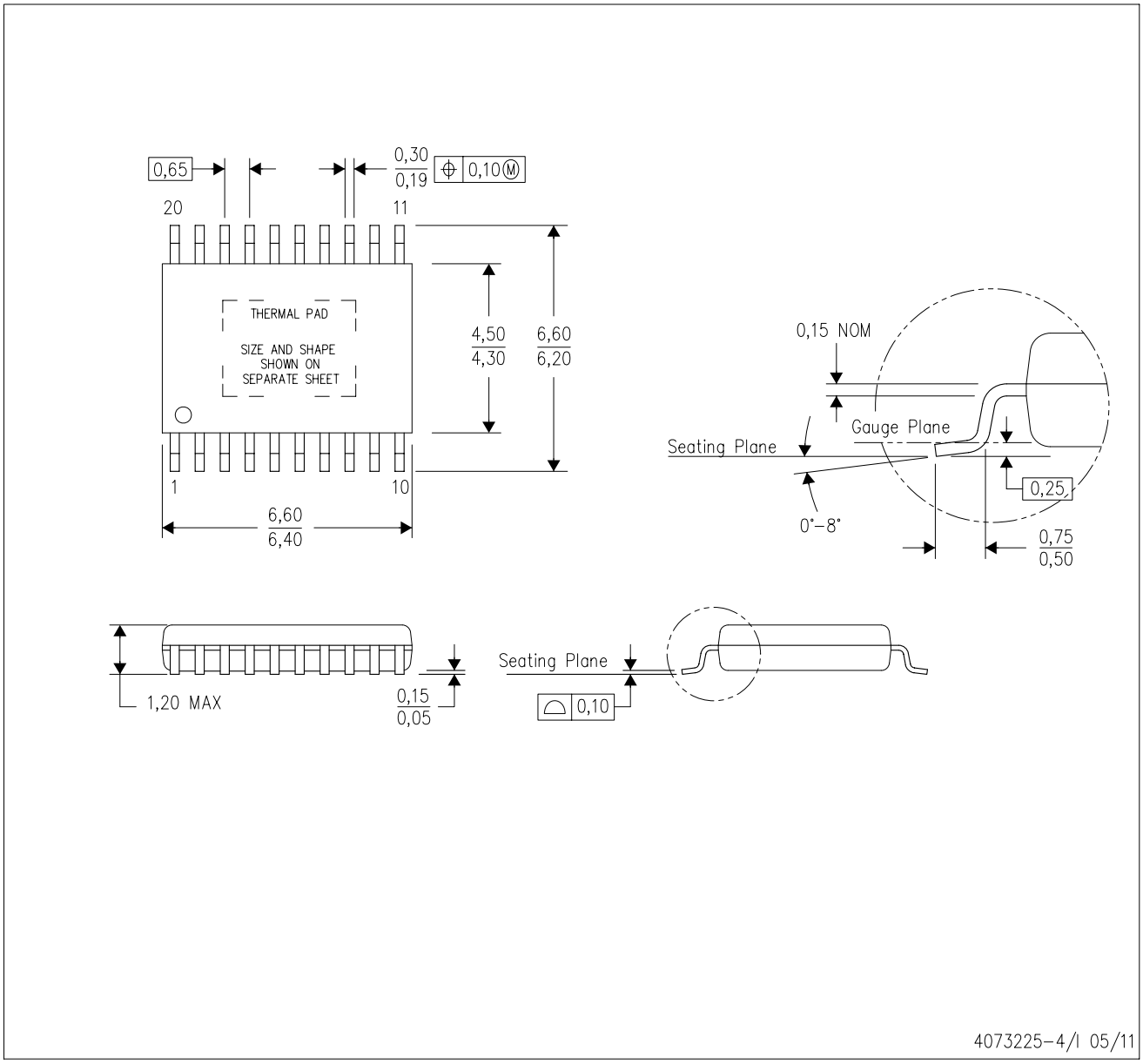
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

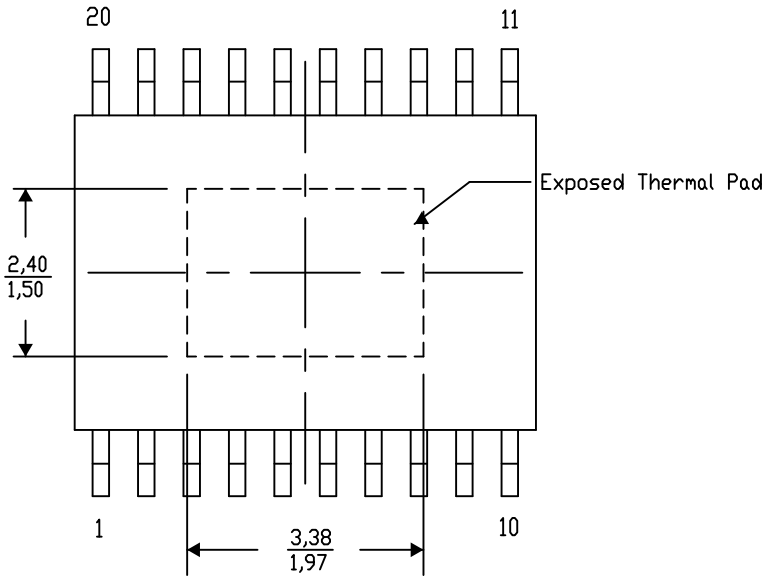
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

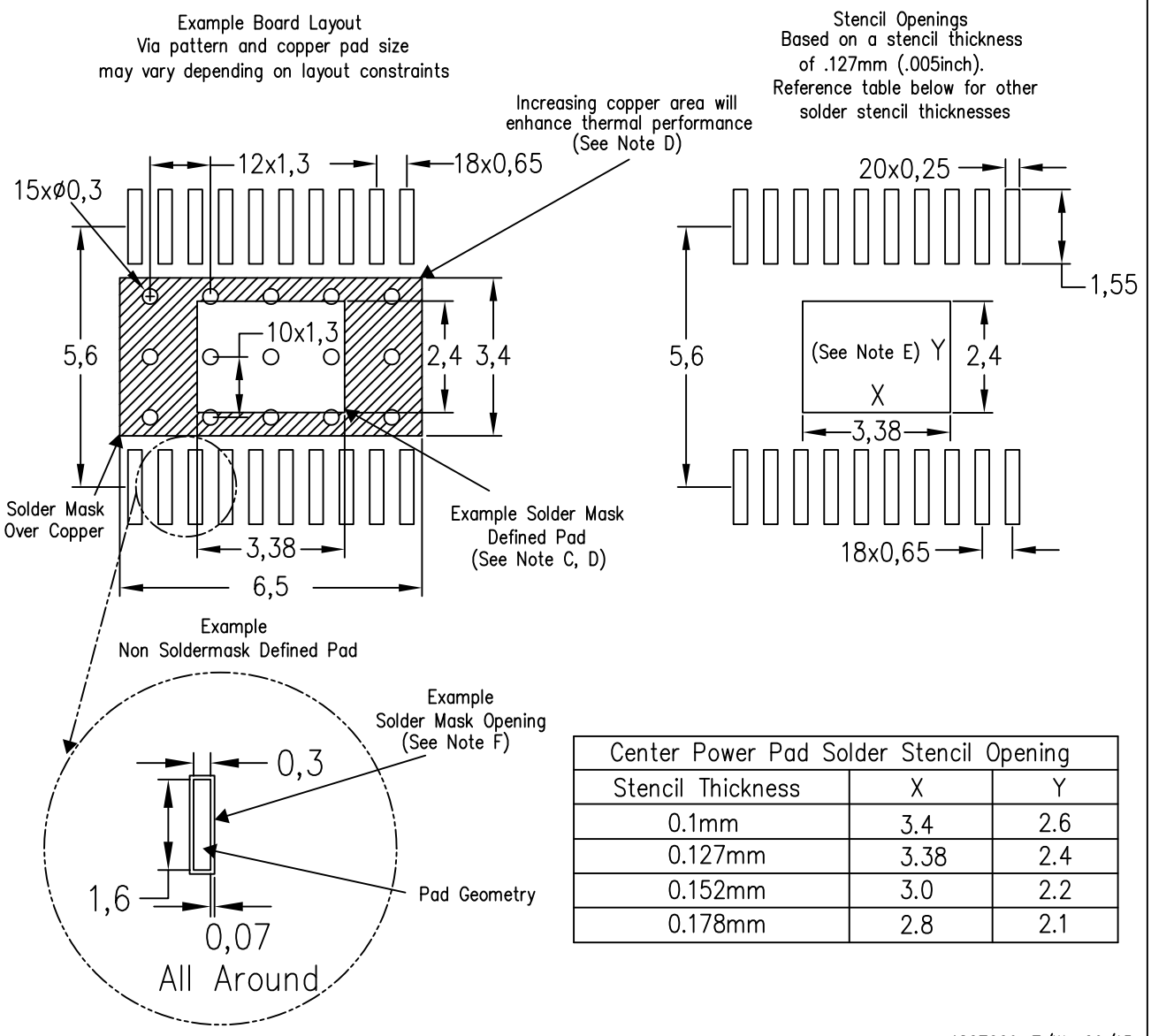
Exposed Thermal Pad Dimensions

4206332–19/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.38	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

4207609–7/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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