TEXAS INSTRUMENTS

TPS60300, TPS60301, TPS60302, TPS60303

SLVS302B – DECEMBER 2000 – REVISED OCTOBER 2015

TPS6030x Single-Cell to 3-V or 3.3-V, 20-mA Dual Output, High-Efficiency Charge Pump

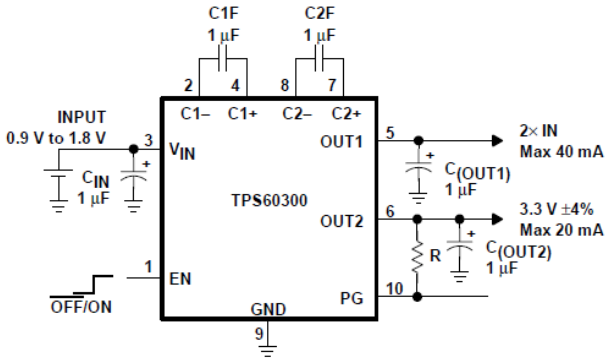
1 Features

- Input Voltage Range From 0.9 V to 1.8 V
- Regulated 3-V or 3.3-V Output Voltage
- Up to 20-mA Output Current
- High Power Conversion Efficiency (up to 90%) Over a Wide Output Current Range, Optimized for 1.2-V Battery Voltage
- Additional Output With 2 Times V_{IN} (OUT1)
- Device Quiescent Current Less Than 35 µA
- Supervisor Included; Open Drain or Push-Pull Power Good Output
- Minimum Number of External Components
  - No Inductors Required
  - Only Five Small, 1-µF Ceramic Capacitors Required
- Load Isolated From Battery During Shutdown
- Micro-Small 10-Pin MSOP (VSSOP) Package

2 Applications

- Pagers
- Battery-Powered Toys
- Portable Measurement Instruments
- Home-Automation Products
- Medical Instruments (Like Hearing Instruments)
- Metering Applications Using MSP430 Micro-Controller
- Portable Smart Card Readers

Typical Application Schematic



3 Description

The TPS6030x devices are a family of switched-voltage converters designed specifically for space-critical battery powered applications.

The TPS6030x step-up, regulated charge pumps generate a 3-V (±4%) or 3.3-V (±4%) output voltage from a 0.9-V to 1.8-V input voltage (one alkaline, NiCd, or NiMH battery).

Only five small 1-µF ceramic capacitors are required to build a complete high efficiency DC-DC charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between a 3× or 4× conversion mode.

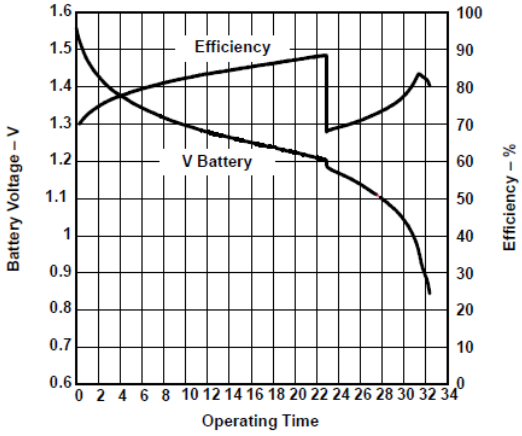
Output 1 (OUT1) can deliver a maximum of 40 mA from a 1-V input, with output 2 (OUT2) not loaded. OUT2 can deliver a maximum of 20 mA from a 1-V input, with OUT1 not loaded. Both outputs can be loaded at the same time, but the total output current of the first voltage doubler must not exceed 40 mA. For example, the load at output 1 is 20 mA and the load at output 2 is 10 mA.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
TPS60300, TPS60301, TPS60302, TPS60303	VSSOP (10)	3.05 mm × 4.98 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Alkaline Battery Operating Time



Operating time (hours) with an alkaline battery (2000 mAh) until power good goes low at I_L = 20 mA

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2001) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (continued)

The devices operate in the newly developed LinSkip mode. In this operating mode, the device switches seamlessly from the power saving, pulse-skip mode at light loads, to the low-noise, constant-frequency linear-regulation mode, when the output current exceeds the device-specific output current threshold.

A power-good function supervises the output voltage of OUT2 and can be used for power-up and power-down sequencing. Power good (PG) is offered as either open-drain or push-pull output.

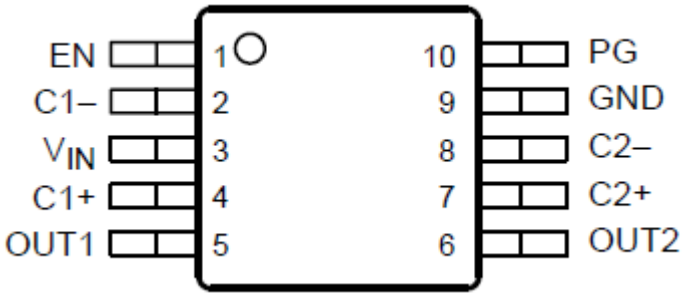
6 Device Comparison Table

PART NUMBER (1)	DGS PACKAGE MARKING	OUTPUT CURRENT 1 [mA] (2)	OUTPUT CURRENT 2 [mA] (3)	OUTPUT VOLTAGE 1 [V]	OUTPUT VOLTAGE 2 [V]	FEATURE
TPS60300DGS	ALF	40	20	$2 \times V_{IN}$	3.3	Open-drain power-good output
TPS60301DGS	ALG	40	20	$2 \times V_{IN}$	3	Open-drain power-good output
TPS60302DGS	ALI	40	20	$2 \times V_{IN}$	3.3	Push-pull power-good output
TPS60303DGS	ALK	40	20	$2 \times V_{IN}$	3	Push-pull power-good output

(1) The DGS package is available taped and reeled. Add R suffix to device type (for example, TPS60300DGSR) to order quantities of 2500 devices per reel.
(2) If OUT2 is not loaded.
(3) If OUT1 is not loaded.

7 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	4	—	Positive pin of the flying capacitor C1F
C1–	2	—	Negative pin of the flying capacitor C1F
C2+	7	—	Positive pin of the flying capacitor C2F
C2–	8	—	Negative pin of the flying capacitor C2F
EN	1	I	Device-enable input – EN = Low disables the device. Output and input are isolated in shutdown mode. – EN = High enables the device.
GND	9	—	Ground
OUT1	5	O	$2 \times V_{IN}$ power output. Bypass OUT1 to GND with the output filter capacitor $C_{(OUT1)}$.
OUT2	6	O	Regulated 3.3-V power output (TPS60300, TPS60302) or 3-V power output (TPS60301, TPS60303), respectively Bypass OUT2 to GND with the output filter capacitor $C_{(OUT2)}$.
PG	10	O	Power good detector output. As soon as the voltage on OUT2 reaches about 98% of its nominal value this pin goes high. Open-drain output on TPS60300 and TPS60301. A pull-up resistor should be connected between PG and OUT1 or OUT2. Push-pull output stage on TPS60302 and TPS60303
VIN	3	I	Supply input. Bypass V_{IN} to GND with a ≥1-µF capacitor.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Input voltage (IN to GND)(2)	–0.3	2	V
V_{OUT}	Output voltage (OUT1,OUT2, EN, PG to GND)(2)	–0.3		V
	Voltage (C1+ to GND)	–0.3		V
	Voltage (C1– to GND, C2– to GND)	–0.3		V
	Voltage (C2+ to GND)	–0.3		V
I_{OUT}	Output current (OUT1)		80	mA
I_{OUT}	Output current (OUT2)		40	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage at EN and PG can exceed IN up to the maximum rated voltage without increasing the leakage current drawn by these pins.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.9		1.8	V
$I_{OUT(OUT2)}$	Output current (OUT2)			20	mA
$I_{OUT(OUT1)}$	Output current (OUT1)			40	mA
C_{IN}	Input capacitor	1			µF
C1F, C2F	Flying capacitors		1		µF
$C_{OUT(1)}$	Output capacitor	1			µF
$C_{OUT(2)}$	Output capacitor	1			µF
T_J	Operating junction temperature	–40		125	°C

8.4 Thermal Information

THERMAL METRIC[1]		TPS6030x DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	156.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

8.5 Electrical Characteristics

C_{IN} = C1F = C2F = $C_{(OUT1)}$ = $C_{(OUT2)}$ = 1 µF, T_C = –40°C to 85°C, V_{IN} = 1 V, $V_{(EN)}$ = V_{IN} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage range			0.9		1.8	V
$I_{OUT(OUT1)}$	Maximum output current for TPS60300, TPS60302		V_{IN} ≥ 1.1 V, $I_{OUT(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	40			mA
			V_{IN} = 0.9 V, $I_{OUT(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	20			
$I_{OUT(OUT2)}$			V_{IN} ≥ 1.1 V, $I_{OUT(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	20			mA
			V_{IN} = 0.9 V, $I_{OUT(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	10			
$I_{OUT(OUT1)}$	Maximum output current for TPS60301, TPS60303		V_{IN} ≥ 1.1 V, $I_{OUT(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	40			mA
			V_{IN} = 0.9 V, $I_{OUT(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	20			
$I_{OUT(OUT2)}$			V_{IN} ≥ 1 V, $I_{OUT(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	20			mA
			V_{IN} = 0.9 V, $I_{OUT(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA	12			
$V_{OUT(OUT2)}$	Output voltage for TPS60300, TPS60302		1.1 V < V_{IN} < 1.8 V, $I_{OUT(OUT1)}$ = 0 mA, 0 < $I_{OUT(OUT2)}$ < 20 mA	3.17	3.30	3.43	V
			0.9 V < V_{IN} < 1.1 V, $I_{OUT(OUT1)}$ = 0 mA, $I_{OUT(OUT2)}$ < 10 mA	3.17	3.30	3.43	
$V_{OUT(OUT2)}$	Output voltage for TPS60301, TPS60303		1.0 V < V_{IN} < 1.8 V, $I_{OUT(OUT1)}$ = 0 mA, 0 < $I_{OUT(OUT2)}$ < 20 mA	2.88	3	3.12	V
			V_{IN} > 1.65 V, $I_{OUT(OUT1)}$ = 0 mA, 25 µA < $I_{OUT(OUT2)}$ < 20 mA	2.88	3	3.15	
V_{P-P}	Output voltage ripple	OUT2	$I_{OUT(OUT2)}$ = 20 mA, $I_{OUT(OUT1)}$ = 0 mA		20		mV_{P-P}
		OUT1	$I_{OUT(OUT1)}$ = 40 mA, $I_{OUT(OUT2)}$ = 0 mA		40		
I_Q	Quiescent current (no-load input current)		$I_{OUT(OUT)}$ = 0 mA, V_{IN} = 1.8 V		35	70	µA
$I_{(SD)}$	Shutdown supply current		V_{IN} = 1.8 V, $V_{(EN)}$ = 0 V[1]		0.05	2.5	µA
			V_{IN} = 1.8 V, $V_{(EN)}$ = 0 V, T_C = 25°C[1]			0.5	
f_{OSC}	Internal switching frequency			470	700	900	kHz
$V_{IL(EN)}$	EN input low voltage		V_{IN} = 0.9 V to 1.8 V			0.3 × V_{IN}	V
$V_{IH(EN)}$	EN input high voltage		V_{IN} = 0.9 V to 1.8 V	0.7 × V_{IN}			V
I_{lkg}	EN input leakage current		$V_{(EN)}$ = 0 V or V_{IN} or $V_{OUT(OUT2)}$ or $V_{OUT(OUT1)}$	0.01	0.1		µA
	LinSkip switching threshold		V_{IN} = 1.25 V		7.5		mA

(1) OUT1 not loaded. If OUT1 is connected to GND through a resistor, leakage current will be increased.

Electrical Characteristics (continued)

C_{IN} = C1F = C2F = $C_{(OUT1)}$ = $C_{(OUT2)}$ = 1 µF, T_C = –40°C to 85°C, V_{IN} = 1 V, $V_{(EN)}$ = V_{IN} (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Short circuit current		V_{IN} = 1.8 V	$V_{OUT(OUT2)}$ = 0 V	5	20	50	mA
				$V_{OUT(OUT1)}$ = 0 V	2	80	150	
	Output leakage current	OUT2	$V_{O(OUT1)}$ = 3 V, $V_{OUT(OUT2)}$ = nominal, EN = 0 V				1	µA
	Output load regulation		V_{IN} = 1.25 V, T_C = 25°C, 2 mA < $I_{OUT(OUT2)}$ < 20 mA			0.1		%/mA
	Output line regulation		1 V < V_{IN} < 1.65 V; T_C = 25°C, $I_{OUT(OUT)}$ = 10 mA			0.75		%/V
	No-load start-up time					400		µs
	Impedance of first charge pump stage					4		Ω
	Start-up performance at OUT2 (minimum start-up load resistance)		V_{IN} ≥ 1.1 V		165			Ω
			V_{IN} ≥ 1 V		330			
			V_{IN} = 0.9 V		1000			
	Start-up performance at OUT1 (minimum start-up load resistance)		V_{IN} = 1 V		500			Ω
FOR POWER GOOD COMPARATOR:								
$V_{(PG)}$	Power good trip voltage		V_{OUT} ramping positive			V_{OUT} – 2%	V_{OUT}	V
V_{hys}	Power good trip voltage hysteresis		V_{OUT} ramping negative			10%		
V_{OL}	Power good output voltage low		V_{OUT} = 0 V, $I_{(PG)}$ = 1.6 mA				0.3	V
I_{lkg}	Power good leakage current	TPS60300	V_{OUT} = 3.3 V, $V_{(PG)}$ = 3.3 V			0.01	0.1	
		TPS60301	V_{OUT} = 3 V, $V_{(PG)}$ = 3 V			0.01	0.1	µA
V_{OH}	Power good output voltage high	TPS60303	$I_{(PG)}$ = –5 mA		3			V
		TPS60302			2.7			
$I_{OUT(PG,0)}$	Output current at power good (sink)	All devices	$V_{(PG)}$ = 0 V		1.6			mA
$R_{(PG,1)}$	Output resistance at power good	TPS60302, TPS60303	$V_{(PG)}$ = $V_{O(OUT2)}$			15		Ω
$R_{(PG,0)}$		All devices	$V_{(PG)}$ = 0 V			100		Ω

8.6 Typical Characteristics

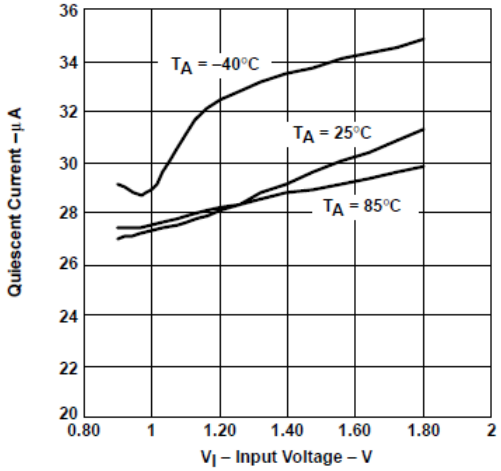


Figure 1. TPS6030x Quiescent Current vs Input Voltage

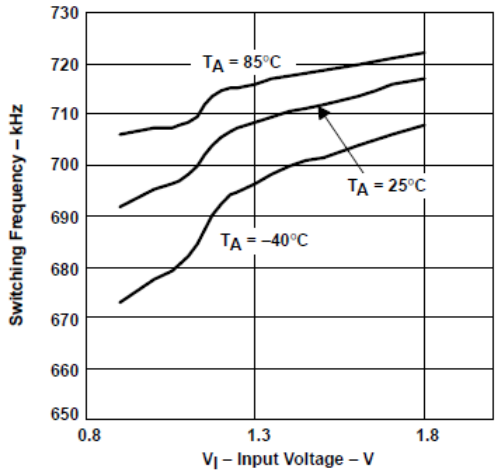


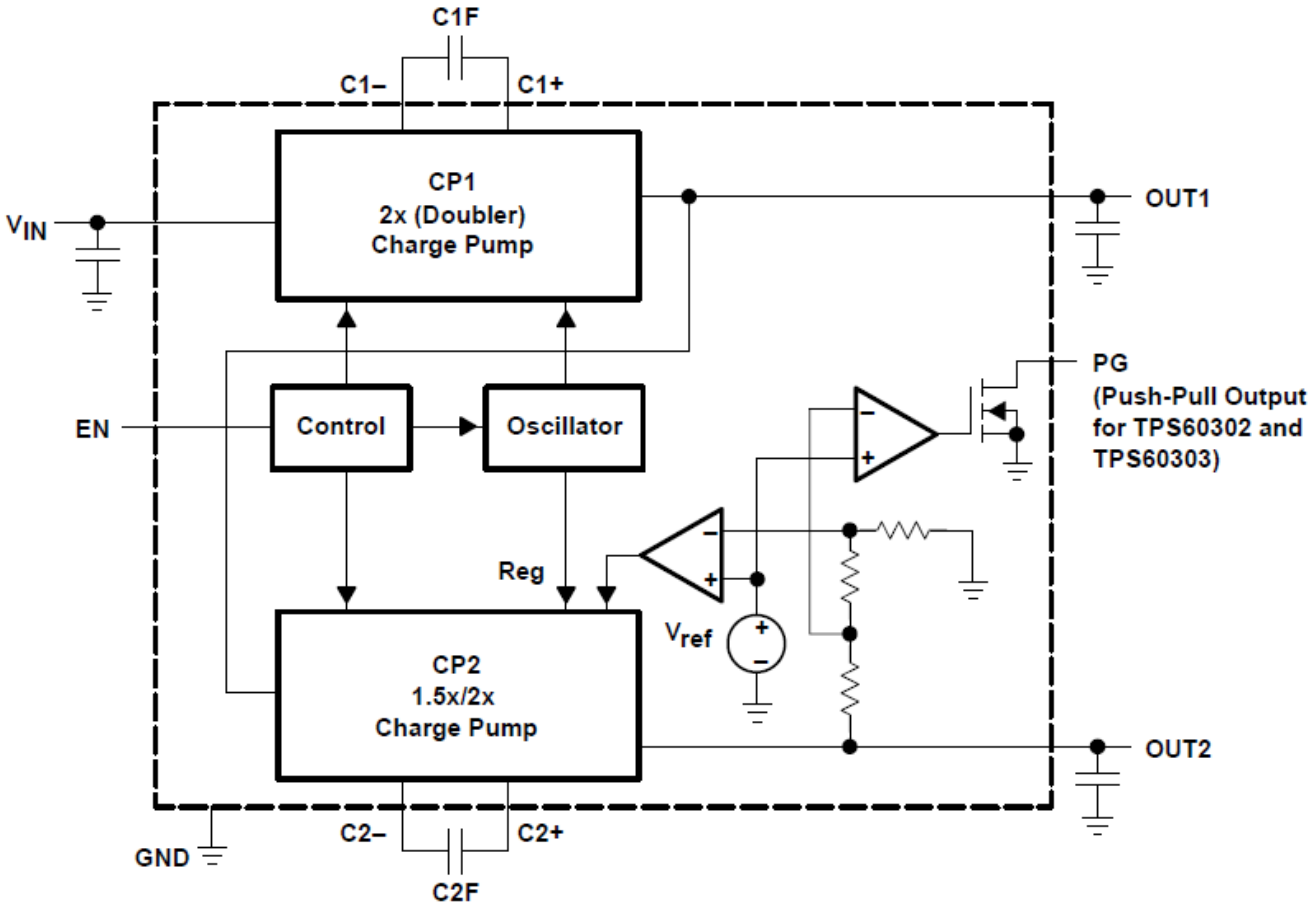
Figure 2. Switching Frequency vs Input Voltage

9 Detailed Description

9.1 Overview

The TPS6030x charge pumps are voltage quadruplers that provide a regulated 3.3-V or 3-V output from a 0.9-V to 1.8-V input. They deliver a maximum load current of 20 mA. Designed specifically for space critical battery powered applications, the complete converter requires only five external capacitors and enables the design to use low-cost, small-sized, 1-µF ceramic capacitors. The TPS6030x circuits consist of an oscillator, a voltage reference, an internal resistive feedback circuit, an error amplifier, two charge pump stages with MOSFET switches, a shutdown and start-up circuit, and a control circuit.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Good Detector

The power-good output is an open-drain output on the TPS60300 and TPS60301 or a push-pull output on the TPS60302 and TPS60303. The PG-output pulls low when the output of OUT2 is out of regulation. When the output rises to within 98% of regulation, the power-good output goes active high. In shutdown, power-good is pulled low. In normal operation, an external pullup resistor with the TPS60300 and TPS60301 is typically used to connect the PG pin to V_{OUT}. The resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected. Output current at PG (TPS60302, TPS60303) will reduce maximum output current at OUT2.

9.4 Device Functional Modes

9.4.1 Start-up Procedure

The device is enabled when EN is set from logic low to logic high. CP1 will first enter a DC start-up mode during which the capacitor on OUT1 is charged up to about V_{IN}. After that, it starts switching to boost the voltage further up to about two times V_{IN}. CP2 will then follow and charge up the capacitor on OUT2 to about the voltage on OUT1, after that, it will also start switching and boost up the voltage to its nominal value. EN must not exceed the highest voltage applied to the device.

NOTE

During start-up with V_{OUT} = 0 V, the highest voltage is the input voltage.

9.4.2 Shutdown

Driving EN low disables the converter. This disables all internal circuits, reducing input current to only 0.05 µA. Leakage current drawn from the output pins OUT1 and OUT2 is a maximum of 1 µA. The device exits shutdown once EN is set high (see *Start-up Procedure*). The typical no-load, start-up time is 400 µs. When the device is disabled, the load is isolated from the input. This is an important feature in battery operated products because it extends the battery shelf life.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6030x is a switched capacitor voltage converter providing low noise, constant-frequency linear regulation mode. It supports regulated output voltages of 3 V and 3.3 V from a 0.9-V to 1.8-V input voltage range.

10.2 Typical Application

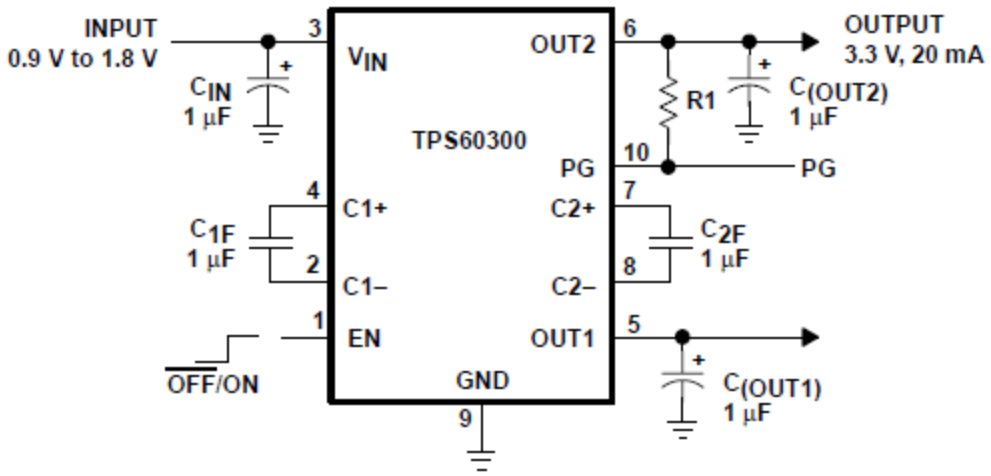


Figure 3. Typical Operating Circuit

10.2.1 Design Requirements

The complete charge pump circuitry requires no inductors and only five small 1-µF ceramic capacitors. It is possible to only use 1-µF capacitors of the same type.

Typical Application (continued)

10.2.2 Detailed Design Procedure

10.2.2.1 Capacitor Selection

The values of the five external capacitors of the TPS6030x charge pumps are closely linked to the required output current and the output noise and ripple requirements.

For the maximum output current and best performance, five ceramic capacitors with a minimum value of 1 µF are recommended. This value is necessary to assure a stable operation of the system due to the linear mode. For lower currents or higher allowed output voltage ripple, other capacitors can be used. With flying capacitors lower than 1 µF, the maximum output power will decrease. This means that the device will work in the linear mode with lower output currents.

The input capacitor improves system efficiency by reducing the input impedance and stabilizing the input current.

The minimum required capacitance of the output capacitor (C_{OUT}) that can be selected is 1 µF. Depending on the maximum allowed output ripple voltage, larger values can be chosen. Table 1 shows capacitor values recommended for low output voltage ripple operation. A recommendation is given for the smallest size.

Table 1. Recommended Capacitor Values for Low Output Voltage Ripple Operation

V_{IN} [V]	$I_{OUT(OUT2)}$ [mA]	C_{IN} [µF]	C_{XF} [µF]	C_{OUT} [µF]	V_{P-P} [mV] At 20 mA / V_{IN} = 1.1 V
		CERAMIC	CERAMIC	CERAMIC	
0.9...1.8	0...20	1	1	1	16
0.9...1.8	0...20	1	1	2.2	10
0.9...1.8	0…20	1	1	10 // 0.1	6

Table 2. Recommended Capacitors

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	805	0.1 µF	Ceramic
	LMK212BJ105KG	805	1 µF	Ceramic
	LMK212BJ225MG	805	2.2 µF	Ceramic
	JMK316BJ475KL	1206	4.7 µF	Ceramic
AVX	0805ZC105KAT2A	805	1 µF	Ceramic
	1206ZC225KAT2A	1206	2.2 µF	Ceramic

Table 3 lists the manufacturers of recommended capacitors. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 3. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t-yuden.com
AVX	X7R/X5R ceramic	www.avxcorp.com
Vishay	X7R/X5R ceramic	www.vishay.com
Kemet	X7R/X5R ceramic	www.kemet.com
TDK	X7R/X5R ceramic	www.component.tdk.com

10.2.2.2 Output Filter Design

The power-good output is capable of driving light loads up to 5 mA (see Figure 4). Therefore, the output resistance of the power-good pin, in addition with an output capacitor, can be used as an RC-filter.

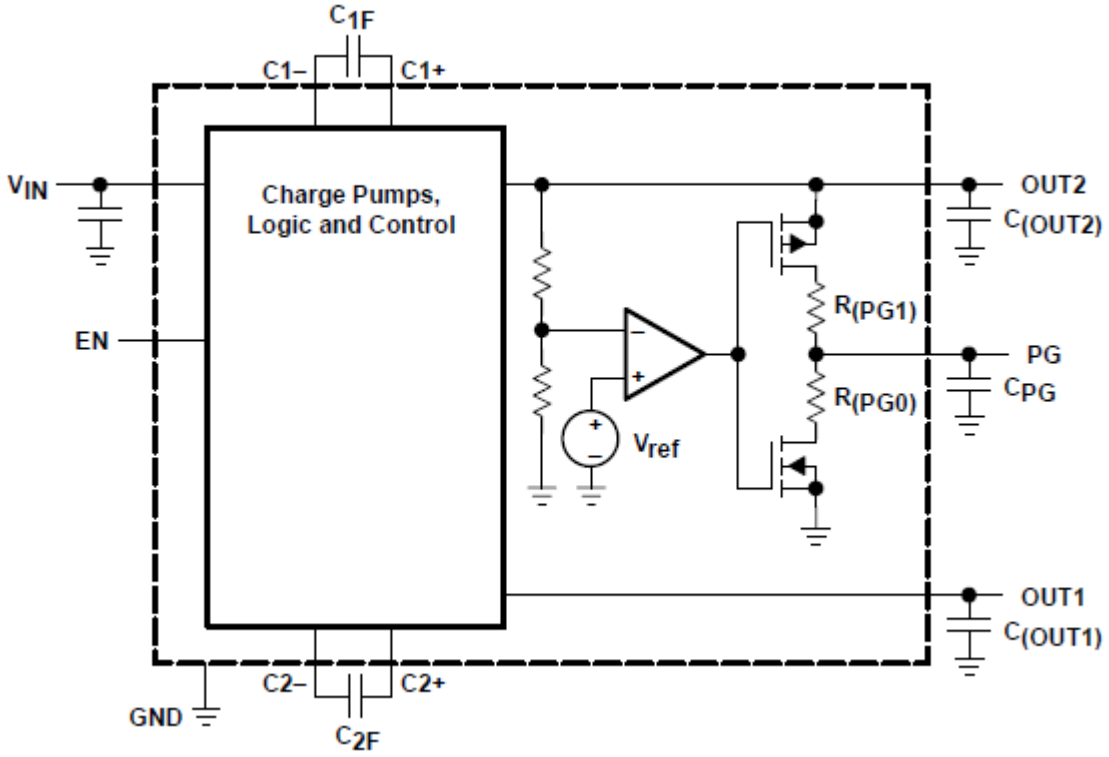


Figure 4. TPS60302, TPS60303 Push-Pull Power-Good Output-Stage as Filtered Supply

Due to $R_{(PG,1)}$, an output filter can easily be formed with an output capacitor (C_{PG}). Cut-off frequency is given by:

$$f_c = \frac{1}{2\pi R_{(PG,1)} C_{(PG)}} \quad (1)$$

and ratio V_{OUT} / V_{IN} is :

$$\left| \frac{V_{(PG,1)}}{V_{O(OUT2)}} \right| = \frac{1}{\sqrt{1 + \left(2\pi f R_{(PG,1)} C_{(PG)}\right)^2}} \quad (2)$$

with $R_{(PG,1)}$ = 15 Ω, $C_{(PG)}$ = 0.1 µF and f = 600 kHz (at nominal switching frequency)

$$\left| \frac{V_{(PG,1)}}{V_{O(OUT2)}} \right| = 0.175 \quad (3)$$

Load current sourced by power-good output reduces maximum output current at OUT2. During start-up (power good going high) current charging $C_{(PG)}$ will discharge $C_{(OUT2)}$. Therefore, $C_{(PG)}$ must not be larger than 0.1 $C_{(OUT2)}$ or the device will not start. By charging $C_{(PG)}$ through $C_{(OUT2)}$, the output voltage at OUT2 will decrease. If the capacitance of $C_{(PG)}$ is to large, the circuit will detect power bad. The power-good output will go low and discharge $C_{(PG)}$. Then the cycle starts again. Figure 5 shows a configuration with an LC-post filter to further reduce output ripple and noise.

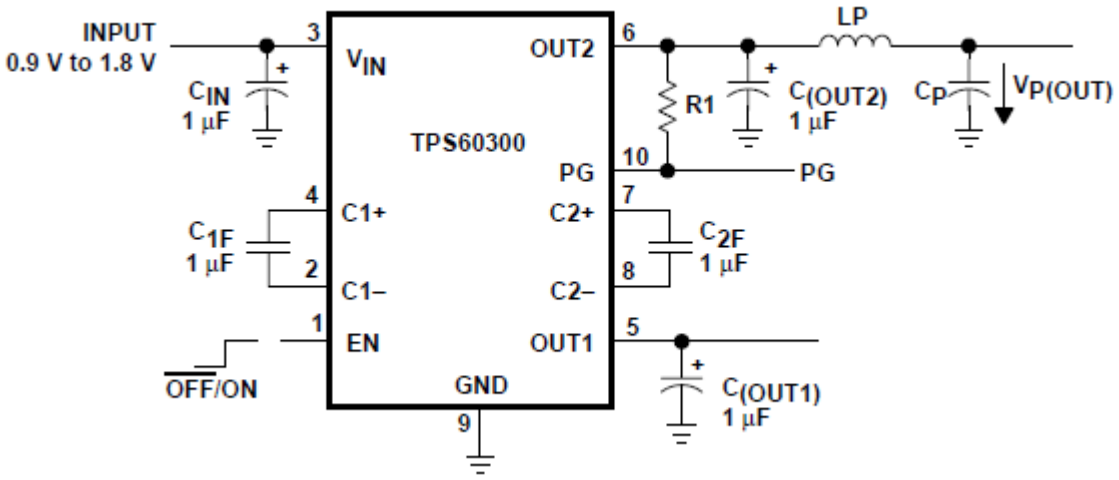


Figure 5. LC-Post Filter

Table 4. Recommended Values for Lowest Output Voltage Ripple

V_{IN} [V]	$I_{O(OUT2)}$ [mA]	C_{IN}[µF]	C_{XF}[µF]	C_{OUT}[µF]	L_P[µH]	C_P[µF]	$V_{P(OUT)}$ V_{P-P}[mV]
		CERAMIC	CERAMIC	CERAMIC		CERAMIC	
0.9...1.8	20	1	1	1	0.1	0.1 (X7R)	16
0.9...1.8	20	1	1	1	0.1	1 // 0.1 (X7R)	12
0.9...1.8	20	1	1	1	1	0.1 (X7R)	14
0.9...1.8	20	1	1	10	1	1 // 0.1 (X7R)	3

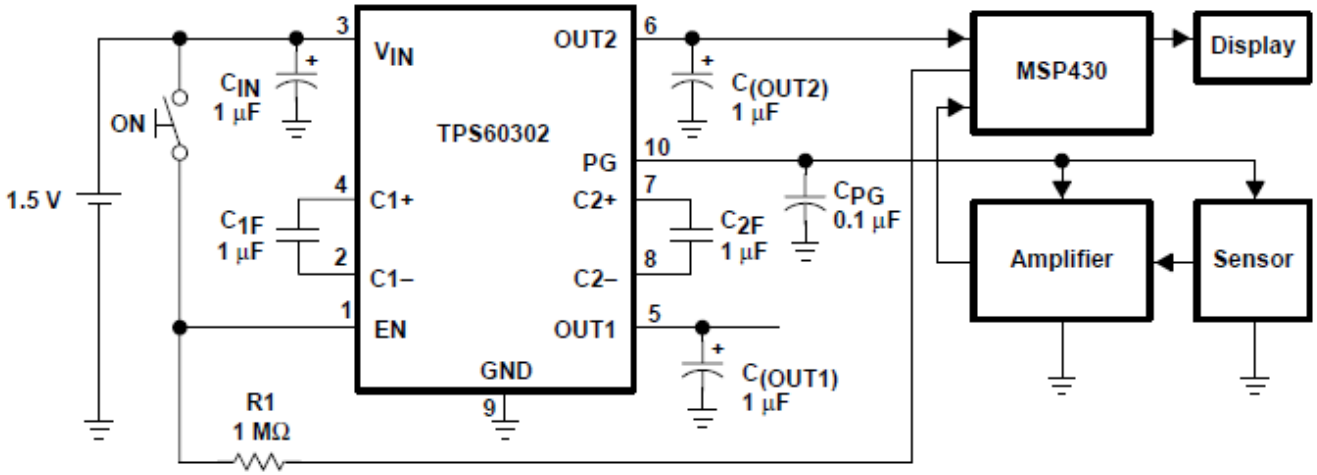


Figure 6. Application With MSP430; PG as Supply for Analog Circuits

10.2.3 Application Curves

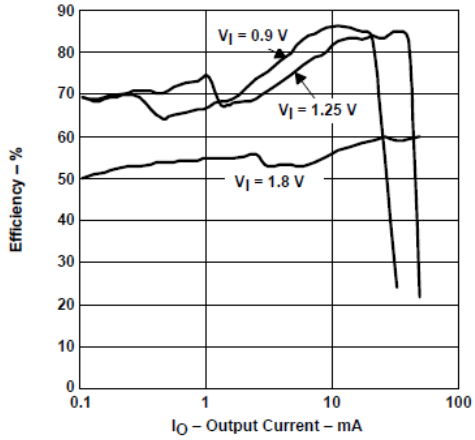


Figure 7. TPS60300, TPS60302
Efficiency vs Output Current

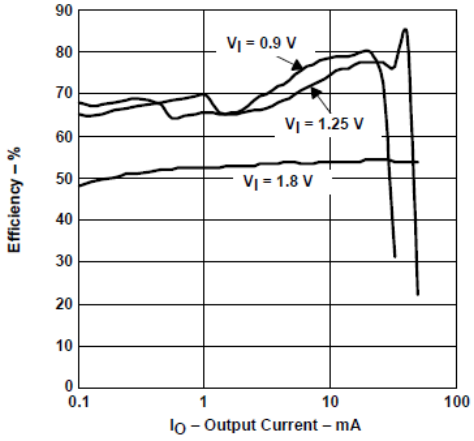


Figure 8. TPS60301, TPS60303
Efficiency vs Output Current

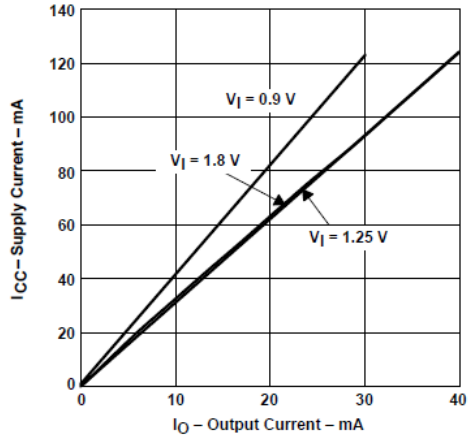


Figure 9. TPS60300
Supply Current vs Output Current

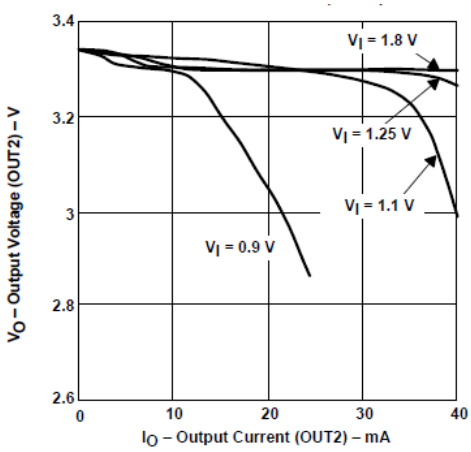


Figure 10. TPS60300, TPS60302
Output Voltage (OUT2) vs Output Current (OUT2)

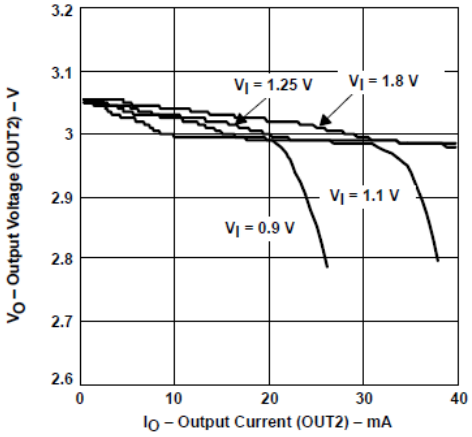


Figure 11. TPS60301, TPS60303
Output Voltage (OUT2) vs Output Current (OUT2)

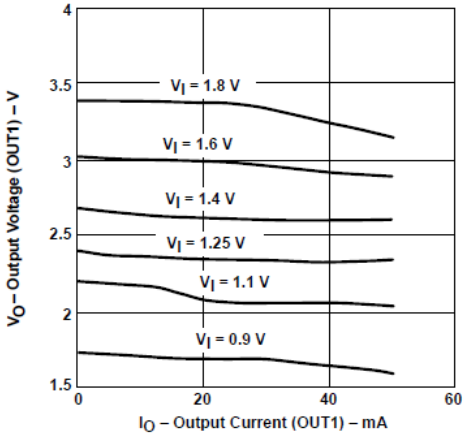


Figure 12. TPS60300, TPS60302
Output Voltage (OUT1) vs Output Current (OUT1)

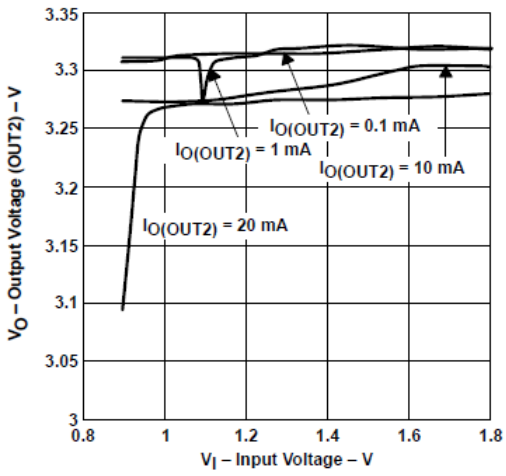


Figure 13. TPS60300, TPS60302
Output Voltage (OUT2) vs Input Voltage

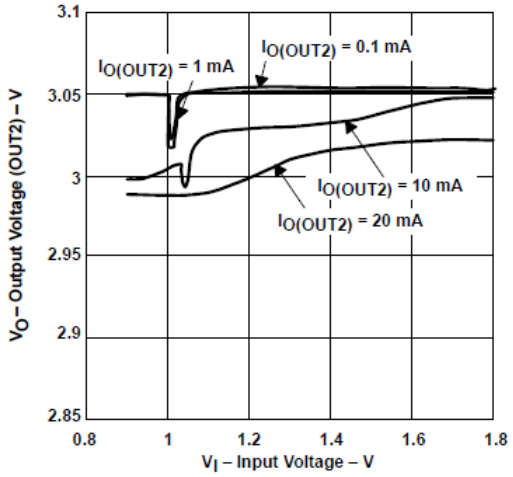


Figure 14. TPS60300, TPS60302
Output Voltage (OUT2) vs Input Voltage

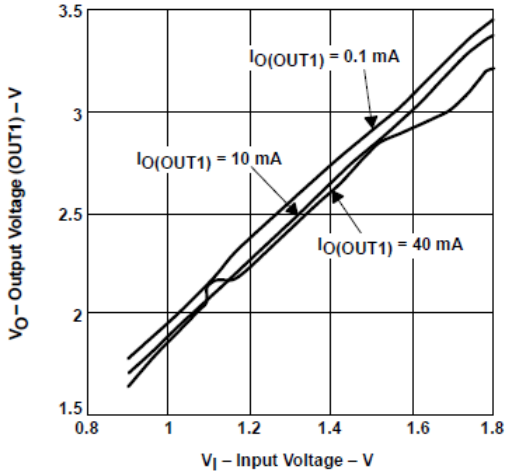


Figure 15. TPS6030x
Output Voltage (OUT1) vs Input Voltage

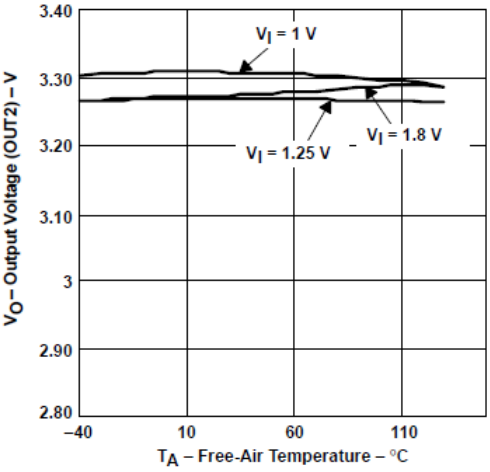


Figure 16. TPS60300, TPS60302
Output Voltage (OUT2) vs Free-Air Temperature

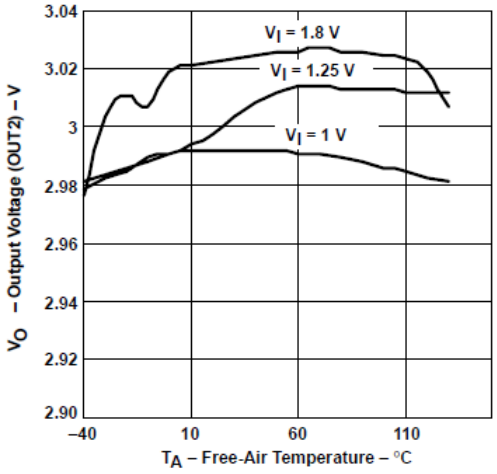


Figure 17. TPS60301, TPS60303
Output Voltage (OUT2) vs Free-Air Temperature

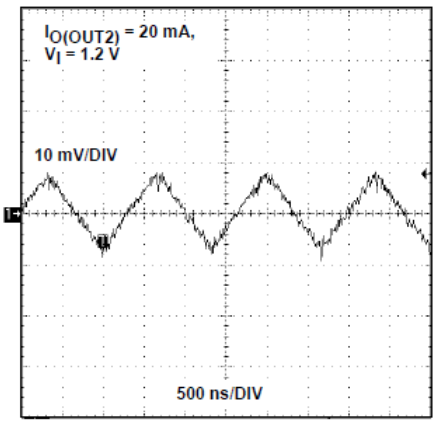


Figure 18. TPS6030x
Output Voltage Ripple (OUT2)

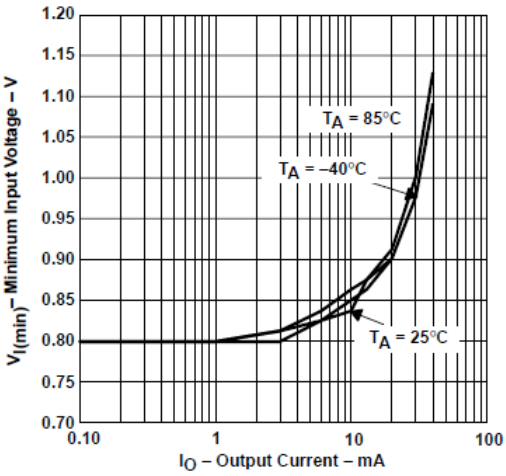


Figure 19. TPS60300, TPS60302
Minimum Input Voltage vs Output Current

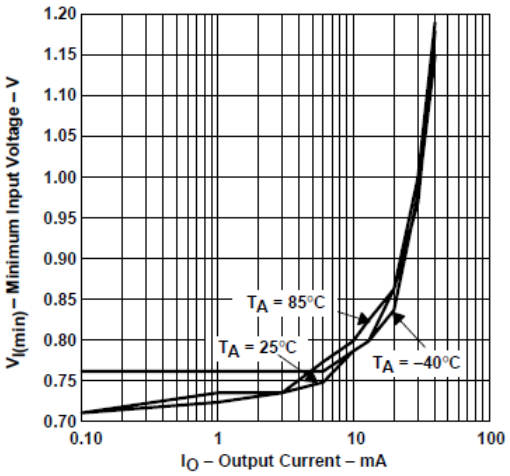


Figure 20. TPS60301, TPS60303
Minimum Input Voltage vs Output Current

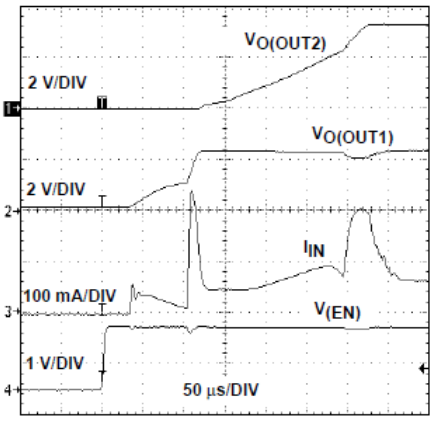


Figure 21. Start-Up Timing Enable

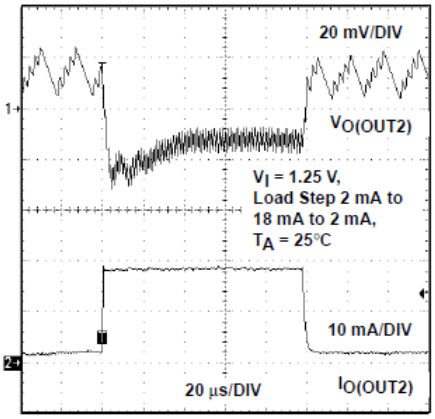


Figure 22. Load Transient Response

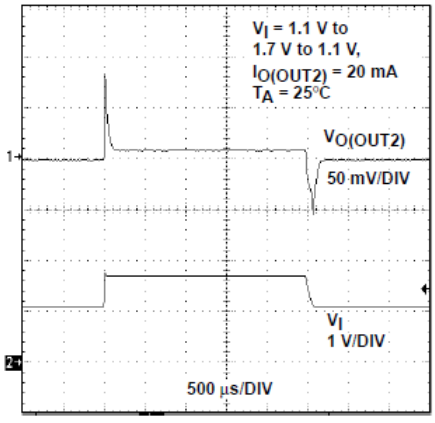


Figure 23. Line Transient Response

11 Power Supply Recommendations

The TPS6030x devices have no special requirements for their input power supply. The output currents of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS6030x.

12 Layout

12.1 Layout Guidelines

All capacitors must be soldered as close as possible to the IC. A PCB layout proposal for a two-layer board is shown in Figure 24. Care has been taken to connect all capacitors as close as possible to the circuit to achieve optimized output voltage ripple performance. The bottom layer is not shown in Figure 24. It only consists of a ground-plane with a single track between the two vias that can be seen in the left part of the top layer.

12.2 Layout Example

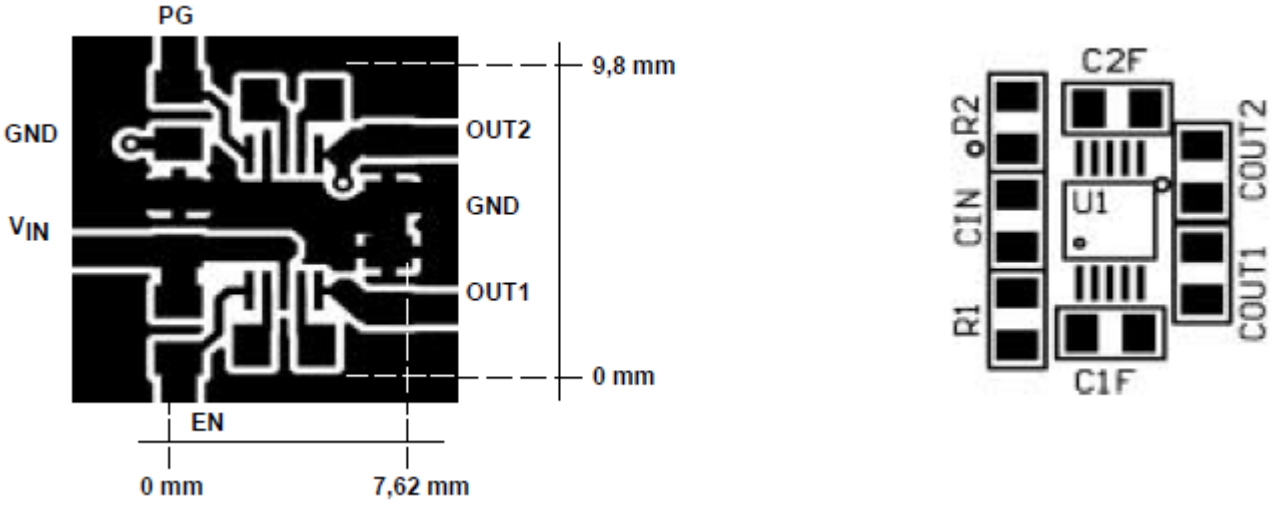


Figure 24. Recommended PCB Layout for TPS6030x (Top Layer)

12.3 Power Dissipation

The thermal resistance of the unsoldered package is $R_{\theta JA}$ = 294°C/W. Soldered on the EVM, a typical thermal resistance of $R_{\theta JA(EVM)}$ = 200°C/W was measured.

The thermal resistance can be calculated as shown in Equation 4.

$$R_{\theta JA} = \frac{T_J - T_A}{P_D}$$

where

- T_J is the junction temperature.
- T_A is the ambient temperature.
- P_D is the power that needs to be dissipated by the device. (4)

The maximum power dissipation can be calculated as shown in Equation 5.

$$P_D = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} = V_{IN(max)} \times [(3 \times I_{OUT} + I_{(SUPPLY)}] - V_{OUT} \times I_{OUT} \quad (5)$$

The maximum power dissipation happens with maximum input voltage and maximum output current:

At maximum load the supply current is approximately 2 mA.

$$P_D = 1.8\ V \times (3 \times 20\ mA + 2\ mA) - 3.3\ V \times 20\ mA = 46\ mW. \quad (6)$$

With this maximum rating and the thermal resistance of the device on the EVM, the maximum temperature rise above ambient temperature can be calculated as shown in Equation 7.

$$\Delta T_J = R_{\theta JA} \times P_D = 200°C/W \times 46\ mW = 10°C \quad (7)$$

This means that internal dissipation increases T_J by 10°C.

The junction temperature of the device must not exceed 125°C.

This means the IC can easily be used at ambient temperatures as seen in Equation 8.

$$T_A = T_{J(max)} - \Delta T_J = 125°C - 10°C = 115°C \quad (8)$$

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS60300	Click here	Click here	Click here	Click here	Click here
TPS60301	Click here	Click here	Click here	Click here	Click here
TPS60302	Click here	Click here	Click here	Click here	Click here
TPS60303	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60300DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALF	Samples
TPS60300DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALF	Samples
TPS60301DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALG	Samples
TPS60301DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALG	Samples
TPS60302DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALI	Samples
TPS60302DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALI	Samples
TPS60303DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

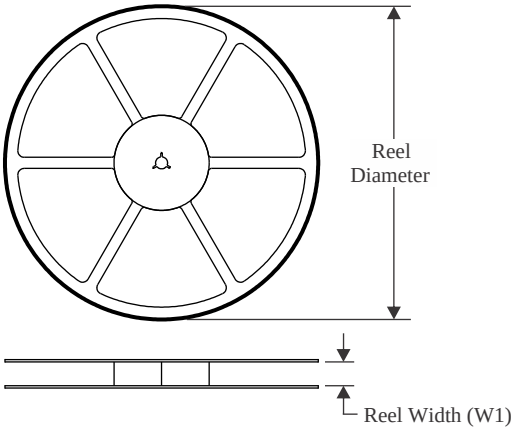
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

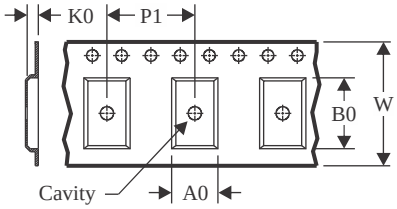
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

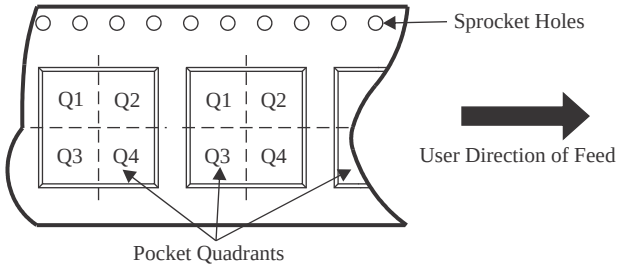


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

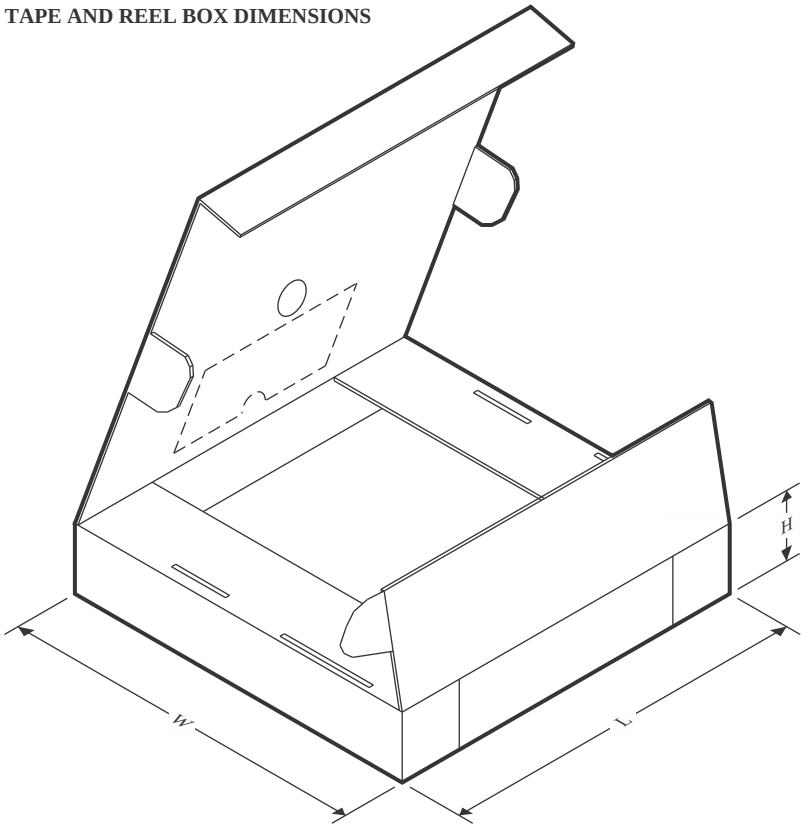
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60300DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60301DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60302DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60303DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

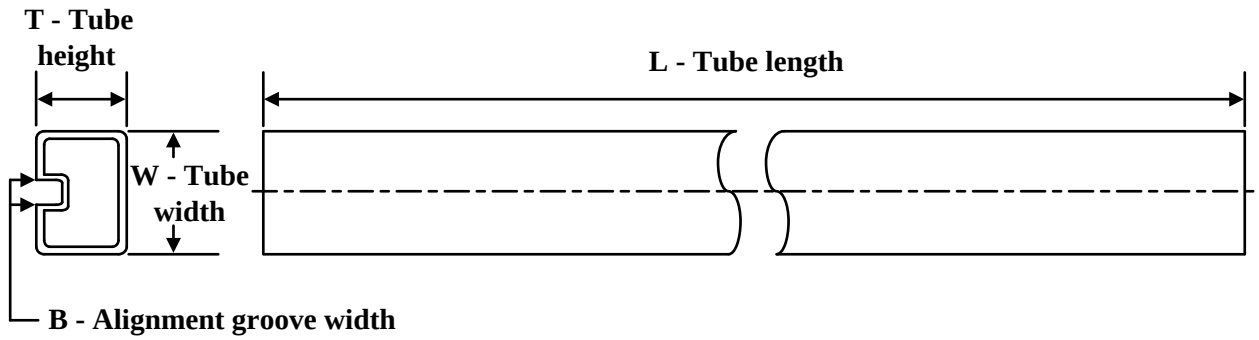
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60300DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60301DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60302DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60303DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

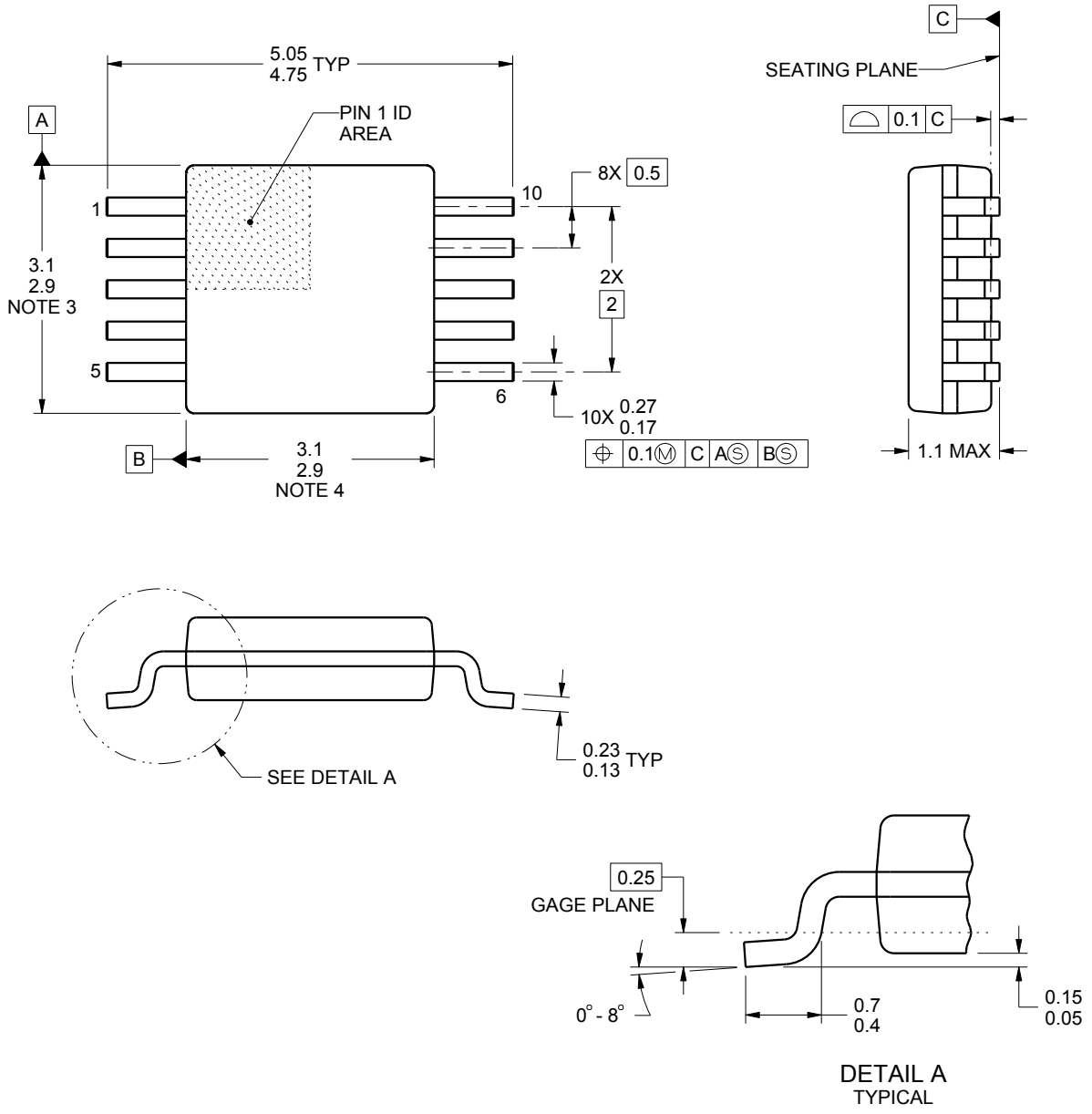
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60300DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60301DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60302DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88

PACKAGE OUTLINE

DGS0010A

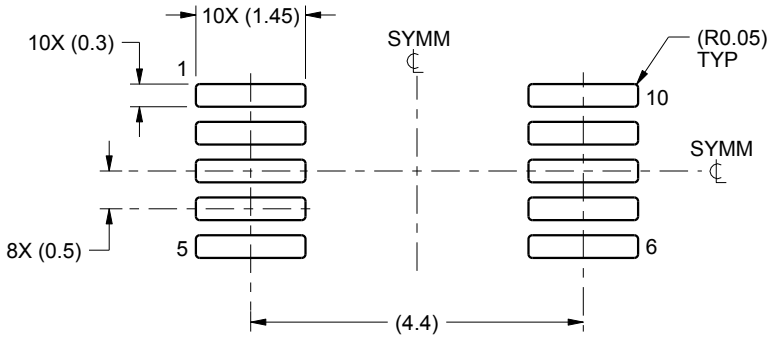
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

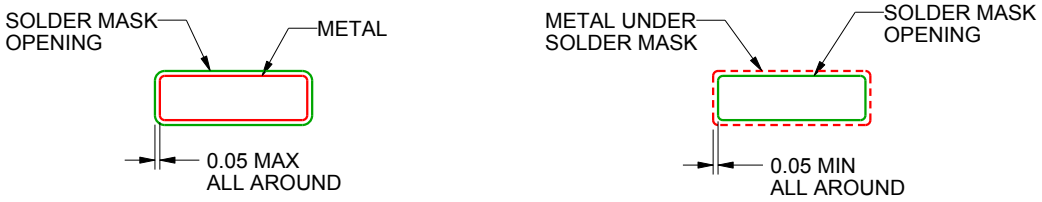


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

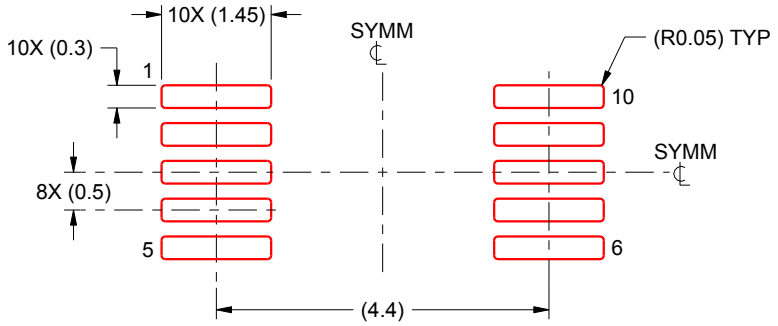


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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