TPS6103x 96% Efficient Synchronous Boost Converter With 4A Switch

1 Features

- 96% Efficient Synchronous Boost Converter With 1000-mA Output Current From 1.8-V Input
- Device Quiescent Current: 20-µA (Typ)
- Input Voltage Range: 1.8-V to 5.5-V
- Fixed and Adjustable Output Voltage Options Up to 5.5-V
- Power Save Mode for Improved Efficiency at Low Output Power
- Low Battery Comparator
- Low EMI-Converter (Integrated Antiringing Switch)
- Load Disconnect During Shutdown
- Over-Temperature Protection
- Available in a Small 4 mm x 4 mm QFN-16 or in a TSSOP-16 Package

2 Applications

All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

3 Description

The TPS6103x devices provide a power supply solution for products powered by either a one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline, NiCd or NiMH battery. The converter generates a stable output voltage that is either adjusted by an external resistor divider or fixed internally on the chip. It provides high efficient power conversion and is capable of delivering output currents up to 1 A at 5 V at a supply voltage down to 1.8 V. The implemented boost converter is based on a fixed frequency, pulse-width- modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. At low load currents the converter enters Power Save mode to maintain a high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. It can also operate synchronized to an external clock signal that is applied to the SYNC pin. The maximum peak current in the boost switch is limited to a value of 4500 mA.

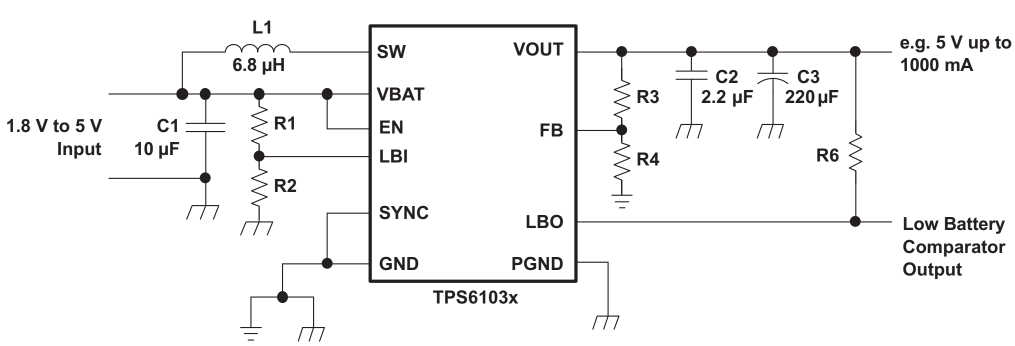
The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61030	TSSOP (16)	5.00 mm × 4.40 mm
TPS61031		
TPS61032		
TPS61030	QFN (16)	4.00 mm x 4.00 mm
TPS61031		
TPS61032		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October 2014) to Revision G	Page
• Moved T_{stg} spec to the Absolute Maximum Ratings table. Changed Handling Ratings to ESD Ratings	4
• Added *System Examples*	16

Changes from Revision E (January 2012) to Revision F	Page
• Added Device Information and Handling Rating tables, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1

Changes from Revision D (April 2004) to Revision E	Page
• Changed the temperature range From: 40°C to 85°C To: -40°C to 85°C	3

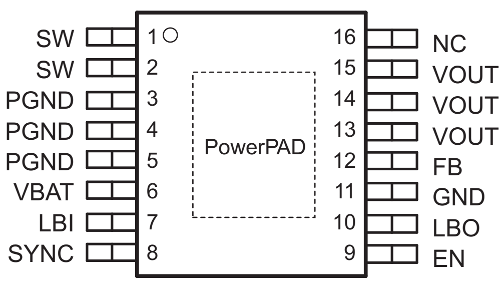
6 Device Comparison Table [1]

T_A	OUTPUT VOLTAGE DC/DC	PACKAGE	PART NUMBER [1]
-40°C to 85°C	Adjustable	16-Pin TSSOP PowerPAD™	TPS61030
	3.3 V		TPS61031
	5 V		TPS61032
	Adjustable	16-Pin QFN	TPS61030
	3.3 V		TPS61031
	5 V		TPS61032

(1) Contact the factory to check availability of other fixed output voltage versions.
(1) For all available packages, see the orderable addendum at the end of the datasheet.

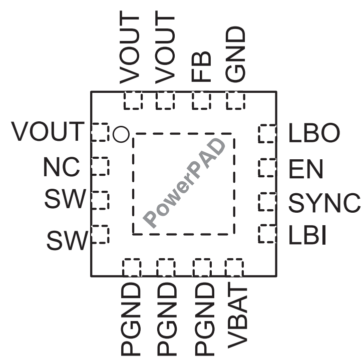
7 Pin Configuration and Functions

PWP Package
16-Pins
Top View



NC − No internal connection

RSA Package
16-Pins
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	PWP	RSA		
EN	9	11	I	Enable input. (1/VBAT enabled, 0/GND disabled)
FB	12	14	I	Voltage feedback of adjustable versions
GND	11	13	I/O	Control/logic ground
LBI	7	9	I	Low battery comparator input (comparator enabled with EN)
LBO	10	12	O	Low battery comparator output (open drain)
NC	16	2		Not connected
PGND	3, 4, 5	5, 6, 7	I/O	Power ground
PowerPAD™				Must be soldered to achieve appropriate power dissipation. Should be connected to PGND.
SYNC	8	10	I	Enable/disable power save mode (1/VBAT disabled, 0/GND enabled, clock signal for synchronization)
SW	1, 2	3, 4	I	Boost and rectifying switch input
VBAT	6	8	I	Supply voltage
VOUT	13, 14, 15	1, 15, 16	O	DC/DC output

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage on LBI	–0.3	3.6	V
	Input voltage on SW, VOUT, LBO, VBAT, SYNC, EN, FB	–0.3	7	V
T_J	Maximum junction temperature	–40	150	°C
T_{stg}	Storage temperature range	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Supply voltage at VBAT	1.8		5.5	V
T_A	Operating ambient temperature range	-40		85	°C
T_J	Operating virtual junction temperature range	-40		125	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS6103x		UNIT
		PWP	RSA	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.9	35.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.8	36.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	19.4	12.9	
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.5	
ψ_{JB}	Junction-to-board characterization parameter	19.3	12.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_I	Input voltage range			1.8		5.5	V
V_O	TPS61030 output voltage range			1.8		5.5	V
V_{FB}	TPS61030 feedback voltage			490	500	510	mV
f	Oscillator frequency			500	600	700	kHz
	Frequency range for synchronization			500		700	kHz
	Switch current limit		VOUT= 5 V	3600	4000	4500	mA
	Start-up current limit				0.4 x I_{SW}		mA
	SWN switch on resistance		VOUT= 5 V		55		mΩ
	SWP switch on resistance		VOUT= 5 V		55		mΩ
	Total accuracy			-3%		3%	
	Line regulation					0.6%	
	Load regulation					0.6%	
	Quiescent current	VBAT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT =5 V		10	25	µA
		VOUT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 5 V		10	20	µA
	Shutdown current		V_{EN}= 0 V, VBAT = 2.4 V		0.1	1	µA
CONTROL STAGE							
V_{UVLO}	Under voltage lockout threshold		V_{LBI} voltage decreasing		1.5		V
V_{IL}	LBI voltage threshold		V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis				10		mV
	LBI input current		EN = VBAT or GND		0.01	0.1	µA
	LBO output low voltage		V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	LBO output low current				100		µA
	LBO output leakage current		V_{LBO}= 7 V		0.01	0.1	µA
V_{IL}	EN, SYNC input low voltage					0.2 × VBAT	V
V_{IH}	EN, SYNC input high voltage			0.8 × VBAT			V
	EN, SYNC input current		Clamped on GND or VBAT		0.01	0.1	µA
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

8.6 Typical Characteristics

Table 1. Table Of Graphs

DC/DC CONVERTER		FIGURE
Maximum output current	vs Input voltage	Figure 1, Figure 2
Efficiency	vs Output current (TPS61030) (V_O = 2.5 V, V_I = 1.8 V, VSYNC = 0 V)	Figure 3
	vs Output current (TPS61031) (V_O = 3.3 V, V_I = 1.8 V, 2.4 V, VSYNC = 0 V)	Figure 4
	vs Output current (TPS61032) (V_O = 5.0 V, V_I = 2.4 V, 3.3 V, VSYNC = 0 V)	Figure 5
	vs Input voltage (TPS61031) (I_O = 10 mA, 100 mA, 1000 mA, VSYNC = 0 V)	Figure 6
	vs Input voltage (TPS61032) (I_O = 10 mA, 100 mA, 1000 mA, VSYNC = 0 V)	Figure 7
Output voltage	vs Output current (TPS61031) (V_I = 2.4 V)	Figure 8
	vs Output current (TPS61032) (V_I = 3.3 V)	Figure 9
No-load supply current into VBAT	vs Input voltage (TPS61032)	Figure 10
No-load supply current into VOUT	vs Input voltage (TPS61032)	Figure 11
Minimum Load Resistance at Startup	vs Input voltage (TPS61032)	Figure 12

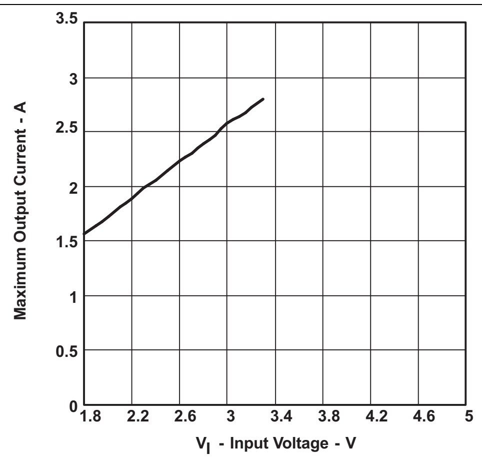


Figure 1. TPS61031 Maximum Output Current vs Input Voltage

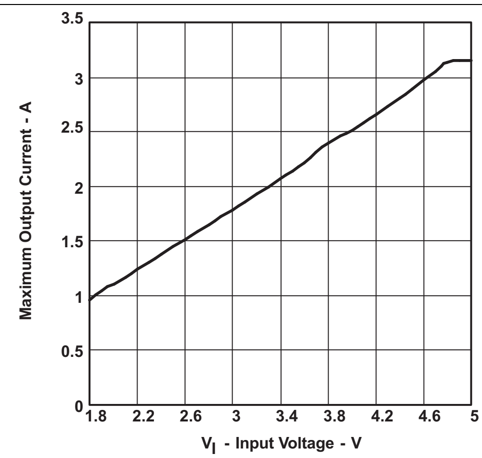
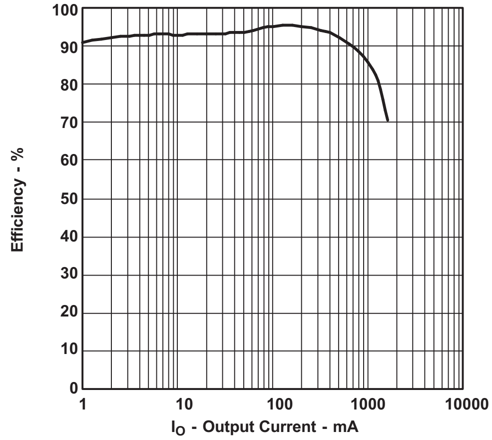
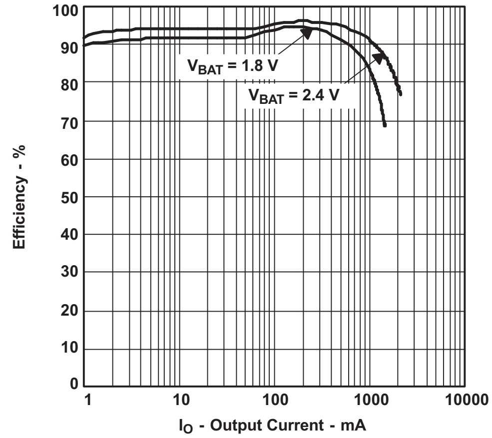


Figure 2. TPS61032 Maximum Output Current vs Input Voltage



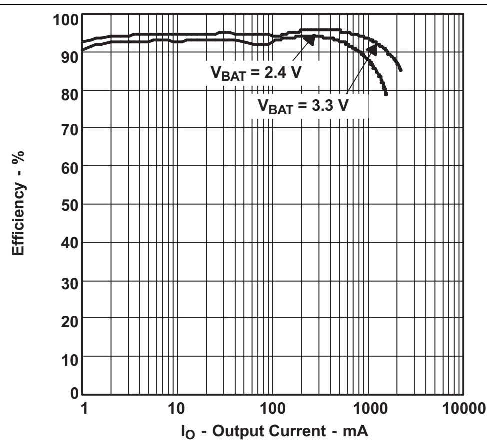
V_O = 2.5 V V_I = 1.8 V

Figure 3. TPS61030 Efficiency vs Output Current



V_O = 3.3 V

Figure 4. TPS61031 Efficiency vs Output Current



V_O = 5 V

Figure 5. Tps61032 Efficiency vs Output Current

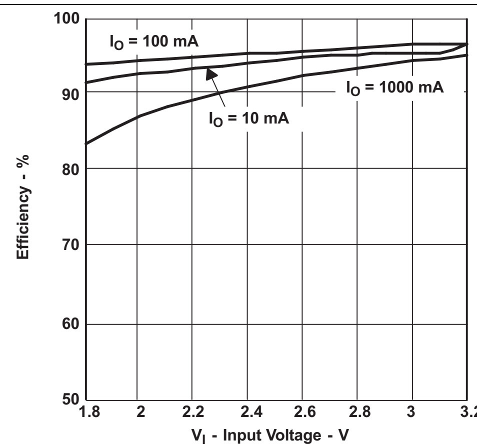


Figure 6. TPS61031 Efficiency vs Input Voltage

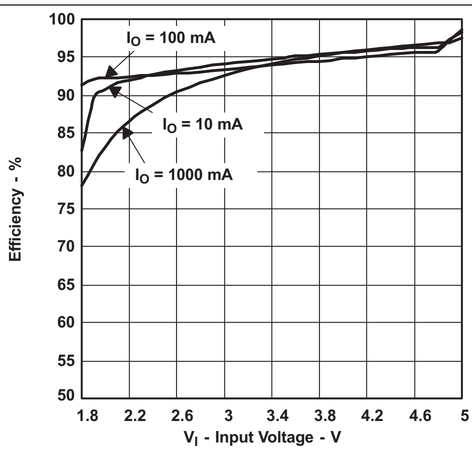
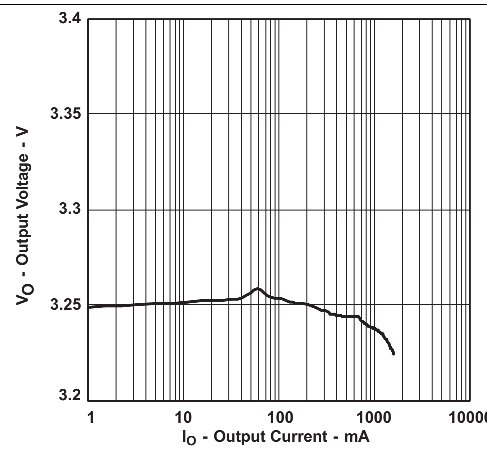
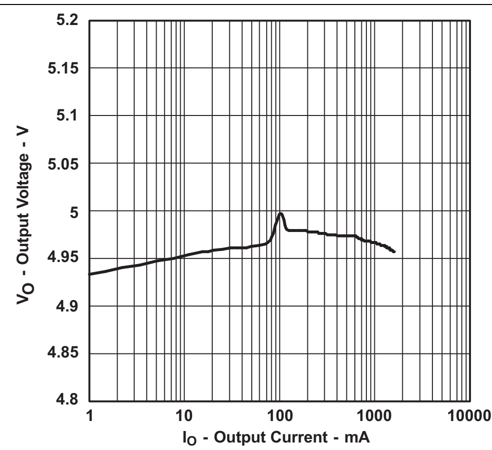


Figure 7. TPS61032 Efficiency vs Input Voltage



VBAT = 2.4 V

Figure 8. TPS61031 Output Voltage vs Output Current



VBAT = 3.3 V

Figure 9. TPS61032 Output Voltage vs Output Current

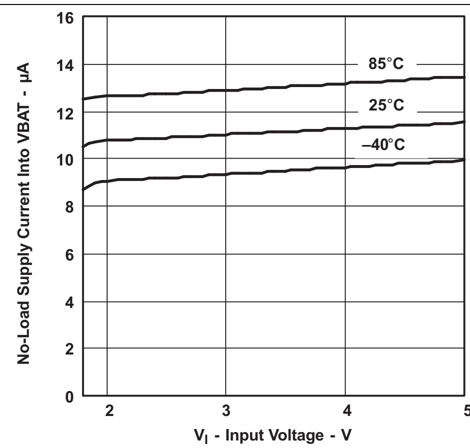


Figure 10. TPS61032 No-Load Supply Current into Vbat vs input Voltage

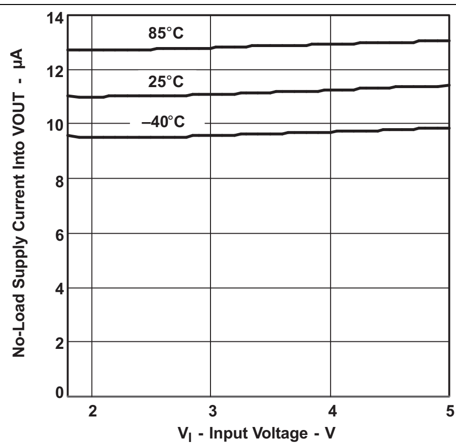


Figure 11. TPS61032 No-Load Supply Current Into Vout vs Input Voltage

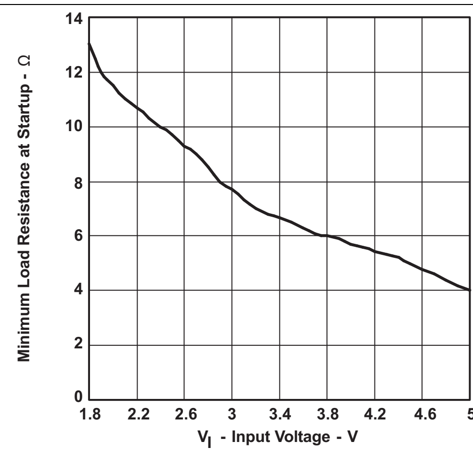
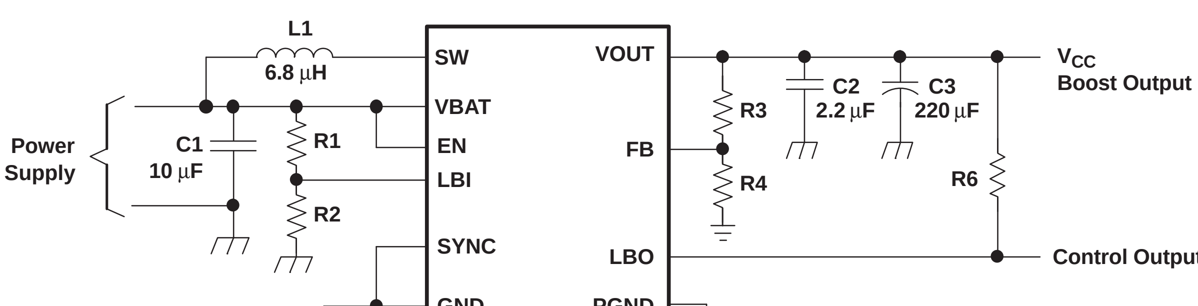


Figure 12. Minimum Load Resistance at Start-Up vs Input Voltage

9 Parameter Measurement Information



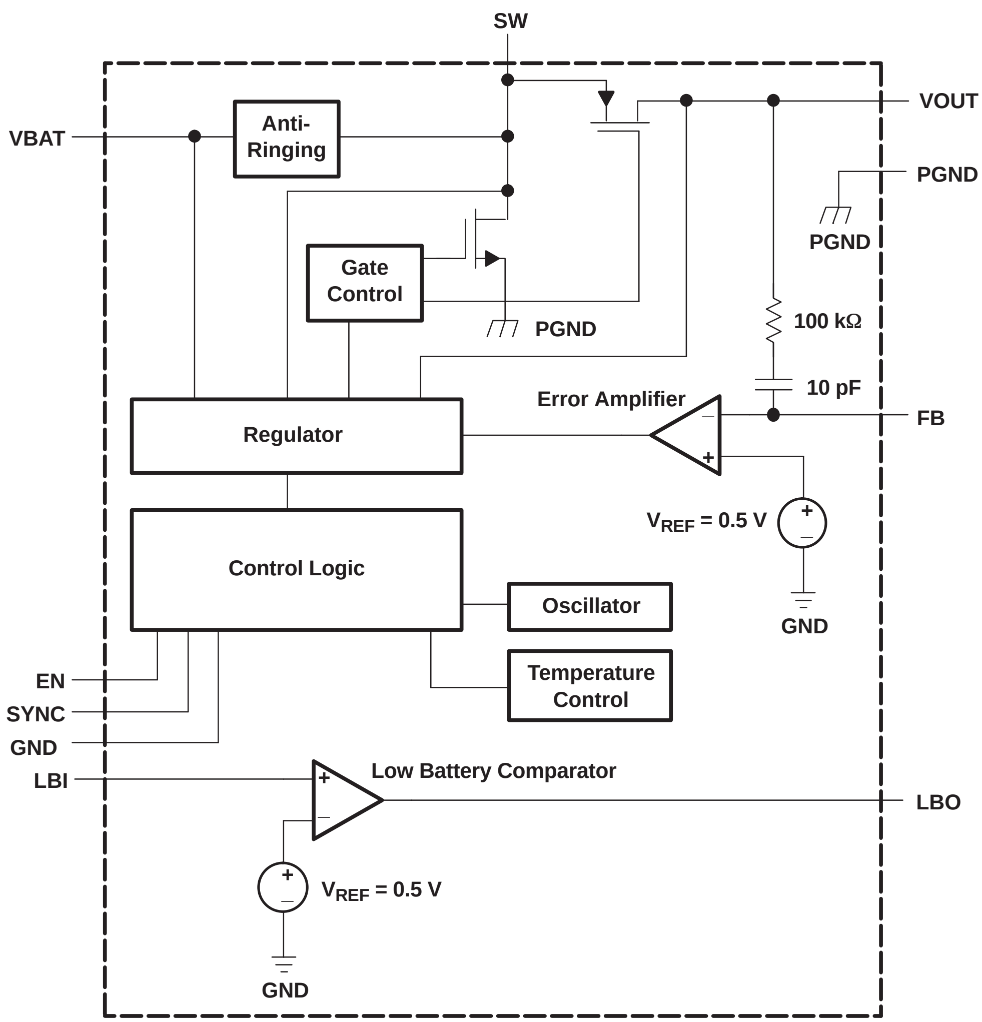
List of Components:
U1 = TPS6103xPWP
L1 = Sumida CDRH124–6R8
C1, C2 = X7R/X5R Ceramic
C3 = Low ESR Tantalum

10 Detailed Description

10.1 Overview

The TPS6103x synchronous step-up converter typically operates at a 600 kHz frequency pulse width modulation (PWM) at moderate to heavy load currents. The converter enters Power Save mode at low load currents to maintain a high efficiency over a wide load. The Power Save mode can also be disabled, forcing the converter to operate at a fixed switching frequency. The TPS6103x family is based on a fixed frequency with multiple feed forward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. It can also operate synchronized to an external clock signal that is applied to the SYNC pin. Additionally, TPS6103x integrated the low-battery detector circuit typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Controller Circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 4000 mA. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

10.3.2 Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

10.4 Device Functional Modes

10.4.1 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

10.4.1.1 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

10.4.2 Softstart

When the device enables the internal start-up cycle starts with the first step, the precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch current is limited in that phase. This also limits the output current under short-circuit conditions at the output. After charging the output capacitor to the input voltage the device starts switching. Until the output voltage is reached, the boost switch current limit is set to 40% of its nominal value to avoid high peak currents at the battery during startup. When the output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

Device Functional Modes (continued)

10.4.3 Power Save Mode And Synchronization

The SYNC pin can be used to select different operation modes. To enable power save, SYNC must be set low. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SYNC to VBAT.

Applying an external clock with a duty cycle between 30% and 70% at the SYNC pin forces the converter to operate at the applied clock frequency. The external frequency has to be in the range of about ±20% of the nominal internal frequency. Detailed values are shown in the electrical characteristic section of the data sheet.

10.4.4 Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

10.4.5 Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TPS6103x dc/dc converters are intended for systems powered by a dual or triple cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6103x is used.

11.2 Typical Application

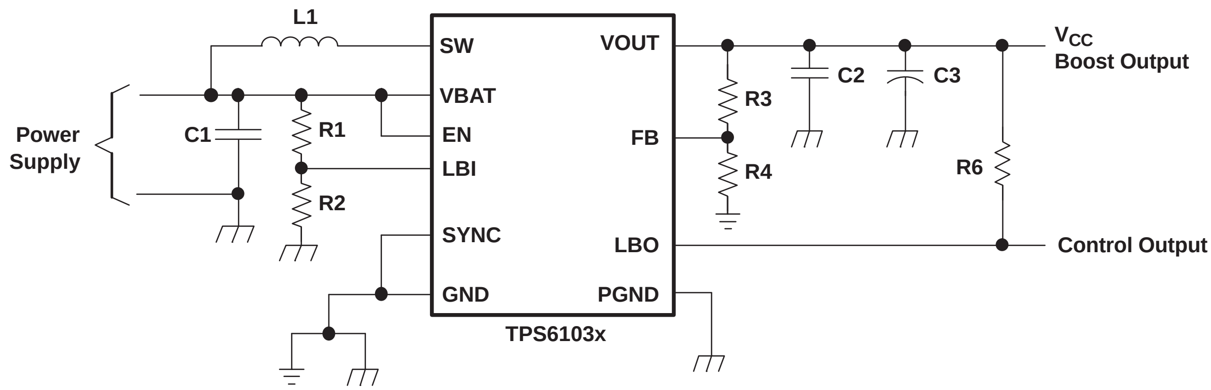


Figure 13. Typical Application Circuit For Adjustable Output Voltage Option

11.2.1 Design Requirements

Use the following typical application design procedure to select external components values for the TPS61030 device.

Table 2. TPS61030 5 V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	1.8 V to 5.5 V
Output Voltage	5.0 V
Output Voltage Ripple	+/- 3% V_{OUT}
Transient Response	+/- 10% V_{OUT}
Input Voltage Ripple	+/- 200mV
Output Current	2A
Operating Frequency	600 kHz

11.2.2 Detailed Design Procedure

11.2.2.1 Programming The Output Voltage

The output voltage of the TPS61030 dc/dc converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R4 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using equation 1:

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \tag{1}$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor should be chosen for R3. If for any reason the value for R4 is chosen significantly lower than 200 kΩ additional capacitance in parallel to R3 is recommended. The required capacitance value can be easily calculated using Equation 2:

$$C_{parR3} = 10\ pF \times \left(\frac{200\ k\Omega}{R4} - 1\right) \tag{2}$$

11.2.2.2 Programming The LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using Equation 3.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1\right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1\right) \tag{3}$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the dc/dc converter. If not used, the LBO pin can be left floating or tied to GND.

11.2.2.3 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6103x's switch is 4500 mA at an output voltage of 5 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 4:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \tag{4}$$

For example, for an output current of 1000 mA at 5 V, at least 3500 mA of average current flows through the inductor at a minimum input voltage of 1.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using Equation 5:

$$L = \frac{V_{BAT} \times \left(V_{OUT} - V_{BAT}\right)}{\Delta I_L \times f \times V_{OUT}} \tag{5}$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 10% × I_L. In this example, the desired inductor has the value of 5.5 µH. In typical applications a 6.8 µH inductance is recommended. The minimum possible inductance value is 2.2 µH. With the calculated inductance and current values, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 4. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TPS6103x converters:

Table 3. List Of Inductors(1)

VENDOR	INDUCTOR SERIES
Sumida	CDRH124
	CDRH103R
	CDRH104R
Wurth Electronik	7447779___
	744771___
EPCOS	B82464G

(1) See *Third-Party Products Disclaimer*

11.2.2.4 Capacitor Selection

11.2.2.4.1 Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

11.2.2.4.2 Output Capacitor

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 6:

$$C_{min} = \frac{I_{OUT} \times \left(V_{OUT} - V_{BAT}\right)}{f \times \Delta V \times V_{OUT}} \tag{6}$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 100 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \tag{7}$$

An additional ripple of 80 mV is the result of using a tantalum capacitor with a low ESR of 80 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 90 mV. Additional ripple is caused by load transients. This means that the output capacitance needs to be larger than calculated above to meet the total ripple requirements.

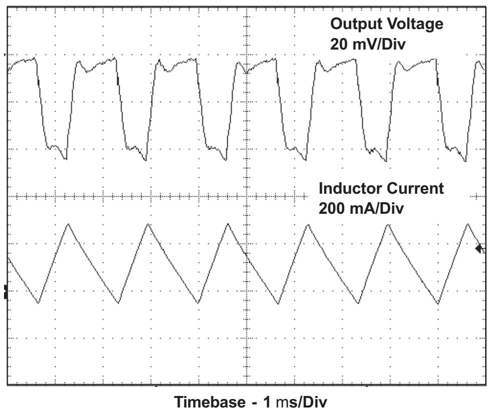
The output capacitor must completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of 100 µF and load transient considerations, a recommended output capacitance value is in around 220 µF. For economical reasons this usually is a tantalum capacitor. Because of this the control loop has been optimized for using output capacitors with an ESR of above 30 mΩ. The minimum value for the output capacitor is 22 µF.

11.2.2.4.2.1 Small Signal Stability

When using output capacitors with lower ESR, like ceramics, it is recommended to use the adjustable voltage version. The missing ESR can be easily compensated there in the feedback divider. Typically a capacitor in the range of 10 pF in parallel to R3 helps to obtain small signal stability with lowest ESR output capacitors. For more detailed analysis the small signal transfer function of the error amplifier and regulator, which is given in Equation 8, can be used.

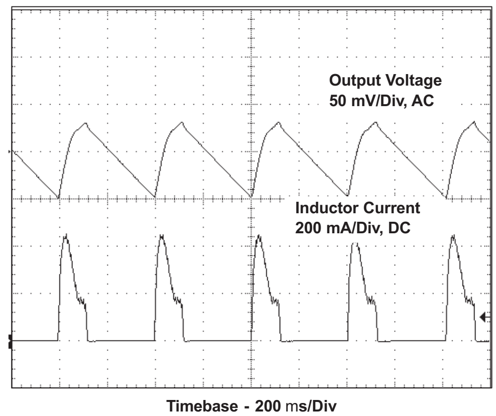
$$A_{REG} = \frac{d}{V_{FB}} = \frac{5 \times (R3 + R4)}{R4 \times (1 + i \times \omega \times 2.3\ \mu s)} \tag{8}$$

11.2.3 Application Curves



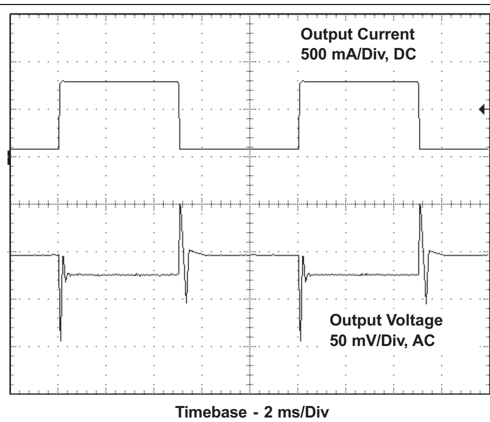
V_I = 3.3 V R_L = 5 Ω

Figure 14. TPS61030 Output Voltage in Continuous Mode



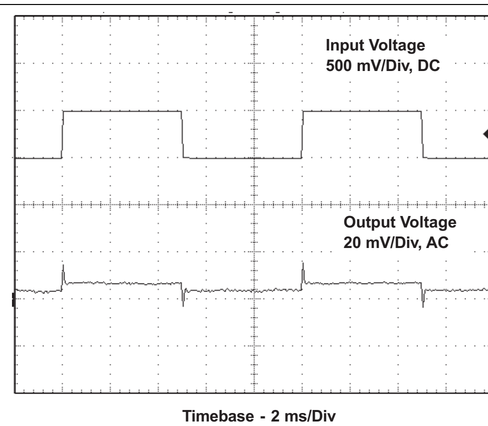
V_I = 3.3 V R_L = 100 Ω

Figure 15. TPS61030 Output Voltage in Power Save Mode



V_I = 2.5 V I_L = 80 mA to 800 mA

Figure 16. TPS61030 Load Transient Response



V_I = 2.2 V to 2.7 V R_L = 50 Ω

Figure 17. TPS61030 Line Transient Response

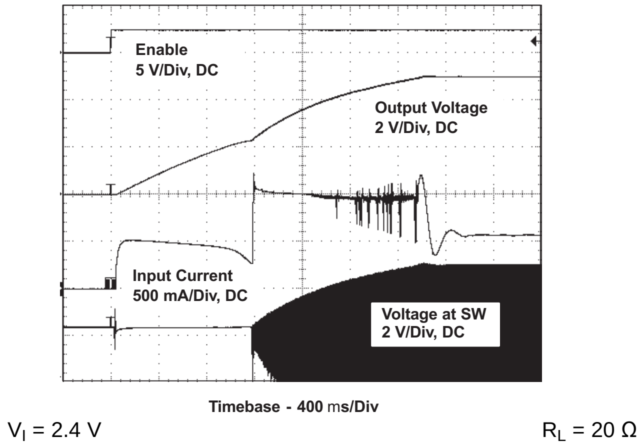


Figure 18. TPS61030 DC/DC Converter Start-Up After Enable

11.2.4 System Examples

11.2.4.1 Power Supply Solution For Maximum Output Power

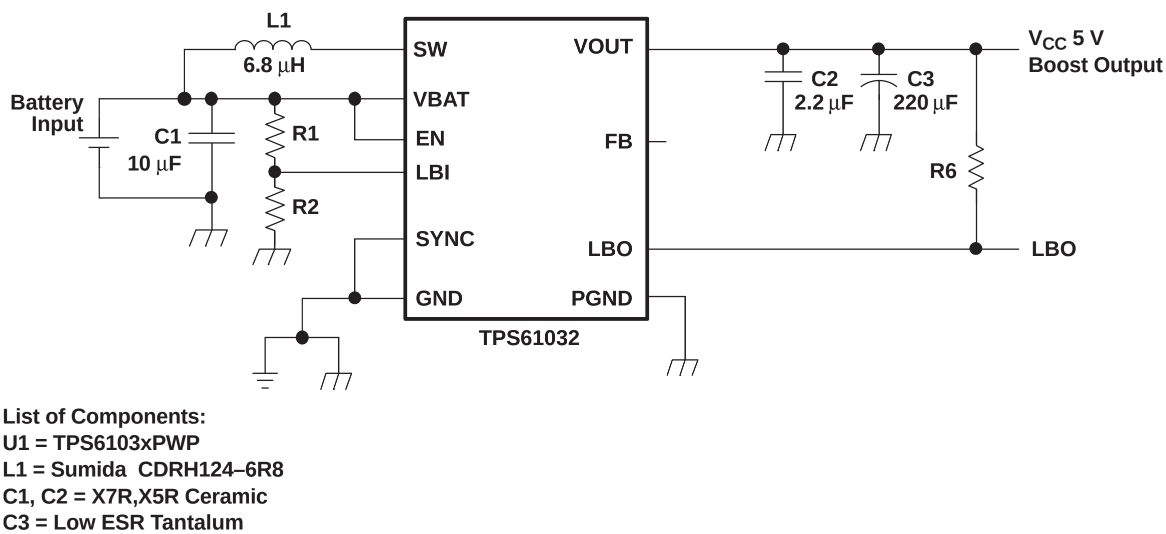


Figure 19. Power Supply Solution For Maximum Output Power

11.2.4.2 Power Supply Solution With Auxiliary Positive Output Voltage

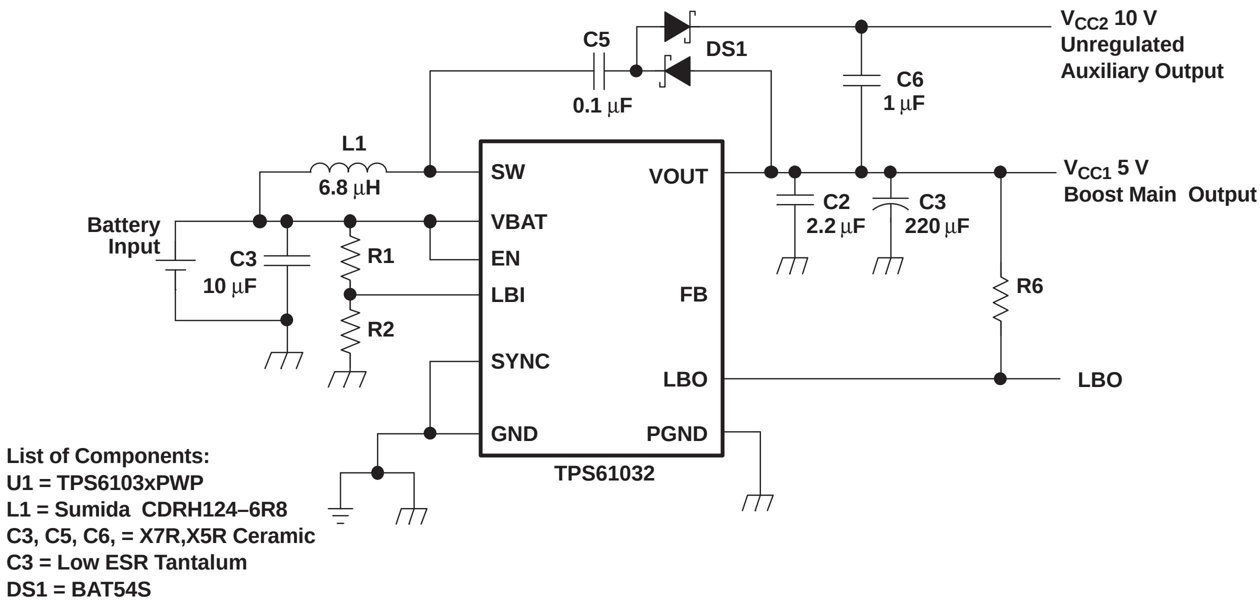


Figure 20. Power Supply Solution With Auxiliary Positive Output Voltage

11.2.4.3 Power Supply Solution with Auxiliary Negative Output Voltage

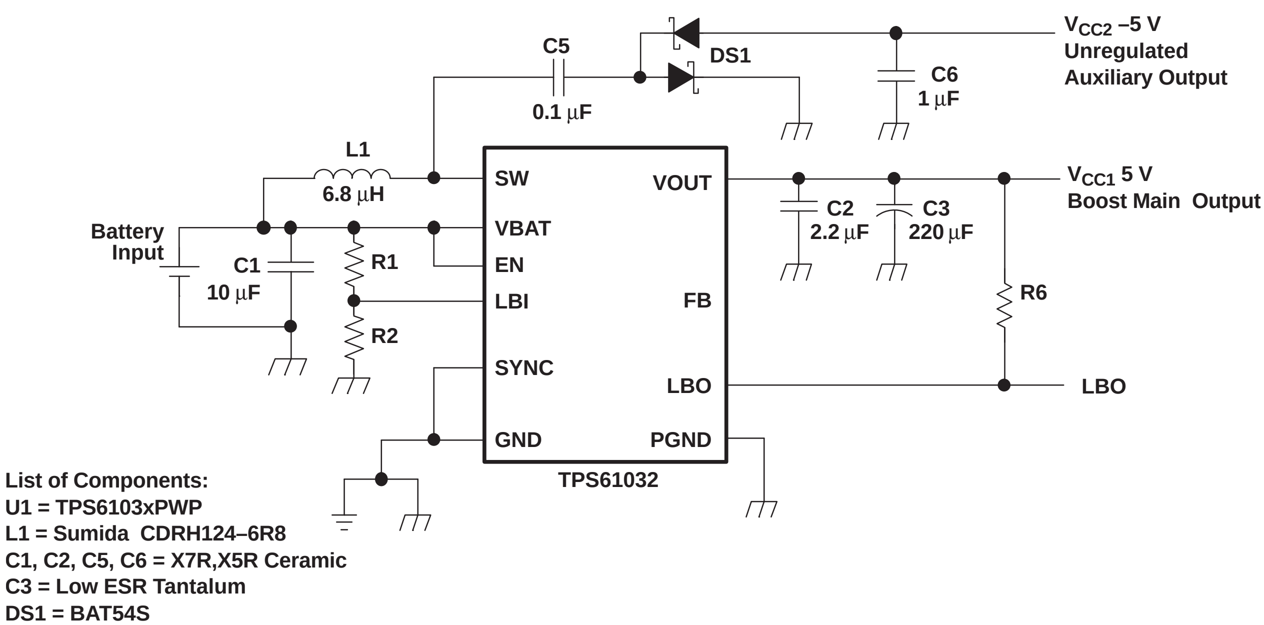


Figure 21. Power Supply Solution With Auxiliary Negative Output Voltage

12 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

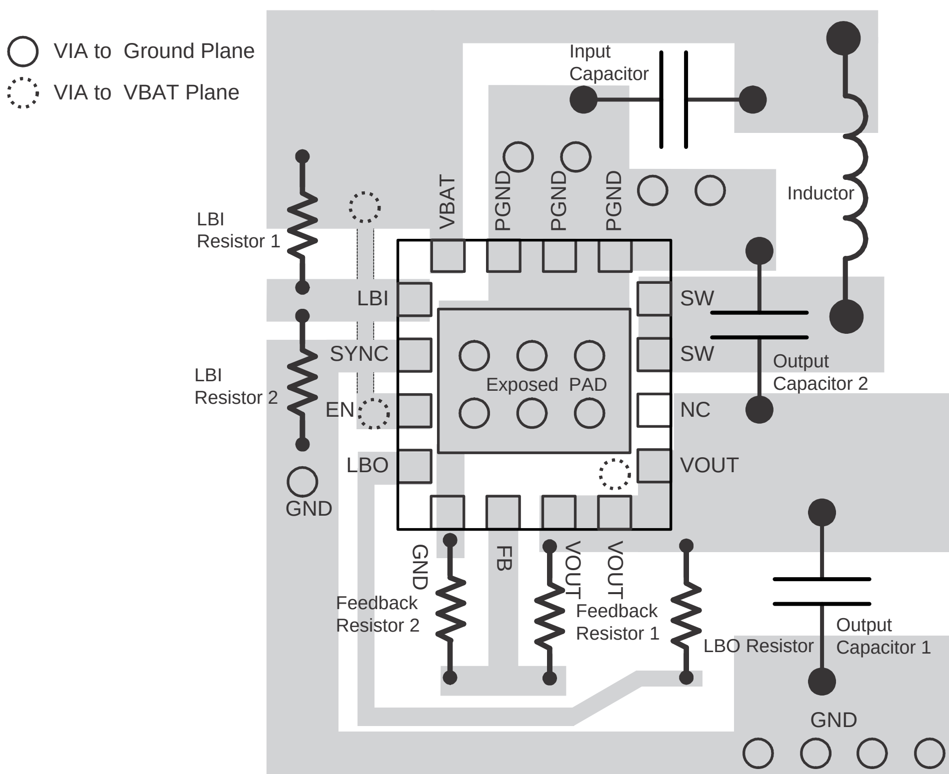
13 Layout

13.1 Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

13.2 Layout Example



13.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Thermal Considerations (continued)

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum junction temperature (T_J) of the TPS6103x devices is 125°C. The thermal resistance of the 16-pin TSSOP PowerPAD package (PWP) is $R_{\Theta JA}$ = 36.5°C/W (QFN package, RSA, 38.1°C/W), if the PowerPAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation for the PWP package is about 1096 mW, for the RSA package it is about 1050 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125°C - 85°C}{36.5°C/W} \tag{9}$$

14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

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14.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61030	Click here	Click here	Click here	Click here	Click here
TPS61031	Click here	Click here	Click here	Click here	Click here
TPS61032	Click here	Click here	Click here	Click here	Click here

14.3 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61030PWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61030
TPS61030PWP.B	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61030
TPS61030PWPG4	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61030
TPS61030PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61030
TPS61030PWPR.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61030
TPS61030PWPRG4	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS61030
TPS61030RSAR	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS6 1030
TPS61030RSAR.B	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS6 1030
TPS61030RSARG4	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS6 1030
TPS61031PWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61031
TPS61031PWP.B	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61031
TPS61031PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61031
TPS61031PWPR.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61031
TPS61031RSAR	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	TPS6 1031
TPS61031RSAR.B	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	TPS6 1031
TPS61031RSARG4	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS6 1031
TPS61031RSARG4.B	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS6 1031
TPS61032PWP	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61032
TPS61032PWP.B	Active	Production	HTSSOP (PWP) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61032
TPS61032PWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61032
TPS61032PWPR.B	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS61032
TPS61032RSAR	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS6 1032

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61032RSAR.B	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS6 1032

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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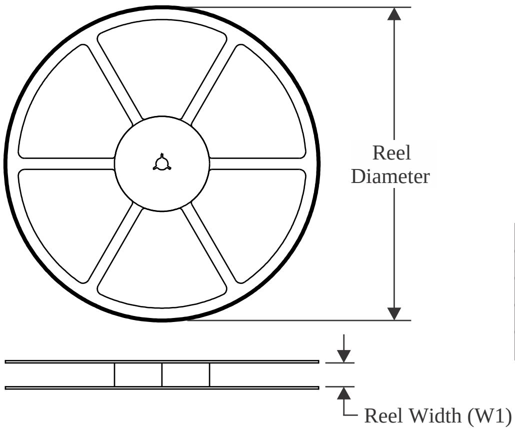
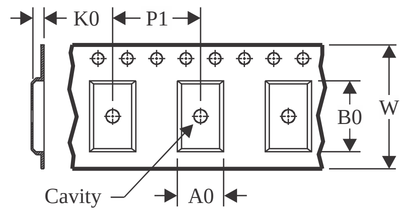
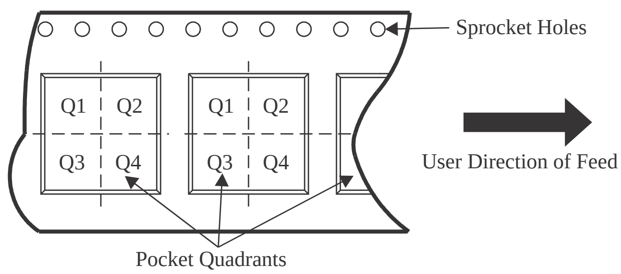
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





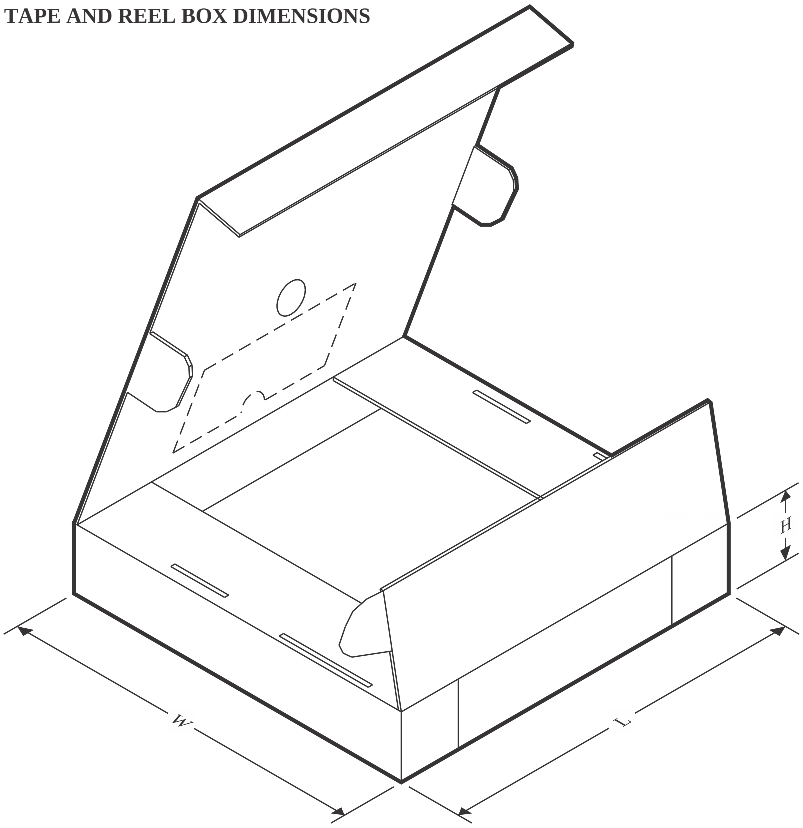
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61030PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS61031PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS61031RSARG4	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS61032PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS61032RSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

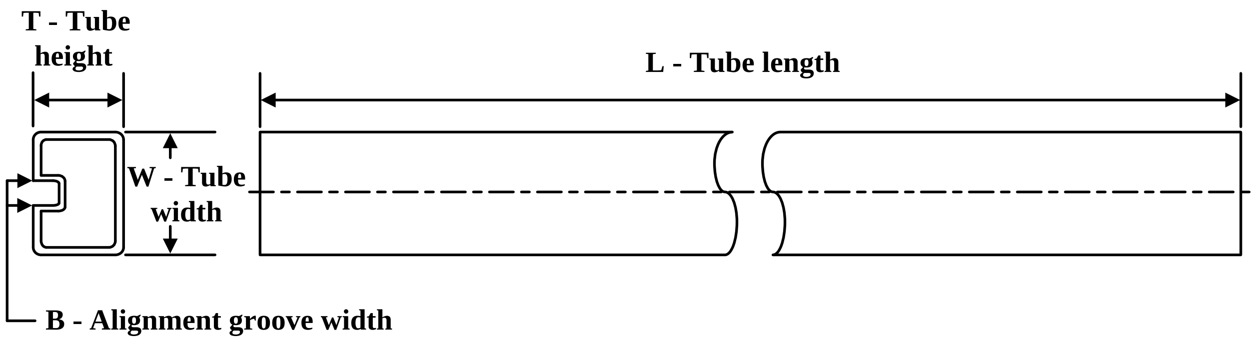
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61030PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS61031PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS61031RSARG4	QFN	RSA	16	3000	350.0	350.0	43.0
TPS61032PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS61032RSAR	QFN	RSA	16	3000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS61030PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS61030PWP.B	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS61030PWPG4	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS61031PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS61031PWP.B	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS61032PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS61032PWP.B	PWP	HTSSOP	16	90	530	10.2	3600	3.5

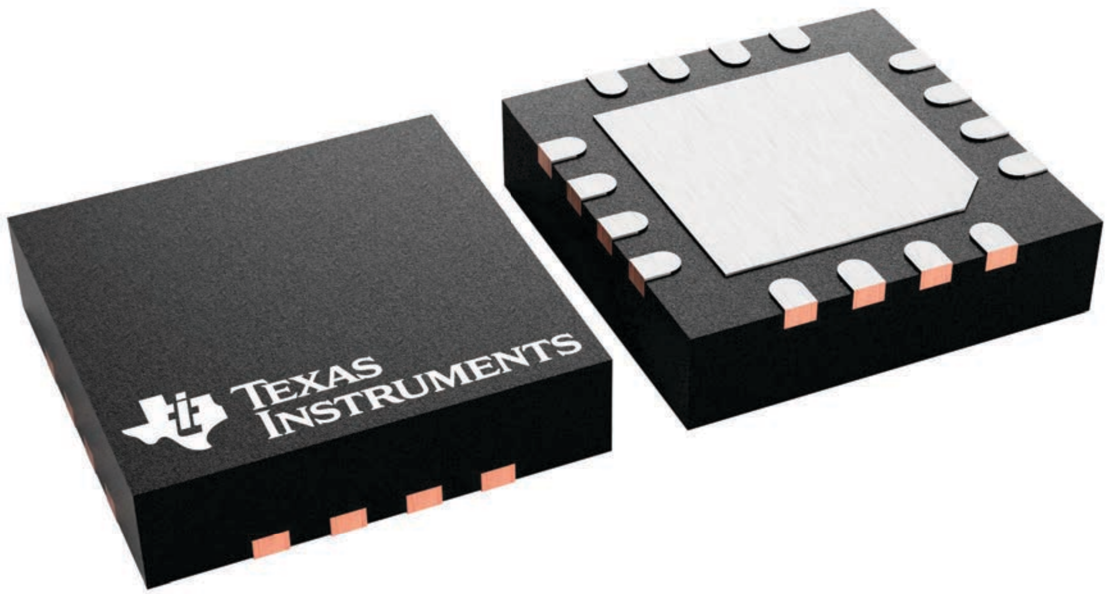
RSA 16

VQFN - 1 mm max height

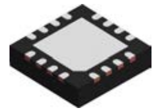
4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



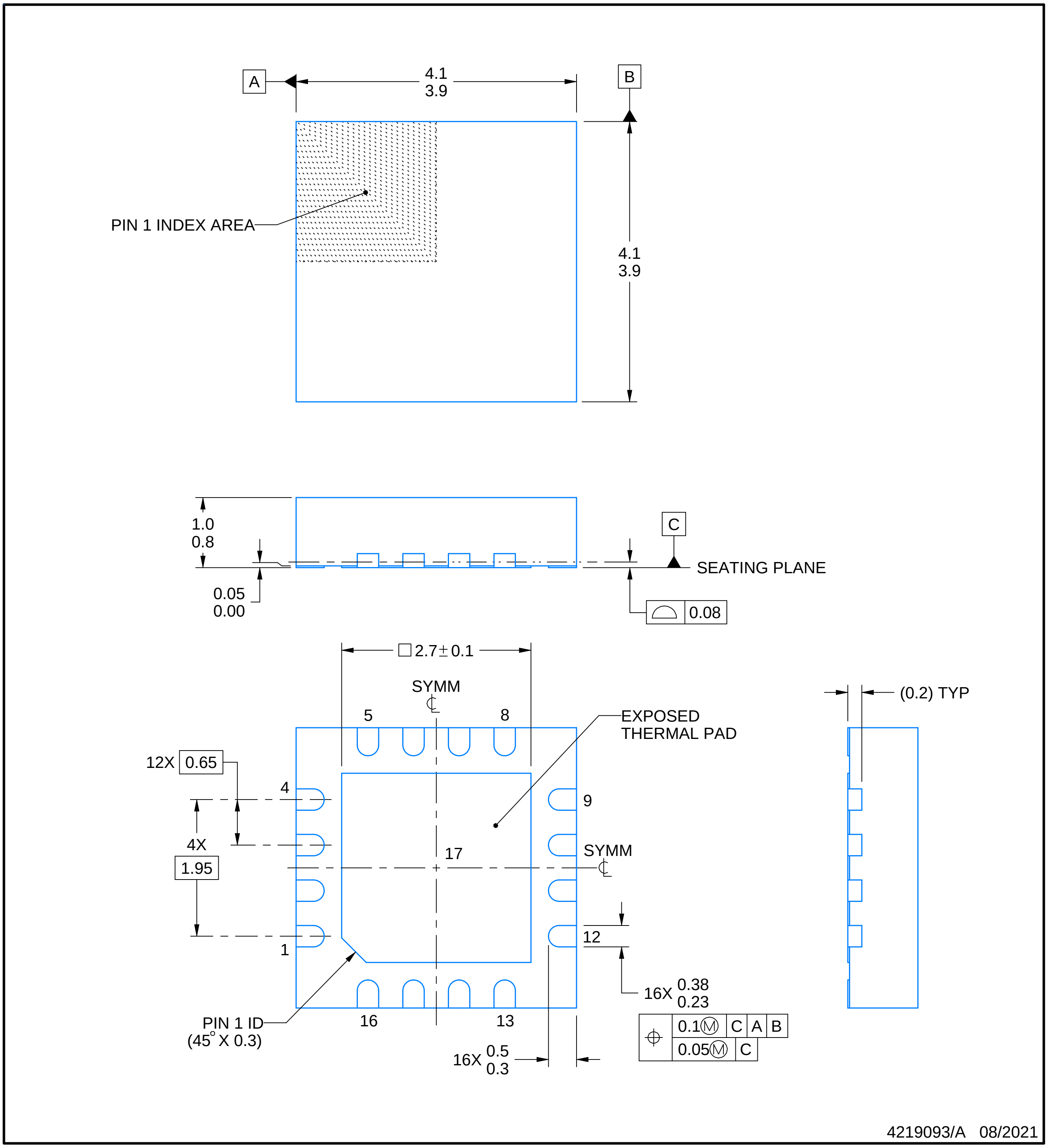
4230969/A



PACKAGE OUTLINE

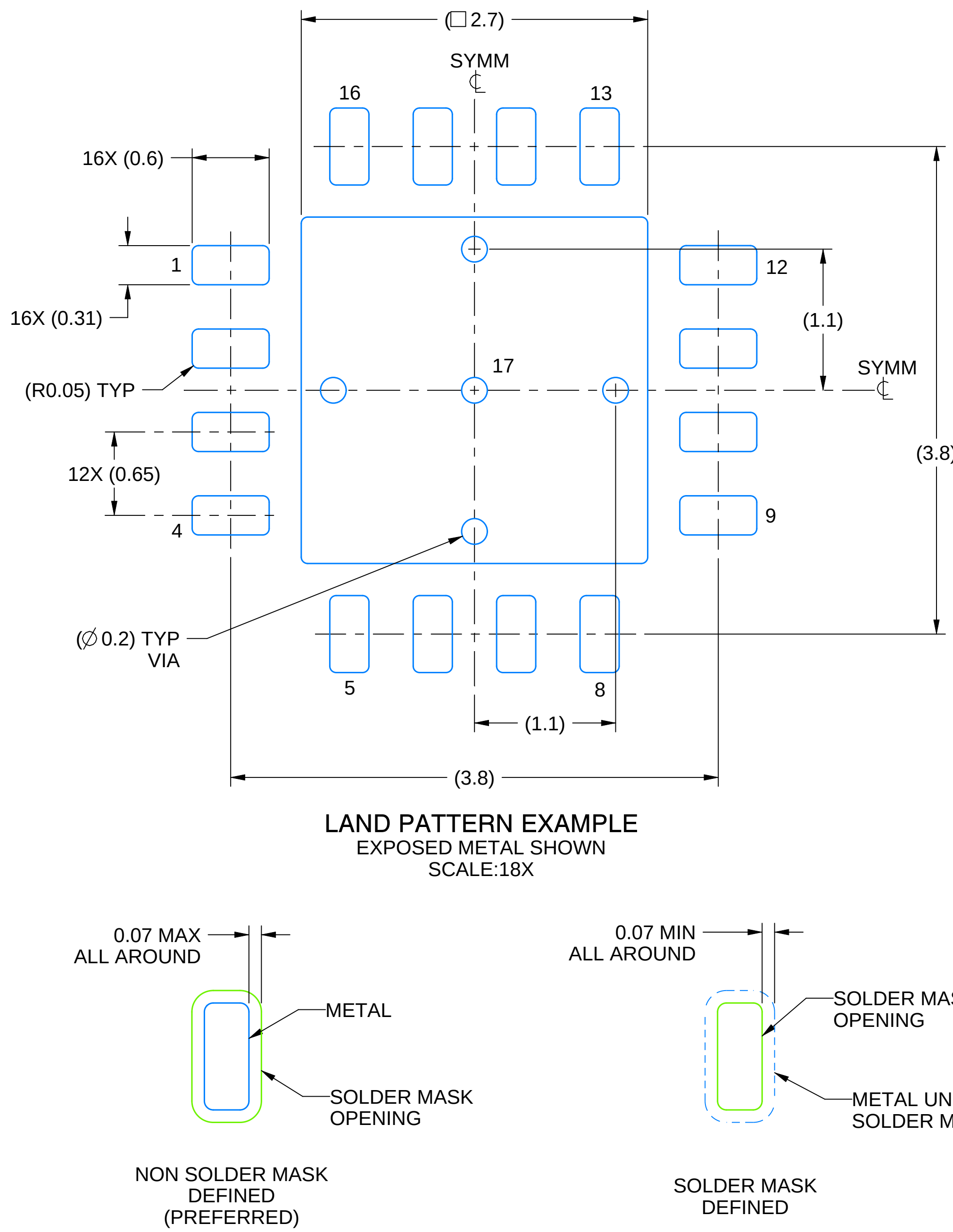
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

NON SOLDER MASK
DEFINED
(PREFERRED)

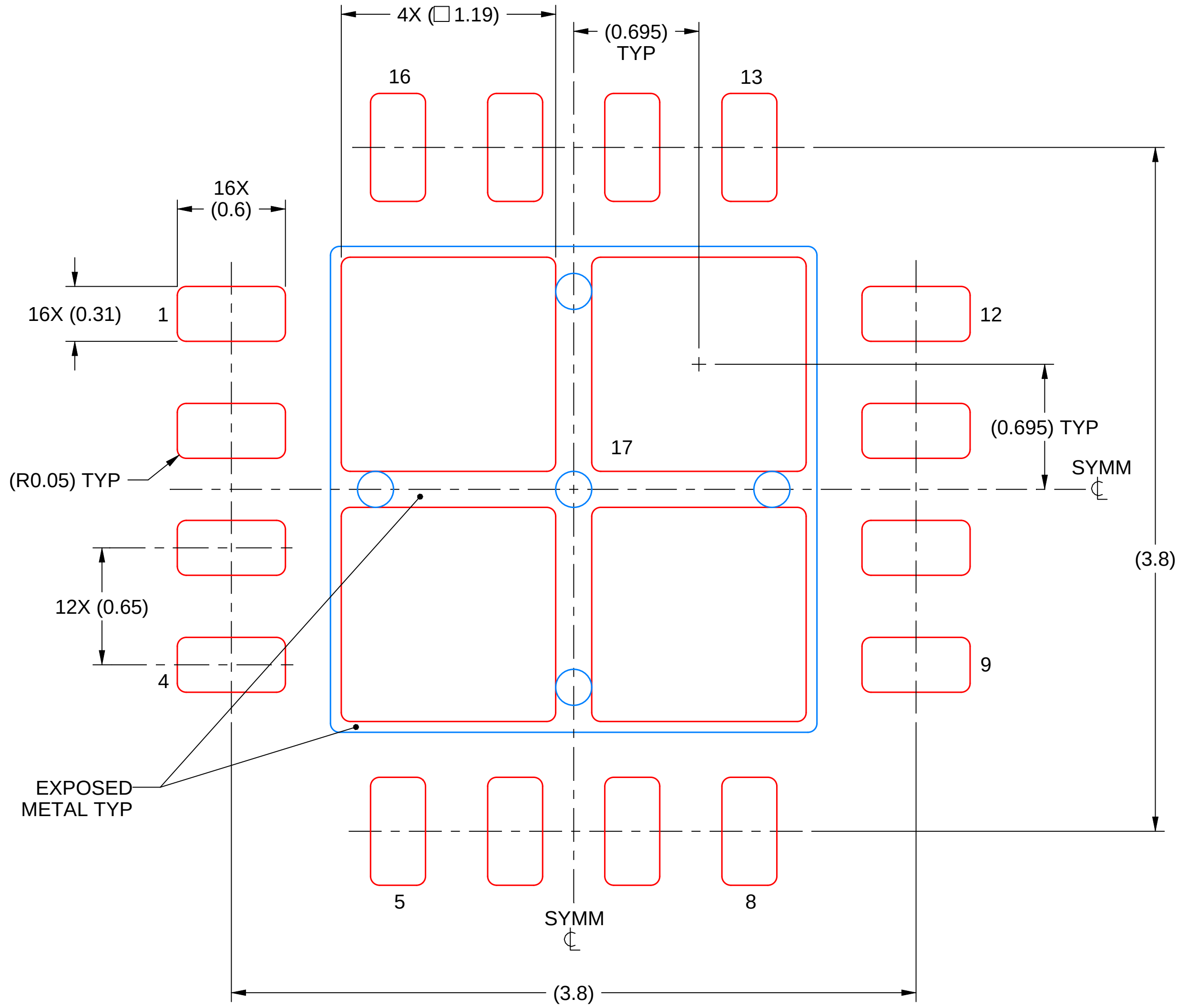
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

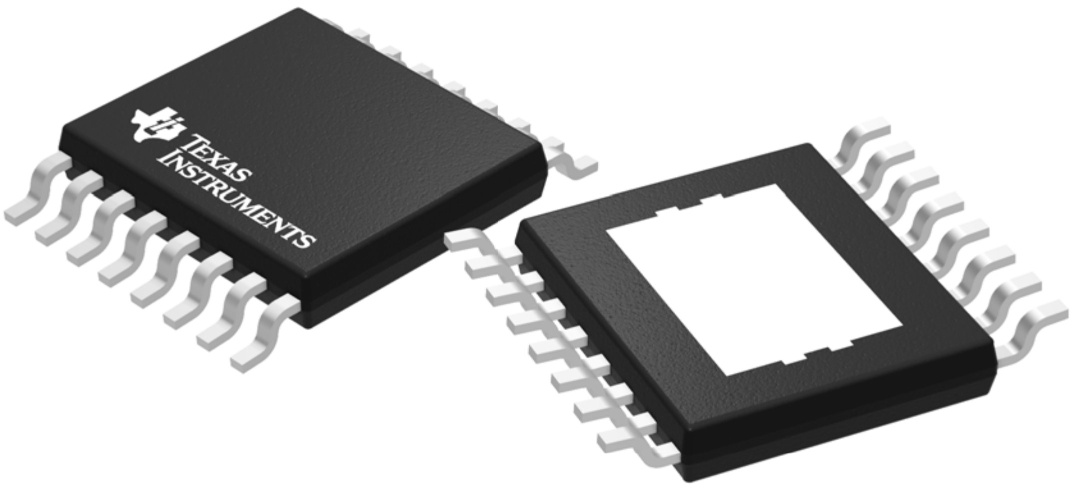
4219093/A 08/2021

NOTES: (continued)

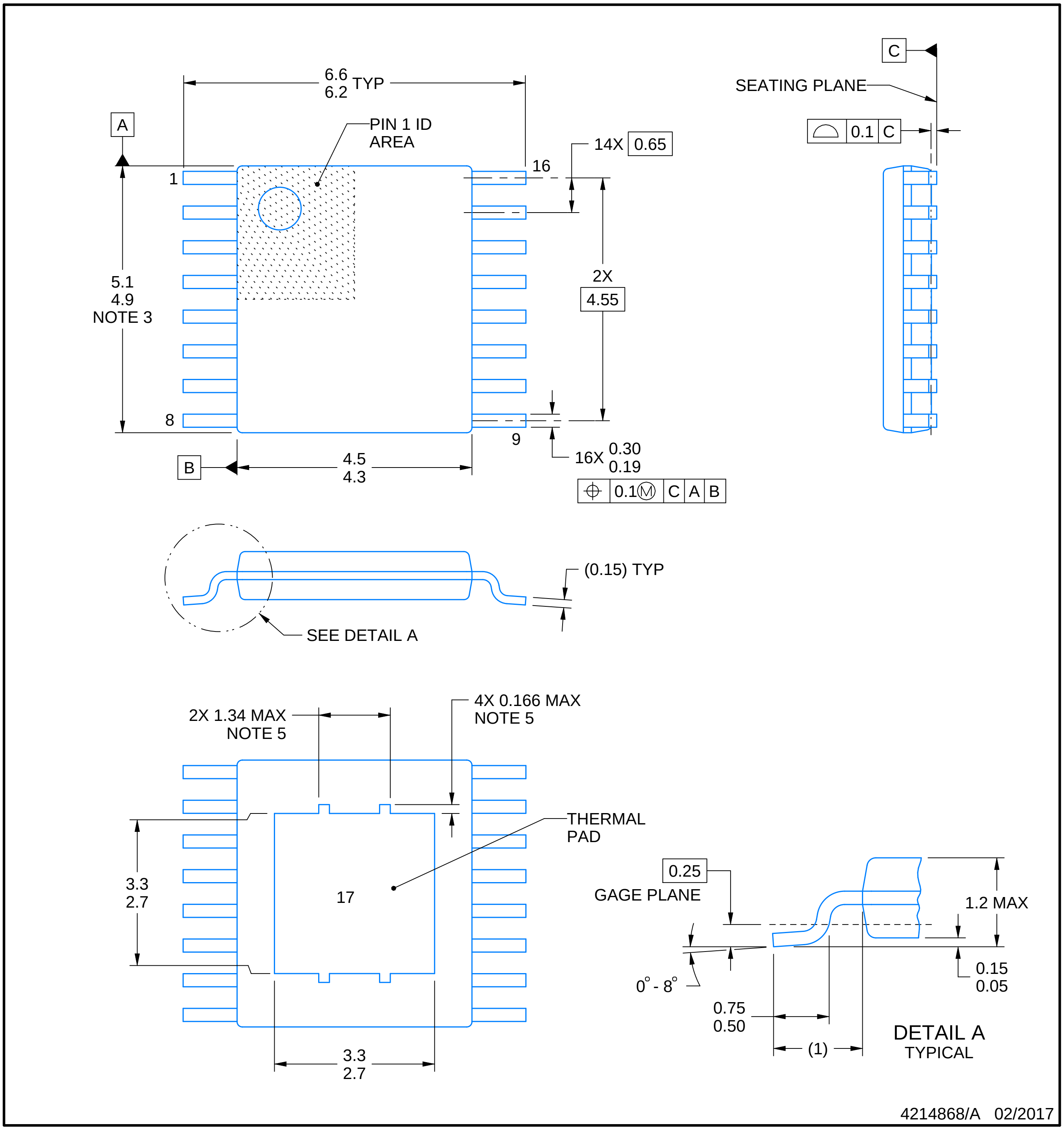
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



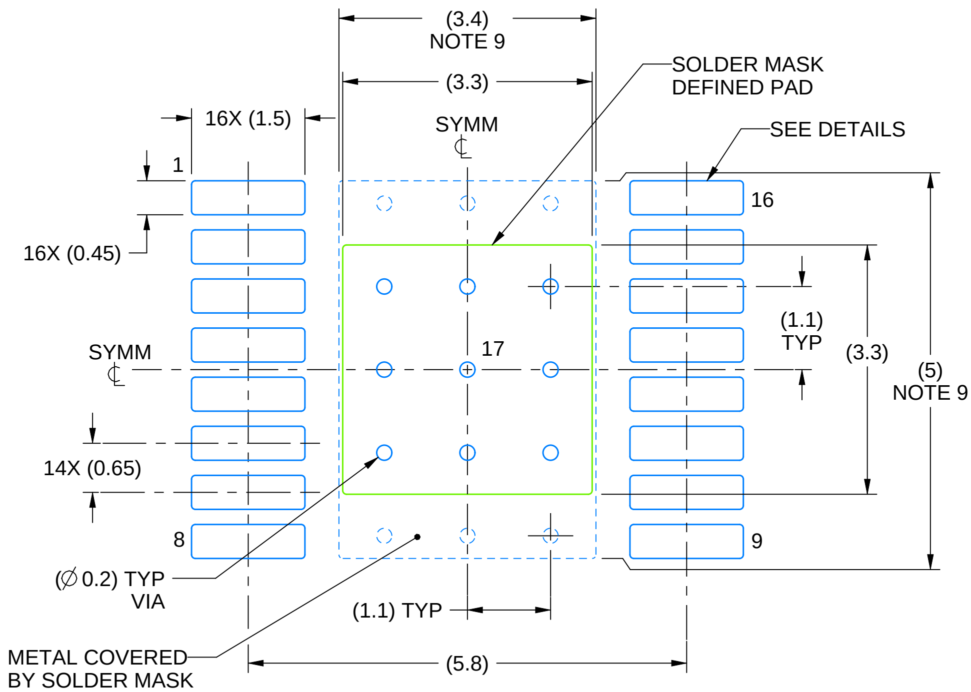
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



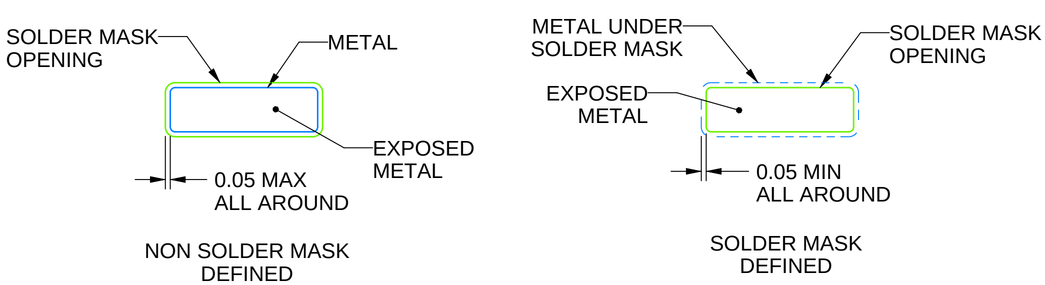
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS
PADS 1-16

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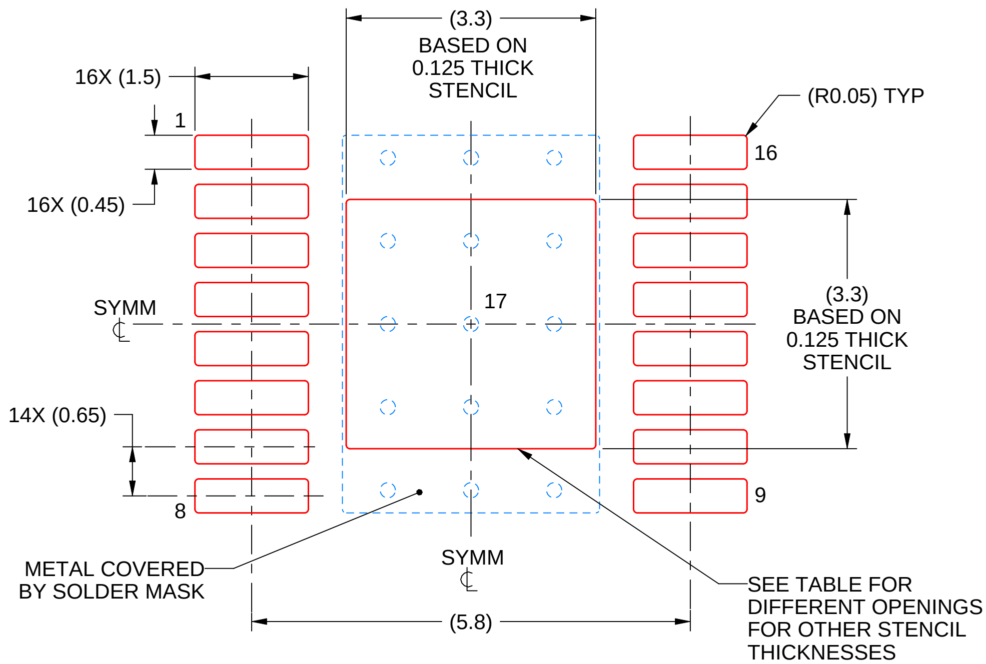
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.