用于笔记本电脑显示器的白光 LED (WLED) 驱动器

查询样品: TPS61181A

特性

- **4.5V** 至 **24V** 输入电压
- **38V** 最大输出电压
- 集成型 **1.5A / 40V MOSFET**
- **1.0MHz** 开关频率
- 自适应升压输出至 **WLED** （白光**LED**） 电压
- 小型外部组件
- 集成环路补偿
- **6** 个 **30mA** 电流宿 **(current sink)**
- 多达 **10** 个 串联的白光 **LED (WLED)**
- **1%** 的典型电流匹配及准确度
- 高达 **1000:1** 的 **PWM** 亮度调光
- 在 **PWM** 调光条件下实现了输出纹波的最小化
- 用于输入**/**输出隔离 **PFET** 的驱动器
- 真正的停机
- 具有过压保护功能
- 白光 **LED (WLED)** 开路**/**短路保护
- 内置软起动功能
- **16L 3mm x 3mm QFN** 封装

应用

- 笔记本电脑 **LCD** 显示器背光源
- **UMPC** （超级移动个人电脑） **LCD** 显示器背光源
- 媒体外形 **(Media Form Factor) LCD** 显示器的背光源

说明

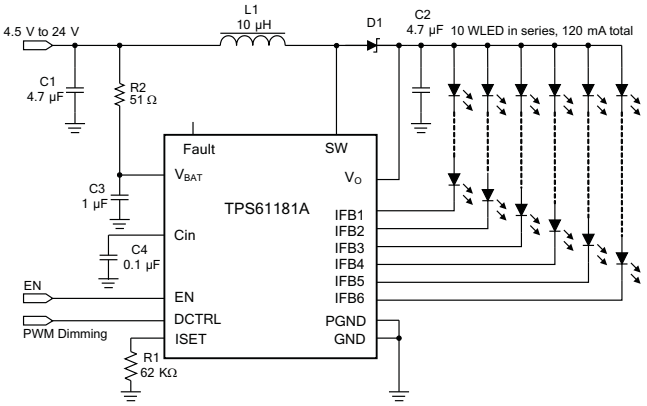
TPS61181A IC 为媒体尺寸 LCD 背光照明提供了高度集成的解决方案。 这些器件具有一个内置的高效率升压型稳压器和集成型 1.5A / 40V 功率 MOSFET。 6 个电流宿稳压器提供了高精度的电流调节和匹配。 该器件总共能够支持多达 60 个白光 LED。 此外，升压输出还可自动地将其电压调节至白光 LED 正向电压以改善效率。

这些器件支持脉宽调制 (PWM) 亮度调光。 在调光期间，以由 DCRTL 引脚的 PWM 信号输入决定的占空比和频率来接通和关断白光 LED 电流。 PWM 的一个潜在的问题是来自陶瓷输出电容器的可听噪声。 TPS61181A 专为在宽阔的调光占空比和频率范围内实现该输出 AC 纹波的最小化而设计，因而降低了这种可听噪声。

TPS61181A 为连接在输入和电感器之间的外部 PFET 提供了一个驱动器输出。 在短路或过流情况下，该 IC 将关断外部 PDET 并把电池与白光 LED 断开。 在 IC 停机期间，PFET 也被关断 （从而实现了 “真正的” 停机），以阻止电池产生任何漏电流。 另外，这款器件还集成了过压保护、软起动和热停机功能。

TPS61181A 具有一个用于提供 IC 电源的内置线性稳压器。 该器件采用 3mm x 3mm QFN 封装。

TPS61181A 的典型应用



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

PACKAGE	PACKAGE MARKING
TPS61181ARTE	QWF

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	MAX	
Voltage Range (2)	V_{BAT} and Fault	–0.3	24	V
	C_{in} and ISET	–0.3	3.6	
	SW and V_O	–0.3	40	
	IFB1 to IFB6, EN and DCTRL	–0.3	20	
ESD Rating(3)	Humen Body Mode – (HBM)		3	kV
	Machine Mode – (MM)		200	V
	Charge Device Mode – (CDM)		1	kV
Continuous power dissipation		See Thermal Information Table		
Operating junction temperature range		–40	150	°C
Storage temperature range		–65	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61181A	UNITS
		QFN (16) PIN	
θ_{JA}	Junction-to-ambient thermal resistance	43.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	38.3	
θ_{JB}	Junction-to-board thermal resistance	14.6	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	14.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.6	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{bat}	Battery input voltage range	4.5		24	V
V_O	Output voltage range	Vin		38	V
L	Inductor	4.7		10	µH
C_O	Output capacitor	2.2		10	µF
F_{PWM}	PWM dimming frequency at D_{PWM} ≥ 1%	0.1		1	kHz
	PWM dimming frequency at D_{PWM} ≥ 5%	1		5	
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{BAT} = 10.8 V, 0.1 µF at Cin, EN = Logic High, IFB current = 20 mA, IFB voltage = 500 mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

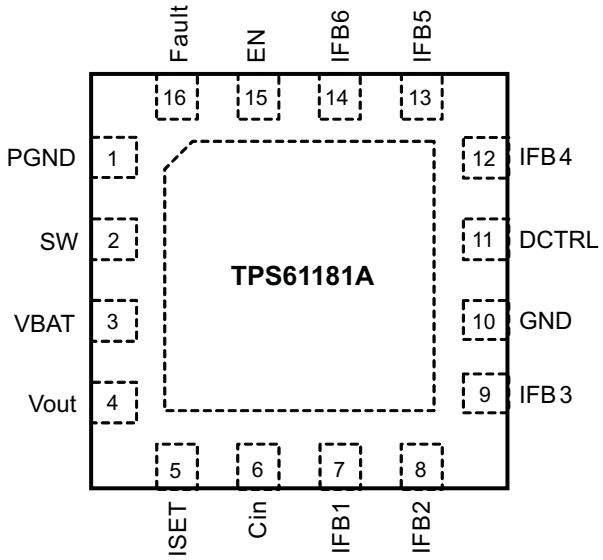
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{BAT}	Battery input voltage range		4.5		24	V
V_{cin}	Cin pin output voltage		2.7	3.15	3.6	V
I_{q_bat}	Operating quiescent current into V_{BAT}	Device enable, switching no load, Vin = 24 V			3	mA
I_{Q_sw}	Operating quiescent current into V_O	V_O = 35V			60	µA
I_{SD}	Shutdown current	EN=GND		2	18	µA
V_{bat_UVLO}	V_{BAT} under-voltage lockout threshold	V_{BAT} rising			4.45	V
		V_{BAT} falling	3.9			
V_{bat_hys}	V_{BAT} under-voltage lockout hysteresis	V_{BAT} rising – V_{BAT} falling		220		mV
EN AND DCTRL						
V_H	EN pin logic high voltage		2.0			V
V_L	EN pin logic low voltage				0.8	V
V_H	DCTRL pin logic high voltage		2.0			V
V_L	DCTRL pin logic low voltage				0.8	V
R_{PD}	Pull down resistor on both pins	$V_{EN,\ DCTRL}$ = 2V	400	800	1600	kΩ
CURRENT REGULATION						
V_{ISET}	ISET pin voltage		1.204	1.229	1.253	V
K_{ISET}	Current multiple Iout/ISET	ISET current = 20 µA	970	1000	1030	
IFB	Current accuracy	ISET current = 20 µA	19.4	20	20.6	mA
K_m	$(I_{max}–I_{min})/I_{AVG}$	ISET current = 20 µA		1	2.5	%
I_{leak}	IFB pin leakage current	IFB voltage = 20 V on all pins			3	µA
I_{IFB_MAX}	Current sink max output current	IFB = 500 mV	30			mA
BOOST OUTPUT REGULATION						
V_{IFB_L}	V_O dial up threshold	ISET current = 20 µA		400		mV
V_{IFB_H}	V_O dial down threshold	ISET current = 20 µA		700		mV
V_{reg_L}	Min Vout regulation voltage				16	V
V_{o_step}	V_O stepping voltage			100	150	mV
POWER SWITCH						
R_{PWM_SW}	PWM FET on-resistance			0.2	0.45	Ω
R_{start}	Start up charging resistance	V_O = 0 V	100		300	Ω
V_{start_r}	Isolation FET start up threshold	$V_{IN}–V_O$, V_O ramp up		1.2	2	V
I_{LN_NFET}	PWM FET leakage current	V_{SW} = 35 V, T_A = 25°C			1	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 10.8 V, 0.1 µF at Cin, EN = Logic High, IFB current = 20 mA, IFB voltage = 500 mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_S	Oscillator frequency		0.9	1.0	1.2	MHz
D_{max}	Maximum duty cycle	IFB = 0 V		94		%
D_{min}	Minimum duty cycle				7	%
OS, SC, OVP AND SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	1.5		3	A
V_{ovp}	V_O overvoltage threshold	Measured on the V_O pin	38	39	40	V
V_{ovp_IFB}	IFB overvoltage threshold	Measured on the IFBx pin	15	17	20	V
V_{sc}	Short circuit detection threshold	V_{IN}-V_O, V_O ramp down		1.7	2.5	V
V_{sc_dly}	Short circuit detection delay during start up			32		ms
Fault OUTPUT						
V_{fault_high}	Fault high voltage	Measured as V_{BAT}–V_{Fault}		0.1		V
V_{fault_low}	Fault low voltage	Measured as V_{BAT}–V_{Fault}, sink 0.1mA, Vin = 15 V	6	8	10	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

PINOUT



PIN ASSIGNMENTS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PGND	I	Power ground of the IC. Internally, it connects to the source of the PWM switch.
2	SW	I	This pin connects to the drain of the internal PWM switch, external Schottky diode and inductor.
3	V_{BAT}	I	This pin is connected to the battery supply. It provides the pull-up voltage for the Fault pin and battery voltage signal. This is also the input to the internal LDO.
4	V_O	O	This pin monitors the output of the boost regulator. Connect this pin to the anode of the WLED strings.
5	ISET	I	The resistor on this pin programs the WLED output current.
6	Cin	I	Supply voltage of the IC. It is the output of the internal LDO. Connect 0.1 µF bypass capacitor to this pin.
7, 8, 9 12, 13, 14	IFB1-IFB3 IFB4-IFB6	I	Current sink regulation inputs. They are connected to the cathode of WLEDs. The PWM loop regulates the lowest V_{IFB} to 400 mV. Each channel is limited to 30 mA current.
10	GND	I	Signal ground of the IC.
11	DCTRL	I	Dimming control logic input. The dimming frequency range is 100 Hz to 1 kHz.
15	EN	I	The enable pin to the IC. A logic high signal turns on the internal LDO and enables the IC. Therefore, do not connect the EN pin to the Cin pin.
16	Fault	I	Gate driver output for an external PFET used for fault protection. It can also be used as signal output for system fault report.

TYPICAL CHARACTERISTICS

Table of Graphs

Description (Reference to application circuit in Figure 15)		Figure
DC Load Efficiency	V_{bat}= 5V, 10.8V, 19V; V_O=28.6V, 9LEDs; L=10uH	Figure 1
DC Load Efficiency	V_{bat}= 5V, 10.8V, 19V; V_O=31.7V, 10LEDs; L=10uH	Figure 2
PWM Dimming Efficiency	V_{bat}= 5V, 10.8V and 19V; V_O=25.5V, 8LEDs; PWM Freq = 1kHz	Figure 3
PWM Dimming Efficiency	V_{bat}= 5V, 10.8V and 19V; V_O=28.6V, 9LEDs; PWM Freq = 1kHz	Figure 4
PWM Dimming Efficiency	V_{bat}= 5V, 10.8V and 19V; V_O=31.7V, 10LEDs; PWM Freq = 1kHz	Figure 5
PWM Dimming Efficiency	V_{bat}= 5V, 10.8V and 19V; V_O=34.8V, 11LEDs; PWM Freq = 1kHz	Figure 6
Dimming Linearity	V_{bat}= 10.8V; V_O=28.6V, 9LEDs; I_{set}= 20μA; PWM Freq = 1kHz	Figure 7
Dimming Linearity	V_{bat}= 10.8V; V_O=28.6V, 9LEDs; I_{set}= 20μA; PWM Freq = 200Hz	Figure 8
Output Ripple	V_O=28.6V; I_{set}= 20μA; PWM Freq = 200Hz; Duty = 50%	Figure 9
Switching Waveform	V_{bat}= 10.8V; I_{set}= 20μA	Figure 10
Output Ripple at PWM Dimming	V_{bat}= 10.8V; I_{set}= 20μA; PWM Freq = 200Hz; Duty = 50%; C_O=4.7μF	Figure 11
Short Circuit Protection	V_{bat}= 10.8V; I_{set}= 20μA	Figure 12
Open WLED Protection	V_{bat}= 10.8V; I_{set}= 20μA	Figure 13
Startup Waveform	V_{bat}= 10.8V; I_{set}= 20μA	Figure 14

EFFICIENCY vs OUTPUT CURRENT

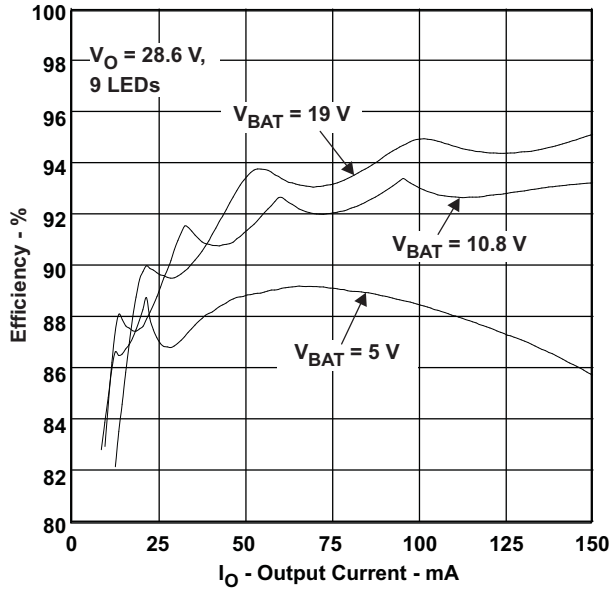


Figure 1.

EFFICIENCY vs OUTPUT CURRENT

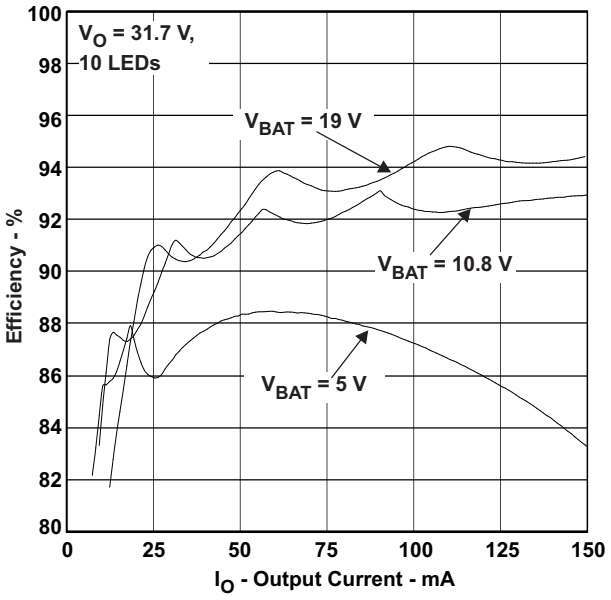


Figure 2.

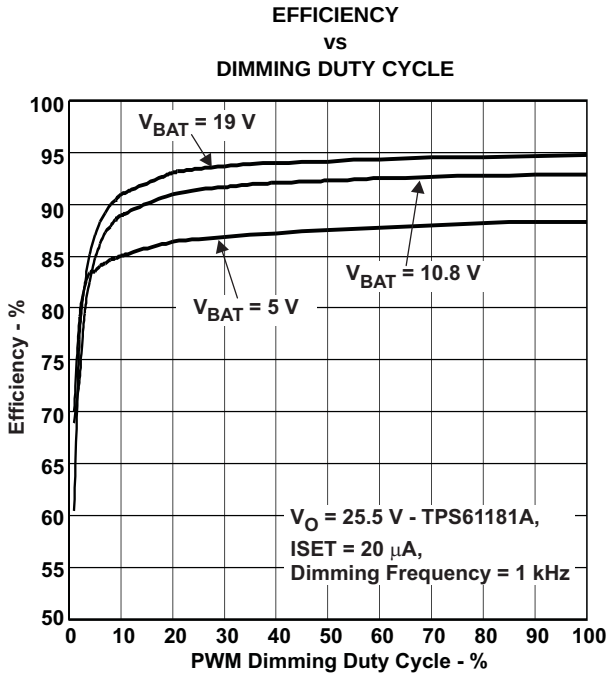


Figure 3.

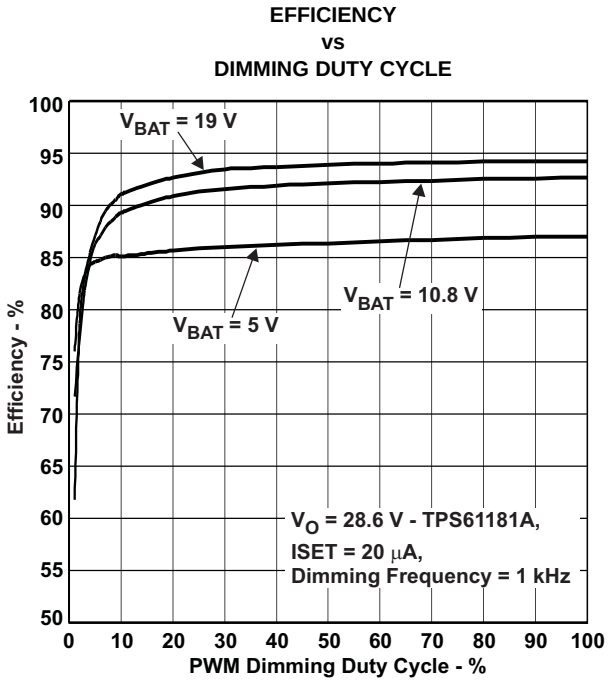


Figure 4.

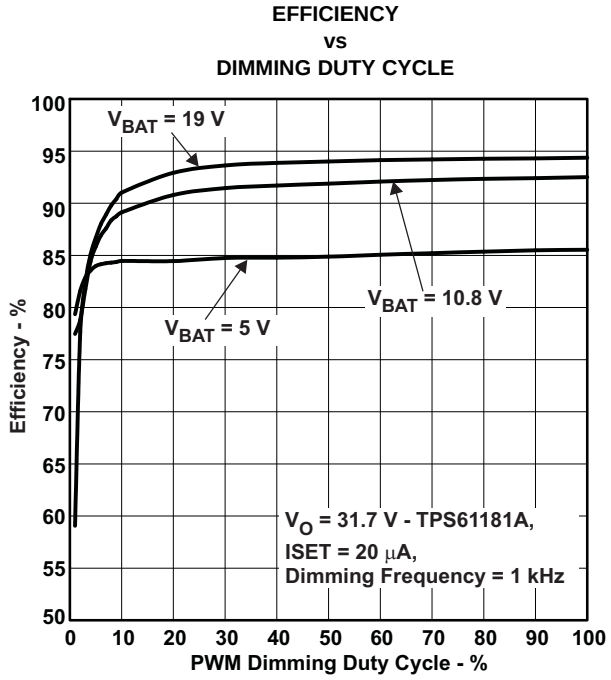


Figure 5.

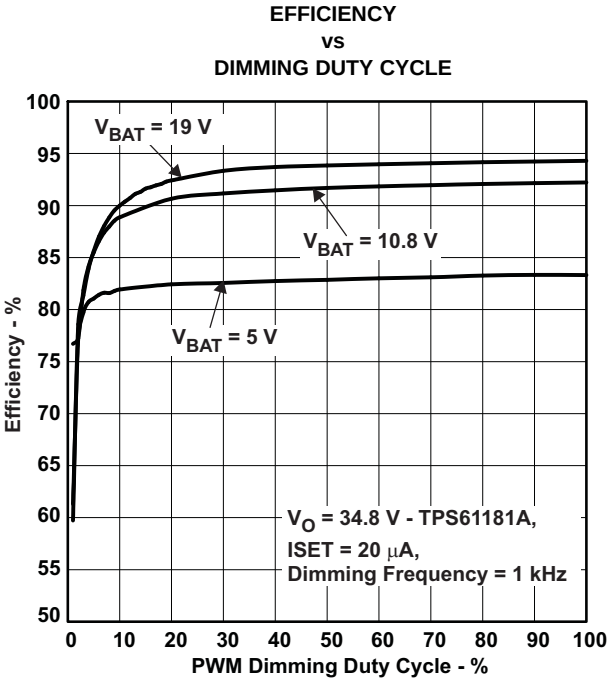


Figure 6.

PWM DIMMING linearity 1kHz

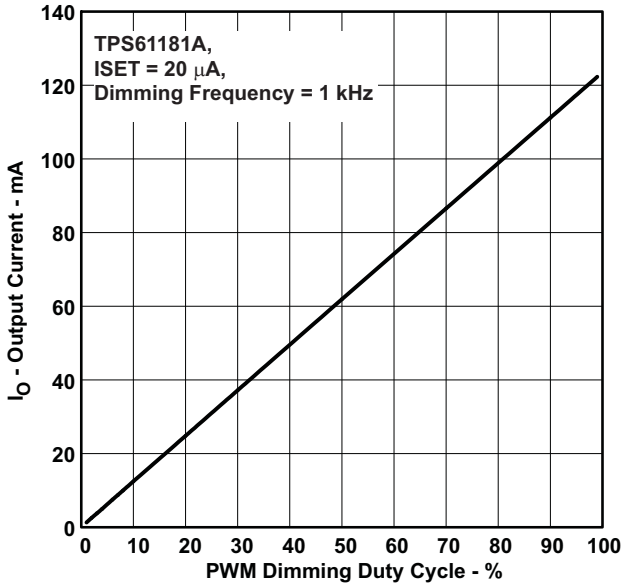


Figure 7.

PWM DIMMING LINEARITY 200Hz

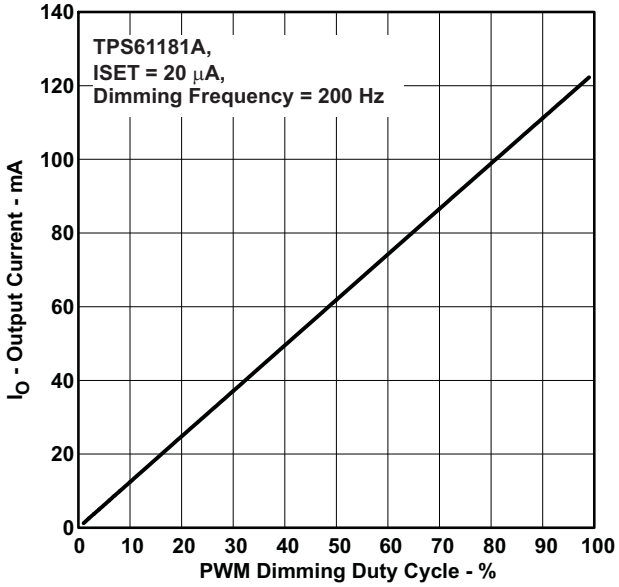


Figure 8.

PWM DIMMING OUTPUT RIPPLE C_O=4.7μF
vs
INPUT VOLTAGE

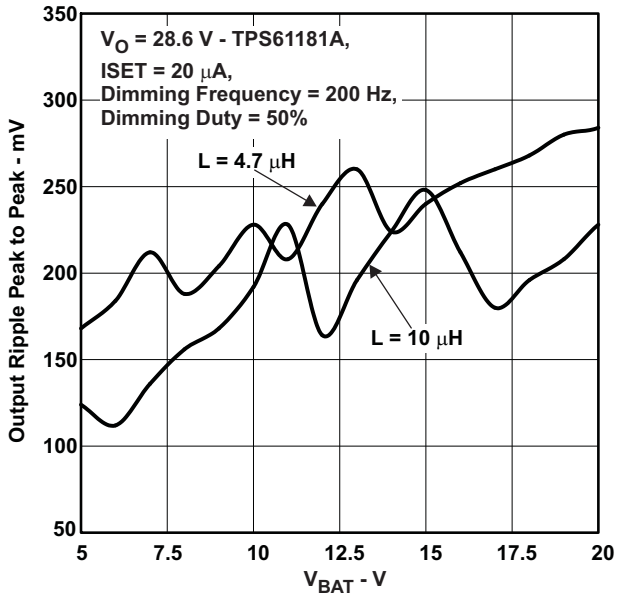


Figure 9.

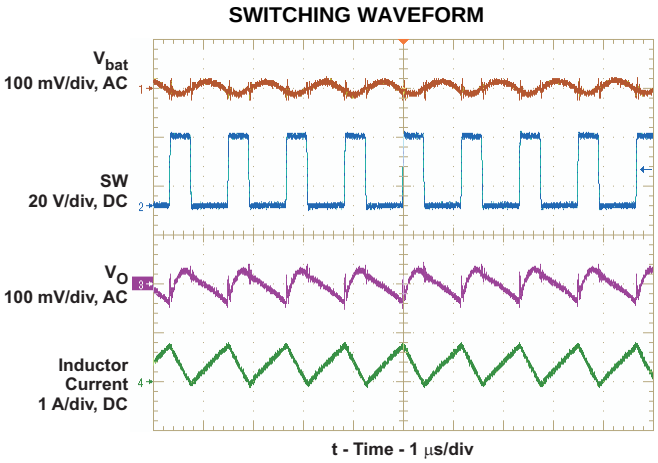


Figure 10.

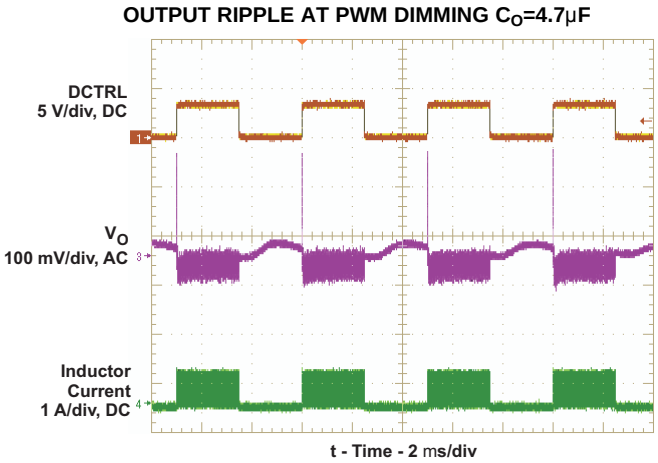


Figure 11.

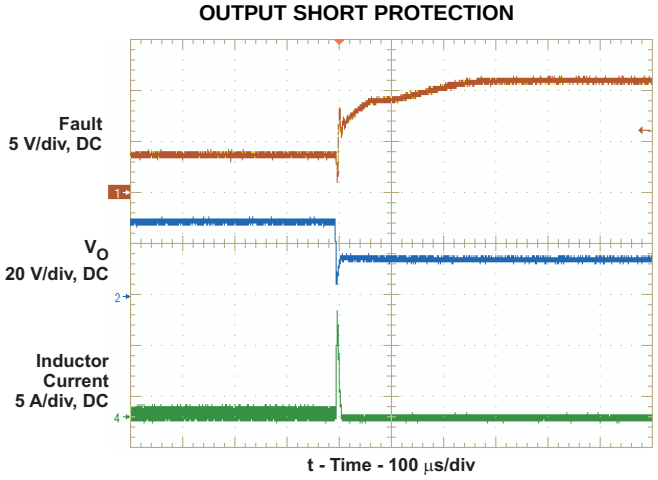


Figure 12.

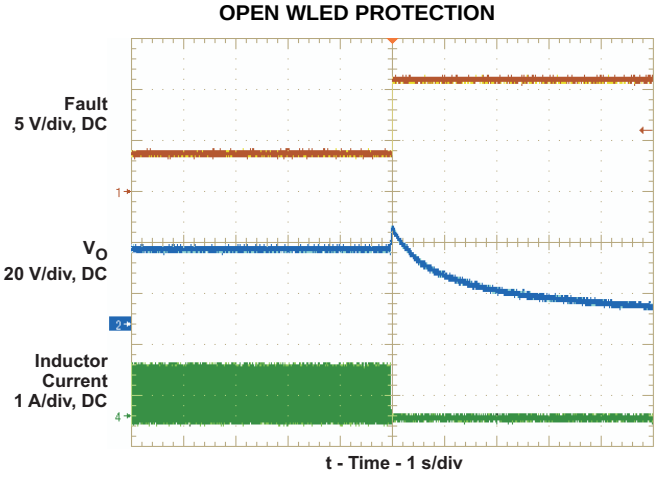


Figure 13.

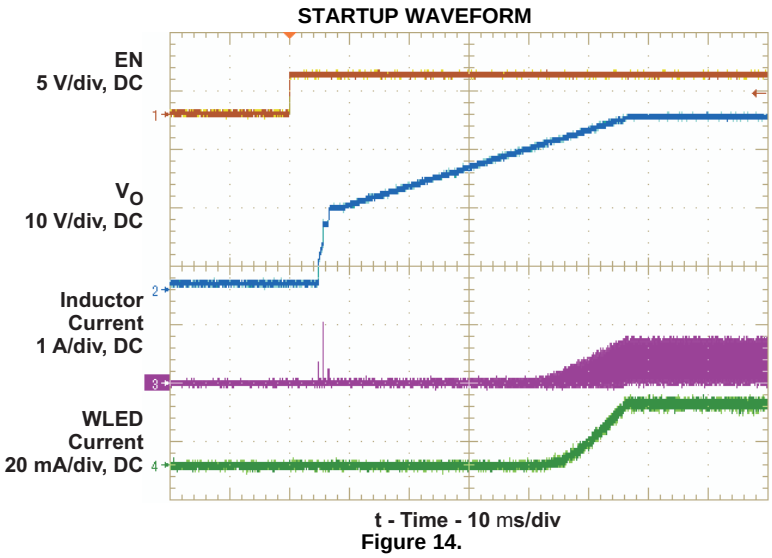
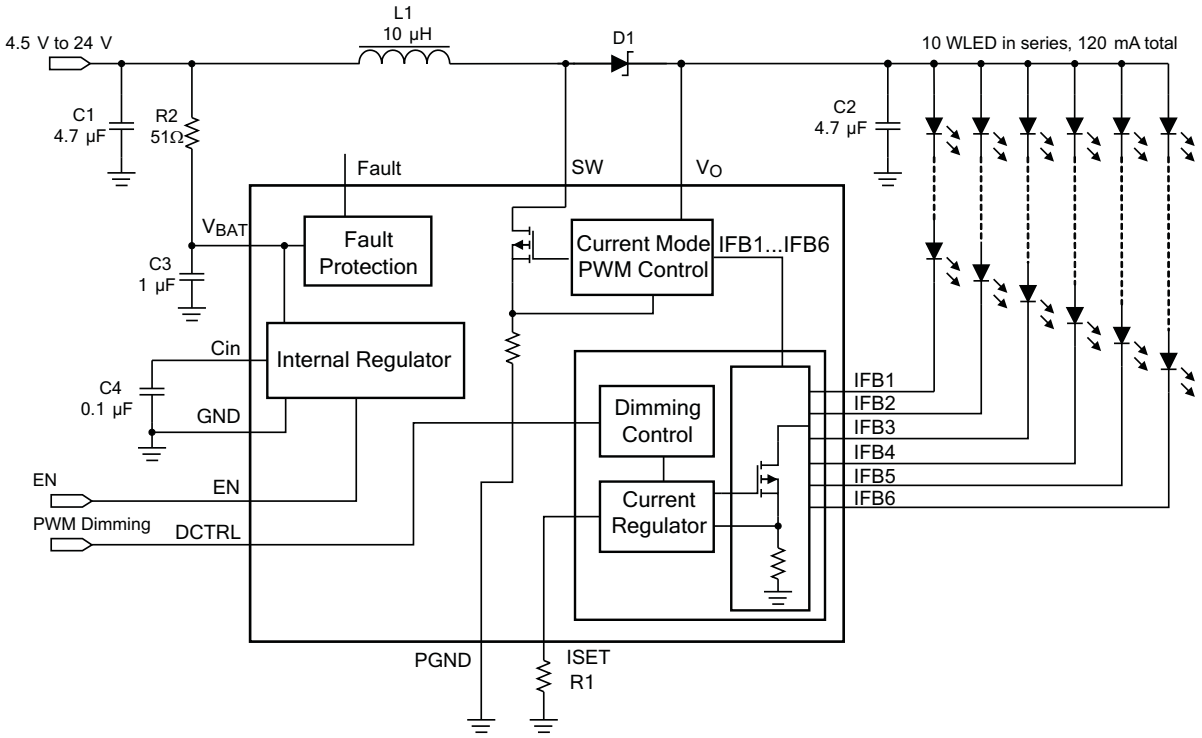


Figure 14.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Recently, WLEDs have gained popularity as an alternative to CCFL for backlighting media size LCD displays. The advantages of WLEDs are power efficiency and low profile design. Due to the large number of WLEDs, they are often arranged in series and parallel, and powered by a boost regulator with multiple current sink regulators. Having more WLEDs in series reduces the number of parallel strings and therefore improves overall current matching. However, the efficiency of the boost regulator declines due to the need for high output voltage. Also, there have to be enough WLEDs in series to ensure the output voltage stays above the input voltage range. Otherwise, a buck-boost (for example, SEPIC) power converter has to be adopted which could be more expensive and complicated.

The TPS61181A IC has integrated all the key function blocks to power and control up to 60 WLEDs. The devices include a 40V/1.5A boost regulator, six 30mA current sink regulators and protection circuit for over-current, over-voltage and short circuit failures. The key advantages of the devices are small solution size, low output AC ripple during PWM dimming control, and the capability to isolate the input and output during fault conditions.

SUPPLY VOLTAGE

The TPS61181A has built-in LDO linear regulator to supply the IC analog and logic circuits. The LDO is powered up when the EN pin is high. The output of the LDO is connected to the Cin pin. A 0.1μF bypass capacitor is required for LDO's stable operation. Do not connect the Cin pin to the EN pin because this prevents the IC from starting up. In addition, avoid connecting the Cin pin to any other circuit as this could introduce noise into the IC supply voltage.

The V_{BAT} connects to the input of the internal LDO, and powers the IC. The voltage on the V_{BAT} pin is also the reference for the pull-up circuit of the Fault pin. In addition, it serves as the input signal to the short circuit protection. There is an under-voltage lockout on the V_{BAT} pin which disables the IC when its voltage reduces to 4.2V (Typical). The IC restarts when the V_{BAT} pin voltage recovers by 220mV.

BOOST REGULATOR

The boost regulator is controlled by current mode PWM, and loop compensation is integrated inside the IC. The internal compensation ensures stable output over the full input and output voltage range. The TPS61181A switches at 1.0MHz which optimize boost converter efficiency and voltage ripple with a small form factor inductor and output capacitor.

The output voltage of the boost regulator is automatically set by the IC to minimize the voltage drop across the IFB pins. The IC automatically regulates the lowest IFB pin to 400mV, and consistently adjusts the boost output voltage to account for any changes of the LED forward voltages.

When the output voltage is too close to the input, the boost regulator may not be able to regulate the output due to the limitation of minimum duty cycle. In this case, increase the number of WLED in series or include series ballast resistors in order to provide enough headroom for the boost operation.

The TPS61181A boost regulator cannot regulate its output to voltages below 15V.

CURRENT PROGRAM AND PWM DIMMING

The six current sink regulators can each provide a maximum of 30mA. The IFB current must be programmed to maximum WLED current using the ISET pin resistor and the following Equation 1.

$$I_{FB} = K_{ISET} \frac{V_{ISET}}{R_{ISET}} \quad (1)$$

Where

K_{ISET} = Current multiple (1000 typical)

V_{ISET} = ISET pin voltage (1.229 V typical)

R_{ISET} = ISET pin resistor

The TPS61181A has six built-in precise current sink regulators. The current matching among the current sinks at 20mA current through is below 2.5%. This means the differential value between the maximum and minimum current of the six current sinks divided by the average current of the six is less than 2.5%.

The WLED brightness is controlled by the PWM signal on the DCTRL pin. The frequency and duty cycle of the DCTRL signal is replicated on the IFB pin current. Keep the dimming frequency in the range of 100Hz to 1kHz to avoid screen flickering and maintain dimming linearity. Screen flickering may occur if the dimming frequency is below the range. The minimum achievable duty cycle increases with the dimming frequency. For example, while a 0.1% dimming duty cycle, giving a 1000:1 dimming range, is achievable at 100 Hz dimming frequency, only 1% duty cycle, giving a 100:1 dimming range, is achievable with a 1 KHz dimming frequency, and 5% dimming duty cycle is achievable with 5KHz dimming frequency. The device could work at high dimming frequency like 20 KHz, but then only 15% duty cycle could be achievable. The TPS61181A is designed to minimize the AC ripple on the output capacitor during PWM dimming. Careful passive component selection is also critical to minimize AC ripple on the output capacitor. See APPLICATION INFORMATION for more information.

ENABLE AND START UP

A logic high signal on the EN pin turns on the IC. For the TPS61181A, taking EN high turns on the internal LDO linear regulator which provides supply to the IC current. Then, an internal resistor, R_{start} (start up charging resistor) is connected between the V_{BAT} pin and V_O pin to charge the output capacitor toward the V_{BAT} pin voltage. The Fault pin outputs high during this time, and thus the external isolation PFET is turned off. Once the V_O pin voltage is within 2 V (isolation FET start up threshold) of the V_{BAT} pin voltage, R_{start} is open, and the Fault pin pulls down the gate of the PFET and connects the V_{BAT} voltage to the boost regulator. This operation is to prevent the in-rush current due to charging the output capacitor.

Once the isolation FET is turned on, the IC starts PWM switching to raise the output voltage above V_{BAT}. Soft-start is implemented by gradually ramping up the reference voltage of the error amplifier to prevent voltage over-shoot and in-rush current. See the start-up waveform of a typical example, Figure 14.

Pulling the EN pin low immediately shuts down the IC, resulting in the IC consuming less than 50μA in the shutdown mode.

OVER-CURRENT, OVER-VOLTAGE AND SHORT-CIRCUIT PROTECTION

The TPS61181A has pulse-by-pulse over-current limit of 1.5A (min). The PWM switch turns off when the inductor current reaches this current threshold. The PWM switch remains off until the beginning of the next switching cycle. This protects the IC and external components under over-load conditions. When there is sustained over-current condition for more than 16ms (under 100% dimming duty cycle), the IC turns off and requires POR or the EN pin toggling to restart.

Under severe over-load and/or short circuit conditions, the V_O pin can be pulled below the input (V_{BAT} pin). Under this condition, the current can flow directly from V_{BAT} to the WLED through the inductor and schottky diode. Turning off the PWM switch alone does not limit current anymore. In this case, the TPS61181A detects the output voltage is 1.7V (V_{sc},short circuit detection threshold) below the input voltage, turns off the isolation FET, and shuts down the IC. The IC restarts after input power-on reset (V_{BAT} POR) or EN pin logic toggling.

During IC start up, if there is short circuit condition on the boost converter output, the output capacitor will not be charged to within 2V of V_{BAT} through R_{start}. After 32ms (V_{sc_dly}short circuit detection delay during start up), the TPS61181A shuts down and does not restart until there is V_{BAT} POR or EN pin toggling. The isolation FET is never turned on under the condition.

If one of the WLED strings is open, the boost output rises to over-voltage threshold (39V typical). The TPS61181A detects the open WLED string by sensing no current in the corresponding IFB pin. As a result, the IC removes the open IFB pin from the voltage feedback loop. Subsequently, the output voltage drops down and is regulated to a voltage for the connected WLED strings. The IFB current of the connected WLED strings keep in regulation during the whole transition. The IC only shuts down if it detects that all of the WLED strings are open.

If the over-voltage threshold is reached, but the current sensed on the IFB pin is below the regulation target, the IC regulates the boost output at the over-voltage threshold. This operation could occur when the WLED is turned on under cold temperature, and the forward voltages of the WLEDs exceed the over-voltage threshold. Maintaining the WLED current allows the WLED to warm up and their forward voltages to drop below the over-voltage threshold.

If any IFB pin voltage exceeds IFB over-voltage threshold (17V typical), the IC turns off the corresponding current sink and removes this IFB pin from V_O regulation loop. The remaining IFB pins' current regulation is not affected. This condition often occurs when there are several shorted WLEDs in one string. WLED mismatch typically does not create such large voltage difference among WLED strings.

IFB PIN UNUSED

If the application requires less than 6 WLED strings, one can easily disable unused IFB pins. The TPS61181A simply requires leaving the unused IFB pin open or shorting it to ground. If the IFB pin is open, the boost output voltage ramps up to V_O over-voltage threshold during start up. The IC then detects the zero current string, and removes it from the feedback loop. If the IFB pin is shorted to ground, the IC detects the short immediately after IC enable, and the boost output voltage does not go up to V_O over-voltage threshold. Instead, it ramps to the regulation voltage after soft start.

APPLICATION INFORMATION

INDUCTOR SELECTION

Because the selection of the inductor affects a power supply's steady state operation, transient behavior and loop stability, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance and saturation current. The TPS61181A ICs are designed to work with inductor values between 4.7µH and 10µH. A 4.7µH inductor may be available in a smaller or lower profile package, while 10µH may produce higher efficiency due to lower inductor ripple. If the boost output current is limited by the over-current protection of the IC, using a 10µH inductor can offer higher output current.

The internal loop compensation for the PWM control is optimized for the recommended component values, including typical tolerances. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20 to 35% from the zero current value depending on how the inductor vendor defines saturation

In a boost regulator, the inductor DC current can be calculated as

$$I_{dc} = \frac{V_O \times I_O}{V_{in} \times \eta} \quad (2)$$

Where

V_O = boost output voltage

Io = boost output current

V_{in} = boost input voltage

η = power conversion efficiency, use 90% for TPS61181A applications

The inductor current peak to peak ripple can be calculated as

$$I_{pp} = \frac{1}{L \times \left(\frac{1}{V_O - V_{bat}} + \frac{1}{V_{bat}} \right) \times F_S} \quad (3)$$

Where

I_{pp} = inductor peak to peak ripple

L = inductor value

F_s= Switching frequency

V_{bat}= boost input voltage

Therefore, the peak current seen by the inductor is

$$I_p = I_{dc} + \frac{I_{pp}}{2} \quad (4)$$

Select the inductor with saturation current at least 25% higher than the calculated peak current. To calculate the worse case inductor peak current, use minimum input voltage, maximum output voltage and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path, switching losses associated with the PWM switch and power diode. Although the TPS61181A ICs have optimized the internal switch resistance, the overall efficiency still relies on the DC resistance (DCR) of the inductor; lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint. Furthermore, shielded inductors typically have a higher DCR than unshielded ones. Table 1 lists recommended inductor models.

Table 1. Recommended Inductor for TPS61181A

	L (μH)	DCR Typ (mΩ)	I_{sat} (A)	Size (LXWXH mm)
TOKO				
A915AY-4R7M	4.7	38	1.87	5.2x5.2x3.0
A915AY-100M	10	75	1.24	5.2x5.2x3.0
TDK				
SLF6028T-4R7M1R6	4.7	28.4	1.6	6.0x6.0x2.8
SLF6028T-100M1R3	10	53.2	1.3	6.0x6.0x2.8

OUTPUT CAPACITOR SELECTION

During PWM brightness dimming, the load transient causes voltage ripple on the output capacitor. Since the PWM dimming frequency is in the audible frequency range, the ripple can produce audible noises on the output ceramic capacitor. There are two ways to reduce or eliminate this audible noise. The first option is to select PWM dimming frequency outside the audible range. This means the dimming frequency needs be to lower than 200Hz or higher than 30KHz. The potential issue with a very low dimming frequency is that WLED on/off can become visible and thus cause a flickering effect on the display. On the other hand, high dimming frequency can compromise the dimming range since the LED current accuracy and current match are difficult to maintain at low dimming duty cycle. The second option is to reduce the amount of the output ripple, and therefore minimize the audible noise.

The TPS61181A adopts a patented technology to limit output ripple even with small output capacitance. In a typical application, the output ripple is less than 200mV during PWM dimming with a 4.7μF output capacitor, and the audible noise is not noticeable. The devices are designed to be stable with output capacitor down to 1.0μF. However, the output ripple will increase with lower output capacitor.

Care must be taken when evaluating a ceramic capacitor's derating due to applied dc voltage, aging and over frequency. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the switching frequency range of the TPS61181A. So the effective capacitance is significantly lower. Therefore, it may be necessary to use small capacitors in parallel instead of one large capacitor.

AUDIBLE NOISE REDUCTION

Ceramic capacitors can produce audible noise if the frequency of its AC voltage ripple is in the audible frequency range. In TPS61181A applications, both input and output capacitors are subject to AC voltage ripple during PWM brightness dimming. The ICs integrate a patented technology to minimize the ripple voltage, and thus audible noises.

To further reduce the audible noise, one effective way is to use two or three small size capacitors in parallel instead of one large capacitor. The application circuit in Figure 15 uses two 2.2-μF/25V ceramic capacitors at the input and two 1-μF/50V ceramic capacitors at the output. All of the capacitors are in 0805 package. Although the output ripple during PWM dimming is higher than with one 4.7μF in a 1206 package, the overall audible noise is lower.

In addition, connecting a 10-nF/50V ceramic capacitor between the V_O pin and IFB1 pin can further reduce the output AC ripple during the PWM dimming. Since this capacitor is subject to large AC ripple, choose a small package such as 0402 to prevent it from producing noise.

ISOLATION MOSFET SELECTION

The TPS61181A provides a gate driver to an external P-channel MOSFET which can be turned off during device shutdown or fault condition. This MOSFET can provide a true shutdown function, and also protect the battery from output short circuit conditions. The source of the PMOS should be connected to the input, and a pull up resistor is required between the source and gate of the FET to keep the FET off during IC shutdown. To turn on the isolation FET, the Fault pin is pulled low, and clamped at 8 V below the V_{BAT} pin voltage.

During device shutdown or fault condition, the isolation FET is turned off, and the input voltage is applied on the

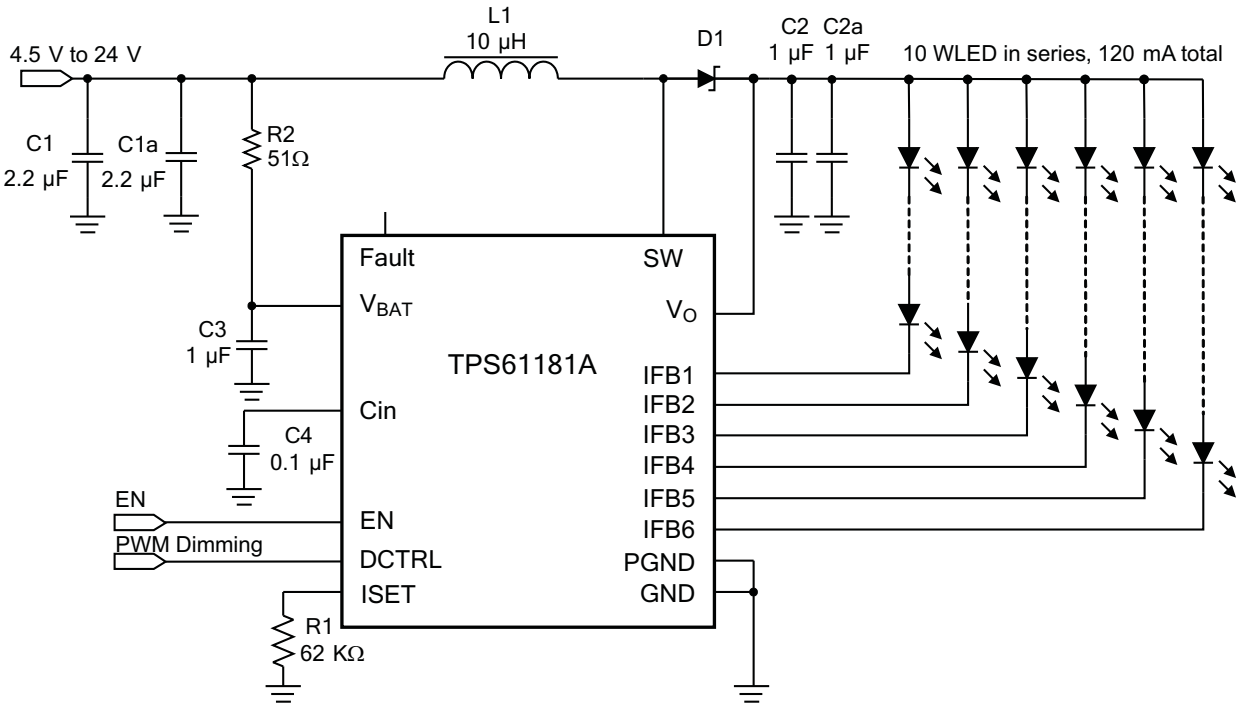
isolation MOSFET. During a short circuit condition, the catch diode (D2 in typical application circuit) is forward biased when the isolation FET is turned off. The drain of the isolation FET swings below ground. The voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select a 30V MOSFET for a 24V maximum input. The on resistance of the FET has a large impact on power conversion efficiency since the FET carries the input voltage. Select a MOSFET with $R_{ds(on)}$ less than 100mΩ to limit the power losses.

LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C3 in the typical application circuit, needs not only to be close to the V_{BAT} pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The input capacitor, C1 in the typical application circuit, should be placed close to the inductor. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the pin to the inductor and Schottky should be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the PGND pin since there is large ground return current flowing between them. When laying out signal ground, it is recommended to use short traces separated from power ground traces, and connect them together at a single point, for example on the thermal pad.

Thermal pad needs to be soldered on to the PCB and connected to the GND pin of the IC. Additional thermal via can significantly improve power dissipation of the IC.

ADDITIONAL APPLICATION CIRCUITS



C1, C1a: Murata GRM 219R61E225K
C2, C2a: Murata GRM 21BR71H105K
C3: Murata GRM 21BR71H105K
C4: Murata GRM 185R61A105K

L1: TOKO A 915AY-100 M
D1: VISHAY SS 2P5-E3/84A

Figure 15. Audible Noise Reduction Circuit

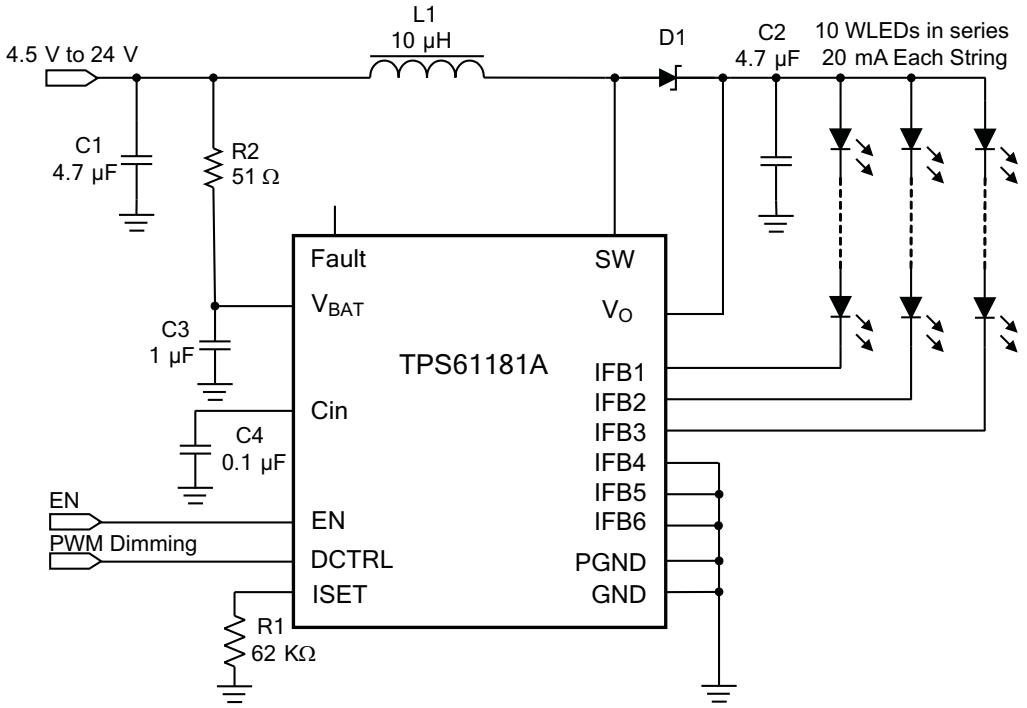


Figure 16. TPS61181A for Three Strings of LEDs

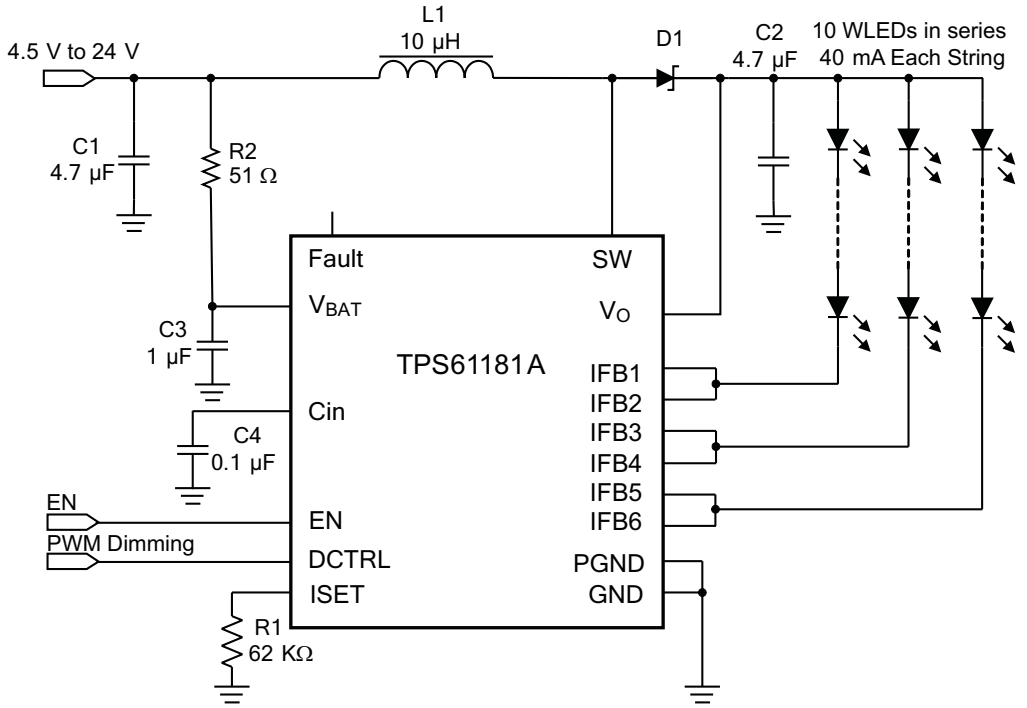


Figure 17. TSP61181A for Three Strings of LEDs with Double Current

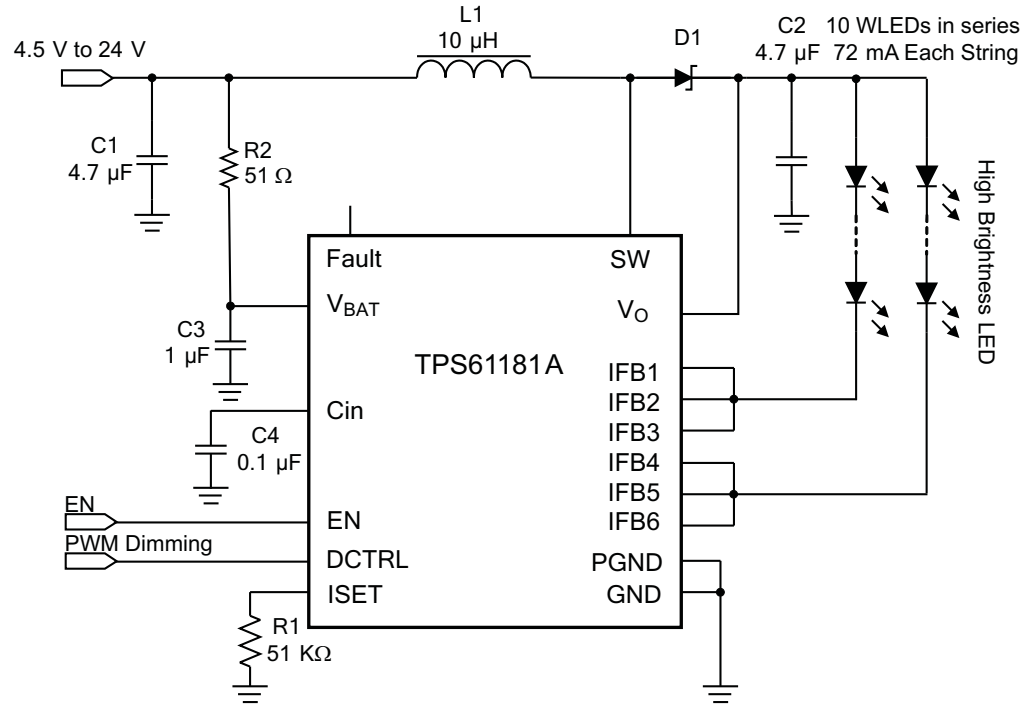


Figure 18. TSP61181A for Two Strings High Brightness LEDs Application

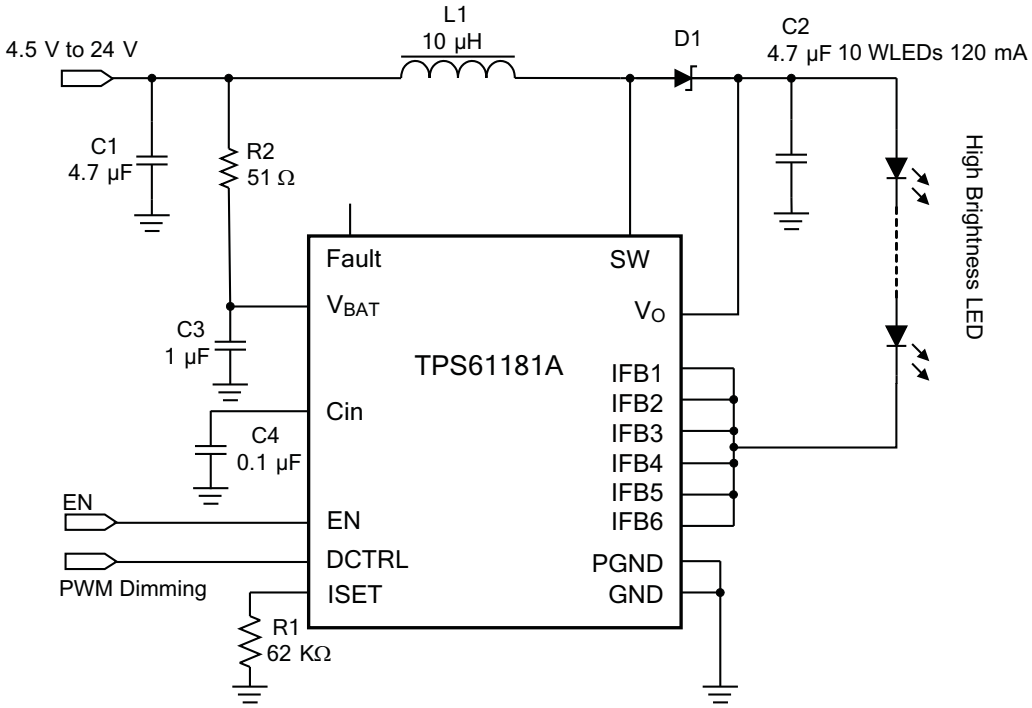


Figure 19. TSP61181A for One String High Brightness LEDs Application

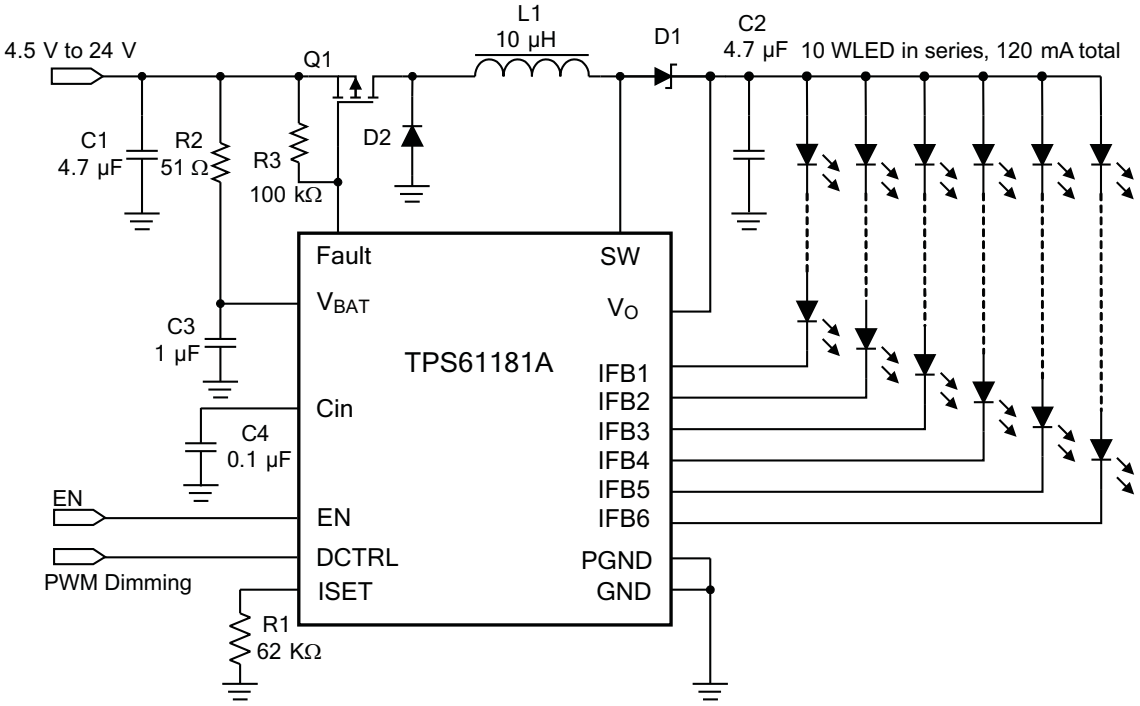


Figure 20. TPS61181A Driving External PFET for True Shutdown Application

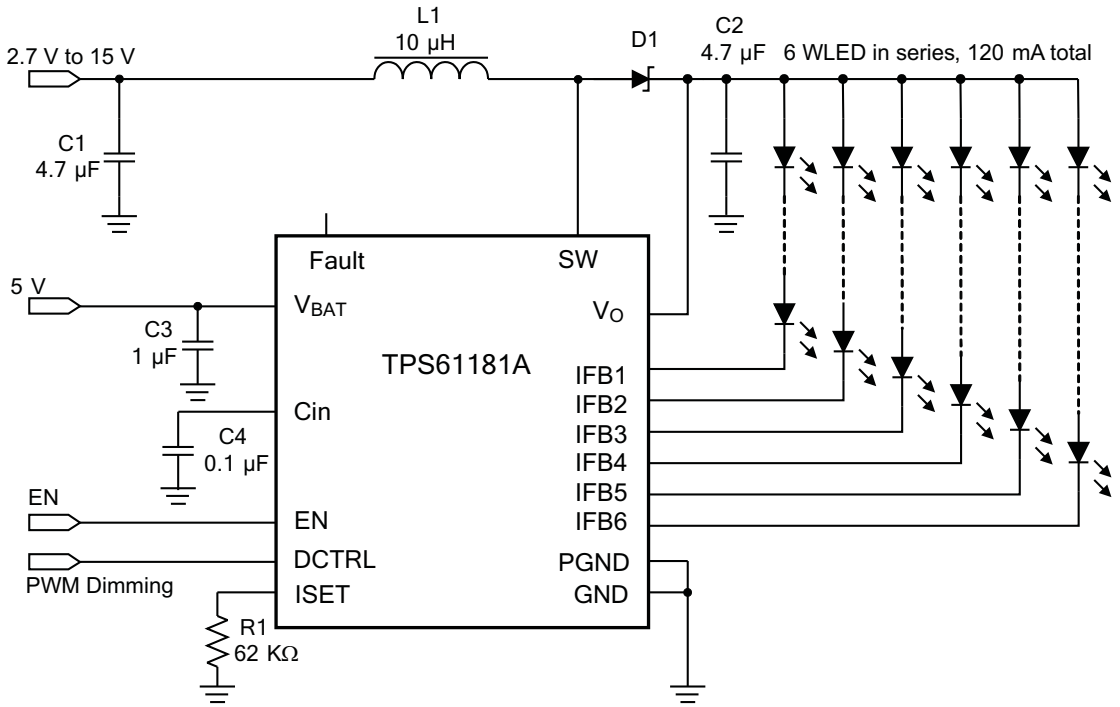


Figure 21. TPS61181A with Separate V_{BAT} Power for Low Voltage Input Application

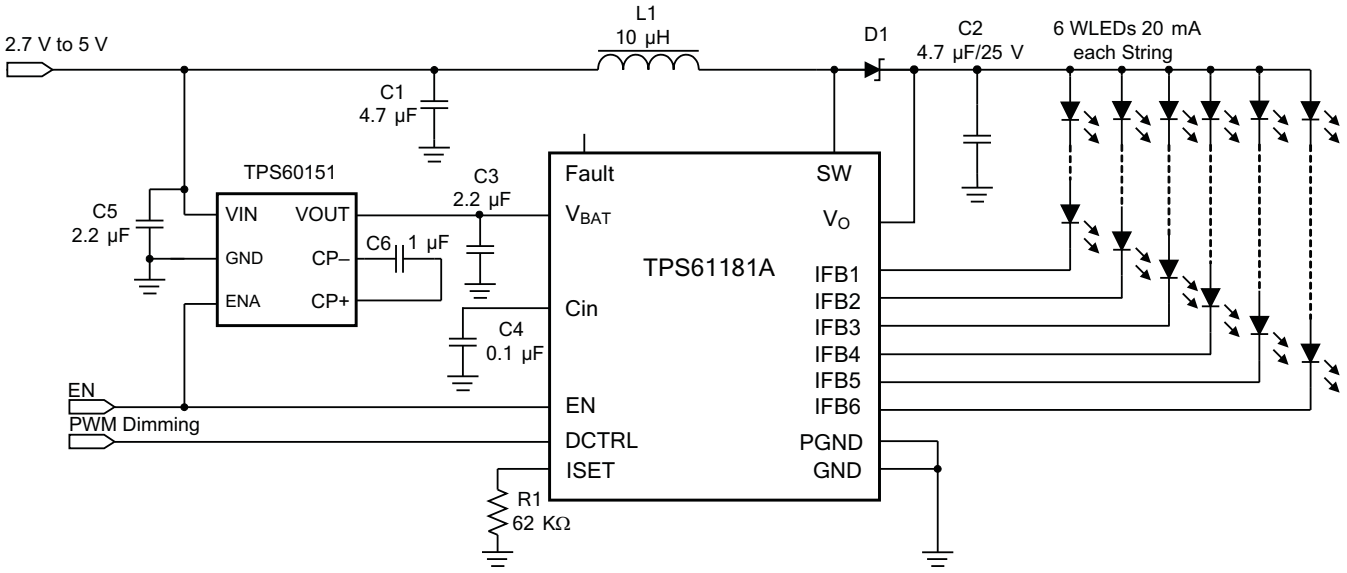


Figure 22. TPS61181A+TPS60151 for One Cell Li-ion Battery Power Application

REVISION HISTORY

Note: Page numbers of current version may differ from previous version.

Changes from Original (February) to Revision A	Page
• Deleted Voltage Range spec for "all other pins" in the Absolute Maximum Ratings table.	2
• Added F_{PWM} spec. for PWM dimming frequency at $D_{PWM} \geq 1\%$ and $D_{PWM} \geq 5\%$	2

重要声明

德州仪器 (TI) 及其下属子公司有权在不事先通知的情况下，随时对所提供的产品和服务进行更正、修改、增强、改进或其它更改，并有权随时中止提供任何产品和服务。 客户在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。 所有产品的销售都遵循在订单确认时所提供的 TI 销售条款与条件。

TI 保证其所销售的硬件产品的性能符合 TI 标准保修的适用规范。 仅在 TI 保修的范围内，且 TI 认为有必要时才会使用测试或其它质量控制技术。 除非政府做出了硬性规定，否则没有必要对每种产品的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。 客户应对其使用 TI 组件的产品和应用自行负责。 为尽量减小与客户产品和应用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 产品或服务的组合设备、机器、流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。 TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。 使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的数据手册或数据表，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。 在复制信息的过程中对内容的篡改属于非法的、欺诈性商业行为。 TI 对此类篡改过的文件不承担任何责任。

在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示授权，且这是非法的、欺诈性商业行为。 TI 对此类虚假陈述不承担任何责任。

可访问以下 URL 地址以获取有关其它 TI 产品和应用解决方案的信息：

产品	
放大器	http://www.ti.com.cn/amplifiers
数据转换器	http://www.ti.com.cn/dataconverters
DSP	http://www.ti.com.cn/dsp
接口	http://www.ti.com.cn/interface
逻辑	http://www.ti.com.cn/logic
电源管理	http://www.ti.com.cn/power
微控制器	http://www.ti.com.cn/microcontrollers
应用	
音频	http://www.ti.com.cn/audio
汽车	http://www.ti.com.cn/automotive
宽带	http://www.ti.com.cn/broadband
数字控制	http://www.ti.com.cn/control
光纤网络	http://www.ti.com.cn/opticalnetwork
安全	http://www.ti.com.cn/security
电话	http://www.ti.com.cn/telecom
视频与成像	http://www.ti.com.cn/video
无线	http://www.ti.com.cn/wireless

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61181ARTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWF	Samples
TPS61181ARTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

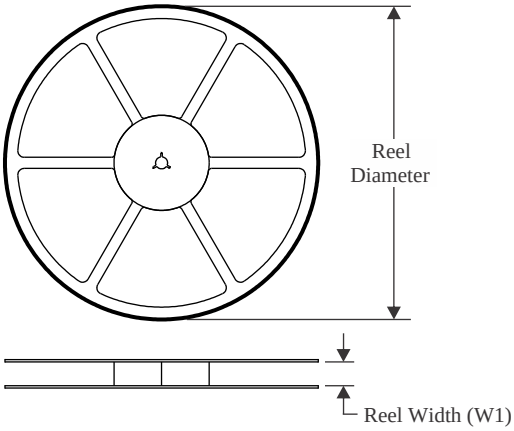
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

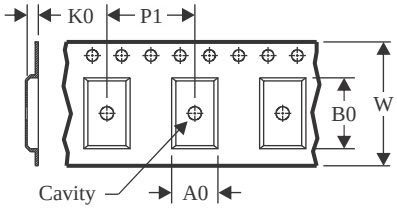
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

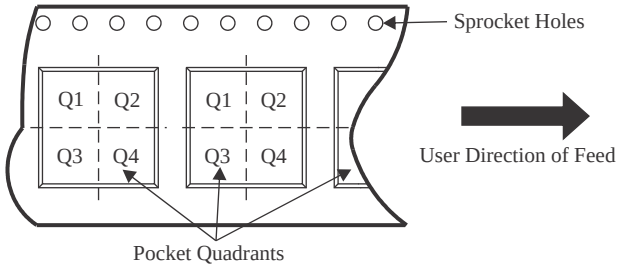


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

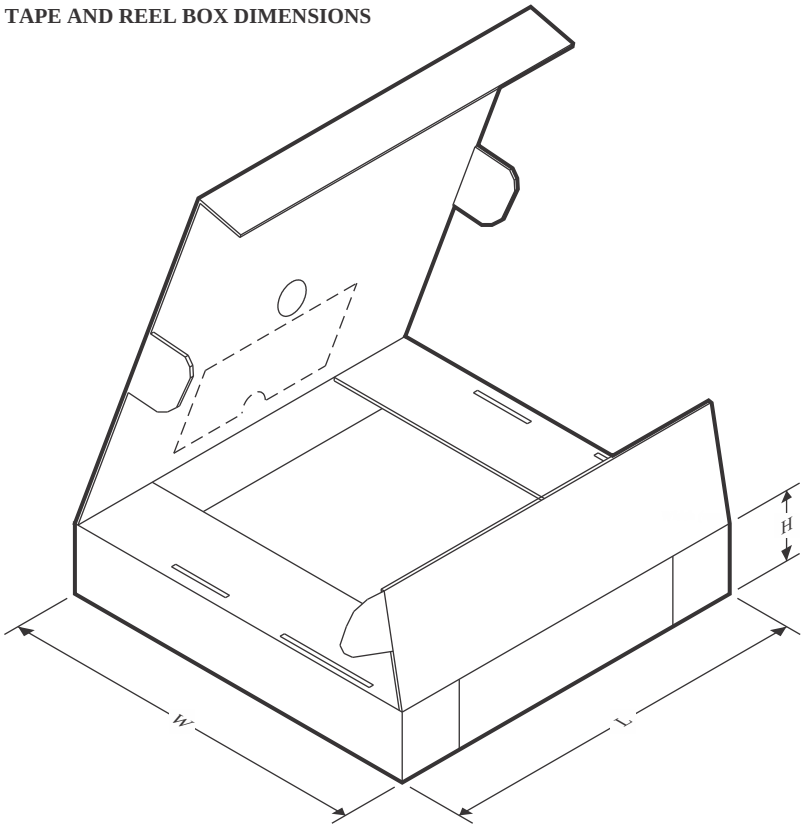
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61181ARTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61181ARTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61181ARTER	WQFN	RTE	16	3000	356.0	356.0	35.0
TPS61181ARTET	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

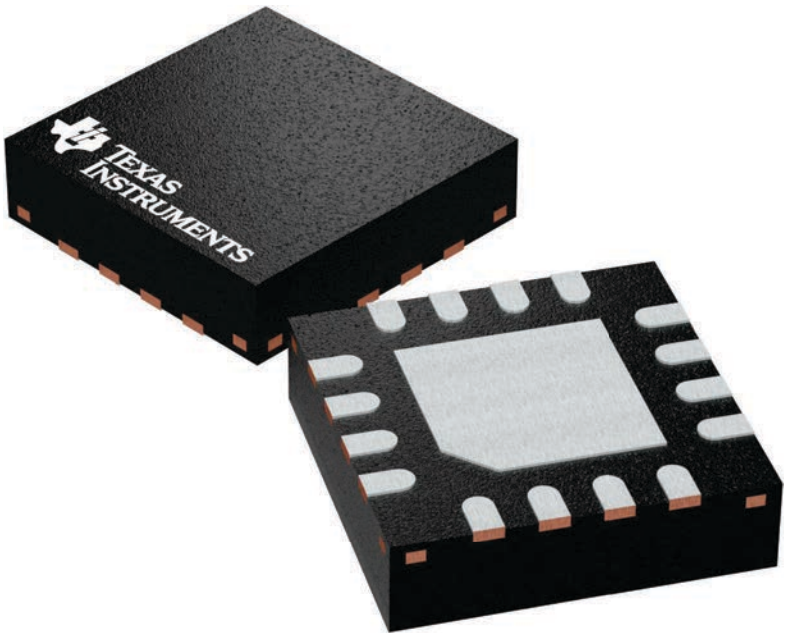
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

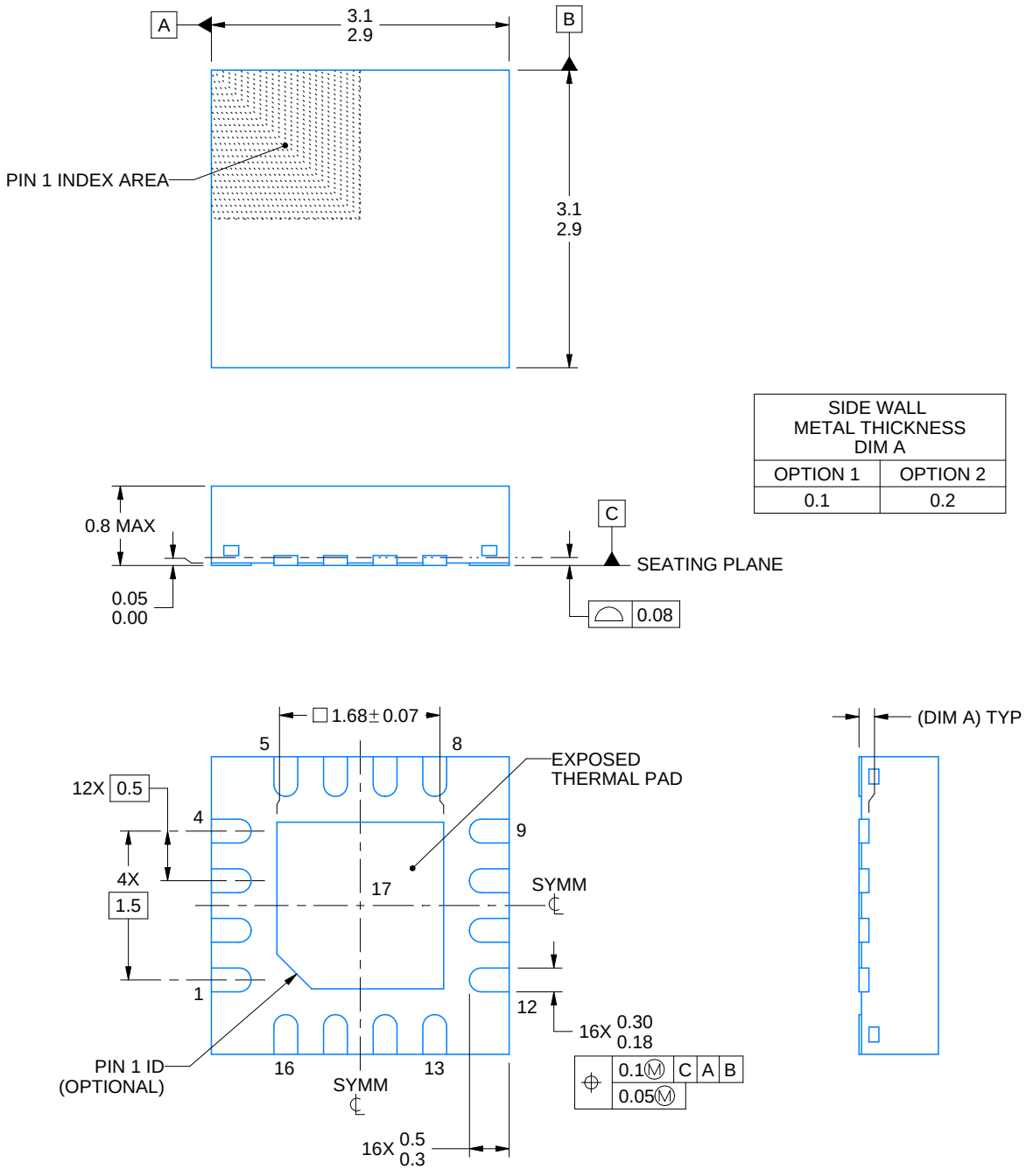


RTE0016C

PACKAGE OUTLINE

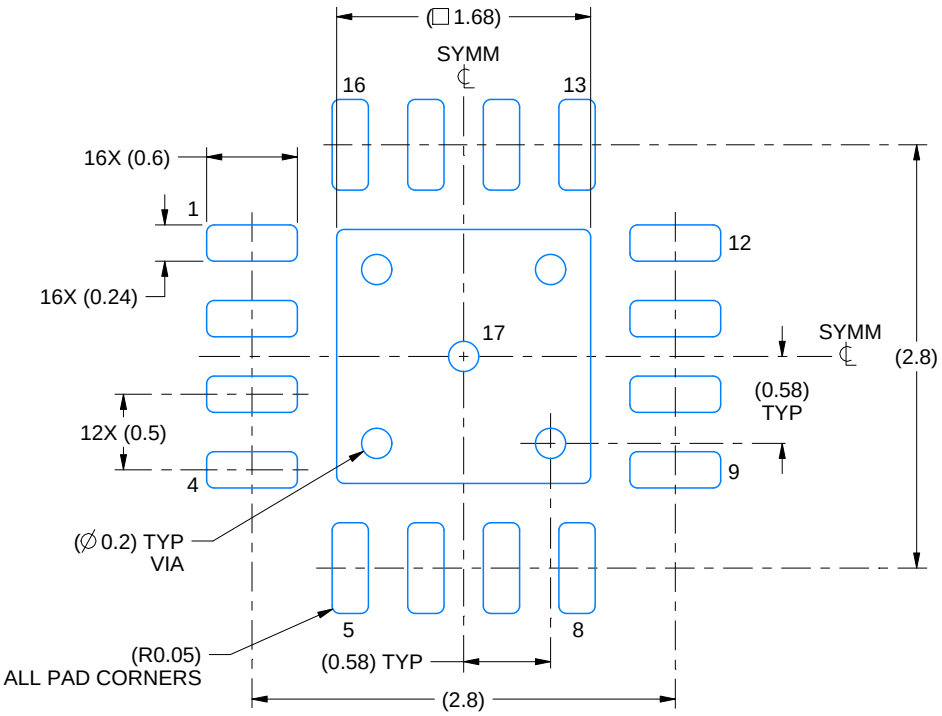
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

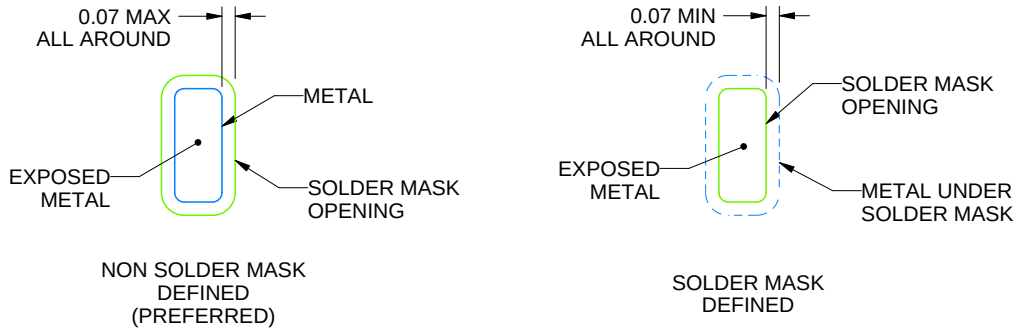


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

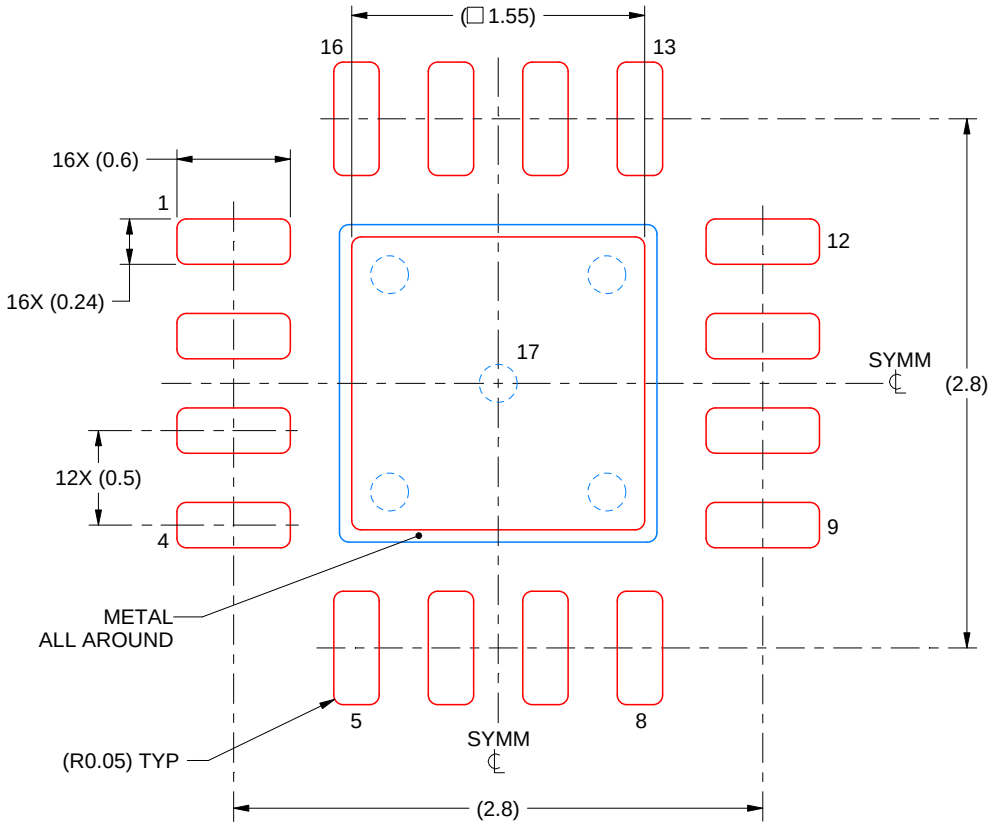


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265