TEXAS INSTRUMENTS

**TPS61390**

ZHCSJN0B −APRIL 2019−REVISED OCTOBER 2019

# TPS61390 85-V$_{OUT}$ 升压转换器，具有电流镜和采样/保持功能

## 1 特性

- 输入电压范围：2.5V 至 5.5V
- 输出电压范围：高达 85V
- 开关 FET 的 R$_{(DS)on}$：0.9Ω
- 开关电流限制：1000mA
- 最短响应时间为 400ns 的采样窗口
- 具有 0.5µs 响应时间的高光功率保护
- 开关频率：700kHz
- 瞬态电流：来自 VIN 时为 110µA，来自 VOUT 时为 340µA，来自 AVCC 时为 140µA
- 软启动时间：4.8ms
- 封装：3mm × 3mm × 0.75mm QFN

## 2 应用

- APD 偏置
- 光线路终端
- 高压传感器电源

## 3 说明

TPS61390 是一个 700kHz 脉宽调制 (PWM) 升压转换器，具有 85V 开关 FET，输入范围为 2.5V 至 5.5V。开关峰值电流高达 1000mA。TPS61390 包括具有两个可选增益选项（1:5 或 4:5）的精确电流镜。

此外，TPS61390 还集成了一个适用于突发模式光学接收器 应用 的采样/保持电路，可捕获流经 APD 的电流并将此电流传递给外部 ADC。当在强弱光学密度之间转换时，此器件可实现快速的响应时间。TPS61390 还提供了高光功率保护，并将一个额外的 FET 与 APD 电源路径串联在一起，典型响应时间为 0.5µs。当高光功率下降时，它能够自动恢复。
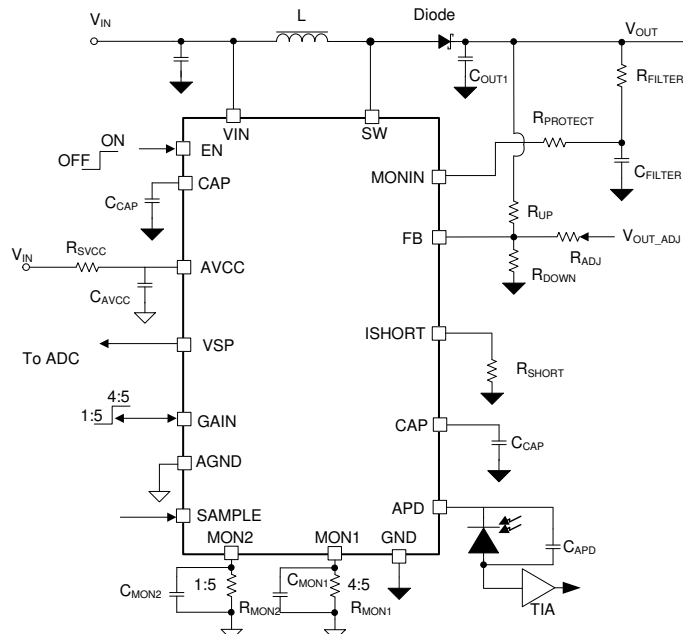
TPS61390 可采用下面带有外露散热垫的 3mm × 3mm QFN 封装。

**器件信息**[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS61390 | WQFN (16) | 3.00mm × 3.00mm |

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路

## 目录

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision A (June 2019) to Revision B**          **Page**

- 已更改 text string in Current Mirror section from "The voltage of MON1 is up to 400 mV......." to "The maximum voltage of MON1 and MON2 is 2.5 V."................................................................................................................ 11

**Changes from Original (April 2019) to Revision A**          **Page**

- 已更改 将状态更改为"生产数据" ............................................................................................................................... 1

# 5 Pin Configuration and Functions

**RTE Package
16-Pin WQFN
Top View**
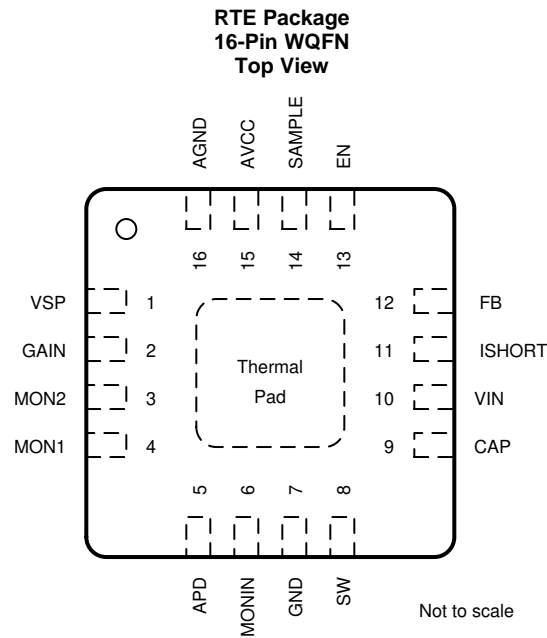


**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VSP | 1 | O | Sample/Hold voltage output with single-ended output. |
| GAIN | 2 | I | GAIN of the current mirror selection indicator of the sample/hold output: |
| | | | Output low: sample/hold for current mirror gain 4 : 5; |
| | | | Output high: sample/hold for current mirror gain 1 : 5; |
| | | | This pin can also be any input pin: |
| | | | Input low: sample/hold for current mirror gain 4 : 5; |
| | | | Input high: sample/hold for current mirror gain 1 : 5 |
| MON2 | 3 | O | Current mirror output pin of 1 : 5 ratio (Mirror current: APD current) |
| MON1 | 4 | O | Current mirror output pin of 4 : 5 ratio (Mirror current: APD current) |
| APD | 5 | O | Power supply for the APD, connect this pin with the cathode of APD |
| MONIN | 6 | I | Current mirror input pin |
| GND | 7 | – | Power Ground |
| SW | 8 | PWR | The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET |
| CAP | 9 | O | Connecting a capacitor externally to lower the noise for current mirror. |
| VIN | 10 | I | IC power supply input |
| ISHORT | 11 | O | Programming the current limit for high optical power protection by a resistor between this pin and GND. |
| FB | 12 | I | Feedback voltage |
| EN | 13 | I | Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode |
| SAMPLE | 14 | I | The sample trigger pin, the rising edge of this pin to trigger the sample and falling edge to hold the sampled voltage. |
| AVCC | 15 | I | Power supply for the sample/hold circuitry |
| AGND | 16 | – | Analog ground for the sample / hold and current mirror circuitry |
| Exposed Thermal Pad | | | Connect with GND, TI recommends connecting to Power GND on PCB |

# 6 Specifications

## 6.1 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.5 | | 5.5 | V |
| $V_{OUT}$ | Output voltage | 20 | | 85 | V |
| $T_J$ | Junction temperature | −40 | | 125 | °C |
| L | Effective Inductance | | 4.7 | | µH |
| $C_{IN}$ | Effective Input Capacitance | | 1 | | µF |
| $C_{OUT}$ | Effective Output Capacitance | | 0.1 | | µF |

## 6.2 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | SW, APD, MONIN,CAP | −0.3 | 85 | V |
| | Other pins | −0.3 | 6 | V |
| $T_J$ | Operating junction temperature | −40 | 125 | °C |
| $T_{stg}$ | Storage temperature | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.3 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins[1] | ±1500 | V |
| | | Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.4 Thermal Information

|  | THERMAL METRIC[1] | TPS61390 | UNIT |
|---|---|---|---|
| | | RTE (WQFN) | |
| | | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 52.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 27.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 2.0 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 27.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 12.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

Over recommended free-air temperature range, $V_{IN}$ = 3.3 V, $AV_{CC}$ = 3.3 V, $V_{MONIN}$ = 20 V to 85 V, $T_J$ = - 40°C to 125°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | | 2.5 | | 5.5 | V |
| $V_{UVLO}$ | Under voltage lock out | $V_{IN}$ falling | | 2.4 | 2.5 | V |
| | Under voltage lock out hysteresis | $V_{UVLO}$ rising - $V_{UVLO}$ falling | | 200 | | mV |
| $I_{Q\_IN}$ | Quiescent current into VIN pin | $V_{IN}$ = 3.3 V, $V_{FB}$ =$V_{REF}$ + 0.1 V, No switching, -40 °C ≤ $T_J$ ≤ 85 °C | | 110 | 140 | uA |
| $I_{Q\_OUT}$ | Quiescent current into VOUT pin | $V_{IN}$ = 3.3 V, $V_{FB}$ =$V_{REF}$ + 0.1 V, No switching, -40 °C ≤ $T_J$ ≤ 85 °C | | 340 | 430 | uA |
| $I_{Q\_VCC}$ | Quiescent current into AVCC pin | AVCC = 3.3 V  -40 °C ≤ $T_J$ ≤ 85 °C | | 140 | 180 | uA |
| $I_{SD}$ | Shutdown current into VIN pin | 2.5 V ≤ VIN ≤ 5.5 V, EN = 0, -40 °C ≤ $T_J$ ≤ 85 °C | | | 1 | uA |
| | Shutdown current into VOUT pin | EN = 0, -40 °C ≤ $T_J$ ≤ 85 °C | | | 1 | uA |
| | Shutdown current into AVCC pin | AVCC = 3.3 V, EN = 0, -40 °C ≤ $T_J$ ≤ 85 °C | | | 1 | uA |
| **OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage range | | | | 85 | V |
| $V_{REF}$ | Feedback regulation reference voltage | $V_{IN}$ = 2.5 V to 5.5 V, $T_J$ = 25 °C | 1.188 | 1.2 | 1.212 | V |
| | | $V_{IN}$ = 2.5 V to 5.5 V, -40 °C ≤ $T_J$ ≤ 125 °C | 1.182 | 1.2 | 1.218 | V |
| $I_{FB}$ | Feedback input leakage current | | | 1 | 25 | nA |
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | Low-side FET on resistance | 3 V ≤ $V_{IN}$ ≤ 5.5 V | | 900 | 1300 | mΩ |
| **SWITCHING CHARACTERISTIC** | | | | | | |
| $f_{SW}$ | Switching frequency | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 60 V | 600 | 700 | 800 | kHz |
| **CURRENT MIRROR** | | | | | | |
| $k_{MON1}$ | 4:5 Current mirror gain | $I_{APD}$ = 5 µA to 200 µA | 0.76 | 0.8 | 0.84 | |
| $k_{MON2}$ | 1:5 Current mirror gain | $I_{APD}$ = 100 µA to 2 mA | 0.19 | 0.2 | 0.21 | |
| $V_{MON}$ | MON1 / MON2 Threshold | | 380 | 400 | 420 | mV |
| $V_{APD\_DRP}$ | Current mirror voltage drop | $I_{APD}$ = 1 mA | 2.2 | 2.5 | 2.8 | V |
| | | $I_{APD}$ = 5 µA | | 2.45 | | V |
| $I_{BIAS}$ | Current mirror bias current | | 15 | 20 | 25 | µA |
| **SAMPLE / HOLD** | | | | | | |
| $V_{ERROR}$ | Sample/hold output error steady,+/-6 sigma | $I_{APD}$ = 20 uA, GAIN = 0.8, $R_{MON}$ = 3 kΩ | -15 | | +15 | % |
| $V_{ERROR}$ | Sample/hold output error steady,+/-6 sigma | $I_{APD}$ = 500 µA, GAIN = 0.2, $R_{MON}$ = 3 kΩ | -5 | | +5 | % |
| $t_{SP\_DEL}$ | Amplifier settling down time | | | | 10 | µs |
| $t_{GAIN\_COMP}$ | Gain selection comparator time | +/-20% gap of threshold | | | 8 | µs |
| $V_{DROP\_SP}$ | Drop voltage during sample/hold | Sample voltage sensing value variation at 10-100 µs, (Max-Min)/Average | | | 1 | % |
| **CURRENT LIMIT** | | | | | | |
| $I_{LIM\_SW}$ | Peak switching current limit | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 60 V | 800 | 1000 | 1200 | mA |
| $I_{SHORT}$ | High optical power current limit | $R_{ISHORT}$ = 25 kΩ | 3.7 | 4 | 4.3 | mA |
| | | $R_{ISHORT}$ = 50 kΩ | 1.8 | 2 | 2.2 | mA |

## Electrical Characteristics (continued)

Over recommended free-air temperature range, $V_{IN}$ = 3.3 V, $AV_{CC}$ = 3.3 V, $V_{MONIN}$ = 20 V to 85 V, $T_J$ = - 40°C to 125°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CONTROL (EN, SAMPLE, GAIN)** | | | | | | |
| $V_{EN\_H}$ | EN Logic high threshold | | | | 1.2 | V |
| $V_{EN\_L}$ | EN Logic low threshold | | 0.4 | | | V |
| $R_{EN}$ | EN pull down resistor | | | 800 | | kΩ |
| $V_{SAMPLE\_H}$ | Sample Logic high threshold | | | | 0.7 x AVCC | V |
| $V_{SAMPLE\_L}$ | Sample Logic low threshold | | 0.3 x AVCC | | | V |
| $V_{GAIN\_H}$ | Gain Logic high threshold | | | | 0.7 x AVCC | V |
| $V_{GAIN\_L}$ | Gain Logic low threshold | | 0.3 x AVCC | | | V |
| $R_{GAIN\_OUT}$ | Output resistor | | | 5.5 | | kΩ |
| **TIMING** | | | | | | |
| $t_{SS}$ | Soft start time | Ref voltage 0 to 1.2V | | 4.8 | | ms |
| $t_{DELAY}$ | Delay time for high optical power protection | $I_{APD}$ = 5 mA, $I_{SHORT}$ = 3 mA | | 0.5 | | µs |
| **THERMAL PROTECTION** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold | $T_J$ rising | | 150 | | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | $T_J$ falling below $T_{SD}$ | | 20 | | °C |

## 6.6 Typical Characteristics



$V_{IN}$ = 3.3 V          L = 4. 7 µH          $C_{OUT}$ = 0.1 µF
Output current
(boost) = 0 to 8 mA
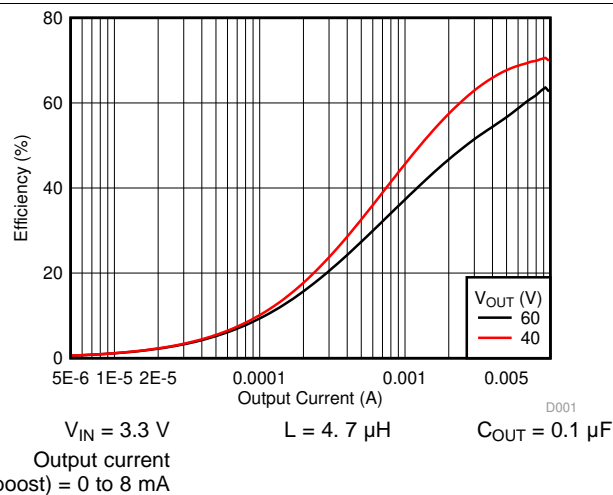
**图 1. Efficiency vs. Output Current**



$V_{IN}$ = 3.3 V          L = 4. 7 µH          $C_{OUT}$ = 0.1 µF
Output current
(boost) = 0 to 8 mA

**图 2. Load regulation**



$V_{IN}$ = 3.3 V          $V_{OUT}$ = 60 V          $C_{OUT}$ = 0.1 µF
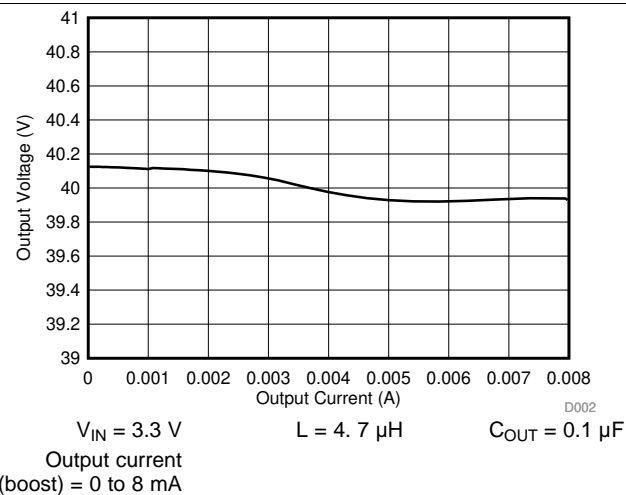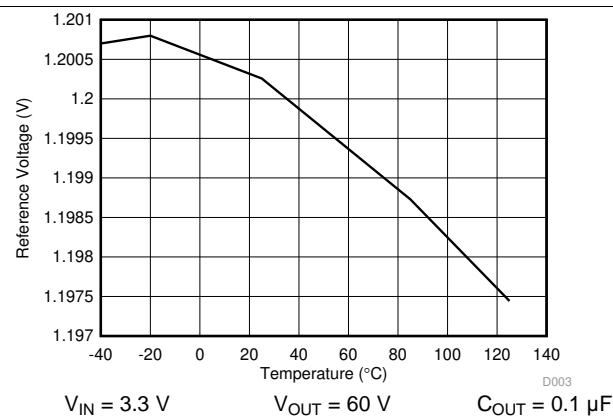
**图 3. Reference voltage**



$V_{OUT}$ = 60 V
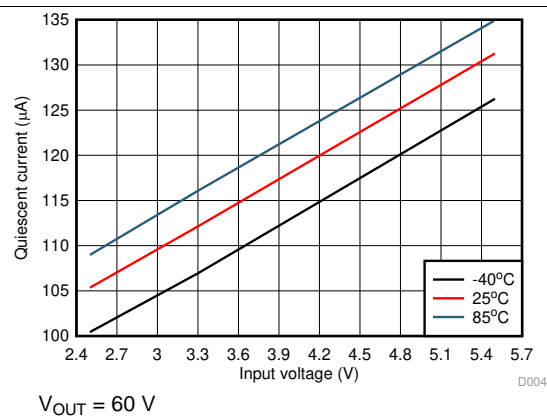
**图 4. Quiescent current vs. Input voltage**



$V_{IN}$ = 3.3 V
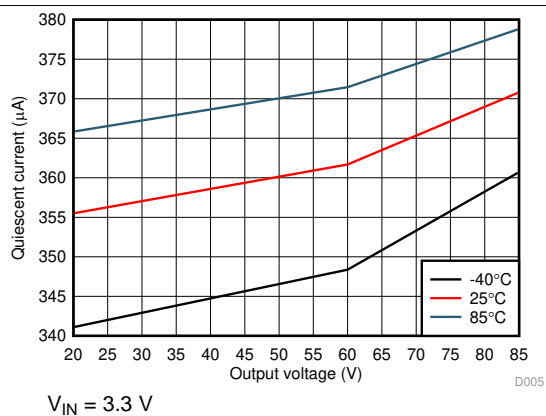
**图 5. Quiescent current vs. Output voltage**



$V_{IN}$ = 3.3 V          $V_{OUT}$ = 60 V
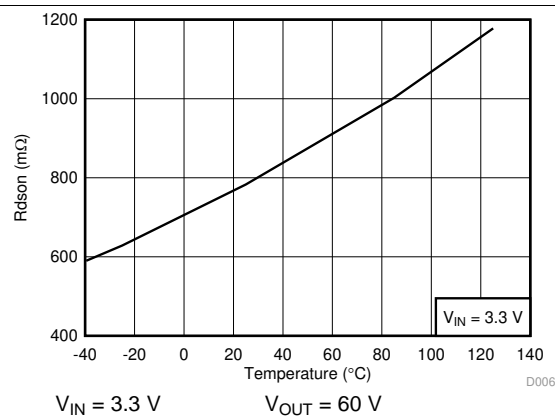
**图 6. Rdson vs. Temperature**

## Typical Characteristics (接下页)



$V_{OUT}$ = 60 V

**图 7. Vin UVLO**



$V_{IN}$ = 3.3 V          $V_{OUT}$ = 60 V
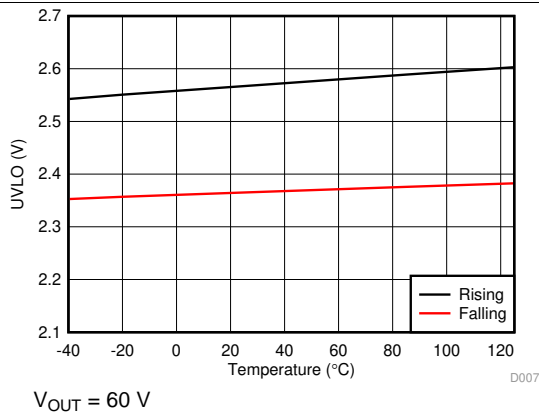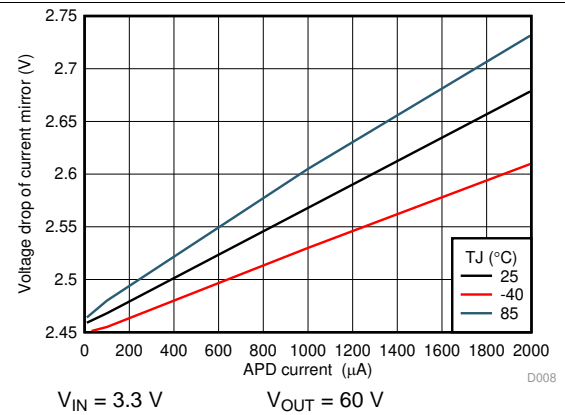
**图 8. Voltage drop of current mirror vs. current**



$V_{IN}$ = 3.3 V          $V_{OUT}$ = 60 V
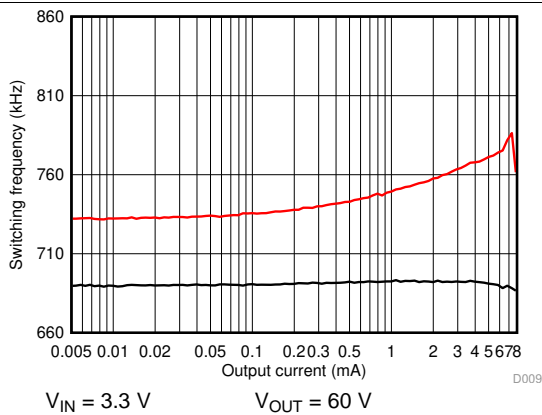
**图 9. Switching frequency vs. Output current**



$V_{IN}$ = 3.3 V          $V_{OUT}$ = 60 V

**图 10. VSP voltage vs. APD current**
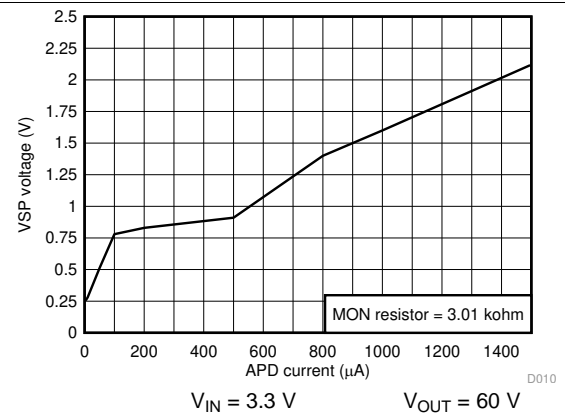
# 7 Detailed Description

## 7.1 Overview

The TPS61390 is a fully integrated boost converter with an 85-V FET to convert a low input voltage to a higher voltage for biasing the APD. The TPS61390 supports an input voltage ranging from 2.5 V to 5.5 V. The device operates at a 700 kHz pulse-width modulation (PWM) crossing the whole load range.

The device can accurately mirror the APD current ranging from 0.5 uA to 2 mA. There are two ratio options for the current proportional to APD current: the MON1 (4 : 5) and MON2 (1 : 5). By connecting a resistor from the mirror output (MON1 or MON2) to GND, the current flowing through the APD is converted into the voltage crossing the resistor from MON1 / MON2 to GND.

With the sample / hold circuitry built-in and triggered by an external sampling clock, the current mirror signal (voltage) is transferred and stored on the holdup capacitor, the voltage on the holdup capacitor is then passed over to the output of an operational amplifier. An external ADC can sense the voltage of the output of the operational amplifier to measure the optical intensity.

Additionally, a high power optical protection is integrated by clamping the pre-set current limit (program by the $I_{SHORT}$ resistor). The response time of the high optical power is typically 0.5 µs. The device could recovery automatically when the high optical power is removed.

The device comes in a 3-mm × 3-mm QFN package with the operating junction temperature covering from –40°C to 125°C.

## 7.2 Functional Block Diagram
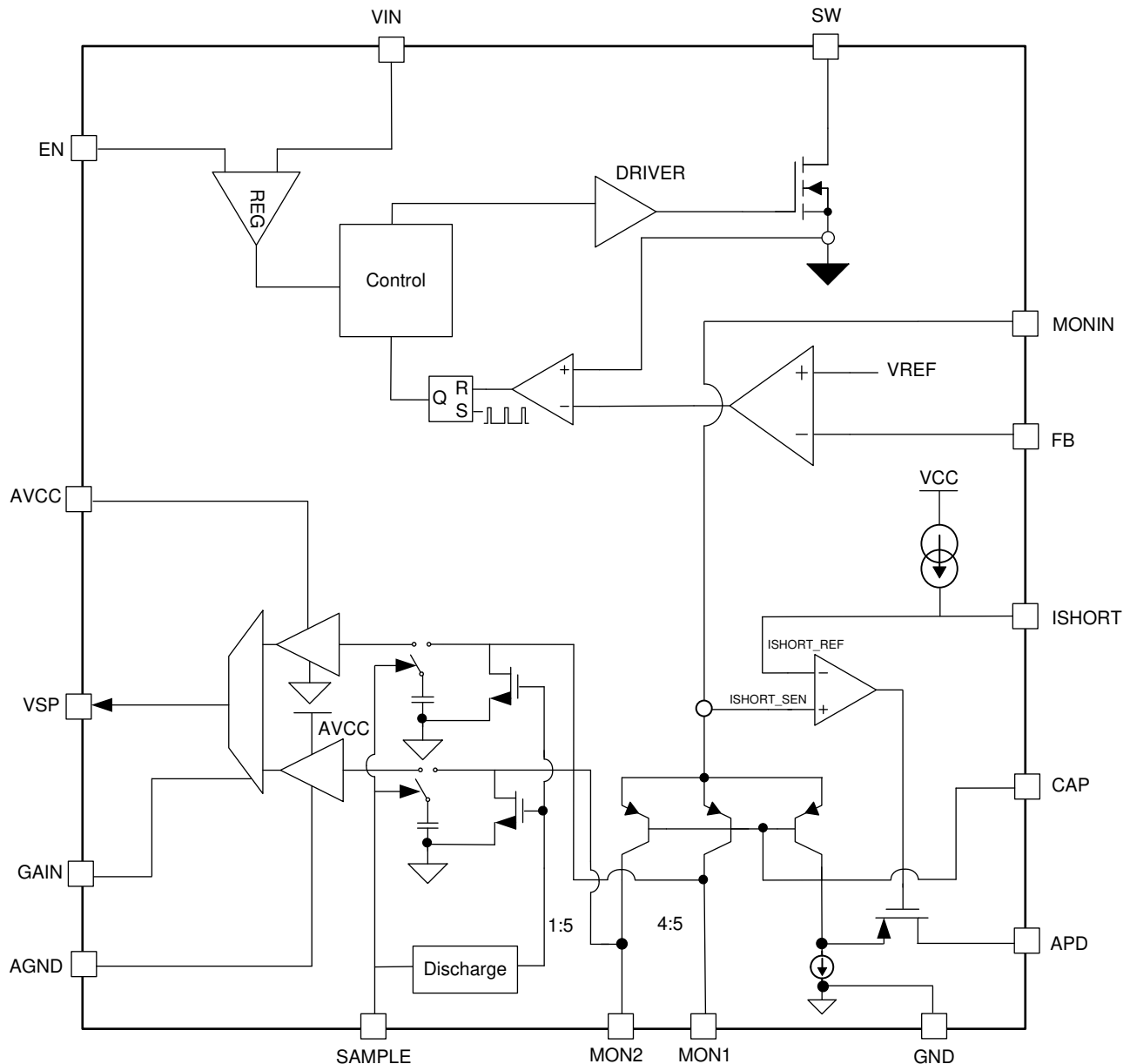


## 7.3 Feature Description

### 7.3.1 Undervoltage Lockout

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 2.5 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 200 mV.

### 7.3.2 Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 2.5 V and the EN pin is pulled above the high threshold (1.2 V min.), the TPS61390 is enabled. When the EN pin is pulled below the low threshold (0.4 maximum), the device goes into shutdown mode.

**Feature Description (接下页)**

### 7.3.3 Current Mirror

There are two current mirror options for TPS61390: the gain of 4: 5 (MON1) and 1: 5 (MON2). The maximum voltage of MON1 and MON2 is 2.5 V.

### 7.3.4 Sample and Hold

The TPS61390 has the sample-and-hold circuitry built in, including a holdup capacitor for storing the voltage capture, a FET switch, and one operational amplifier, illustrated in *Functional Block Diagram*.

To sample the current mirror signal, the switch connects the capacitor to the input of the common-mode operational amplifier. The amplifier converts the voltage of the capacitor to the output terminal with 4:1 ratio.

In hold mode the switch disconnects the hold-up capacitor from the operation amplifier, the voltage of the capacitor is discharged to 0 before connecting with current mirror output terminal (MON1 and MON2).

These are two ratios of the current mirror that can be selected automatically by comparing the MON1 voltage with the internal 400-mV reference. The voltage of MON1 is sampled if the MON1 voltage is below 400 mV, while the voltage of MON2 is sampled if MON1 being larger than 400 mV. The GAIN pin reports which ratio is selected for the sample and hold, the logic low (0) for MON1 while logic high (AVCC) for MON2 selected.

Also, the GAIN can be externally selected, pulling low to select the 1 : 5 while high for 4 : 5 ratio.

The voltage measured on VSP pin is calculated by 公式 1 and 公式 2 :

$$VSP = 4 \times \left(0.8 \times I_{APD} \times RMON1\right) + 4 \times \left(I_{BIAS} \times RMON1\right)$$

where

- VSP is the voltage sampled on VSP pin
- $I_{APD}$ is the current flowing through the APD pin.
- RMON1 is the resistor connecting with MON1 pin
- $I_{BIAS}$ is the bias current of current mirror                                                                                  (1)

$$VSP = 4 \times \left(0.2 \times I_{APD} \times RMON2\right) + 4 \times \left(I_{BIAS} \times RMON2\right)$$

where

- RMON2 is the resistor connecting with MON2 pin                                                                            (2)

The bias current is around 20 µA (typical) when there is no APD current flowing through. The bias voltage of MON1 or MON2 is 60 mV given a 3-kΩ MON resistor connected with MON1 or MON2. Also, the VSP voltage is reset to 250 mV prior to every sample clock coming. The maximum voltage of the MON1 is clamped to 400 mV while maximum of MON2 is 2.5 V. The maximum voltage of VSP is close to the $A_{VCC}$ (0.1 V lower typically), which is the supply voltage of the sample and hold circuitry.

As the timing diagram shown in 图 11, the sample and hold is enabled by the rising edge of an external clock connecting to the SAMPLE pin, the holdup capacitor captures the voltage of current mirror signal (the voltage of MON1 and MON2).

At the falling edge, the sampling is stopped, and the voltage stored on the holdup capacitor is transferred to the output of the operational amplifier. The minimum time of the sampling time the TPS61390 supports is 350 ns (typically). The voltage on the stored capacitor is switched to the amplifier's input voltage. There is approximately 10-µs delay time to make the output voltage of the amplifier ready.

The GAIN selector is always active and the GAIN value is captured by the falling edge of the sample signal.
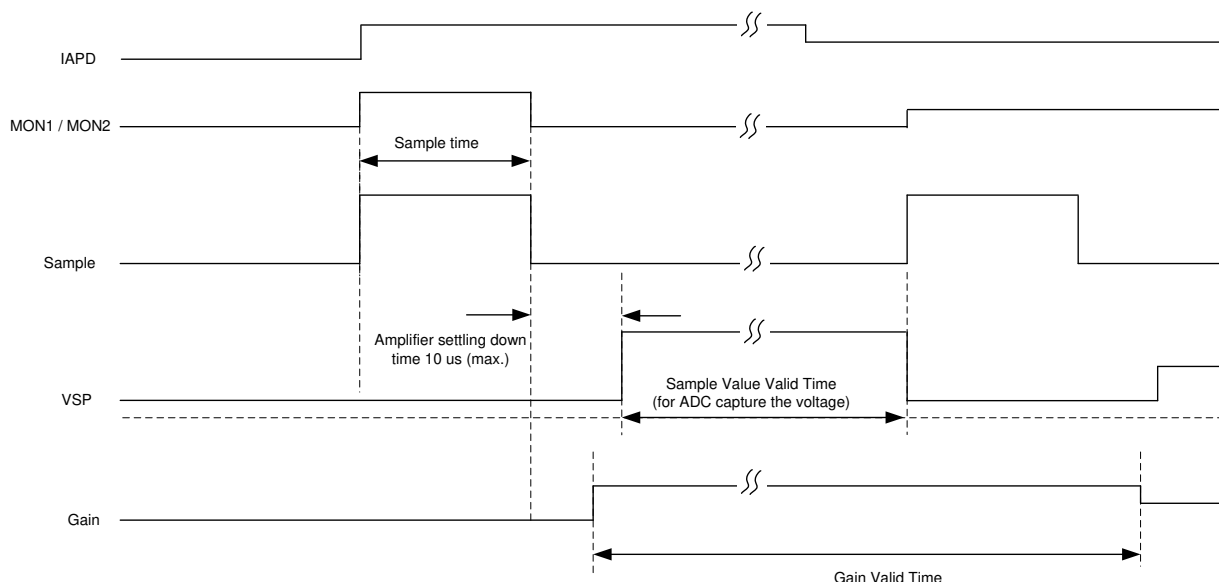
**Feature Description (接下页)**



**图 11. TPS61390 Sample / Hold Circuit Timing**

The output settling time of the operational amplifier is 10 µs while the maximum duration time is 100 µs with 1% derating (with the nominal voltage).

### 7.3.5 High Optical Power Protection

There is an additional FET in series of power path connecting with the APD. When the current flowing through the APD exceeds the short protection threshold (set by connecting the resistor from $I_{SHORT}$ to GND), the on resistance of the FET becomes larger to clamp the current within the protection threshold by lowering the APD bias voltage. It takes typically 0.5 µs for the FET to respond in case of high optical power occuring.

When the high optical power condition releases, the TPS61390 recovers automatically back to the normal operation mode.

## 7.4 Device Functional Mode

### 7.4.1 PFM Operation

The TPS61390 integrates a power save mode with pulse frequency modulation (PFM) at the light load. When a light load condition occurs, the COMP pin voltage naturally decreases and reduces the peak current. When the COMP pin voltage further goes down with the load lowered and reaches the pre-set low threshold, the output of the error amplifier is clamped at this threshold and does not go down any more. If the load is further lowered, the device skips the switching cycles and reduces the switching losses and improves efficiency at the light load condition by reducing the average switching frequency.

# 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS61390 is a step-up DC/DC converter with current monitor and sample / hold circuitry integrated. The following design procedure can be used to select component values for the TPS61390. This section presents a simplified discussion of the design process.

## 8.2 Typical Application

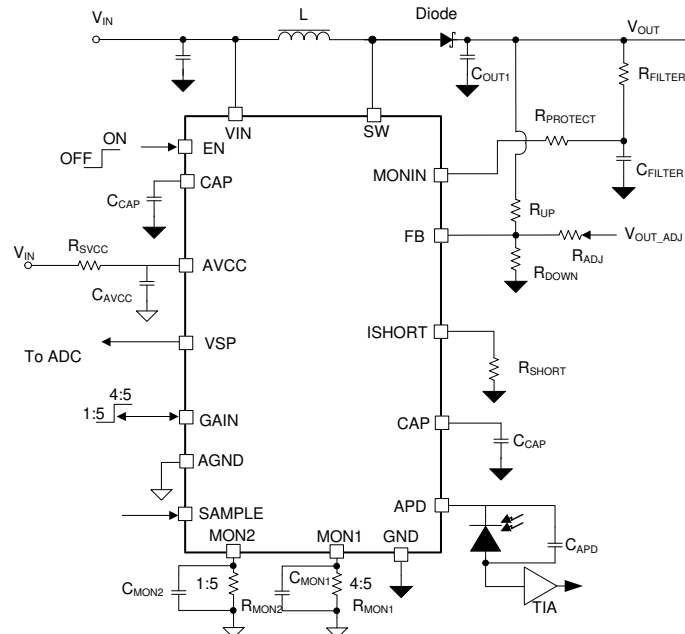This application is designed for 2.5-V to 5.5-V input, and 60-V output user case



图 12. TPS61390 Typical Application

### 8.2.1 Design Requirement

For this design example, use 表 1 as the design parameters.

表 1. Design Parameters

| PARAMETER | VALUE |
| --- | --- |
| Input voltage range | 2.5 V to 5.5 V |
| Output voltage | 60 V |
| Operating frequency | 700 kHz |
| APD Current | 0 to 2 mA |

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Selecting the Rectifier Diode

A Schottky diode is the preferred type for the rectifier diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus the switching node ringing. Also, it must be able to handle the average output current.

#### 8.2.2.2 Selecting the Inductor

It is suggested that the TPS61390 device works in the DCM operation; otherwise the output voltage would not be delivered for low input voltage to high output voltage.

With the device working in DCM operation, the maximum inductor could be calculated by equation 公式 3 and 公式 4:

$$L_{MAX} = \frac{V_{IN} \times D}{f_{SW} \times I_{LIM}}$$

where

- $V_{IN}$ is input voltage
- D is duty cycle
- $f_{SW}$ is switching frequency
- $I_{LIM}$ is current limit (3)

For instance, if $V_{IN}$ = 3.3 V, $V_{OUT}$ = 60 V, $f_{SW}$ = 600 kHz, $I_{LIM}$ = 0.8 A, the $L_{MAX}$ = 6.5 µH

However, there is minimum inductance is determined by the power delivered to the output side at given input condition.

$$L_{MIN} = 2 \times \frac{V_{OUT} \times I_{OUT}}{eff \times f_{SW} \times I_{LIM}^2}$$

where

- $V_{OUT}$ is output voltage
- $I_{OUT}$ is output current
- eff is the efficiency
- $f_{SW}$ is switching frequency
- $I_{LIM}$ is current limit (4)

For instance, if $I_{OUT}$ = 8 mA, $V_{OUT}$ = 60 V, $f_{SW}$ = 600 kHz, $I_{LIM}$ = 0.8 A, eff = 0.6, the $L_{MIN}$ = 4.2 µH

With the calculation aforementioned, the operating inductor is recommended between the $L_{MIN}$ and $L_{MAX}$.

The 4.7 µH inductance is optimum value for using the TPS61390 in application.

#### 8.2.2.3 Selecting Output Capacitor

Use low ESR capacitors at the output to minimize output voltage ripple. Use only X5R and X7R types, which retain their capacitance over wider voltage and temperature ranges than other types. Typically use a 0.1-µF to 1-µF capacitor for output voltage. Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate its capacitance at its rated voltage. Therefore, consider enough margins on the voltage rating to ensure adequate capacitance at the required output voltage.

#### 8.2.2.4 Selecting Filter Resistor and Capacitor

TI recommends an additional R-C filter be added for low ripple applications. The filter parameters is characterized based on the ripple requirement. Typically, use a 100-Ω and 0.1-µF filter to reduce the switching output ripple.

#### 8.2.2.5 Setting the Output Voltage

The output voltage of the TPS61390 is externally adjustable using a resistor divider network. The relationship between the output voltage and the resistor divider is given by 公式 5.

$$V_{OUT} = V_{FB} \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

where

- $V_{OUT}$ is the output voltage
- $R_{UP}$ the top divider resistor
- $R_{DOWN}$ is the bottom divider resistor                                                    (5)

Choose $R_{DOWN}$ to be approximately 10 k$\Omega$. Slightly increasing or decreasing $R_{DOWN}$ can result in closer output voltage matching when using standard value resistors. In this design, $R_{DOWN}$ = 10 k$\Omega$ and $R_{UP}$ = 487 k$\Omega$, resulting in an output voltage of 60 V.

### 8.2.2.6  Selecting Sample Window

A pulse signal is connected with SAMPLE pin; the minimum window is 350 ns while the frequency of the pulse is lower than 100 kHz.

### 8.2.2.7  Selecting Capacitor for CAP pin

TI recommends placing a ceramic capacitor from CAP pin to GND to lower the noise for the APD current mirror. A ceramic capacitor between 10 nF and 100 nF is recommended from CAP pin to GND.

### 8.2.2.8  Selecting Capacitor for AVCC pin

The control circuitry is powered by AVCC. A ceramic capacitor must be placed close to AVCC, with a typical capacitor value of 2.2 µF.

### 8.2.2.9  Selecting Capacitor for APD pin

A ceramic capacitor is required to make the APD current mirror more accurately against the noise coupling. The recommended values are from 100 pF to 470 pF.

### 8.2.2.10  Selecting the Resistors of MON1 or MON2

The TPS61390 provides two currents proportional to APD current on the MON pins, 4 : 5 and 1 : 5. The voltage of the resistors connecting to the MON pins convert the APD current to voltage. The relation between APD current and the voltage on MON 1 or MON 2 pins is shown in 公式 1 and 公式 2 .

The resistor value depends on the VSP pin voltage. While RC time constant of MON 1 and MON 2 is recommended to be 1/10 of the sample window time.

### 8.2.2.11  Selecting the Capacitors of MON1 or MON2

The capacitors are added to the MON1 or MON2 pins to decouple the noise of APD transient current. Suggested RC time (formed by the MON1 or MON2 is 1/10 with that of the sample window. With 3-k$\Omega$ $R_{MON}$ resistance, TI recommends a 10-pF capacitor connecting MON1 or MON2 pins to make sure the voltage on MON1 or MON2 is stable before sample signal coming.

It is recommended that RC time constant of MON 1 and MON 2 is around 1/10 of the sample window time.

### 8.2.2.12  Selecting the Resistor of Gain pin

The GAIN pin can be configured as both input and output. If the GAIN pin is configured as output pin, TI recommends that it be directly connected with the external I/O.

If the pin is configured as the input pin to select the current mirror ratio, the pull up or pull down resistor must be lower than 1-k$\Omega$ as there is an internal 5-k$\Omega$ resistor on the GAIN pin.

### 8.2.2.13  Selecting the Short Current Limit

The output current short-protection threshold of the TPS61390 can be programmed by an external resistor with 公式 6 .The short protection threshold is calculated by 公式 1 and 公式 2:

$$I_{SHORT} = \frac{100}{R_{SHORT}}$$

where

- $I_{SHORT}$ (mA) is the short protection threshold
- $R_{SHORT}$(kΩ) is the resistor connecting from ISHORT pin to GND

(6)

For instance, if $R_{SHORT}$ = 25 kΩ, the $I_{SHORT}$ = 4 mA.

## 8.2.3 Application Curves

Typical condition $V_{IN}$ = 3.3 V, $V_{OUT}$ = 60 V, $R_{SHORT}$ = 5 kΩ, $R_{MON1/2}$ = 3.01 kΩ and $C_{MON1/2}$ = 10 pF.
Application waveforms are measured with the inductor 4.7 µH and the output capacitance 0.1 µF at room temperature.



| $V_{IN}$ = 3.3 V | $V_{OUT}$ = 60 V | APD current = 1mA to 5 µA transient |
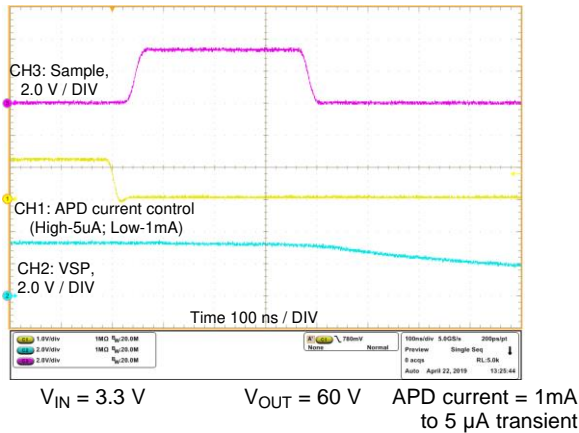
图 13. APD current transient



| $V_{IN}$ = 3.3 V | $V_{OUT}$ = 60 V | APD current = 0 to 4 mA transient |
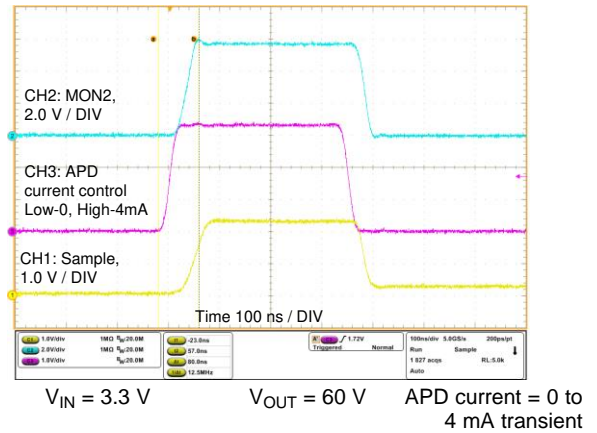
图 14. High optical current protection



| $V_{IN}$ = 3.3 V | $V_{OUT}$ = 60 V | APD current = 1 mA |
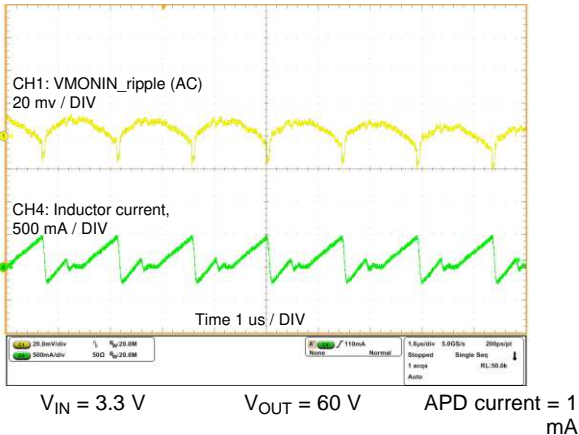
图 15. Output voltage ripple with 100 Ω / 0.1 µF filter



| $V_{IN}$ = 3.3 V | $V_{OUT}$ = 60 V | APD current = 1 mA |

图 16. MON 1 settling time

$V_{IN}$ = 3.3 V     $V_{OUT}$ = 60 V     APD current = 1mA
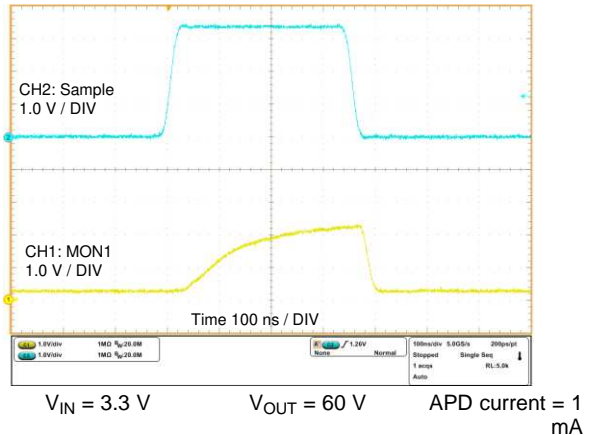
图 **17. Startup**

# 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

# 10 Layout

## 10.1 Layout Guidelines

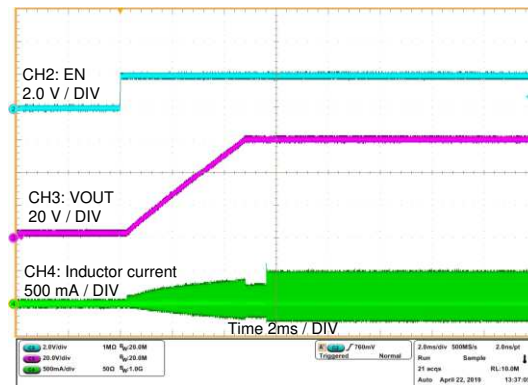The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems. Use the following checklist to get good performance for a well-designed board:

- Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di / dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise;
- Place the noise sensitive network like sample hold and current mirror output (MON1, MON2) being far away from the SW trace;
- Split the ground for the power GND, signal GND. Use a separate ground trace to connect the sample/hold and boost circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.
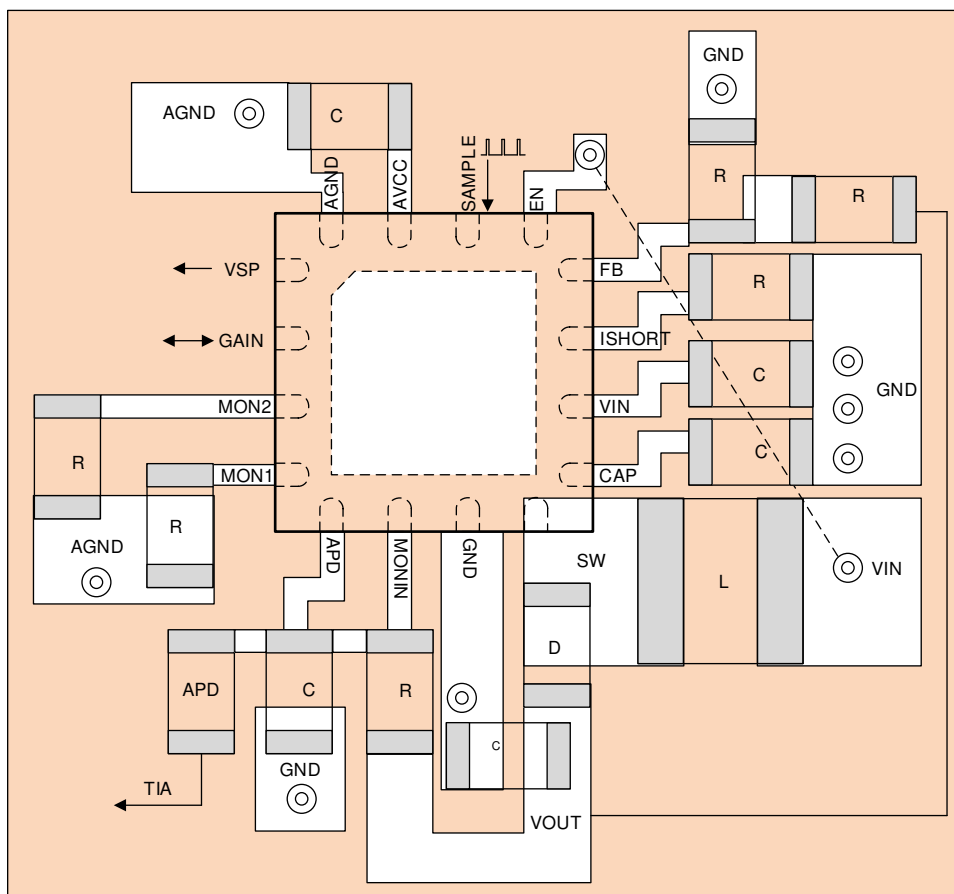
## 10.2 Layout Example



图 18. **Layout Example**

## 11  器件和文档支持

### 11.1  接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2  社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.3  商标

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### 11.4  静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5  Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12  机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS61390RTER | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1XQH |
| TPS61390RTER.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1XQH |
| TPS61390RTET | Active | Production | WQFN (RTE) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1XQH |
| TPS61390RTET.A | Active | Production | WQFN (RTE) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1XQH |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61390RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61390RTET | WQFN | RTE | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| TPS61390RTER | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS61390RTET | WQFN | RTE | 16 | 250 | 210.0 | 185.0 | 35.0 |

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A

A | 3.1 / 2.9 | B

PIN 1 INDEX AREA

3.1 / 2.9

| SIDE WALL METAL THICKNESS DIM A | |
|---|---|
| OPTION 1 | OPTION 2 |
| 0.1 | 0.2 |

0.8 MAX

0.05 / 0.00

C

SEATING PLANE

⌒ 0.08

□ 1.68 ± 0.07

5    8

12X 0.5

4

4X

1.5

1

17

EXPOSED THERMAL PAD

9

SYMM ₵

12

PIN 1 ID (OPTIONAL)

16    SYMM ₵    13

16X 0.30 / 0.18

⊕ 0.1 Ⓜ C A B
  0.05 Ⓜ
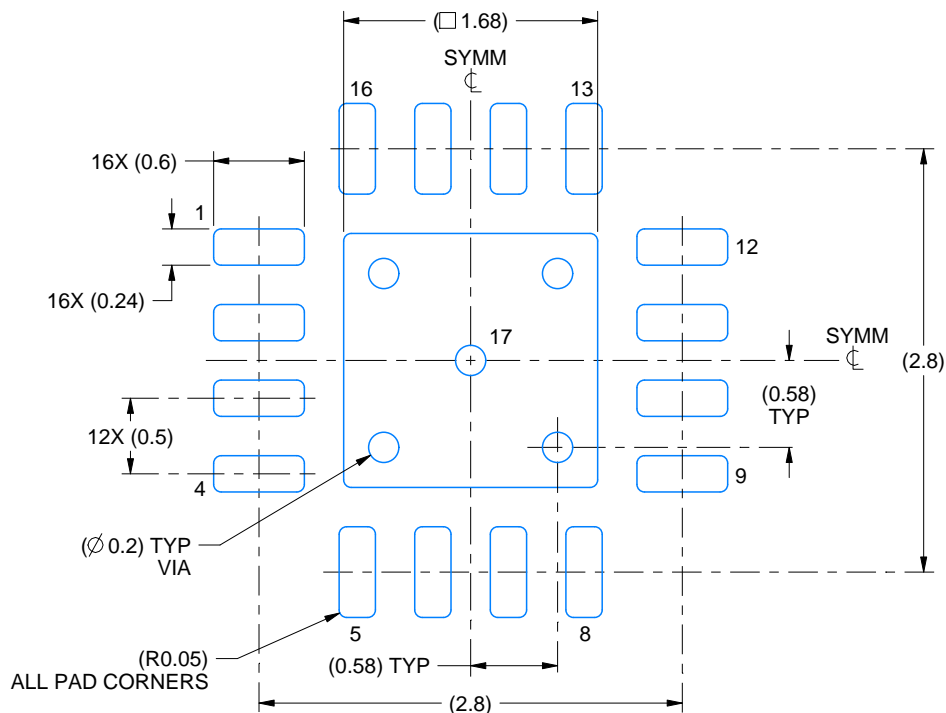
16X 0.5 / 0.3

(DIM A) TYP

4219117/B   04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

(□ 1.68)

SYMM

16    13
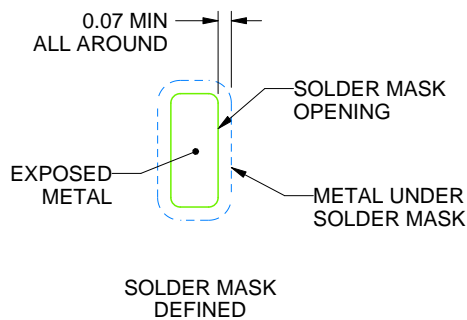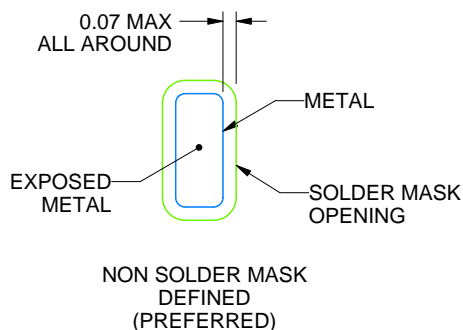
16X (0.6)

1

16X (0.24)

12

17

SYMM

(2.8)

12X (0.5)

(0.58) TYP

4

9

(⌀ 0.2) TYP
VIA

5    8

(R0.05)
ALL PAD CORNERS

(0.58) TYP

(2.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

METAL

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

(□ 1.55)

16

13

16X (0.6)

1

16X (0.24)

12

17

SYMM

(2.8)

12X (0.5)

4

9

METAL
ALL AROUND

5

8

SYMM

(R0.05) TYP

(2.8)

## SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

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