

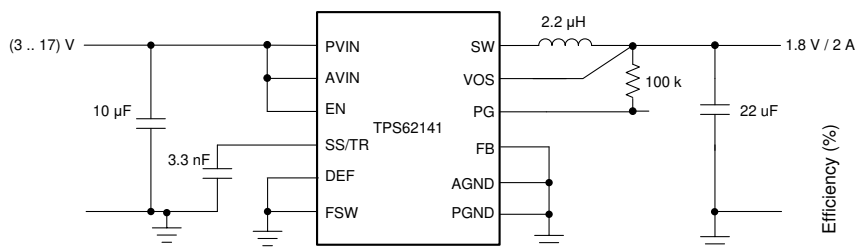
## TPS6214x 采用 3 x 3 QFN 封装的 3V 至 17V、2A 降压转换器

### 1 特性

- DCS-Control™ 拓扑
- 输入电压范围：3 V 至 17 V
- 高达 2A 的输出电流
- 可调输出电压范围为 0.9 V 至 6 V
- 引脚可选输出电压（标称值，+5%）
- 可编程软启动和跟踪
- 无缝节能模式转换
- 17 $\mu$ A 静态电流（典型值）
- 可选工作频率
- 电源正常状态输出
- 100% 占空比模式
- 短路保护
- 过热保护
- 与 TPS62130 和 TPS62150 引脚对引脚兼容
- 采用 3mm × 3mm VQFN-16 封装
- 使用 TPS82140 缩短设计时间

### 2 应用

- 标准 12V 电源轨
- 由单节或多节锂离子电池组成的 POL 电源
- 固态硬盘
- 嵌入式系统
- LDO 替代产品
- 移动 PC、平板、调制解调器、摄像头
- 服务器、微型服务器
- 数据终端、销售终端 (ePOS)



典型应用原理图

### 3 说明

TPS6214x 是一款易于使用的同步降压直流/直流转换器，此转换器针对高功率密度应用进行了优化。该器件的开关频率典型值高达 2.5MHz，允许使用小型电感，利用 DCS-Control 拓扑技术提供快速瞬态响应。

该系列器件具有 3V 至 17V 宽运行输入电压范围，非常适用于由锂离子或其他电池以及 12V 中间电源轨供电的系统。其输出电压为 0.9V 至 6V，支持高达 2A 的持续输出电流（使用 100% 占空比模式）。此输出电压启动斜坡由软启动引脚控制，这可使器件作为独立电源运行或运行在跟踪配置下。通过配置使能 (EN) 和开漏电源正常 (PG) 引脚也有可能实现电源排序。

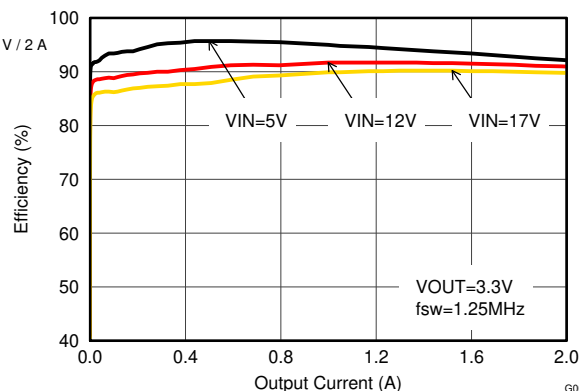
在省电模式下，该器件可根据输入电压 (VIN) 生成约 17 $\mu$ A 的静态电流。负载较小时可自动且无缝进入节能模式，同时该模式可保持整个负载范围内的高效率。该器件在关断模式下处于关断状态，期间的流耗低于 2 $\mu$ A。

此器件分为可调和固定输出电压型号，采用 3mm × 3mm (RGT) 16 引脚超薄四方扁平无引线 (VQFN) 封装。

#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
TPS6214x	VQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



效率与输出电流间的关系

G001



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2016) to Revision F (October 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 添加了 TPS82140 产品文件夹链接.....	1

Changes from Revision D (October 2015) to Revision E (September 2016)	Page
• 向特性列表添加了“与 TPS62130 和 TPS62150 引脚对引脚兼容”.....	1
• Changed the $T_J$ MAX value From: 125°C To: 150°C in the <i>Absolute Maximum Rating</i> .....	4
• Changed the 节 7.4 values.....	4
• Changed ( $T_J = -40^\circ\text{C}$ to 85°C) To: ( $T_J = -40^\circ\text{C}$ to 125°C) in the 节 7.5 conditions.....	5
• Added a test condition for IQ at $T_A = -40^\circ\text{C}$ to +85°C in the 节 7.5.....	5
• Added 表 8-1 and 表 8-2.....	9
• Added indicators (C1, C3, and C5) for capacitances to 图 9-1.....	12
• Added Switching Frequency graphs for 1.0-V, 1.8-V, and 5.0-V applications ( 图 9-18 through 图 9-25).....	18
• Changed <i>Layout Example</i> .....	28

## 5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	POWER GOOD LOGIC LEVEL (EN = LOW)
TPS62140	Adjustable	High Impedance
TPS62140A	Adjustable	Low
TPS62141	1.8 V	High Impedance
TPS62142	3.3 V	High Impedance
TPS62143	5.0 V	High Impedance

## 6 Pin Configuration and Functions

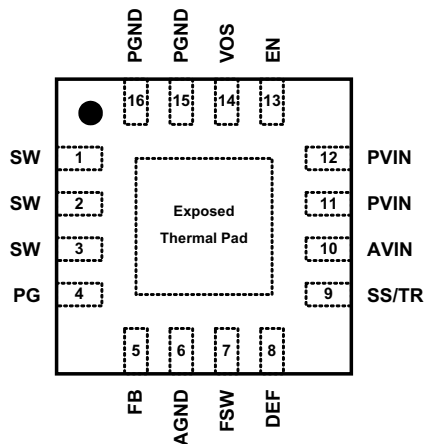


图 6-1. 16-Pin VQFN RGT Package (Top View)

表 6-1. Pin Functions

PIN <sup>(1)</sup>		I/O	DESCRIPTION
NO.	NAME		
1,2,3	SW	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and the output capacitor.
4	PG	O	Output power good (high = $V_{OUT}$ ready, low = $V_{OUT}$ below nominal regulation); open drain (requires pullup resistor)
5	FB	I	Voltage feedback of the adjustable version. Connect a resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
6	AGND		Analog ground. Must be connected directly to the exposed thermal pad and common ground plane.
7	FSW	I	Switching frequency select (low $\approx$ 2.5 MHz, high $\approx$ 1.25 MHz <sup>(2)</sup> for typical operation) <sup>(3)</sup>
8	DEF	I	Output voltage scaling (low = nominal, high = nominal + 5%) <sup>(3)</sup>
9	SS/TR	I	Soft-start/tracking [in. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
10	AVIN	I	Supply voltage for control circuitry. Connect to the same source as PVIN.
11,12	PVIN	I	Supply voltage for power stage. Connect to the same source as AVIN.
13	EN	I	Enable input (high = enabled, low = disabled) <sup>(3)</sup>
14	VOS	I	Output voltage sense pin and connection for the control loop circuitry
15,16	PGND		Power ground. Must be connected directly to the exposed thermal pad and common ground plane.
	Exposed Thermal Pad		Must be connected to AGND (pin 6), PGND (pin 15, 16), and common ground plane. See 图 11-1. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

- (1) For more information about connecting pins, see 节 8 and 节 9.  
(2) Connect FSW to VOUT or PG in this case.  
(3) An internal pulldown resistor keeps the logic level low, if pin is floating.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage <sup>(2)</sup>	AVIN, PVIN	- 0.3	20	V
	EN, SS/TR	- 0.3	V <sub>IN</sub> +0.3	
	SW	- 0.3	V <sub>IN</sub> +0.3	V
	DEF, FSW, FB, PG, VOS	- 0.3	7	V
Power-good sink current	PG		10	mA
Temperature	Operating junction temperature, T <sub>J</sub>	- 40	150	°C
	Storage temperature, T <sub>stg</sub>	- 65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge <sup>(3)</sup>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

### 7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>IN</sub> (at AVIN and PVIN)	3		17	V
Operating junction temperature, T <sub>J</sub>	- 40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS6214x	UNIT
		RGT (VQFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	45	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	53.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case(bottom) thermal resistance	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

over operating junction temperature ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ), typical values at  $V_{IN}=12\text{V}$  and  $T_A=25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY</b>							
$V_{IN}$	Input voltage range <sup>(1)</sup>		3		17	V	
$I_Q$	Operating quiescent current	EN = High, $I_{OUT} = 0\text{ mA}$ , device not switching $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		17	30	$\mu\text{A}$	
				17	25		
$I_{SD}$	Shutdown current <sup>(2)</sup>	EN = Low $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1.5	25	$\mu\text{A}$	
				1.5	4		
$V_{UVLO}$	Undervoltage lockout threshold	Falling input voltage (PWM mode operation)	2.6	2.7	2.8	V	
		Hysteresis		200		mV	
$T_{SD}$	Thermal shutdown temperature			160		$^\circ\text{C}$	
	Thermal shutdown hysteresis			20			
<b>CONTROL (EN, DEF, FSW, SS/TR, PG)</b>							
$V_H$	High level input threshold voltage (EN, DEF, FSW)		0.9	0.65		V	
$V_L$	Low level input threshold voltage (EN, DEF, FSW)			0.45	0.3	V	
$I_{LKG}$	Input leakage current (EN, DEF, FSW)	EN = $V_{IN}$ or GND; DEF, FSW = $V_{OUT}$ or GND		0.01	1	$\mu\text{A}$	
$V_{TH\_PG}$	Power-good threshold voltage	Rising (% $V_{OUT}$ )	92%	95%	98%		
		Falling (% $V_{OUT}$ )	87%	90%	94%		
$V_{OL\_PG}$	Power-good output low voltage	$I_{PG} = -2\text{ mA}$		0.07	0.3	V	
$I_{LKG\_PG}$	Input leakage current (PG)	$V_{PG} = 1.8\text{ V}$		1	400	nA	
$I_{SS/TR}$	SS/TR pin source current		2.3	2.5	2.7	$\mu\text{A}$	
<b>POWER SWITCH</b>							
$r_{DS(on)}$	High-side MOSFET ON-resistance	$V_{IN} \geq 6\text{ V}$		90	170	$\text{m}\Omega$	
		$V_{IN} = 3\text{ V}$		120			
	Low-side MOSFET ON-resistance	$V_{IN} \geq 6\text{ V}$		40	70	$\text{m}\Omega$	
		$V_{IN} = 3\text{ V}$		50			
$I_{LIMF}$	High-side MOSFET forward current limit <sup>(3)</sup>	$V_{IN} = 12\text{ V}$ , $T_A = 25^\circ\text{C}$	2.45	3	3.5	A	
<b>OUTPUT</b>							
$I_{LKG\_FB}$	Input leakage current (FB)	TPS62140, $V_{FB} = 0.8\text{ V}$		1	100	nA	
$V_{OUT}$	Output voltage range (TPS62140)	$V_{IN} \geq V_{OUT}$	0.9		6.0	V	
	DEF (output voltage programming)	DEF = 0 (GND)		$V_{OUT}$			
		DEF = 1 ( $V_{OUT}$ )		$V_{OUT} + 5\%$			
	Initial output voltage accuracy <sup>(4)</sup>	PWM mode operation, $V_{IN} \geq V_{OUT} + 1\text{ V}$		785.6	800	814.4	mV
		PWM mode operation, $V_{IN} \geq V_{OUT} + 1\text{ V}$ , $T_A = -10^\circ\text{C}$ to $85^\circ\text{C}$		788.0	800	812.8	
		Power-save mode operation, $C_{OUT} = 22\text{ }\mu\text{F}$		781.6	800	822.4	
	Load regulation <sup>(5)</sup>	$V_{IN} = 12\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , PWM mode operation		0.05		%/A	
Line regulation <sup>(5)</sup>	$3\text{ V} \leq V_{IN} \leq 17\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 1\text{ A}$ , PWM mode operation		0.02		%/V		

(1) The device is still functional down to undervoltage lockout (see parameter  $V_{UVLO}$ ).

(2) Current into AVIN + PVIN pins

(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see [节 8.4.4](#)).

(4) This is the accuracy provided at the FB pin for the adjustable  $V_{OUT}$  version (line and load regulation effects are not included). For the fixed-voltage versions the (internal) resistive divider is included.

(5) Line and load regulation depend on external component selection and layout (see [图 9-16](#) and [图 9-17](#)).

## 7.6 Typical Characteristics

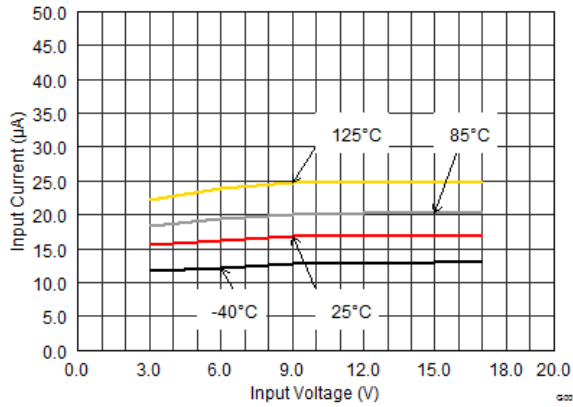


图 7-1. Quiescent Current

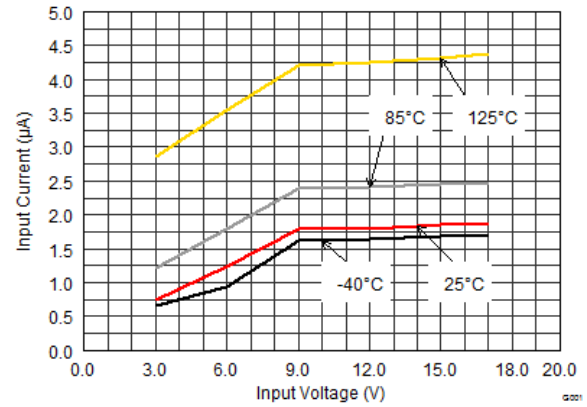


图 7-2. Shutdown Current

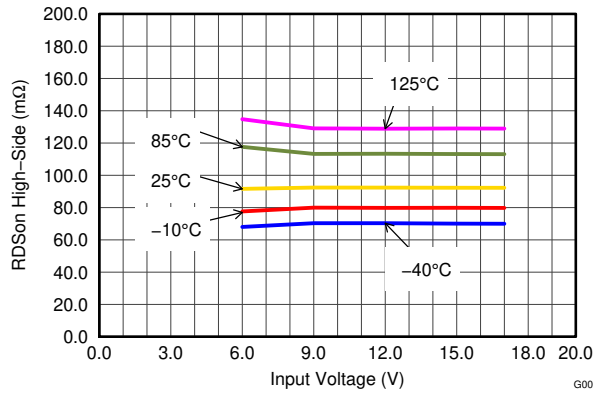


图 7-3. High-Side Switch Resistance

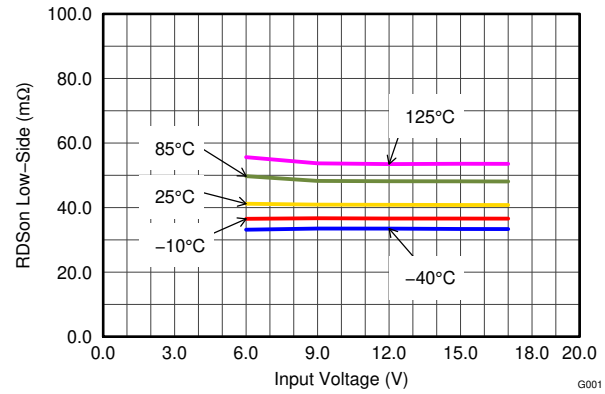


图 7-4. Low-Side Switch Resistance

## 8 Detailed Description

### 8.1 Overview

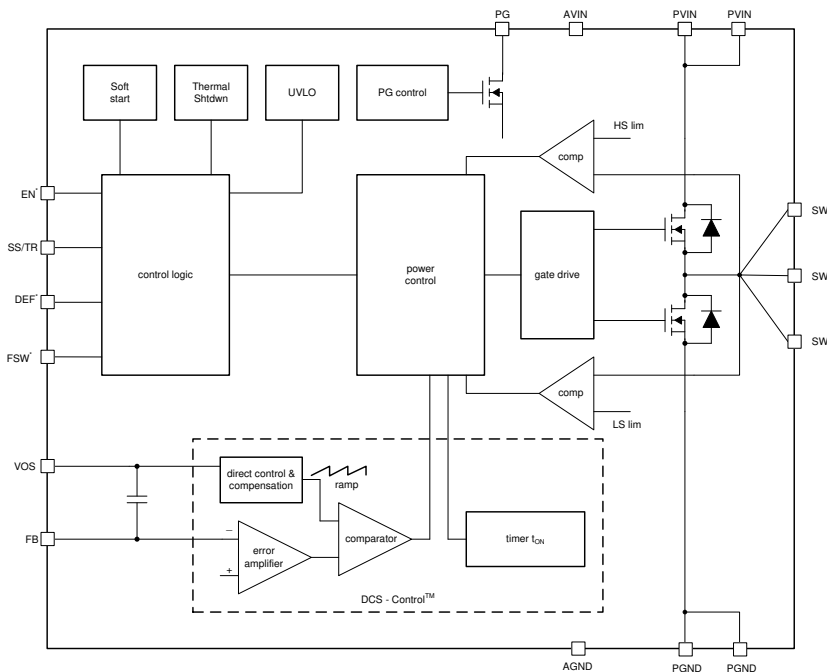
The TPS6214x synchronous switched-mode power converters are based on DCS-Control (Direct Control with Seamless Transition into Power-Save Mode), an advanced regulation topology that combines the advantages of hysteretic, voltage mode, and current mode control including an ac loop directly associated with the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

The DCS-Control topology supports Pulse Width Modulation (PWM) mode for medium and heavy load conditions and Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5 MHz or 1.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode, the switching frequency decreases linearly with the load current. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

Fixed output-voltage versions provide the smallest solution size and lowest current consumption, requiring only three external components. An internal current limit supports nominal output currents of up to 2 A.

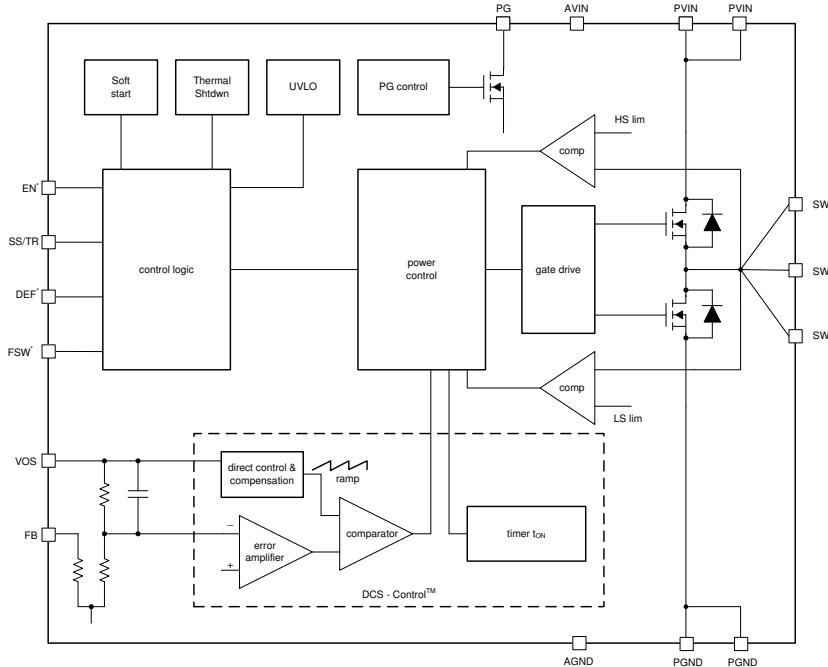
The TPS6214x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

### 8.2 Functional Block Diagrams



\* This pin is connected to a pull down resistor internally (see 节 8.3)

**图 8-1. TPS62140 and TPS62140A (Adjustable Output Voltage)**



\* This pin is connected to a pull down resistor internally (see 节 8.3)

图 8-2. TPS62141/2/3 (Fixed Output Voltage)

## 8.3 Feature Description

### 8.3.1 Enable/Shutdown (EN)

When Enable (EN) is set High, the device starts operation. Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5  $\mu\text{A}$ . During shutdown, the internal power MOSFETs and entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. The EN signal must be set externally to High or Low. An internal pulldown resistor of about 400  $\text{k}\Omega$  is connected and keeps EN logic low if Low is set initially and then the pin gets floating. It is disconnected if the pin is set High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

### 8.3.2 Soft-Start/Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output-voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50  $\mu\text{s}$ , and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See 图 9-34 and 图 9-35 for typical start-up operation.

Using a very small capacitor (or leaving SS/TR pin un-connected) provides fastest start-up behavior. There is no theoretical limit for the longest start-up time. The TPS6214x can start into a pre-biased output. During monotonic pre-biased start-up, both the power MOSFETs are not allowed to turn on until the internal ramp of the device sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5 V, a reduced current limit of typically 1.6 A is set internally. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a primary voltage. The output voltage follows this voltage in both directions, up and down (see 节 9).



### 8.3.3 Power Good (PG)

The TPS6214x has a built-in power-good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic-low level. With the TPS62140, it is high-impedance when the device is turned off due to EN, UVLO, or thermal shutdown. The TPS62140A features PG = Low in this case and can be used to actively discharge VOUT (see [图 9-41](#)). VIN must remain present for the PG pin to stay Low. See [TPS62130A Differences to TPS62130 Application Report](#) for application details. If not used, the PG pin should be connected to GND but may be left floating.

**表 8-1. Power Good Pin Logic Table (TPS62140)**

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable (EN = High)	$V_{FB} \geq V_{TH\_PG}$	✓	
	$V_{FB} \leq V_{TH\_PG}$		✓
Shutdown (EN = Low)		✓	
UVLO	$0.7\text{ V} < V_{IN} < V_{UVLO}$	✓	
Thermal Shutdown	$T_J > T_{SD}$	✓	
Power Supply Removal	$V_{IN} < 0.7\text{ V}$	✓	

**表 8-2. Power Good Pin Logic Table (TPS62140A)**

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable (EN = High)	$V_{FB} \geq V_{TH\_PG}$	✓	
	$V_{FB} \leq V_{TH\_PG}$		✓
Shutdown (EN = Low)			✓
UVLO	$0.7\text{ V} < V_{IN} < V_{UVLO}$		✓
Thermal Shutdown	$T_J > T_{SD}$		✓
Power Supply Removal	$V_{IN} < 0.7\text{ V}$	✓	

### 8.3.4 Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6214x devices can be increased by 5% above the nominal voltage by setting the DEF pin to High<sup>1</sup>. When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using the TPS6214x can be found in [Voltage Margining Using the TPS62130 Application Report](#). A pulldown resistor of about 400 k $\Omega$  is internally connected to the pin, ensuring a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

### 8.3.5 Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to high. It is mandatory to start with FSW = low to limit inrush current, which can be done by connecting to VOUT or PG. Running with lower frequency a higher efficiency, but also a higher output voltage ripple, is achieved. Pull FSW to Low for high frequency operation (2.5 MHz typ.). To get low ripple and full output current at the lower switching frequency, it is recommended to use an inductor of at least 2.2  $\mu$ H. The switching frequency can be changed during operation, if needed. A pulldown resistor of about 400 k $\Omega$  is internally connected to the pin, acting the same way as at the DEF pin (see above).

<sup>1</sup> Maximum allowed voltage is 7 V. Therefore, it is recommended to connect it to VOUT or PG, not VIN.

### 8.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents incorrect operation of the device by switching off both the power FETs. The undervoltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

### 8.3.7 Thermal Shutdown

The junction temperature ( $T_J$ ) of the device is monitored by an internal temperature sensor. If  $T_J$  exceeds 160°C (typ.), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes high-impedance. When  $T_J$  decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature.

## 8.4 Device Functional Modes

### 8.4.1 Pulse-Width Modulation (PWM) Operation

The TPS6214x operates with pulse-width modulation in continuous-conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on  $V_{IN}$ ,  $V_{OUT}$ , and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor ripple current. To maintain high efficiency at light loads, the device enters power-save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor ripple current.

### 8.4.2 Power Save Mode Operation

The TPS6214x enters its built-in power-save mode seamlessly if the load current decreases. This secures a high efficiency in light-load operation. The device remains in power-save mode as long as the inductor current is discontinuous.

In power-save mode, the switching frequency decreases linearly with the load current, maintaining high efficiency. The transition into and out of power-save mode happens within the entire regulation scheme and is seamless in both directions.

TPS6214x includes a fixed-on-time circuit. An estimate for this on-time, in steady-state operation with FSW = low, is:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400ns \quad (1)$$

For very small output voltages, an absolute minimum on-time of about 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such case. Using  $t_{ON}$ , the typical peak inductor current in Power Save Mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \quad (2)$$

When  $V_{IN}$  decreases to typically 15% above  $V_{OUT}$ , the TPS6214x does not enter power-save mode, regardless of the load current. The device maintains output regulation in PWM mode.

### 8.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by  $D = V_{OUT}/V_{IN}$  and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty-cycle operation, turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input-to-output voltage differences, for example, for the longest operation time of battery-powered applications. In 100% duty-cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} (R_{DS(on)} + R_L) \quad (3)$$

where

- $I_{OUT}$  is the output current
- $R_{DS(on)}$  is the  $R_{DS(on)}$  of the high-side FET
- $R_L$  is the DC resistance of the inductor used

### 8.4.4 Current Limit and Short Circuit Protection

The TPS6214x devices are protected against heavy load and short-circuit events. If a short circuit is detected ( $V_{OUT}$  drops below 0.5 V), the current limit is reduced to 1.6 A, typically. If the output voltage rises above 0.5 V, the device runs in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot through current, then the low-side FET switches on to allow the inductor current to decrease. The low-side current limit is typically 2.4 A. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current-limit threshold.

The output current of the device is limited by the current limit (see [节 7.5](#)). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where

- $I_{LIMF}$  is the static current limit, specified in [节 7.5](#)
- $L$  is the inductor value
- $V_L$  is the voltage across the inductor ( $V_{IN} - V_{OUT}$ )
- $t_{PD}$  is the internal propagation delay

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \quad (5)$$

## 9 Application and Implementation

### Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The TPS62140 is a switched mode step-down converter, able to convert a 3-V to 17-V input voltage into a 0.9-V to 6-V output voltage, providing up to 2 A. It needs a minimum amount of external components. Apart from the LC output filter and the input capacitor, only the TPS62140 (TPS62140A) with an adjustable output voltage needs an additional resistive divider to set the output voltage level.

### 9.2 Typical Application

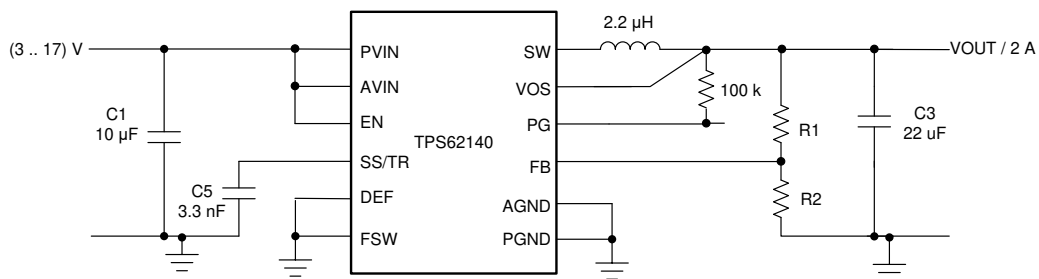


图 9-1. 3.3-V/2-A Step-Down Converter

#### 9.2.1 Design Requirements

The following design guideline provides a component selection to operate the device within the recommended operating conditions. Using the FSW pin, the design can be optimized for highest efficiency or smallest solution size and lowest output voltage ripple. For highest efficiency set FSW = high and the device operates at the lower switching frequency. For smallest solution size and lowest output voltage ripple set FSW = low and the device operates with higher switching frequency. The typical values for all measurements are  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ , and  $T = 25^\circ\text{C}$ , using the external components of 表 9-1.

#### 9.2.2 Detailed Design Procedure

The component selection used for measurements is given as follows:

表 9-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER <sup>(1)</sup>
IC	17-V, 2-A step-down converter, QFN	TPS62140RGT, Texas Instruments
L1	2.2-µH, 3.1-A, 0.165 in × 0.165 in	XFL4020-222MEB, Coilcraft
C1	10-µF, 25-V, ceramic, 1210	Standard
C3	22-µF, 6.3-V, ceramic, 0805	Standard
C5	3300-pF, 25-V, ceramic, 0603	
R1	Dependent on Vout	
R2	Dependent on Vout	
R3	100-k Ω, chip, 0603, 1/16W, 1%	Standard

(1) See [Third-Party Products](#) Disclaimer

### 9.2.2.1 Programming the Output Voltage

While the output voltage of the TPS62140 (TPS62140A) is adjustable, the TPS62141, TPS62142, and TPS62143 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and can be left floating. It is recommended to connect to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from [方程式 6](#). It is recommended to choose resistor values which allow a current of at least 2  $\mu$ A, meaning the value of R2 should not exceed 400 k $\Omega$ . Lower resistor values are recommended for highest accuracy and most-robust design. For applications requiring lowest current consumption, the use of fixed output-voltage versions is recommended.

$$R_1 = R_2 \left( \frac{V_{OUT}}{0.8V} - 1 \right) \quad (6)$$

In case the FB pin is opened, the device clamps the output voltage at the VOS pin internally to about 7.4 V.

### 9.2.2.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6214x is optimized to work within a range of external components. The inductance of the LC output filter and capacitance have to be considered in conjunction, creating a double pole, responsible for the corner frequency of the converter (see [节 9.2.2.4](#)). [表 9-2](#) can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application. See [Optimizing the TPS62130/40/50/60 Output Filter Application Report](#) for details.

**表 9-2. Recommended LC Output Filter Combinations**

	4.7 $\mu$ F	10 $\mu$ F	22 $\mu$ F	47 $\mu$ F	100 $\mu$ F	200 $\mu$ F	400 $\mu$ F
0.47 $\mu$ H <sup>(1)</sup>							
1 $\mu$ H			✓	✓	✓	✓	
2.2 $\mu$ H		✓	✓ <sup>(2)</sup>	✓	✓	✓	
3.3 $\mu$ H		✓	✓	✓	✓		
4.7 $\mu$ H							

(1) The values in the table are nominal values. The effective capacitance was considered to vary by +20% and -50%.

(2) This LC combination is the standard value and recommended for most applications.

The TPS6214x can be run with an inductor as low as 1  $\mu$ H or 2.2  $\mu$ H. FSW should be set low in this case. However, for applications running with the low-frequency setting (FSW = high) or with low input voltages, 3.3  $\mu$ H is recommended.

#### Note

**DC bias effect:** High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

### 9.2.2.2.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point, and efficiency. In addition, the inductor selected must be rated for appropriate saturation

current and DC resistance (DCR). 方程式 7 和 方程式 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \tag{7}$$

$$\Delta I_{L(max)} = V_{OUT} \cdot \left( \frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \cdot f_{SW}} \right) \tag{8}$$

where

- $I_L(max)$  is the maximum inductor current
- $\Delta I_L$  is the peak-to-peak inductor ripple current
- $L(min)$  is the minimum effective inductor value
- $f_{SW}$  is the actual PWM switching frequency

Calculating the maximum inductor current using the actual operating conditions gives the minimum required inductor saturation current. It is recommended to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6214x and are recommended for use:

表 9-3. List of Inductors

TYPE	INDUCTANCE (μH)	CURRENT (A) <sup>(1)</sup>	DIMENSIONS [L x B x H] (mm)	MANUFACTURER <sup>(2)</sup>
XFL4020-222ME_	2.2 μH, ±20%	3.5	4 x 4 x 2.1	Coilcraft
XFL4020-332ME_	3.3 μH, ±20%	2.9	4 x 4 x 2.1	Coilcraft
IHLP1212BZ-11	2.2 μH, ±20%	3.0	3 x 3.6 x 2	Vishay
IHLP1616AB-11	2.2 μH, ±20%	2.75	4.05 x 4.45 x 1.2	Vishay
DEM4518C 1235AS-H-3R3M	3.3 μH, ±20%	2.5	4.5 x 4.7 x 1.9	Toko

(1) Lower of  $I_{RMS}$  at 40°C rise or  $I_{SAT}$  at 30% drop.

(2) See [Third-Party Products](#) disclaimer

The inductor value also determines the load current at which the power-save mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \tag{9}$$

Using 方程式 8, this current level can be adjusted by changing the inductor value.

### 9.2.2.2.2 Capacitor Selection

#### 9.2.2.2.2.1 Output Capacitor

The recommended value for the output capacitor is 22  $\mu\text{F}$ . The architecture of the TPS6214X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output-voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value can have some advantages, like smaller voltage ripple and a tighter DC output accuracy in power-save mode (see [Optimizing the TPS62130/40/50/60 Output Filter Application Report](#)).

Note: In power-save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

#### 9.2.2.2.2.2 Input Capacitor

For most applications, 10  $\mu\text{F}$  is sufficient and is recommended, though a larger value reduces input-current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it is recommended to place a capacitance of 0.1  $\mu\text{F}$  from AVIN to AGND, to avoid potential noise coupling.

#### 9.2.2.2.2.3 Soft-Start Capacitor

A capacitance connected between the SS/TR pin and AGND allows a user-programmable start-up slope of the output voltage. A constant-current source provides 2.5  $\mu\text{A}$  to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \cdot \frac{2.5\mu\text{A}}{1.25\text{V}} \quad [F] \quad (10)$$

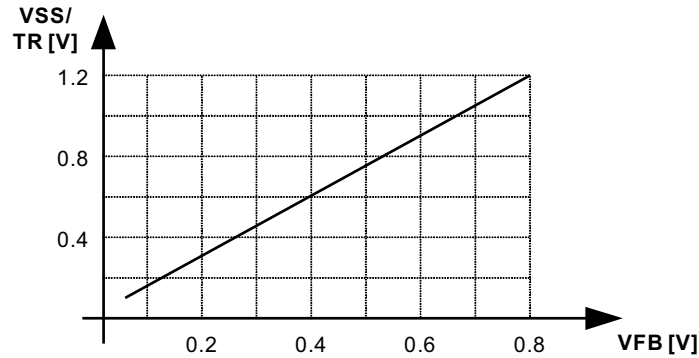
where

- $C_{SS}$  is the capacitance (F) required at the SS/TR pin
- $t_{SS}$  is the desired soft-start ramp time (s).

### 9.2.2.3 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin tracks the SS/TR pin voltage as described in [方程式 11](#) and shown in [图 9-2](#).

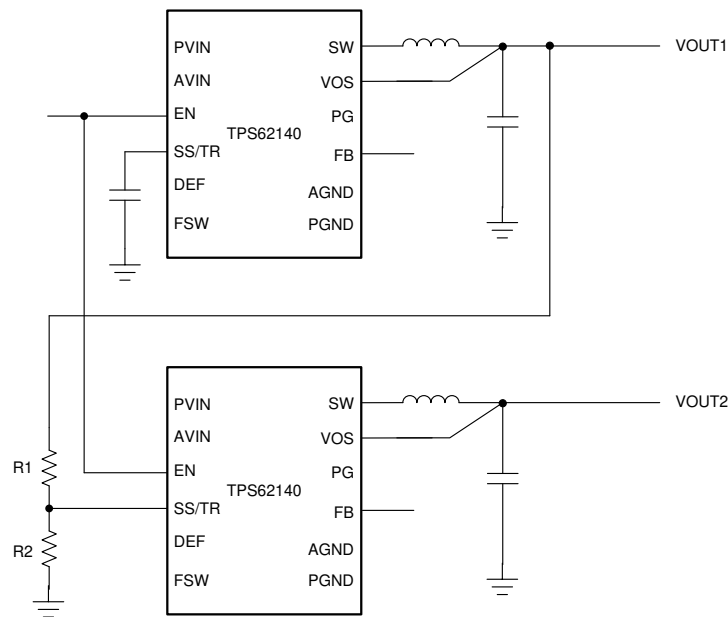
$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \quad (11)$$



**图 9-2. Voltage Tracking Relationship**

Once the SS/TR pin voltage reaches about 1.2V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device doesn't sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is  $V_{IN}+0.3V$ .

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage goes to zero, independent of the tracking voltage. 图 9-3 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.



**图 9-3. Sequence for Ratiometric and Simultaneous Startup**

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. A ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. 方程式 10 calculates the soft-start time, though the SS/TR current must be doubled. Details about these and other tracking and



sequencing circuits are found in [Sequencing and Tracking With the TPS621-Family and TPS821-Family Application Report](#).

Note: If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

#### 9.2.2.4 Output Filter and Loop Stability

The devices of the TPS6214x family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with [方程式 12](#):

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (12)$$

Proven nominal values for inductance and ceramic capacitance are given in [表 9-2](#) and are recommended for use. Different values may work, but care must be taken on the loop stability, which is affected. More information including a detailed L-C stability matrix can be found in [Optimizing the TPS62130/40/50/60 Output Filter Application Report](#).

The TPS6214x devices, both fixed and adjustable versions, include an internal 25 pF feed-forward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equations [方程式 13](#) and [方程式 14](#):

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25 pF} \quad (13)$$

$$f_{pole} = \frac{1}{2\pi \cdot 25 pF} \cdot \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \quad (14)$$

Though the TPS6214x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power-save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability vs transient response can be found in [Optimizing Transient Response of Internally Compensated DC-DC Converters Application Report](#) and [Feedforward Capacitor to Improve Stability and Bandwidth of TPS621/821-Family Application Report](#).

### 9.2.3 Application Curves

$V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

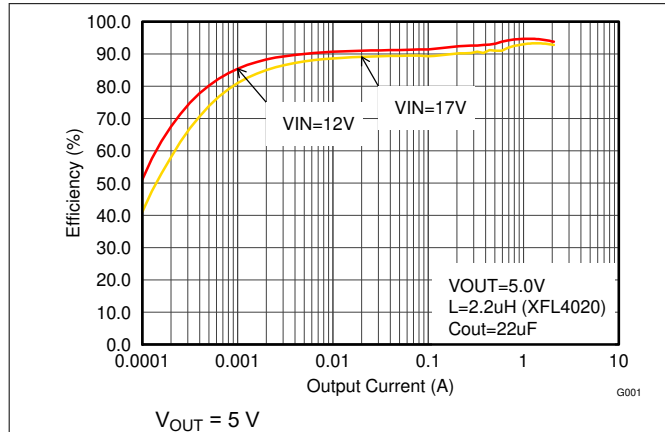


图 9-4. Efficiency With 1.25 MHz

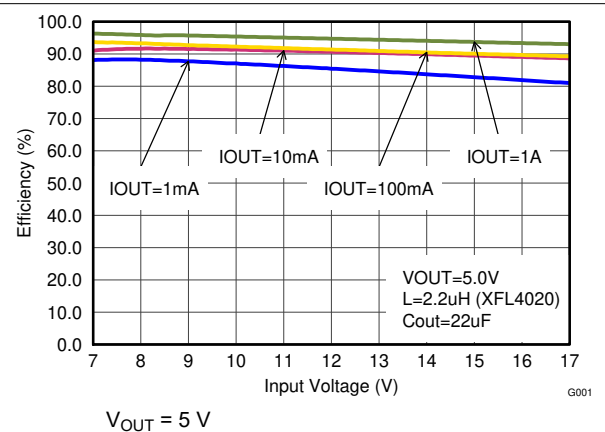


图 9-5. Efficiency With 1.25 MHz

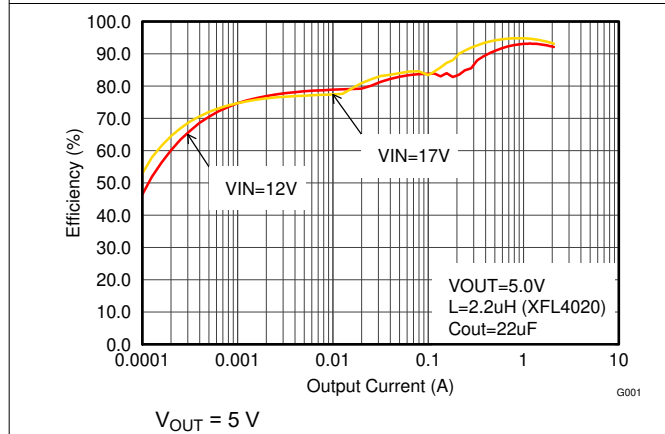


图 9-6. Efficiency With 2.5 MHz

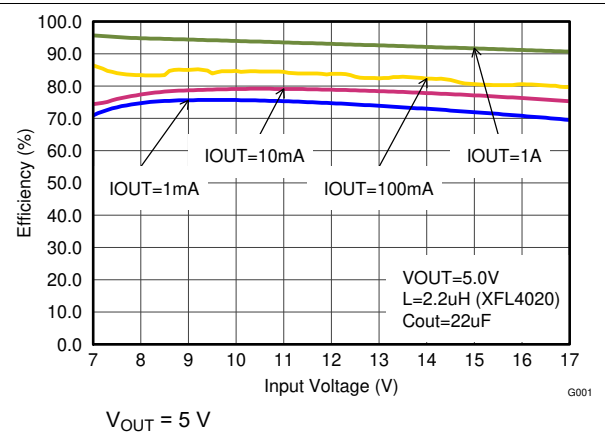


图 9-7. Efficiency With 2.5 MHz

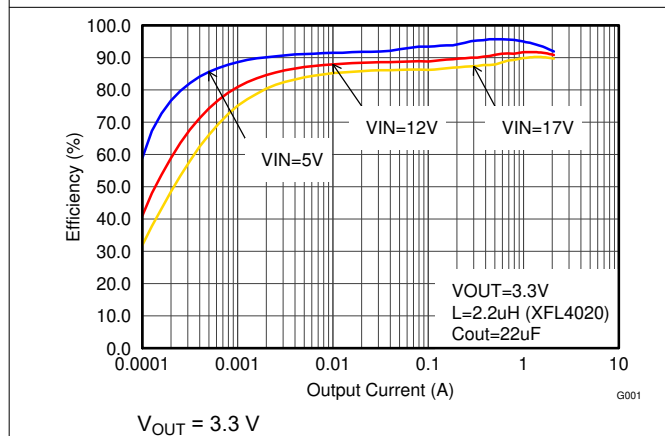


图 9-8. Efficiency With 1.25 MHz

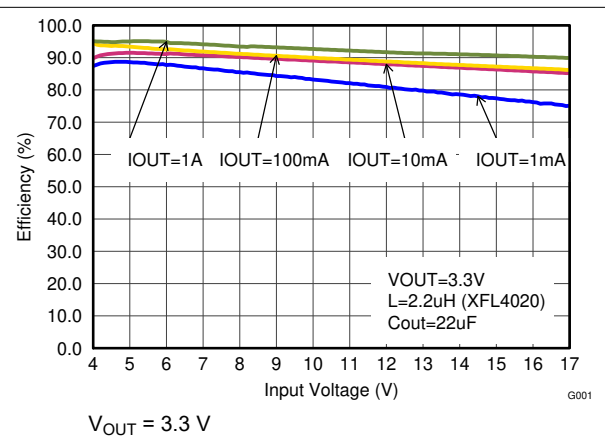
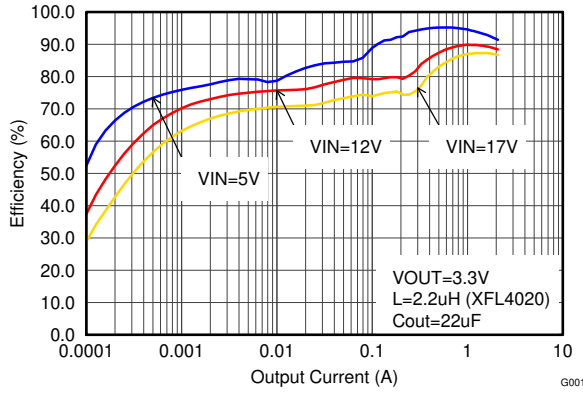
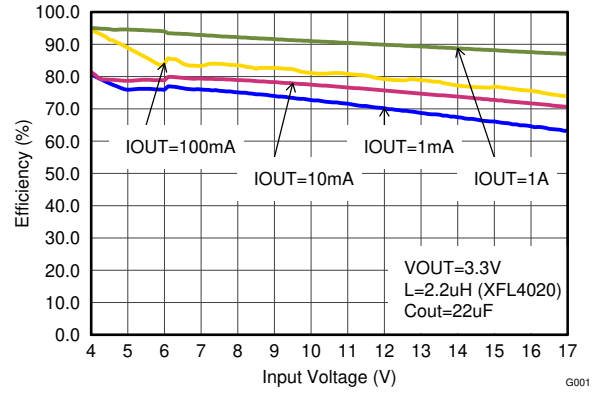


图 9-9. Efficiency With 1.25 MHz



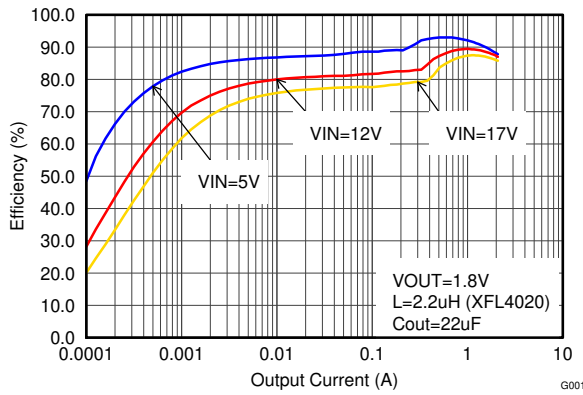
$V_{OUT} = 3.3\text{ V}$

**图 9-10. Efficiency With 2.5 MHz,**



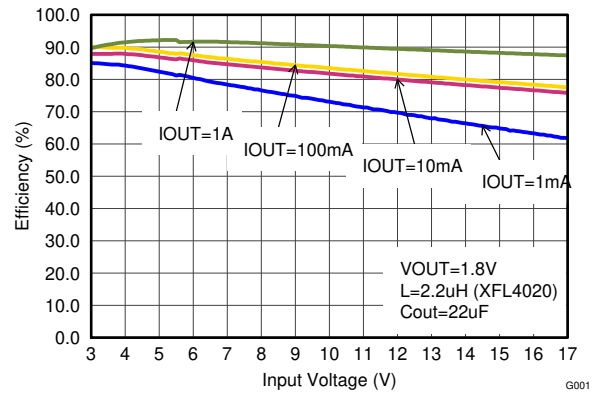
$V_{OUT} = 3.3\text{ V}$

**图 9-11. Efficiency With 2.5 MHz**



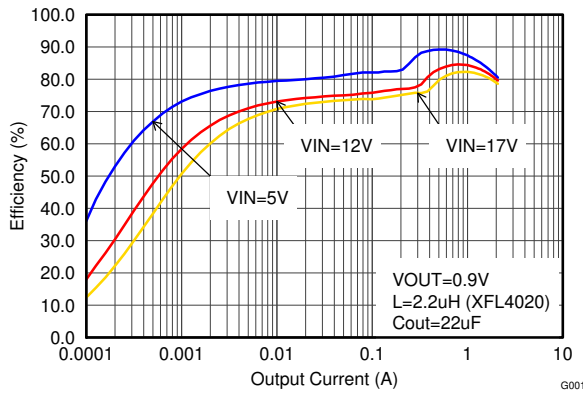
$V_{OUT} = 1.8\text{ V}$

**图 9-12. Efficiency With 1.25 MHz**



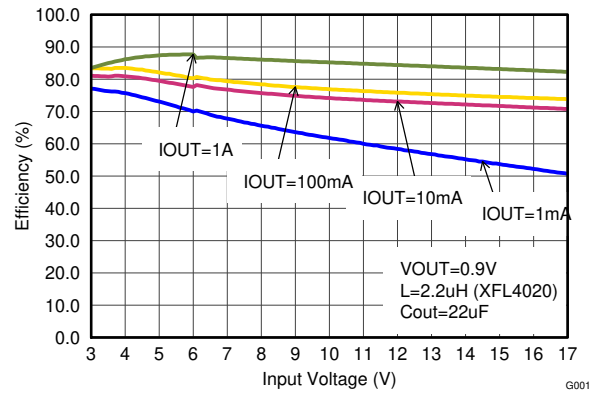
$V_{OUT} = 1.8\text{ V}$

**图 9-13. Efficiency With 1.25 MHz**



$V_{OUT} = 0.9\text{ V}$

**图 9-14. Efficiency With 1.25 MHz**



$V_{OUT} = 0.9\text{ V}$

**图 9-15. Efficiency With 1.25 MHz**

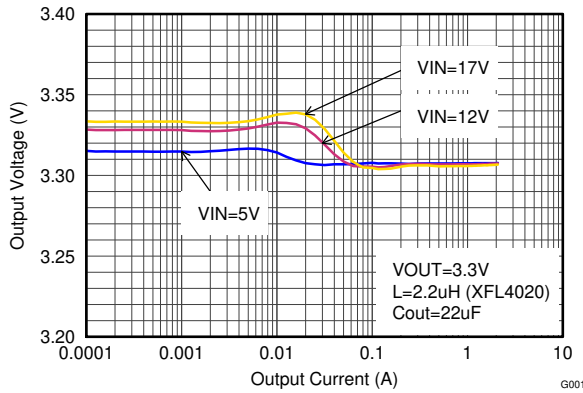


图 9-16. Output Voltage Accuracy (Load Regulation)

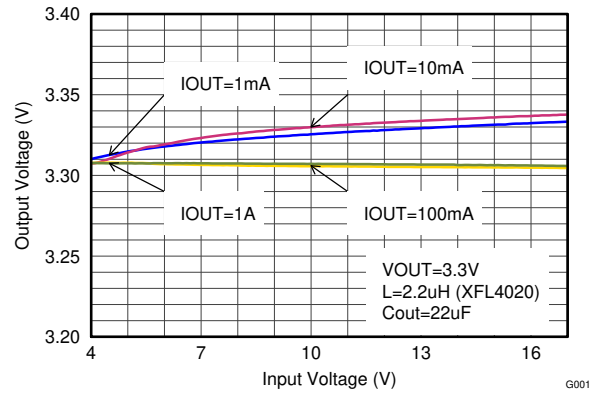


图 9-17. Output Voltage Accuracy (Line Regulation)

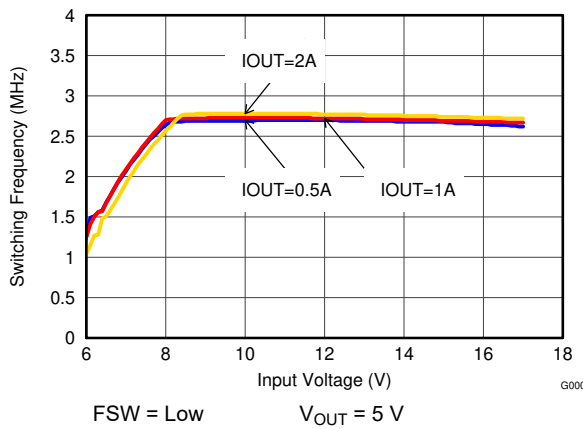


图 9-18. Switching Frequency vs Input Voltage

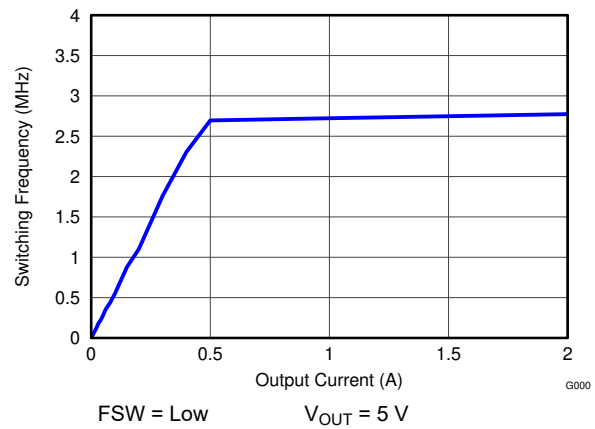


图 9-19. Switching Frequency vs Output Current

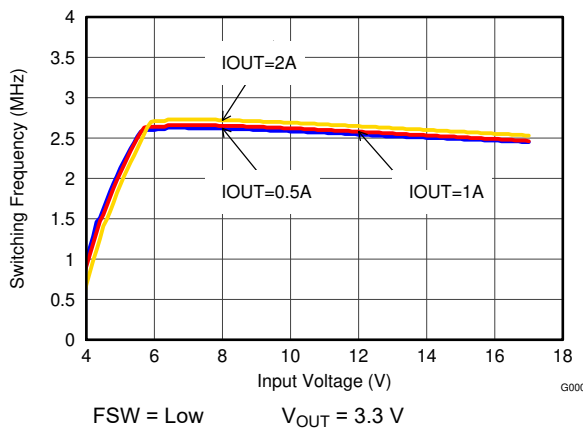


图 9-20. Switching Frequency vs Input Voltage

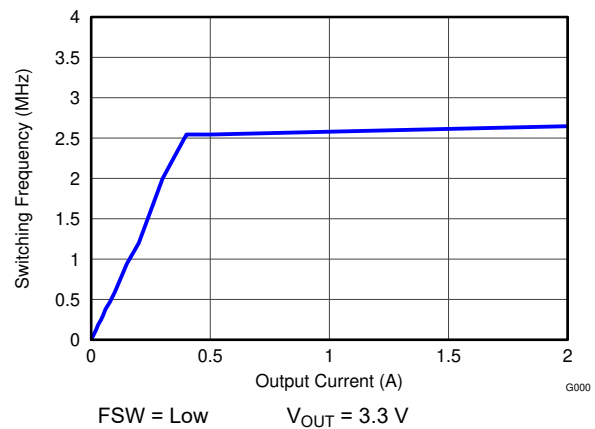
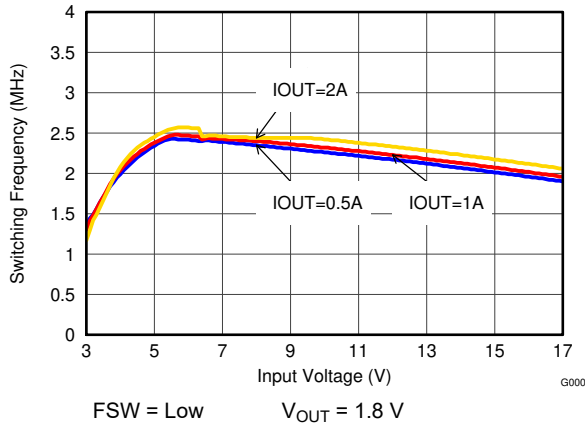
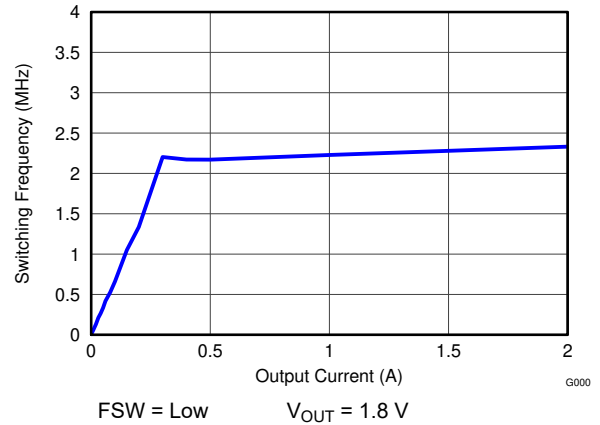


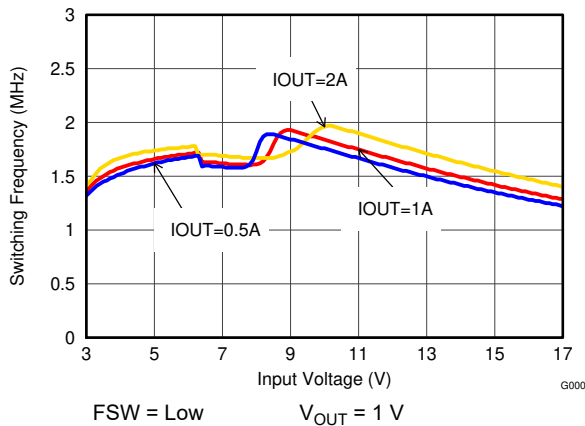
图 9-21. Switching Frequency vs Output Current



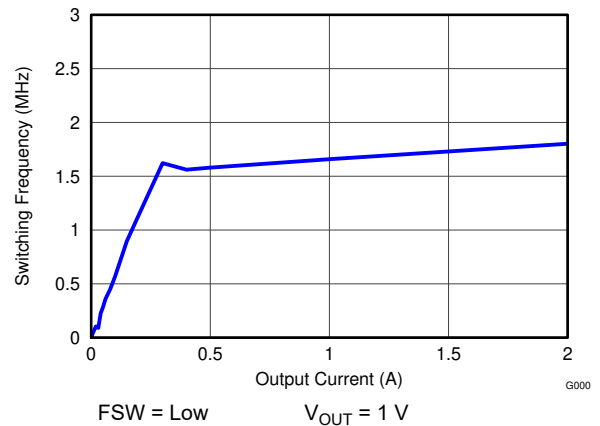
**图 9-22. Switching Frequency vs Input Voltage**



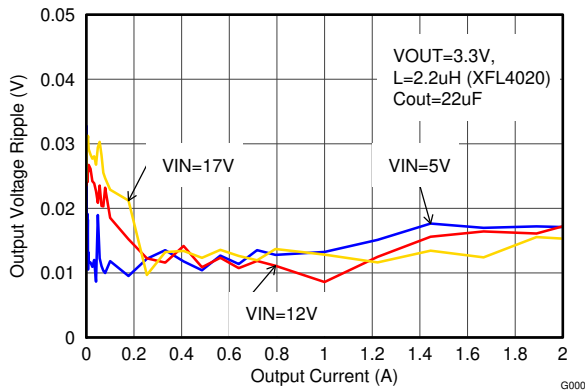
**图 9-23. Switching Frequency vs Output Current**



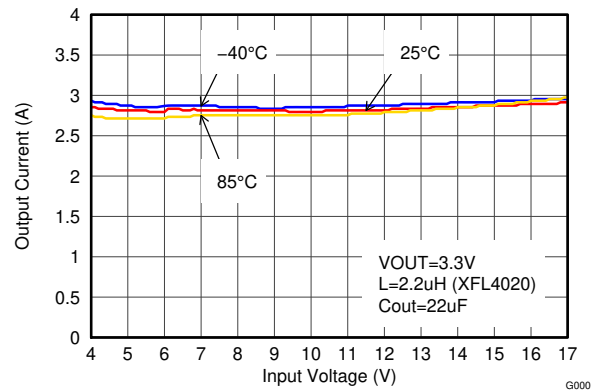
**图 9-24. Switching Frequency vs Input Voltage**



**图 9-25. Switching Frequency vs Output Current**



**图 9-26. Output Voltage Ripple**



**图 9-27. Maximum Output Current**

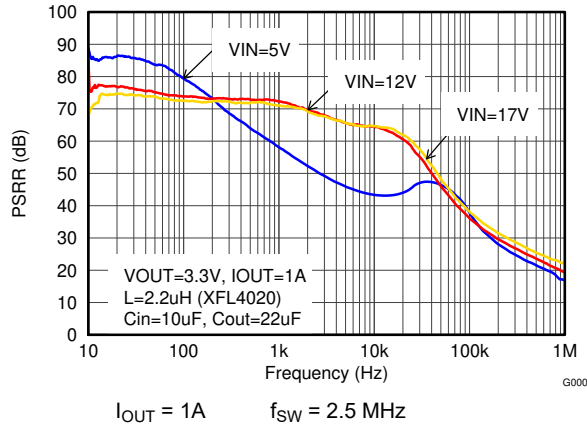


图 9-28. Power-Supply Rejection Ratio

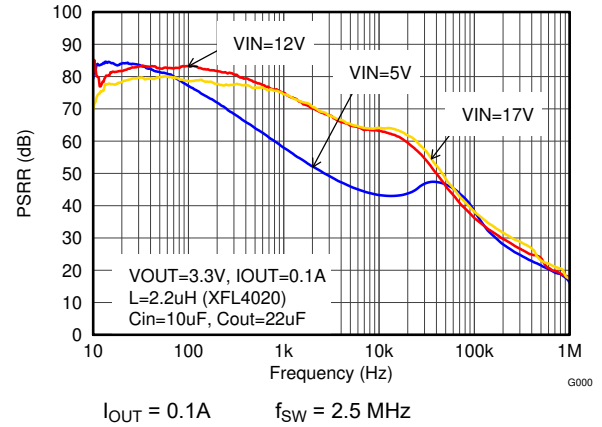
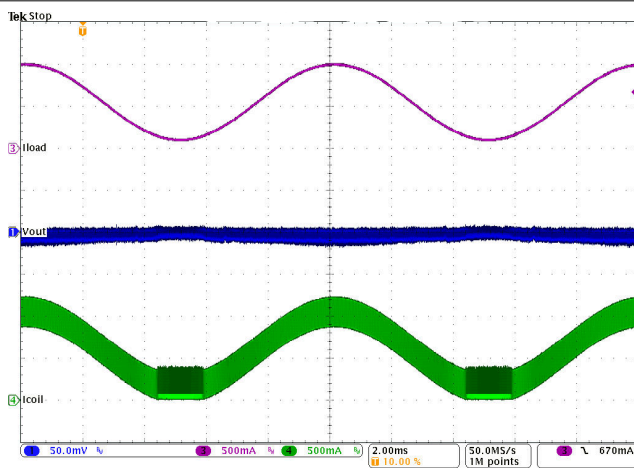
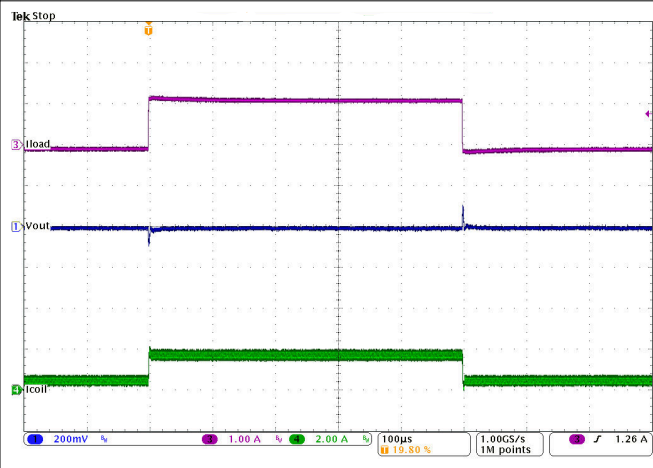


图 9-29. Power-Supply Rejection Ratio



$V_{IN} = 12\text{ V}$        $V_{OUT} = 3.3\text{ V}$  With 50 mV/div

图 9-30. PWM-PSM-Transition



$I_{OUT} = 0.5\text{ to }2\text{ to }0.5\text{ A}$        $V_{IN} = 12\text{ V}$        $V_{OUT} = 3.3\text{ V}$

图 9-31. Load Transient Response

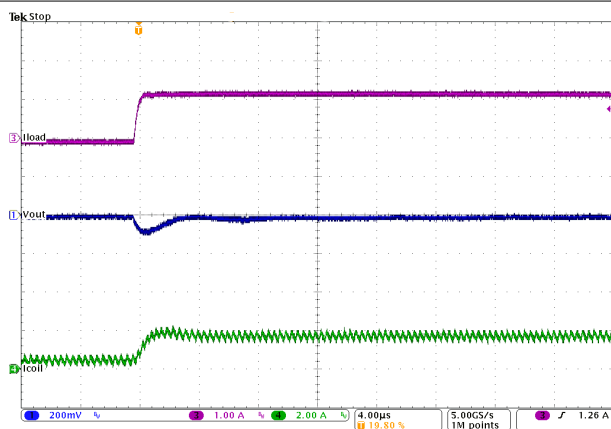


图 9-32. Line Transient Response of 图 9-31, Rising Edge

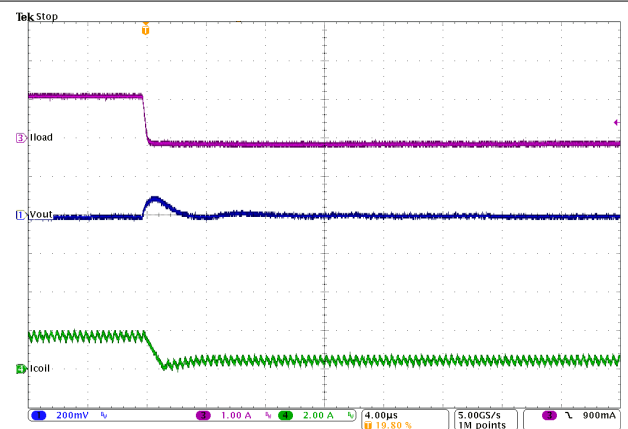
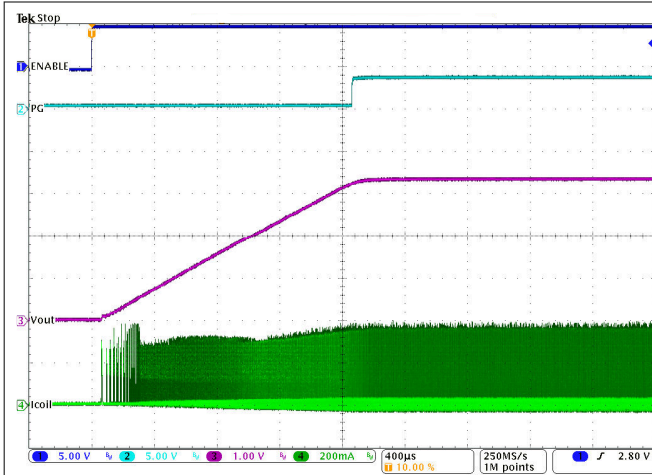
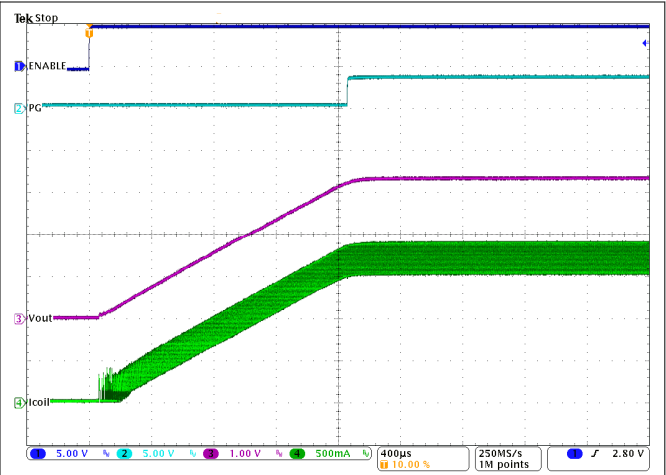


图 9-33. Line Transient Response of 图 9-31, Falling Edge



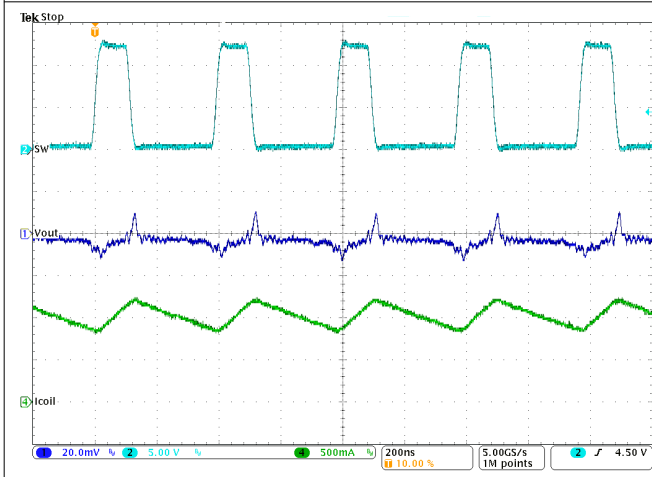
$V_{IN} = 12\text{ V}$       $V_{OUT} = 3.3\text{ V}$

**图 9-34. Start-Up Into 100 mA**



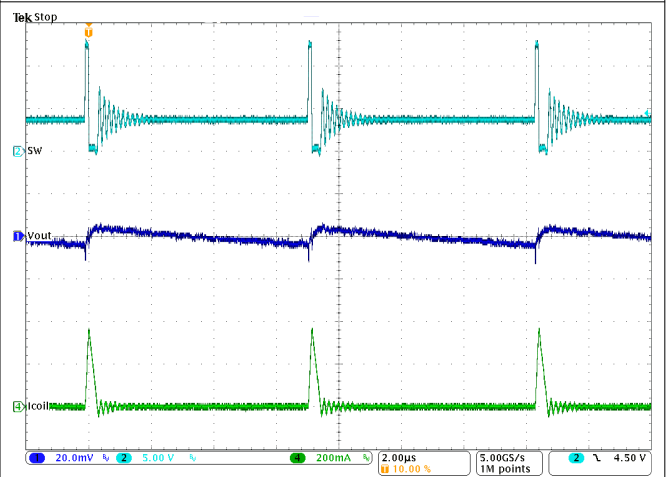
$V_{IN} = 12\text{ V}$       $V_{OUT} = 3.3\text{ V}$

**图 9-35. Start-Up into 2 A**



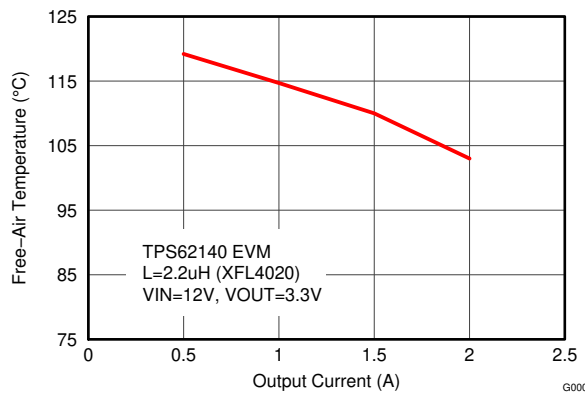
$I_{OUT} = 1\text{ A}$

**图 9-36. Typical Operation in PWM Mode**

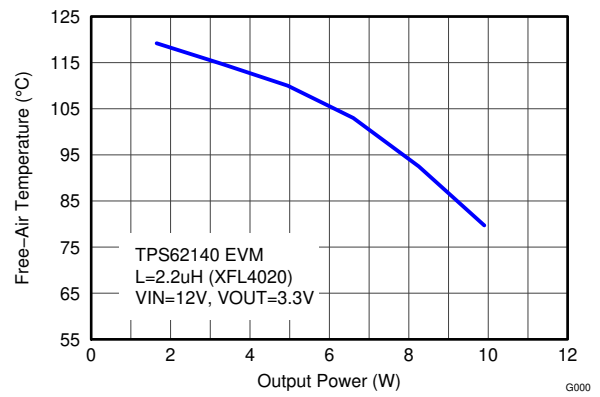


$I_{OUT} = 10\text{ A}$

**图 9-37. Typical Operation in Power-Save Mode**



**图 9-38. Maximum Ambient Temperature**

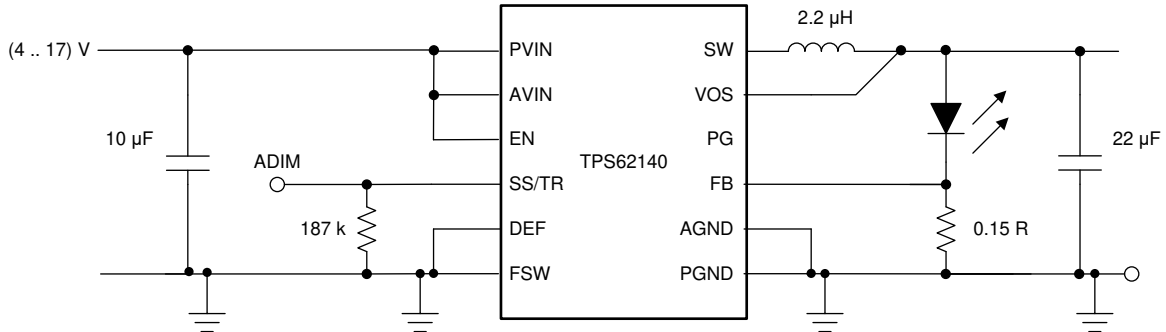


**图 9-39. Maximum Ambient Temperature**

## 9.3 System Examples

### 9.3.1 LED Power Supply

The TPS62140 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Because this pin provides 2.5  $\mu\text{A}$ , the feedback pin voltage can be adjusted by an external resistor per [方程式 15](#). This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62140. [图 9-40](#) shows an application circuit, tested with analog dimming:



**图 9-40. Single Power LED Supply**

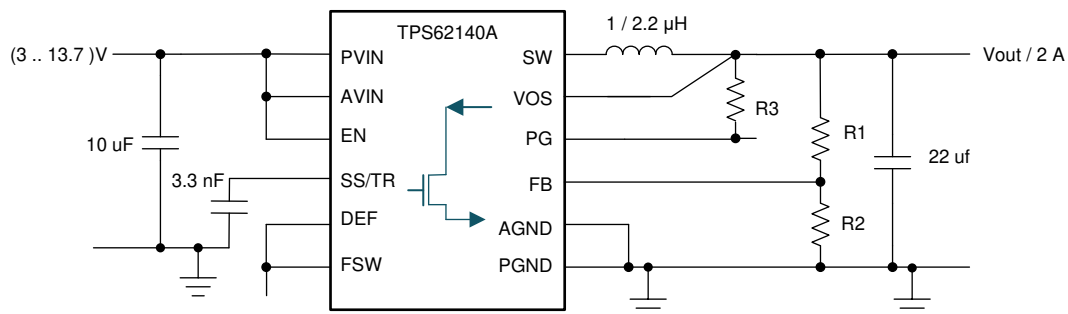
The resistor at SS/TR sets the FB voltage to a level of about 300 mV and is calculated from [方程式 15](#).

$$V_{FB} = 0.64 \cdot 2.5\mu\text{A} \cdot R_{SS/TR} \quad (15)$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage must be rated according to the forward voltage needed by the LED used. More information is available in the application note [Step-Down LED Driver With Dimming With the TPS621-Family and TPS821-Family Application Report](#).

### 9.3.2 Active Output Discharge

The TPS62140A pulls the PG pin Low, when the device is shut down by EN, UVLO or thermal shutdown. Connecting PG to Vout through a resistor can be used to discharge Vout in those cases (see [图 9-41](#)). The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10mA.



**图 9-41. Discharge Vout through PG Pin With TPS62140A**



### 9.3.3 Inverting Power Supply

The TPS6214x can be used as inverting power supply by rearranging external circuitry as shown in 图 9-42. As the former GND node now represents a voltage level below system ground, the voltage difference between  $V_{IN}$  and  $V_{OUT}$  has to be limited for operation to the maximum supply voltage of 17V (see 方程式 16).

$$V_{IN} + |V_{OUT}| \leq V_{INmax} \quad (16)$$

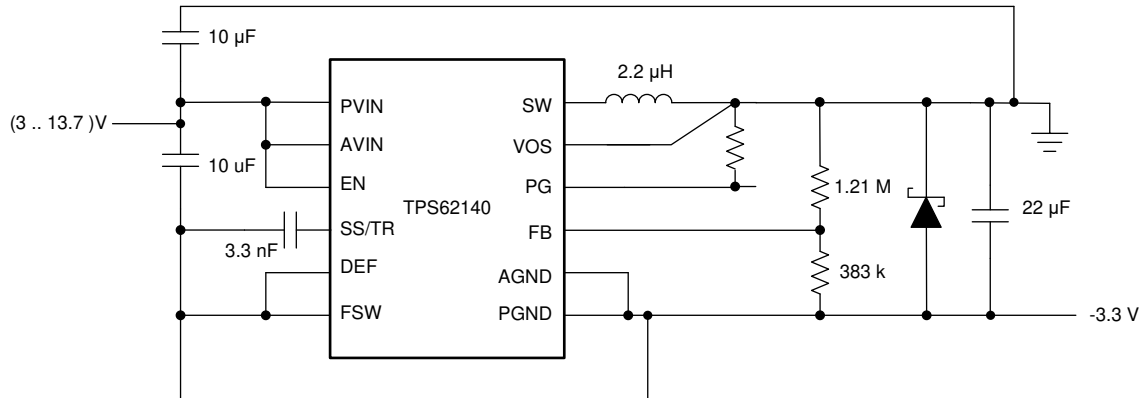


图 9-42. - 3.3V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22µF is recommended. A detailed design example is given in [Using the TPS6215x in an Inverting Buck-Boost Topology Application Report](#).

### 9.3.4 Various Output Voltages

The following example circuits show how to use the various devices and configure the external circuitry to furnish different output voltages at 2A.

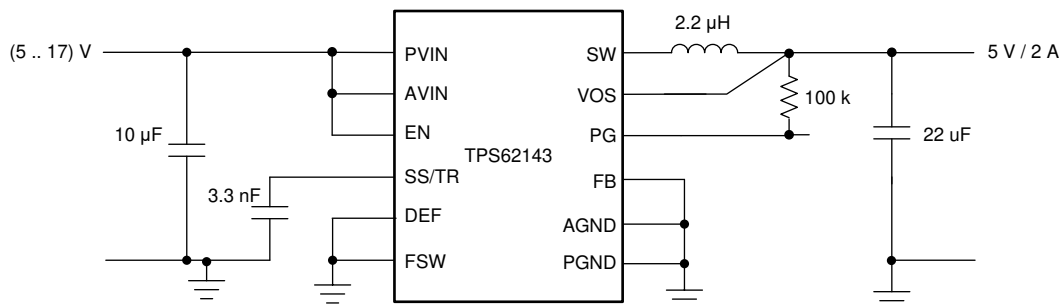


图 9-43. 5-V/2-A Power Supply

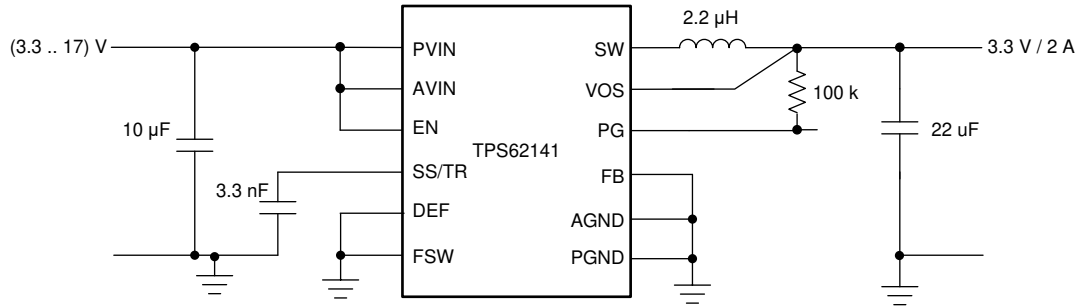


图 9-44. 3.3-V/2-A Power Supply

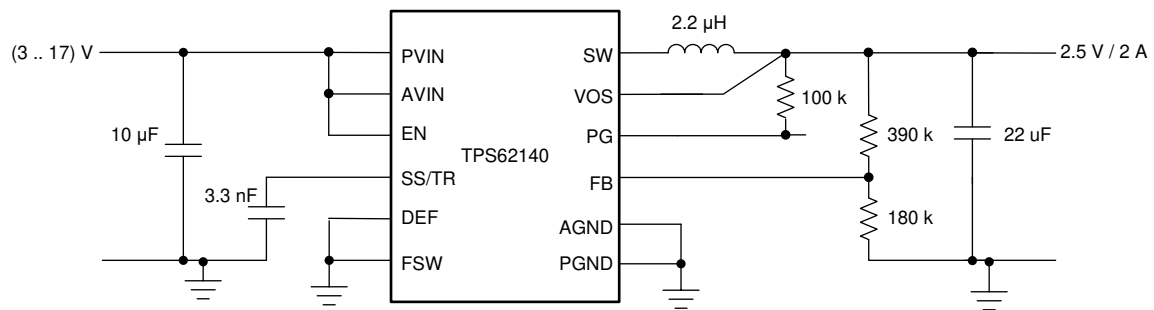


图 9-45. 2.5-V/2-A Power Supply

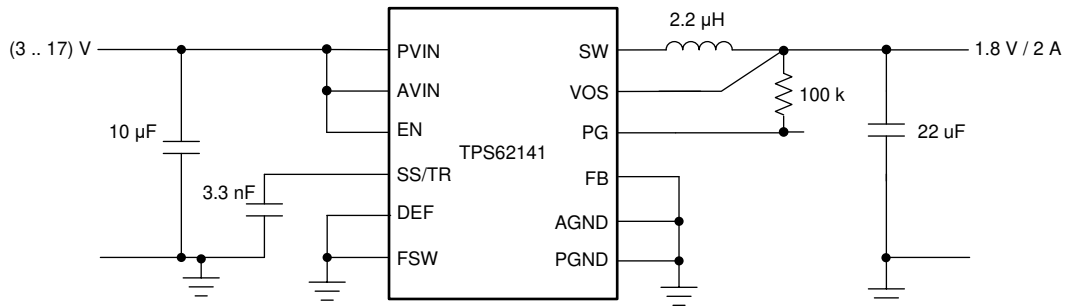
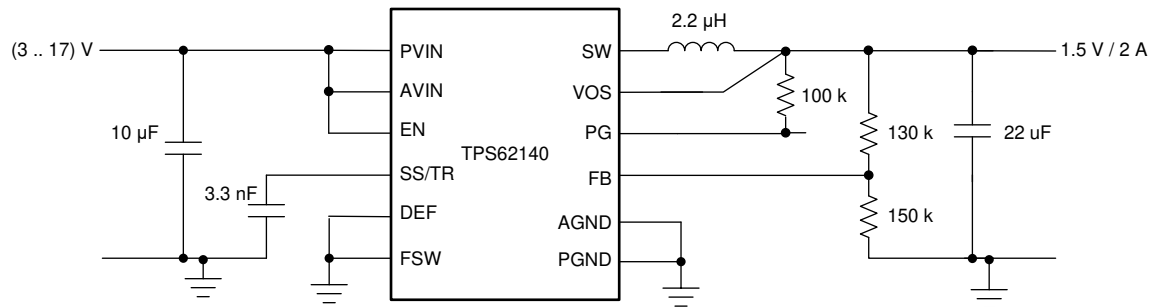
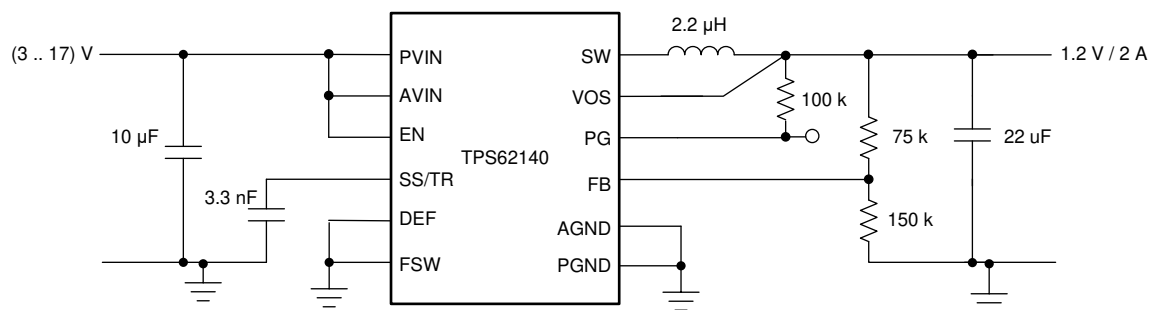


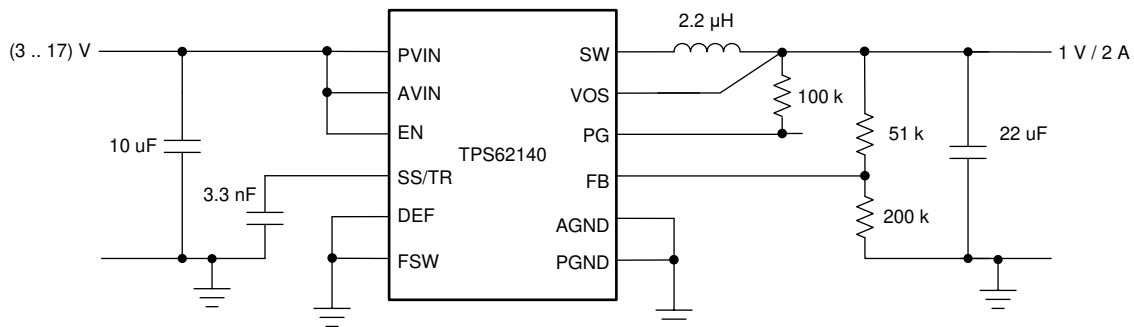
图 9-46. 1.8-V/2-A Power Supply



**图 9-47. 1.5-V/2-A Power Supply**



**图 9-48. 1.2-V/2-A Power Supply**



**图 9-49. 1-V/2-A Power Supply**

## 10 Power Supply Recommendations

The TPS6214X are designed to operate from a 3-V to 17-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

## 11 Layout

### 11.1 Layout Guidelines

A proper layout is critical for the operation of a switched-mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6214x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

See [Figure 11-1](#) for the recommended layout of the TPS6214x, which is designed for common external ground connections. Therefore both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to VOUT at the output capacitor. To avoid noise coupling into the VOS line, this connection should be separated from the VOUT power line/plane as shown in [Section 11.2](#).

Provide low inductive and resistive paths for loops with high  $di/dt$ . Therefore, paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high  $dv/dt$ . Therefore, the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high  $dv/dt$  signals (that is, SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in its Users Guide, [TPS6213x Buck Converter Evaluation Module User's Guide](#). Additionally, the [Gebers for HPA505 EVM](#) are available for download.

### 11.2 Layout Example



## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 第三方产品免责声明

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

- Users Guide, [SLVU437](#)
- EVM Gerber Data, [SLVC394](#)
- Thermal Characteristics Application Note, [SZZA017](#) and [SPRA953](#)

#### 12.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 12.4 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

#### 12.5 Trademarks

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#### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62140ARGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PA7I	<a href="#">Samples</a>
TPS62140ARGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA7I	<a href="#">Samples</a>
TPS62140RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTZ	<a href="#">Samples</a>
TPS62140RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTZ	<a href="#">Samples</a>
TPS62141RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWA	<a href="#">Samples</a>
TPS62141RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWA	<a href="#">Samples</a>
TPS62142RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWB	<a href="#">Samples</a>
TPS62142RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWB	<a href="#">Samples</a>
TPS62143RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWC	<a href="#">Samples</a>
TPS62143RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWC	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62140ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140ARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62143RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62143RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62143RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62143RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62140ARGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62140ARGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62140RGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62140RGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62140RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62141RGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62141RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62141RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62141RGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62142RGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62142RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62142RGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62142RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62143RGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62143RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62143RGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62143RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS62140ARGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62140ARGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62140RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62140RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62141RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62141RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62142RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62142RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS62143RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62143RGTT	RGT	VQFN	16	250	381	4.83	2286	0

**RGT 16**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/D 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

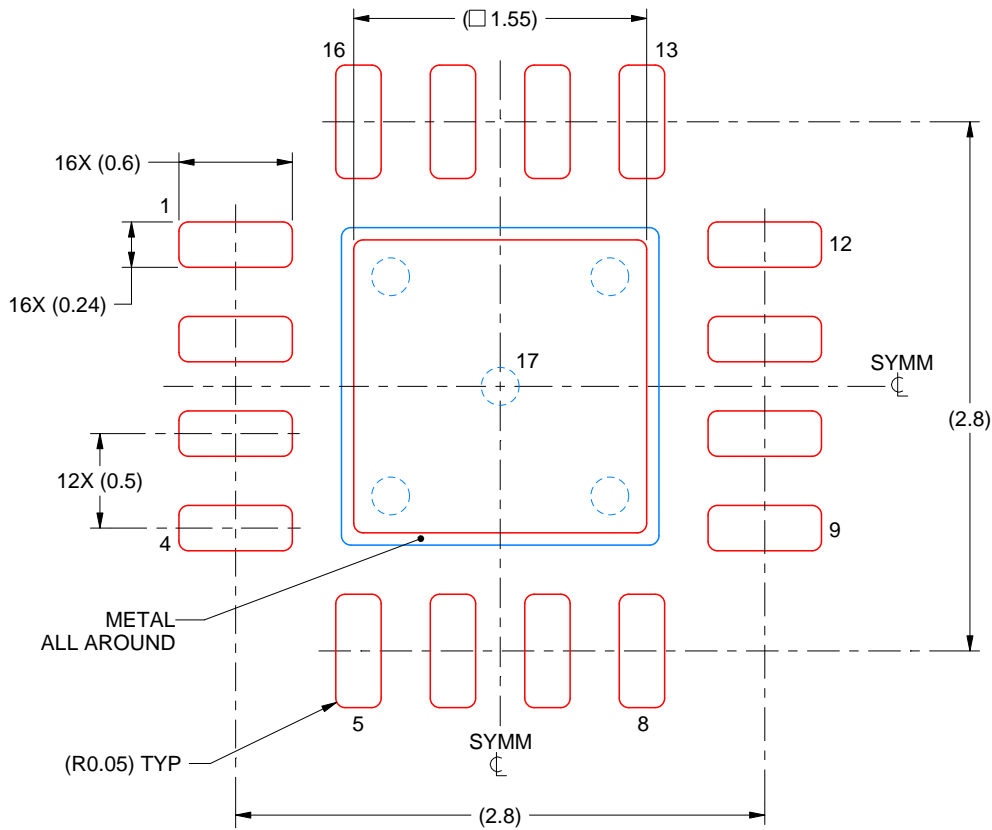


# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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