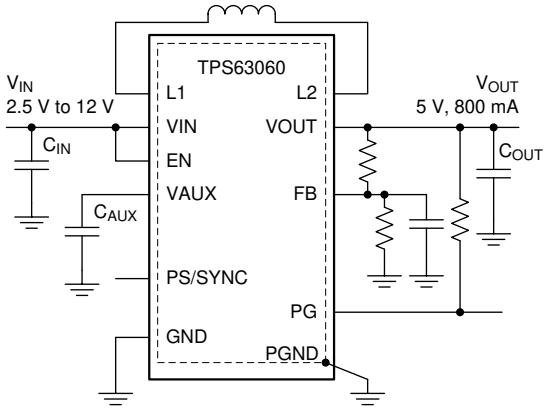
TPS6306x 具有 2A 开关电流的高输入电压降压/升压转换器

1 特性

- 输入电压范围：2.5 V 至 12 V
- 效率：高达 93%
- 5V 时的输出电流 (V_{IN} < 10V)：
  降压模式下为 2A
- 5V 时的输出电流 (V_{IN} > 4V)：
  升压模式下为 1.3A
- 在降压和升压模式之间自动转换
- 器件典型静态电流：< 30 μA
- 输出电压可以是固定的，也可以调节，范围是 2.5 V 至 8 V
- 省电模式，改善低输出功率时的效率
- 2.4MHz 强制固定频率运行，可实现同步
- 电源正常状态输出
- Buck-Boost Overlap Control™
- 关断期间负载断开
- 提供过热保护
- 过压保护

2 应用

- 双锂离子电池应用
- 数码相机 (DSC) 和便携式摄像机
- 笔记本电脑
- 工业计量设备
- 超便携电脑和移动互联网设备
- 个人医疗产品
- 大功率 LED



简化版应用

3 说明

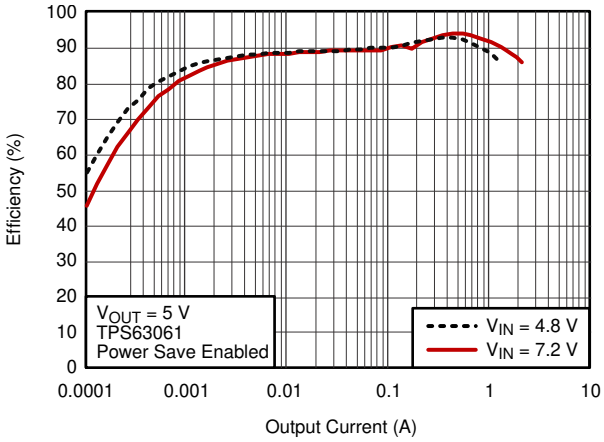
TPS6306x 器件可以为由 3 节到 6 节碱性、镍镉或镍氢电池或单节、两节锂离子或锂聚合物电池供电的产品提供电源解决方案。使用两节双锂离子或者锂聚合物电池时，输出电流可升高至 2A，放电电压可达 5V 或者更低。此升压/降压转换器基于一个频率固定的脉宽调制 (PWM) 控制器。该控制器可通过同步整流实现效率最大化。在负载电流较低的情况下，该转换器会进入节能模式，以在宽负载电流范围内保持高效率。禁用省电模式则会强制转换器以固定开关频率运行。开关的最大平均电流为 2.25 A（典型值）。输出电压可通过外部电阻分频器进行编程，或者在内部芯片上固定。可通过禁用转换器来最大限度地减少电池消耗。在关断期间，负载从电池断开。

这些器件采用 3mm×3mm 10 引脚 WSON (DSC) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS63060	WSON (10)	3.00mm × 3.00mm
TPS63061		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率与输出电流之间的关系

Table of Contents

4 Revision History

Changes from Revision B (December 2014) to Revision C (September 2020) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 将*应用*从 DSC 和便携式摄像机更改为：数码相机 (DSC) 和便携式摄像机 1
- 从*说明* 中删除了 PowerPAD™ 封装 1
- 更改了*典型应用原理图* 1
- Removed PACKAGE MARKING from the *Device Comparison Table* 3
- Changed From: PowerPAD™ To: Exposed Thermal Pad in the *Pin Functions* table 4
- Changed L1 and L2 values in the *Absolute Maximum Ratings* table 5
- Deleted Machine model (MM) from the *ESD Ratings* table 5
- Added "Thermal shutdown" and "Thermal Shutdown hysteresis" to the *Electrical Characteristics* table 6
- Deleted "Overtemperature protection" and "Overtemperature hysteresis" from the *Electrical Characteristics* table 6
- Added "Maximum reverse current" to the *Electrical Characteristics* table 6
- Added condition footnote to *Electrical Characteristics* table 6
- Changed the *Overview* section 8
- Changed 图 8-1 Title From: TPS63061 Fixed Output To: TPS63060 Adjustable 8
- Changed 图 8-2 Title From: TPS63060 Adjustable To: TPS63061 Fixed Output 8
- Split the *Soft-Start Function* and *Short-Circuit Protection* into two separate sections 9
- Moved *Synchronization* from the *Power-Save Mode* section into a separate section 11
- Changed C2 (2 x 10 µF) To: C1 (2 x 10 µF) in 图 9-1 13
- Deleted two graphs "Output Current vs Input Voltage" and "Output Current vs Input Voltage" from the *Application Curves* 16

Changes from Revision A (February 2012) to Revision B (December 2014) **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式* 部分、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 1

5 Device Comparison

Part Number (2) (1)	Output Voltage DC/DC
TPS63060DSC	Adjustable
TPS63061DSC	5 V

(1) Contact the factory to confirm availability of other fixed-output voltage versions.
(2) For detailed ordering information please check the *Package Option Addendum* section at the end of this data sheet.

6 Pin Configuration and Functions

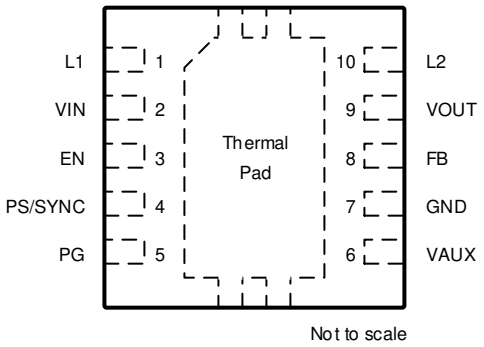


图 6-1. DSC Package 10 Pins (Top View)

Pin Functions

Pin		I/O	Description
Name	No.		
EN	3	I	Enable input (1 enabled, 0 disabled)
FB	8	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	7		Control and logic ground
L1	1	I	Connection for inductor
L2	10	I	Connection for inductor
PG	5	O	Output power good (1 good, 0 failure, open drain)
PS/SYNC	4	I	Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization)
VAUX	6		Connection for capacitor
VIN	2	I	Supply voltage for power stage
VOUT	9	O	Buck-boost converter output
Exposed Thermal Pad			Must be soldered to achieve the appropriate power dissipation. Must be connected to PGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range	EN, FB, PS/SYNC, VIN, VOUT, PG, L1, L2	– 0.3	17	V
	L1, L2 (AC, less than 10ns)	-5	18	V
	VAUX, FB	– 0.3	7.5	V
Operating virtual junction temperature range, T_J		– 40	125	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage at VIN	2.5	12	V
Output current I_{OUT} (1)		1	A
Operating free air temperature range, T_A	– 40	85	°C
Operating virtual junction temperature range, T_J	– 40	125	°C

(1) $10 \leqslant V_{IN} \leqslant 12$ V

7.4 Thermal Information

THERMAL METRIC(1)		TPS63060 TPS63061 DSC 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	19.8	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	19.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			2.5		12	V
V_{IIN}	Minimum input voltage for startup					2.5	V
V_{OUT}	Output voltage		TPS63060	2.5		8	V
		$V_{PS/SYNC}$ = GND referenced to 5 V	TPS63061	0.6%		5%	
D_{MIN}	Minimum duty-cycle in step down conversion				10%	20%	
I_{OUT}	Output current at 5V in buck mode	V_{IN} <10 V			2		A
	Output current at 5V in boost mode	V_{IN} >4 V			1.3		A
V_{FB}	Feedback voltage	$V_{PS/SYNC}$ = V_{IN}	TPS63060	495	500	505	mV
		$V_{PS/SYNC}$ = GND referenced to 500 mV		0.6%		5%	
f_{OSC}	Oscillator frequency			2200	2400	2600	kHz
	Frequency range for synchronization			2200	2400	2600	kHz
I_{SW}	Average inductance current limit	V_{IN} = 5 V		2000	2250	2500	mA
$R_{DS(on)H}$	High-side MOSFET on-resistance	V_{IN} = 5 V			90		mΩ
$R_{DS(on)L}$	Low-side switch MOSFET on-resistance	V_{IN} = 5 V			95		mΩ
	Line regulation	Power save mode disabled			0.5%		
	Load regulation	Power save mode disabled			0.5%		
I_Q	Input voltage quiescent current	I_{OUT} = 0 mA, V_{EN} = V_{IN} = 5 V, V_{OUT} = 5 V			30	60	µA
I_Q	Output voltage quiescent current				7	15	µA
R_{FB}	FB input impedance	V_{EN} = HIGH	TPS63061		1.5		MΩ
I_S	Shutdown current	V_{EN} = 0 V, V_{IN} = 5 V			0.3	2	µA
CONTROL STAGE							
V_{AUX}	Maximum bias voltage	V_{IN} > V_{OUT}		V_{IN}		7	V
		V_{IN} < V_{OUT}		V_{OUT}		7	V
I_{AUX}	Load current at V_{AUX}					1	mA
UVLO	Under voltage lockout threshold	V_{IN} falling		1.8	1.9	2.2	V
	Under voltage lockout hysteresis				300		mV
	Thermal shutdown	Temperature rising			140		°C
	Thermal Shutdown hysteresis				20		°C
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current	Clamped on GND or V_{IN}			0.01	0.1	µA
	PG output low voltage	V_{OUT} = 5 V, I_{PGL} = 10 µA			0.04	0.4	V
	PG output leakage current				0.01	0.1	µA
	Output overvoltage protection			12		16	V
I_{lim_neg}	Maximum reverse current	V_{IN} = 5 V				900	mA
t_{trans}	Time from PS/SYNC pin going low to start operating in PFM(1)				4.8	10	µs

(1) Specified by design. Not production tested.

7.6 Typical Characteristics

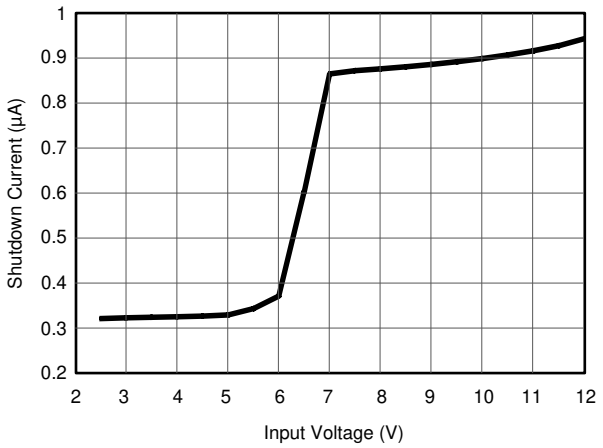


图 7-1. Shutdown Current vs Input Voltage

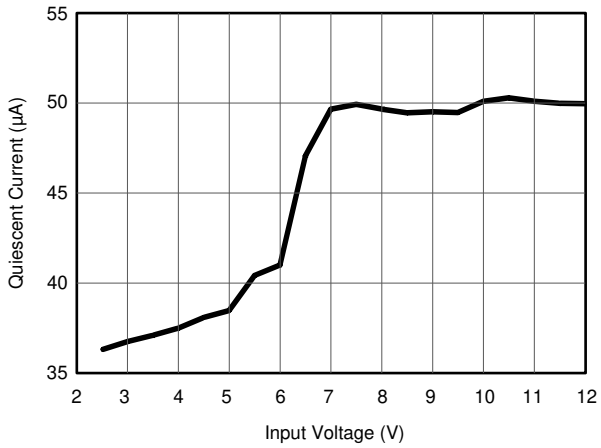


图 7-2. Quiescent Current vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS6306x use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over the complete input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch is held on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching at the same time. Keeping one switch on and one switch off eliminates their switching losses. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep higher efficiency.

The device provides a seamless transition from buck to boost or from boost to buck operation.

8.2 Functional Block Diagrams

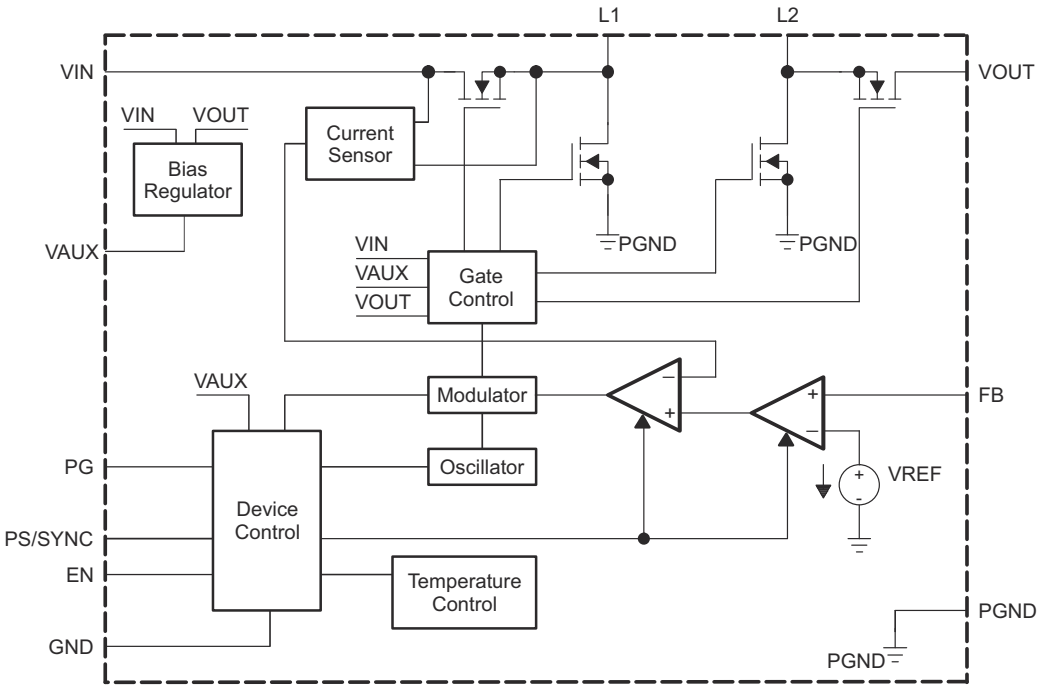


图 8-1. TPS63060 Adjustable

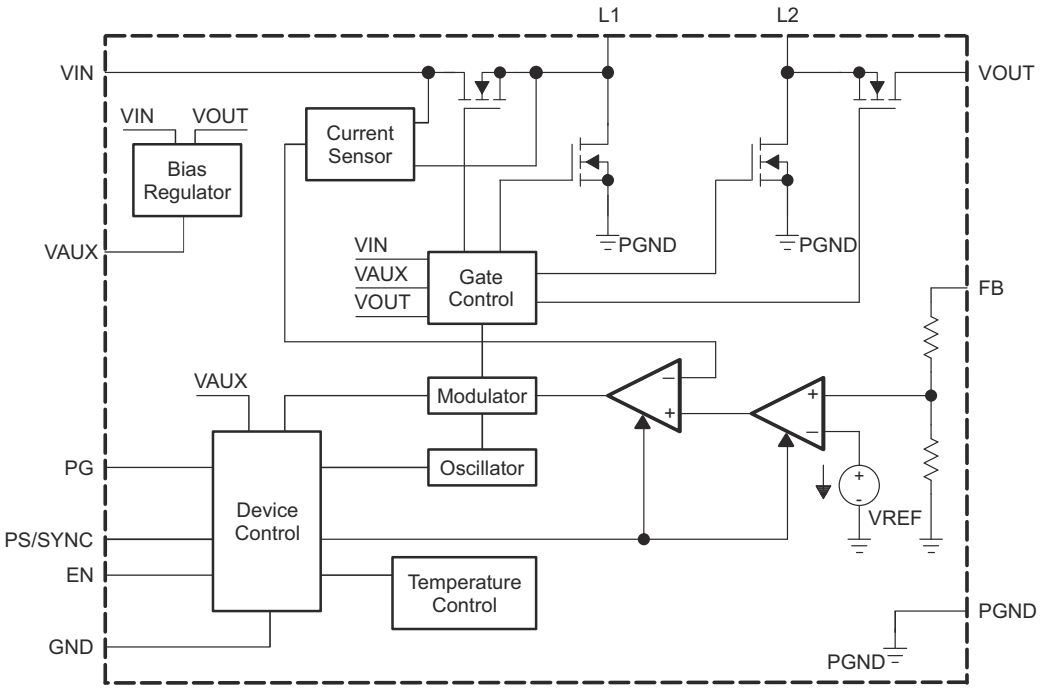


图 8-2. TPS63061 Fixed Output

8.3 Feature Description

8.3.1 Power Good

The device has a built in power good function to indicate whether the output voltage is regulated properly. As soon as the average inductor current gets limited to a value below the current the voltage regulator demands for maintaining the output voltage the power good output gets low impedance. The output is open drain, so its logic function can be adjusted to any voltage level the connected logic is using, by connecting a pull up resistor to the supply voltage of the logic. By monitoring the status of the current control loop, the power good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react.

8.3.2 Soft-Start Function

After being enabled, the device starts operating. The average current limit ramps up from an initial 400 mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit does not increase. The device implements no timer. Thus, the output voltage overshoot at startup, as well as the inrush current, remains at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output.

8.3.3 Short-Circuit Protection

When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. During a short-circuit situation on the output, the device maintains the current limit below 2 A typically (minimum average inductance current).

8.3.4 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage no longer works. Therefore, overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it supplies. The implemented overvoltage protection circuit monitors the output voltage internally as well. If it reaches the overvoltage threshold, the voltage amplifier regulates the output voltage to this value.

8.3.5 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VIN is lower than approximately its threshold (see the 节 7.5 table). When in operation, the device automatically enters the shutdown mode if the voltage on VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

8.3.6 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal device temperature. If the temperature exceeds the programmed threshold (see the 节 7.5 table) the device stops operating. As soon as the device temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at device temperatures at the overtemperature threshold.

8.4 Device Functional Modes

8.4.1 Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when the input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses.

8.4.2 Control Loop

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. 图 8-3 shows the control loop.

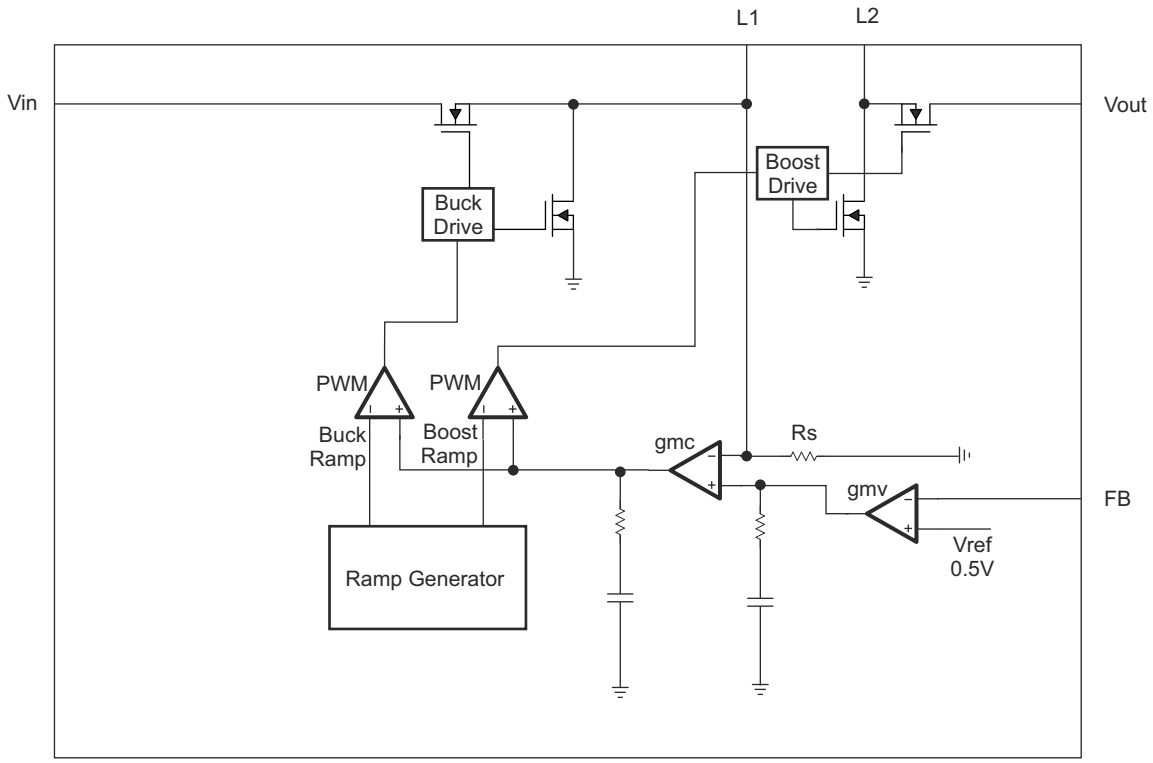


图 8-3. Average Current Mode Control

The non inverting input of the transconductance amplifier, g_{MV}, is assumed to be constant. The output of g_{MV} defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the on time of the same MOSFET. During the off time, the current is reconstructed internally starting from the peak value at the end of the on-time cycle. The average current is compared to the desired value and the difference, or current error, is amplified and compared to the buck or the boost sawtooth ramp. Depending on which of the two ramps the g_{MC} amplified output crosses, the device acitvates either the buck MOSFETs or the boost MOSFETs. When the input voltage is close to the output voltage, one boost cycle always follows a buck cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

8.4.3 Power-Save Mode

The PS/SYNC pin can be used to select different operation modes. Power save mode improves efficiency at light load. To enable power save mode, PS/SYNC must be set low. The device enters power save mode when the average inductor current falls to a level lower than approximately 100 mA. In that situation, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

During the power save mode operation, the output voltage is monitored with a comparator by the threshold comparator low and comparator high. When the device enters power save mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comparator low threshold set to 2.5% typical above the output voltage, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter continues these pulses until the comparator high threshold, set to typically 3.5% above the nominal output voltage, is reached and the average inductor current gets lower than about 100 mA. When the load increases above the minimum forced inductor current of about 100 mA, the device automatically switches to PWM mode.

The power save mode can be disabled by programming the PS/SYNC high.

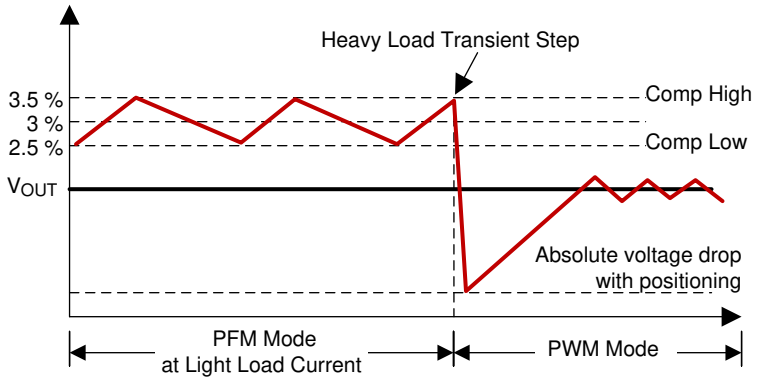


图 8-4. Power-Save Mode Thresholds and Dynamic Voltage Positioning

8.4.4 Synchronization

Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a PLL to lower and higher frequencies compared to the internal clock. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

8.4.5 Dynamic Voltage Positioning

The output voltage is typically 3% above the nominal output voltage at light-load currents, as the device is operating in power save mode. This operation mode allows additional headroom for the voltage drop during a load transient from light load to full load. This additional headroom allows the converter to operate with a small

output capacitor and maintain a low absolute voltage drop during heavy load transient changes. See 图 8-4 for detailed operation of the power save mode operation.

8.4.6 Dynamic Current Limit

The dynamic current limit function maintains the output voltage regulation when the power source becomes weaker. The maximum current allowed through the switch depends on the voltage applied at the input terminal of the TPS6306x devices. 图 8-5 shows this dependency, and the I_{SW} vs V_{IN}. The dynamic current limit has its lowest value when reaching the minimum recommended supply voltage at V_{IN}.

Given the I_{SW} value from 图 8-5, is then possible to calculate the output current reached in boost mode using 方程式 1 and 方程式 2 and in buck mode using 方程式 3 and 方程式 4.

Duty Cycle Boost $$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

Maximum Output Current Boost $$I_{OUT} = \eta \times I_{SW} \times (1 - D) \quad (2)$$

Duty Cycle Buck $$D = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Maximum Output Current Buck $$I_{OUT} = I_{SW} \quad (4)$$

where

- η is the estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
- f is the converter switching frequency (typical 2.4 MHz)
- L is the selected inductor value

If the die temperature increases above the recommended maximum temperature, the dynamic current limit becomes active. The current limit is reduced with temperature increasing.

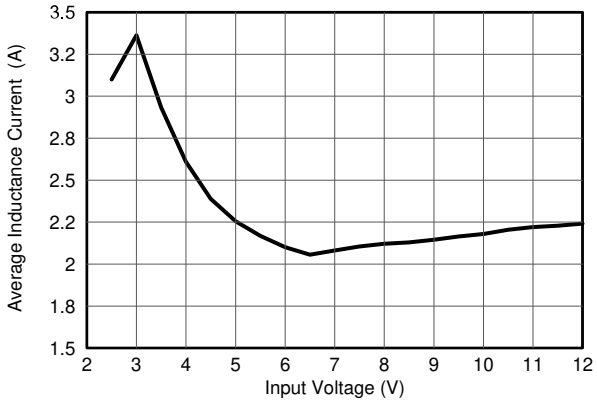


图 8-5. Average Inductance Current vs Input Voltage

8.4.7 Device Enable

The device operates when EN is set high. The device enters a shutdown sequence when EN is set to GND. During the shutdown sequence, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. It is possible for the output voltage to drop below the input voltage during shutdown. During the start-up sequence, the device limits the duty cycle and the peak current in order to avoid high peak currents flowing from the input.

9 Application and Implementation

备注

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPS6306x devices provide a power supply solution for products powered by either three-cell up to six-cell alkaline, NiCd or NiMH battery, or a one-cell or dual-cell Li-Ion or Li-polymer battery. Output currents can go as high as 2-A while using a dual-cell Li-Ion or Li-polymer battery, and discharge it down to 5 V or lower.

9.2 Typical Application

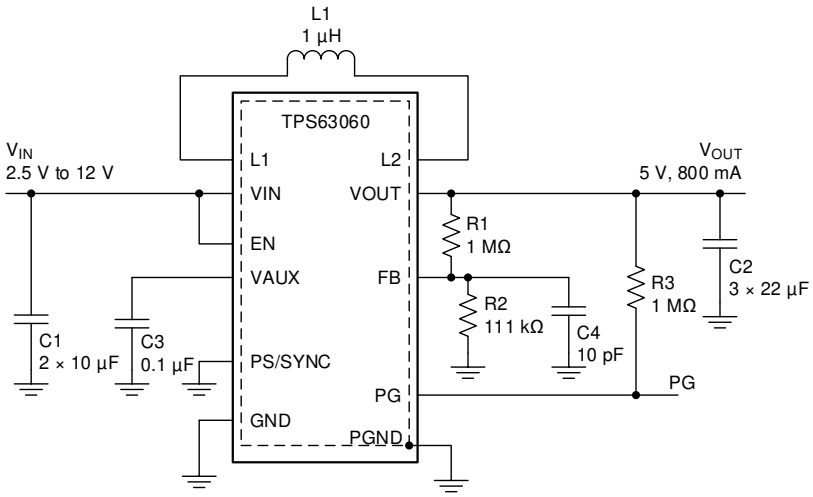


图 9-1. 5-V Adjustable Buck-Boost Converter Application

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. 表 9-1 lists the components used in this application.

表 9-1. Components for Application Characteristic Curves

Reference	Description	Manufacturer(1)
	TPS63060 and TPS63061	Texas Instruments
L1	1 µH, 3 mm x 3 mm x 1.5 mm	Coilcraft , XFL4020-102
C1	2 × 10 µF 16V, 0805, X5R ceramic	Taiyo Yuden, EMK212BJ
C2	3 × 22 µF 16V, 0805, X5R ceramic	Taiyo Yuden, LMK212BJ
C3	0.1 µF, X5R ceramic	
C4	10 pF, ceramic	
R1, R2	Depending on the output voltage at TPS63060 and TPS63061: R1=0, C4 and R2 n.a.	

(1) See 节 12.1

9.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, use 表 9-2 to compare inductor and capacitor value combinations.

9.2.2.1 Step One: Output Filter Design

表 9-2. Output Capacitor and Inductor Combinations

Inductor Value [µH](1)	Output Capacitor Value [µF](2)		
	44	66	100
1.0	√	√ (3)	√
1.5	√	√	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and – 30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and – 50%.
(3) Typical application. Other check mark indicates recommended filter combinations

9.2.2.2 Step Two: Inductor Selection

The inductor selection is affected by several parameters including inductor ripple current, output voltage ripple, transition point into power-save mode, and efficiency. See 表 9-3 for typical inductors.

表 9-3. List of Recommended Inductors

Inductor Value (µH)	Component Suplier(1)	Size (L×W×H) (mm)	Current Saturation (I_{SAT}) (A)	DCR (mΩ)
1	Coilcraft XFL4020-102	4 × 4 × 2.1	5.1	10.8
1	TOKO DEM2815 1226AS-H-1R0N	3 × 3.2 × 1.5	2.7	27
1.5	Coilcraft XFL4020-152	4 × 4 × 2.1	4.4	14.4

(1) See 节 12.1

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, with the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. 方程式 1 and 方程式 5 show how to calculate the peak current I_{PEAK}. Only the equation which defines the switch current in boost mode is reported because this is providing the highest value of current and represents the critical current value for selecting the right inductor.

$$I_{PEAK} = \frac{I_{OUT}}{\eta \times (1 - D)} + \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \quad (5)$$

where

- D is the duty cycle during boost mode operation
- f_{SW} is the converter switching frequency (typical 2.4 MHz)
- L is the selected inductor value
- η is the estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
- The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It's recommended to choose an inductor with a saturation current 20% higher than the value calculated using 方程式 5. Possible inductors are listed in 表 9-3.

9.2.2.3 Step Three: Capacitor Selection

9.2.2.3.1 Input Capacitors

To improve transient behavior of the regulator and EMI behavior of the total power supply circuit, this design suggests a minimum input capacitance of 20 µF. Place a ceramic capacitor placed as close as possible to the VIN and PGND pins of the device.

9.2.2.3.2 Output Capacitor

For the output capacitor, use of a small ceramic capacitor placed as close as possible to the VOUT and PGND pins of the device is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the device, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and PGND pins of the device. The recommended typical output capacitor value is 66 µF with a variance as outlined in 表 9-1.

There is also no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

When choosing input and output capacitors, it needs to be kept in mind, that the value of capacitance experiences significant losses from their rated value depending on the operating temperature and the operating DC voltage. It is not uncommon for a small surface mount ceramic capacitor to lose 50% and more of its rated capacitance. For this reason, it is important to use a larger value of capacitance or a capacitor with higher voltage rating in order to ensure the required capacitance at the full operating voltage.

9.2.2.3.3 *Bypass Capacitor*

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor is connected between VAUX and GND. Using a ceramic capacitor with a value of 0.1 µF is recommended. The capacitor needs to be placed close to the VAUX pin. The value of this capacitor should not be higher than 0.22 µF.

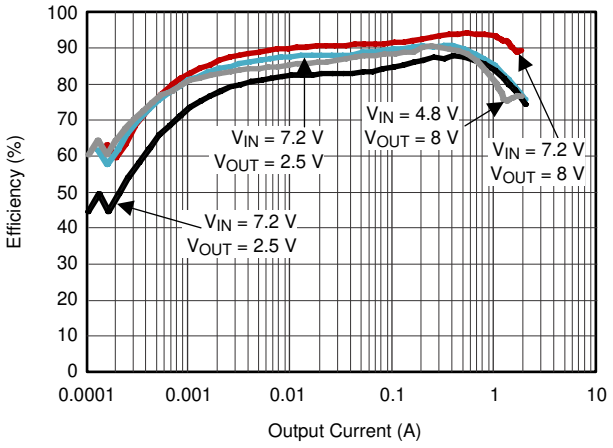
9.2.2.4 Step Four: Setting the Output Voltage

When the adjustable output voltage version TPS63060 is used, the output voltage is set by the external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. The maximum recommended value for the output voltage is 8V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 500 kΩ, in order to set the divider current at 3 µA or higher. It is recommended to keep the value for this resistor in the range of 200 kΩ. From that, the value of the resistor connected between the VOUT pin and the FB pin, (R1) depending on the needed output voltage can be calculated using 方程式 6.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (6)$$

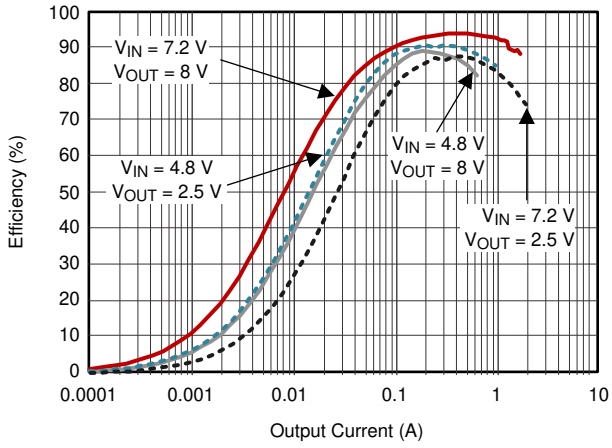
Place a small capacitor (C4, 10 pF) in parallel with R2 when using the power save mode and the adjustable version, to provide filtering and improve the efficiency at light load.

9.2.3 Application Curves



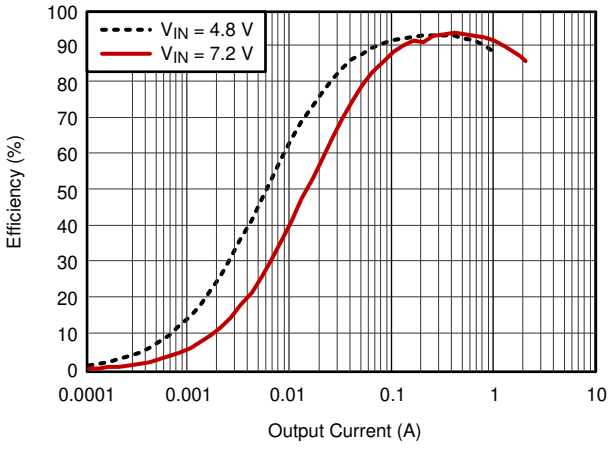
TPS63060 Power Save Enabled

图 9-2. Efficiency vs. Output Current



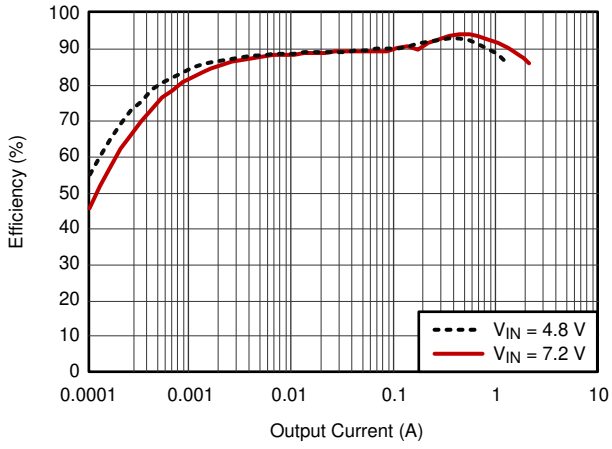
TPS63060 Power Save Disabled

图 9-3. Efficiency vs. Output Current



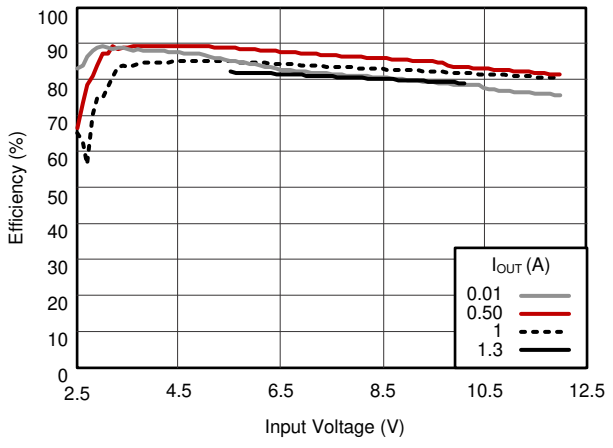
TPS63061 Power Save Disabled

图 9-4. Efficiency vs. Output Current



TPS63061 Power Save Enabled

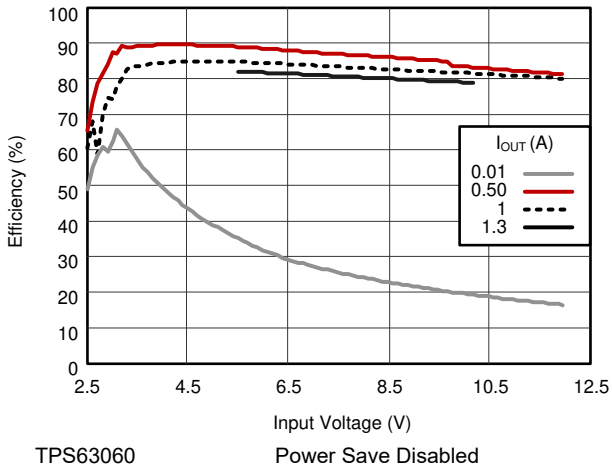
图 9-5. Efficiency vs. Output Current



TPS63060 Power Save Enabled

V_{OUT} = 2.5 V

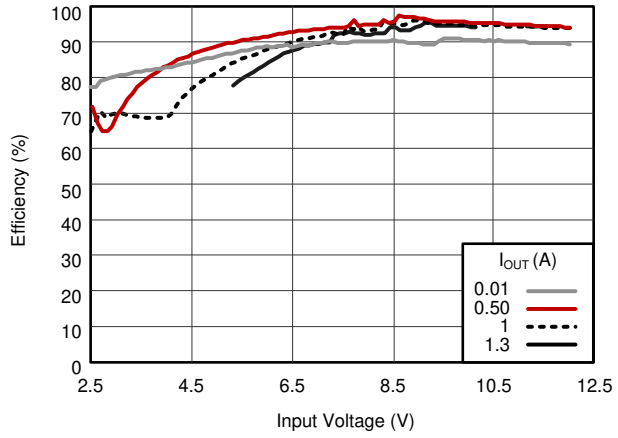
图 9-6. Efficiency vs. Input Voltage



TPS63060 Power Save Disabled

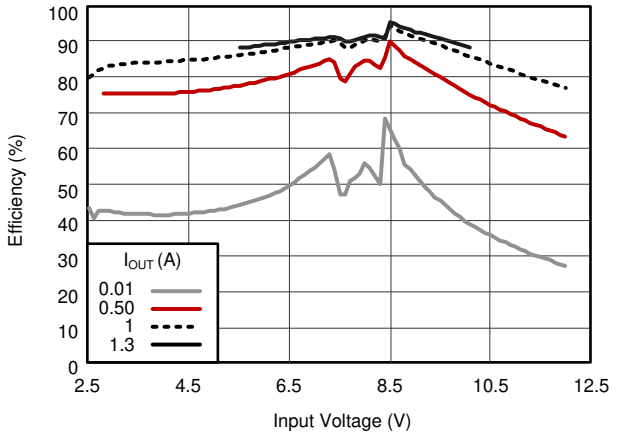
V_{OUT} = 2.5 V

图 9-7. Efficiency vs. Input Voltage



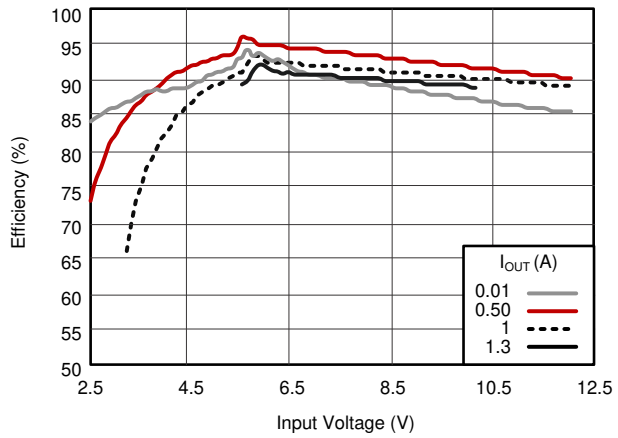
TPS63060 Power Save Enabled
V_{OUT} = 8 V

图 9-8. Efficiency vs. Input Voltage



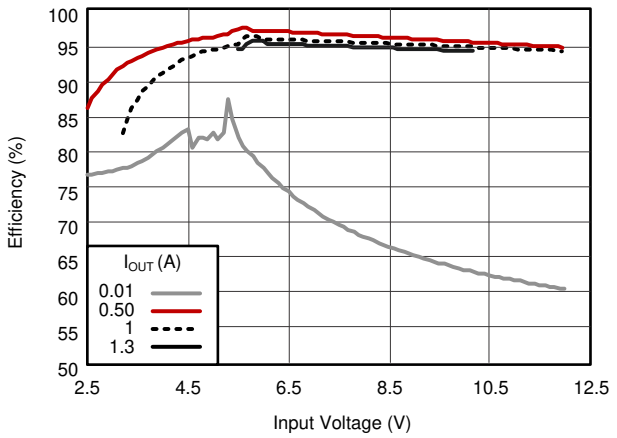
TPS63060 Power Save Disabled
V_{OUT} = 8 V

图 9-9. Efficiency vs. Input Voltage



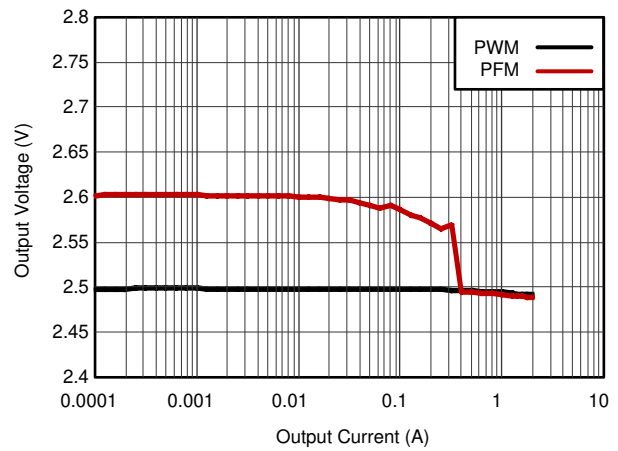
TPS63061 Power Save Enabled
V_{OUT} = 5 V

图 9-10. Efficiency vs. Input Voltage



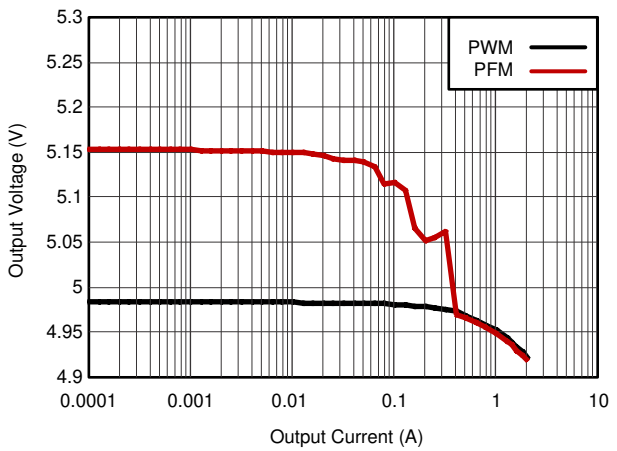
TPS63061 Power Save Disabled
V_{OUT} = 5 V

图 9-11. Efficiency vs. Input Voltage



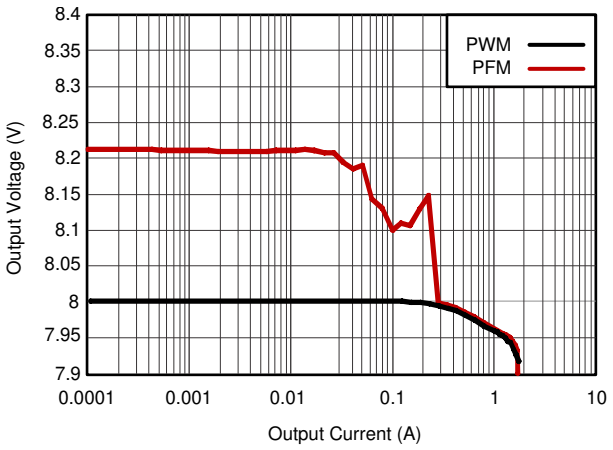
TPS63060 Power Save Disabled
V_{OUT} = 2.5 V V_{IN} = 7.2 V

图 9-12. Output Voltage vs Output Current



TPS63061
V_{IN} = 7.2 V

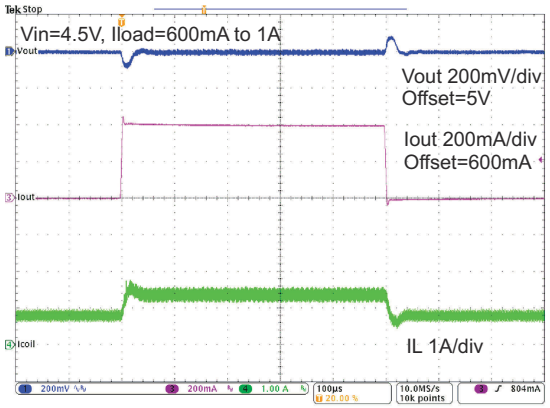
图 9-13. Output Voltage vs Output Current



TPS63060

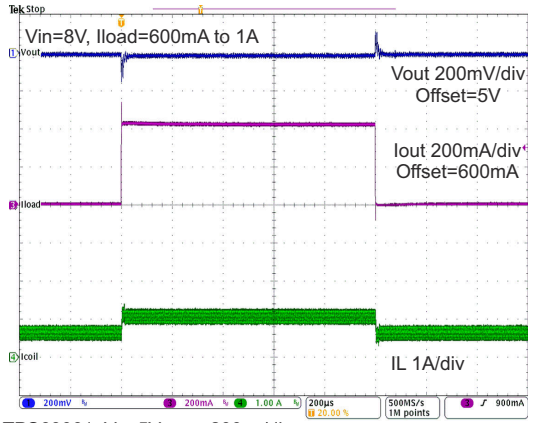
V_{OUT} = 8 V V_{IN} = 7.2 V

图 9-14. Output Voltage vs Output Current



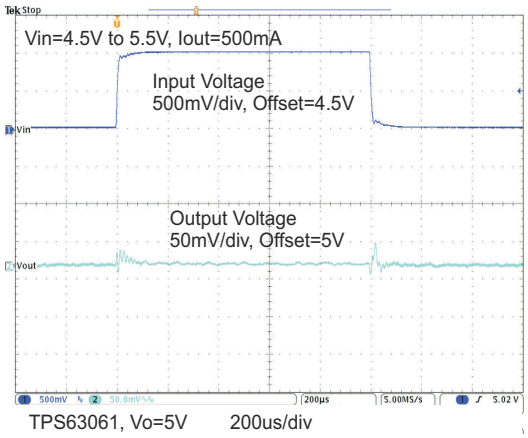
TPS63061, Vo=5V 100us/div

图 9-15. Load Transient Response



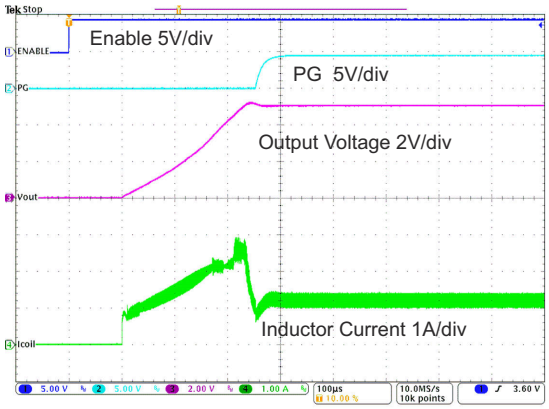
TPS63061, Vo=5V 200us/div

图 9-16. Load Transient Response



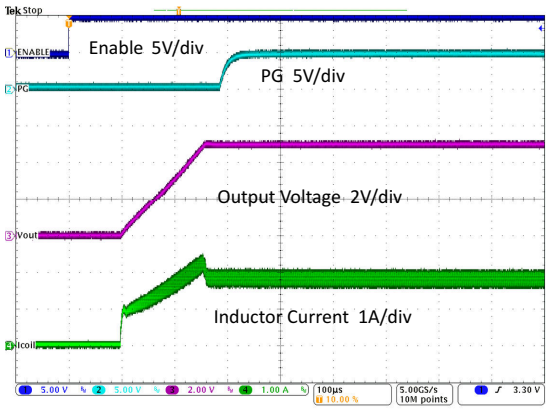
TPS63061, Vo=5V 200us/div

图 9-17. Line Transient Response



TPS63061, Vo=5V 100us/div Vin=4.5V, Io=1A

图 9-18. Startup After Enable



TPS63061, Vo=5V 100us/div Vin=8V, Io=2A

图 9-19. Startup After Enable

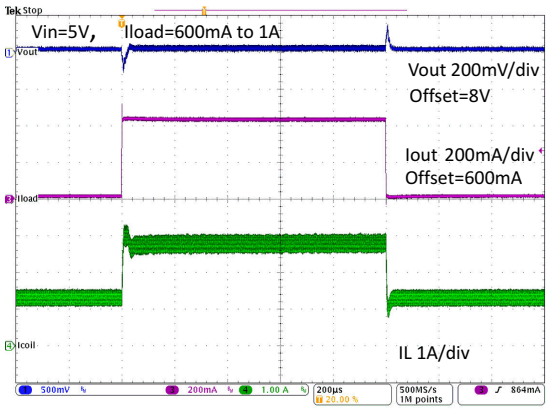


图 9-20. Load Transient

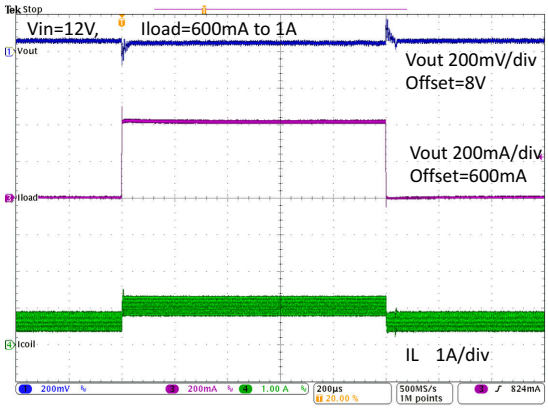


图 9-21. Load Transient

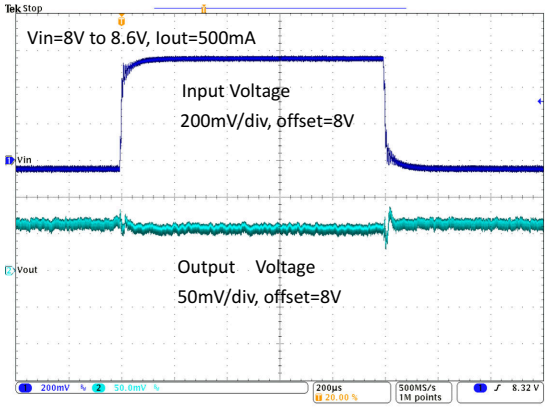


图 9-22. Line Transient

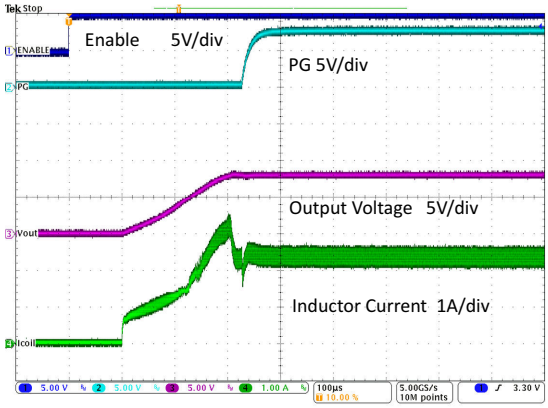


图 9-23. Startup After Enable

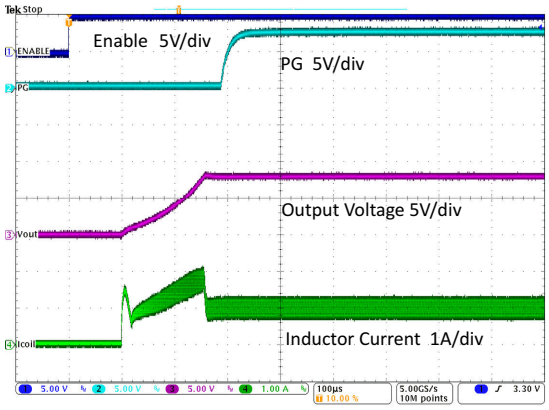


图 9-24. Startup After Enable

10 Power Supply Recommendations

The TPS6306x device family has no special requirements for its input power supply. The input supply output current must be rated according to the supply voltage, output voltage and output current of the TPS6306x.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the device. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the device.

The feedback divider should be placed as close as possible to the control ground pin of the device. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

11.2 Layout Example

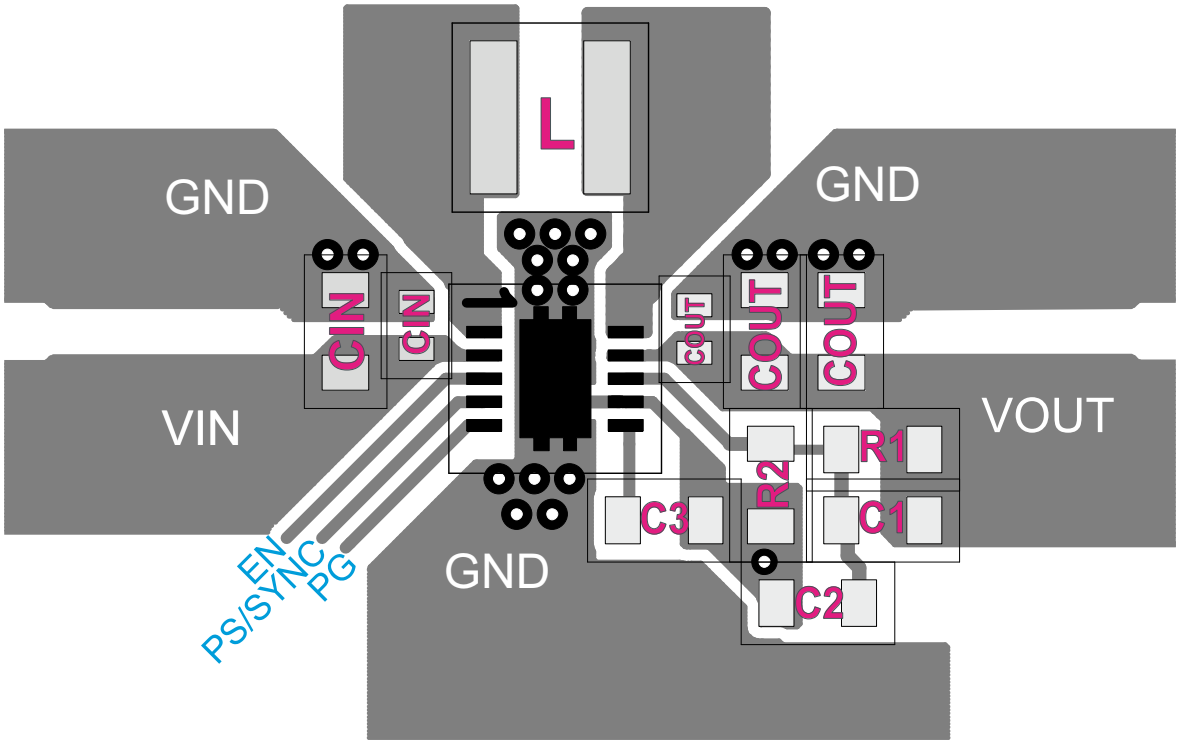


图 11-1. TPS6306x Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- TPS63060EVM-619 2.25-A, Buck-Boost Converter Evaluation Module (click here)
- TPS63060EVM-619 Gerber Files (SLVC409)
- TPS63060 PSpice Transient Model (SLVM477)

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Design Calculations for Buck-Boost Converters (SLVA535)
- Extending the Soft-Start Time in the TPS63010 Buck-Boost Converter (SLVA553)
- Different Methods to Drive LEDs Using TPS63xxx Buck-Boost Converters (SLVA419)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

12.5 Trademarks

Buck-Boost Overlap Control™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63060DSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QUJ	Samples
TPS63060DSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QUJ	Samples
TPS63061DSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QUK	Samples
TPS63061DSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QUK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS63060 :

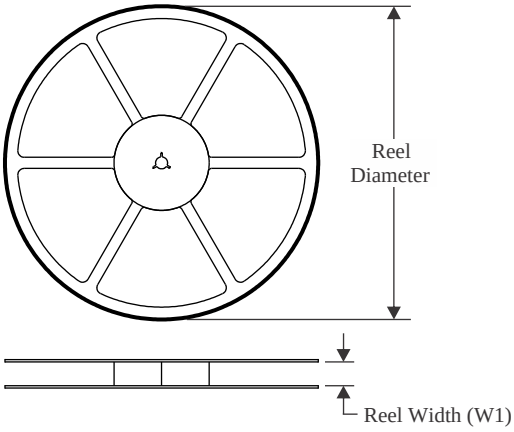
- Enhanced Product : TPS63060-EP

NOTE: Qualified Version Definitions:

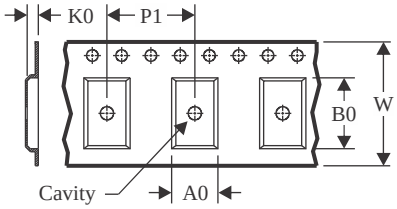
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

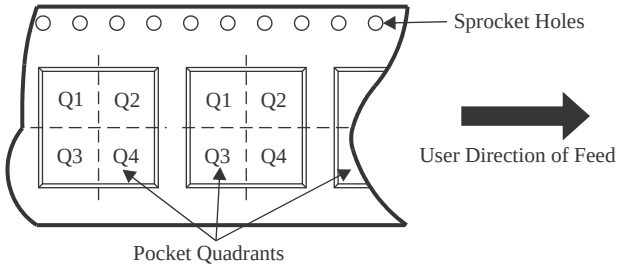


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

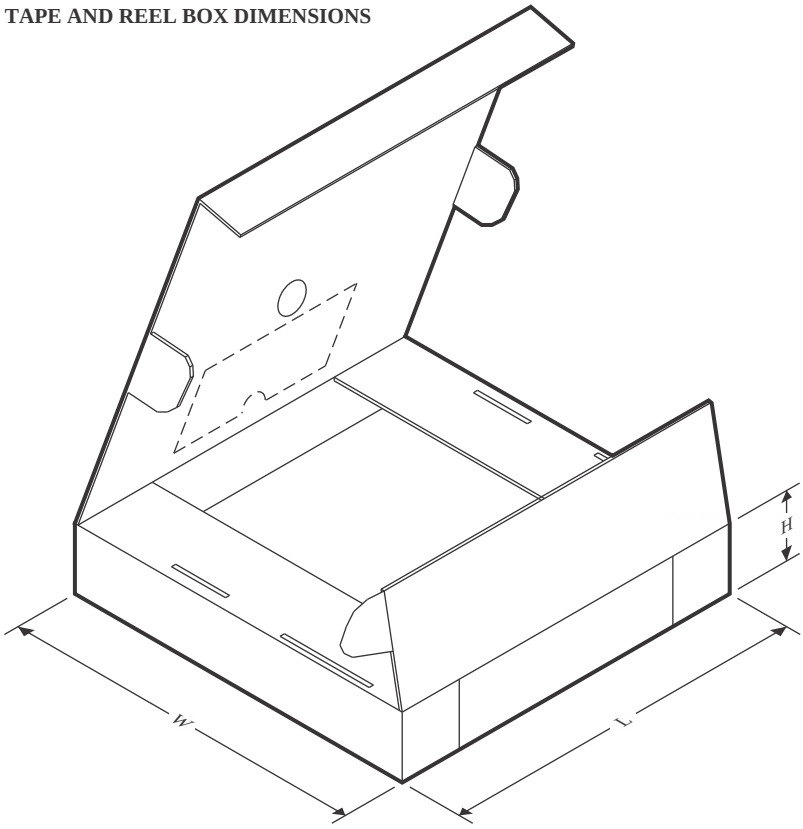
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63060DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63060DSCT	WSON	DSC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS63061DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63061DSCT	WSON	DSC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



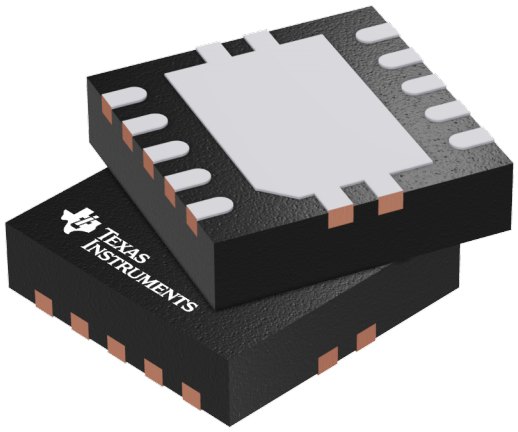
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63060DSCR	WSON	DSC	10	3000	356.0	356.0	35.0
TPS63060DSCT	WSON	DSC	10	250	205.0	200.0	33.0
TPS63061DSCR	WSON	DSC	10	3000	356.0	356.0	35.0
TPS63061DSCT	WSON	DSC	10	250	205.0	200.0	33.0

GENERIC PACKAGE VIEW

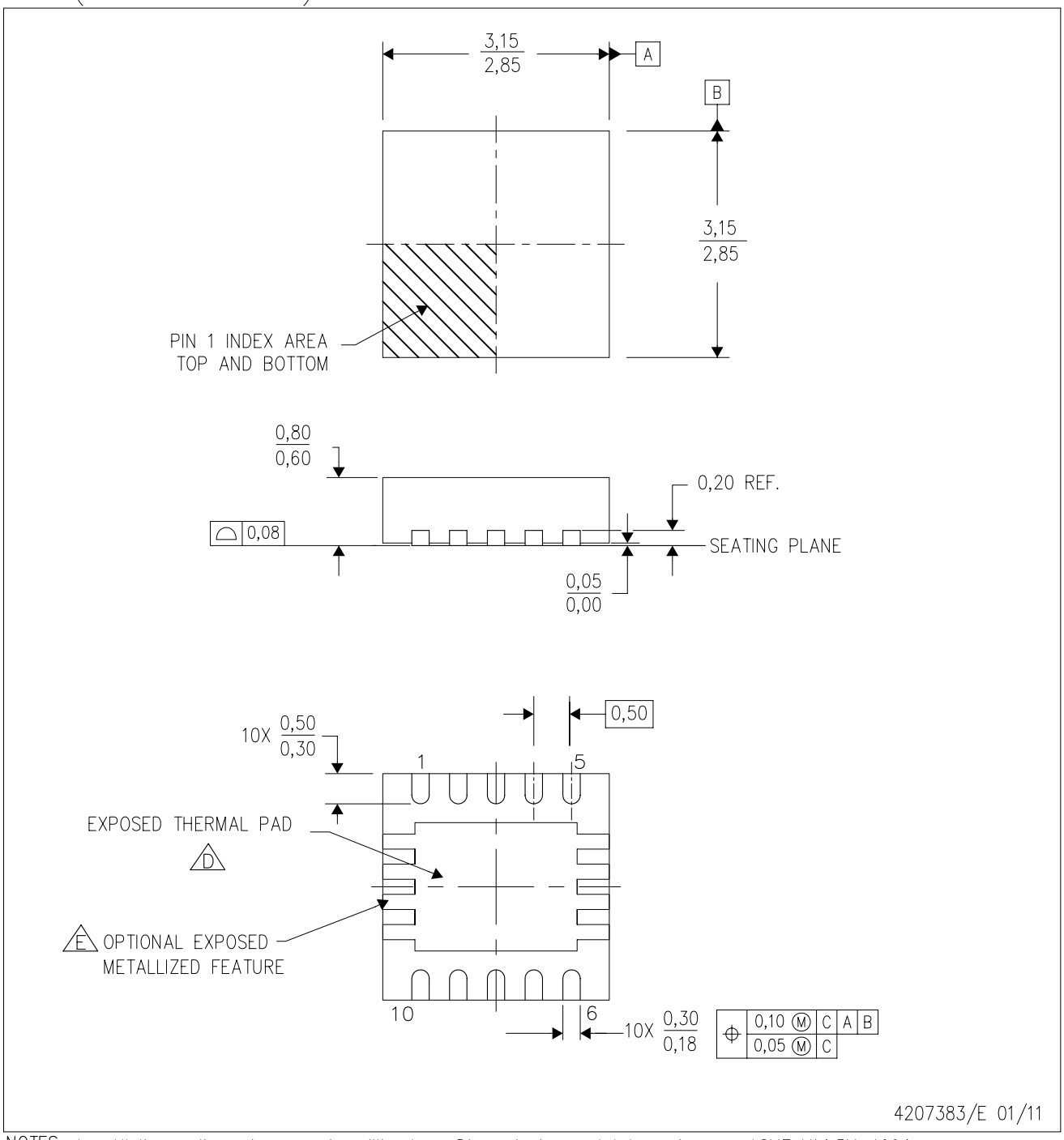
DSC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

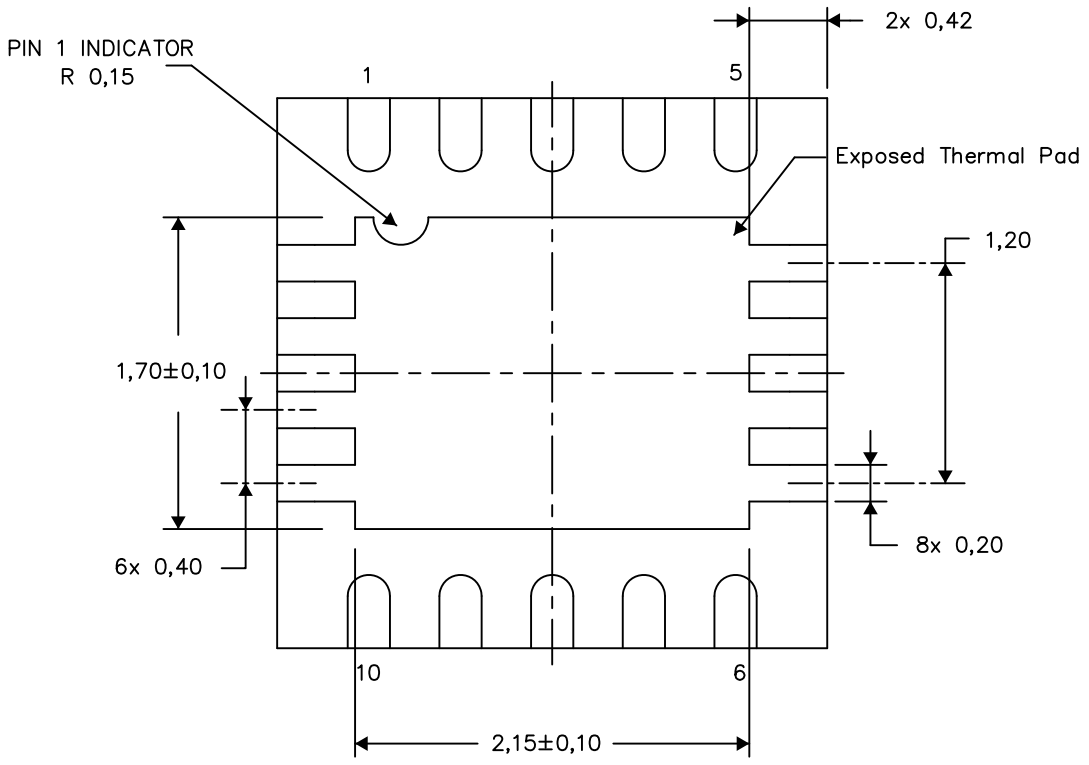
DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



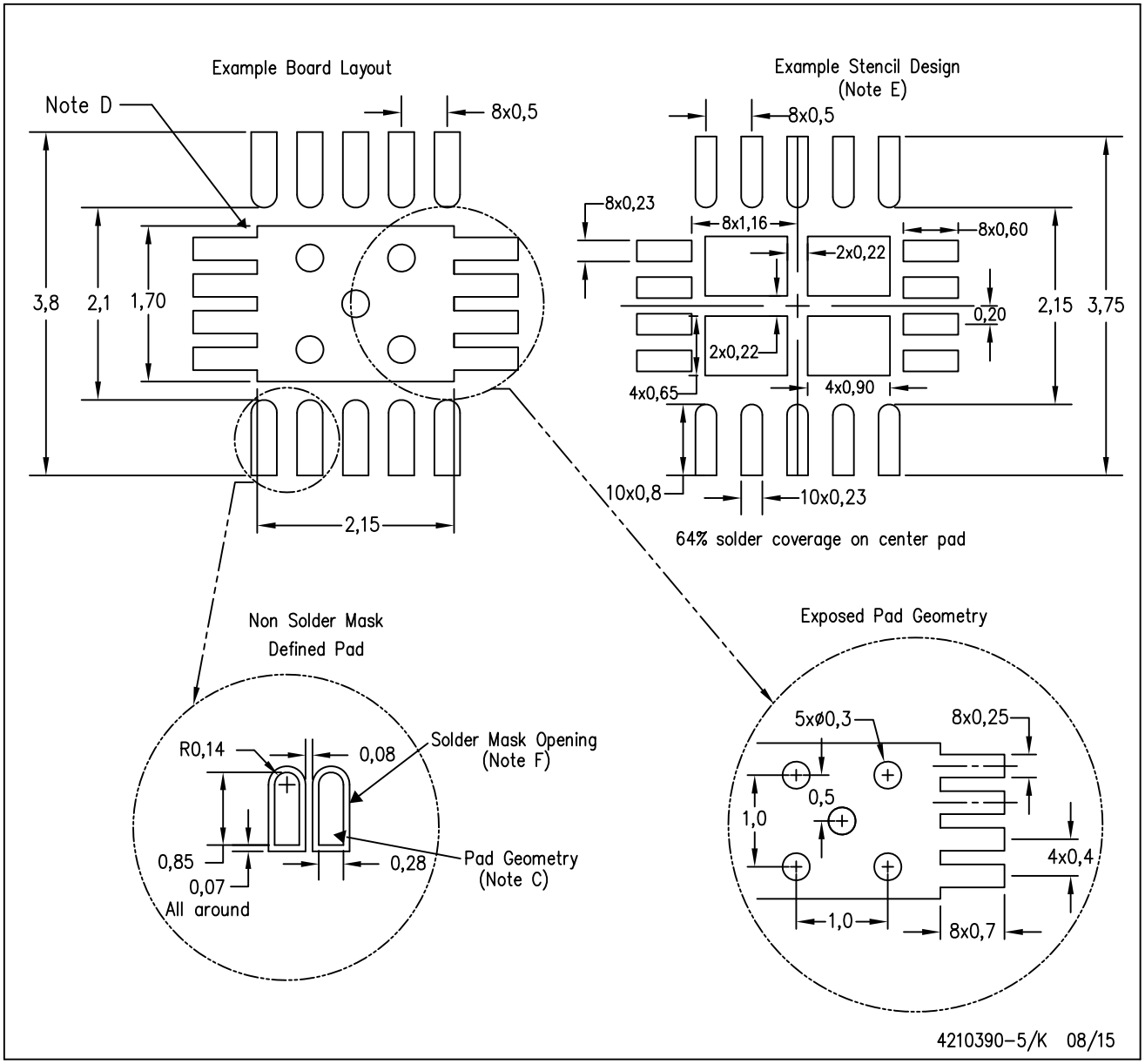
Bottom View

Exposed Thermal Pad Dimensions

4210391–5/Q 08/15

NOTE: A. All linear dimensions are in millimeters

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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