

TPS65631W 双输出有源矩阵有机发光二极管 (AMOLED) 显示屏电源

1 特性

- 2.9V 至 4.5V 输入电压范围
- 4.6V 固定正输出电压
- 25°C 至 85°C 温度范围内， V_{POS} 精度 0.5%
- 单独的 V_{POS} 输出感测引脚
- -1.4V 至 -4.4V 的数字可编程负输出电压（缺省值 -4V）
- 支持高达 200mA 的输出电流
- 出色的线路瞬态稳压
- 短路保护功能
- 热关断
- 采用 2.5mm x 2.5mm 10 引脚四方扁平无引线 (QFN) 封装

2 应用范围

AMOLED 显示屏

3 说明

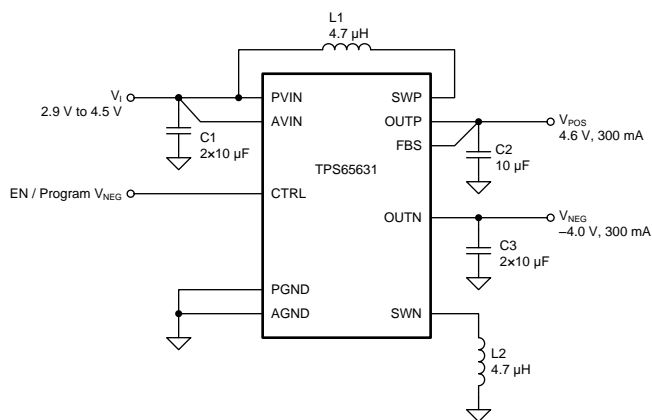
TPS65631W 被设计用于驱动需要正负电源轨的 AMOLED 显示屏。此器件集成了一个针对 V_{POS} 的升压转换器和一个针对 V_{NEG} 的反相降压升压转换器，非常适合于电池供电类产品。数字控制引脚 (CTRL) 允许用数字步长设定负输出电压。TPS65631W 采用创新技术，能够实现出色线路瞬态性能。

器件信息⁽¹⁾

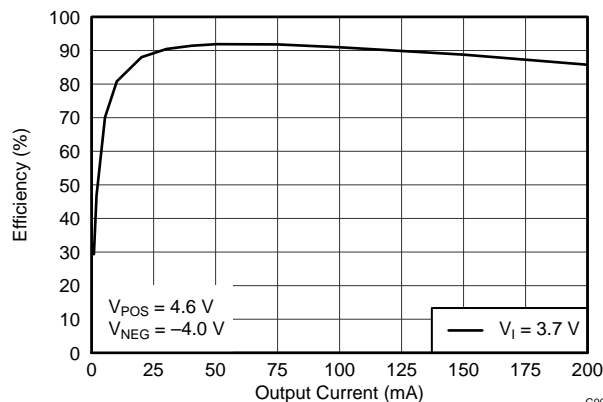
部件号	封装	封装尺寸 (标称值)
TPS65631W	QFN (10)	2.50mm x 2.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



效率与输出电流间的关系



G001



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5 修订历史记录

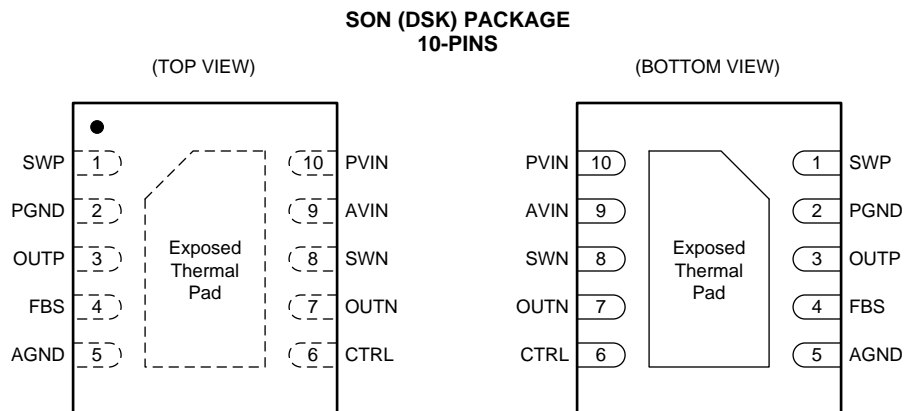
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2013) to Revision A

Page

• 添加了器件信息表和处理额定值表, 特性描述部分, 器件功能模式, 编程部分, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分	1
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6 Pin Configuration and Functions



Pin Functions

NAME	NO.	I/O	DESCRIPTION
AGND	5	—	Analog ground.
AVIN	9	—	Input supply voltage for internal analog circuits (both converters).
CTRL	6	I	Control pin. Combined device enable and inverting buck-boost converter output voltage programming pin.
FBS	4	I	Feedback sense pin of the boost converter output voltage.
PGND	2	—	Power ground of the boost converter.
PVIN	12	—	Input supply voltage pin for the inverting buck-boost converter.
SWN	8	O	Switch pin of the inverting buck-boost converter.
SWP	1	O	Switch pin of the boost converter.
OUTN	7	O	Rectifier pin of the inverting buck-boost converter.
OUTP	3	O	Rectifier pin of the boost converter.
Exposed Thermal Pad	13	—	Connect this pad to AGND and PGND.

7 Specifications

7.1 Absolute Maximum Ratings ⁽¹⁾

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Input voltage ⁽²⁾	SWP, OUTP, FBS, PVIN, AVIN	-0.3	6	V
	OUTN	-0.3	-6	V
	SWN	-6	6	V
	CTRL	-0.3	5.5	V
Operating junction temperature range, T _J		-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) With respect to AGND pin.

7.2 Handling Ratings

		MIN	MAX	UNIT	
T _{STG}	Storage temperature range	-65	150	°C	
V _{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	-2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	-500	500	V
		Machine model (MM) ESD stress voltage	-200	200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process..

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V _I	Input supply voltage range	2.9	3.7	4.5	V
V _O	Output voltage range	V _{POS}	4.6		V
		V _{NEG}	-4.4	-4	
I _O	Output current range	I _{POS}	0		mA
		I _{NEG}	200		
T _A	Operating ambient temperature	-40	25	85	°C
T _J	Operating junction temperature	-40	85	125	

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DSK	UNIT
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	47.1	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	57.8	
R _{θJB}	Junction-to-board thermal resistance	21.1	
ψ _{JT}	Junction-to-top characterization parameter	0.8	
ψ _{JB}	Junction-to-board characterization parameter	21.4	
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	4.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

$V_I = 3.7\text{ V}$, $V_{(CTRL)} = 3.7\text{ V}$, $V_{POS} = 4.6\text{ V}$, $V_{NEG} = -4.0\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_I	Shutdown current into AVIN and PVIN	CTRL pin connected to ground.		0.1		μA
V_{UVLO}	Undervoltage lockout threshold	V_I rising.			2.4	V
		V_I falling.			2.1	
BOOST CONVERTER						
V_O	Output voltage			4.6		V
	Output voltage tolerance	$25^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$, no load	-0.5%		0.5%	
		$-40^\circ\text{C} \leq T_J < 85^\circ\text{C}$, no load	-0.8%		0.8%	
$r_{DS(ON)}$	Switch (low-side) on-resistance	$I_{(SWP)} = 200\text{ mA}$		200		m Ω
	Rectifier (high-side) on-resistance	$I_{(SWP)} = 200\text{ mA}$		350		
	Switching frequency	$I_O = 200\text{ mA}$		1.7		MHz
	Switch current limit	Inductor valley current	0.8	1		A
	Short-circuit threshold voltage in operation	V_O falling		4.1		V
	Short-circuit detection time during operation			3		ms
	Output sense threshold voltage using OUTP	$V_{(OUTP)} - V_{(FBS)}$ increasing		300		mV
	Output sense threshold voltage using FBS	$V_{(OUTP)} - V_{(FBS)}$ decreasing		200		mV
	Input resistance of FBS	Between FBS pin and ground		4		M Ω
	Discharge resistance	CTRL pin connected to ground, $I_O = 1\text{ mA}$		30		Ω
	Line regulation	$I_O = 200\text{ mA}$		0.002		%/V
	Load regulation			0.01		%/A
INVERTING BUCK-BOOST CONVERTER						
V_O	Output voltage default			-4.0		V
	Output voltage range		-4.4		-1.4	
	Output voltage tolerance		-0.05		0.05	
$r_{DS(ON)}$	Switch (high-side) on-resistance	$I_{(SWN)} = 200\text{ mA}$		200		m Ω
	Rectifier (low-side) on-resistance	$I_{(SWN)} = 200\text{ mA}$		300		
	Switching frequency	$I_O = 10\text{ mA}$		1.7		MHz
	Switch current limit	$V_I = 2.9\text{ V}$	1.5	2.2		A
	Short-circuit threshold voltage during operation	Voltage drop from nominal V_O		500		mV
	Short-circuit threshold voltage during start-up		180	200	230	
t_{SCP}	Short-circuit detection time during start-up			10		ms
	Short-circuit detection time during operation			3		ms
	Discharge resistance	CTRL pin connected to ground, $I_O = 1\text{ mA}$		150		Ω
	Line regulation	$I_O = 200\text{ mA}$		0.006		%/V
	Load regulation			0.31		%/A

Electrical Characteristics (continued)

$V_I = 3.7\text{ V}$, $V_{(CTRL)} = 3.7\text{ V}$, $V_{POS} = 4.6\text{ V}$, $V_{NEG} = -4.0\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CTRL						
	High-level threshold voltage				1.2	V
	Low-level threshold voltage		0.4			V
	Pull-down resistance		150	400	860	k Ω
OTHER						
t_{INIT}	Initialization time			300	400	μs
t_{OFF}	Shut-down time		30		80	μs
t_{STORE}	Data storage time		30		80	μs
T_{SD}	Thermal shutdown temperature			145		$^\circ\text{C}$

7.6 Timing Requirements

		MIN	TYP	MAX	UNIT
CTRL Interface					
t_{HIGH}	High-level pulse duration	2	10	25	μs
t_{LOW}	Low-level pulse duration	2	10	25	μs

7.7 Typical Characteristics

At $T_A = 25^\circ\text{C}$, unless otherwise noted.

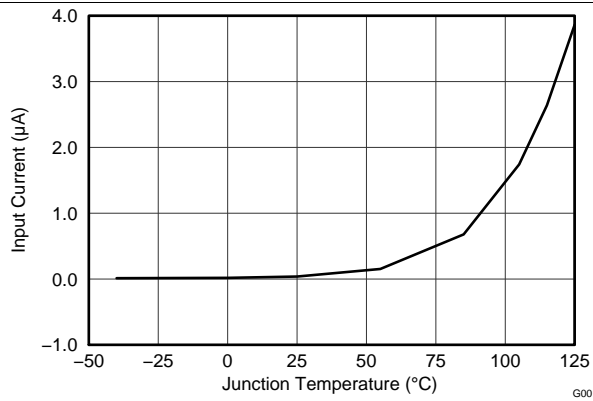


Figure 1. Shutdown Current into AVIN and PVIN

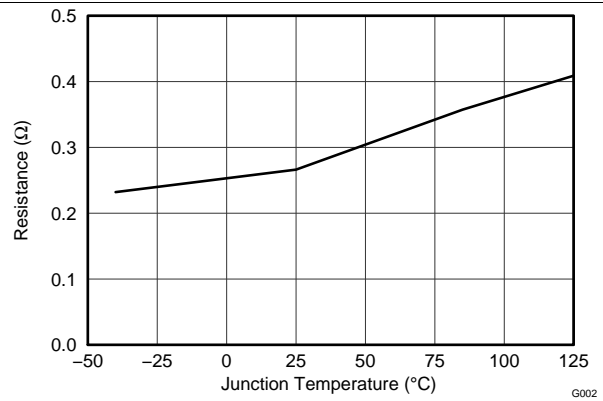


Figure 2. Boost Converter Switch $r_{DS(ON)}$

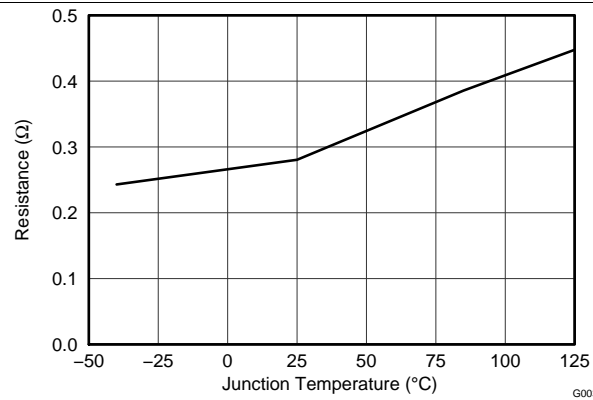


Figure 3. Boost Converter Rectifier $r_{DS(ON)}$

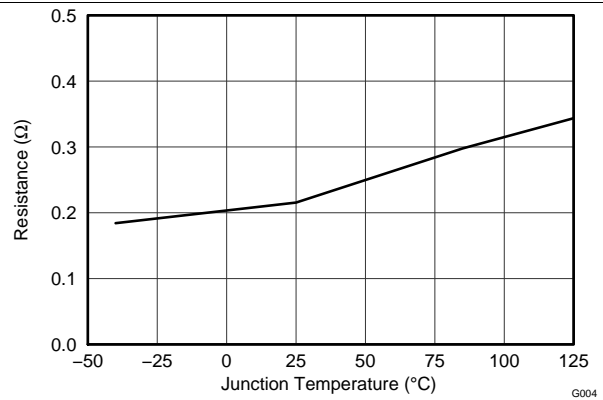


Figure 4. Inverting Buck-Boost Converter Switch $r_{DS(ON)}$

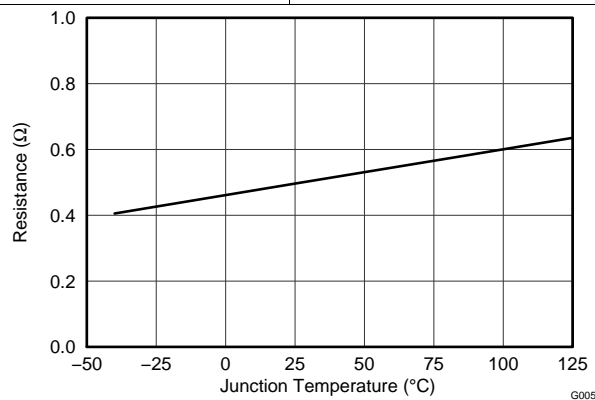


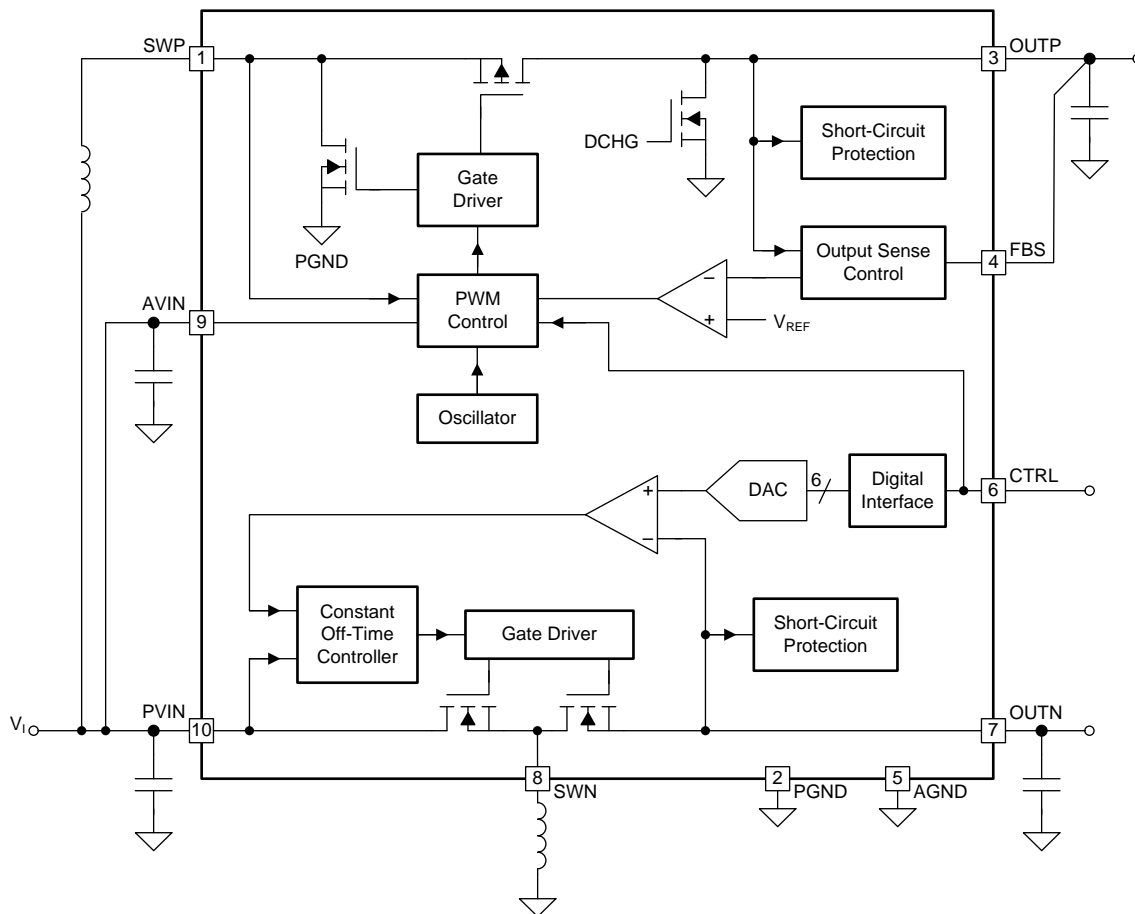
Figure 5. Inverting Buck-Boost Converter Rectifier $r_{DS(ON)}$

8 Detailed Description

8.1 Overview

The TPS65631W consists of a boost converter and an inverting buck boost converter. The V_{POS} output is fixed at 4.6 V and V_{NEG} output is programmable via a digital interface in the range of -1.4 V ~ -4.4 V, the default is -4 V. The transition time of V_{NEG} output is adjustable by the CT pin capacitor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Boost Converter

The boost converter uses a fixed-frequency current-mode topology, and its output voltage (V_{POS}) is fixed at 4.6 V. For the highest output voltage accuracy, connect the output sense pin (FBS) directly to the positive pin of the output capacitor. If not used, the FBS pin can be left floating or connected to ground. If the FBS pin is not used, the boost converter senses its output voltage using the OUTP pin.

8.3.2 Inverting Buck-Boost Converter

The inverting buck-boost converter uses a constant-off-time peak-current mode topology. The converter's default output voltage (V_{NEG}) is -4 V, but it can be programmed to any voltage in the range -1.4 V to -4.4 V (see [Programming \$V_{NEG}\$](#)).

Feature Description (continued)

8.3.3 Soft-Start and Start-Up Sequence

The TPS65631W features a soft-start function to limit inrush current. When the device is enabled by a high-level signal applied to the CTRL pin, the boost converter starts switching with a reduced switch current limit. Ten milliseconds after the CTRL pin goes high, the inverting buck-boost converter starts with a default value of -4 V. A typical start-up sequence is shown in Figure 6.

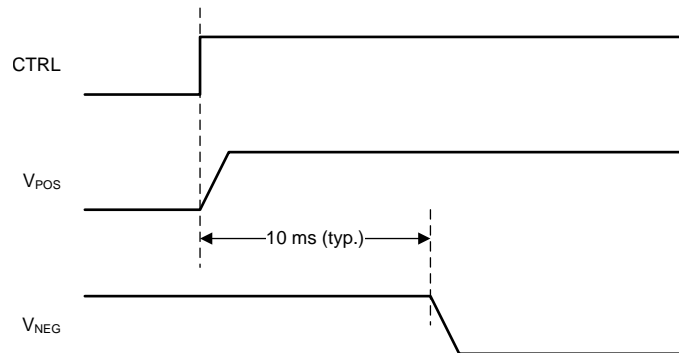


Figure 6. Typical Start-Up Sequence

8.3.4 Enable (CTRL)

The CTRL pin serves two functions. One is to enable and disable the device, and the other is to program the output voltage (V_{NEG}) of the inverting buck-boost converter (see [Programming \$V_{NEG}\$](#)). If the digital interface is not required, the CTRL pin can be used as a standard enable pin for the device, which will come up with its default value on V_{NEG} of -4 V. When CTRL is pulled high, the device is enabled. The device is shut down with CTRL low.

8.3.5 Undervoltage Lockout

The TPS65631W features an undervoltage lockout function that disables the device when the input supply voltage is too low for normal operation.

8.3.6 Short Circuit Protection

The TPS65631W is protected against short-circuits of V_{POS} and V_{NEG} to ground and to each other.

8.3.6.1 Short-Circuits During Normal Operation

During normal operation an error condition is detected if V_{POS} falls below 4.1 V for more than 3 ms or V_{NEG} is pulled above the programmed nominal output by 500 mV for longer than 3 ms. In either case the device enters shutdown mode: the converters are disabled and their outputs are disconnected from the input. To resume normal operation either cycle the input supply voltage or toggle the CTRL pin low and then high again.

8.3.6.2 Short-Circuits During Start-Up

During start up an error condition is detected if:

- V_{POS} is not in regulation 10 ms after a high-level is applied to the CTRL pin.
- V_{NEG} is higher than threshold level 10 ms after a high-level is applied to the CTRL pin.
- V_{NEG} is not in regulation 20 ms after a high-level is applied to the CTRL pin.

To resume normal operation either cycle the input supply voltage or toggle the CTRL pin low and then high again.

8.3.7 Output Discharge During Shutdown

The TPS65631W actively discharges its outputs during shutdown. [Figure 7](#) shows the output discharge control.

Feature Description (continued)

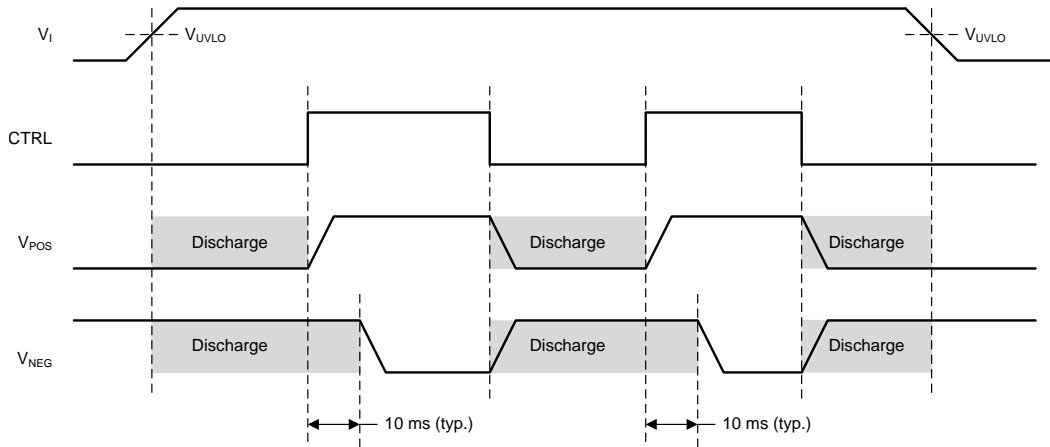


Figure 7. Active Discharge of V_{POS} and V_{NEG} During Shutdown

8.3.8 Thermal Shutdown

The TPS65631W enters thermal shutdown mode if its junction temperature exceeds 145°C (typical). During thermal shutdown mode none of the device functions are available. To resume normal operation, either cycle the input supply voltage or toggle the CTRL pin low and then high again.

8.4 Device Functional Modes

8.4.1 Operation with $V_I < 2.9\text{ V}$

The recommended minimum input supply voltage for full performance is 2.9 V. The device continues to operate with input supply voltages below 2.9 V; however, full performance is not guaranteed. The device does not operate with input supply voltages below the UVLO threshold.

8.4.2 Operation with $V_I \approx V_{POS}$ (Diode Mode)

The TPS65631W features a "diode" mode that enables it to regulate its output voltage even when the input supply voltage is close to V_{POS} (that is, too high for normal boost operation). When operating in diode mode the converter's high-side switch stops switching and its body diode is used as the rectifier. Boost converter efficiency is reduced when operating in diode mode. At low output currents ($\approx 2\text{ mA}$ and below), the boost converter automatically transitions from pulse-width modulation to pulse-skip mode. This ensures that V_{POS} stays in regulation but increases the output voltage ripple on V_{POS} .

8.4.3 Operation with CTRL

When a low-level signal is applied to the CTRL pin the device is disabled and switching is inhibited. When the input supply voltage is above the UVLO threshold and a high-level signal is applied to the CTRL pin the device is enabled and its start-up sequence begins.

8.5 Programming

8.5.1 Programming V_{NEG}

The output voltage of the inverting buck-boost converter (V_{NEG}) can be programmed using the CTRL pin. If output voltage programming is not required, the CTRL pin can be used as a standard enable pin (see [Enable \(CTRL\)](#)).

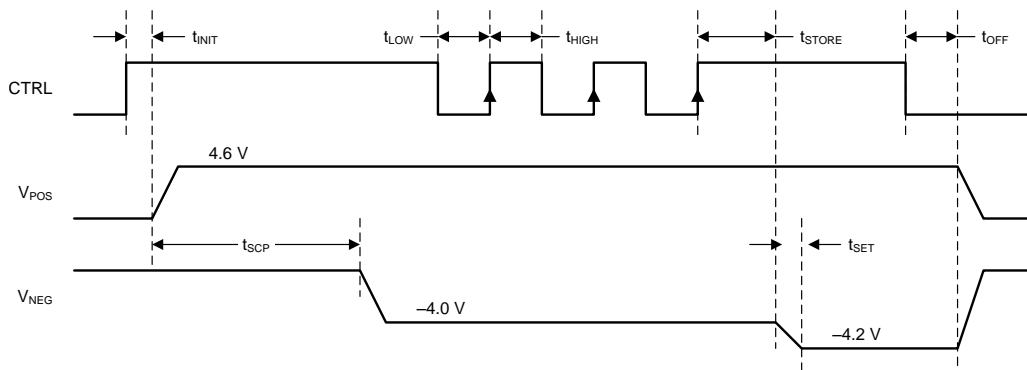


Figure 8. Programming V_{NEG} Using the CTRL Pin

When the CTRL pin is pulled high, the inverting buck-boost converter starts up with its default voltage of $-4V$. The device now counts the rising edges applied to the CTRL pin and sets the output voltage (V_{NEG}) according to [Table 1](#). For the timing diagram shown in [Figure 8](#), V_{NEG} is programmed to $-4.2V$, since three rising edges are detected.

The CTRL interface is designed to work with pulses whose duration is between $2\mu s$ and $25\mu s$. Pulses shorter than $2\mu s$ or longer than $25\mu s$ are not ensured to be recognized.

Table 1. Programming Table for V_{NEG}

Number of Rising Edges	V_{NEG}	Number of Rising Edges	V_{NEG}
0 / no pulses	$-4V$	16	$-2.9V$
1	$-4.4V$	17	$-2.8V$
2	$-4.3V$	18	$-2.7V$
3	$-4.2V$	19	$-2.6V$
4	$-4.1V$	20	$-2.5V$
5	$-4.0V$	21	$-2.4V$
6	$-3.9V$	22	$-2.3V$
7	$-3.8V$	23	$-2.2V$
8	$-3.7V$	24	$-2.1V$
9	$-3.6V$	25	$-2.0V$
10	$-3.5V$	26	$-1.9V$
11	$-3.4V$	27	$-1.8V$
12	$-3.3V$	28	$-1.7V$
13	$-3.2V$	29	$-1.6V$
14	$-3.1V$	30	$-1.5V$
15	$-3.0V$	31	$-1.4V$

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 9 shows a typical application circuit suitable for supplying AMOLED displays in smartphone applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates a positive output voltage V_{POS} of 4.6 V and a negative output voltage of -4 V. Both outputs are capable of supplying up to 300 mA of output current.

9.2 Typical Application

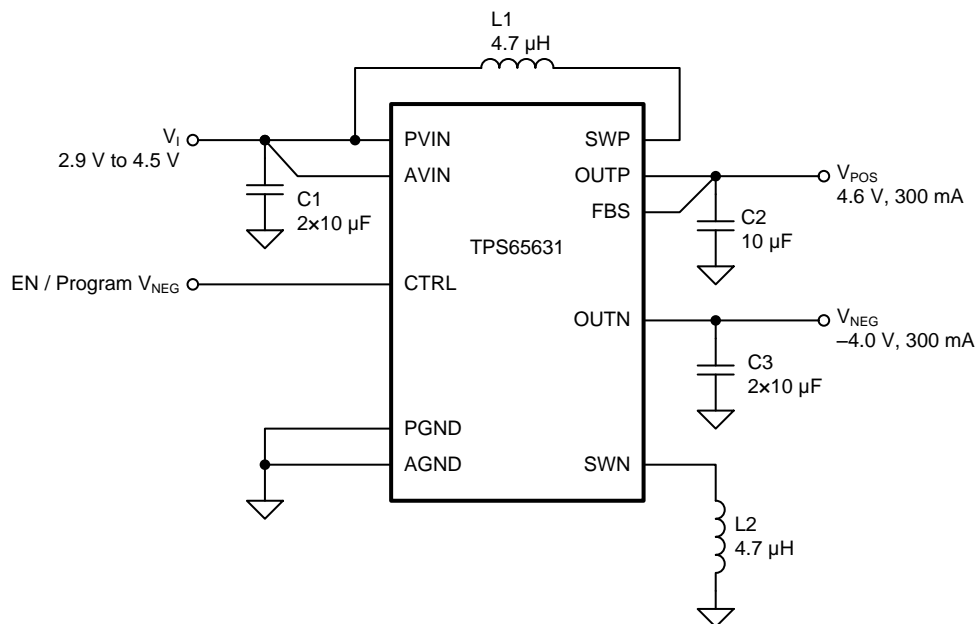


Figure 9. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the following input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE
Input voltage range	2.9 V to 4.5 V
Output voltage	$V_{POS} = 4.6\text{V}$, $V_{NEG} = -4\text{V}$

9.2.2 Detailed Design Procedure

In order to maximize performance, the TPS65631W has been optimized for use with a relatively narrow range of component values, and customers are strongly recommended to use the application circuit shown in Figure 9 with the components listed in Table 3 and Table 4.

9.2.2.1 Inductor Selection

The boost converter and inverting buck-boost converter have been optimized for use with 10 μH inductors, and it is recommended that this value be used in all applications. Customers using other values of inductor are strongly recommended to characterize circuit performance on a case-by-case basis.

Table 3. Inductor Selection⁽¹⁾

PARAMETER	VALUE	MANUFACTURER	PART NUMBER
L1, L2	10 μH	Toko	DFE252012C-100M
		ABCO	LPP252012-100M
		Taiyo Yuden	MDKK2020T-100M

(1) See [Third-Party Products Disclaimer](#)

9.2.2.2 Capacitor Selection

The recommended capacitor values are shown in [Table 4](#). Applications using less than the recommended capacitance (e.g. to save PCB area) may experience increased voltage ripple. In general, the lower the output power, the lower the necessary capacitance.

Table 4. Capacitor Selection⁽¹⁾

PARAMETER	VALUE	MANUFACTURER	PART NUMBER
C1	2 × 10 μF	Murata	GRM21BR71A106KE51
C2	10 μF	Murata	GRM21BR71A106KE51
C3	2 × 10 μF	Murata	GRM21BR71A106KE51
C4	100 nF	Murata	GRM21BR71E104KA01

(1) See [Third-Party Products Disclaimer](#)

9.2.2.3 Stability

Applications using component values that differ significantly from those recommended in [Table 3](#) and [Table 4](#) should be checked for stability over the full range of operating conditions.

9.2.3 Application Curves

The performance shown in the following graphs was obtained using the circuit shown in Figure 9 and the external components shown in Table 3 and Table 4. The output voltage settings for these measurements were $V_{POS} = 4.6\text{ V}$ and $V_{NEG} = -4\text{ V}$.

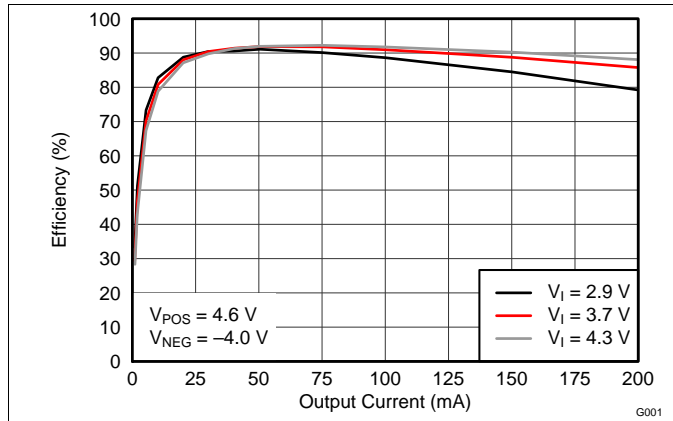


Figure 10. Efficiency vs. Output Current

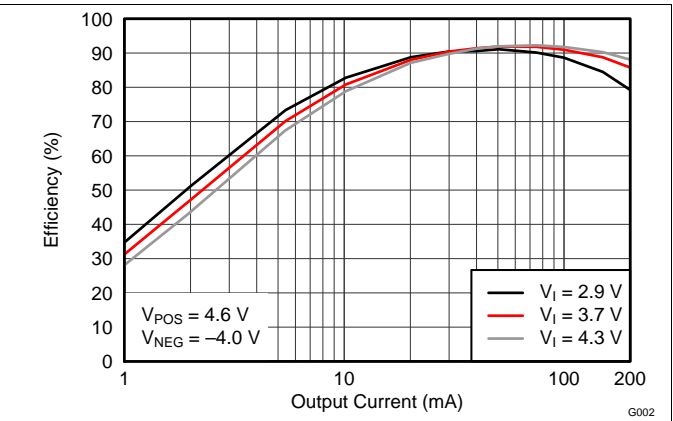


Figure 11. Efficiency vs. Output Current (Log Scale)

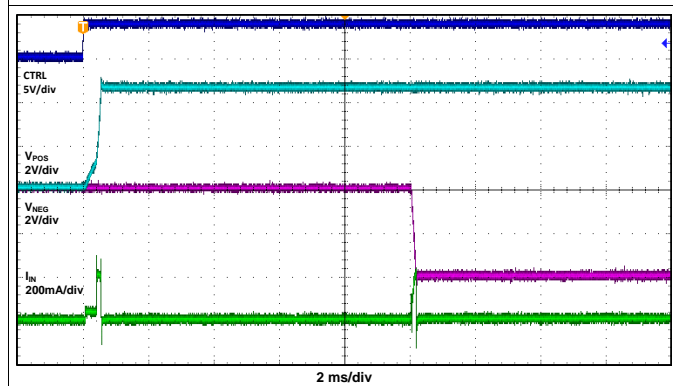


Figure 12. Start-Up Waveforms

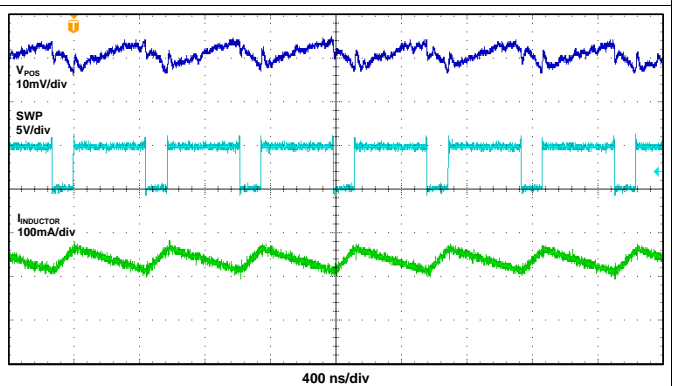


Figure 13. V_{POS} Switch Voltage, Inductor Current and Output Voltage Ripple ($I_O = 100\text{ mA}$)

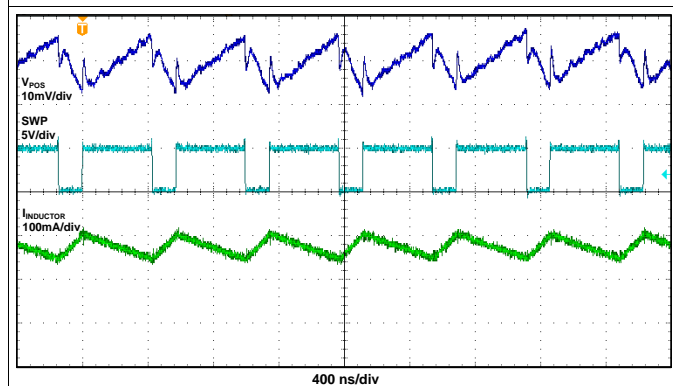


Figure 14. V_{POS} Switch Voltage, Inductor Current and Output Voltage Ripple ($I_O = 200\text{ mA}$)

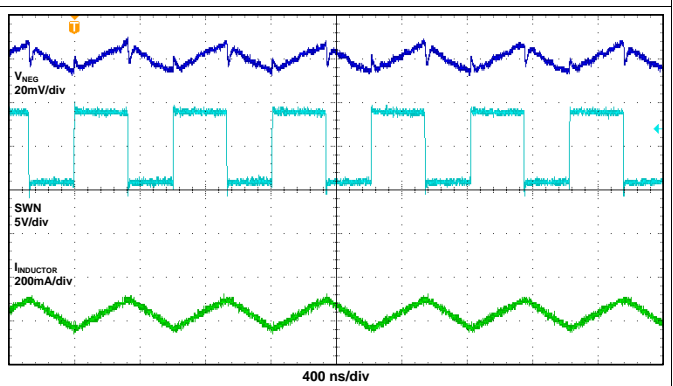


Figure 15. V_{NEG} Switch Voltage, Inductor Current and Output Voltage Ripple ($I_O = 100\text{ mA}$)

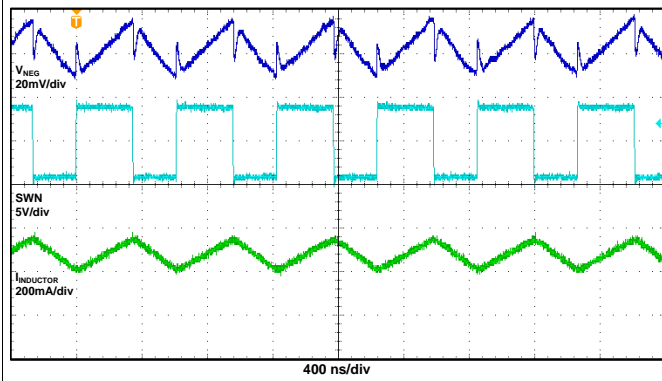


Figure 16. V_{NEG} Switch Voltage, Inductor Current and Output Voltage Ripple ($I_O = 200$ mA)

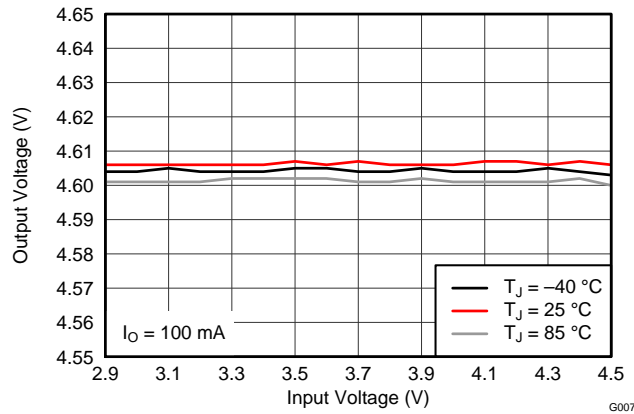


Figure 17. Boost Converter Line Regulation

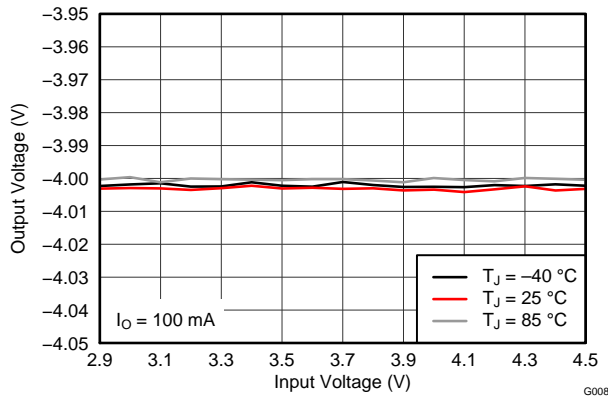


Figure 18. Inverting Buck-Boost Converter Line Regulation

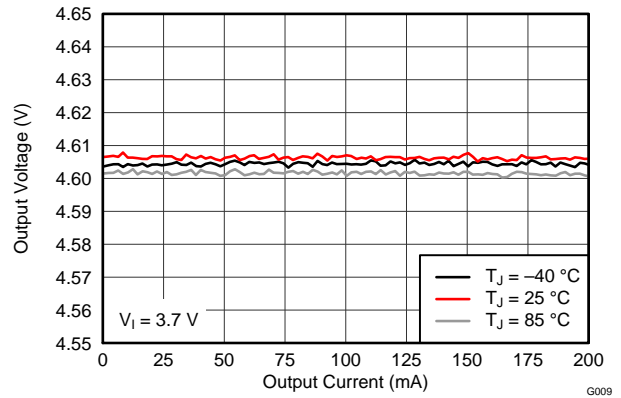


Figure 19. Boost Converter Load Regulation

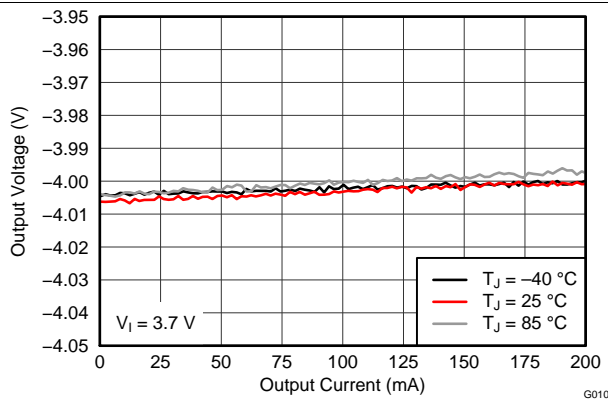


Figure 20. Inverting Buck-Boost Converter Load Regulation

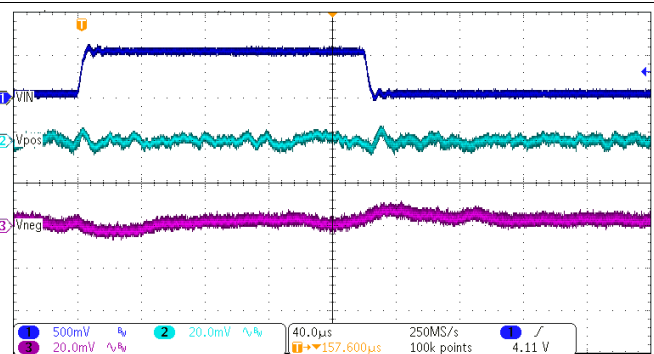
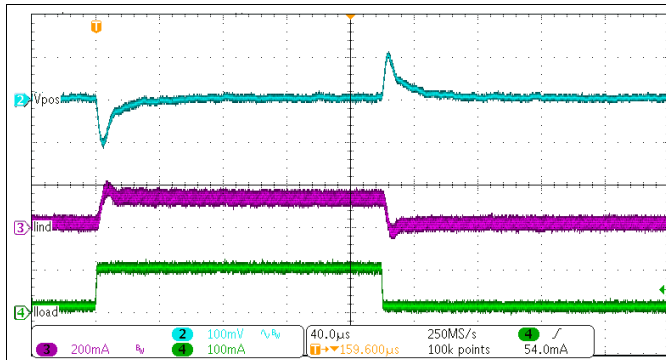
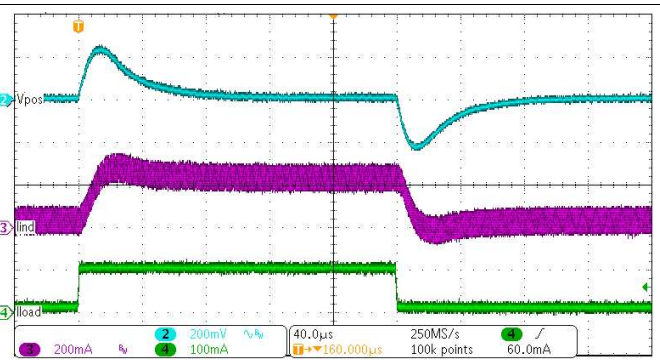


Figure 21. Line Transient Response


Figure 22. Boost Converter Load Transient Response

Figure 23. Inverting Buck-Boost Converter Load Transient Response

10 Power Supply Recommendations

The TPS65631W is designed to operate from an input voltage supply range between 2.9 V and 4.5 V. If the input supply is located more than a few centimeters from the TPS65631W additional bulk capacitance may be required. The 2x10 μF shown in the schematics in this data sheet are a typical choice for this function.

11 Layout

11.1 Layout Guidelines

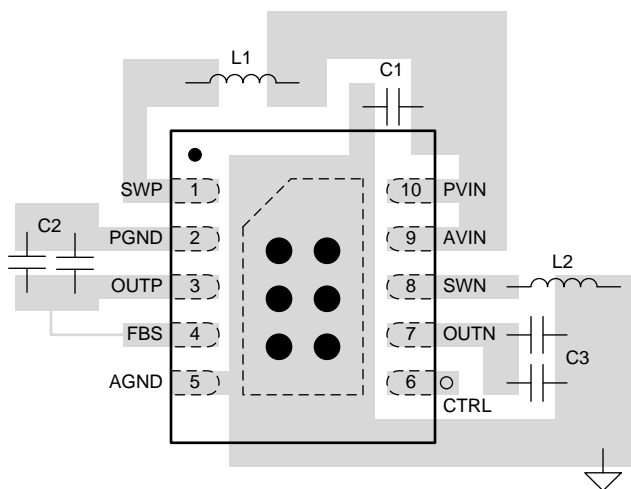
No PCB layout is perfect and compromises are always necessary. However, following the basic principles listed below (in order of importance) should go a long way to achieving good performance:

- Route switching currents on the top layer using short, wide traces. Do not route these signals through vias, which have relatively high parasitic inductance and resistance.
- Use a copper pour on layer 2 as a ground plane and thermal spreader, and connect the thermal pad to it using a number of thermal vias.
- Place C1 as close as possible to pin 10.
- Place C2 as close as possible to pins 2 and 3.
- Place C3 as close as possible to pin 7.
- Place L1 as close as possible to pin 1.
- Place L2 as close as possible to pin 10.
- Use the thermal pad to join AGND and PGND.
- Connect the FBS pin directly to the positive pin of C2, that is, keep this connection separate from the connection between OUTP and C2.

Figure 24 illustrates how a PCB layout following the above principles may be realized in practice.

11.2 Layout Example

Figure 24 shows the above principles implemented for the circuit of Figure 9.



- Via to signal layer on internal or bottom layer.
- Thermal via to copper pour on internal or bottom layer.

Figure 24. PCB Layout Example

12 器件和文档支持

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12.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 5. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
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12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

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DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65631WDSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SJN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65631WDSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65631WDSKR	SON	DSK	10	3000	182.0	182.0	20.0

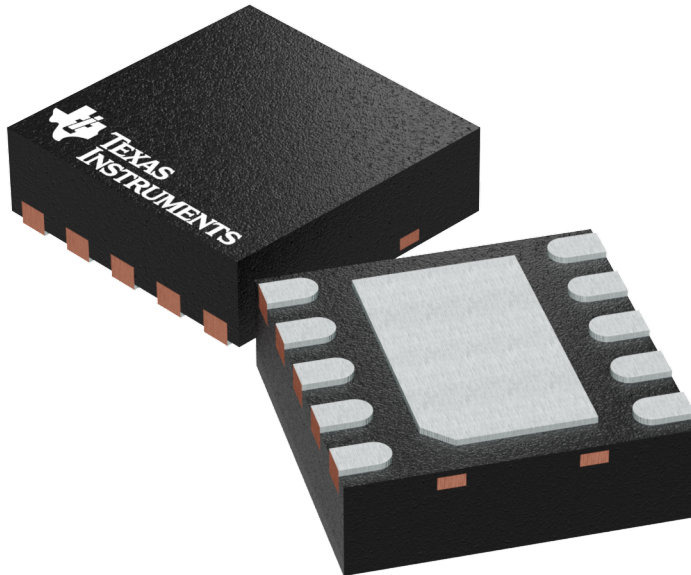
GENERIC PACKAGE VIEW

DSK 10

WSON - 0.8 mm max height

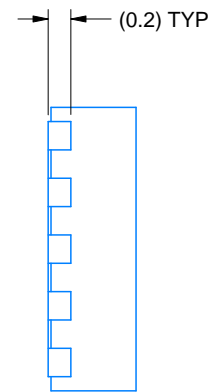
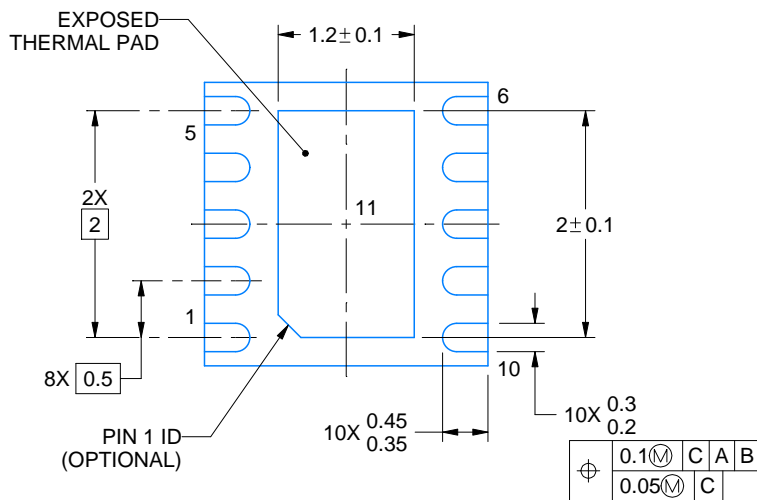
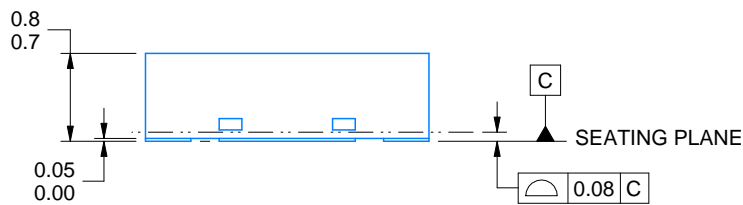
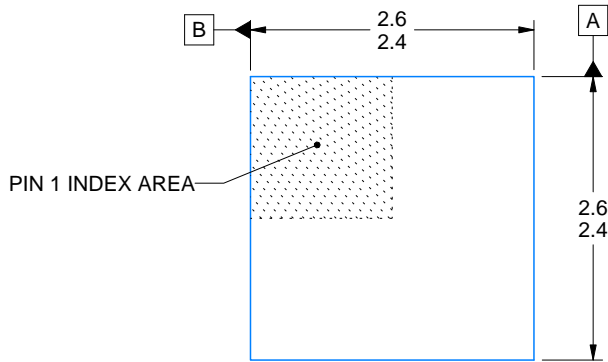
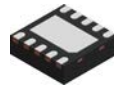
2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225304/A



4218903/B 10/2020

NOTES:

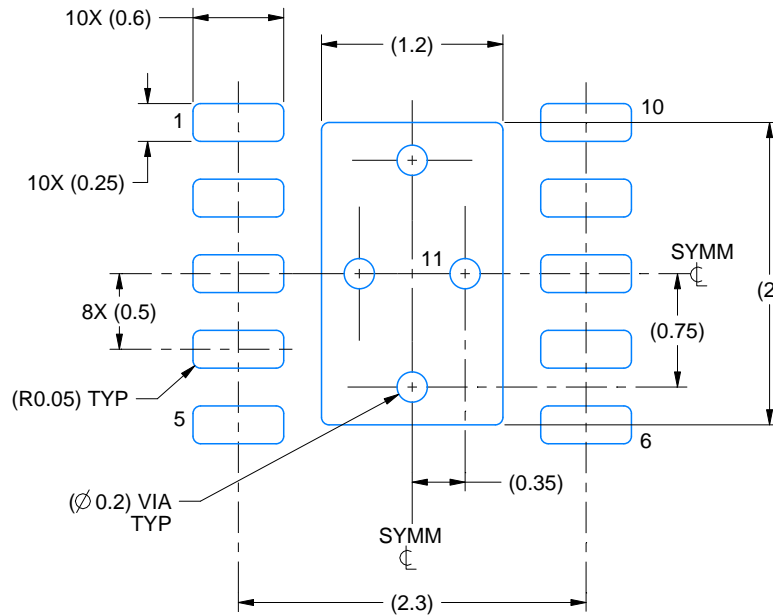
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

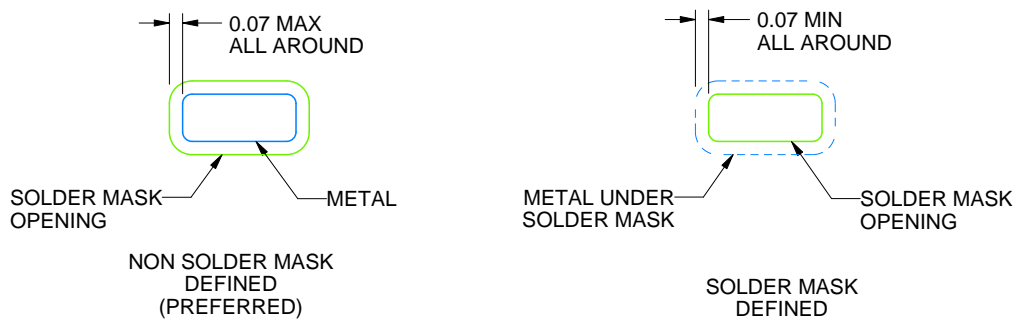
DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

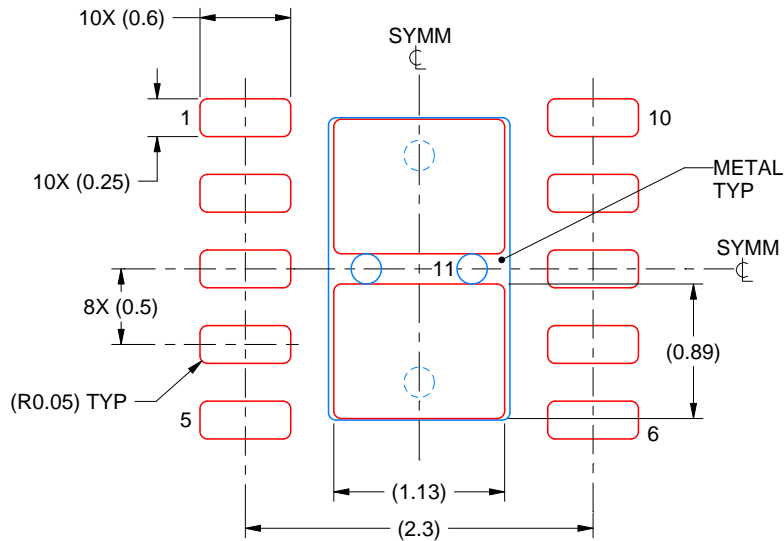
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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