LCD Bias With Digital VCOM Buffer for Notebook PCs and Tablet PCs

Check for Samples: TPS65640

FEATURES

- **2.5-V to 5.5-V Input Voltage Range**
- **3.6 to 12.7 V Boost Converter (AV_{DD})**
- **15 to 37 V Boost Converter with Temperature Compensation (V_{GH})**
- **–8 V to –3.8 V Linear Negative Voltage Regulator (V_{GL} or NAV_{DD})**
- **1.5-V to 3-V Alternative Buck Converter or Low Dropout Regulator (V_{25})**
- **7 bits Programmable V_{COM} Calibrator With One Integrated Buffer Amplifiers**
- **0.8 V to 5.1 V Programmable V_{COM} Voltage Output for Full AV_{DD} Application**
- **–4.1 V to 0.2 V Programmable V_{COM} Voltage Output for Positive and Negative AV_{DD} Application**
- **Two Operational Amplifiers**
- **Gate Voltage Shaping**
- **Programmable V_{GH} and V_{COM} Temperature Compensation**
- **T_{CON} Reset Signal Generator With Programmable Delay**
- **I^2C Interface for E^2PROM Programming**
- **Thermal Shutdown**
- **Supports GIP and Non-GIP Displays**
- **28 Pins, 5.5-mm × 3.5-mm 0.5-mm Pitch QFN**

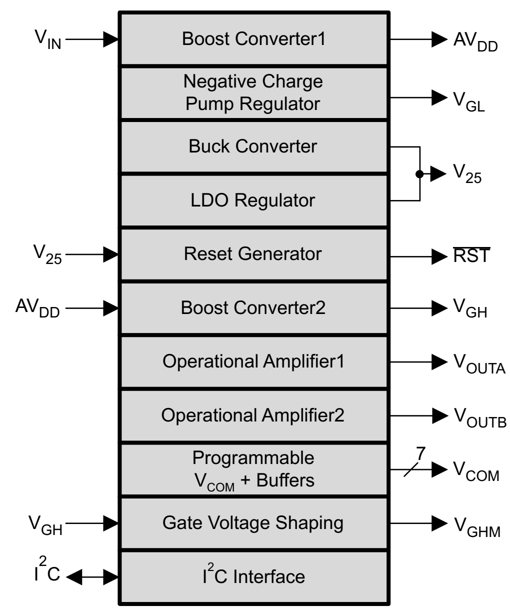
APPLICATIONS

- **Notebook PCs**
- **Tablet PCs**

DESCRIPTION

The TPS65640 is a compact LCD bias solution primarily intended for use in notebook and tablet PCs. The device comprises two boost converters to supply the LCD panel's source driver and gate driver or level shifter; one buck converters or a LDO regulator alternatively to supply the time controller logic voltages; a linear negative voltage regulator to supply gate off voltage or provide negative voltage for source driver; a programmable VCOM generator with one high-speed amplifier; a gate voltage shaping function and two high speed operational amplifiers.

All the regulators and V_{COM} voltage outputs are programmed through I^2C interface and stored in the TPS65640 integrated E^2PROM. The TPS65640 is available in 5.5-mm × 3.5-mm, 28-lead QFN package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65640	5.5-mm x 3.5-mm 28-pin QFN	PZXI

(1) The device is supplied taped and reeled, with 3000 devices per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Pin Voltage(2)	VIN, V25, V25_LX, $\overline{\text{RESET}}$, COMP, SCL, SDA, VFLK, VT	–0.3	7	V
	VIN (100ms) Pulse	–0.3	12	V
	AVDD, LX	–0.3	20	V
	VCOM_OUT, INA+, INA–, OUTA, INB+, INB–, OUTB	–5	5	V
	VGH_LX, VGH, VGHM, RE	–0.3	40	V
	DRVN, VGL, NAVDD	–12	0.3	V
ESD Rating(3)	Human Body Model		2000	V
	Machine Model		200	V
	Charged Device Model		700	V
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65640	UNITS
		RHR	
		28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	26.3	
θ_{JB}	Junction-to-board thermal resistance(4)	8.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	8.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.5		5.5	V
BOOST CONVERTER 1					
AV_{DD}	Boost converter 1 output voltage range	3.6		11	V
I_{AVDD}	Boost converter 1 output current when 5.5 V ≥ VIN ≥ 2.5 V			400	mA
L_1	Boost converter #1 inductor range	4.7		10	µH
C_{OUT1}	Boost converter #1 output capacitance	10			µF
BOOST CONVERTER 2					
AV_{DD}	Input voltage range	3.6		11 (1)	V
V_{GH}	Output voltage range	15		37	V
I_{GH}	Output current		15	40	mA
L_4	Inductor	4.7	10	10	µH
C_{OUT4}	Output capacitance	1	2.2		µF
R_{NTC}	Thermistor resistance at 25 °C		10		kΩ
BUCK CONVERTER (V_{25})					
V_{25}	Output voltage	1.5		3	V
I_{25}	Output current			600	mA
L_2	Inductor	2.2	4.7	10	µH
C_{OUT2}	Output capacitance	4.7	10	22	µF
LDO Regulator (V_{25})					
V_{25}	Output voltage	1.5		3	V
I_{25}	Output current			350	mA
C_{OUT2}	Output capacitance	1	4.7		µF

(1) $V_{GH} – AV_{DD}$ must be greater than 6 volts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.3 V; V_{25} = 2.5 V, AV_{DD} = 8.5 V, V_{GH} = 23 V, V_{GL} = –6 V, R_{CAMP}=200kΩ, C_{CAMP}=1 nF, NAV_{DD} = AGND = PGND = 0V, T_A = –40 °C to 85 °C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{IN}	Supply current into VIN	Converters not switching		2	3	mA
	Supply current into AVDD	No load on op-amp outputs		5	8.5	mA
	Supply current into VGH	No load on V_{GHM}		0.1	1	mA
UNDER VOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.3	2.35	2.4	V
		V_{IN} falling T_A = 25°C	2.05	2.2	2.25	
	Hysteresis	V_{IN} rising – V_{IN} falling		0.15		
BOOST CONVERTER 1 (AV_{DD})						
AV_{DD}	Output voltage range		3.6		11	V
	Tolerance		–2%		2%	
V_{UVP1}	Undervoltage threshold	AV_{DD} falling	75	80	85	% of AV_{DD}
T_{DLY_UVP1}				160		ms
V_{SCP1}	Short circuit threshold	AV_{DD} falling	25	30	35	%
V_{OVP1}	Over Voltage threshold	AV_{DD} rising	14.5	15	16	V
I_{LK1}	Switch leakage current	AV_{DD} = 13.5 V		10	20	µA
$r_{DS(ON)1}$	Switch ON resistance	I_{LX} = 1 A		0.2	0.3	Ω
I_{LIM1}	AVDD switch current limit	**AVDD ILIM** = 0, T_A = 25 °C	0.8	1	1.2	A
		AVDD ILIM = 1, T_A = 25 °C	1.6	2	2.4	

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.3 V; V_{25} = 2.5 V, AV_{DD} = 8.5 V, V_{GH} = 23 V, V_{GL} = –6 V, R_{CAMP}=200kΩ, C_{CAMP}=1 nF, NAV_{DD} = AGND = PGND = 0V, T_A = –40 °C to 85 °C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_{MAX1}	Maximum Duty Cycle	**FREQ1** = 01	80%			
f_{SW1}	Oscillator frequency	**FREQ1** = 00, T_A = 25°C	480	600	720	kHz
		FREQ1 = 01, T_A = 25°C	600	750	900	
		FREQ1 = 10, T_A = 25°C	720	900	1080	
		FREQ1 = 11, T_A = 25°C	800	1000	1200	
V_{LIR1}	Line regulation, $V_{LIR}=\Delta AV_{DD}/(AV_{DD}\times\Delta V_{IN})$	V_{IN} = 2.5 V to 5.5 V, A_{VDD} = 8.5 V, T_A = 25 °C		±0.1	±0.15	%/V
V_{LOR1}	Load regulation, $V_{LOR}=(AV_{DD\_20mA}–AV_{DD\_200mA})/AV_{DD\_20mA}$	V_{IN} = 3.3 V, AV_{DD} = 8.5 V, I_{AVDD} = 20 mA to 200 mA		1		%/A
V_{SS1}	AV_{DD} soft stat duration	**SS1** = 00		20		ms
		SS1 = 01		40		
		SS1 = 10		60		
		SS1 = 11		80		
T_{f1}	AV_{DD} switch ON voltage slew rate	**LX1TS** = 00		0.5		V/ns
		LX1TS = 01		0.7		
		LX1TS = 10		0.9		
		LX1TS = 11		1.1		
BUCK CONVERTER (V_{25Buck})						
V_{25Buck}	Output voltage		1.5		3	V
	Tolerance	$(V_{25}-V_{25\_setting})/V_{25\_seeting}$	–2%		2%	
V_{UVP2}	Undervoltage threshold	V_{25} falling	0.8	1	1.2	V
	Hysteresis	V_{25} rising		0.1		
T_{DLY_UVP2}				160		ms
I_{LIM2}	Switch current limit	I_{SW2A} ramps from 0 A to 2 A	1	1.2	1.4	A
T_{SS2}	Soft start duration			4		ms
$r_{DS(ON)2A}$	Switch ON resistance	High-side, I_{SW2A} = I_{LIM2}		250	450	mΩ
$r_{DS(ON)2B}$		Low-side, I_{SW2B} = 1 A		100	200	
f_{SW2}	Switching frequency	V_{IN} = 3.3 V; V_{25} = 2.5 V, I_{25} = 200 mA	1000	1250	1500	kHz
V_{LIR2}	Line regulation, $V_{LIR} = \Delta V_{25} / (AV_{25}\times\Delta V_{IN})$	V_{IN} = 2.5 V to 5.5 V		±0.1	±0.15	%/V
V_{LOR2}	Load regulation	V_{IN} = 3.3 V, I_{25} = 1 mA to 400 mA		1%		
LINEAR REGULATOR (V_{25LDO})						
V_{25LDO}	Output voltage		1.5		3.0	V
	Tolerance		–2.5%		2.5%	
V_{UVP3}	Undervoltage threshold	V25 falling	0.8	1	1.2	V
	Hysteresis	V25 rising		0.1		
T_{DLY_UVP3}				160		ms
V_{DO3}	Dropout voltage	I_{25} = 350 mA, V_{25} = –3%		300	500	mV
V_{LIR3}	Line regulation, $V_{LIR} = \Delta V_{25} / (V_{25}\times\Delta V_{IN})$	V_{IN} = 2.8 V to 5.5 V, I_{25} = 100 mA		0.1	±0.15	%/V
V_{LOR3}	Load regulation	V_{IN} = 3.3 V, I_{25} = 1 mA to 300 mA		1		%/A
BOOST CONVERTER 2 (V_{GH})						
V_{GH}	Output voltage range		15		37	V
	Tolerance		–3%		3%	
V_{OVP4}	Overvoltage threshold	T_A = 25 °C	38	39	40	V
V_{UVP4}	Undervoltage threshold	V_{GH} falling	75	80	85	% of V_{GH}
T_{DLY_UVP4}	Undervoltage protection shutdown delay			160		ms
I_{LK4}	Switch leakage current	Switching off V_{VGH_LX} = 38 V		10	20	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.3 V; V_{25} = 2.5 V, AV_{DD} = 8.5 V, V_{GH} = 23 V, V_{GL} = –6 V, R_{CAMP}=200kΩ, C_{CAMP}=1 nF, NAV_{DD} = AGND = PGND = 0V, T_A = –40 °C to 85 °C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW4}	VGH swithching frequency	**FREQ4** = 0	300	400	500	kHz
		FREQ4 = 1	600	800	1000	
$r_{DS(ON)4}$	VGH switch ON resistance	I_{VGH_LX} = 1 A		0.5	1	Ω
I_{LIM4}	VGH switch current limit		0.9	1.2	1.5	A
T_{SS4}	VGH soft start duration	**SS4** = 00		4		ms
		SS4 = 01		8		
		SS4 = 10		12		
		SS4 = 11		16		
D_{MAX4}			88%	90%		
I_{VT}	Thermistor reference current	V_{VT} = 1 V		40		µA
V_{LIR4}	Line regulation	AV_{DD} = 3.6 V to 11 V		±0.1	±0.15	%/V
V_{LOR4}	Load regulation	I_{GH} = 5 mA to 40 mA		1		%/A
PROGRAMMABLE V_{COM} CALIBRATOR						
$V_{S+} – V_{S–}$	VCOM buffer supply voltage				15	V
V_{COM}	V_{COM} voltage accuracy, V_{COM}–$V_{COM\_setting}$	I_{OUT} = 0 mA	–6		6	LSB
	Load regulation	AV_{DD} = 8.5 V, NAV_{DD} = 0 V, V_{COM_OUT} = AV_{DD} / 2, I_{SOURCE} = 1mA to 20mA		1	2	V/A
		AV_{DD} = 5 V, NAV_{DD} = –5 V, V_{COM_OUT} = 0 V, I_{SOURCE} = 1 mA to 20 mA		1	2	
		AV_{DD} = 8.5 V, NAV_{DD} = 0 V, V_{COM_OUT} = AV_{DD} / 2, I_{SINK} = –1 mA to –20 mA		1	2	
		AV_{DD} = 5 V, NAV_{DD} = –5 V, V_{COM_OUT} = 0 V, I_{SINK} = –1 mA to –20 mA		1	2	
I_{SC2}	Short circuit current	AV_{DD} = 5 V, V_{COM_OUT} = AVDD, NAV_{DD} = –5 V		–200		mA
		AV_{DD} = 5 V, V_{COM_OUT} = NAV_{DD} = –5 V		200		
SR_2	Slew rate	V_{COM_OUT} = AV_{DD} / 2 + 1 V		12		V/µs
BW_2	Small signal 3dB bandwidth	V_{COM_OUT} = AV_{DD} / 2, V_{SIGNAL} = 60 mV_{PP}, no load		12		MHz
OPERATIONAL AMPLIFIER 1 and 2 (AV_{DD} = 5 V, NAV_{DD} = –5 V, R_L = 10 kΩ, C_L = 10 pF, T_A = 25°C)						
V_{IO1}	Input offset voltage	V_{CM} = (AV_{DD} + NAV_{DD}) / 2	–15		15	mV
$ΔV_{IO}/Δ_T$	Average offset voltage drift	T_A = –40°C to 85°C		5		µV/°C
R_{IN1}	Input impedance			1		GΩ
C_{IN1}	Input capacitance			1.35		pF
V_{CM1}	Input common mode voltage range	AV_{DD} = 5 V, NAV_{DD} = –5 V	–4		3	V
A_{VOL1}	Open loop gain	V_{CM} = (AV_{DD} + NAV_{DD}) / 2	75	95		dB
$PSRR_1$	Power supply rejection ratio	V_{CM} = (AV_{DD} + NAV_{DD}) / 2	60	70		dB
$CMRR_1$	Common mode rejection ration	V_{CM} = (AV_{DD} + NAV_{DD}) / 2	50	80		dB
V_{OL1}	Output swing low	I_L = 5 mA		4.85	4.92	V
V_{OH1}	Output swing High	I_L = –5 mA	–4.92	–485		V
I_{OC1}	Continuous output current			±35		mA
I_{PK1}	Peak output current	V_{IN+} = (AV_{DD} + NAV_{DD}) / 2, $V_{IN–}$ = (AV_{DD} + NAV_{DD}) / 2 ±1 V, open-loop	±120			mA
tS	Setting to ±0.1%	A_V = –1, $V_{IN–}$ = (AV_{DD} + NAV_{DD}) / 2 ±1 V		500		ns
SR_1	Slew rate	A_V = –1, $V_{IN–}$ = (AV_{DD} + NAV_{DD}) / 2 ±1 V		12		V/µs
BW_1	Small signal 3 dB bandwidth	A_V = –1, V_{CM} = (AV_{DD} + NAV_{DD}) / 2, V_{SIGNAL} = 60 mV_{PP}		5		MHz
PM	Phase margin			50		Degree
CS	Channel Separation	A_V = –1, V_{CM} = (AV_{DD} + NAV_{DD}) / 2, V_{SIGNAL} = 60 mV_{PP}, f = 5 MHz		75		dB
GATE OFF REGULATION CONTROLLER (V_{GL})						

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.3 V; V_{25} = 2.5 V, AV_{DD} = 8.5 V, V_{GH} = 23 V, V_{GL} = –6 V, R_{CAMP}=200kΩ, C_{CAMP}=1 nF, NAV_{DD} = AGND = PGND = 0V, T_A = –40 °C to 85 °C. Typical values are at 25°C (unless noted otherwise).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GL}	V_{GL} voltage regulate accuracy	Output voltage	–3.8		-8	V
		Tolerance	–3%		3%	
I_{DRVN}	DRVN source current		1	4	6	mA
V_{LIR5}	Line regulation	I_{DRVN} = 1 mA, V_{IN} = 2.5 V to 5.5 V		1	6	mV
GATE VOLTAGE SHAPING						
$r_{DS(ON)H}$	VGH to VGHM ON resistance	V_{GH} = 24 V, I_{GHM} = 10 mA, V_{FLK} = 2.5 V		13	25	Ω
$r_{DS(ON)L}$	VGHM to RE ON resistance	V_{GHM} = 24 V, I_{GHM} = 10 mA, V_{FLK} = 0 V		13	25	Ω
V_{IH}	High-level input voltage	V_{FLK} rising	1.5			V
V_{IL}	Low-level input voltage	V_{FLK} falling			0.6	V
t_{PLH}	Propagation delay	V_{GHM} rising, 2.5 V, 50% thresholds, C_{OUT} = 150 pF, R_E = 0 mΩ		100	200	ns
t_{PHL}		V_{GHM} falling, 2.5 V, 50% thresholds, C_{OUT} = 150 pF, R_E = 0 mΩ		100	200	
t_{DLY}	Gate voltage shaping / LCD bias ready delay range	**DLY** = 00		0		ms
		DLY = 01		20		
		DLY = 10		40		
		DLY = 11		60		
T_{CON} RESET GENERATOR						
V_{DIV}	Detecting voltage falling threshold	**VDIV** = 000	1.08	1.2	1.32	V
		VDIV = 001	1.26	1.4	1.54	
		VDIV = 010	1.44	1.6	1.76	
		VDIV = 011	1.62	1.8	1.98	
		VDIV = 100	1.8	2	2.2	
		VDIV = 101	1.98	2.2	2.42	
		VDIV = 110	2.16	2.4	2.64	
		VDIV = 111	2.34	2.6	2.86	
	Hysteresis			150		mV
$V_{OL(\overline{RST})}$	Output voltage	$I_{\overline{RST}}$ = 1 mA (sinking)			0.5	V
$I_{LK(\overline{RST})}$	Leakage current	$V_{\overline{RST}}$ = 2.5 V			1	µA
t_{RESET} (1)	Reset delay time	**RESET** = 0000		0		ms
		…		**…**		
		RESET = 1111		30		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	T_J rising		150		°C
I^2C INTERFACE						
ADDR	Configuration parameters slave address			E8		
	Programmable V_{COM} slave address			9E		
V_{IL}	Low level input voltage	Supply = 2.5 V, V_{IN} falling, standard and fast modes			0.3 × V_{25}	V
V_{IH}	High level input voltage	Supply = 2.5 V, V_{IN} rising, standard and fast[4] modes	0.7 × V_{25}			V
V_{HYS}	Hysteresis	Supply = 2.5 V, applicable to fast mode only	125			mV
V_{OL}	Low level output voltage	Sinking 3 mA			500	mV
C_I	Input capacitance				10	pF
f_{SCL}	Clock frequency	Standard mode			100	kHz
		Fast mode			400	
t_{LOW}	Clock low period	Standard mode	4.7			µs
		Fast mode	1.3			
t_{HIGH}	Clock high period	Standard mode	4			µs
		Fast mode	0.6			

(1) Refer to Table 12 for RESET time delay break down.

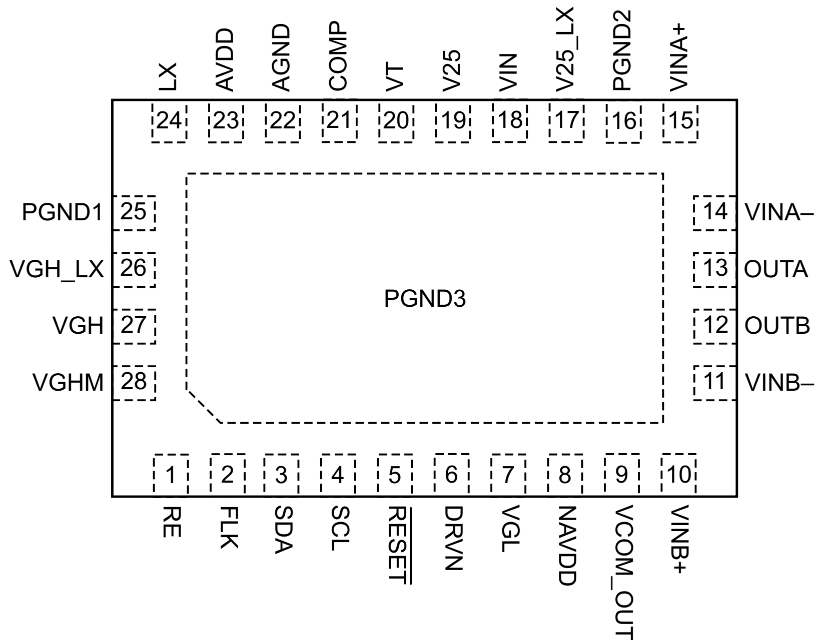
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.3 V; V_{25} = 2.5 V, AV_{DD} = 8.5 V, V_{GH} = 23 V, V_{GL} = –6 V, R_{CAMP}=200kΩ, C_{CAMP}=1 nF, NAV_{DD} = AGND = PGND = 0V, T_A = –40 °C to 85 °C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
$t_{hd:STA}$	Hold time for a repeated START condition	Standard mode	4			µs
		Fast mode	0.6			
$t_{su:STA}$	Set-up time for a repeated START condition	Standard mode	4			µs
		Fast mode	0.6			
$t_{su:DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
$t_{hd:DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	
t_{RCL1}	Rise time of SCL after a repeated START condition and after an ACK bit	Standard mode	20 + $0.1C_B$		1000	ns
		Fast mode	20 + $0.1C_B$		1000	
t_{RCL}	Rise time of SCL	Standard mode	20 + $0.1C_B$		1000	ns
		Fast mode	20 + $0.1C_B$		300	
t_{FCL}	Fall time of SCL	Standard mode	20 + $0.1C_B$		300	ns
		Fast mode	20 + $0.1C_B$		300	
t_{RDA}	Rise time of SDA	Standard mode	20 + $0.1C_B$		1000	ns
		Fast mode	20 + $0.1C_B$		300	
t_{FDA}	Fall time of SDA	Standard mode	20 + $0.1C_B$		300	ns
		Fast mode	20 + $0.1C_B$		300	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4			µs
		Fast mode	0.6			
C_B	Capacitive load on SDA and SCL	Standard mode			400	pF
		Fast mode			400	
E^2PROM						
N_{WRITE}	Number of write cycles		1000			
t_{WRITE}	Write time				100	ms
	Data retention	Storage temperature = 150°C	100000			hrs

DEVICE INFORMATION

PIN ASSIGNMENT
28 PIN 5.5mm × 3.5mm RHR PACKAGE
TOP VIEW



PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	22	P	Ground
AVDD	23	I	AVDD sense pin
COMP	21	O	Boost converter 1 compensation. Connect a suitable compensation network (typically a series R-C combination) between this pin and ground
DRVN	6	O	Drive output for negative linear regulator
FLK	2	I	Gate voltage shaping flicker clock input
LX	24	P	Boost convert 1 switch node
NAVDD	8	I	Negative AVDD voltage input
OUTA	13	O	Operational amplifier A output
OUTB	12	O	Operational amplifier B output
PGND1	25	P	Power Ground 1 for boost converter 2
PGND2	16	P	Power Ground 2 for buck converter
PGND3	29	P	Power Ground 3 for boost converter 1
RE	1	O	Gate voltage shaping discharge resistor connection
RESET	5	O	T-CON reset output
SCL	4	I	I^2C Interface serial clock
SDA	3	I/O	I^2C Interface serial data
VCOM_OUT	9	O	VCOM amplifier output
VGH	27	P	Gate voltage shaping input and boost converter 2 output sense
VGH_LX	26	P	Boost converter 2 switch node
VGHM	28	O	Gate voltage shaping output
VGL	7	I	Negative linear regulator sense pin
VIN	18	P	Supply voltage

PIN FUNCTIONS (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
VINA+	15	I	Operational amplifier B non-inverting input
VINA–	14	I	Operational amplifier A inverting input
VINB+	10	I	Operational amplifier B non-inverting input
VINB–	11	I	Operational amplifier B inverting input
VT	20	I	Boost converter 2 and V_{COM} reference external thermistor network connection
V25	19	O	Buck converter or LDO regulator output sense
V25_LX	17	P	Buck converter switch node or LDO regulator output

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

PARAMETER	CONDITIONS	FIGURE
BOOSTER CONVERTER 1		
Efficiency vs. Load Current	V_{IN} = 3.3 V, AV_{DD} = 5.5 V and 8.5V, L = 10 µH, f_{SW} = 1 MHz	Figure 1
Output Voltage Ripple	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, I_{AVDD} = 200 mA, f_{SW} = 1 MHz	Figure 2
Load Transient Response	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, I_{AVDD} = 20 mA to 200 mA	Figure 3
Startup	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, f_{SW} = 1 MHz, I_{LOAD} = 55 Ω	Figure 4
Over Voltage Protection	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, f_{SW} = 1 MHz	Figure 5
Under Voltage Protection	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, f_{SW} = 1 MHz	Figure 6
BUCK CONVERTER		
Efficiency vs. Load Current	V_{IN} = 3.3 V, V_{25} = 1.8 V and 2.5 V	Figure 7
Output Voltage Ripple	V_{IN} = 3.3 V, V_{25} = 2.5 V, I_{V25} = 600 mA	Figure 8
Load Transient Response	V_{IN} = 3.3 V, V_{25} = 2.5 V, I_{V25} = 20 to 200 mA	Figure 9
Startup	V_{IN} = 3.3 V, V_{25} = 2.5 V, I_{LOAD} = 12.5 Ω	Figure 10
Undervoltage Protection	V_{IN} = 3.3 V, V_{25} = 2.5 V	Figure 11
LDO VOLTAGE REGULATOR		
Load Transient Response	V_{IN} = 3.3 V, V_{25} = 2.5 V, I_{V25} = 20 to 200 mA	Figure 12
Startup	V_{IN} = 3.3 V, V_{25} = 2.5 V, I_{LOAD} = 12.5 Ω	Figure 13
Undervoltage Protection	V_{IN} = 3.3 V, V_{25} = 2.5 V	Figure 14
BOOST CONVERTER 2		
Efficiency vs. Load Current	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GH} = 16 V, L = 10 µH, f_{SW} = 800 kHz	Figure 15
Efficiency vs. Load Current	V_{IN} = 3.3 V, AV_{DD} = 8.5 V, V_{GH} = 25 V, L = 10 µH, f_{SW} = 800 kHz	Figure 16
Output Voltage Ripple	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GH} = 16 V, L = 10 µH, I_{VGH} = 50 mA, f_{SW} = 800 kHz	Figure 17
Load Transient Response	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GH} = 16 V, L = 10 µH, I_{VGH} = 10 to 50 mA	Figure 18
Startup	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GH} = 16 V, L = 10 µH, f_{SW} = 800 kHz	Figure 19
Under Voltage Protection	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GH} = 16 V, L = 10 µH, f_{SW} = 800 kHz	Figure 20
NEGATIVE CHARGE PUMP REGULATOR CONTROL		
Output Voltage Ripple	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GL} = –4.5 V, I_{GL} = 50 mA	Figure 21
Load Transient Response	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GL} = –4.5 V, I_{GL} = 10 to 50 mA	Figure 22
GATE VOLTAGE SHAPING	V_{IN} = 3.3 V, AV_{DD} = 5 V, AV_{DD} = 5 V,	Figure 23
OPERATIONAL AMPLIFIER SLEW RATE	V_{IN} = 3.3 V, V_{GH} = 16 V, NAV_{DD} = –5 V, INA+ = –1 V to 1 V	Figure 24
POWER ON SEQUENCY	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GH} = 16 V, V_{GL} = –4.5 V	Figure 25
POWER OFF SEQUENCY	V_{IN} = 3.3 V, AV_{DD} = 5.5 V, V_{GH} = 16 V, V_{GL} = –4.5 V	Figure 26

EFFICIENCY vs LOAD CURRENT

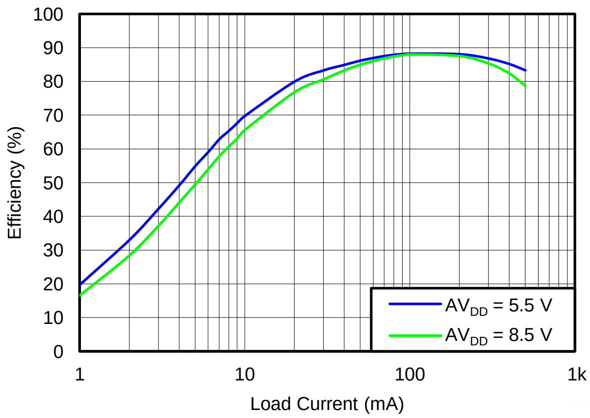


Figure 1. Boost Converter 1 Efficiency

OUTPUT VOLTAGE RIPPLE

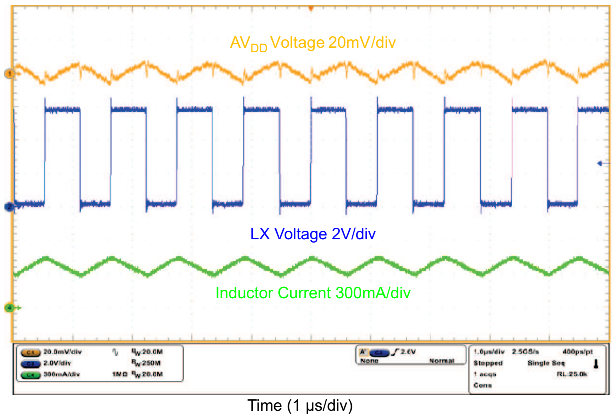


Figure 2. Boost Converter 1 Output Ripple

LOAD TRANSIENT RESPONSE

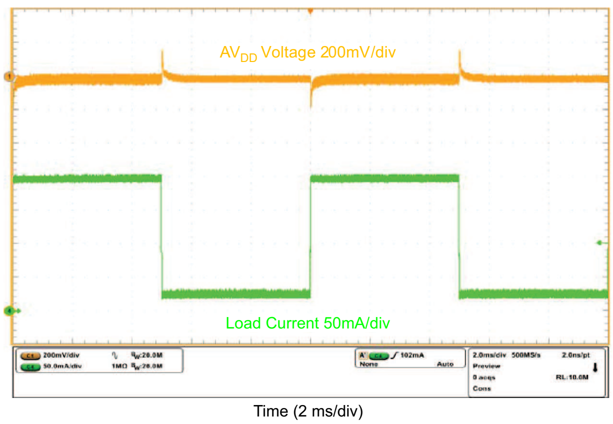


Figure 3. Boost Converter 1 Load Transient Response

STARTUP

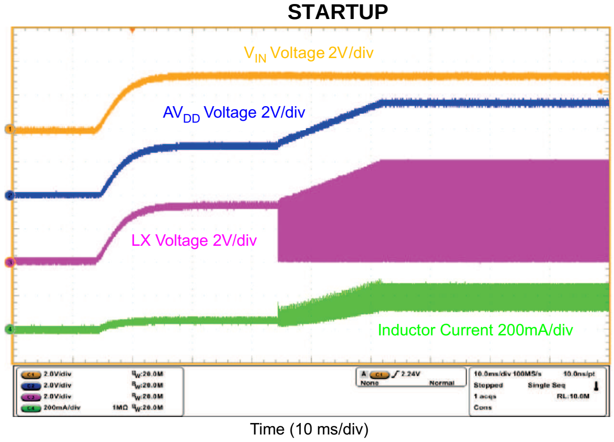


Figure 4. Boost Converter 1 Startup

OVERVOLTAGE PROTECTION

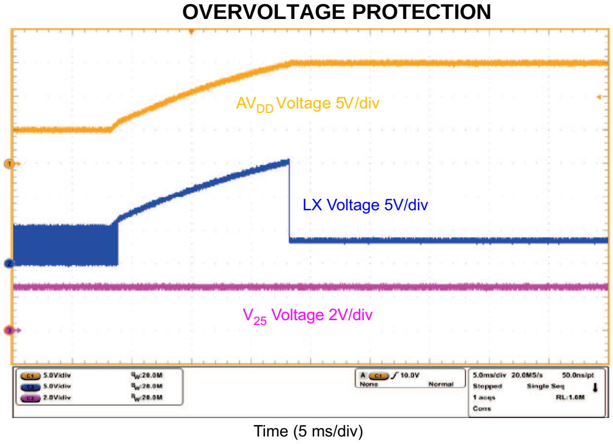


Figure 5. Boost Converter 1 Overvoltage Protection

UNDERVOLTAGE PROTECTION

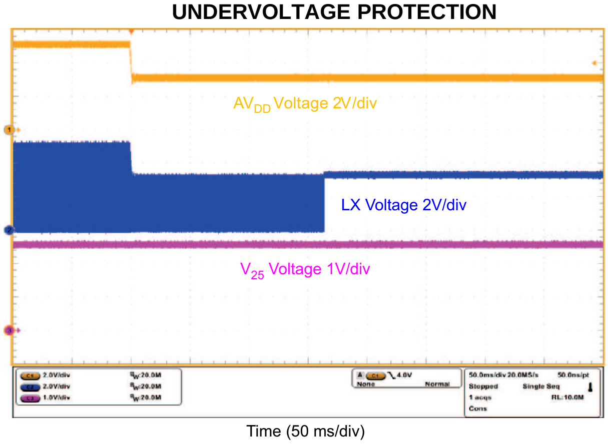


Figure 6. Boost Converter 1 Undervoltage Protection

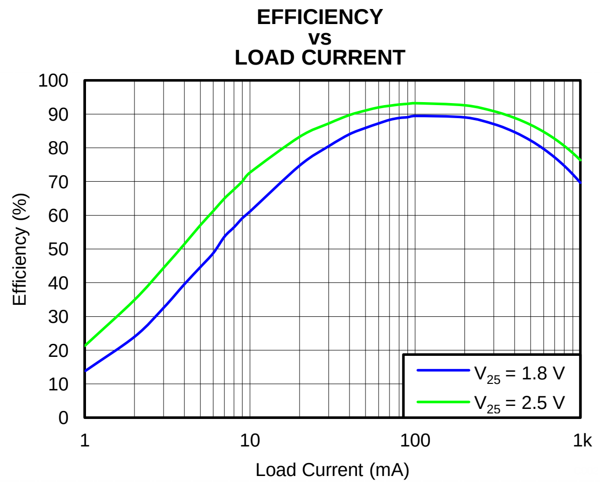


Figure 7. Buck Converter Efficiency

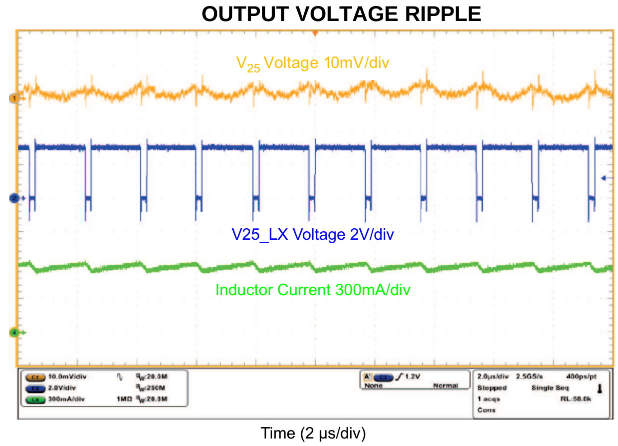


Figure 8. Buck Converter Output Ripple

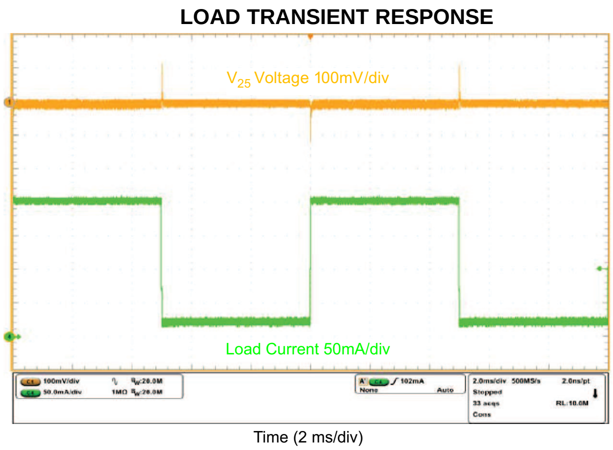


Figure 9. Buck Converter Load Transient Response

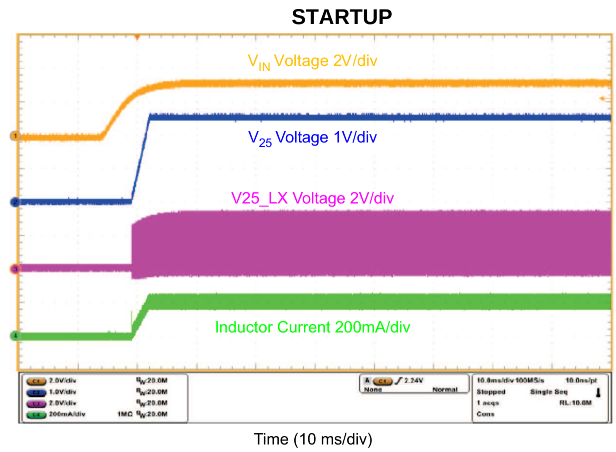


Figure 10. Buck Converter Startup

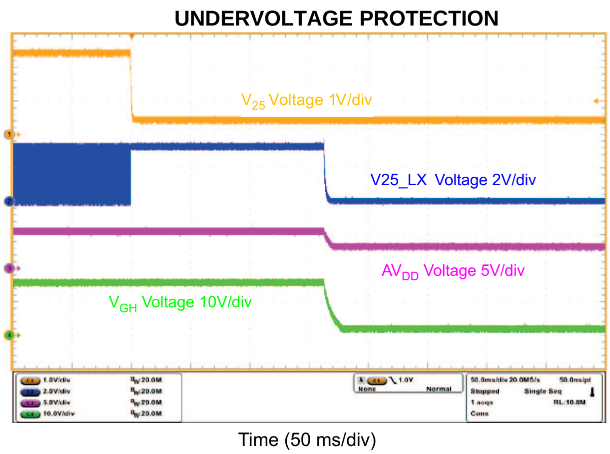


Figure 11. Buck Converter Undervoltage Protection

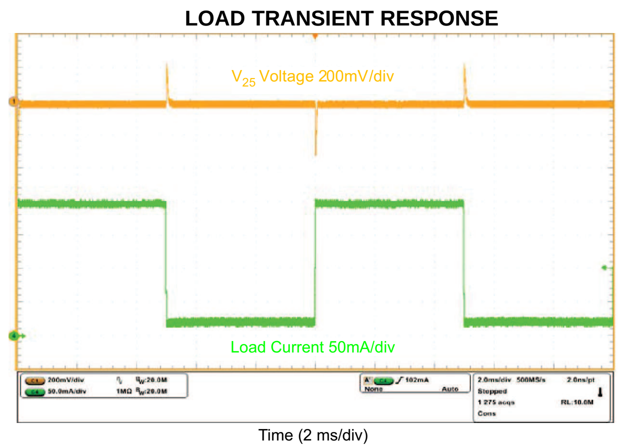


Figure 12. LDO Load Transient Response

STARTUP

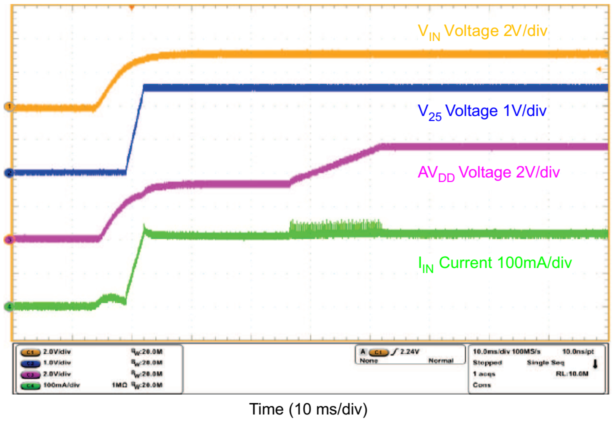


Figure 13. LDO Startup

UNDERVOLTAGE PROTECTION

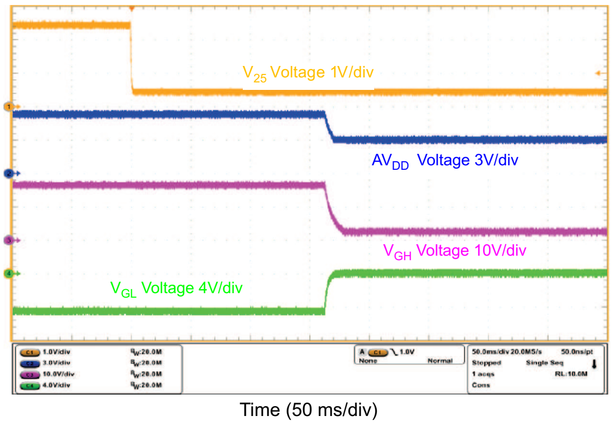


Figure 14. LDO Undervoltage Protection

EFFICIENCY
vs
LOAD CURRENT

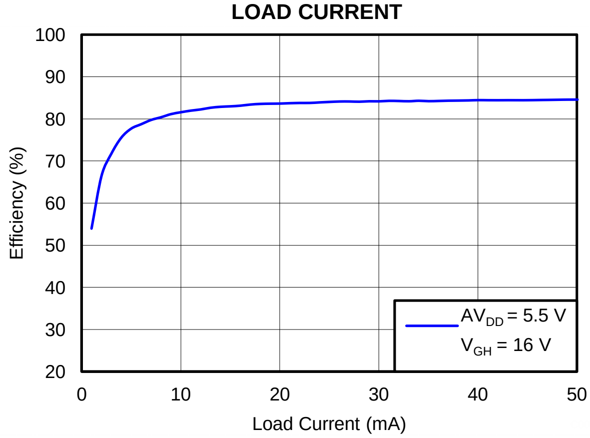


Figure 15. Boost Converter 2 Efficiency

EFFICIENCY
vs
LOAD CURRENT

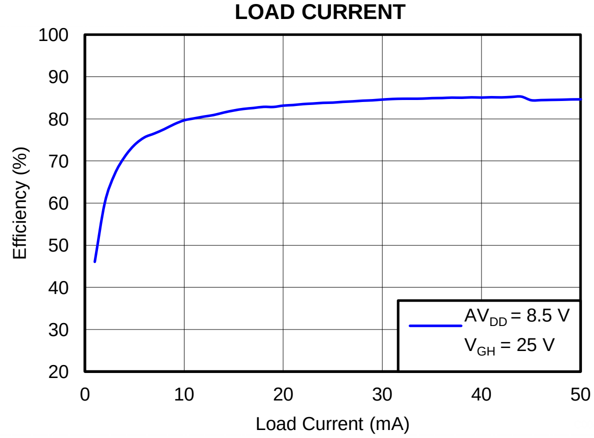


Figure 16. Boost Converter 2 Efficiency

OUTPUT VOLTAGE RIPPLE

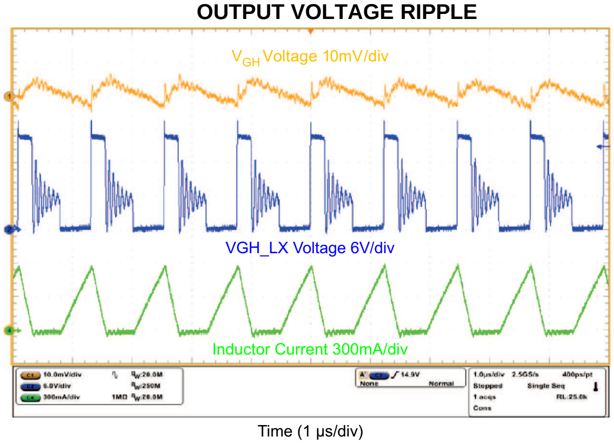


Figure 17. Boost Converter 2 Output Ripple

LOAD TRANSIENT RESPONSE

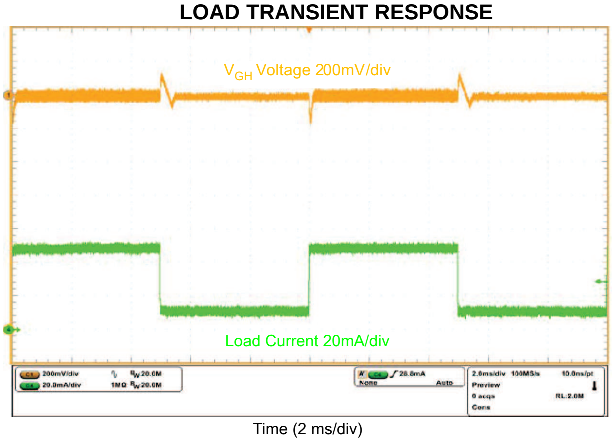
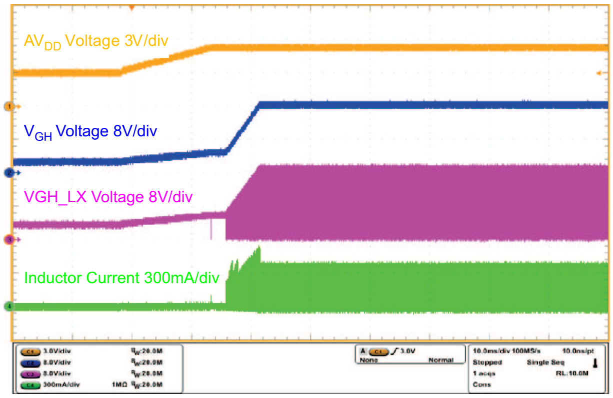


Figure 18. Boost Converter 2 Load Transient Response

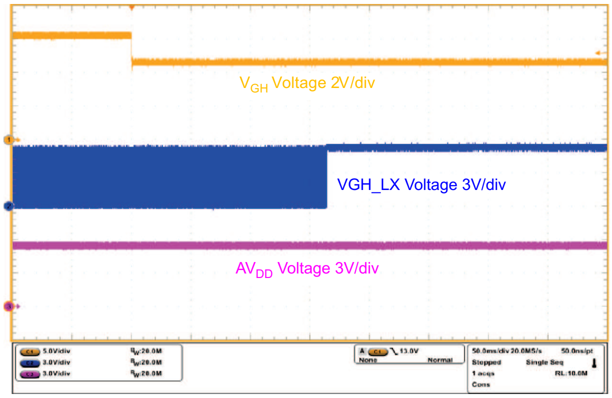
STARTUP



Time (10 ms/div)

Figure 19. Boost Converter 2 Startup

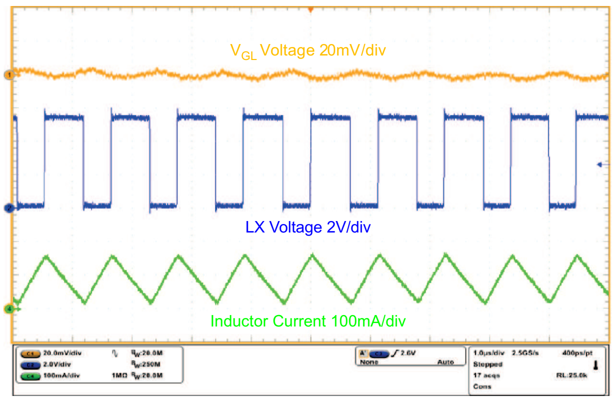
UNDERVOLTAGE PROTECTION



Time (50 ms/div)

Figure 20. Boost Converter 2 Undervoltage Protection

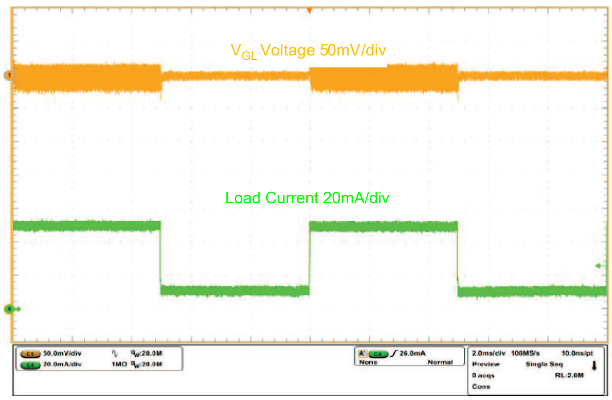
OUTPUT VOTLAGE RIPPLE



Time (1 µs/div)

Figure 21. Negative Charge Pump Output Ripple

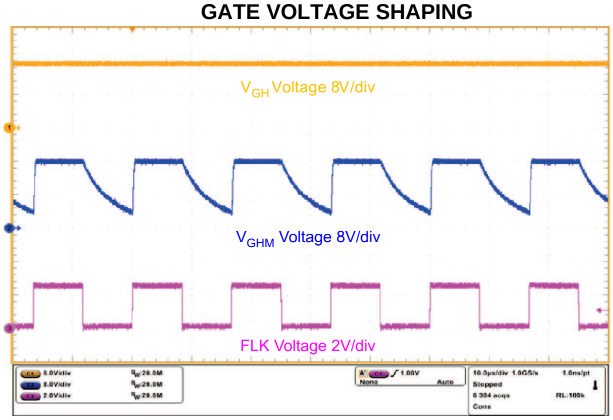
LOAD TRANSIENT RESPONSE



Time (2 ms/div)

Figure 22. Negative Charge Pump Load Transient Response

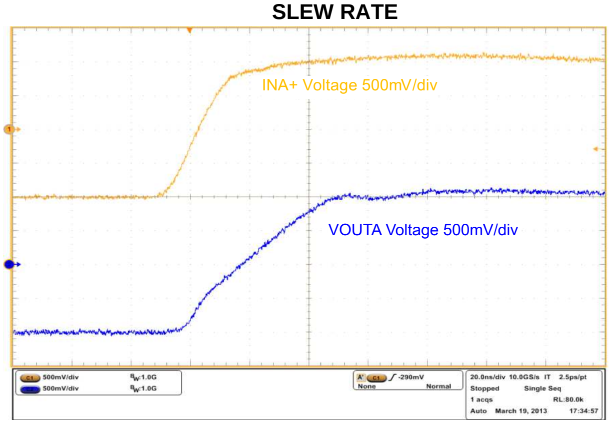
GATE VOLTAGE SHAPING



Time (10 µs/div)

Figure 23. Gate Voltage Shaping

SLEW RATE



Time (20 ns/div)

Figure 24. Operational Amplifier Slew Rate

POWER ON SEQUENCY

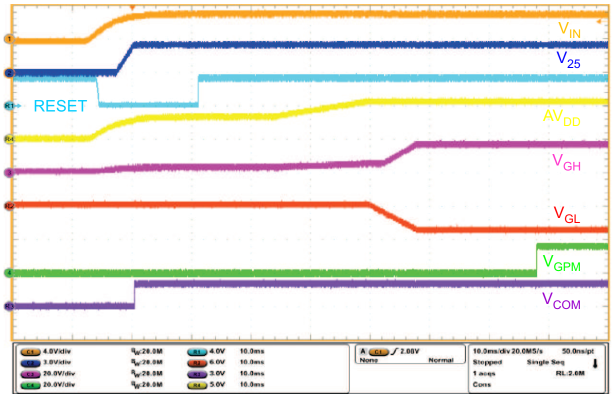


Figure 25. Power Off Sequency

POWER OFF SEQUENCY

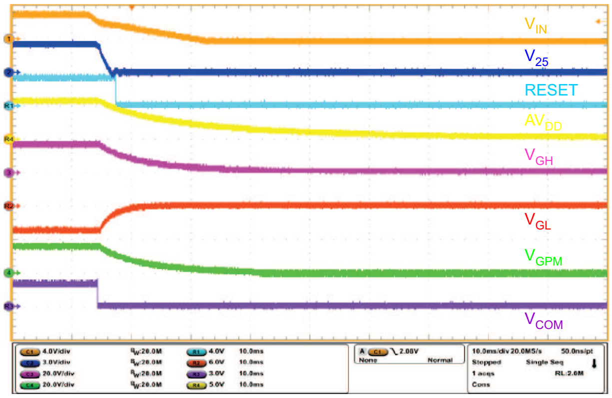


Figure 26. Power Off Sequency

DETAILED DESCRIPTION

An internal block diagram of the TPS65640 is shown in Figure 27.

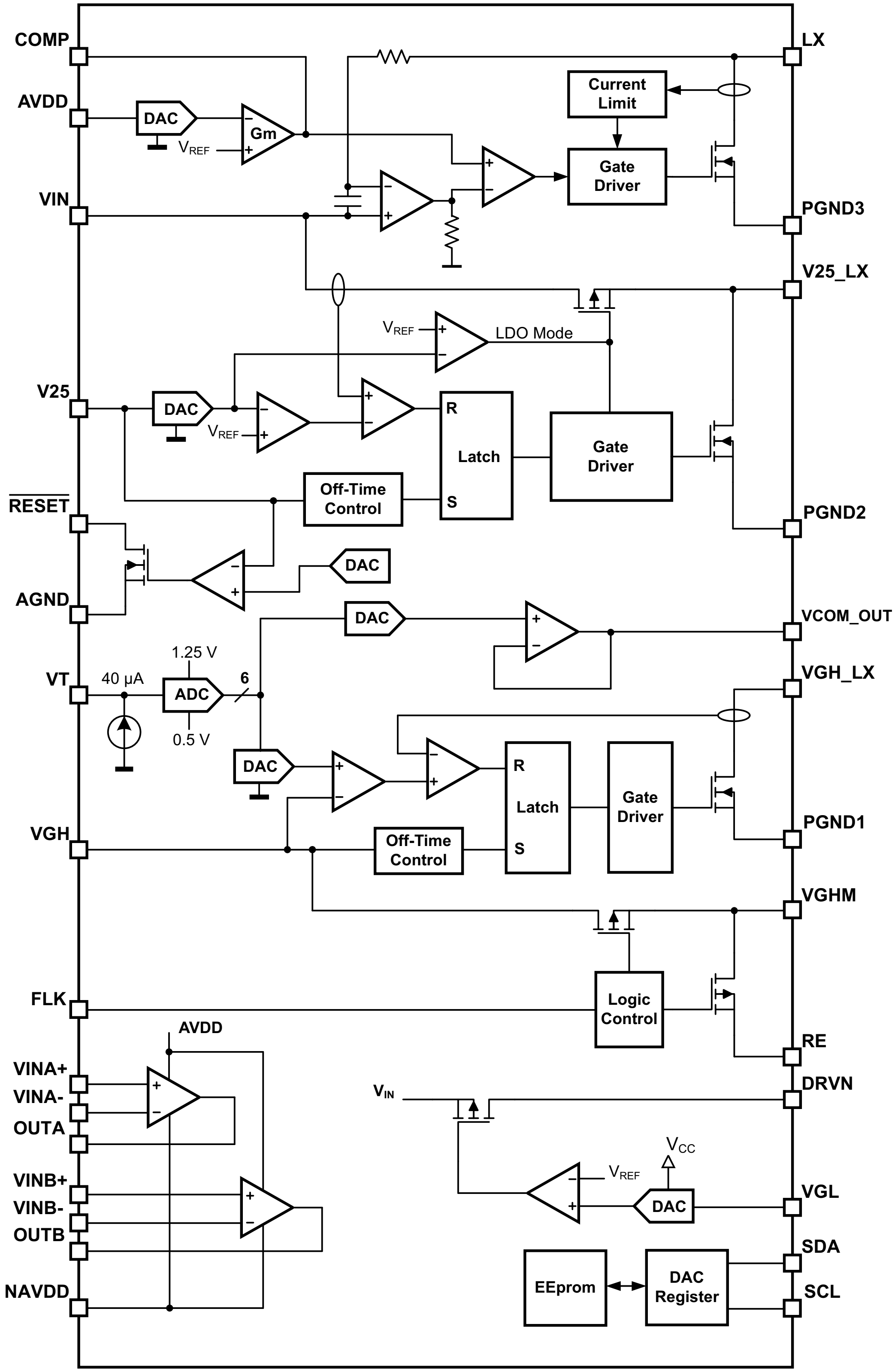


Figure 27. Internal Block Diagram

BOOST CONVERTER 1 (AV_{DD})

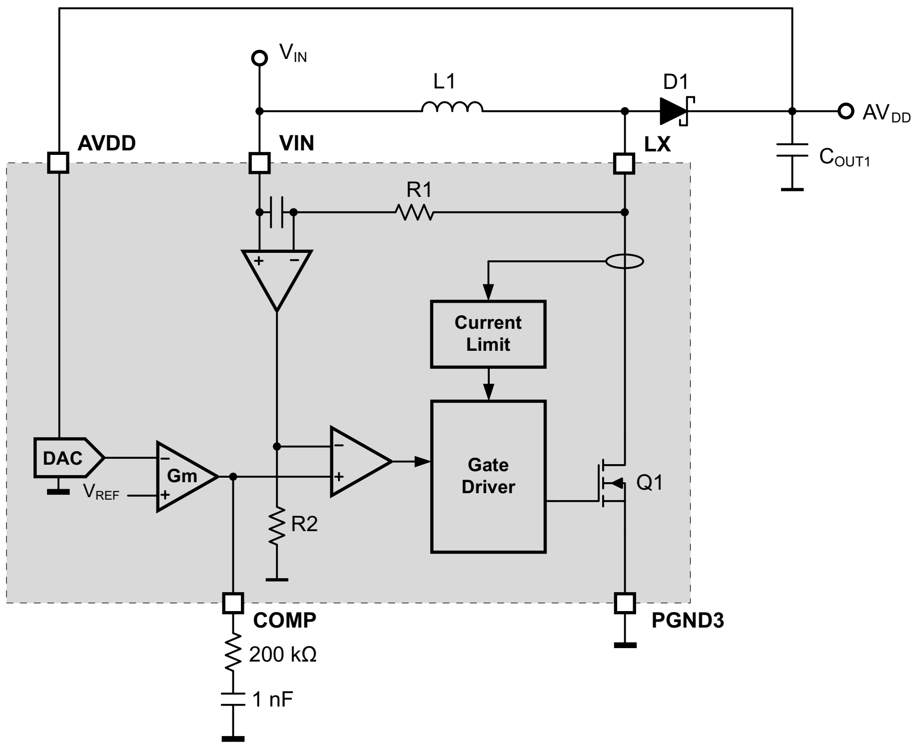


Figure 28. Boost Converter 1 Internal Block Diagram

Switching Frequency (Boost Converter 1)

Boost Converter 1 can be configured to operate at 600 kHz, 800 kHz, 1000 kHz, or 1200 kHz. In general, the higher switching frequency offers better transient performance at the expense of slightly reduced efficiency. In some applications, it may be necessary to select a particular switching frequency to minimize EMI problems. The switching frequency is determined by the state of the **FREQ1** configuration bit in the **AVDDCONFIG** register.

Compensation (Boost Converter 1)

Boost Converter 1 uses an external compensation network connected to its COMP pin to stabilize its feedback loop. A simple series R-C network connected between this pin and ground is sufficient to achieve good performance (that is, stable and with good transient response) in most applications. Good starting values, which will work for many applications, are 200 kΩ and 1 nF.

In some applications (for example, those using electrolytic output capacitors), it may be necessary to include a second compensation capacitor between the COMP pin and ground. This has the effect of adding an additional pole in the feedback loop's frequency response, which can be used to cancel the zero introduced by the electrolytic output capacitor's ESR.

Output Voltage (Boost Converter 1)

Boost converter 1's output voltage can be programmed from 3.6 V to 11 V with 100-mV increment using the **AVDD** register. Because changing the output voltage in big steps can temporarily demand switch currents greater than the switch's current limit, it is recommended that AV_{DD} be changed in 100-mV steps, for example, first change AV_{DD} from 7 V to 7.1 V, then to 7.2 V, then to 7.3 V, and so on until the desired output voltage has been achieved.

Start-Up (Boost Converter 1)

Boost converter 1 starts immediately after the V_{25} voltage raming to its programmed voltage.

To minimize inrush current during start-up, boost converter 1 ramps its output voltage in t_{SS1} milliseconds. The value of t_{SS1} can be programmed from 20ms to 80ms using the **SS1** bits in **AVDDCONFIG** register.

Boost converter 1's internal power good signal is asserted when two conditions are met:

- the converter's soft-start ramp has reached its final value
- the converter's output voltage is greater than its UVP threshold.

The power good signal is latched and will only be reset when the supply voltage is cycled.

Current limit (Boost Converter 1)

The boost converter 1 has built-in cycle-by-cycle current limit for the power MOSFET. When the inducotr current or the power MOSFET current reaches I_{LIM}, the power MOSFET will be tuned off immediately until the next switching cycle. The I_{LIM} can be programmed from 1 A to 2 A using the **AVDD ILIM** bit in **AVDDCONFIG** register.

Design Procedure (Boost Converter 1)

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter 1 supports the specific application requirements.

1. Converter Duty Cycle:

$$D = 1 - \frac{V_{IN} \times \eta}{V_{AVDD}} \quad (1)$$

2. Inductor Ripple Current:

$$\Delta I_L = \frac{V_{IN} \times D}{f_s \times L} \quad (2)$$

3. Maximum Output Current:

$$I_{OUT\_max} = \left(I_{LIM\_min} - \frac{\Delta I_L}{2}\right) \times (1 - D) \quad (3)$$

4. Peak Switching Current:

$$I_{SWPEAK} = \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2} \quad (4)$$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 0.9 as an estimation)

f_S = Switching frequency

L = Selected inductor value (typ. 10 µH)

I_{LIM_min}: Minimum current limit

I_{SWPEAK} = Peak switch current for the used output current

ΔI_L = Inductor peak-to-peak ripple current

The peak switch current I_{SWPEAK} is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

Inducotr Selection (Boost Converter 1)

Inductor Value:	4.7 µH ≤ L ≤ 10 µH	Higher the inductor value the lower the inductor current ripple and the output voltage ripple but the slower the transient response.
Saturation Current:	$I_{SAT} \ge I_{SWPEAK}$ or $I_{SAT} \ge I_{LIM\_max}$	The inductor saturation current must be higher than the switch peak current for the max. peak output current or as a more conservative approach higher than the max. switch current limit.
DC Resistance:	The lower the inductors resistance the lower the losses and the higher the efficiency.	

Rectifier Diode Selection (Boost Converter 1)

Diode type: Schottky or super barrier rectifier (SBR) for better efficiency.

Forward voltage: The lower the forward voltage VF the higher the efficiency and the lower the diode temperature.

Reverse voltage: V_R must be higher than the output voltage and should be higher than the OVP voltage typically 15 V.

Thermal characteristics: The diode must be able to handle the dissipated power of $P_D = V_F \times I_{OUT}$.

Output Capacitor Selection (Boost Converter 1)

For best output voltage filtering, TI recommends low-ESR ceramic capacitors. Two 4.7 µF (or four 2.2-µF) ceramic capacitors work for most applications. To improve the load transient response more capacitance can be added between the rectifier diode.

To calculate the output voltage ripple the following equations can be used:

$$\Delta V_{C\_RIPPLE} = \frac{V_{AVDD} - V_{IN}}{V_{AVDD} \times f_s} \text{ x } \frac{I_{OUT}}{C_{OUT}} + \Delta V_{C\_ESR} \quad (5)$$

$$\Delta V_{C\_ESR} = I_{SWPEAK} \times R_{C\_ESR} \quad (6)$$

BUCK CONVERTER (V_{25})

The buck converter uses a current mode, quasi-constant off-time topology that offers high efficiency, fast transient response, and constant ripple current amplitude under all operating conditions (see Figure 29). The converter's off time is inversely proportional V_{25} and therefore constant when the converter is in regulation. Thus for a given V_{IN} the converter operates at a constant frequency that changes temporarily when the converter reacts to load changes.

When the latch is set, transistor Q_1 is turned on and transistor Q_2 is turned off. As inductor L_2 charges, the current flowing through Q_1 ramps up at a rate determined by the difference between V_{IN} and V_{CORE} and the value of L_2. The ramping current is sensed across Q_1, and when it reaches the level demanded by error amplifier A_1 the output of comparator A_2 goes high, resetting the latch. The reset latch turns off Q_1 and turns on Q_2. Inductor L_2 now discharges through Q_2 for a fixed off time. At the end of the off time, the latch is set, turning on Q_1 and turning off Q_2, and the cycle repeats.

The sensed output voltage is divided down by a multiplying DAC and used as negative feedback to amplifier A_1. The output of A_1 is the error signal required to regulate V_{25} at the desired voltage.

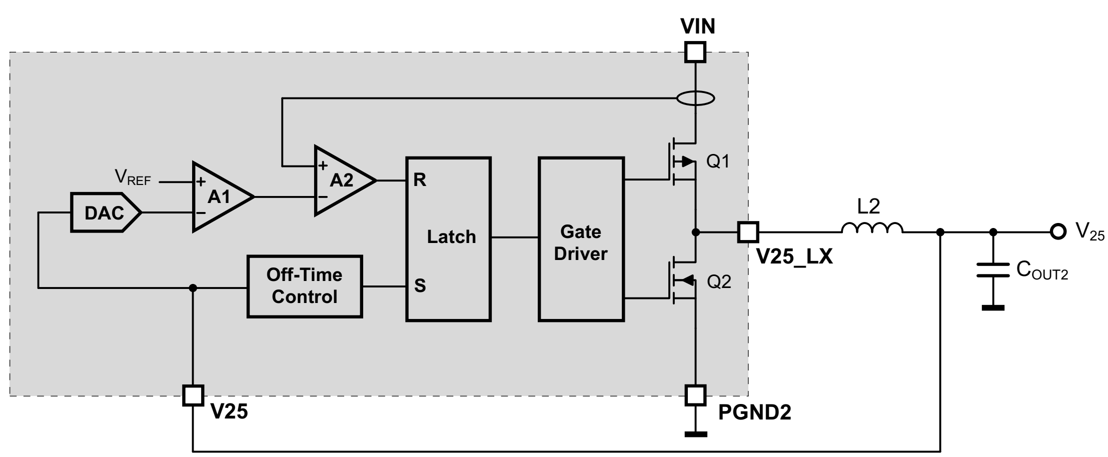


Figure 29. Buck Converter 1 Block Diagram

Output Voltage (Buck Converter)

Buck converter's output voltage can be programmed from 1.5 V to 3.0 V using the **V25** register.

Start-Up (Buck Converter)

Buck converter starts as soon as the supply voltage exceeds the under-voltage lockout threshold (the same time as the linear regulator starts).

To minimize inrush current during start-up, buck converter ramps V_{25} from 0 V to programmed voltage in t_{SS2} milliseconds. The value of t_{SS2} is around 0.5 ms to 4.0 ms.

The same ramp rate is used for both buck converter and the linear regulator (LDO).

Current limit (Buck Converter)

The buck converter has built-in cycle-by-cycle current limit for the high side power MOSFET, Q1 in Figure 29. When the inductor current or the MOSFET Q1 current reaches I_{LIM}, the Q1 is tuned off immediately until the next switching cycle. The I_{LIM} is typically 1.2 A.

Design Procedure (Buck Converter)

The first step in the design procedure is to verify whether the maximum possible output current of the buck converter supports the specific application requirements.

1. Switching Frequency:

$$f_s = \frac{V_{IN} \times \eta - V_{25}}{V_{IN} \times \eta \times T_{off}} \tag{7}$$

2. Converter Duty Cycle

$$D = \frac{V_{25}}{V_{IN} \times \eta} \tag{8}$$

3. Inductor Ripple Current:

$$\Delta I_L = \frac{(V_{IN} - V_{25}) \times D}{f_s \times L} \tag{9}$$

4. Maximum Output Current:

$$I_{OUT\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2} \tag{10}$$

5. Peak Switching Current:

$$I_{SWPEAK} = I_{OUT} + \frac{\Delta I_L}{2} \tag{11}$$

T_{off} = Buck boost switch duty off time (typ. 200 ns)

η = Estimated boost converter efficiency (use the number from the efficiency plots or 0.8 as an estimation)

f_S = Switching frequency

L = Selected inductor value (typ. 10 µH)

I_{LIM_min}: Minimum current limit

I_{SWPEAK} = Peak switch current for the used output current

ΔI_L = Inductor peak-to-peak ripple current

The peak switch current I_{SWPEAK} is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

Inducotr Selection (Buck Converter)

Inductor Value:	4.7 µH ≤ L ≤ 10 µH	Higher the inductor value the lower the inductor current ripple and the output voltage ripple but the slower the transient response.

Saturation Current:	$I_{SAT} \geq I_{SWPEAK}$ or $I_{SAT} \geq I_{LIM\_max}$	The inductor saturation current must be higher than the switch peak current for the max. peak output current or as a more conservative approach higher than the max. switch current limit.
DC Resistance:	The lower the inductors resistance the lower the losses and the higher the efficiency.	

Output Capacitor Selection (Buck Converter)

For best output voltage filtering, TI recommends low-ESR ceramic capacitors. Two 4.7-µF (or four 2.2-µF) ceramic capacitors work for most applications. To improve the load transient response more capacitance can be added between the rectifier diode.

To calculate the output voltage ripple the following equations can be used:

$$\Delta V_{C\_RIPPLE} = \frac{V_{25}}{V_{IN} \times f_s} \times \frac{I_{OUT}}{C_{OUT}} + \Delta V_{C\_ESR} \quad (12)$$

$$\Delta V_{C\_ESR} = I_{SWPEAK} \times R_{C\_ESR} \quad (13)$$

LDO REGULATOR (V_{25})

A low-dropout (LDO) linear regulator generates V_{25} (see Figure 30). The linear regulator is supplied from V_{IN} and it's an alternative option to buck converter. The V_{25} voltage could be supplied either by Buck converter or LDO determined by the state of the **BUCK/LDO** configuration bit in the **CONFIG** register.

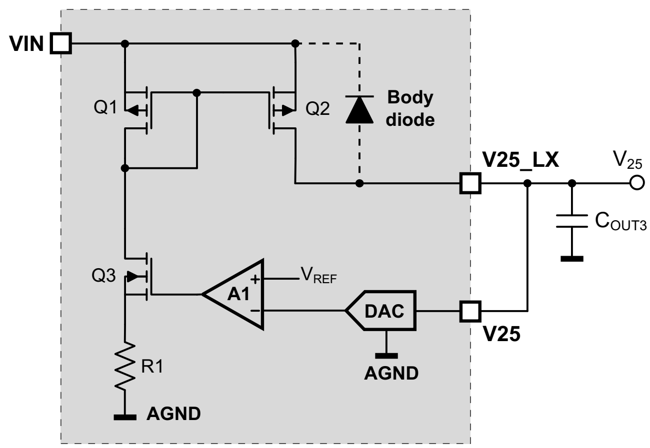


Figure 30. Linear Regulator Block Diagram

Amplifier A_1 regulates the current through Q_3 by comparing a reduced version of the output voltage with a bandgap voltage reference V_{REF}. The output of Q_3 is mirrored by Q_1 and Q_2 to generate the desired output voltage. In practice, Q_2 is made much bigger than Q_1. This means that the current flowing through Q_1 and Q_3 is smaller than the output current by the same ratio as the transistor areas.

The maximum output current is inherently limited by the maximum output voltage of A_1, the value of resistor R_1, and the characteristics of transistor Q_3.

Output Voltage (LDO Regulator)

LDO's output voltage can be programmed from 1.5 V to 3.0 V using the **V25** register. Because the V25_LX pin alternates for LDO regulator's output voltage and buck converter's switch node, select buck converter with LDO circuit configuration can make the permanent damage. The LDO regulator mode is factory default setup.

Start-Up (Low Dropout Regulator)

LDO starts as soon as the supply voltage exceeds the under-voltage lockout threshold (the same time as the buck converter starts).

To minimize inrush current during start-up, LDO regulator ramps V_{25} from 0V to programmed voltage in t_{SS2} milliseconds. The value of t_{SS2} is around 0.5 ms to 4.0 ms.

The same ramp rate is used for both buck converter and the linear regulator.

BOOST CONVERTER 2 (V_{GH})

Boost converter 2 is a low-power boost converter that can be used to generate the LCD panel's gate ON voltage V_{GH}. Operating the converter in DCM removes the right-half-plane zero from its transfer function, simplifying its stabilization and allowing the use of small chip inductors. To simplify its application and to minimize the external parts required, boost converter 2 features internal compensation and soft-start circuitry.

A simplified block diagram of boost converter 2 is shown in Figure 31.

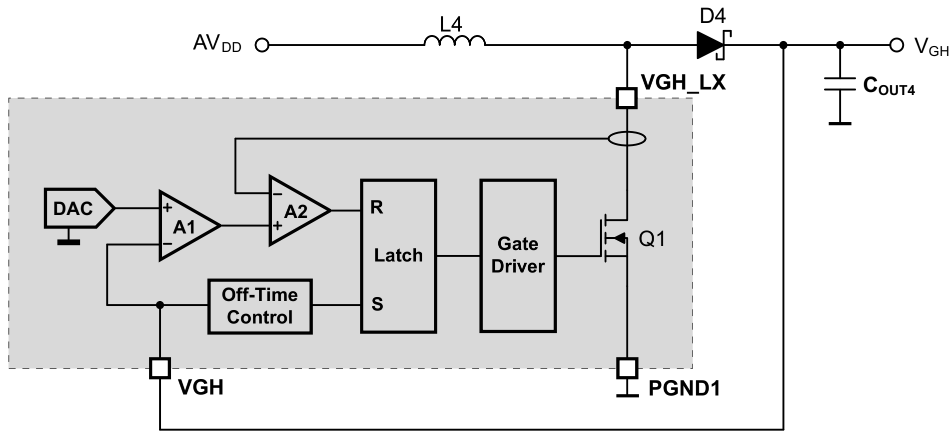


Figure 31. Boost Converter 2 Block Diagram

Switching Frequency (Boost Converter 2)

Boost Converter 2 can be configured to operate at 400 kHz or 800 kHz. The switching frequency is determined by the state of the **FREQ4** configuration bit in the **VGHCONFIG** register.

Output Voltage Temperature Compensation (Boost Converter 2)

Boost converter 2 can be temperature compensated, allowing its output voltage to transition from a higher voltage at low temperatures $V_{GH(COLD)}$ to a lower voltage at high temperatures $V_{GH(HOT)}$ (see Figure 32 and Figure 33).

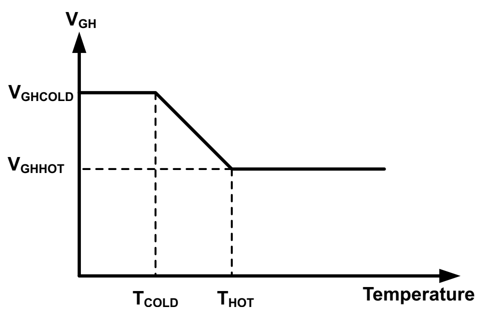


Figure 32. Boost Converter 2 Temperature Compensation Characteristic

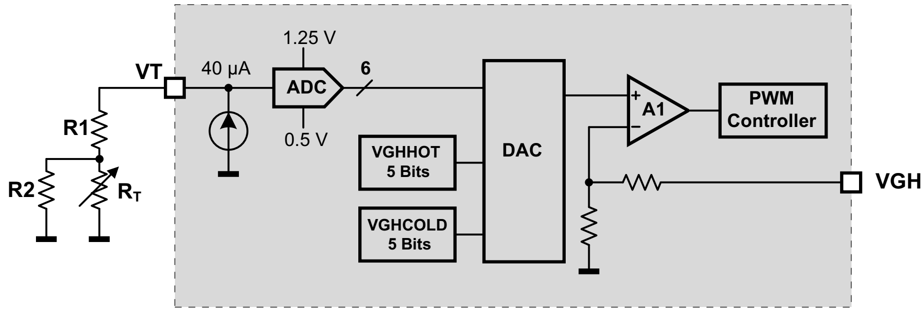


Figure 33. Boost Converter 2 Temperature Compensation Block Diagram

Referring to Figure 33, The thermistor network formed by R1, R2, and R_T [(1)] generates a voltage at the VT pin whose value decreases with increasing temperature. With proper selection [(2)] of the external components R_T, R1 and R2, temperatures T_{HOT} and T_{COLD} can be configured to suit each display's characteristics. A spreadsheet allowing easy calculation of component values is available from Texas Instruments free of charge.

Output Voltage (Boost Converter 2)

The output voltage of boost converter 2 at cold temperatures can be programmed from 15 V to 37 V using the **VGHCOLD** register.

The output voltage of boost converter 2 at hot temperatures can be programmed from 15 V to 37 V using the **VGHHOT** register.

In applications that do not require temperature compensation, the **VGHT** bit in **CONFIG** register should be set to 1 and the **VGHHOT** register used to set the voltage of V_{GH}.

Because changing the output voltage in big steps can temporarily demand switch currents greater than the switch's current limit, it is recommended that V_{GH} be changed in 1 V steps, i.e. first change V_{GH} from 15 V to 16 V, then to 16 V, then to 17 V, and so on until the desired output voltage has been achieved.

Start-Up (Boost Converter 2)

Boost converter 2 is enabled when AVDD has finished ramping to its programmed voltage.

To minimize inrush current during start-up, boost converter 2 ramps V_{GH} to its programmed value in t_{SS4} seconds. The value of t_{SS4} can be programmed from 4 ms to 16 ms using the **SS4** bits in **VGHCONFIG** register. The same ramp rate is used for both boost converter 2 and the negative charge pump regulator.

Boost converter 2's internal power good signal is asserted when two conditions are met:

- the converter's soft-start ramp has reached its final value
- the converter's output voltage is greater than its UVP threshold.

The power good signal is latched and will only be reset when the supply voltage is cycled.

Current limit (Boost Converter 2)

The boost converter 2 has built-in cycle-by-cycle current limit for the power MOSFET. When the inducotr current or the power MOSFET current reaches I_{LIM}, the power MOSFET will be tuned off immediately until the next switching cycle. The I_{LIM} is typically 1.2 A for boost converter 2.

Design Procedure (Boost Converter 2)

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements.

1. Converter Duty Cycle:

(1) R_T should be a negative temperature coefficient (NTC) type whose resistance at 25°C is 10kΩ.
(2) Texas Instruments can provide a spreadsheet that calculates suitable component values automatically.

$$D = 1 - \frac{V_{AVDD} \times \eta}{V_{GH}} \quad (14)$$

2. Inductor Ripple Current:

$$\Delta I_L = \frac{V_{AVDD} \times D}{f_s \times L} \quad (15)$$

3. Maximum Output Current:

$$I_{OUT\_max} = \left(I_{LIM\_min} - \frac{\Delta I_L}{2} \right) \times (1 - D) \quad (16)$$

4. Peak Switching Current:

$$I_{SWPEAK} = \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2} \quad (17)$$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 0.9 as an estimation)

f_S = Switching frequency

L = Selected inductor value (typ. 10 µH)

I_{LIM_min}: Minimum current limit

I_{SWPEAK} = Peak switch current for the used output current

ΔI_L = Inductor peak-to-peak ripple current

The peak switch current I_{SWPEAK} is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

Inducotr Selection (Boost Converter 2)

Inductor Value:	4.7 µH ≤ L ≤ 10 µH	Higher the inductor value the lower the inductor current ripple and the output voltage ripple but the slower the transient response.
Saturation Current:	$I_{SAT} \geq I_{SWPEAK}$ or $I_{SAT} \geq I_{LIM\_max}$	The inductor saturation current must be higher than the switch peak current for the max. peak output current or as a more conservative approach higher than the max. switch current limit.
DC Resistance:	The lower the inductors resistance the lower the losses and the higher the efficiency.	

Rectifier Diode Selection (Boost Converter 2)

Diode type: Schottky or super barrier rectifier (SBR) for better efficiency.

Forward voltage: The lower the forward voltage VF the higher the efficiency and the lower the diode temperature.

Reverse voltage: V_R must be higher than the output voltage and should be higher than the OVP voltage 39 V.

Thermal characteristics: The diode must be able to handle the dissipated power of $P_D = V_F$ x I_{OUT}.

Output Capacitor Selection

For best output voltage filtering, TI recommends low-ESR ceramic capacitors. Two 4.7-µF (or four 2.2-µF) ceramic capacitors work for most applications. To improve the load transient response more capacitance can be added between the rectifier diode.

To calculate the output voltage ripple the following equations can be used:

$$\Delta V_{C\_RIPPLE} = \frac{V_{GH} - V_{AVDD}}{V_{GH} \times f_s} \times \frac{I_{OUT}}{C_{OUT}} + \Delta V_{C\_ESR} \quad (18)$$

$$\Delta V_{C\_ESR} = I_{SWPEAK} \times R_{C\_ESR} \quad (19)$$

NEGATIVE CHARGE PUMP VOLTAGE REGULATOR CONTROL (V_{GL})

The negative charge pump voltage regulator control an external NPN transistor to regulate the V_{GL} output. As typical application circuit Figure 34 illustrated, a one time negative voltage charge pump based on the AV_{DD} boost switching provides the source voltage to the emitter of NPN transistor. Depending on the feedback voltage applied on the VGL pin, A_1 error amplifier regulates the current through Q3. The proportional current mirrored by Q1 to Q2 sends to the base of NPN transistor from DRVN pin. Therefore, the regulation is achieved by controlled voltage drop between collector and emitter of NPN transition.

Normally the negative charge pump regulator is to provide gate OFF voltage to the gate driver or level shift. In additional, for positive and negative AV_{DD} application, it can also be used for negative AV_{DD} regulating. Because of charge bump voltage loss, it is recommended to leave enough voltage guard band (for example, 1 V for 50-mA load) between positive AV_{DD} to negative AV_{DD}.

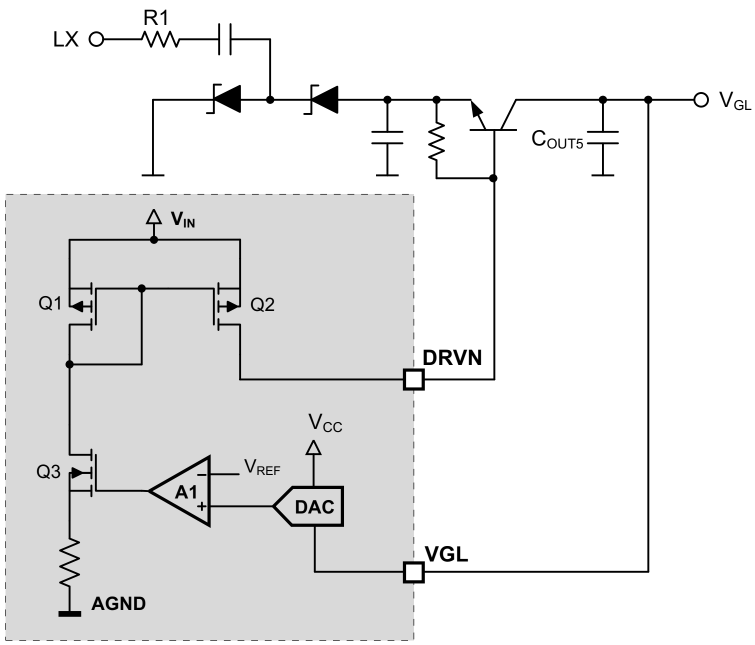


Figure 34. Negative Charge Pump Block Diagram

Output Voltage (Negative Charge Pump)

Negative charge pump's output voltage can be programmed from –8 V to –3.8 V using the **VGL** register.

Start-Up (Negative Charge Pump)

Negative charge pump is enabled together with booster converter 2 when AVDD has finished ramping to its programmed voltage.

The same ramp rate is shared for both boost converter 2 and negative charge pump regulator. The negative charge pump regulator ramps V_{GL} to its programmed value from 0V in t_{SS4} seconds. The value of t_{SS4} can be programmed from 4 ms to 16 ms using the **SS4** bits in **VGHCONFIG** register.

NPN Transistor Selection (Negative Charge Pump)

The NPN transistor used to regulator V_{GL} or Negtive AV_{DD} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able withstand voltages up to V_{IN} across its collector-emitter (V_{CE}).

The power dissipated in the transistor is given by Equation 20. The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends on adequate PCB thermal design.

$$P_Q = [V_{IN} - (2 \times V_F) - |V_{GL}|] \times I_{GL} \quad (20)$$

Where I_{GL} is the mean (not RMS) output current drawn from the charge pump.

Diode Selection (Negative Charge Pump)

Small-signal diodes can be used for most low current applications (<50 mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by Equation 21

$$P_D = I_{GL} \times V_F \quad (21)$$

The peak current through the diode occurs during start-up and for a few cycles may be as high as a few amps. However, this condition typically lasts for <1 ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to at least 2 × V_{IN}.

Capacitor Selecion (Negative Charge Pump)

For the lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and 1 µF to 10 µF is suitable for most applications. Large capacitors provide better performance in applications where large load transient currents are present.

A flying capacitor in the range of 100 nF to 1 µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages or currents, or both, to be achieved. Smaller values tend to be physically smaller and cheaper.

OVER-VOLTAGE AND UNDER-VOLTAGE PROTECTION (AV_{DD}, V_{25}, V_{GH})

Each voltage regulator output is protected against under-voltages and over-voltages.

Over-voltage conditions are detected if AV_{DD} output rises over typical 15 V or V_{GH} output rises over typical 39 V, in which cases the AV_{DD} boost switch or VGH boost switch will be turned off until the overvoltage conditions is removed.

Undervoltage conditions are detected if a regulator output falls below certain level of its programmed voltage for longer than a time period, in which case the relevant voltage regulator is disabled. To recover normal operation following an under-voltage condition, the cause of the error condition must be removed and the supply voltage V_{IN} cycled.

Table 1. Under Voltage Protection

UVP	ERROR CONDITION	TIME PERIOD	PROTECT BEHAVIOR	RECOVERY CONDITION
V_{25}	< 1 V	> 160 ms	V_{25} buck converter or LDO, AV_{DD} boost converter, V_{GH} boost converter and V_{GL} regulator are disabled. $\overline{RESET}$ pin is pulled low.	Error condition is removed and V_{IN} is cycled (POR).
AV_{DD}	< 80%	> 160 ms	AV_{DD} boost converter, V_{GH} boost convert and V_{GL} voltage regulator are disabled.	Error condition is removed and V_{IN} is cycled (POR).
V_{GH}	< 80%	> 160 ms	V_{GH} boost converter is disabled.	Error condition is removed and V_{IN} is cycled (POR).

RESET GENERATOR

The $\overline{RESET}$ pin generates an active-low reset signal for the T-CON (see Figure 35). During power-up the reset timer (t_{RESET}) starts when V_{25} has finished ramping. The reset pulse duration can be programmed from 0 ms to 30 ms using the **RESET** register.

The $\overline{RESET}$ output is an open-drain type that requires an external pull-up resistor. Pull-up resistor values in the range 10 kΩ to 100 kΩ are recommended for most applications.

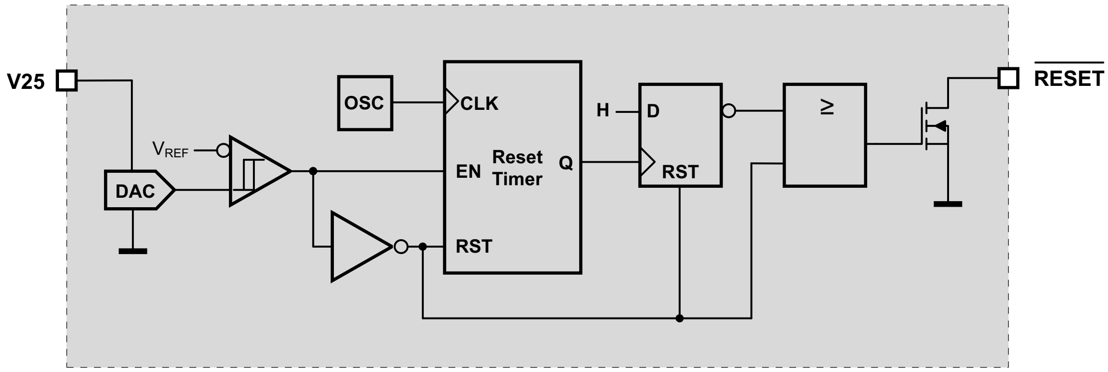


Figure 35. Reset Internal Block Diagram

GATE VOLTAGE SHAPING

The gate voltage shaping function can be used to reduce image sticking in LCD panels by modulating the LCD panel's gate ON voltage (VGH). Figure 36 shows a block diagram of the gate voltage shaping function and Figure 37 shows the typical waveforms during operation.

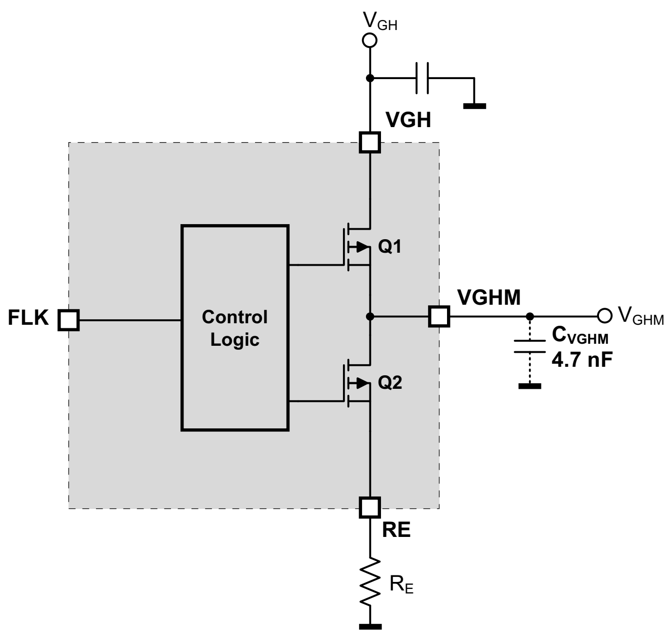


Figure 36. Gate Voltage Shaping Block Diagram

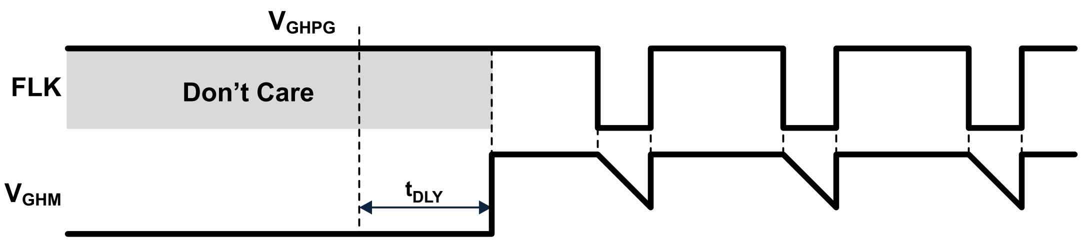


Figure 37. Gate Voltage Shaping Waveforms

Gate voltage shaping is controlled by the FLK input. When FLK is high, Q_1 is on, Q_2 is off, and V_{GHM} is equal to V_{GH}. On the falling edge of FLK, Q_1 is turned off, Q_2 is turned on, and the LCD panel load connected to the VGHM pin discharges through the external resistor connected to the RE pin.

During power-up Q_2 is held permanently on and Q_1 permanently off, regardless of the state of the FLK signal, until t_{DLY} milliseconds after boost converter 2 (V_{GH}) has finished ramping. The value of t_{DLY} can be programmed from 0ms to 60ms using the **DLY** register.

During power-down Q_2 is held permanently on and Q1 permanently off, regardless of the state of the FLK signal.

PROGRAMMABLE V_{COM} CALIBRATOR (V_{COM})

The programmable VCOM calibrator uses a DAC to generate an offset Voltage for LCD panel common voltage reference.

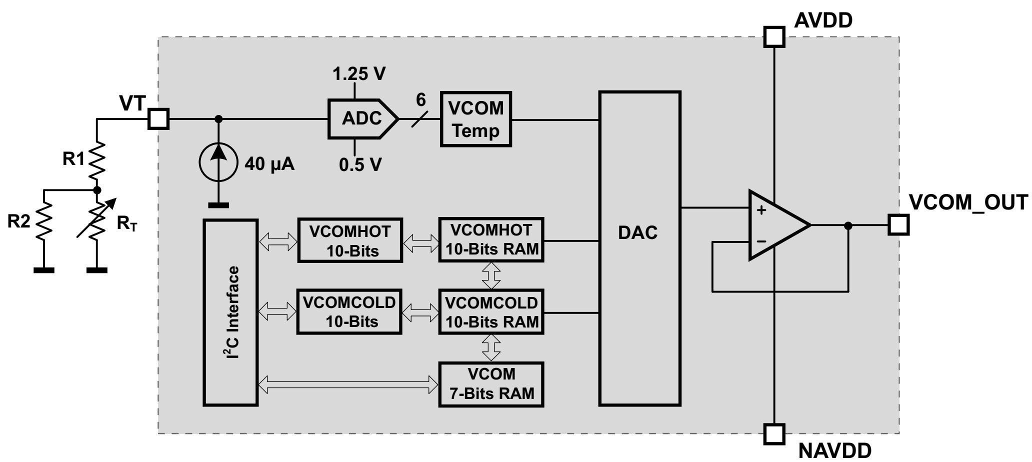


Figure 38. Programmable V_{COM} Calibrator Block Diagram

The VCOM voltage calibration needs two steps for adjustment.

First step is to set the central value of V_{COM} voltage according to the AV_{DD}, V_{GH} and LCD panel characteristic. The VCOM voltage is programmable from 1.5 V to 5.0 V or –4 V to 0.8 V by **VCOMHOT** register. The first step is normally done by PCB assembly manufacturer.

Second step is to calibrate the V_{COM} voltage on the LCD panel assembly line by **VCOM** RAM register through I^2C digital interface. The **VCOM** register value indicates the voltage increment or decrement of VCOM_OUT which is preset by **VCOMHOT**. Once the proper value is identified, the VCOM_OUT voltage value can be renewed with **VCOM** register value added. The default value for VCOM register is **1000000**. If 1000001 is written into **VCOM** register, the VCOM_OUT voltage will increase with one DAC step, 10mV. In the other hand if 0111111 is written to **VCOM** register, the VCOM_OUT voltage will decrease with one DAC step, 10 mV.

The VCOM voltage also supports temperature compensation and allows its output voltage to transition from a lower voltage at low temperatures $V_{COMCOLD}$ to a higher voltage at high temperatures V_{COMHOT} (see Figure 39). The temperature compensation for VCOM could be turn on/off by bit **VCOMT** in register **CONFIG**. If temperature compensation for VCOM is ON state, both **VCOMHOT** and **VCOMCOLD** need to be input. Otherwise only **VCOMHOT** is active for VCOM voltage setting without temperature compensation.

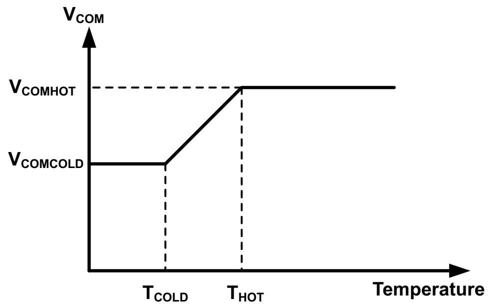


Figure 39. V_{COM} Temperature Compensation Characteristic

OPERATIONAL AMPLIFIERS

Like most operational amplifiers, the V_{COM} amplifiers are not designed to drive purely capacitive loads, so it is not recommended to connect a capacitor directly to their outputs in an attempt to increase performance; however, the amplifiers are capable of delivering high peak currents that make such capacitors unnecessary.

To optimize performance, the V_{COM} amplifiers' positive supplies are connected internally to the AVDD pin and negative supplies are connected internally to NAVDD pin (See Figure 40 for operational amplifier internal block diagram).

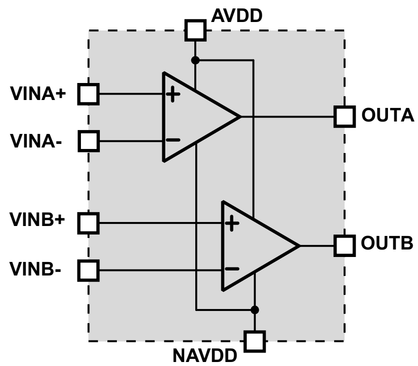


Figure 40. Operational Amplifier Block Diagram

The two integrated operational amplifiers are able to be disabled for non-used application to minimize the power consumption. Setting the **OPA_A** bit or **OPA_B** bit in **CONFIG** register can turn on/off operational amplifier A or B individually.

To minimize the addtional power dissipated when operational amplifier is turned off, it is recommanded to short the both inverter input and non-inverter input to same voltage bias or leave them floating.

CONFIGURATION PARAMETERS

The TPS65640 divides the configuration parameters into two categories:

- VCOM calibration
- All other configuration parameters

In typical applications, all configuration parameters except VCOM are programmed by the subcontractor during PCB assembly, and VCOM is programmed by the display manufacturer during display calibration.

RAM and E^2PROM

Configuration parameters can be changed by writing the desired values to the appropriate RAM register or registers. The RAM registers are volatile and their contents are lost when power is removed from the device. By writing to the Control Register, it is possible to store the active configuration in non-volatile E^2PROM so that it will subsequently be used as the default setting upon when the device is powered up.

Configuration Parameters (Excluding VCOM Calibration)

Table 2 shows the memory map of the configuration parameters.

Table 2. Configuration Memory Map

Register Address	Register Name	Factory Default	Description
00h	CONFIG	FAh	Sets function control bits
01h	AVDD	3Ah	Sets the output voltage of AVDD boost converter
02h	AVDDCONFIG	0Ah	Sets miscellaneous configuration bits for AVDD boost converter
03h	VGHHOT	09h	Sets the output voltage of VGH boost converter at high temperatures (VGHT = 0) or VGH boost converter (VGHT=1)
04h	VGHCOLD	09h	Sets the output voltage of VGH boost converter at low temperatures (VGHT=0)
05h	VGHCONFIG	02h	Sets miscellaneous configuration bits for VGH boost converter
06h	VGL	1Fh	Sets the output voltage of VGL linear regulator
07h	V25	0Ah	Sets the output voltage of buck converter.
08h	VDIV	01h	Sets the threshold of the /RST signals
09h	RESET	06h	Sets the reset pulse duration
0Ah	DLY	01h	Sets the gate voltage shaping delay
0Bh	VCOMHOT	5Fh	Presets the output voltage of VCOM reference at high temperatures (VCOMT = 0) or VCOM reference (VCOMT=1)
0Ch	VCOMCOLD	5Fh	Presets the output voltage of VCOM reference at low temperatures (VCOMT=0)
FFh	Control	00h	Controls whether read and write operations access RAM or E^2PROM registers

CONFIG (00h)

The **CONFIG** register can be written to and read from.

Table 3. CONFIG Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOMR	**VCOMT**	**OPA_B**	**OPA_A**	**BUCK/LDO**	**VGL**	**VGHT**	**VGH**

VGH	Bit 0	This bit enables/disables the boost converter for VGH voltage regulator.	
		0	Enables the VGH boot converter
		1	Disables the VGH boost converter
VGHT	Bit 1	This bit enables/disables the temperature compensation for VGH regulator.	
		0	Enables the temperature compensation for VGH voltage regulator
		1	Disables the temperature compensation for VGH voltage regulator
VGL	Bit 2	This bit enables/disables the VGL linear voltage regulator.	
		0	Enables the VGL linear voltage regulator
		1	Disables the VGL linear voltage regulator
BUCK/LDO	Bit 3	This bit selects the operation mode for V25 voltage regulator.	
		0	Selects the Buck converter for V25 voltage regulator
		1	Selects the LDO for V25 voltage regulator
OPA_A	Bit 4	This bit enables/disables the OPA_A operational amplifier.	
		0	Enables the OPA_A operational amplifier
		1	Disables the OPA_A operational amplifier
OPA_B	Bit 5	This bit enables/disables the OPA_B operational amplifier.	
		0	Enables the OPA_B operational amplifier
		1	Disables the OPA_B operational amplifier
VCOMT	Bit 6	This bit enables/disables the temperature compensation for VCOM voltage	
		0	Enables the temperature compensation for VCOM voltage
		1	Disables the temperature compensation for VCOM voltage
VCOMR	Bit 7	This bit sets the V_{COM} voltage output range	
		0	V_{COM} = 0.8 V ~ 5 V for full AV_{DD} Application
		1	V_{COM} = –4.1 V ~ 0.2 V for PN AV_{DD} Application

AVDD (01h)

The **AVDD** register can be written to and read from.

Table 4. AVDD Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	**AVDD**						

AVDD Bits 6-0: These bits select boost converter 1's output voltage (AVDD)

0000000	N.A.	1000010	AV_{DD} = 6.6 V	1100010	AV_{DD} = 9.8 V
……	N.A.	1000011	AV_{DD} = 6.7 V	1100011	AV_{DD} = 9.9 V
0100100	AV_{DD} = 3.6 V	1000100	AV_{DD} = 6.8 V	1100100	AV_{DD} = 10.0 V
0100101	AV_{DD} = 3.7 V	1000101	AV_{DD} = 6.9 V	1100101	AV_{DD} = 10.1 V
0100110	AV_{DD} = 3.8 V	1000110	AV_{DD} = 7.0 V	1100110	AV_{DD} = 10.2 V
0100111	AV_{DD} = 3.9 V	1000111	AV_{DD} = 7.1 V	1100111	AV_{DD} = 10.3 V
0101000	AV_{DD} = 4.0 V	1001000	AV_{DD} = 7.2 V	1101000	AV_{DD} = 10.4 V
0101001	AV_{DD} = 4.1 V	1001001	AV_{DD} = 7.3 V	1101001	AV_{DD} = 10.5 V
0101010	AV_{DD} = 4.2 V	1001010	AV_{DD} = 7.4 V	1101010	AV_{DD} = 10.6 V
0101011	AV_{DD} = 4.3 V	1001011	AV_{DD} = 7.5 V	1101011	AV_{DD} = 10.7 V
0101100	AV_{DD} = 4.4 V	1001100	AV_{DD} = 7.6 V	1101100	AV_{DD} = 10.8 V
0101101	AV_{DD} = 4.5 V	1001101	AV_{DD} = 7.7 V	1101101	AV_{DD} = 10.9 V
0101110	AV_{DD} = 4.6 V	1001110	AV_{DD} = 7.8 V	1101110	AV_{DD} = 11.0 V
0101111	AV_{DD} = 4.7 V	1001111	AV_{DD} = 7.9 V	1101111	AV_{DD} = 11.1 V
0110000	AV_{DD} = 4.8 V	1010000	AV_{DD} = 8.0 V	1110000	AV_{DD} = 11.2 V
0110001	AV_{DD} = 4.9 V	1010001	AV_{DD} = 8.1 V	1110001	AV_{DD} = 11.3 V
0110010	AV_{DD} = 5.0 V	1010010	AV_{DD} = 8.2 V	1110010	AV_{DD} = 11.4 V
0110011	AV_{DD} = 5.1 V	1010011	AV_{DD} = 8.3 V	1110011	AV_{DD} = 11.5 V
0110100	AV_{DD} = 5.2 V	1010100	AV_{DD} = 8.4 V	1110100	AV_{DD} = 11.6 V
0110101	AV_{DD} = 5.3 V	1010101	AV_{DD} = 8.5 V	1110101	AV_{DD} = 11.7 V
0110110	AV_{DD} = 5.4 V	1010110	AV_{DD} = 8.6 V	1110110	AV_{DD} = 11.8 V
0110111	AV_{DD} = 5.5 V	1010111	AV_{DD} = 8.7 V	1110111	AV_{DD} = 11.9 V
0111000	AV_{DD} = 5.6 V	1011000	AV_{DD} = 8.8 V	1111000	AV_{DD} = 12.0 V
0111001	AV_{DD} = 5.7 V	1011001	AV_{DD} = 8.9 V	1111001	AV_{DD} = 12.1 V
0111010	AV_{DD} = 5.8 V	1011010	AV_{DD} = 9.0 V	1111010	AV_{DD} = 12.2 V
0111011	AV_{DD} = 5.9 V	1011011	AV_{DD} = 9.1 V	1111011	AV_{DD} = 12.3 V
0111100	AV_{DD} = 6.0 V	1011100	AV_{DD} = 9.2 V	1111100	AV_{DD} = 12.4 V
0111101	AV_{DD} = 6.1 V	1011101	AV_{DD} = 9.3 V	1111101	AV_{DD} = 12.5 V
0111110	AV_{DD} = 6.2 V	1011110	AV_{DD} = 9.4 V	1111110	AV_{DD} = 12.6 V
0111111	AV_{DD} = 6.3 V	1011111	AV_{DD} = 9.5 V	1111111	AV_{DD} = 12.7 V
1000000	AV_{DD} = 6.4 V	1100000	AV_{DD} = 9.6 V		
1000001	AV_{DD} = 6.5 V	1100001	AV_{DD} = 9.7 V		

AVDDCONFIG (02h)

The **AVDDCONFIG** register can be written to and read from.

Table 5. AVDDCONFIG Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	**AVDD ILIM**	**SSI**		**FREQ1**		**LX1TS**	

LX1TS	Bit 1-0	These bits configure the falling speed of AVDD boost switch.	
		00	Tf = 0.5 V/ns
		01	Tf = 0.7 V/ns
		10	Tf = 0.9 V/ns
		11	Tf = 1.1 V/ns
FREQ1	Bit 3-2	These bits configure the switching frequency of AVDD boost.	
		00	f_{LX} = 600 kHz
		01	f_{LX} = 800 kHz
		10	f_{LX} = 1000 kHz
		11	fL_{X} = 1200 kHz
SSI	Bit 5-4	These bits configure the soft start duration for AVDD boost regulator	
		00	t_{SS1} = 20 ms
		01	t_{SS1} = 40 ms
		10	t_{SS1} = 60 ms
		11	t_{SS1} = 80 ms
AVDD ILIM	Bit 6	This bit select the AVDD boost current limite value	
		0	I_{LIM} = 1 A
		1	I_{LIM} = 2 A
Reserved	Bits 7	This bit is reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.	

VGHHOT (03h)

The **VGHHOT** register can be written to and read from.

Table 6. VGHHOT Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			**VGHHOT**				

VGHHOT	Bits 4-0	These bits select VGH output voltage at hot temperatures (VGHT=0) or all temperature range (VGHT=1).			
		00000	N.A.	10000	V_{GHHOT} = 22 V
		00001	N.A.	10001	V_{GHHOT} = 23 V
		00010	N.A.	10010	V_{GHHOT} = 24 V
		00011	N.A.	10011	V_{GHHOT} = 25 V
		00100	N.A.	10100	V_{GHHOT} = 26 V
		00101	N.A.	10101	V_{GHHOT} = 27 V
		00110	N.A.	10110	V_{GHHOT} = 28 V
		00111	N.A.	10111	V_{GHHOT} = 29 V
		01000	N.A.	11000	V_{GHHOT} = 30 V
		01001	V_{GHHOT} = 15 V	11001	V_{GHHOT} = 31 V
		01010	V_{GHHOT} = 16 V	11010	V_{GHHOT} = 32 V
		01011	V_{GHHOT} = 17 V	11011	V_{GHHOT} = 33 V
		01100	V_{GHHOT} = 18 V	11100	V_{GHHOT} = 34 V
		01101	V_{GHHOT} = 19 V	11101	V_{GHHOT} = 35 V
		01110	V_{GHHOT} = 20 V	11110	V_{GHHOT} = 36 V
		01111	V_{GHHOT} = 21 V	11111	V_{GHHOT} = 37 V
Reserved	Bits 7-5	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.			

VGHCOLD (04h)

The **VGHCOLD** register can be written to and read from.

Table 7. VGHCOLD Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			**VGHCOLD**				

VGHCOLD	Bits 4-0	These bits select VGH output voltage at cold temperatures (VGHT=0)			
		00000	N.A.	10000	V_{GHCOLD} = 22 V
		00001	N.A.	10001	V_{GHCOLD} = 23 V
		00010	N.A.	10010	V_{GHCOLD} = 24 V
		00011	N.A.	10011	V_{GHCOLD} = 25 V
		00100	N.A.	10100	V_{GHCOLD} = 26 V
		00101	N.A.	10101	V_{GHCOLD} = 27 V
		00110	N.A.	10110	V_{GHCOLD} = 28 V
		00111	N.A.	10111	V_{GHCOLD} = 29 V
		01000	N.A.	11000	V_{GHCOLD} = 30 V
		01001	V_{GHCOLD} = 15 V	11001	V_{GHCOLD} = 31 V
		01010	V_{GHCOLD} = 16 V	11010	V_{GHCOLD}= 32 V
		01011	V_{GHCOLD} = 17 V	11011	V_{GHCOLD} = 33 V
		01100	V_{GHCOLD} = 18 V	11100	V_{GHCOLD} = 34 V
		01101	V_{GHCOLD} = 19 V	11101	V_{GHCOLD} = 35 V
		01110	V_{GHCOLD} = 20 V	11110	V_{GHCOLD}= 36 V
		01111	V_{GHCOLD} = 21 V	11111	V_{GHCOLD} = 37 V
Reserved	Bits 7-5	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.			

VGHCONFIG (05h)

The VGHMISC register can be written to and read from.

Table 8. VGHCONFIG Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			**FREQ4**	**SS4**		**LX4TS**	

LX4TS	Bit 1-0	These bits configure the falling speed of VGH boost switch.	
		00	Tf = 2.2 V/ns
		01	Tf = 3.5 V/ns
		10	Tf = 4.8 V/ns
		11	Tf = 6 V/ns
SS4	Bit 3-2	These bits configure the soft start duration for VGH boost regulator	
		00	t_{SS4} = 4 ms
		01	t_{SS4} = 8 ms
		10	t_{SS4} = 12 ms
		11	t_{SS4} = 16 ms
FREQ4	Bit 4	This bit configures the switching frequency of VGH boost regulator	
		0	F_{VGH_LX} = 400 kHz
		1	F_{VGH_LX} = 800 kHz
Reserved	Bits 7-5	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.	

VGL (06h)

The **VGL** register can be written to and read from.

Table 9. VGL Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		**VGL**					

VGL	Bits 5-0	These bits select VGL output voltage					
		000000	N.A.	010110	V_{GL} = –3.9 V	101100	V_{GL} = –6.1 V
		000001	N.A.	010111	V_{GL} = –4.0 V	101101	V_{GL} = –6.2 V
		000010	N.A.	011000	V_{GL} = –4.1 V	101110	V_{GL} = –6.3 V
		000011	N.A.	011001	V_{GL} = –4.2 V	101111	V_{GL} = –6.4 V
		000100	N.A.	011010	V_{GL} = –4.3 V	110000	V_{GL} = –6.5 V
		000101	N.A.	011011	V_{GL} = –4.4 V	110001	V_{GL} = –6.6 V
		000110	N.A.	011100	V_{GL} = –4.5 V	110010	V_{GL} = –6.7 V
		000111	N.A.	011101	V_{GL} = –4.6 V	110011	V_{GL} = –6.8 V
		001000	N.A.	011110	V_{GL} = –4.7 V	110100	V_{GL} = –6.9 V
		001001	N.A.	011111	V_{GL} = –4.8 V	110101	V_{GL} = –7.0 V
		001010	N.A.	100000	V_{GL} = –4.9 V	110110	V_{GL} = –7.1 V
		001011	N.A.	100001	V_{GL} = –5.0 V	110111	V_{GL} = –7.2 V
		001100	N.A.	100010	V_{GL} = –5.1 V	111000	V_{GL} = –7.3 V
		001101	N.A.	100011	V_{GL} = –5.2 V	111001	V_{GL} = –7.4 V
		001110	N.A.	100100	V_{GL} = –5.3 V	111010	V_{GL} = –7.5 V
		001111	N.A.	100101	V_{GL} = –5.4 V	111011	V_{GL} = –7.6 V
		010000	N.A.	100110	V_{GL} = –5.5 V	111100	V_{GL} = –7.7 V
		010001	N.A.	100111	V_{GL} = –5.6 V	111101	V_{GL} = –7.8 V
		010010	N.A.	101000	V_{GL} = –5.7 V	111110	V_{GL} = –7.9 V
		010011	N.A.	101001	V_{GL} = –5.8 V	111111	V_{GL} = –8.0 V
		010100	N.A.	101010	V_{GL} = –5.9 V		
		010101	V_{GL} = –3.8 V	101011	V_{GL} = –6.0 V		
Reserved	Bits 7-6	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.					

V25 (07h)

The **V25** register can be written to and read from.

Table 10. V25 Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				**V25**			

V25	Bits 3-0	These bits select V25 buck converter's output voltage			
		0000	V_{25} = 1.5 V	1000	V_{25} = 2.3 V
		0001	V_{25} = 1.6 V	1001	V_{25} = 2.4 V
		0010	V_{25} = 1.7 V	1010	V_{25} = 2.5 V
		0011	V_{25} = 1.8 V	1011	V_{25} = 2.6 V
		0100	V_{25} = 1.9 V	1100	V_{25} = 2.7 V
		0101	V_{25} = 2.0 V	1101	V_{25} = 2.8 V
		0110	V_{25} = 2.1 V	1110	V_{25} = 2.9 V
		0111	V_{25} = 2.2 V	1111	V_{25} = 3.0 V
Reserved	Bits 7-4	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.			

VDIV (08h)

The **VDIV** register can be written to and read from.

Table 11. VDIV Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				**VDIV**			

VDIV	Bits 3-0	These bits select the threshold voltage of the $\overline{RESET}$ signal	
		000	V_{DIV} = 1.2 V
		001	V_{DIV} = 1.4 V
		010	V_{DIV} = 1.6 V
		011	V_{DIV} = 1.8 V
		100	V_{DIV} = 2.0 V
		101	V_{DIV} = 2.2 V
		110	V_{DIV} = 2.4 V
		111	V_{DIV} = 2.6 V
Reserved	Bits 7-4	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.	

RESET (09h)

The **RESET** register can be written to and read from.

Table 12. RESET Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				**RESET**			

RESET	Bits 3-0	These bits select the $\overline{RESET}$ generate delay time period			
		0000	T_{RESET} = 0 ms	1000	T_{RESET} = 16 ms
		0001	T_{RESET} = 2 ms	1001	T_{RESET} = 18 ms
		0010	T_{RESET} = 4 ms	1010	T_{RESET} = 20 ms
		0011	T_{RESET} = 6 ms	1011	T_{RESET} = 22 ms
		0100	T_{RESET} = 8 ms	1100	T_{RESET} = 24 ms
		0101	T_{RESET} = 10 ms	1101	T_{RESET} = 26 ms
		0110	T_{RESET} = 12 ms	1110	T_{RESET} = 28 ms
		0111	T_{RESET} = 14 ms	1111	T_{RESET} = 30 ms
Reserved	Bits 7-4	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.			

DLY (0Ah)

The **DLY** register can be written to and read from.

Table 13. DLY Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						**DLY**	

DLY	Bits 1-0	These bits configure the gate voltage shaping delay time period	
		00	V_{DLY} = 0 ms
		01	V_{DLY} = 20 ms
		10	V_{DLY} = 40 ms
		11	V_{DLY} = 60 ms
Reserved	Bits 7-2	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.	

VCOMHOT (0Bh)

The **VCOMHOT1** register can be written to and read from.

Table 14. VCOMHOT Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOMHOT							

VCOMHOT Bits — These bits select VCOM output voltage at hot temperatures (VCOMT = 0) or all temperature range (VCOMT = 1).

	VCOMR = 0	**VCOMR = 1**
00000000	V_{COMHOT} = N.A	V_{COMHOT} = N.A
00000001	V_{COMHOT} = N.A	V_{COMHOT} = N.A
00000010	V_{COMHOT} = N.A	V_{COMHOT} = N.A
…..	V_{COMHOT} = N.A	V_{COMHOT} = N.A
00100111	V_{COMHOT} = N.A	V_{COMHOT} = N.A
00101000	V_{COMHOT} = 0.80 V	V_{COMHOT} = 0.20 V
00101001	V_{COMHOT} = 0.82 V	V_{COMHOT} = 0.18 V
00101010	V_{COMHOT} = 0.84 V	V_{COMHOT} = 0.16 V
00101011	V_{COMHOT} = 0.86 V	V_{COMHOT} = 0.14 V
10111100	V_{COMHOT} = 0.86 V	V_{COMHOT} = 0.12 V
…..	…..	…..
11111101	V_{COMHOT} = 5.06 V	V_{COMHOT} = –4.06 V
11111110	V_{COMHOT} = 5.08 V	V_{COMHOT} = –4.08 V
11111111	V_{COMHOT} = 5.10 V	V_{COMHOT} = –4.10 V

VCOMCOLD (0Ch)

The **VCOMCOLD** register can be written to and read from.

Table 15. VCOMCOLD Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOMCOLD							

VCOMCOLD Bits — These bits select VCOM output voltage at cold temperatures (VCOMT=0)

	VCOMR = 0	**VCOMR = 1**
00000000	$V_{COMCOLD}$ = N.A	$V_{COMCOLD}$ = N.A
00000001	$V_{COMCOLD}$ = N.A	$V_{COMCOLD}$ = N.A
00000010	$V_{COMCOLD}$ = N.A	$V_{COMCOLD}$ = N.A
…..	$V_{COMCOLD}$ = N.A	$V_{COMCOLD}$ = N.A
00100111	$V_{COMCOLD}$ = N.A	$V_{COMCOLD}$ = N.A
00101000	$V_{COMCOLD}$ = 0.80 V	$V_{COMCOLD}$ = 0.20 V
00101001	$V_{COMCOLD}$ = 0.82 V	$V_{COMCOLD}$ = 0.18 V
00101010	$V_{COMCOLD}$ = 0.84 V	$V_{COMCOLD}$ = 0.16 V
00101011	$V_{COMCOLD}$ = 0.86 V	$V_{COMCOLD}$ = 0.14 V
10111100	$V_{COMCOLD}$ = 0.86 V	$V_{COMCOLD}$ = 0.12 V
…..	…..	…..
11111101	$V_{COMCOLD}$ = 5.06 V	$V_{COMCOLD}$ = –4.06 V
11111110	$V_{COMCOLD}$ = 5.08 V	$V_{COMCOLD}$ = –4.08 V
11111111	$V_{COMCOLD}$ = 5.10 V	$V_{COMCOLD}$ = –4.10 V

Control (FFh)

Table 16. Control Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WED	**Reserved**						**RED**

RED	Bit 0	The state of this bit determines whether read operations return the contents of the DAC registers or the contents of the E^{2}PROM	
		0	Read operations return the contents of the DAC registers
		1	Read operations return the contents of the E^{2}PROM
Reserved	Bits 6-1	These bits are reserved for future use. During write operations data intended for these bits is ignored, and during read operations 0 is returned.	
WED	Bit 7	Setting this bit forces the contents of all DAC registers to be copied into E^{2}PROM, thereby making them the default values during power-up. When the contents of all the DAC registers have been written to the E^{2}PROM, the TPS65640 automatically resets this bit.	

Example – Writing to a Single RAM Register

1. Bus master sends START condition.
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65640 acknowledges.
4. Bus master sends address of RAM register (00h).
5. TPS65640 acknowledges.
6. Bus master sends data to be written.
7. TPS65640 acknowledges.
8. Bus master sends STOP condition.

Figure 41. Writing to a Single RAM Register

Example – Writing to Multiple RAM Registers

1. Bus master sends START condition.
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65640 acknowledges.
4. Bus master sends address of first RAM register to be written to (00h).
5. TPS65640 acknowledges.
6. Bus master sends data to be written to first RAM register.
7. TPS65640 acknowledges.
8. Bus master sends data to be written to RAM register at next higher address (auto-increment).
9. TPS65640 acknowledges.
10. Steps (8) and (9) repeated until data for final RAM register has been sent.
11. TPS65640 acknowledges.
12. Bus master sends STOP condition.

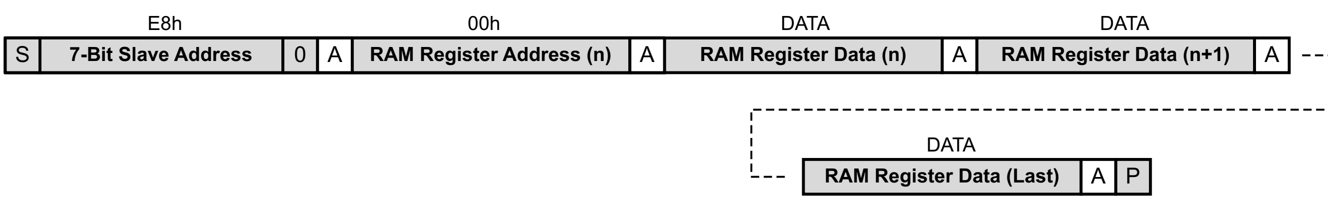


Figure 42. Writing to Multiple RAM Registers

Example – Saving Contents of all RAM Registers to E^2PROM

1. Bus master sends START condition.
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65640 acknowledges.
4. Bus master sends address of Control Register (FFh).
5. TPS65640 acknowledges.
6. Bus master sends data to be written to the Control Register (80h).
7. TPS65640 acknowledges.
8. Bus master sends STOP condition.

	E8h			FFh		80h		
S	7-Bit Slave Address	0	A	Control Register Address	A	Control Register Data	A	P

Figure 43. Saving Contents of all RAM Registers to E^2PROM

The TPS65640 needs 50ms time period after TPS65640 receiving STOP condition for saving all RAM registers data to E^2PROM. If bus master send 7-bit slave address to call TPS65640 again within 50ms period, the TPS65640 will pull down the SCL line to LOW until the all RAM registers data saving to E^2PROM is completed.

Example – Reading from a Single RAM Register

1. Bus master sends START condition.
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65640 acknowledges.
4. Bus master sends address of Control Register (FFh).
5. TPS65640 acknowledges.
6. Bus master sends data for Control Register (00h).
7. TPS65640 acknowledges.
8. Bus master sends STOP condition.
9. Bus master sends START condition.
10. Bus master sends 7-bit slave address plus low R/W bit (E8h).
11. TPS65640 acknowledges.
12. Bus master sends address of RAM register (00h).
13. TPS65640 acknowledges.
14. Bus master sends REPEATED START condition.
15. Bus master sends 7-bit slave address plus high R/W bit (E9h).
16. TPS65640 acknowledges.
17. TPS65640 sends RAM register data.
18. Bus master does not acknowledge.
19. Bus master sends STOP condition.

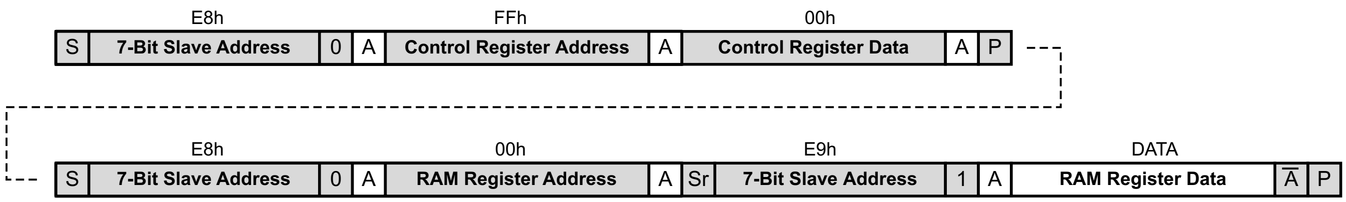


Figure 44. Reading from a Single RAM Register

Example – Reading from a Single E^2PROM Register

1. Bus master sends START condition.
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65640 acknowledges.
4. Bus master sends address of Control Register (FFh).
5. TPS65640 acknowledges.
6. Bus master sends data for Control Register (01h).
7. TPS65640 acknowledges.
8. Bus master sends STOP condition.
9. Bus master sends START condition.
10. Bus master sends 7-bit slave address plus low R/W bit (E8h).
11. TPS65640 acknowledges.
12. Bus master sends address of E^2PROM register (00h).
13. TPS65640 acknowledges.
14. Bus master sends REPEATED START condition.
15. Bus master sends 7-bit slave address plus high R/W bit (E9h).
16. TPS65640 acknowledges.
17. TPS65640 sends E^2PROM register data.
18. Bus master does not acknowledge.
19. Bus master sends STOP condition.

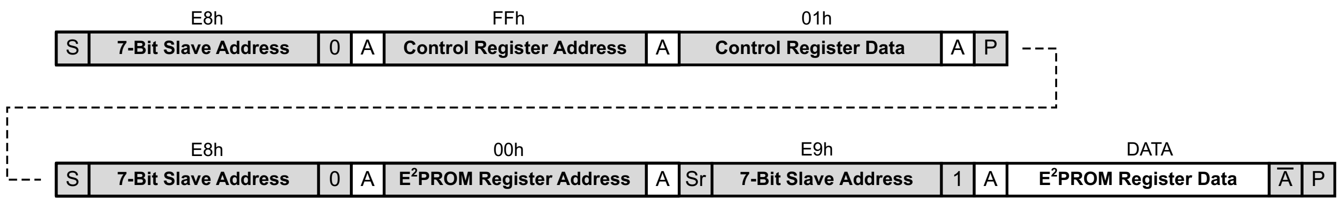


Figure 45. Reading from a Single E^2PROM Register

Example – Reading from Multiple RAM Registers

1. Bus master sends START condition.
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65640 acknowledges.
4. Bus master sends address of Control Register (FFh).
5. TPS65640 acknowledges.
6. Bus master sends data for Control Register (00h).
7. TPS65640 acknowledges.
8. Bus master sends STOP condition.
9. Bus master sends START condition.
10. Bus master sends 7-bit slave address plus low R/W bit (E8h).
11. TPS65640 acknowledges.
12. Bus master sends address of first register to be read (00h).
13. TPS65640 acknowledges.
14. Bus master sends REPEATED START condition.
15. Bus master sends 7-bit slave address plus high R/W bit (E9h).
16. TPS65640 acknowledges.
17. TPS65640 sends contents of first RAM register to be read.
18. Bus master acknowledges.
19. Bus master sends contents of second RAM register to be read.
20. Bus master acknowledges.
21. TPS65640 sends contents of third (last) RAM register to be read.
22. Bus master does not acknowledge.
23. Bus master sends STOP condition.

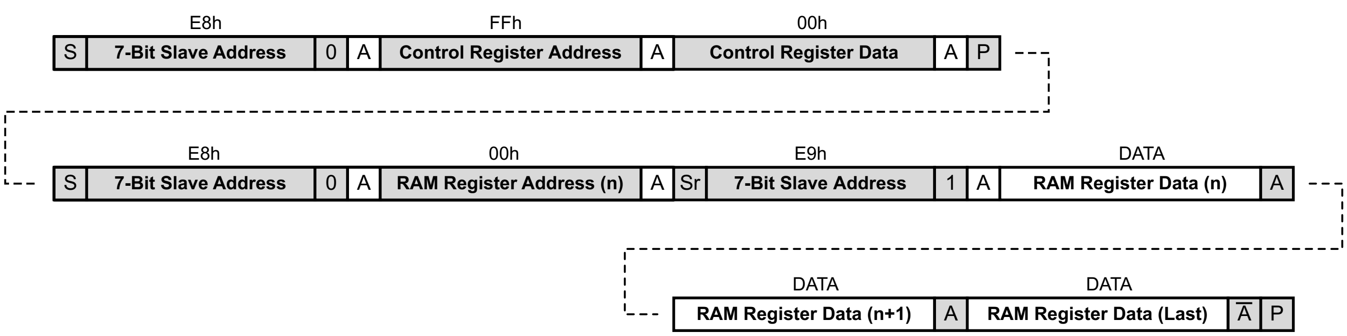


Figure 46. Reading from Multiple RAM Registers

Example – Reading from Multiple E^{2}PROM Registers

1. Bus master sends START condition.
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65640 acknowledges.
4. Bus master sends address of Control Register (FFh).
5. TPS65640 acknowledges.
6. Bus master sends data for Control Register (01h).
7. TPS65640 acknowledges.
8. Bus master sends STOP condition.
9. Bus master sends START condition.
10. Bus master sends 7-bit slave address plus low R/W bit (E8h).
11. TPS65640 acknowledges.
12. Bus master sends address of first E^{2}PROM register to be read (00h).
13. TPS65640 acknowledges.
14. Bus master sends REPEATED START condition.
15. Bus master sends 7-bit slave address plus high R/W bit (E9h).
16. TPS65640 acknowledges.
17. TPS65640 sends contents of first E^{2}PROM register to be read.
18. Bus master acknowledges.
19. Bus master sends contents of second E^{2}PROM register to be read.
20. Bus master acknowledges.
21. TPS65640 sends contents of third (last) E^{2}PROM register to be read.
22. Bus master does not acknowledge.
23. Bus master sends STOP condition.

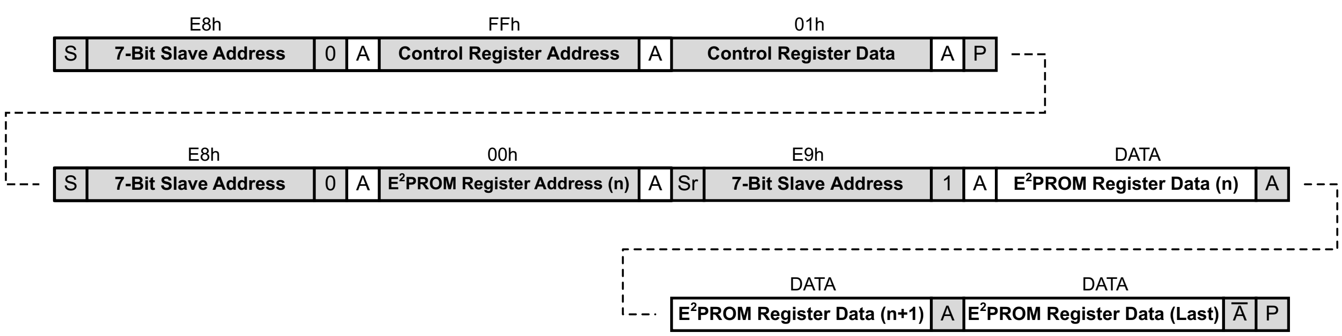


Figure 47. Reading from Multiple E^{2}PROM Registers

Configuration Parameter VCOM

The **VCOM** register can be written to and read from.

Table 17. VCOM Register Bit Allocation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOM							**P**

P	Bit 0	During write operations, this bit determines the target for the data: 0 = Data written to E2PROM and RAM register 1 = Data written to RAM register only During read operations this bit indicates whether the contents of the E2PROM and RAM register are the same 0 = E2PROM and RAM register contents are the same 1 = E2PROM and RAM register contents are different
VCOM	Bits 7-1	During write operations, these bits contain the data to be written. During read operations, these bits return the contents of the RAM. The factory default setting is **1000000.** Where VCOM is a 7-bit integer between 0 and 127 decimal.

Example – Writing a VCOM Value of 77h to VCOM Register Only

1. The bus master sends a START condition.
2. The bus Master sends (9E hexadecimal (7-bit slave address plus low R/W bit).
3. TPS65640 slave acknowledges.
4. The bus master sends EF hexadecimal (data to be written plus LSB = '1').
5. The TPS65640 slave acknowledges.
6. The bus master sends a STOP condition.

	9Eh			EFh			
S	**7-Bit Slave Address**	0	A	**Data to be Written**	1	A	P

Figure 48. Writing a VCOM Value of 77h to RAM Only

Example – Writing a VCOM Value of 77h to E^2PROM and RAM

1. The bus master sends a START condition.
2. The bus Master sends 9E hexadecimal (7-bit slave address plus low R/W bit).
3. TPS65640 slave acknowledges.
4. The bus master sends EE hexadecimal (data to be written plus LSB = '0').
5. The TPS65640 slave acknowledges.
6. The bus master sends a STOP condition.

	9Eh			EEh			
S	**7-Bit Slave Address**	0	A	**Data to be Written**	0	A	P

Figure 49. Writing a VCOM Value of 77h to E^2PROM and RAM

Example – Reading a VCOM Value of 77h from RAM when E^2PROM Contents are Identical

1. The bus master sends a START condition.
2. The bus Master sends 9F hexadecimal (7-bit slave address plus low R/W bit).
3. TPS65640 slave acknowledges.
4. The bus master sends EE hexadecimal from E^2PROM (data to be read plus LSB = '0').
5. The bus master does not acknowledge.
6. The bus master sends a STOP condition.

	9Fh			EEh			
S	**7-Bit Slave Address**	1	A	**Data to be Read**	0	A	P

Figure 50. Reading 77h from RAM when E^2PROM Contents are Identical

Example – Reading a VCOM Value of 77h from RAM when E^2PROM Contents are Different

1. The bus master sends a START condition.
2. The bus Master sends 9F hexadecimal (7-bit slave address plus low R/W bit).
3. TPS65640 slave acknowledges.
4. The bus master sends EF hexadecimal from RAM (data to be read plus LSB = '1').
5. The bus master does not acknowledge.
6. The bus master sends a STOP condition.

	9Fh			EFh			
S	**7-Bit Slave Address**	1	A	**Data to be Read**	1	A	P

Figure 51. Reading 77h from E^2PROM when RAM Contents are Different

I^2C INTERFACE

Configuration parameters and the V_{COM} voltage setting are programmed via an industry standard I^2C serial interface. The TPS65640 always works as a slave device and supports standard (100kbps) and fast (400kbps) modes of operation.

During write operations, all further attempts to access its slave addresses are ignored until the current write operation has completed.

POWER SEQUENCY

Buck converter (V_{25Buck}) or the linear regulator (V_{25LDO}) start as soon as $V_{IN} > V_{UVLO}$.

The reset generator holds $\overline{RST}$ low until t_{RESET} seconds after V_{25} has reached power good status.

Boost converter 1 starts after V_{25} reached power good status.

Boost converter 2 starts as soon as AV_{DD} has reached power good status.

Figure 52 show the typical power-up/down characteristic of the TPS65640.

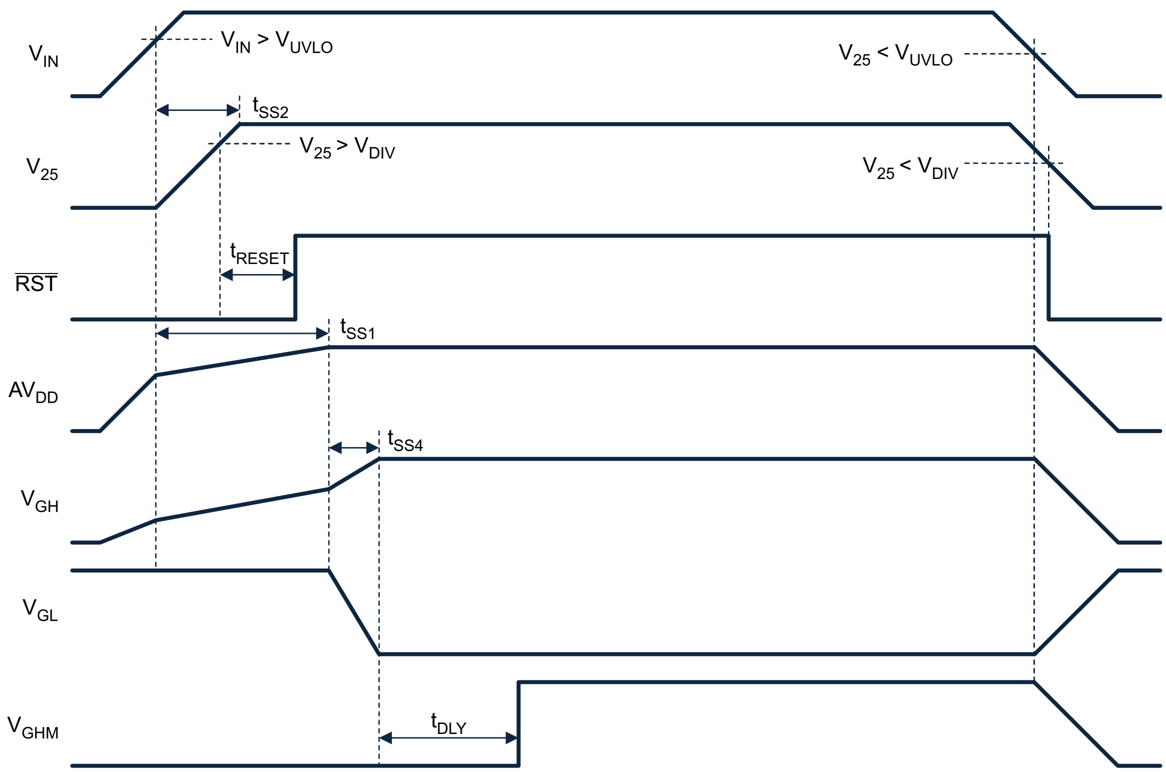


Figure 52. Power-Up and Power-Down Sequencing

UNDERVOLTAGE LOCKOUT

An undervoltage lockout function disables the IC when the supply voltage is too low for proper operation. A low-pass filter at the input of the UVLO comparator ensures that short transients on V_{IN} do not cause premature shutdown of the IC.

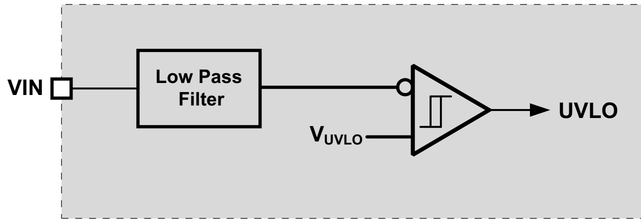


Figure 53. Undervoltage Lockout Comparator with Low-Pass Filter

THERMAL SHUTDOWN

A thermal shutdown function automatically disables all functions if the device's junction temperature exceeds the safe maximum. The device automatically starts operating again once it has cooled down and operation may safely continue. A restart after a thermal shutdown event follows the same sequence as following a normal power-up condition (see Figure 52).

APPLICATION INFORMATION

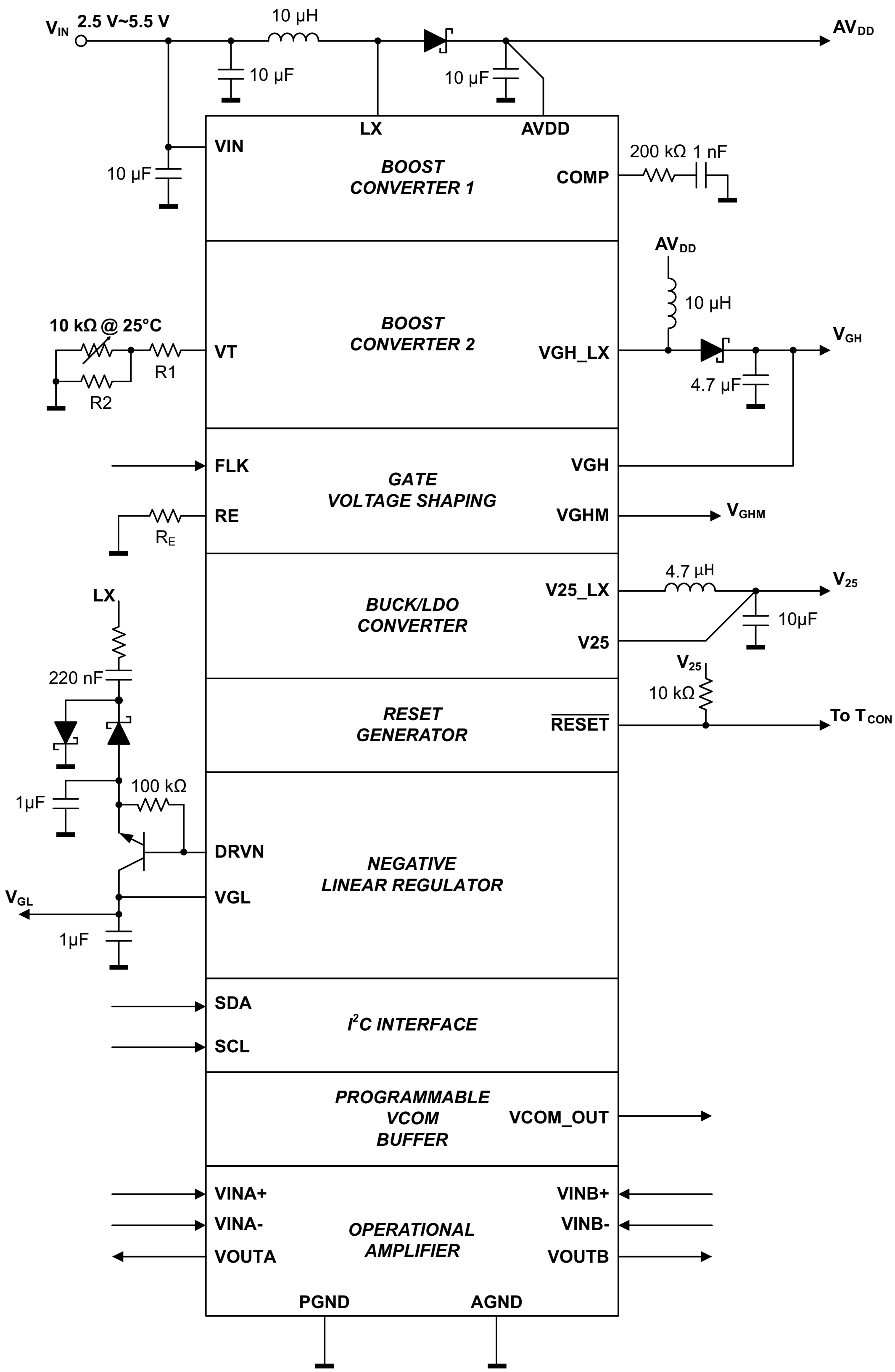
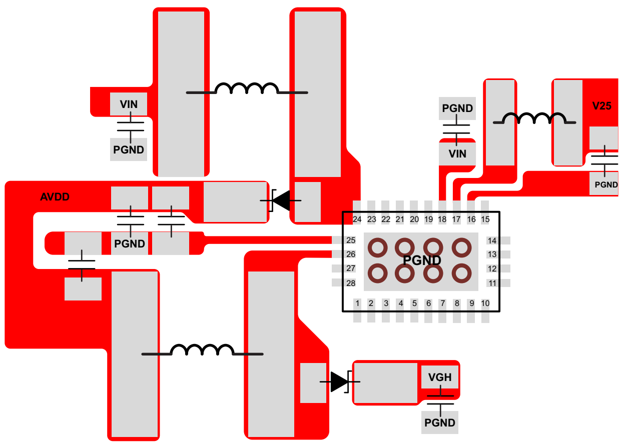


Figure 54. Typical Application Circuit

LAYOUT RECOMMENDATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor in the typical application circuit, should also be placed close to the VIN pin, but also to the GND in order to reduce the input ripple seen by the IC. The LX pin carries high current with fast rising and falling edges. Therefore, the connection between the pin to the inductor and schottky diode should be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor for both Boost converter 1, Boost converter 2 and Buck converter close to the PGND pin since there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point, for example on the thermal pad. The thermal pad needs to be soldered on to the PCB and connected to the GND pin of the IC. An additional thermal via can significantly improve power dissipation of the IC.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65640RHRR	PREVIEW	WQFN	RHR	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PZXI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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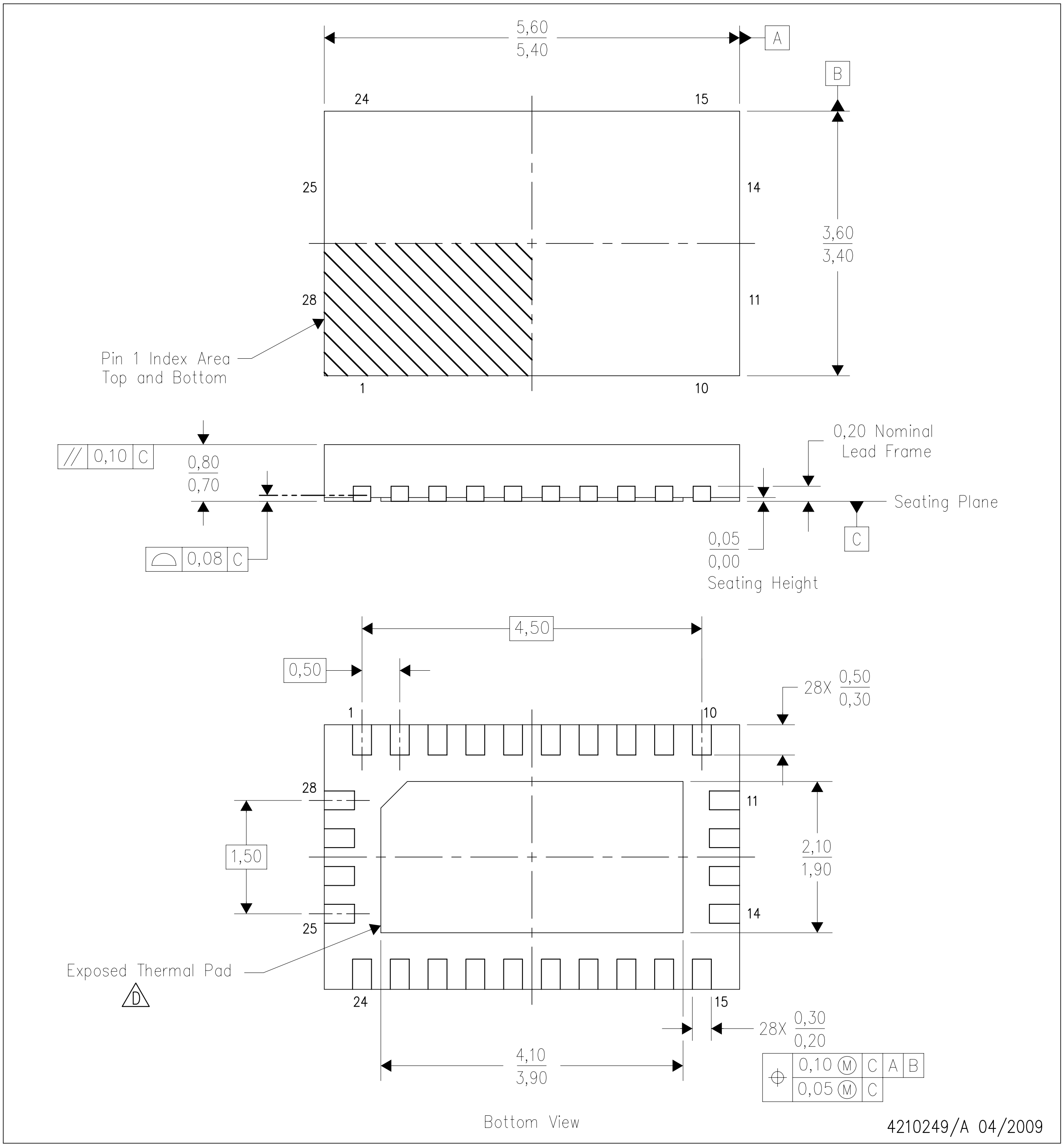
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RHR (R-PWQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. Reference JEDEC MO–220.

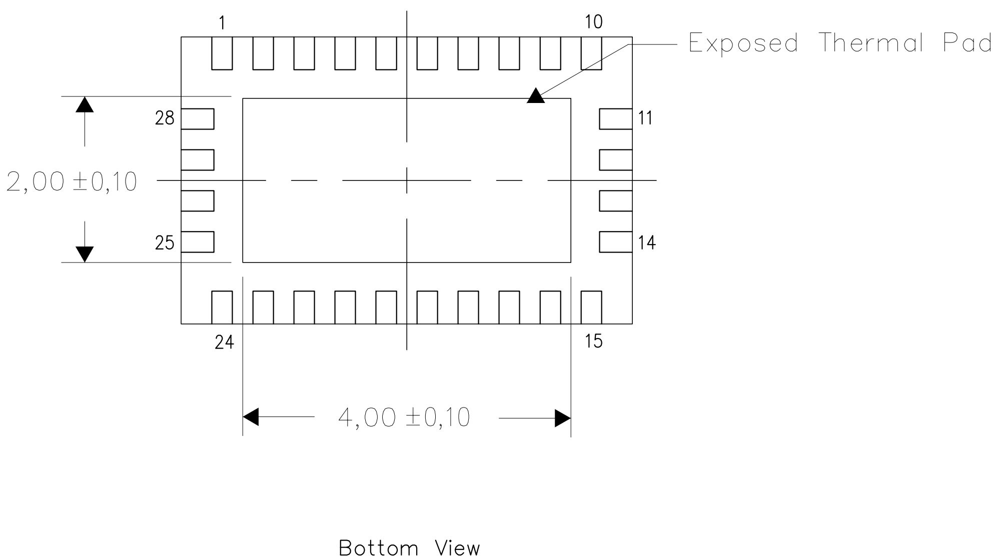
RHR (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4210524/D 04/11

NOTE: A. All linear dimensions are in millimeters

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65640RHRR	ACTIVE	WQFN	RHR	28	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PZXI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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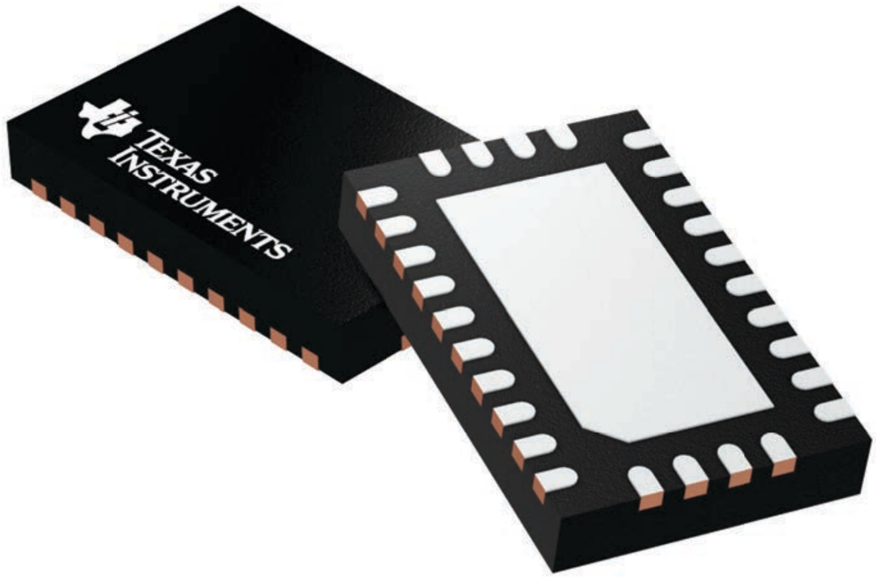
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RHR 28

WQFN - 0.8 mm max height

3.5 x 5.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



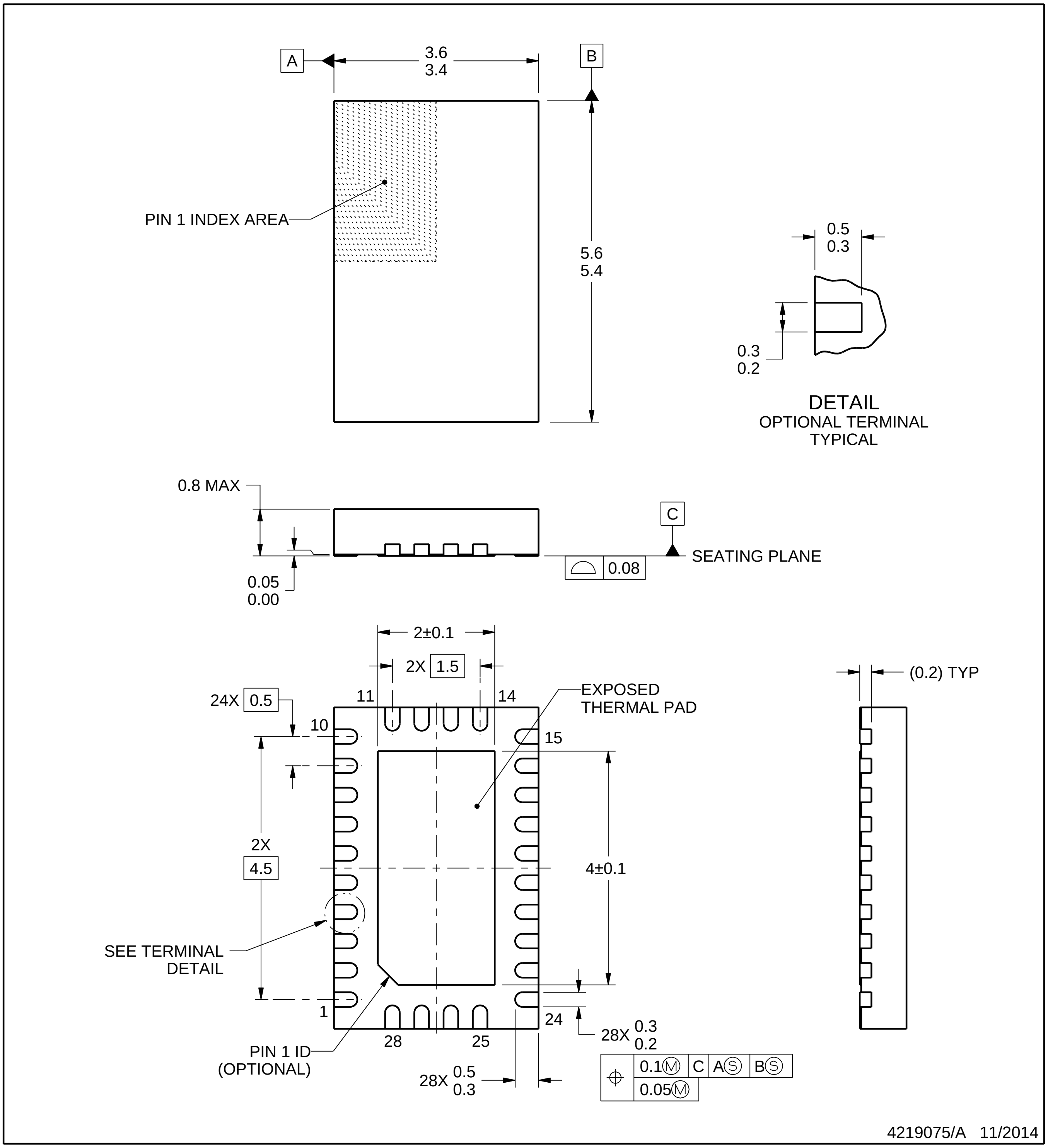
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4210249/B

RHR0028A

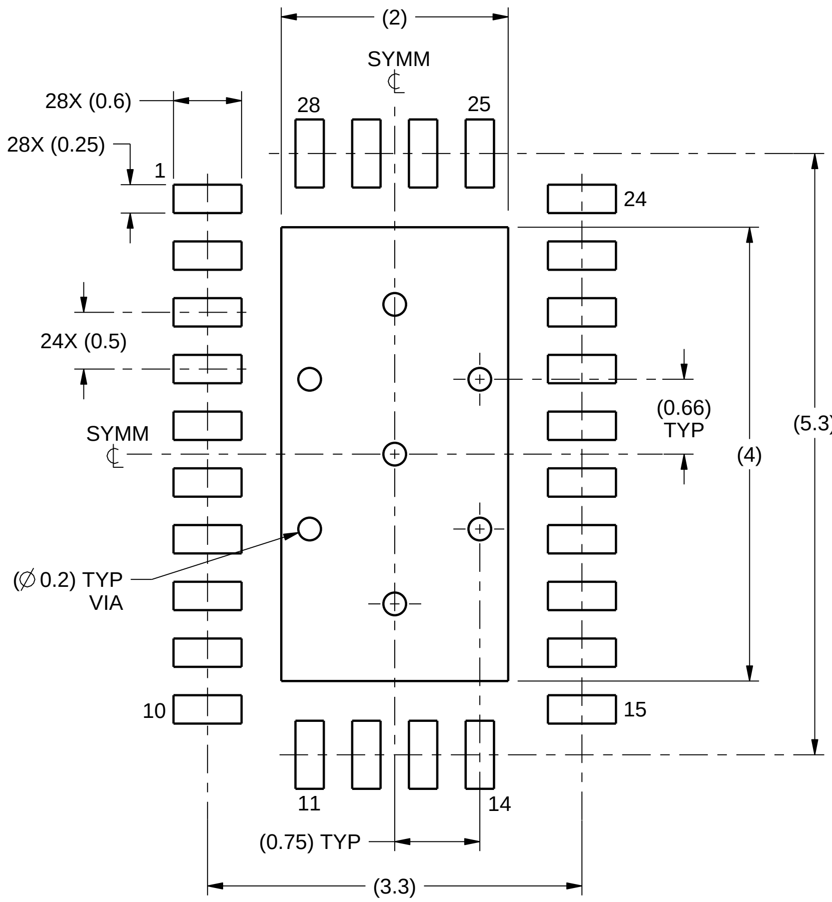
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

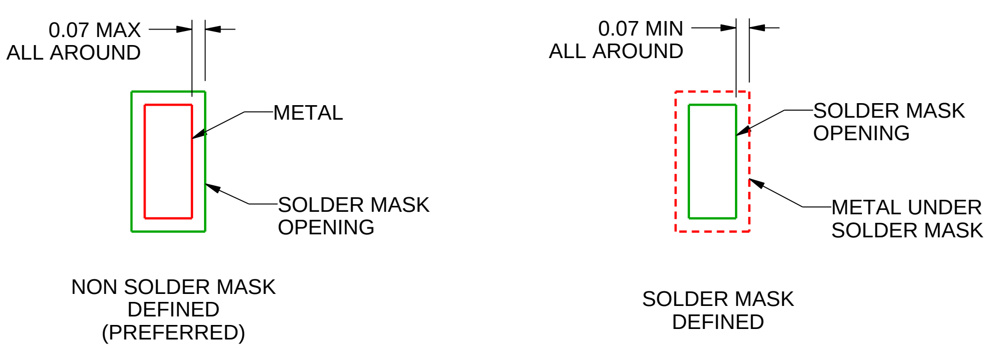


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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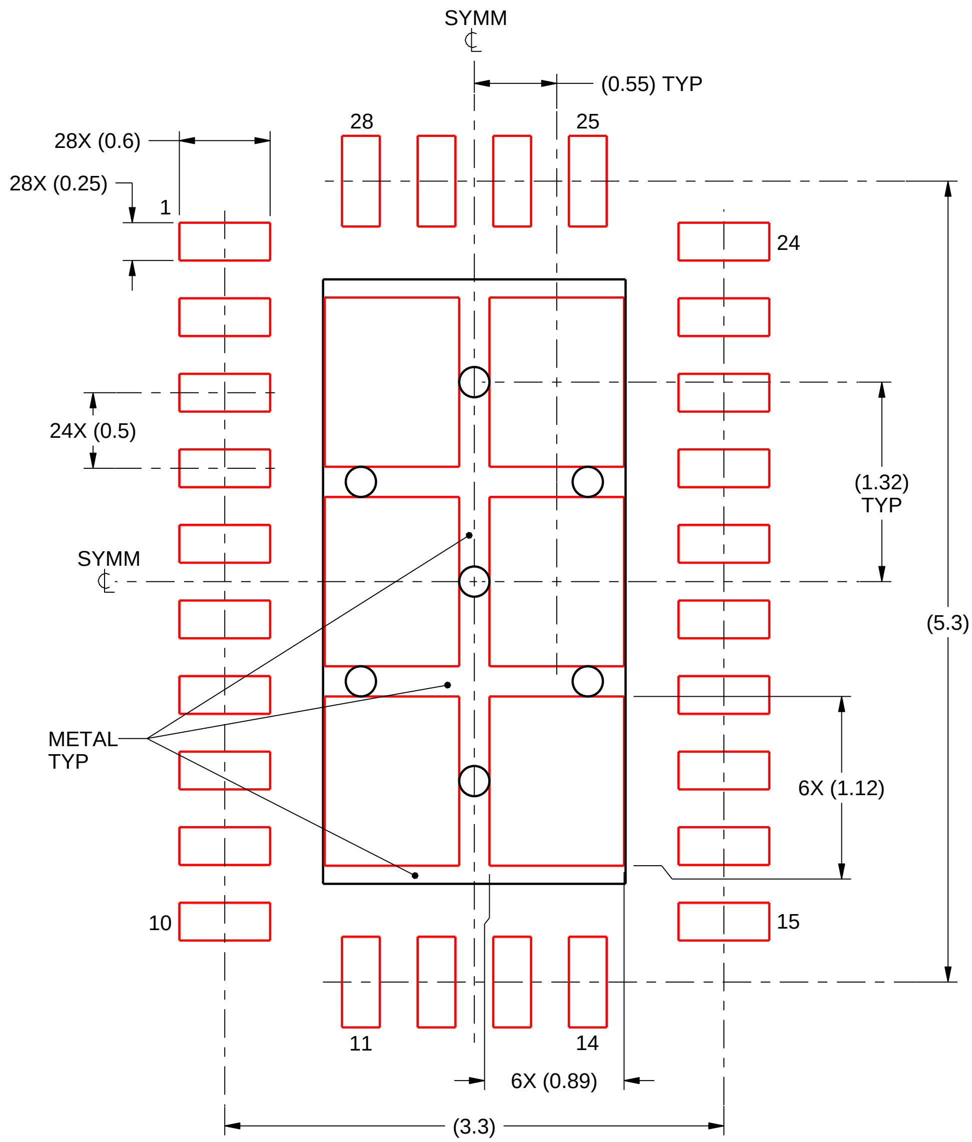
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219075/A 11/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.