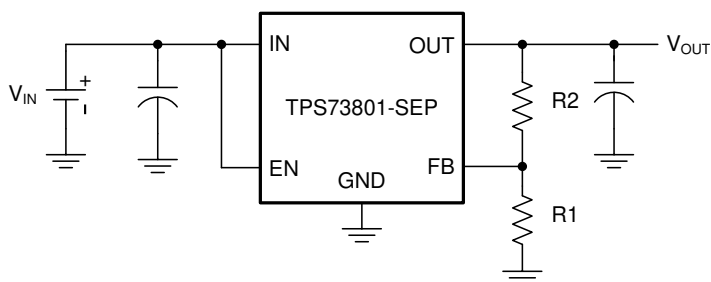


## TPS73801-SEP 1A 采用增强型航天塑料的低噪声快速瞬态响应低压降稳压器

### 1 特性

- VID V62/18616
- 耐辐射
  - SEL、SEB 和 SEGR 对于 LET 的抗扰度高达 43MeV-cm<sup>2</sup>/mg
  - SET 和 SEFI 的 LET 特征值高达 43MeV-cm<sup>2</sup>/mg
  - 每个晶圆批次的保障 TID 高达 20krad(Si)
  - TID 特征值高达 50krad(Si)
- 增强型航天塑料
  - Au 键合线和 NiPdAu 铅涂层
  - 采用增强型塑封实现低释气
  - 制造、组装和测试一体化基地
  - 延长了产品生命周期
  - 延长了产品变更通知周期
  - 产品可追溯性
- 针对快速瞬态响应进行了优化
- 输出电流：1A
- 压降电压：300mV
- 低噪声：45 μV<sub>RMS</sub> (10Hz 至 100kHz)
- 1mA 静态电流
- 无需保护二极管
- 压降中的受控静态电流
- 可调节输出电压：1.21V 至 20V
- 关断模式下静态电流小于 1μA
- 与 10μF 输出电容器搭配使用时可保持稳定
- 与陶瓷电容器搭配使用时可保持稳定
- 反向电池保护
- 无反向电流
- 热限制



简化版原理图

### 2 应用

- 支持近地轨道 (LEO) 航天应用
- 用于射频、VCO、接收器和放大器的耐辐射低噪声线性稳压器电源
- 洁净模拟电源要求
- 航天卫星有效载荷
- 命令和数据处理 (C&DH)
- 光学成像有效载荷
- 雷达成像有效载荷
- 卫星电力系统 (EPS)

### 3 说明

TPS73801-SEP 是一款针对快速瞬态响应进行了优化的低压降 (LDO) 稳压器。该器件可提高 1A 的输出电流 (压降为 300mV)。工作静态电流为 1mA，在关断时下降至小于 1μA。与许多其他稳压器相比，静态电流受到很好的控制，在压降时不上升。除了快速瞬态响应，TPS73801-SEP 稳压器还有很低的输出噪声，因此非常适合灵敏射频电源应用。

输出电压范围是 1.21V 至 20V，与低至 10μF 的输出电容器搭配使用时可保持稳定。使用小型陶瓷电容器可无需额外的 ESR。内部保护电路包括反向电池保护、电流限制、热限制和反向电流保护。TPS73801-SEP 稳压器可采用 6 引脚 TO-223 (DCQ) 封装，提供可调的 1.21V 基准电压。

#### 器件信息

器件型号 <sup>(1)</sup>	等级	封装
TPS73801MDCQTPSEP	20krad(Si) RLAT	SOT-223 (6) 6.55mm × 7.26mm 质量 = 119.8mg <sup>(2)</sup>
TPS73801MDCQPSEP		

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
- (2) 质量误差在 ±10% 以内。



## Table of Contents

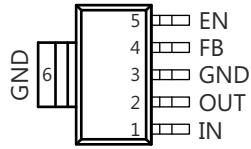
<b>1 特性</b> .....	1	<b>8 Application and Implementation</b> .....	14
<b>2 应用</b> .....	1	8.1 Application Information.....	14
<b>3 说明</b> .....	1	8.2 Typical Application.....	14
<b>4 Revision History</b> .....	2	<b>9 Power Supply Recommendations</b> .....	17
<b>5 Pin Configuration and Functions</b> .....	3	<b>10 Layout</b> .....	18
<b>6 Specifications</b> .....	4	10.1 Layout Guidelines.....	18
6.1 Absolute Maximum Ratings.....	4	10.2 Layout Example.....	18
6.2 ESD Ratings.....	4	10.3 Thermal Considerations.....	18
6.3 Recommended Operating Conditions.....	4	<b>11 Device and Documentation Support</b> .....	20
6.4 Thermal Information.....	4	11.1 Receiving Notification of Documentation Updates..	20
6.5 Electrical Characteristics.....	5	11.2 支持资源.....	20
6.6 Typical Characteristics.....	7	11.3 Trademarks.....	20
<b>7 Detailed Description</b> .....	11	11.4 Electrostatic Discharge Caution.....	20
7.1 Overview.....	11	11.5 Glossary.....	20
7.2 Functional Block Diagram.....	11	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	21
7.3 Feature Description.....	11		
7.4 Device Functional Modes.....	13		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2018) to Revision A (May 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 更新了 <i>特性</i> 部分中的耐辐射和增强型航天塑料要点.....	1
• 更新了 <i>应用</i> 部分.....	1
• 向“器件信息”表添加了器件质量和尺寸.....	1

## 5 Pin Configuration and Functions



**图 5-1. DCQ Package  
SOT-223  
Top View**

**表 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	—	Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 $\mu\text{F}$ to 10 $\mu\text{F}$ is sufficient. The TPS73801-SEP regulators are designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
2	OUT	—	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10 $\mu\text{F}$ is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients.
3	GND	—	Ground.
4	FB	I	Feedback. This is the input to the error amplifier. This pin is internally clamped to $\pm 7$ V. It has a bias current of 3 $\mu\text{A}$ that flows into the pin. The FB pin voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 V to 20 V.
5	EN	I	Enable. The EN pin is used to put the TPS73801-SEP regulators into a low-power shutdown state. The output is off when the EN pin is pulled low. The EN pin can be driven either by 5-V logic or open-collector gate, normally several microamperes, and the EN pin current, typically 3 $\mu\text{A}$ . If unused, the EN pin must be connected to the IN pin. The device is in the low-power shutdown state if the EN pin is not connected.
6	GND	—	Ground.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	IN	- 20	20	V
	OUT	- 20	20	
	Input-to-output differential <sup>(2)</sup>	- 20	20	
	FB	- 7	7	
	EN	- 20	20	
t <sub>short</sub>	Output short-circuit duration	Indefinite		
T <sub>J</sub>	Operating virtual-junction temperature	- 55	150	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT cannot exceed ±20 V.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		V
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	V <sub>OUT</sub> + V <sub>D0</sub>	20	V
V <sub>IH</sub>	EN high-level input voltage	2	20	V
V <sub>IL</sub>	EN low-level input voltage		0.25	V
T <sub>J</sub>	Recommended operating junction temperature	- 55	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS73801-SEP	UNIT
		DCQ (SOT-223)	
		6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	50.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	31.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	5.1	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over operating temperature range  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_J$	MIN	TYP <sup>(9)</sup>	MAX	UNIT
$V_{IN}$	Input voltage <sup>(1) (2)</sup>		$25^\circ\text{C}$	2.2	1.9	20	V
$V_{FB}$	FB pin voltage <sup>(1) (3)</sup>	$V_{IN} = 2.21\text{ V}$ , $I_{LOAD} = 1\text{ mA}$	$25^\circ\text{C}$	1.192	1.21	1.228	V
		$V_{IN} = 2.5\text{ V}$ to $20\text{ V}$ , $I_{LOAD} = 1\text{ mA}$ to $1\text{ A}$	Full range	1.174	1.21	1.246	
	Line regulation <sup>(1)</sup>	$\Delta V_{IN} = 2.21\text{ V}$ to $20\text{ V}$ , $I_{LOAD} = 1\text{ mA}$	Full range		1.5	5	mV
	Load regulation <sup>(1)</sup>	$V_{IN} = 2.5\text{ V}$ , $\Delta I_{LOAD} = 1\text{ mA}$ to $1\text{ A}$	$25^\circ\text{C}$		2	8	mV
			Full range			18	
$V_{DO}$	Dropout voltage <sup>(2) (5) (4)</sup> $V_{IN} = V_{OUT(NOMINAL)}$	$I_{LOAD} = 1\text{ mA}$	$25^\circ\text{C}$		0.02	0.06	V
			Full range			0.10	
		$I_{LOAD} = 100\text{ mA}$	$25^\circ\text{C}$		0.1	0.17	
			Full range			0.22	
		$I_{LOAD} = 500\text{ mA}$	$25^\circ\text{C}$		0.19	0.27	
			Full range			0.35	
$I_{LOAD} = 1\text{ A}$	$25^\circ\text{C}$		0.24	0.30			
	Full range			0.40			
$I_{GND}$	GND pin current <sup>(4) (6)</sup> $V_{IN} = V_{OUT(NOMINAL)} + 1$	$I_{LOAD} = 0\text{ mA}$	Full range		1	1.5	mA
		$I_{LOAD} = 1\text{ mA}$	Full range		1.1	1.6	
		$I_{LOAD} = 100\text{ mA}$	Full range		3.8	5.5	
		$I_{LOAD} = 500\text{ mA}$	Full range		15	25	
		$I_{LOAD} = 1\text{ A}$	Full range		35	80	
$V_N$	Output voltage noise	$C_{OUT} = 10\text{ }\mu\text{F}$ , $I_{LOAD} = 1\text{ A}$ , $B_W = 10\text{ Hz}$ to $100\text{ kHz}$	$25^\circ\text{C}$		45		$\mu\text{V}_{RMS}$
$I_{FB}$	FB pin bias current <sup>(1) (7)</sup>		$25^\circ\text{C}$		3	10	$\mu\text{A}$
$V_{EN}$	Shutdown threshold	$V_{OUT} = \text{OFF}$ to $\text{ON}$	Full range		0.9	2	V
		$V_{OUT} = \text{ON}$ to $\text{OFF}$	Full range	0.15	0.75		
$I_{EN}$	$\overline{\text{EN}}$ pin current	$V_{EN} = 0\text{ V}$	$25^\circ\text{C}$		0.01	1	$\mu\text{A}$
		$V_{EN} = 20\text{ V}$	$25^\circ\text{C}$		3	30	
	Quiescent current in shutdown	$V_{IN} = 6\text{ V}$ , $V_{EN} = 0\text{ V}$	$25^\circ\text{C}$		0.01	1	$\mu\text{A}$
PSRR	Ripple rejection <sup>(10)</sup>	$V_{IN} - V_{OUT} = 1.5\text{ V}$ (avg), $V_{RIPPLE} = 0.5\text{ V}_{P-P}$ , $f_{RIPPLE} = 120\text{ Hz}$ , $I_{LOAD} = 0.75\text{ A}$	$25^\circ\text{C}$	55	63		dB
$I_{CL}$	Current limit	$V_{IN} = 7\text{ V}$ , $V_{OUT} = 0\text{ V}$	$25^\circ\text{C}$		2		A
		$V_{IN} = V_{OUT(NOMINAL)} + 1$	Full range		1.6		
$I_{REV}$	Input reverse leakage current	$V_{IN} = -20\text{ V}$ , $V_{OUT} = 0\text{ V}$	Full range			1	mA
$I_{RO}$	Reverse output current <sup>(8)</sup>	$V_{OUT} = 1.21\text{ V}$ , $V_{IN} < 1.21\text{ V}$	$25^\circ\text{C}$		300	600	$\mu\text{A}$

- (1) The TPS73801-SEP is tested and specified for these conditions with the FB pin connected to the OUT pin.
- (2) Dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
- (3) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
- (4) To satisfy requirements for minimum input voltage, the TPS73801-SEP is tested and specified for these conditions with an external resistor divider (two 4.12-k $\Omega$  resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-mA DC load on the output.
- (5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to  $V_{IN} - V_{DROPOUT}$ .
- (6) GND pin current is tested with  $V_{IN} = (V_{OUT(NOMINAL)} + 1\text{ V})$  and a current source load. The GND pin current decreases at higher input voltages.
- (7) FB pin bias current flows into the FB pin.
- (8) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

- (9) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
- (10) Parameter is specified by characterization and is not tested in production.

## 6.6 Typical Characteristics

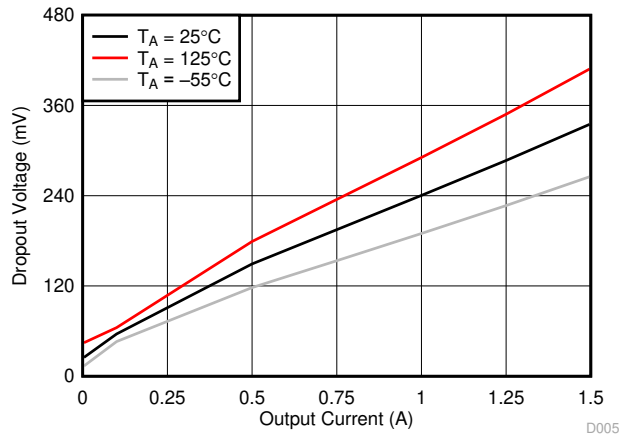


图 6-1. Dropout Voltage vs Output Current

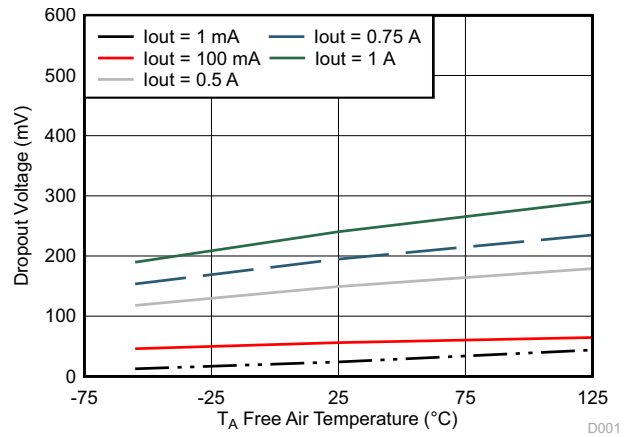


图 6-2. Dropout Voltage vs Temperature

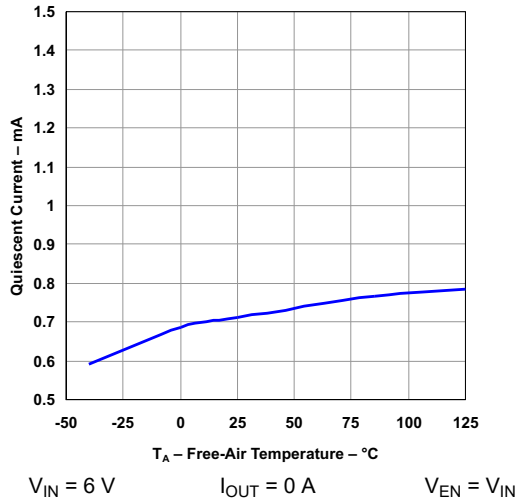


图 6-3. Quiescent Current vs Temperature

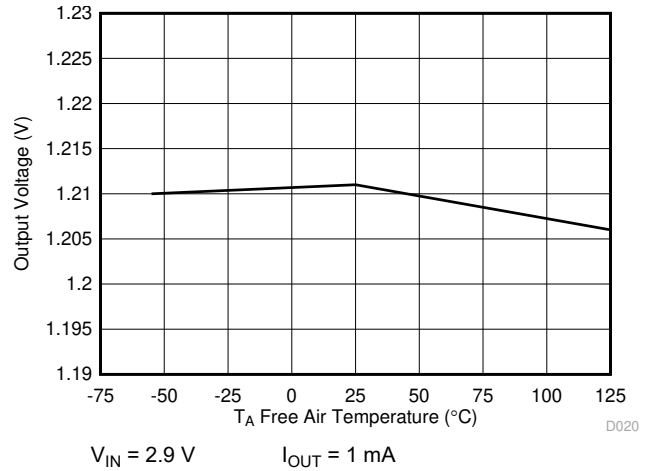


图 6-4. Output Voltage vs Temperature

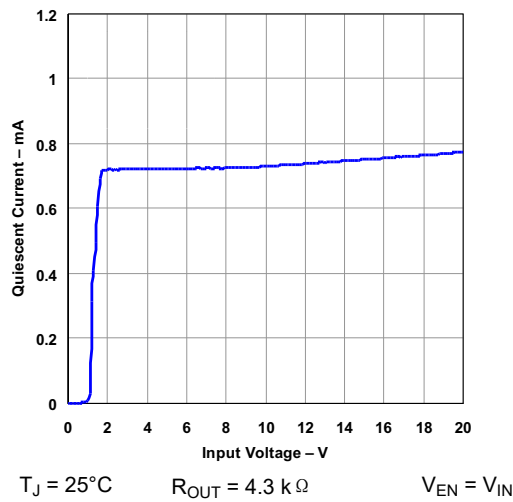


图 6-5. Quiescent Current vs Input Voltage

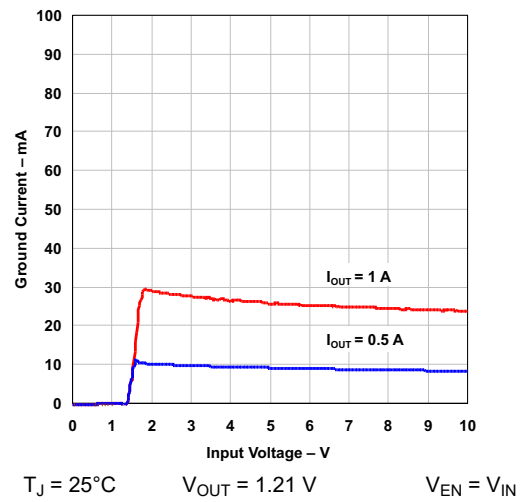
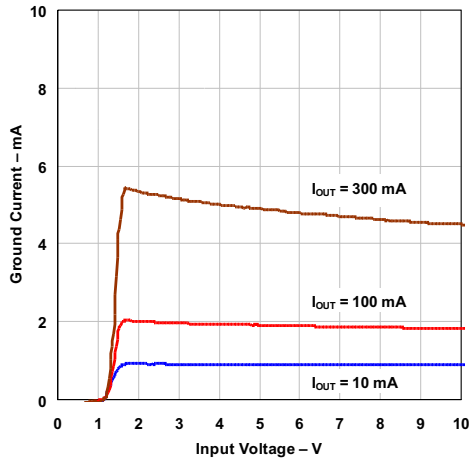


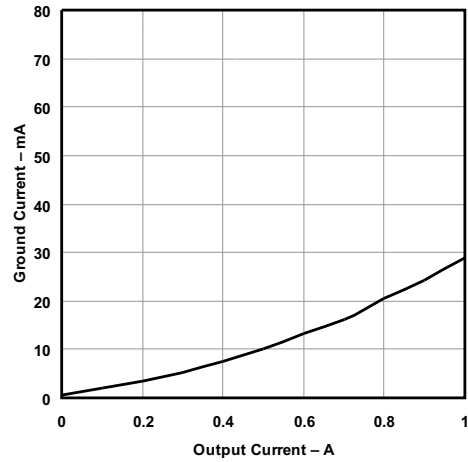
图 6-6. Ground Current vs Input Voltage

### 6.6 Typical Characteristics (continued)



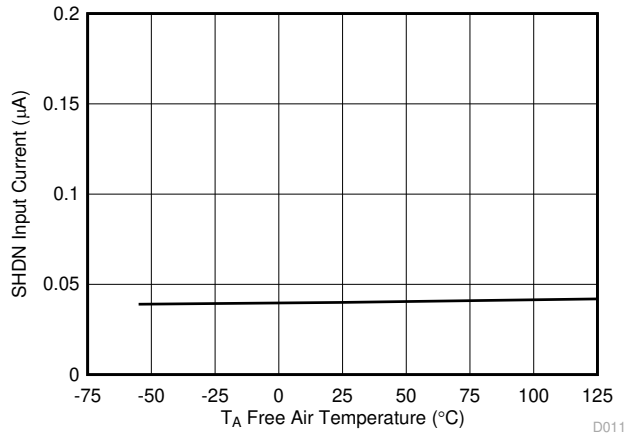
$T_J = 25^\circ\text{C}$      $V_{OUT} = 1.21\text{ V}$      $V_{EN} = V_{IN}$

图 6-7. Ground Current vs Input Voltage



$V_{IN} = V_{OUT(nom)} + 1$

图 6-8. Ground Current vs Output Current



$V_{EN} = 0\text{ V}$

图 6-9. EN Input Current vs Temperature

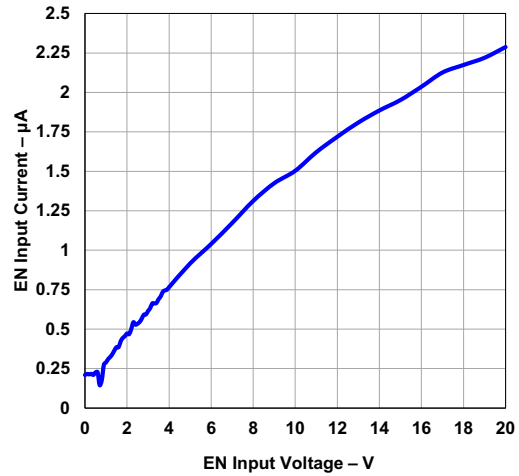
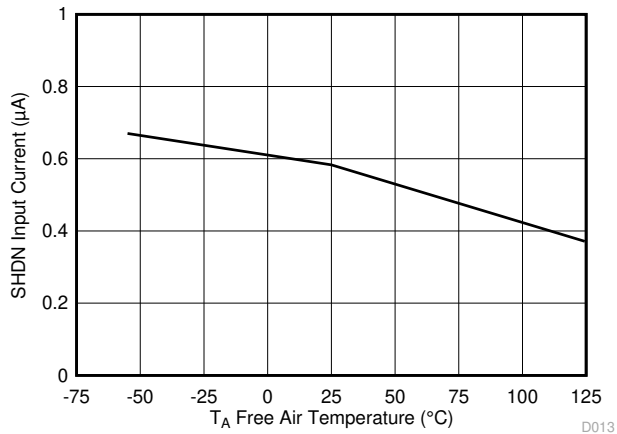
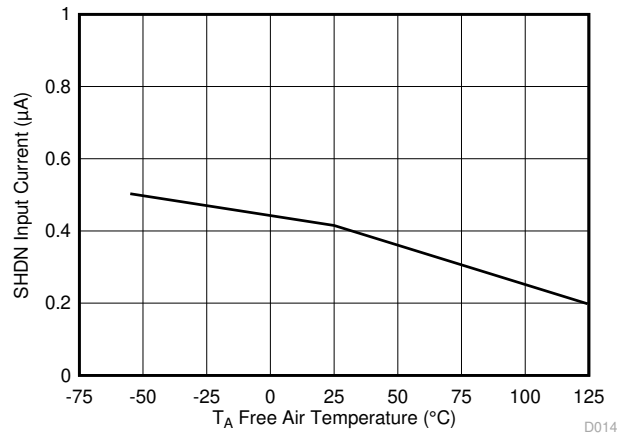


图 6-10. EN Input Current vs EN Input Voltage



$I_{OUT} = 1\text{ mA}$

图 6-11. EN Threshold (Off to On) vs Temperature



$I_{OUT} = 1\text{ mA}$

图 6-12. EN Threshold (On to Off) vs Temperature



### 6.6 Typical Characteristics (continued)

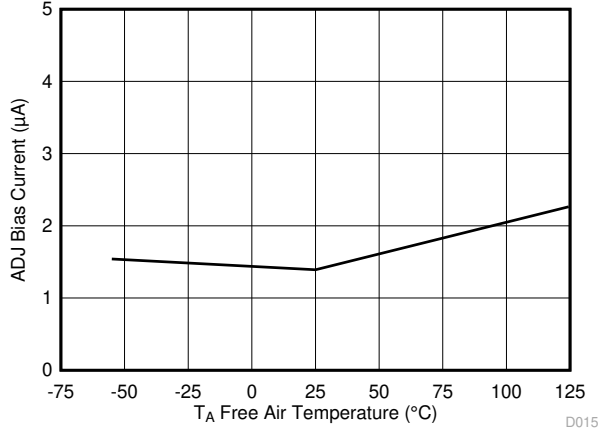
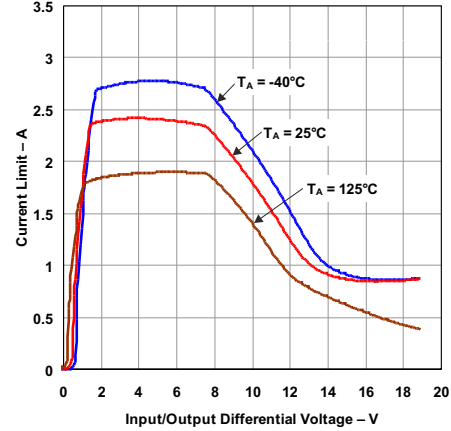
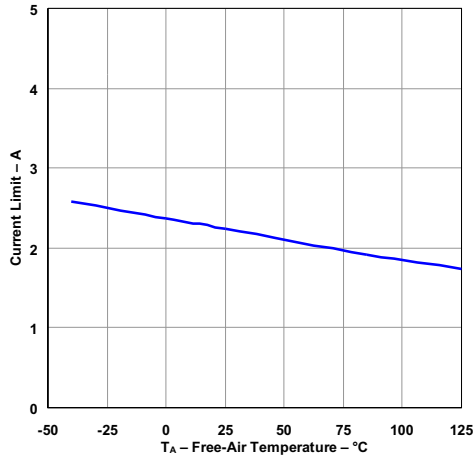


图 6-13. FB Bias Current vs Temperature



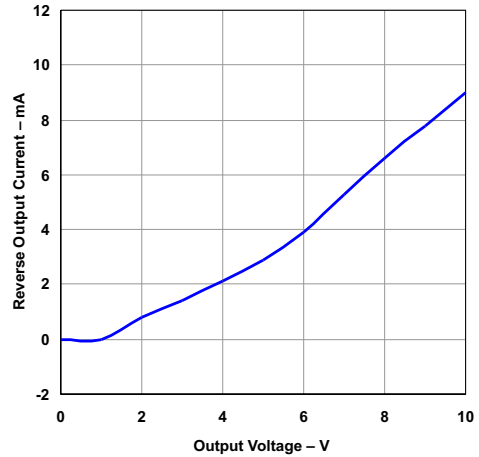
$\Delta V_{OUT} = 100 \text{ mV}$

图 6-14. Current Limit vs Input/Output Differential Voltage



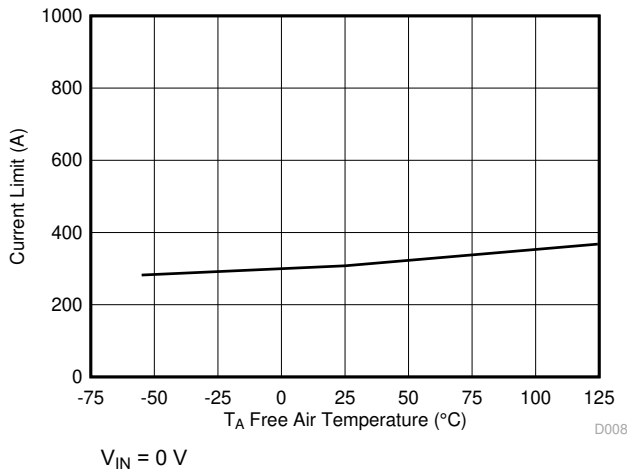
$V_{IN} = 7 \text{ V}$        $V_{OUT} = 0 \text{ V}$

图 6-15. Current Limit vs Temperature



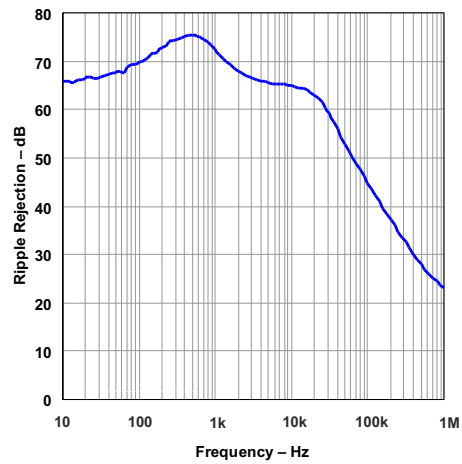
$T_J = 25^\circ\text{C}$        $V_{IN} = 0 \text{ V}$       Current flows into OUT pin

图 6-16. Reverse Output Current vs Output Voltage



$V_{IN} = 0 \text{ V}$

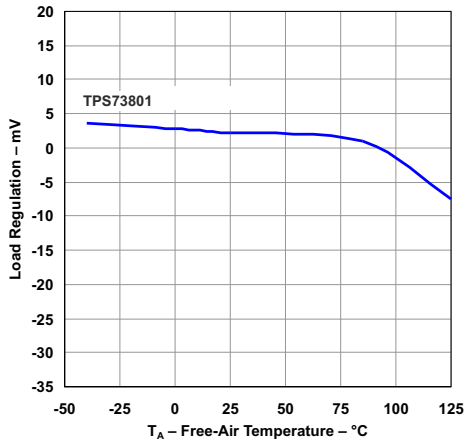
图 6-17. Reverse Output Current vs Temperature



$V_{IN} = 2.7 \text{ V}$        $V_{RIPPLE} = 0.05 V_{PP}$        $I_{OUT} = 750 \text{ mA}$   
 $C_{IN} = 0$        $C_{OUT} = 10 \mu\text{F (ceramic)}$        $T_A = 25^\circ\text{C}$

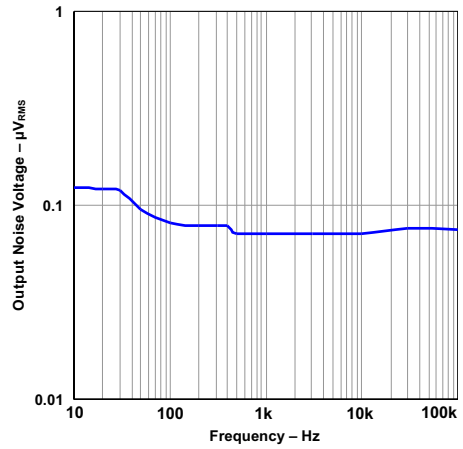
图 6-18. Ripple Rejection vs Frequency

### 6.6 Typical Characteristics (continued)



$I_{OUT} = 1\text{ A}$

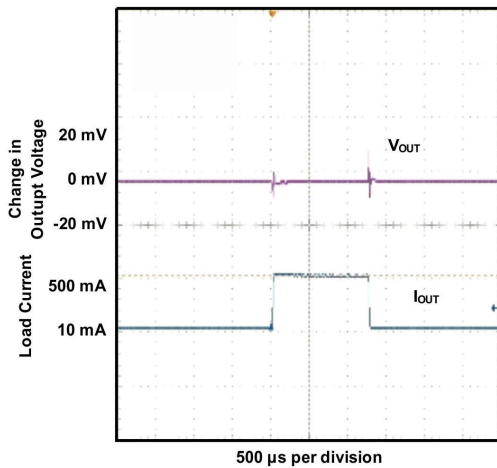
图 6-19. Load Regulation vs Temperature



$C_{OUT} = 10\ \mu\text{F}$  (ceramic)

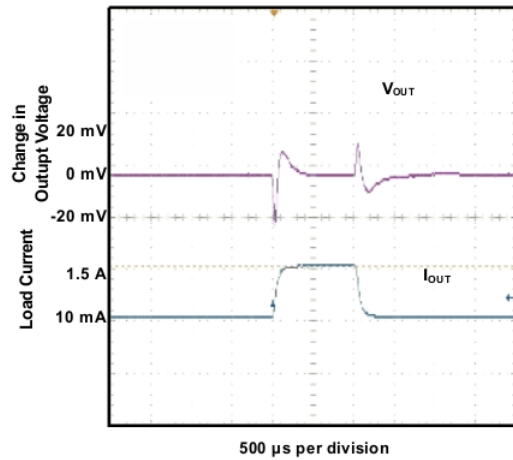
$I_{OUT} = 1\text{ A}$

图 6-20. Output Noise Voltage vs Frequency



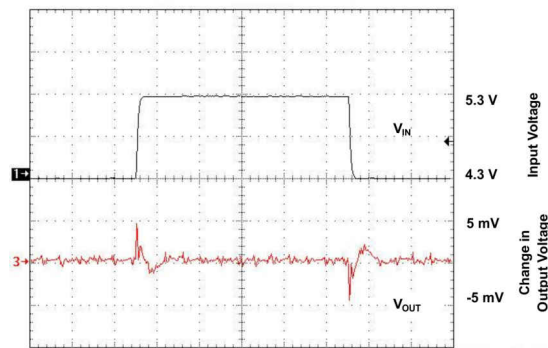
$V_{IN} = 4.3\text{ V}$     $C_{IN} = 10\ \mu\text{F}$     $C_{OUT} = 10\ \mu\text{F}$  (ceramic)

图 6-21. Load Transient Response



$V_{IN} = 4.3\text{ V}$     $C_{IN} = 10\ \mu\text{F}$     $C_{OUT} = 10\ \mu\text{F}$  (ceramic)

图 6-22. Max Load Transient Response



$I_{OUT} = 1.5\text{ A}$

$C_{IN} = 10\ \mu\text{F}$

$C_{OUT} = 10\ \mu\text{F}$  (ceramic)

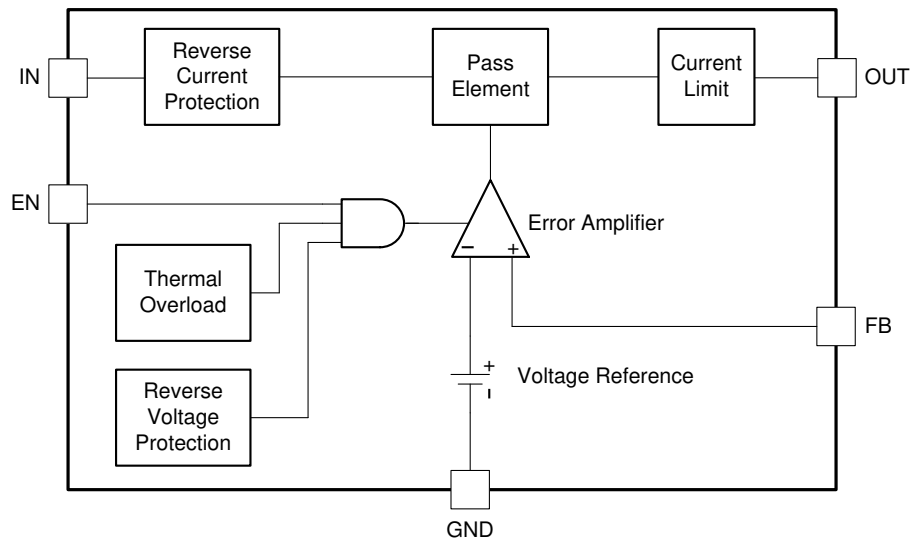
图 6-23. Line Transient Response

## 7 Detailed Description

### 7.1 Overview

The TPS73801-SEP is a 1-A LDO regulator optimized for fast transient response. The devices are capable of supplying 1 A at a dropout voltage of 300 mV. The low operating quiescent current (1 mA) drops to less than 1  $\mu$ A in shutdown. In addition to the low quiescent current, the TPS73801-SEP regulators incorporate several protection features which make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the input is pulled to ground, the TPS73801-SEP acts as if it has a diode in series with its output and prevents reverse current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20 V and still allow the device to start and operate.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Adjustable Operation

The TPS73801-SEP has an adjustable output voltage range of 1.21 V to 20 V. The output voltage is set by the ratio of two external resistors as shown in 图 7-1. The device maintains the voltage at the FB pin at 1.21 V referenced to ground. The current in R1 is then equal to  $(1.21 \text{ V} / R1)$ , and the current in R2 is the current in R1 plus the FB pin bias current. The FB pin bias current, 3  $\mu$ A at 25°C, flows through R2 into the FB pin. The output voltage can be calculated using the formula shown in 方程式 1. The value of R1 should be less than 4.17 k $\Omega$  to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown the output is turned off, and the divider current is zero.

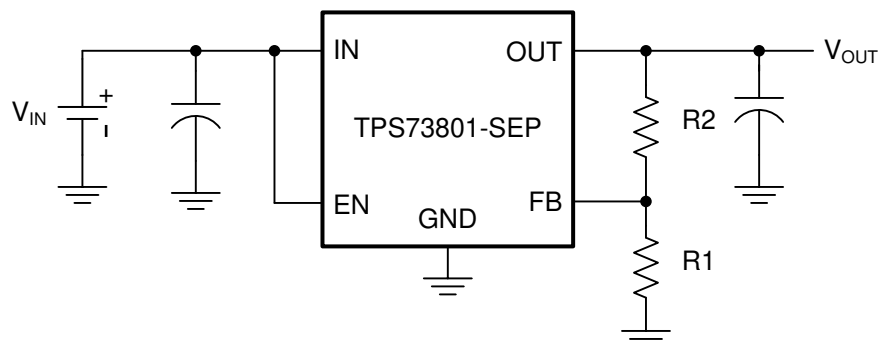


图 7-1. Adjustable Operation

The output voltage can be set using the following equations:

$$V_{OUT} = 1.21 V \left(1 + \frac{R_2}{R_1}\right) + I_{FB} \times R_2 \quad (1)$$

$$V_{FB} = 1.21 V \quad (2)$$

$$I_{FB} = 3 \mu A \text{ at } 25^\circ C \quad (3)$$

$$\text{Output Range} = 1.21 \text{ to } 20 V \quad (4)$$

### 7.3.2 Fixed Operation

The TPS73801-SEP can be used in a fixed voltage configuration. By connecting the FB pin to OUT, the TPS73801-SEP will regulate the output to 1.21 V. During fixed voltage operation, the FB pin can be used for a Kelvin connection if routed separately to the load. This allows the regulator to compensate for voltage drop across parasitic resistances ( $R_p$ ) between the output and the load. This becomes more crucial with higher load currents.

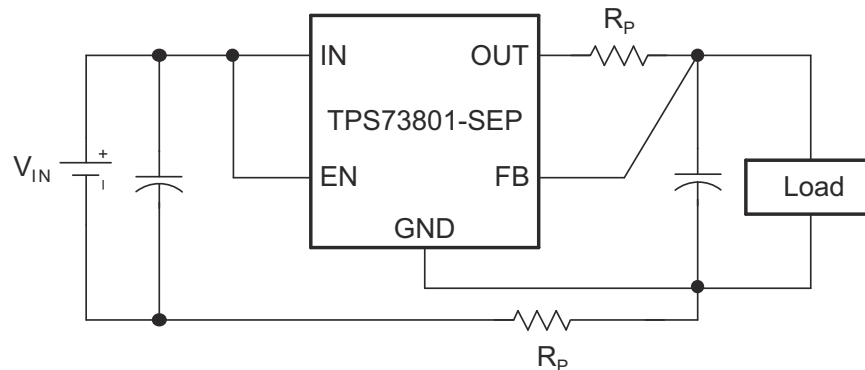


图 7-2. Kelvin Sense Connection

### 7.3.3 Overload Recovery

Like many IC power regulators, the TPS73801-SEP has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TPS73801-SEP.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

### 7.3.4 Output Voltage Noise

The TPS73801-SEP regulators have been designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically  $40 \text{ nV} / \sqrt{\text{Hz}}$  over this frequency bandwidth for the TPS73801-SEP. For higher output voltages (generated by using a resistor divider), the output voltage noise is gained up accordingly. This results in RMS noise over the 10-Hz to 100-kHz bandwidth of  $14 \mu\text{VRMS}$  for the TPS73801-SEP.

Higher values of output voltage noise may be measured when care is not exercised with regards to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TPS73801-SEP. Power supply ripple rejection must also be considered; the TPS73801-SEP regulators do not have unlimited power-supply rejection and pass a small portion of the input noise through to the output.

### 7.3.5 Protection Features

The TPS73801-SEP regulators incorporate several protection features that make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TPS73801-SEP can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. The output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the EN pin turns off the device and stops the output from sourcing the short-circuit current.

The FB pin can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the FB pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the FB pin is connected to a resistor divider that would pull the FB pin above its 7-V clamp voltage if the output is pulled high, the FB pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the FB pin to less than 5 mA when the FB pin is at 7 V. The 13-V difference between OUT and FB pins divided by the 5-mA maximum current into the FB pin yields a minimum top resistor value of 2.6 kΩ.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. When the IN pin of the TPS73801-SEP is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 µA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin has no effect on the reverse output current when the output is pulled above the input.

### 7.4 Device Functional Modes

See the device modes in [表 7-1](#).

**表 7-1. Device Modes**

EN	DEVICE STATE
H	Regulated voltage
L	Shutdown

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Output Capacitance and Transient Response

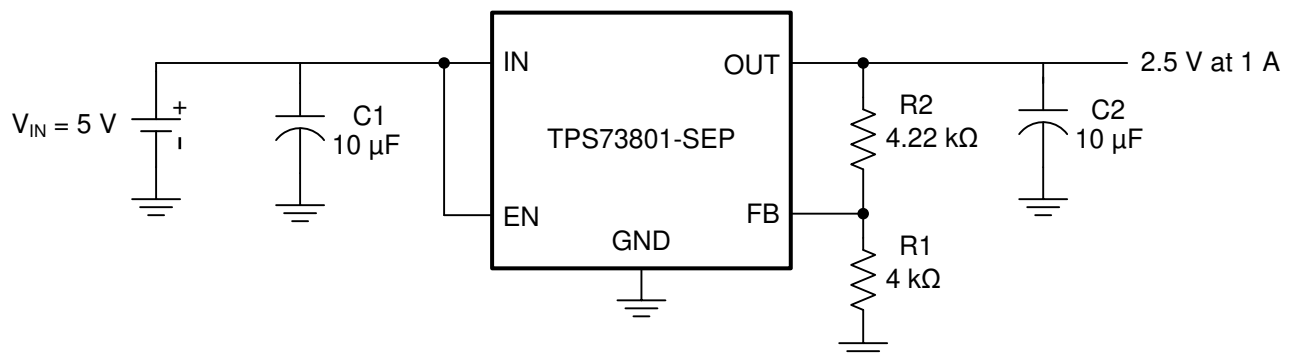
The TPS73801-SEP regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10  $\mu\text{F}$  with an ESR of 3  $\Omega$  or less is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS73801-SEP, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10- $\mu\text{F}$  Y5V capacitor can exhibit an effective value as low as 1  $\mu\text{F}$  to 2  $\mu\text{F}$  over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

### 8.2 Typical Application

This section will highlight some of the design considerations when implementing this device in various applications.



All capacitors are ceramic.

图 8-1. Adjustable Output Voltage Operation

## 8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage ( $V_{IN}$ )	5 V
Output voltage ( $V_{OUT}$ )	2.5 V
Output current ( $I_{OUT}$ )	0 to 1 A
Load regulation	1%

## 8.2.2 Detailed Design Procedure

The TPS73801-SEP has an adjustable output voltage range of 1.21 to 20 V. The output voltage is set by the ratio of two external resistors R1 and R2 as shown in [Adjustable Output Voltage Operation](#). The device maintains the voltage at the FB pin at 1.21 V referenced to ground. The current in R1 is then equal to  $(1.21 \text{ V} / R1)$ , and the current in R2 is the current in R1 plus the FB pin bias current. The FB pin bias current, 3  $\mu\text{A}$  at 25°C, flows through R2 into the FB pin. The output voltage can be calculated using [方程式 5](#).

$$V_{OUT} = 1.21 \text{ V} \left(1 + \frac{R2}{R1}\right) + I_{FB} \times R2 \quad (5)$$

The value of R1 should be less than 4.17 k $\Omega$  to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown the output is turned off, and the divider current is zero. For an output voltage of 2.50 V, R1 will be set to 4.0 k $\Omega$ . R2 is then found to be 4.22 k $\Omega$  using the equation above.

$$V_{OUT} = 1.21 \text{ V} \left(1 + \frac{4.22 \text{ k}\Omega}{4.0 \text{ k}\Omega}\right) + 3 \mu\text{A} \times 4.22 \text{ k}\Omega \quad (6)$$

$$V_{OUT} = 2.50 \text{ V} \quad (7)$$

The adjustable device is tested and specified with the FB pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V:  $V_{OUT} / 1.21 \text{ V}$ . For example, load regulation for an output current change of 1 mA to 1.5 A is - 2 mV (typ) at  $V_{OUT} = 1.21 \text{ V}$ . At  $V_{OUT} = 2.50 \text{ V}$ , the typical load regulation is:

$$(2.50 \text{ V} / 1.21 \text{ V})(- 2 \text{ mV}) = - 4.13 \text{ mV} \quad (8)$$

图 8-2 shows the actual change in output is approximately 3 mV for a 1-A load step. The maximum load regulation at 25°C is - 8 mV. At  $V_{OUT} = 2.50 \text{ V}$ , the maximum load regulation is:

$$(2.50 \text{ V} / 1.21 \text{ V})(- 8 \text{ mV}) = - 16.53 \text{ mV} \quad (9)$$

Since 16.53 mV is 0.7% of the 2.5-V output voltage, the load regulation will meet the design requirements.

### 8.2.3 Application Curve

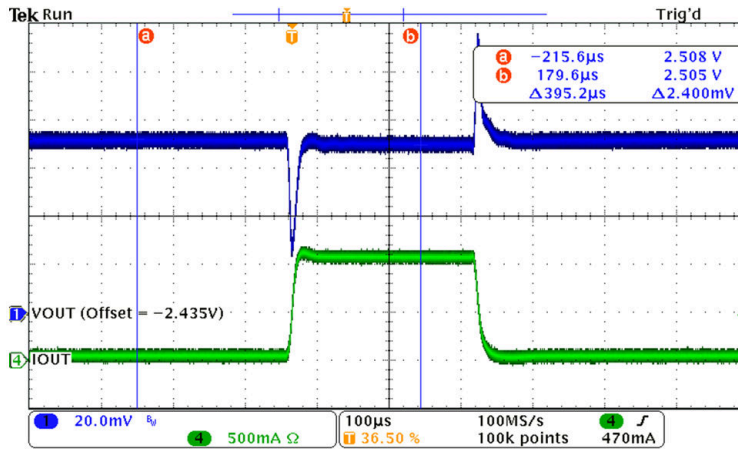


图 8-2. 1-A Load Transient Response



## 9 Power Supply Recommendations

The device is designed to operate with an input voltage supply up to 20 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

## 10 Layout

### 10.1 Layout Guidelines

1. For best performance, all traces should be as short as possible.
2. Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
3. A minimum output capacitor of 10  $\mu\text{F}$  with an ESR of 3  $\Omega$  or less is recommended to prevent oscillations. X5R and X7R dielectrics are preferred.
4. Place the output capacitor as close as possible to the OUT pin of the device.
5. The tab of the DCQ package should be connected to ground.

### 10.2 Layout Example

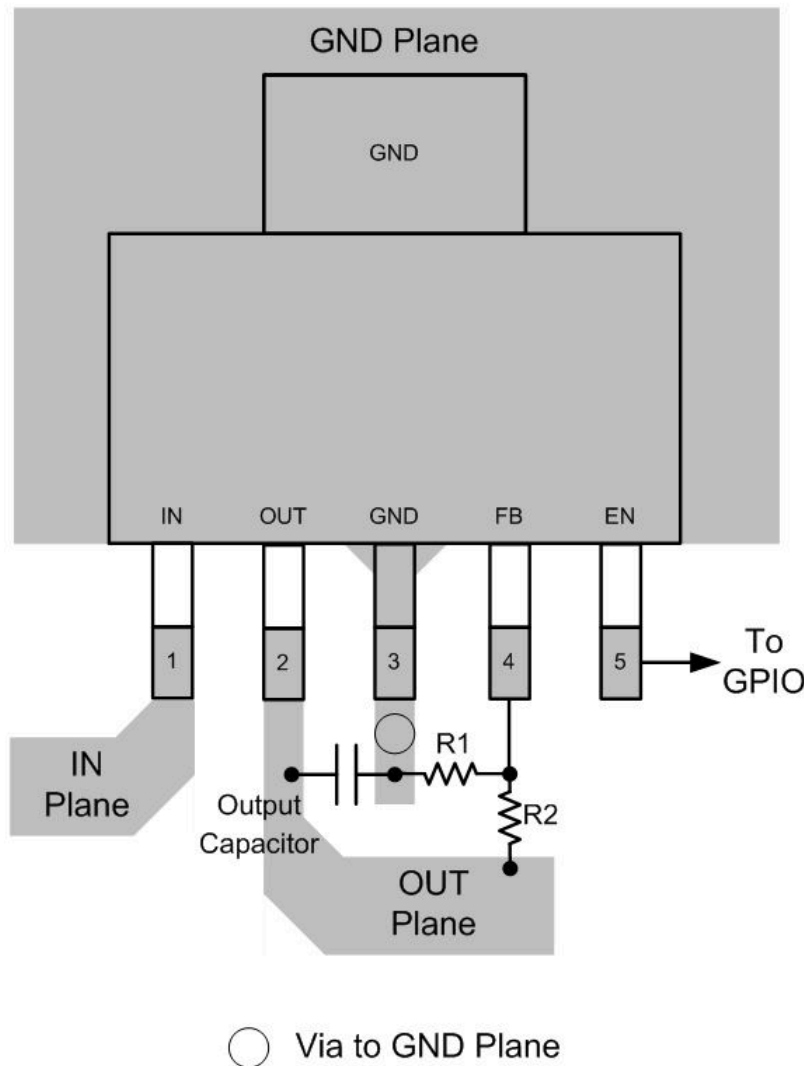


图 10-1. SOT-223 Layout Example (DCQ)

### 10.3 Thermal Considerations

The power handling capability of the device is limited by the recommended maximum operating junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential:  $I_{\text{OUT}} (V_{\text{IN}} - V_{\text{OUT}})$
2. GND pin current multiplied by the input voltage:  $I_{\text{GND}} \times V_{\text{IN}}$

The GND pin current can be found using the GND Pin Current graphs in [节 6.6](#) . Power dissipation is equal to the sum of the two components listed above.

The TPS73801-SEP series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the recommended maximum operating junction temperature is 125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

### 10.3.1 Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 V to 6 V, an output current range of 0 mA to 500 mA, and a maximum ambient temperature of 50°C, what is the operating junction temperature?

The power dissipated by the device is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)}) \quad (10)$$

where

- $I_{OUT(MAX)} = 500 \text{ mA}$
- $V_{IN(MAX)} = 6 \text{ V}$
- $I_{GND}$  at ( $I_{OUT} = 500 \text{ mA}$ ,  $V_{IN} = 6 \text{ V}$ ) = 10 mA

So,

$$P = 500 \text{ mA} \times (6 \text{ V} - 3.3 \text{ V}) + 10 \text{ mA} \times 6 \text{ V} = 1.41 \text{ W} \quad (11)$$

The thermal resistance of the DCQ package is 50.5°C/W. So the junction temperature rise above ambient is approximately equal to:

$$1.41 \text{ W} \times 50.5^\circ\text{C/W} = 71.2^\circ\text{C} \quad (12)$$

The junction temperature rise can then be added to the maximum ambient temperature to find the operating junction temperature ( $T_J$ ):

$$T_J = 50^\circ\text{C} + 71.2^\circ\text{C} = 121.2^\circ\text{C} \quad (13)$$

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要声明和免责声明

TI 提供技术和可靠性数据 (包括数据表)、设计资源 (包括参考设计)、应用或其他设计建议、网络工具、安全信息和其他资源, 不保证没有瑕疵且不做任何明示或暗示的担保, 包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任: (1) 针对您的应用选择合适的 TI 产品, (2) 设计、验证并测试您的应用, (3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更, 恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务, TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com/legal/termsofsale.html>) 或 [ti.com](https://www.ti.com) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, 德州仪器 (TI) 公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73801MDCQPSEP	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP	<a href="#">Samples</a>
TPS73801MDCQTPSEP	ACTIVE	SOT-223	DCQ	6	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP	<a href="#">Samples</a>
V62/18616-01XE	ACTIVE	SOT-223	DCQ	6	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP	<a href="#">Samples</a>
V62/18616-01XE-T	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	73801-SP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73801MDCQTPSEP	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

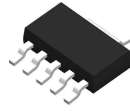
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73801MDCQTPSEP	SOT-223	DCQ	6	250	213.0	191.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS73801MDCQPSEP	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
V62/18616-01XE-T	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68

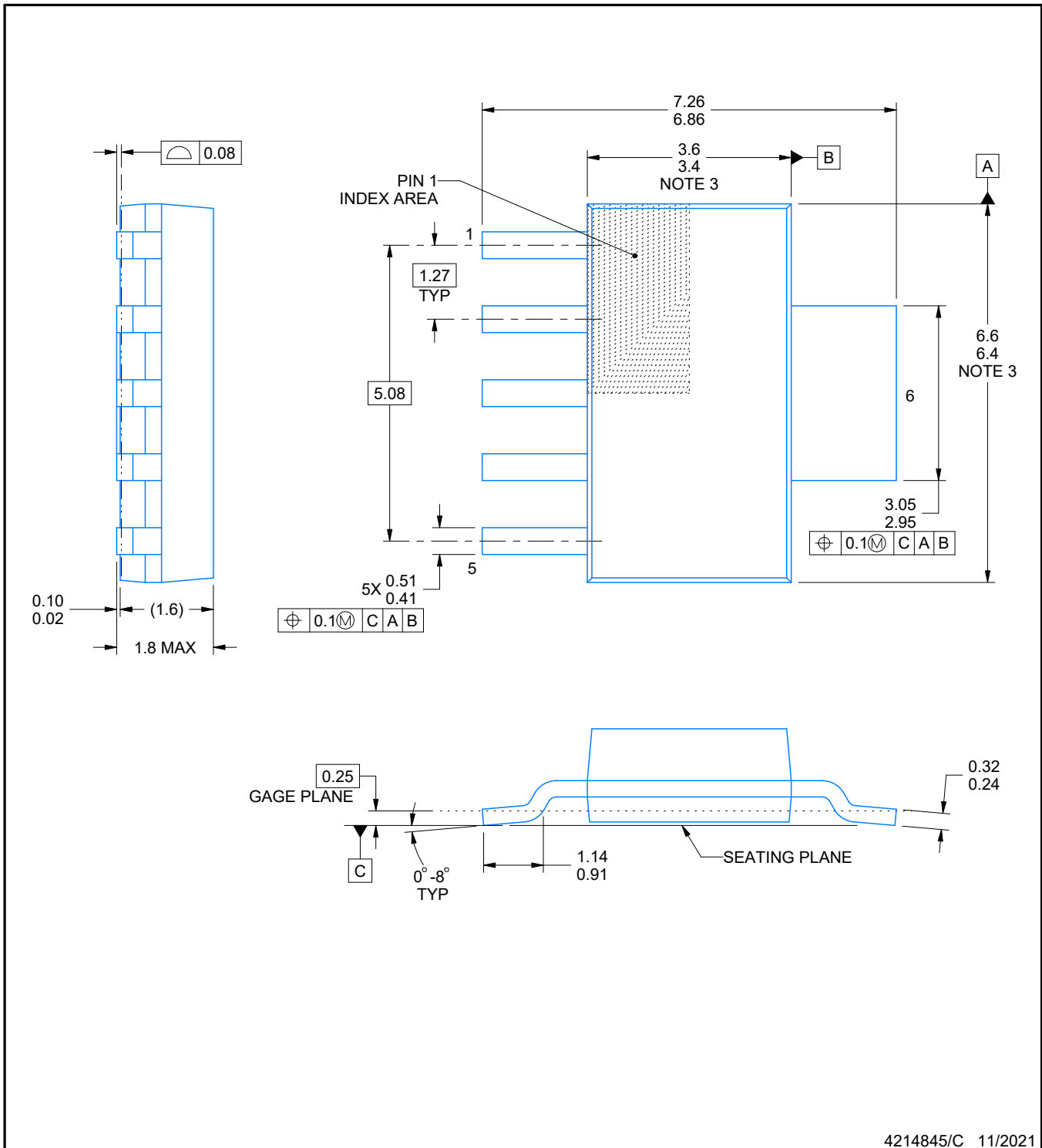
# DCQ0006A



# PACKAGE OUTLINE

## SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



4214845/C 11/2021

**NOTES:**

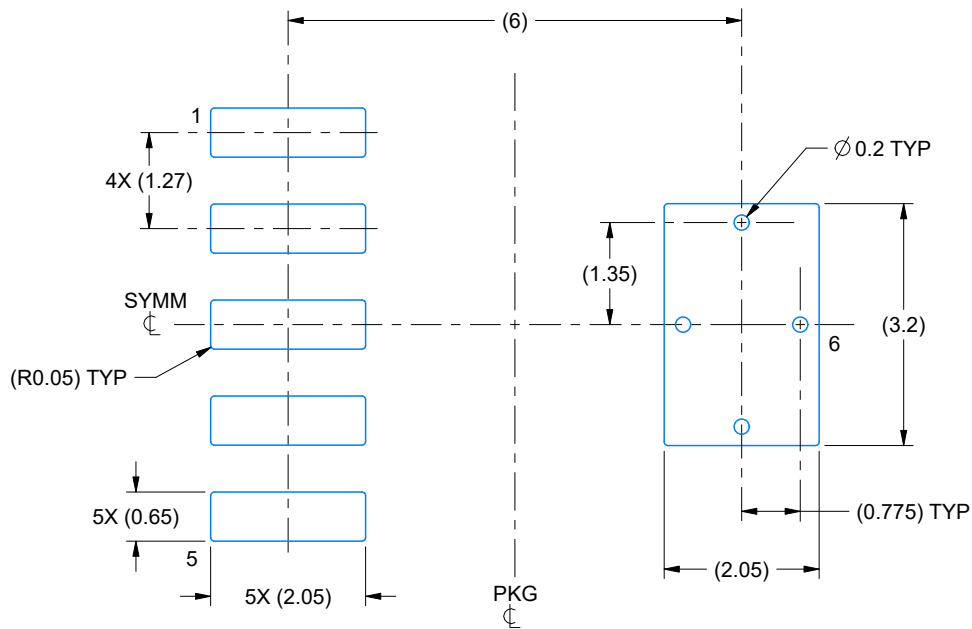
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

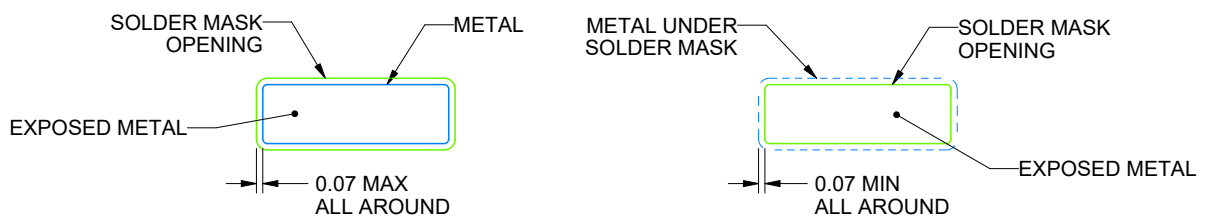
DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司